MASTER

Design of a multi-bit Sigma Delta analog to digital convertor with variable resolution

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Design of a multi-bit Sigma Delta analog to digital converter with variable resolution.

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Abstract

This report contains a feasibility study of a multi-bit sigma-delta A/D-converter with variable resolution.

The use of noise shaping techniques seems to be promising for our study, because of the fact that with a single type of noise-shaping converter, several signals can be determined of which the resolution is dependent on the chosen bandwidth. A measurement application is investigated. As a first research topic, multi-bit sigma-delta converters are analyzed. Very important are also the decimating filters behind the noise shaper. In this report we have used special monotonic half-band filters which have the advantage of an increasing passband ripple at increasing passband width.

A 7-bit sigma-delta converter has been designed with an appropriate filter structure to meet the preliminary specifications. Simulations of the design have proved to be satisfactory also after using finite word length in the filters.

A first estimation of the chip area of the filter structure has been made which indicates that the size will be large. Using an improved smaller feature size process will make the chip realizable.

Finally further points of investigation are indicated.

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Preface

First, I want to express my thanks to prof.dr.ir. R.J. van de Plassche and ir. P.A.C.M. Nuijten for giving me the opportunity to do my graduation work at Philips Research Laboratories. I appreciate the support and coaching by them very much. Also many thanks to the members of the group Wouda. Without them the completion of this thesis would have been more difficult and less pleasant.

Gerard J.H.M. van Hal
Eindhoven,
Oct 1991.

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Chapter 1

Introduction

This master thesis contains the feasibility study for a multi-bit sigma-delta Analog-to-Digital converter. The study is intended to be used within the Philips product division Test & Measurements of Almelo and performed at Philips Research Laboratories in Eindhoven. The goal is to find out whether it is possible to design an Analog-to-Digital converter with variable resolution which can work at different signal band widths. Special attention had to be paid to the relation between signal bandwidth and resolution. The product division is very interested in using the sigma-delta A/D-converter or the bitstream converter principle. Because of the fact that with a single type of noise-shaping converter, several signals can be determined of which the resolution is dependent on the chosen bandwidth.

This report first contains an overview of the application area of the design followed by a specific product in which the converter would be used. The second chapter describes the basic theoretical analog-to-digital converter principles. Then the theory is focused on sigma-delta conversion in chapter 3.

The first design is described in chapter 4 followed by the problem of filtering and downsampling. In this chapter the designed filter structure and filter sections are given. Also the use of half-band filters is put forward.

Chapter 6 will describe problems with finite word length in the filters and will provide a first estimation of the die size of the designed filters. This die size estimation has first been done for the C3DM process (1.5 μm) and the C200 process (1.0 μm). The last chapter contains conclusions and some recommendations for further investigation.

1.1 Application area of the converter

Within Test & Measurements, research is done to a new test system for all car electronics. This system contains a multi-function card which measures or generates several electrical signals. It also contains a digital processor for signal adaptation. On this multi-function card both analog-to-digital and digital-to-analog conversion has to take place. Currently several A/D and D/A converters are incorporated in order to get a flexible measurement system. The study described in this report has been restricted to the analog-to-digital conversion part.

If the study is successful other application fields are also interesting. Wherever

variable resolution is requested the converter can be applied, which will be mainly in measurement devices. This is also a necessity because the development of a complete new converter only for a multi-function card is not economical feasible.

In a first orientation discussion the product division, Test and Measurements (T & M), postulated the following bands of interrest and resolutions :

- Bandwidth 5 MHz
  Resolution 8 bit

- Bandwidth 1 MHz
  Resolution 10 - 12 bit

- Bandwidth 20 kHz
  Resolution 16 bit

Currently a specific converter is used for each frequency band which is a rather expensive solution.

1.2 Basic design of the multifunction card

The product division provides a basic scheme of the multi-function card in which the A/D- and D/A-converter has to be implemented (figure 1.1). The input and output filters are already specified. The digital signal processor, DSP 1, has to perform the operations between the I/O-bus and the serial link. The DSP also performs simple signal processing operations. Both the DAC and ADC have to operate on the I/O-bus.
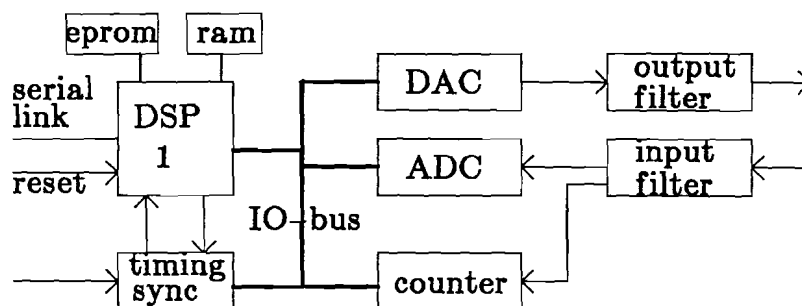
Figure 1.1: Basic scheme multi-function card.

According to this we have to implement the DAC and ADC as in figure 1.2. The DAC will normally need an oversampling filter in front of the sigma-delta modulator because of the relative slow speed of data at the input. Then the real conversion takes place and the analog bandwidth is limited using an analog low-pass filter to reduce noise

which has been shaped to higher frequencies by the sigma-delta modulator. In the ADC the (over)sampling is done in the sigma-delta modulator, then the signal is converted into a digital signal. Before downsampling, to receive uniform data for the I/O-bus, digital low-pass filtering has to be performed to avoid folding back unwanted signals into the signal band (see chapter 5).
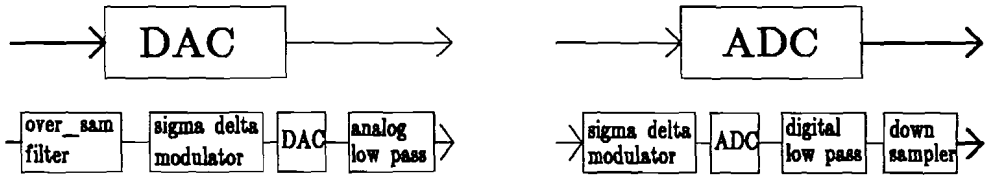
Figure 1.2: The DAC and ADC.

The product division indicates that anti-aliasing filters will be implemented in the input filters of figure 1.1 or will not be implemented. In this case the applicant has to avoid aliasing.

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Chapter 2

Basic A/D converter principles

2.1 Introduction

An analog-to-digital converter forms the bridge between the time-continuous signal and the time- and amplitude discrete signal or so called digital world.

In an A/D-converter two actions have to take place. First a signal has to be made time-discrete or sampled and further the signal must be made amplitude-discrete or quantized. When performing those two actions errors and distortion are introduced. Sampling of a signal or making it time-discrete, will introduce a repetition of the input signal spectrum around the sampling frequency and its multiples. This gives us the restriction of limiting the signal bandwidth to half the sampling frequency (Nyquist criterion). Otherwise a part of the repeated spectrum will fold back into the original signal band and cause so called aliasing. Limiting of the signal band has to take place before the analog-to-digital converter. For that purpose we have to use a time-continuous anti-aliasing filter in front of the converter.

Quantization of the amplitude of a signal causes errors because we only have a limited number of quantization levels. The error is often called quantization noise because it usually has a random character which is in accordance with a noise spectrum. The dynamic range of a converter is defined as the ratio of maximum input signal to the noise. Thus the dynamic range can be specified by signal-to-noise ratio in which the noise-bandwidth is equal to half the sampling frequency. The dynamic range depends on the number of quantization levels.

First we'll look at the quantization of the amplitude then we'll determine the basic S/N ratio and look at the influence of oversampling. Finally in this chapter, an overview of some realization possibilities is given, followed by some provisional conclusions.

2.2 Quantization

If we have an analog signal, the amplitude of the signal is quantized to a discrete level thus introducing an error. In figure 2.1 we see a number of quantization levels, the analog signal A will be quantized to the nearest level, A_{quant}. The decision levels are the dashed lines. Every signal value between two decision levels will be quantized to the

same quantization level.
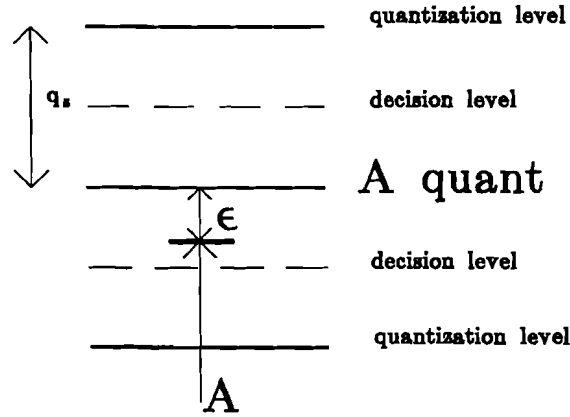
Figure 2.1: Signal quantization.

The distance between two quantization levels is q_s so when quantizing, the maximum error ε in amplitude level to a quantization level is $q_s/2$. If we now have a sufficient varying signal, we will receive a uniform error distribution over an interval of $-q_s/2$ and $+q_s/2$ around each quantization level. The average error in this distribution is zero. We now can calculate the mean squared value of ε.

$$E(\varepsilon^2) = \frac{1}{q_s} \int_{-\frac{q_s}{2}}^{+\frac{q_s}{2}} \varepsilon^2 \, d\varepsilon \qquad (2.1)$$

Solving this equation and expressing the statical expectation $E(\varepsilon^2)$ as quantization error voltage ε_{qns}^2 results in :

$$\varepsilon_{qns}^2 = \frac{1}{12} q_s^2 \qquad (2.2)$$

2.3 S/N ratio

After determining the noise density we now want to estimate the dynamic range. The dynamic range is specified as the maximum input signal level to the noise measured over the baseband. We have to define the signal value. We will use an input sine with peak to peak amplitude given by equation 2.3

$$A_{pp} = M \times q_s \qquad (2.3)$$

Where M is the number of quantization intervals. This gives a rms value A_{rms} of A_{pp} :

$$A_{rms} = \frac{M \times q_s}{2\sqrt{2}} \qquad (2.4)$$

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If we assume that the amplitude of the input sine covers the complete quantization interval than follows

$$M = 2^n - 1 \tag{2.5}$$

Where n is the number of bits. The signal-to-noise ratio is given by combining equation 2.2 and the square root of equation 2.4

$$S/N_{nyq} = (2^n - 1)\sqrt{1.5} \tag{2.6}$$

When the number of quantization intervals is large ($n \gg 1$) this equation simplifies to

$$S/N_{nyq} = 2^n \sqrt{1.5} \tag{2.7}$$

or

$$S/N_{nyq} = n \times 6.02 + 1.76 \text{ dB} \tag{2.8}$$

This is the basic S/N ratio of converters. The dynamic range is defined as signal-to-noise ratio measured over half of the bandwidth to the sampling frequency.

2.4 Oversampling

With the given signal-to-noise ratio of section 2.3 we will now look at systems with a sample frequency larger than two times the signal bandwidth. We call this an oversampled system. Within this whole report the definition of oversampling ratio or oversampling factor is :

$$\text{oversampling factor} = \frac{f_s}{2f_b} \tag{2.9}$$

This has been based on the number of times the sample frequency is higher then in a Nyquist converter, in which $f_s = 2f_b$.

Figure 2.2 shows the noise reduction of a four times oversampled converter compared to a Nyquist converter. The total noise power is equal in both situations but when performing four times oversampling the noise density is reduced, because it is spread over a four times larger band than the original Nyquist converter.

When using the noise definition of section 2.2, the assumption that the noise is white, gives that its power density is uniformly distributed until $\frac{f_s}{2}$. We have to normalize it per unit bandwidth which results in :

$$\varepsilon_{qn}^2(f) = \frac{1}{12} \frac{q_s^2}{\frac{f_s}{2}} \tag{2.10}$$

This gives a S/N ratio of

$$S/N(f) = 2^n \sqrt{1.5} \sqrt{\frac{f_s}{2}} \tag{2.11}$$
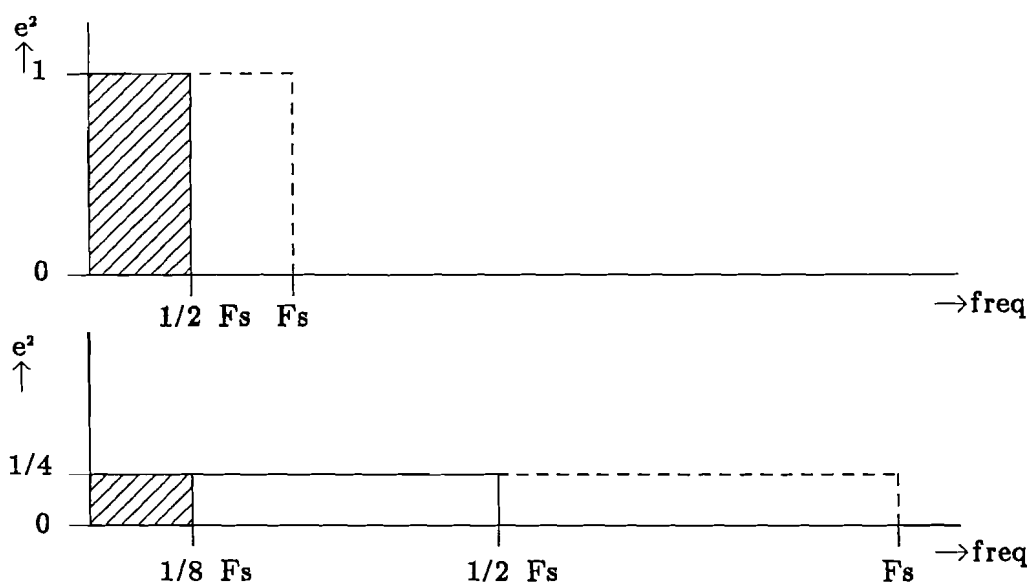
Figure 2.2: Quantization noise of a Nyquist converter and of a four times oversampled converter. Dashed area is baseband noise.

Further we have to adapt the signal-to-noise ratio for a system with signal bandwidth f_b. Normalized over a bandwidth f_b this S/N becomes :

$$S/N = 2^n \sqrt{1.5} \sqrt{\frac{f_s}{2f_b}}$$ (2.12)

Which is in decibels

$$S/N = n \times 6.02 + 1.76 + 10 \log \frac{f_s}{2f_b} \quad \text{dB}$$ (2.13)

In a four times oversampled converter the noise power has reduced by a factor 4, so the improvement in the S/N ratio is 6 dB or 1 bit.

2.5 Possible realization

In section 2.4, the basic dynamic range of an A/D converter has been determined. In equation 2.12 the only parameters are the sample frequency and the number of bits. When using A/D-converters a larger dynamic range or higher signal-to-noise ratio can be reached by :

• enlarge the number of bits

• increase the oversampling ratio

Of course we can not expand the number of bits unlimited for we have restrictions in linearity and other realization problems. Also the number of comparators in an A/D

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converter increase with the number of bits. Figure 2.3 depicts a four bit flash converter which has $16 = (2^4)$ comparators. These are connected to a resistor ladder and the input signal. In the PLA the output code of the comparators is converted into a four-bit code. Also overflow can be detected.
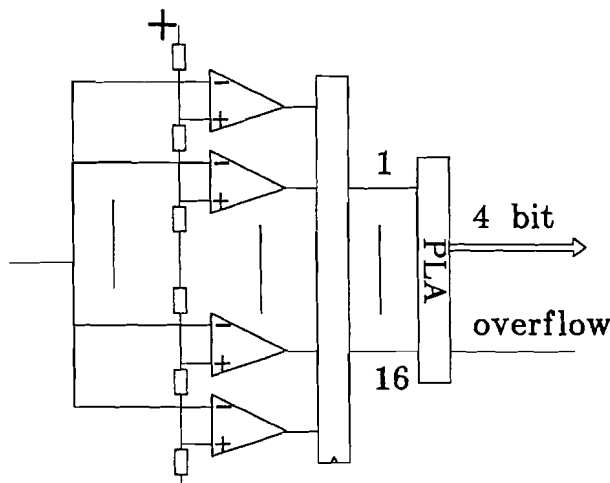
Figure 2.3: Four bit flash converter.

When changing to 5 bit, we need $2^5 = 32$ comparators. This implies an increase of chip area which is not allowed.

Therefore multi-step converters have been designed (see figure 2.4). In this type of converter the input signal is sampled and after a coarse quantization has taken place the difference between the original signal and the output signal of the DAC is taken to a fine quantizer. These converters require a smaller number of comparators. When we compare a 10-bit flash converter with a two-step 10-bit flash converter the ratio is 1024 to 64 (2^{10} to 2×2^5) which reduces the die size used by comparators with a factor 16 !! The linearity of the first flash converter which determines the coarse quantization must meet the 10-bit specifications.

The sample frequency of a converter can be increased and gives normally a good improvement but hereby we have the restriction of the maximal reachable frequencies on the chip. The oversampling factor for audio with a maximum signal frequency of 20 kHz, can still be large. For instance a 40 MHz sampling frequency would give an oversampling factor of 1000 times. This implies according to equation 2.13 a 30 dB improvement in dynamic range. When using video signals with a maximum signal frequency of 5 MHz, the oversampling factor with the same sampling frequency becomes only 8 times. This gives only a 9 dB better S/N ratio than the original without oversampling.

2.6 Conclusions

The basic signal-to-noise ratio of converters has been found and we have seen the improvement caused by oversampling. The use of multi-step converters proved to be very
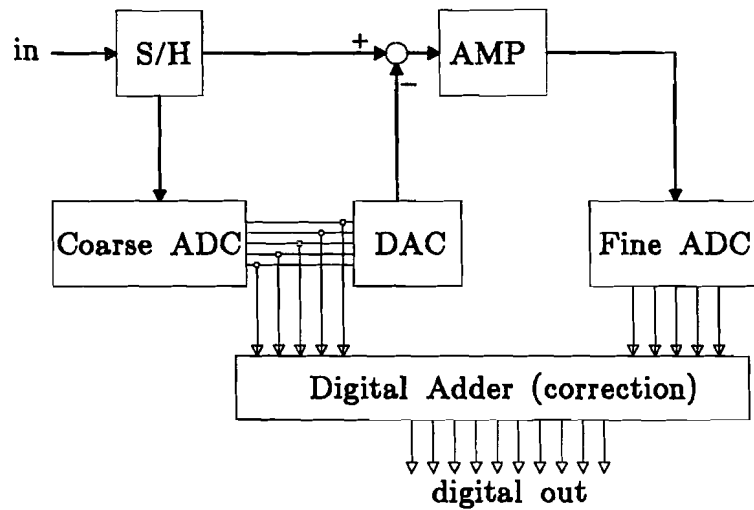
Figure 2.4: Two-step converter.

useful in limiting the number of components and thus chip-size. The increase of the sample frequency is not unlimited. We have to restrict ourselves to physical limits.

Now we have to look to other techniques to reduce the baseband noise. The increase of quantization levels is restricted to technical limitations of matching reference sources.

Chapter 3

Sigma-Delta A/D conversion

3.1 Introduction

In order to obtain a large dynamic range, the noise in the signal band needs to be reduced more and therefore we introduce sigma-delta conversion. First we will look at the fundamentals of this technique, then we'll describe the influence of the filter-order in a sigma-delta converter. Next the theoretical dynamical range curves will be derived and finally multi-bit conversion is discussed.

3.2 Sigma-delta conversion

A basic sigma-delta converter is given in figure 3.1. It consists of an analog filter G, a quantizer Q and a D/A-converter in the feedback loop. The basic idea of sigma-delta modulation is to shape the quantization noise to higher frequencies and hence the dynamic range in the baseband is increased.
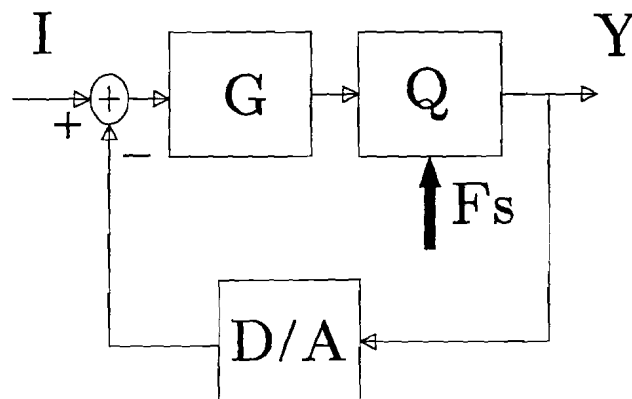
Figure 3.1: Sigma-delta converter block diagram.

In figure 3.1 we see that we have to deal with a non-linear element as a quantizer. After quantization in a multi-bit quantizer, we expect to have our original signal plus some distorsion. This is why we model our quantizer as in figure 3.2.
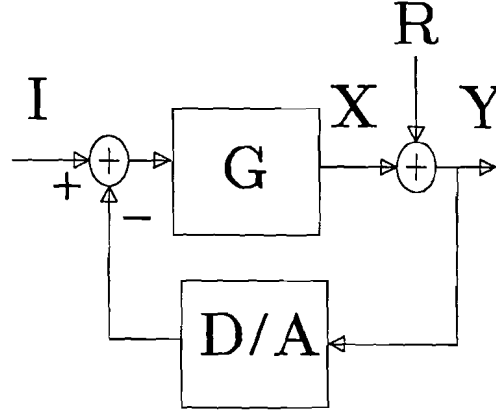
Figure 3.2: Sigma-delta converter with modeled quantizer.

In figure 3.2 the quantizer input signal is X. The quantizer transfer function is :

$$y(k) = x(k) + r(k) \tag{3.1}$$

Thus follows :

$$Y(z) = \frac{G(z)}{1 + G(z)} I(z) + \frac{1}{1 + G(z)} R(z) \tag{3.2}$$

This is the basic transfer function of a sigma-delta modulator. To minimize noise, the filter transfer function $G(z)$ must be large. Then the transfer function of the input signal approximates 1. When $G(z) >> 1$ equation 3.2 yields :

$$Y(z) \approx I(z) + \frac{1}{G(z)} R(z) \tag{3.3}$$

3.3 Theory of a first-order sigma-delta converter

We will now use a first-order filter G which has a transfer function $G(z) = \frac{1}{z-1}$ which is an integrator. Substitution into equation 3.2 yields :

$$Y(z) = z^{-1}I(z) + (1 - z^{-1}) R(z) \tag{3.4}$$

To calculate the signal power, Parsevals equation gives :

$$signal\ power = \frac{1}{2\pi} \int_{-\pi}^{+\pi} (power\ density(\theta))\, d\theta \tag{3.5}$$

Which gives for the noise power in a sigma-delta converter :

$$\varepsilon_{noise}^2 = \frac{1}{2\pi} \int_{-\pi}^{+\pi} |R(\theta)|^2 \frac{1}{|1 + G(\theta)|^2}\, d\theta \tag{3.6}$$

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We suppose that the quantization error is random and there is no correlation with the input signal. The noise is assumed to be white with an average power density of $\frac{q^2}{12}$. The total baseband quantization error can be found by integrating the error over the bandwidth θ_1 which results in :

$$\varepsilon_{baseband}^2 = \frac{1}{\pi} \int_0^{\theta_1} \frac{q_s^2}{12} |1 - z^{-1}|^2 \, d\theta \tag{3.7}$$

In this equation G(z) has been used, which has to be adapted to G(θ). Inserting into the equation $z = e^{j\theta}$ and substituting $\theta_1 = \frac{2\pi f_b}{f_s}$ follows :

$$|1 - z^{-1}|^2 = \frac{|e^{j\theta} - 1|^2}{|e^{j\theta}|^2} \tag{3.8}$$

$$|1 - z^{-1}|^2 = 2(1 - \cos\theta) \tag{3.9}$$

$$\begin{aligned}
\varepsilon_{baseband}^2 &= \frac{1}{\pi} \int_0^{\theta_1} \frac{q_s^2}{12} 2(1 - \cos\theta) \, d\theta \\
&= \frac{q_s^2}{12\pi} [2(\theta_1 - \sin\theta_1)]
\end{aligned} \tag{3.10}$$

Without noise shaping the total baseband noise would be :

$$\varepsilon_{without}^2 = \frac{1}{\pi} \int_0^{\theta_1} \frac{q_s^2}{12} \, d\theta = \frac{q_s^2}{12\pi} \theta_1 \tag{3.11}$$

So the improvement factor F, in dynamic range, due to sigma-delta modulation equals :

$$F = \frac{\varepsilon_{baseband}}{\varepsilon_{without}} = \sqrt{2(1 - \frac{\sin\theta_1}{\theta_1})} \tag{3.12}$$

Approximating $\frac{\sin\theta_1}{\theta_1}$ with $1 - \frac{1}{6}\theta_1^2$ yields :

$$F = \sqrt{2(1 - \frac{\sin\theta_1}{\theta_1})} = \sqrt{\frac{1}{3}} \theta_1 = \sqrt{\frac{1}{3}} \frac{2\pi f_b}{f_s} \tag{3.13}$$

We now also see that the improvement factor depends on the oversampling factor. This indicates that using a high oversampling factor increases the improvement factor F.

Figure 3.3 depicts the quantization noise density at the output of a Nyquist converter, a four times oversampled converter and a first-order sigma-delta converter at 4 times oversampling.

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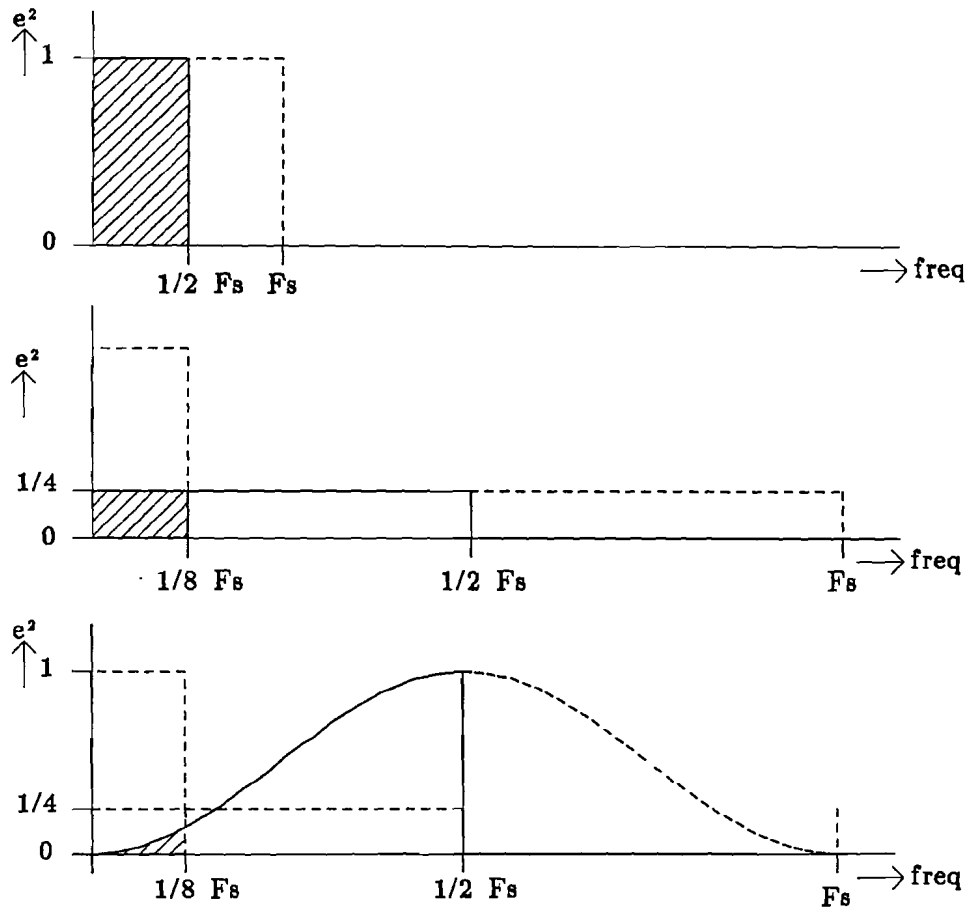
Figure 3.3: Quantization noise in a (a) Nyquist converter, (b) Four times oversampled converter, (c) First-order sigma-delta converter.

The quantization noise in the baseband decreases while it increases at higher frequencies. Our goal is to decrease the baseband noise in which we have been successful.

3.4 Theory of high-order filters in sigma-delta modulation

When using a higher order filter in a sigma-delta modulator the noise shaping will change. A higher order filter is now assumed to be a cascade of first-order filter sections. The transfer function of a n'th order filter now becomes $G(z) = \left(\frac{1}{z-1}\right)^n$. When using this in equation 3.2 equation 3.9 results in :

$$|1 - z^{-1}|^{2n} = [2(1 - \cos\theta)]^n \qquad (3.14)$$

Using the fact that the sample frequency f_s is large compared to the bandwidth f_b, we can approximate $\cos\theta$ by $1 - \frac{\theta^2}{2!}$. Thus we get formula :

$$|1 - z^{-1}|^{2n} = [2(1 - [1 - \frac{\theta^2}{2!}])]^n = 2\frac{\theta^2}{2!}^n = \theta^{2n} \qquad (3.15)$$

Now the total inband quantization noise in the noise shaper becomes :

$$\mathcal{E}^2_{total} = \frac{1}{\pi}\int_0^{\theta_1} \frac{q_s^2}{12}\theta^{2n}\,d\theta = \frac{q_s^2}{12\pi}\frac{\theta_1^{2n+1}}{2n+1} \qquad (3.16)$$

With this the improvement factor F, compared with formula 3.12, becomes :

$$F(n) = \sqrt{\frac{1}{2n+1}}\theta_1^n \qquad (3.17)$$

The total improvement factor for the dynamic range ratio, also including the improvement caused by oversampling, we get is :

$$H(n) = \frac{1}{\sqrt{\frac{1}{2n+1}}\theta_1^n\sqrt{\frac{2f_b}{f_s}}} \qquad (3.18)$$

Substitution of $\theta_1 = \frac{2\pi f_b}{f_s}$ gives :

$$H(n) = \frac{1}{\sqrt{\frac{1}{2n+1}}\left(\frac{2\pi f_b}{f_s}\right)^n\sqrt{\frac{2f_b}{f_s}}} = \frac{\sqrt{2n+1}}{(\pi)^n}\left(\frac{f_s}{2f_b}\right)^{(n+\frac{1}{2})} \qquad (3.19)$$

The S/N ratio of this system now becomes :

$$S/N(n) = A\sqrt{1.5}\,\frac{\sqrt{2n+1}}{(\pi)^n}\left(\frac{f_s}{2f_b}\right)^{n+1/2} \qquad (3.20)$$

Now introducing the number of quantization levels as 2^m, $m \gg 1$ this becomes

$$S/N(n) = 2^m\sqrt{1.5}\,\frac{\sqrt{2n+1}}{(\pi)^n}\left(\frac{f_s}{2f_b}\right)^{n+1/2} \qquad (3.21)$$

or in decibels

$$S/N = m \times 6.02 + 1.76 + 20(n + \frac{1}{2})\log\frac{f_s}{2f_{sig}} - 20n\log\pi + 10\log(2n+1) \quad \text{dB} \qquad (3.22)$$

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With these formulas calculations of dynamic ranges can be done. After a specification of dynamic performance has been given a designer can decide which number of bits and which order of sigma-delta modulator should be taken. Although he has to remind the assumptions we have made in approximating $\cos\theta$ ($f_s >> f_b$) and the physical limits of the used integrated circuit technology e.g. CMOS maximum frequency of 50 MHz which restricts the oversampling factor.

3.5 Adaptation of stable high-order filters in one-bit sigma-delta modulation

In the theory we've assumed a combination of ideal integrators in the filter. Now we have to adapt this according to stability demands of the filter. We now use G(z) as uniform expression for the filter transfer function. We have a sigma-delta converter with a one-bit quantizer, according to figure 3.4.
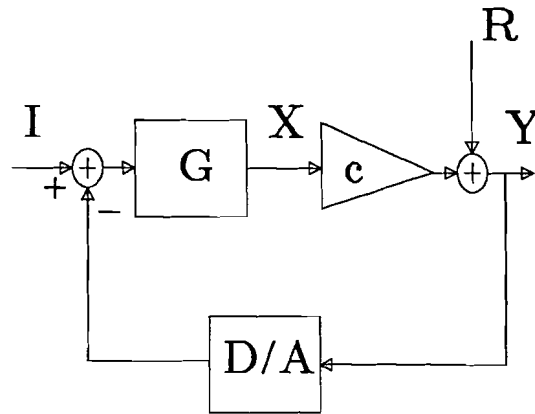
Figure 3.4: Sigma-delta modulator with 1-bit quantizer.

In this figure the quantizer is replaced by the linear model :

$$y(k) = cx(k) + r(k) \tag{3.23}$$

Where :

$$Y(z) = \frac{cG(z)}{1 + cG(z)} I(z) + \frac{1}{1 + cG(z)} R(z) \tag{3.24}$$

We now calculate the total noise power according to Parsevals equation 3.5, using equation 3.24 yields :

$$P_n = \frac{1}{\pi} \int_0^\pi |R(z)|^2 \frac{1}{|1 + cG(z)|^2} d\theta \tag{3.25}$$

Both G(z) and R(z) have been used, which have to be adapted to $G(\theta)$ and $R(\theta)$. This equation has to be in agreement with the power equation of the sigma-delta modulator :

$$P_n + P_i = P_y \tag{3.26}$$

The output power P_y is calculated as the quantizer quantizes between $+\frac{q_s}{2}$ and $-\frac{q_s}{2}$. Important, note that we now use a *one-bit* quantizer. We also assume that there is no input signal so from equation 3.26 follows :

$$P_{ni} = P_y = \frac{q_s^2}{4} \tag{3.27}$$

This gives, after substitution for $G(z) = \frac{(z-a)^n - (z-1)^n}{(z-1)^n}$ which is a filter of order (n) filter with n poles at z = 1 to maintain stability, in equation 3.25 an idle channel inband noise power of :

$$P_{ni} = \frac{1}{\pi} \int_0^\pi |R(z)|^2 \frac{1}{|1 - c + c\frac{(z-a)^n}{(z-1)^n}|^2} d\theta \tag{3.28}$$

Using $z = e^{j\theta}$ and approximating $\cos\theta$ by $1 - \frac{\theta^2}{2!}$ when $\theta \ll 1$ gives :

$$P_{ni} \approx \frac{1}{\pi} \int_0^{\theta_1} \frac{q_s^2}{12} \frac{\theta^{2n}}{c^2(1-a)^{2n}} d\theta = \frac{q_s^2}{12\pi} \frac{\theta_1^{2n+1}}{c^2(1-a)^{2n}(2n+1)} \tag{3.29}$$

In this equation the noise spectrum R(z) is assumed to be uniform and uncorrelated with the input spectrum and having a value of $\frac{q_s^2}{12}$. Now we see that when choosing a value a for the filter, c is found from equation 3.25 and 3.26. With this value of c the idle channel inband noise power can be determined. The values for c which have been found in this way, are shown in table 3.1.

Order	a	c
1	0	1.333
2	0	0.667
3	0.5	0.905

Table 3.1: Gain factor of 1 bit quantizer as function of filter-order.

Now we can calculate again the dynamic range of the high-order sigma-delta converter. Substitution of $\theta_1 = \frac{2\pi f_b}{f_s}$ gives :

$$S/N(n) \approx \frac{A\sqrt{1.5}}{\sqrt{\frac{1}{2n+1}} \frac{1}{c(1-a)^n} \left(\frac{2\pi f_b}{f_s}\right)^n \sqrt{\frac{2f_b}{f_s}}} = A\sqrt{1.5} \frac{c(1-a)^n\sqrt{2n+1}}{(\pi)^n} \left(\frac{f_s}{2f_b}\right)^{(n+\frac{1}{2})} \tag{3.30}$$

From this equation we see that a given stable loop filter, which provides a value for c, also has a certain dynamic range, depending on the oversampling factor. The dynamic range is depicted in figure 3.5.

S/N approx (1-order) [dB]

S/N approx (2-order) [dB]

S/N approx (3-order) [dB]
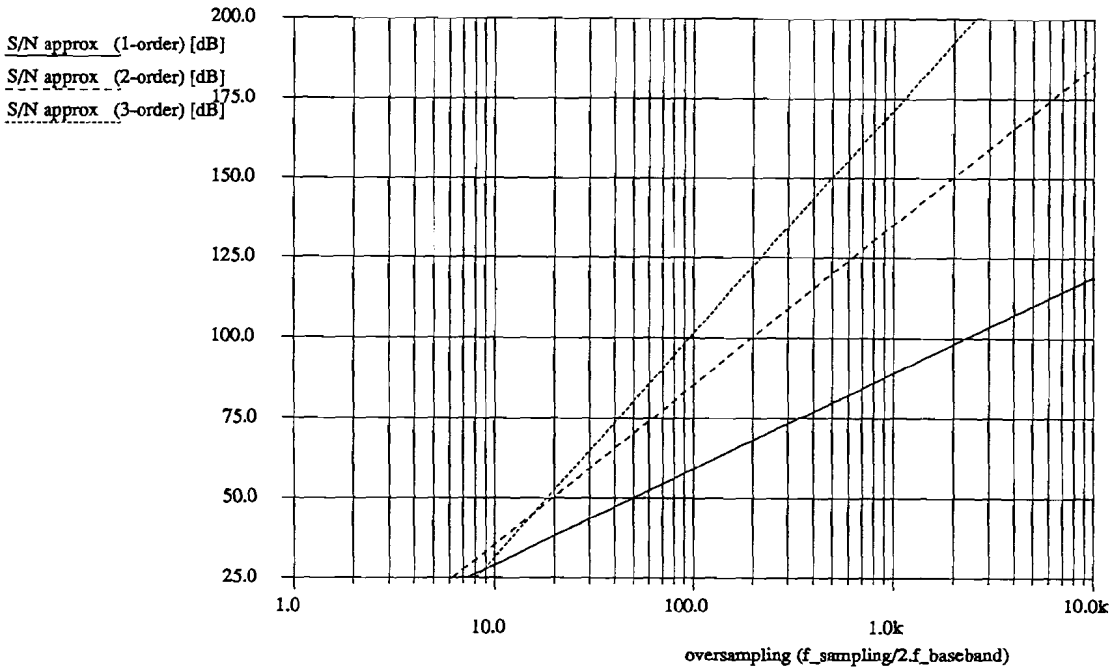
Figure 3.5: Dynamic range as function of the oversampling ratio.

From figure 3.5 we see that the dynamic range can be increased when the loop filter order is increased.

At low oversampling ratios, a numerical approximation program is used to calculate the integral in equation 3.25. When using an oversampling factor of one (Nyquist converter), the idle noise power equals $q_s^2/4$ and the maximum signal power is $q_s^2/8$ so a dynamic range of -3 [dB] results. This is depicted by figure 3.6, the two theory curves are numerically calculated.

The theoretical curves form the basis of the noise-shaping theory. We also see that the approximations made for a large oversampling factor are correct. In figure 3.6 the difference between the approx- and theoretical curves of the same filter order is already minimal at five times oversampling.

Now we have seen that the dynamic range can be expanded by increasing the loop-filter order, we could conclude that we only have to use a very high-order filter and any dynamic range can be realized. Theoretically this is true for a large oversampling factor. But there are also stability criteria for the sigma-delta loop so these filters will become very complex. The curves show that at low oversampling ratios the dynamic range decreases for a higher filter order. In figure 3.6 the curves of the second-order filter are below the ones of the first-order filter.

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S/N theory   (1-order) [dB]
S/N approx   (1-order) [dB]
S/N theory   (2-order) [dB]
S/N approx   (2-order) [dB]

oversampling (f_sampling/2.f_baseband)
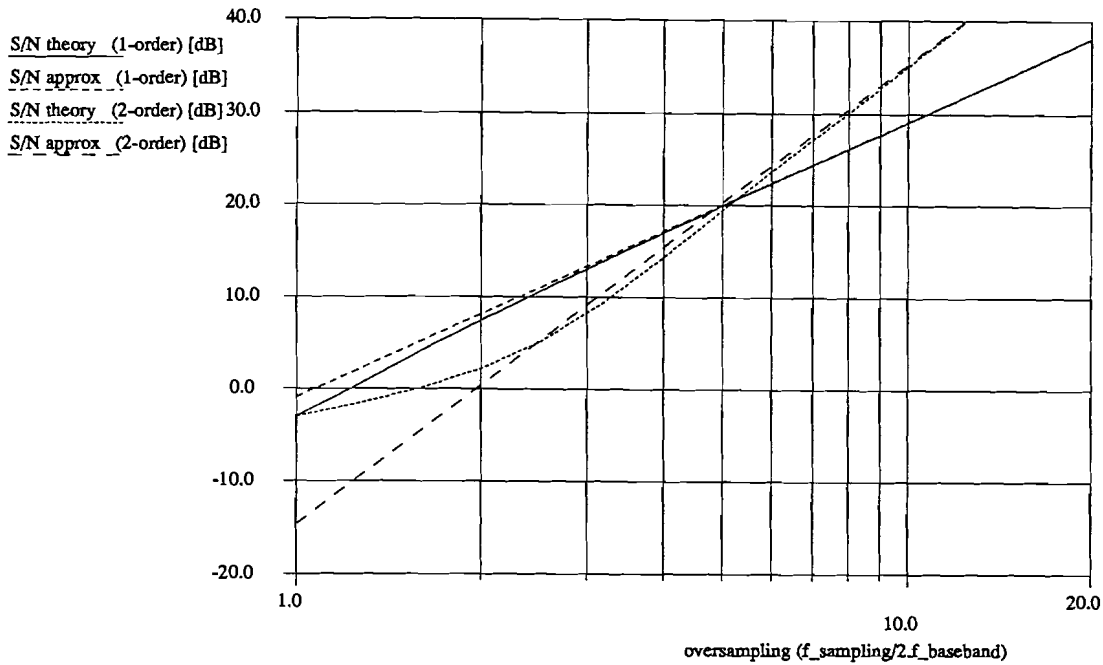
Figure 3.6: Dynamic range at low oversampling.

3.6   Multi-bit quantizer

In our basic sigma-delta modulator scheme we now have seen the influence of the filter order on the dynamic range. We have deduced exactly the one-bit quantizer case. Now we will look at the situation when using a multi-bit quantizer (figure 3.7). The outputs of the multi-bit quantizer are coupled by a multi-bit D/A-converter to the input. In this case we give up the ideal linearity which we had when using a one-bit D/A-converter in the feedback loop. The now used DAC has to have the highest requested linearity of the system. This gives in our system a 16 bit linearity !

Now assuming the gain of the quantizer to be one. This should be valid for a random signal over all quantization levels. The increase of the number of levels implies an improvement, for the noise power is reduced.

In figure 3.8 we see that an increment of quantization bits gives more intervals which give a decrease of absolute quantization error when matched on the original quantization interval. The theoretical improvement is given in table 3.2.

22
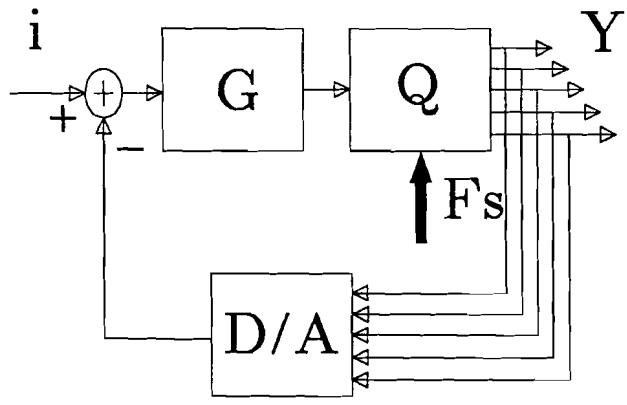
Figure 3.7: Sigma-delta converter with multi-bit quantizer
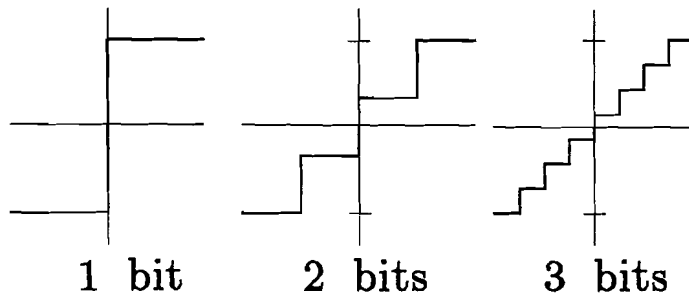
Figure 3.8: Change of individual quantization interval due to multi-bit.

Number of bits	Number of quantization levels	Improvement to level before [dB]	Improvement to 1 bit level [dB]
1	1	*	*
2	3	9.5	9.5
3	7	7.4	16.9
4	15	6.6	23.5
5	31	6.3	29.8
n	$2^n - 1$	$20\log \frac{2^{n-1}-1}{2^n-1}$	$20\log 2^n - 1$

Table 3.2: Improvement to one-bit quantizer with gain = 1 by increasing number of bits.

The original shaping curves also change a fraction, we now use a gain of 1 and satisfy the power equation this gives curves from figure 3.9.

23
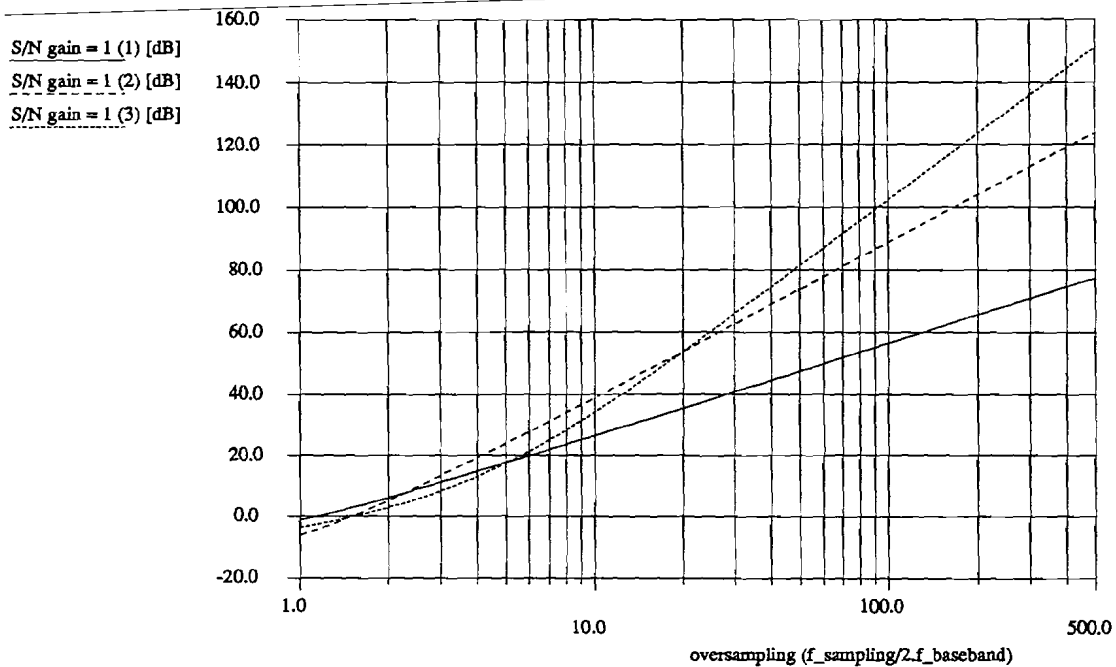
Figure 3.9: Dynamic range, gain = 1.

3.7 Conclusions

The dynamic range of a sigma-delta modulation system has been derived for both filter order and the number of bits of the quantizer. We have seen that the improvement in dynamic range due to the noise shaping performance of the modulator is dependent on the oversampling factor, the filter order and the number of bits of the quantizer. When going to a multi-bit quantizer, we loose our absolute linearity in the D/A-converter.

This principle is avoided in the present audio D/A-converters. We have the capability to use a large oversampling factor, hence the audio-signal band is only 20 kHz, and we don't want to loose linearity so we use a one-bit DAC which is oversampled 256 times. When using a second order filter we theoretically would get a dynamic range of more than 100 dB.

Chapter 4

Specifying the sigma-delta A/D-converter with variable resolution

4.1 Introduction

In this chapter the specifications are resumed and a possible realization is proposed. Then a design is presented and the theoretical specs are given, finally the first simulation results will be given.

4.2 Minimum requirements of the product division

After determining the theory of sigma-delta conversion, we have to look at our application. We now resume the, by the product division, Test and Measurements (T & M), postulated bands of interest and resolutions.

- Bandwidth 5 MHz
  Resolution 8 bit (dynamic range of 48 dB)

- Bandwidth 1 MHz
  Resolution 10-12 bit (dynamic range between 60 and 72 dB)

- Bandwidth 20 kHz
  Resolution 16 bit (dynamic range of 96 dB)

4.3 Minimum theoretical design

To realize all the specifications mentioned in the section before in a single design, first a uniform sample frequency is chosen. Due to technical limitations of the CMOS technology and operating speed of digital signal processors, we have restricted ourselves to a 20 MHz sample frequency.

Another advantage of this choice is that a 20 MHz signal is already present on the multi-function card. In this case we have the following oversampling ratios :

- 2 times oversampling

- 10 times oversampling

- 500 times oversampling

Reviewing the theory of chapter 3, we use the numerical curves of figure 3.6. When calculating the dynamic range of a *1-bit* sigma-delta A/D-converter as function of oversampling ratio, we find in table 4.1 the values using a first to third order loop-filter at the given oversampling values.

Oversampling factor	Dynamic Range [dB]			
	First Order Filter	Second Order Filter	Third Order Filter	requested
2	7.4	2.2	2.4	48
10	29.1	35.1	33.2	60
500	80.0	120.3	150.4	96

Table 4.1: Dynamic range as function of oversampling ratio and loop-filter order. When a 1-bit quantizer is used.

Considering the requested resolution at the given bandwidths (see section 4.2) we see that only the third requirement can be realized with a one-bit sigma-delta A/D-converter. To realize the other requirements we must switch to multi-bit quantization and than reconsidering again the minimum requested filter order (curves gain = 1 figure 3.9). With this decision we give up the ideal linearity, when using a one-bit D/A-converter in the feedback loop of the sigma-delta modulator. Now the D/A-converter in the feedback loop has to satisfy a linearity of 16 bit which is the highest requirement in the system. Table 4.2 gives the basic dynamic range values at given oversampling ratios for a multi-bit situation.

Oversampling factor	Dynamic Range [dB]			
	First Order Filter	Second Order Filter	Third Order Filter	requested
2	6.1	5.1	2.8	48
10	26.6	38.9	34.2	60
500	77.6	123.6	151.3	96

Table 4.2: Dynamic range as function of oversampling ratio and loopfilter order, multi-bit situation simulated with a 1-bit quantizer with gain 1.

Using the theoretical improvement when using a multi-bit quantizer from section 3.6, we see that the first requirement can be realized when using a 7 bit quantizer. For the second requirement we must have at least a 4 bit quantizer in combination with a second order loop-filter (10 bit). Or a 6 bit quantizer with a second order filter for 12 bit resolution. This gives the following minimum realization of the preliminary specifications :

Oversampling factor	Filter order	Dynamic Range [dB]			requested # bits
		Filter	requested	difference	
2	1	6.1	48	41.9	7
2	2	5.1	48	42.9	8
10	1	26.6	60	33.4	6
10	2	38.9	60	21.1	4
500	1	77.6	96	18.4	4
500	2	123.6	96	+27.6	*
500	2	120.3	96	+23.3	1

Table 4.3: Requested number of bits to use in quantizer in sigma-delta modulator. The * means no multi-bit quantizer required.

Using these demands we would have to make three parallel sigma-delta A/D-converters which would be selected after choosing one range. But this was not the goal of the product division so now we have to adapt the preliminary specifications such that only one sigma-delta loop can be used for all bands of interest.

4.4 First proposed design

We have to design a minimal uniform sigma-delta loop, we want to use the most easy realization. With the given minimum requirements we need to have a 7-bit quantizer (first demand) and a first-order filter. The use of this quantizer implies also the use of a 7-bit D/A-converter in the loop. The loop will be hard to realize.

With this given structure we receive theoretically the following dynamic ranges.

Oversampling factor	Dynamic Range [dB]			Theoretical resolution [bits]
	First Order Filter	Multibit	Total	
2	6.12	42.14	48.26	8
10	26.61	42.14	68.75	11
500	77.59	42.14	119.73	19

Table 4.4: Theoretical dynamic ranges of the design.

We also see that all specifications met. The dynamic range of the 20 kHz band is even overdone with more than 20 dB. In the realization the bands of interest will be filtered out in a digital filter and downsampled, which can be carried out partly by a digital signal processor. The basic design is shown in figure 4.1. The design uses a 7-bit quantizer and a first order filter.
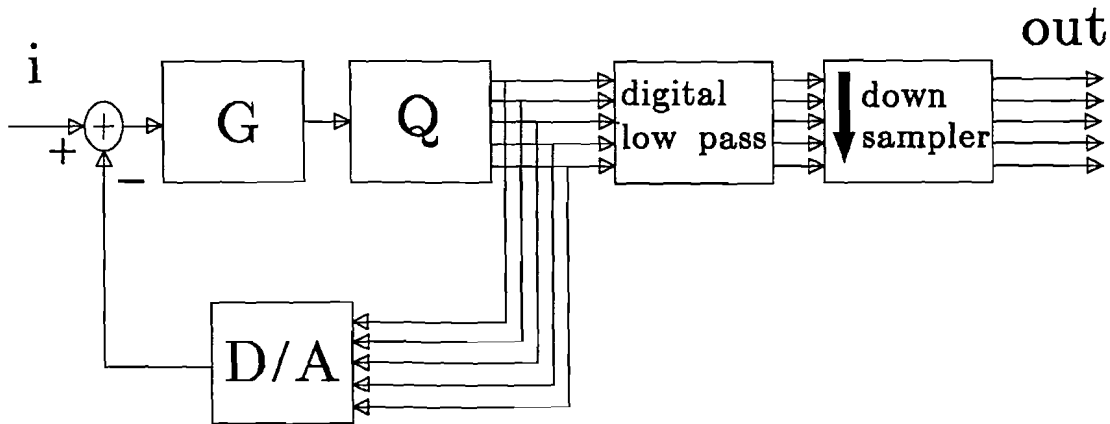

Figure 4.1: Practical design

In the basic design we have used only one digital low-pass filter and one downsampler, in the practical realization we need to have more parallel filter downsampler combinations which will be chosen after selecting a range. With this proposed structure we also can see that we have an important problem. The 7-bit D/A-converter in the feedback loop has to have a 16 bit accuracy to sustain the 16 bit 20 kHz demand. Present using current calibration techniques only 90 dB (15 bit) can be realized. We see that the specifications restrict us from using advantages of one technique, for the 5 MHz band specs we have to give up the one-bit quantizer, which linearity would have been very useful in realizing the 20 kHz band specs.

4.5 First simulations of the designed sigma-delta modulator

With the mixed level simulator MILES the design has been simulated. The input signal of the system is a sine wave with amplitude 0.7447 Volt and a frequency of 10 kHz. On the simulation results a Fourier transformation has been performed. The output spectrum at the quantizer output is given in figure 4.2.

During the transformation also the signal-to-noise ratio for each band of interest has been calculated. These values have to be corrected for the amplitude of the input signal has a larger range (max 1 Volt). All values are given in table 4.5.
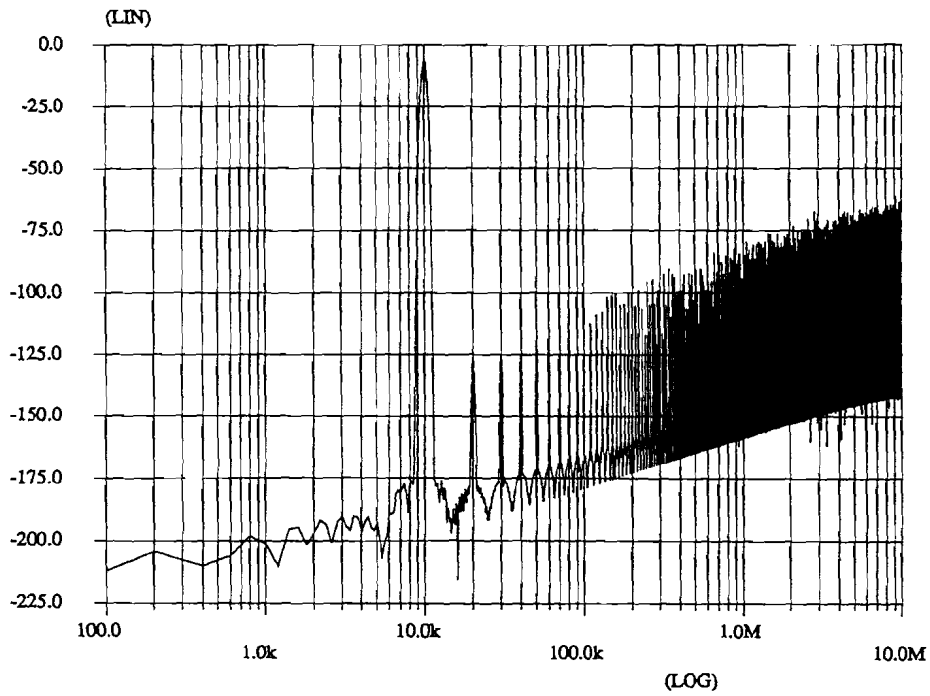
Figure 4.2: Spectrum at the quantizer output of the sigma-delta converter

signalband [kHz]	noiseband [Hz]	S/N ratio [dB]	input correction	simulated S/N [dB]	theoretical S/N [dB]	difference [dB]
8.6 - 11.4	1k - 5M	45.80	2.56 dB	48.36	48.26	+0.1
8.6 - 11.4	1k - 1M	66.37	2.56 dB	68.93	68.75	+0.2
8.6 - 11.4	1k - 20k	123.19	2.56 dB	125.75	119.73	+6.0

Table 4.5: Simulated S/N ratios of the bands, input frequency 10 kHz 50 periods.

We see that the simulation results almost exactly match the theoretical values except for the high (500 times) oversampling factor. That's why the performance of the 7-bit first-order sigma-delta modulator is also simulated at other oversampling ratios. The results are in table 4.6.

oversampling factor	S/N ratio [dB]	input correction	simulated S/N [dB]	theoretical S/N [dB]	difference [dB]
2	45.80	2.56 dB	48.36	48.26	+0.1
10	66.37	2.56 dB	68.92	68.75	+0.2
20	74.69	2.56 dB	77.25	77.73	-0.5
50	86.85	2.56 dB	89.41	89.73	-0.3
100	95.69	2.56 dB	98.25	98.73	-0.5
200	106.88	2.56 dB	109.44	107.73	+1.7
500	123.19	2.56 dB	125.75	119.73	+6.0

Table 4.6: Simulated S/N ratios of the bands, input frequency 10 kHz 50 periods.

We see that for high oversampling ratios the sigma-delta modulator has a better performance than theoretically expected. This is caused by correlation for other simulations gave a lower S/N ratio.

4.6 Conclusions

According to the specifications a multi-bit sigma-delta A/D-converter has been designed. The design has been simulated and has proved to be satisfactory. For high oversampling ratios, the simulated values are even better than the theoretical. We now assume that the design will at least match the specifications.

Now with this first design we continue and we have to look at the output stage of the sigma-delta loop. The data coming out of the quantizer has a sample rate of 20 MHz and to be able to process this data we have to decrease this rate.

Chapter 5

The filter structure

5.1 Introduction

According to the first design proposal, the system clock frequency of the sigma-delta converter is chosen to be 20 MHz and a 7-bits quantizer is used. The PCM code at the output of the sigma-delta loop, of the three specified bandwidths are derived by means of individual low-pass filtering, followed by down-sampling.

The allowed passband ripple specification of Test & Measurements equated :

- Passband Ripple < 0.2 dB DC to 100 kHz (T & M)

- Passband Ripple < 1.0 dB 100 kHz to 500 kHz (T & M)

- Passband Ripple < 1.0 dB 500 kHz to 5 MHz (own specification)

In this chapter we will look at the basic function of the downsampling filters. How downsampling can be done and what implication this has on the filter structure. After determining the individual filter specifications, the individual filter sections are designed. Next the first simulation results of the designed filter structure with the already designed sigma-delta modulator are given. Finally the conclusions are forwarded.

5.2 Downsampling

When we want to decrease the sampling frequency, we can see according to figure 5.1 that the input spectrum is repeated around the new sample frequency Fs' and its multiplications. This action doesn't cause any aliasing when the input spectrum is band-limited and the new sample frequency is at least twice the maximum signal frequency in the baseband (Nyquist criterion).

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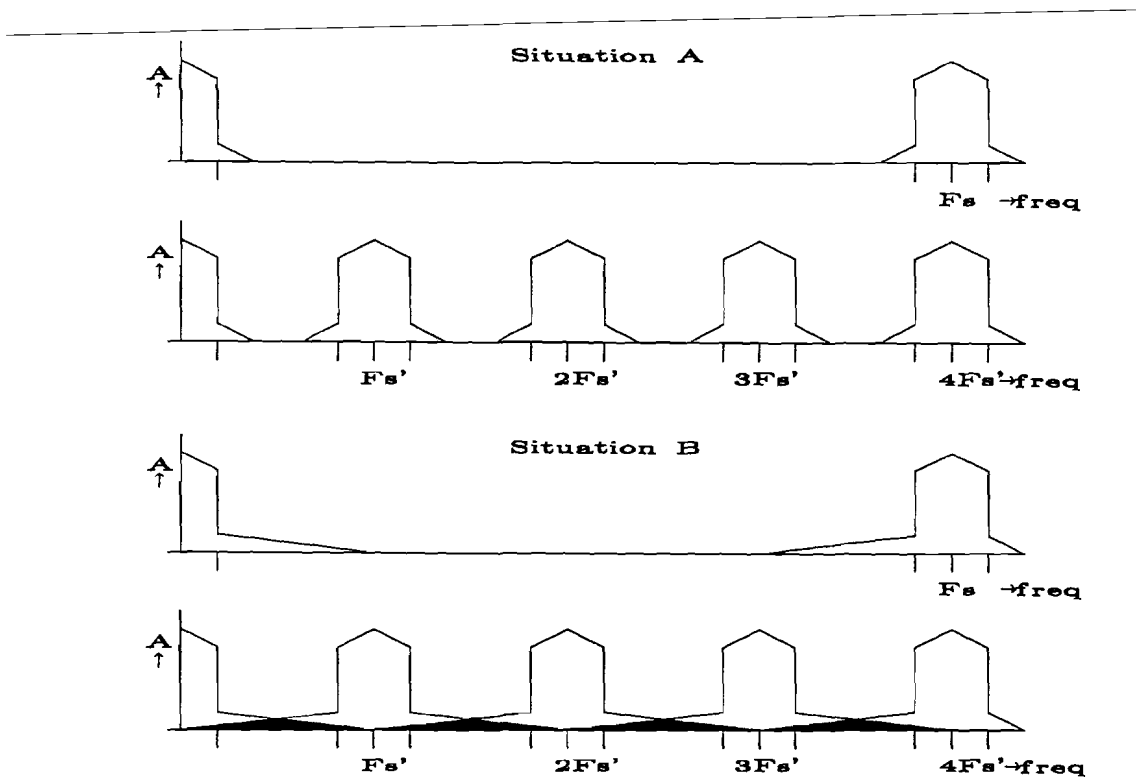
Figure 5.1: Downsampling and aliasing : Situation A an original spectrum and the four times downsampled spectrum. Situation B a spectrum and its downsampled spectrum in which aliasing has taken place.

In situation B this condition is not fulfilled and after downsampling is performed, frequencies higher than $f_s/2$ are folded back in the baseband spectrum (aliasing). The baseband spectrum of the original and the downsampled version differ, so our output signal is deteriorated.

To avoid aliasing an ideal low-pass filter is inserted before the downsampler (figure 5.2). This filter with a cut-off frequency of Fs'/2 removes all frequencies higher than Fs'/2 and now no aliasing occurs during downsampling so our original baseband signal is retrieved.
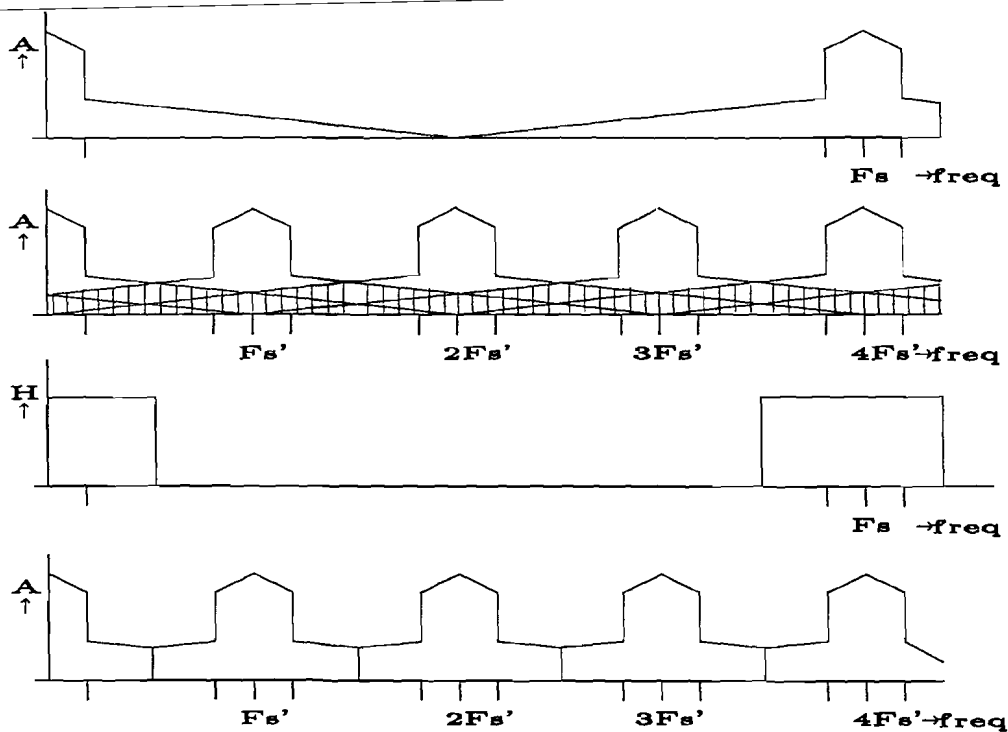
Figure 5.2: Downsampling and aliasing : an original spectrum and the four times downsampled spectrum. Ideal low-pass filter transfer and the downsampled spectrum in which no aliasing has taken place.

In practice an ideal low-pass behavior can only be approximated. The low-pass filter attenuation must reduce the high frequencies in the input signal at such an extence that when folded back the degradation of the signal-to-noise ratio in the baseband is not too large.

5.3 Low-pass filters complexity

In figure 5.3 the design criteria of a low-pass filter are depicted. The downsampling factor and our original signal determines specifications for the stopband attenuation and for the length of the stopband. The complexity of a low-pass filter depends on :

- Width of transition band.

- Place upper passband point u_p.

- Passband ripple δ_1.

- Stopband ripple δ_2.

This influences the filter order and hence the number of coefficients. Of course low-order filters with simple coefficients, which take less chip area, are preferred. Also the
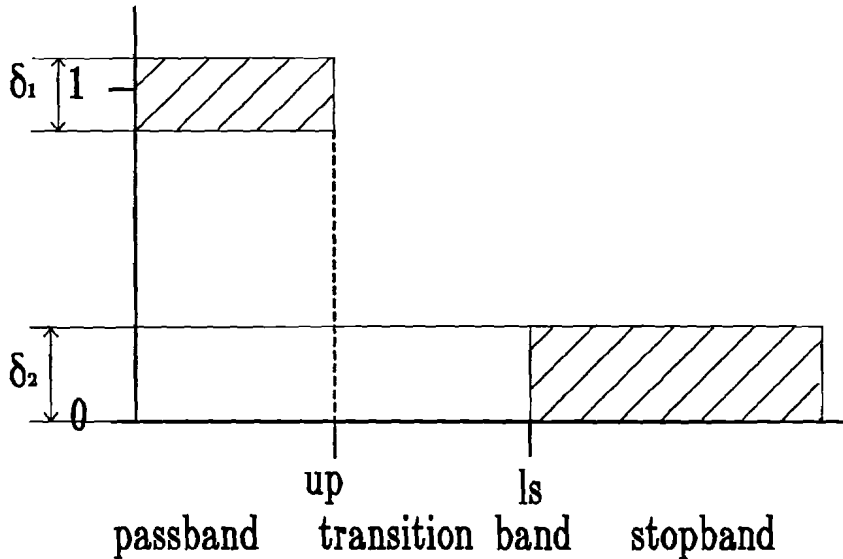
Figure 5.3: Filter design criteria.

speed they have to operate on, is a limiting factor because a high-order complex filter requires very fast logic.

5.4 Decimating filter structure

In principle a decimating filter which consists of a low-pass filter and a down-sampler, could be designed for each individual bandwidth. In the design we tried to combine filter sections for the different bandwidths as much as possible in order to get a more efficient realization. The way decimating filters are constructed also implies possible merging of different filter sections.
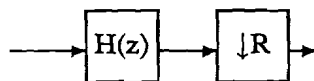
Figure 5.4: Decimating filter with downsampling factor R.

Figure 5.4 depicts a decimating filter which contains a low-pass filter to avoid aliasing and a downsampler. When the downsampling factor is large, this filter is realized as a cascade of decimation sections, which significantly reduces the complexity of the filters. If only one filter and one downsampler are used, the requested filter order is very high and hence the low-pass filter becomes complex and thus large. When using cascaded sections all filters become more simple because the relative width of the transition band increases.

In figure 5.5 we see a decimating filter, which consists of three decimating sections. Mostly the downsampling factor is divided into prime numbers and than a cascade is formed in which the largest prime number of the downsampling factor is used in the first decimating filter. In this way the speed demands for the multipliers and adders are decreased as fast as possible.
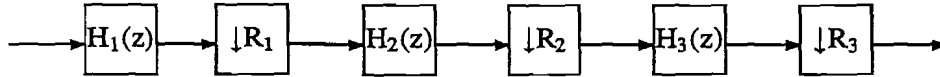

Figure 5.5: Sectioned decimating filter with downsampling factor $R = R_1 * R_2 * R_3$

The goal of the A/D-converter with variable resolution is, instead of having the three parallel decimating filters, to combine the filter sections as much as possible. Therefore a cascaded structure where the bands of interest are available at different places in the structure is investigated, see figure 5.6.
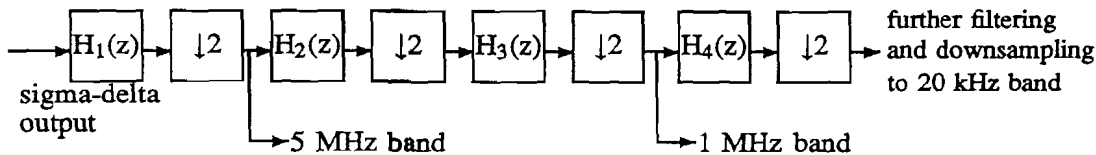

Figure 5.6: Cascaded decimation structure.

The decimating filter for the 20 kHz band forms the basis of this filter structure. The filter is split up in decimating sections with a downsampling factor of 2. Note that all the filters have to meet together the 0.2 dB ripple demand over the 20 kHz passband.

The first filters operate at the highest sample frequencies of the system (first filter at 20 MHz clock rate). Besides all this the attenuation of the following bands of interest has to be sufficient large to derive the required resolution. In the first filter also the 5 MHz band has to be filtered out. After the third section we have the same problem, a very small ripple, a small transition band (from 1 to 1.25 MHz) and sufficient attenuation for the 20 kHz band. This yields relative complex filters.

Direct partioning of the 20 kHz decimating filter with intermediate taps for the 5 MHz and 1 MHz bandwidth, doesn't yield relative simple filters. Especially the first filter in the string must have a large number of coefficients and has to operate at high speeds so it is expensive and very hard to realize. Also the following filter sections, just before each band is split up, must have complex coefficients thus their size will be large.

5.5 Adapted filter structure

To overcome the difficulties mentioned in the previous section a new filter structure has been designed as shown in figure 5.7.
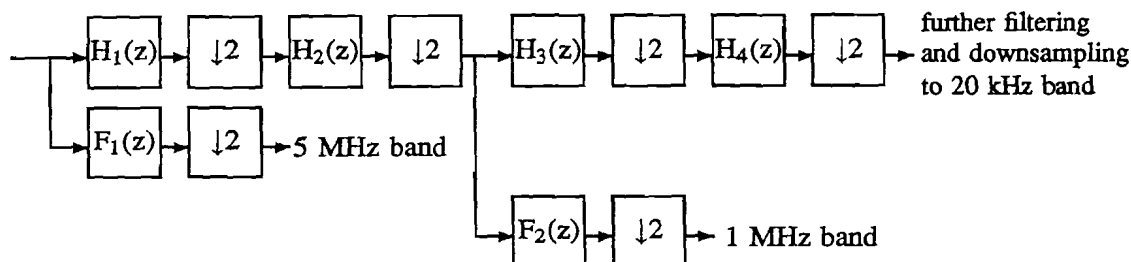

Figure 5.7: Adapted filter structure.

Each band now has a specific last downsampling section so that the specific demands of that band of interest can be realized without influencing the other bands. In this way the filter complexity reduces because the required stop-band attenuation is larger and not determined by the 20 kHz band. This structure has the following advantages :

- Minimum overlap
  (only two filters per band of interest are put in parallel.)

- Specific filter for each band of interest
  (this filter can exactly match the specifications of the band of interest.)

- Expandible
  (each other band of interest can be split off with an extra specific filter.)

We will now look how the decimating filters will be implemented and which filter types are used for the implementation of the decimating sections.

5.6 Filter types and their properties

The filter structure is completely designed with finite impulse response (FIR) filters. The use of FIR-filters in this structure implies :

- Linear phase can easily be designed.
  (a constant group delay is obtained)

- Round-off noise can be made small for nonrecursive structures.

- Stable.
  (no feedback loops in the filter)

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The FIR-filters are designed as equiripple filters, with a specified passband ripple δ_1 and a stopband ripple δ_2, see figure 5.8. With the design program DESFIR an optimum solution for the given number of filter coefficients is obtained. The program calculates the obtained passband ripple and stopband attenuation and the filter length has to be adapted until all requirements are met.
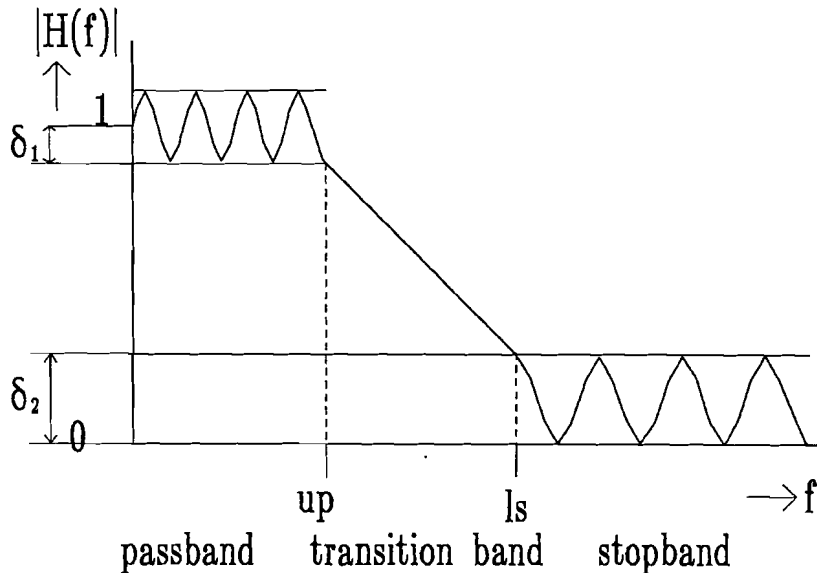

Figure 5.8: Example of low-pass filter with equiripple characteristic.

If we use an equiripple design, the given specifications have to be adapted, the specified ripple is namely given in dB's. We have to calculate the absolute allowed ripple δ_1. A ripple of -1 dB implies an absolute δ_1 of 0.10875 and a ripple of +1 dB 0.12202 . The used value for the ripple in the filter design program is the maximal allowed δ_1 adapted to the + dB value.

Where possible in the filter structure of figure 5.7 half-band filters are applied. These half-band filters form a special class of FIR-filters. In the filter structure of figure 5.7 $H_n(z)$ boxes and $F_n(z)$ boxes indicate were respectively half-band and normal FIR filter are used.

Half-band filters have the very important following advantages :

- Half of the coefficients are zero
  (all even coefficients except H(0))

- The chip area is relative small
  (due to efficient realization of less coefficients)

When using half-band filters all specifications have to be symmetric around one fourth of the sample frequency e.g. passband / stopband, passband ripple / stopband attenuation.

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When using figure 5.8 this means :

- $\delta_1 = \delta_2$

- $\pi/2 - \theta_l = \theta_h - \pi/2$

The performance of a special group of half-band filters is monotonic down [6]. This implies that the passband ripple increases with the passband length. At one fourth of the sample frequency the attenuation of a half-band filter is always -6 dB or 0.5. In figure 5.9 the transfer function of some of these special half-band filters is shown.
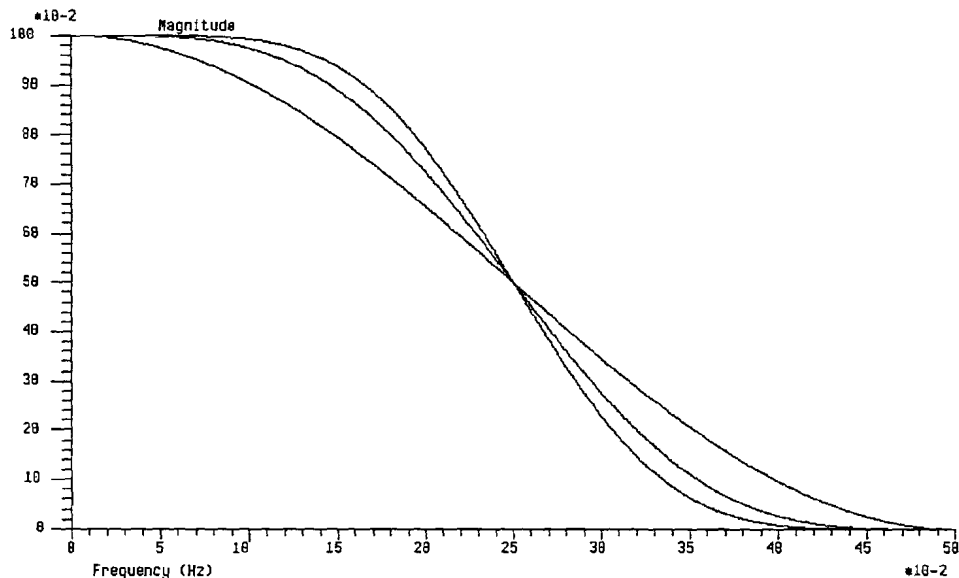

Figure 5.9: Monotonic amplitude responses of special class of half-band filters with lengths 3, 7 and 11.

In our application a monotonic amplitude response is ideally suited because the ripple in the lower band is always smaller and the attenuation at the end of the stopband is always larger. This matches exactly our specifications namely a higher resolution in the lower bands. Finally only the passband ripples of the individual half-band sections have to be added, to determine the total ripple at the end of the string before the FIR-filter. This will be the worst-case ripple and this in combination with the maximum FIR-filter ripple has to satisfy the ripple specifications for each band of interest. The total amplitude transfer function of the string at any place in the string will be monotonic down. Another advantage of using these specific half-band filters is the DC gain which is always 1.

5.7 Specifications of the individual filter sections

Now we have seen the filter types and their properties, the specifications of the filter-sections in the designed filter structure have to be derived. The complexity of the filters must also be remembered.

The 5 MHz band can not be realized. The downsampling factor of 2, on the original 20 MHz sampling frequency, implies a maximum signal bandwidth of 5 MHz (Nyquist criterion). But this is practical not realizable because of a zero transition bandwidth. Therefore the bandwidth has been restricted to 4.5 MHz which gives a transition bandwidth of 0.5 MHz.

The filter structure has to process the output spectrum of the sigma-delta modulator. As we know the quantization noise has been shaped to higher frequencies and a filter has to attenuate the high-frequency noise sufficiently so that the noise folded back during downsampling is below the baseband noise.
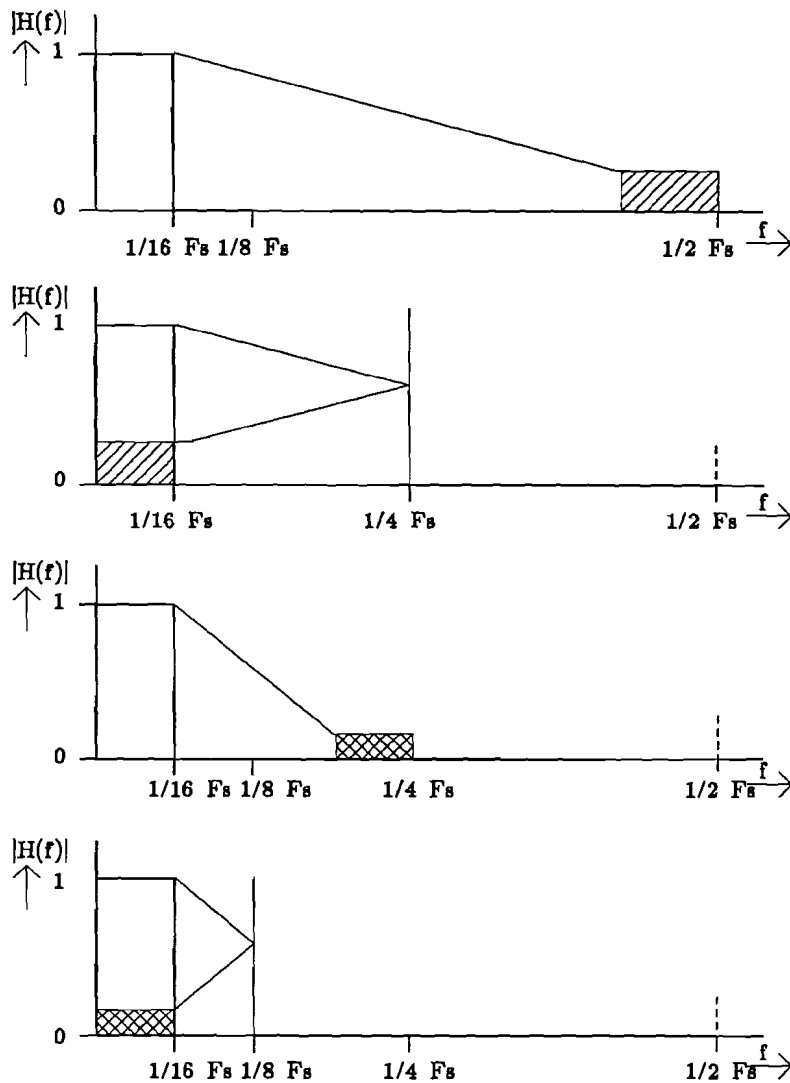

Figure 5.10: Quantization noise which is folded back during downsampling. This figure shows two successive downsampling operations.

Figure 5.10 shows the folding back during downsampling. The part of the spectrum that folds back is dashed in the first spectrum. The transfer function of the filter has to have sufficient attenuation so that the folded back part is below the baseband noise. This requires a relative large attenuation because the quantization noise is specially shaped to this part of the band. The second downsampling section in figure 5.10 has to attenuate the crossed band. This attenuation seems have a smaller value but in the spectrum above we see that in the crossed band already one time folding back of noise has taken place. The high-frequency noise can be strongly correlated in some circumstances. In a worst-case situation, it can be a single harmonic which occurs in the higher part of the frequency band. The attenuation has to be sufficiently large to eliminate the original and the one time folded back noise value when folded back in the baseband again in the second downsampling action. In this way each part of the original spectrum is one time folded back in the base band.

This means that the minimum stopband rejection of the filter has to be :

$$A_{stopband} = n * 6.02 + \text{safety margin} \qquad (5.1)$$

Where n is the number of extra resolution bits.
In our filters this will give the following minimum attenuation requirements :

- 4.5 MHz band $A_{stopband}$ 6.02 dB (8 bit, 1 additional bit)

- 1 MHz band $A_{stopband}$ 30.10 dB (12 bit, 5 additional bits)

- 20 kHz band $A_{stopband}$ 54.18 dB (16 bit, 9 additional bits)

The passband ripple has to satisfy the specifications mentioned already in section 5.1 :

- Passband Ripple < 0.2 dB DC to 100 kHz

- Passband Ripple < 1.0 dB 100 kHz to 4.5 MHz

With the filter-design program DESFIR all the filter sections have been designed. The most stringent ripple requirement is a 0.2 dB ripple in the 20 kHz band which also must have a 16 bit resolution.

Due to the advantages mentioned before, each filter section is preferably implemented by means of half-band filters. The half-band filters are designed to satisfy a very small ripple of 0.002 dB for the 20 kHz band which gives less stringent requirements for the last FIR-filter. Worst case for the 20 kHz band the passband ripple after 7 decimating half-band sections will be 0.014 dB so a 0.186 dB passband ripple in the last FIR filter is allowed.

By choosing this passband ripple the stopband attenuation of the half-band filters automatically equals -72 dB. This implies a maximum extra resolution of 11 bit according to equation 5.1. When using a 7 bit sigma-delta loop the maximum extra resolution needed is 9 bit to get 16 bit at 20 kHz so also that requirement will be satisfied. The extra attenuation can be used as margin to compensate other losses due to aliasing and truncation of the filter coefficients.

The filters H1 and H2 which satisfy the 20 kHz demands have been reviewed to see whether they also meet the 1 MHz band requirements. In the next section the realization

of the half-band filters, the specifications of the designed sections have been reviewed to see whether they satisfy the requirements or not.

filter	f_s	type	passband	ripple	stopband	attenuation
H1	20 MHz	hb	0 - 1 MHz	0.2 dB	9 - 10 MHz	-33 dB
H1	20 MHz	hb	0 - 20 kHz	0.002 dB	9.98 - 10 MHz	-72 dB
H2	10 MHz	hb	0 - 1 MHz	0.2 dB	4 - 5 MHz	-33 dB
H2	10 MHz	hb	0 - 20 kHz	0.002 dB	4.98 - 5 MHz	-72 dB
H3	5 MHz	hb	0 - 20 kHz	0.002 dB	2.48 - 2.50 MHz	-72 dB
H4	2.5 MHz	hb	0 - 20 kHz	0.002 dB	1.23 - 1.25 MHz	-72 dB
H5	1.25 MHz	hb	0 - 20 kHz	0.002 dB	605 - 625 kHz	-72 dB
H6	625 kHz	hb	0 - 20 kHz	0.002 dB	292.5 - 312.5 kHz	-72 dB
H7	312 kHz	hb	0 - 20 kHz	0.002 dB	136.25 - 156.25 kHz	-72 dB
F1	20 MHz	fir	0 - 4.5 MHz	1.0 dB	5 - 10 MHz	-8 dB
F2	5 MHz	fir	0 - 1 MHz	0.996 dB	1.25 - 2.5 MHz	-33 dB
F3	156 kHz	fir	0 - 20 kHz	0.186 dB	39 - 78.125 kHz	-57 dB

Table 5.1: Specification requirements for the individual filter sections.

The FIR-filters have been designed with a larger attenuation than required to allow a margin for degrading effects such as coefficient word length, truncation and aliasing.

5.8 Specifications of the individual half-band filter sections

With these specifications, the dipro program DESFIR has been used to determine the number of coefficients and the response of the individual filter sections. After truncating the filter coefficients to finite word length, the following filter parameters are obtained (table 5.2).

filter	# coef	passband	ripple[dB]	stopband	attenuation
H1	3	0 - 1 MHz	0.215	9 - 10 MHz	-32 dB
H1	3	0 - 20 kHz	0.00009	9.98 - 10 MHz	-100 dB
H1	7	0 - 1 MHz	0.0154	9 - 10 MHz	-55 dB
H1	7	0 - 20 kHz	$< 10^{-5}$	9.98 - 10 MHz	-190 dB
H2	3	0 - 1 MHz	0.875	4 - 5 MHz	-19.5 dB
H2	3	0 - 20 kHz	0.00035	4.98 - 5 MHz	-88 dB
H2	7	0 - 1 MHz	0.22	4 - 5 MHz	-31.5 dB
H2	7	0 - 20 kHz	$< 10^{-5}$	4.98 - 5 MHz	-166 dB
H3	7	0 - 20 kHz	0.00006	2.48 - 2.5 MHz	-142 dB
H4	7	0 - 20 kHz	0.00011	1.23 - 1.25 MHz	-118 dB
H5	7	0 - 20 kHz	0.00017	605 - 625 kHz	-94 dB
H6	7	0 - 20 kHz	0.00027	292.5 - 312.5 kHz	-70 dB
H7	7	0 - 20 kHz	0.04	136.25 - 156.25 kHz	-46 dB
H7	11	0 - 20 kHz	0.0052	136.25 - 156.25 kHz	-64 dB

Table 5.2: Designed half-band filter sections with truncated coefficients.

From this table it can be concluded that the first half-band filter H1 can be realized with three coefficients and H2 - H6 with seven. When H2 is realized with three coefficients this yields a too large passband ripple and a too small stopband attenuation of the 1 MHz band. Due to the fact that half-band filters are used, H2 - H6 are realizable with only five coefficients because two coefficients are zero. For H7 we need eleven coefficients of which only seven have to be realized. The first section has the fewest number of coefficients due to the fact that it has the largest transition band.

The ripple at the output is obtained by adding the individual half-band filter ripples as tabulated in table 5.3. In this table also the number of bits necessary to realize the filter coefficients is given.

filter	type	# coef.	coefficient word length	passband	ripple [dB]	total ripple in passband [dB]
H1	hb	3	2	0 - 1 MHz	0.215	0.215
H2	hb	7	5	0 - 1 MHz	0.22	0.435
H1	hb	3	2	0 - 20 kHz	0.00009	0.00009
H2	hb	7	5	0 - 20 kHz	$< 10^{-5}$	0.00009
H3	hb	7	5	0 - 20 kHz	0.00006	0.00015
H4	hb	7	5	0 - 20 kHz	0.00011	0.00026
H5	hb	7	5	0 - 20 kHz	0.00017	0.00043
H6	hb	7	5	0 - 20 kHz	0.00027	0.00070
H7	hb	11	9	0 - 20 kHz	0.0052	0.00590

Table 5.3: Passband ripples of the individual half-band filters and the total ripple at the 1 MHz and 20 kHz outputs.

The coefficients of the half-band filter sections are chosen in such a way that they have the least ones in two's complement. This has the advantage that only a few adders have to be realized when constructing a multiplier in hardware. This has to be done for almost all filter sections due to the fact that they operate at such a high sampling frequency that the multiplications and summations can't be done with a processor architecture. In the next chapter an estimation of the chip area of each filter section will be made. Without precautions the data word length will increase rapidly which is also discussed in the next chapter.

5.9 Specifications of the individual FIR-filter sections

The FIR filter sections which have to match the specifications of table 5.1, are also found with the dipro program DESFIR. The acquired values of the filter coefficients have to be truncated to such a number of bits that the filter still meets the specifications. In table 5.4 the performance of the designed filters with the truncated coefficient word lengths are given. The number of bits of the truncated filter coefficients are also given.

filter	# coef	coefficient word length	passband	ripple [dB]	stopband	attenuation [dB]
F1	16	8	0 - 4.5 MHz	1.0	5 - 10 MHz	-8
F2	23	9	0 - 1 MHz	0.9	1.25 -2.5 MHz	-32
F3	21	11	0 - 20 kHz	0.182	39.00 - 78.125 kHz	-57.9

Table 5.4: Designed FIR-filter sections.

Due to an error in specification of the allowed ripple of the FIR-filter F2 a too large ripple occurs in the 1 MHz band between 990 kHz and 1 MHz. Because of time limitations this has not yet been adapted.

5.10 Decimating passband transfers for the 4.5 MHz, 1 MHz and 20 kHz band

In figure 5.11 the transfer function of FIR-filter F1 with truncated coefficients is shown.

The attenuation of the stopband carried out by a half-band filter would not be sufficient to meet the original specifications of the 4.5 MHz band so the use of a FIR-filter is necessary (see section 5.7).
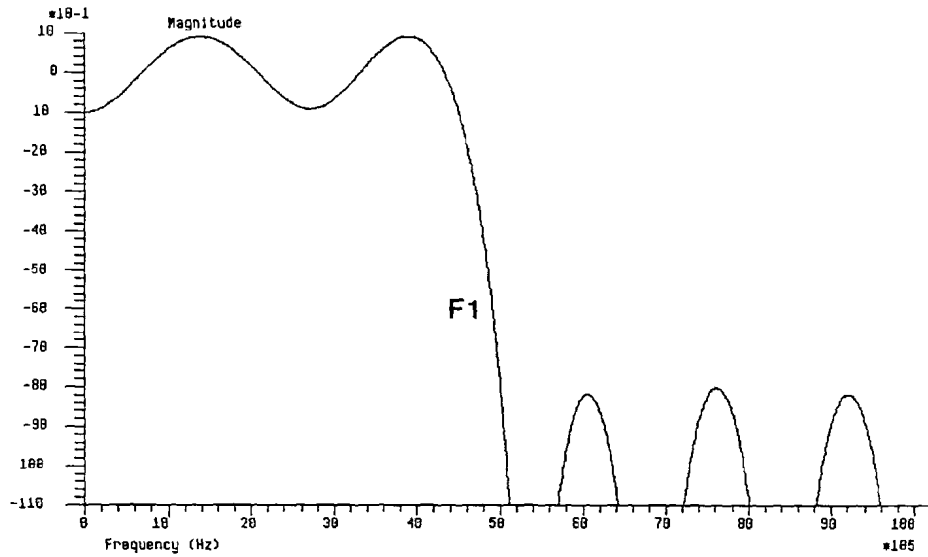
**Figure 5.11:** Transfer function of F1.
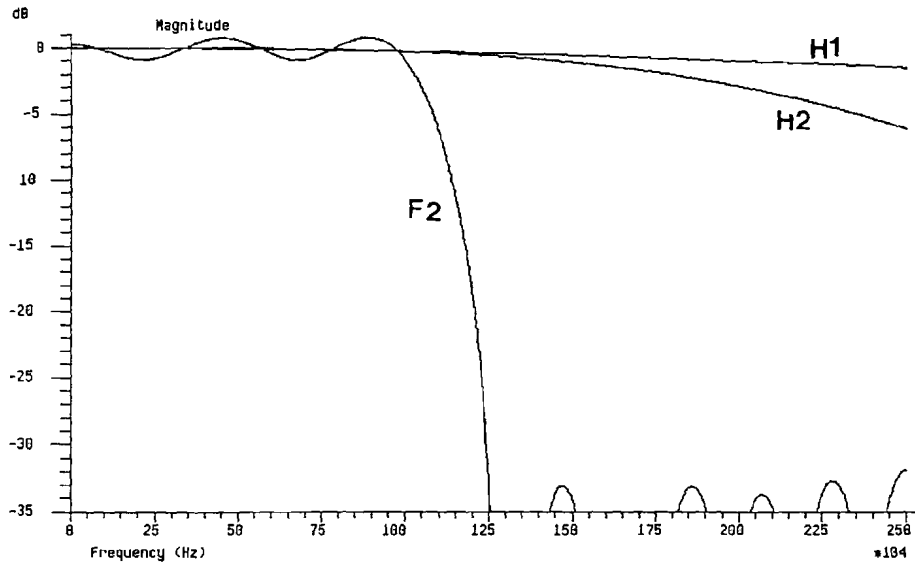
Figure 5.12: Transfer functions of H1, H2 and F2.

The 1 MHz band decimating path consists of the filter sections H1, H2 and F2. Their transfers functions are depicted in figure 5.12.

Figure 5.13 depicts the transfer function of the FIR-filter F3 and half-band filters H1 - H7.

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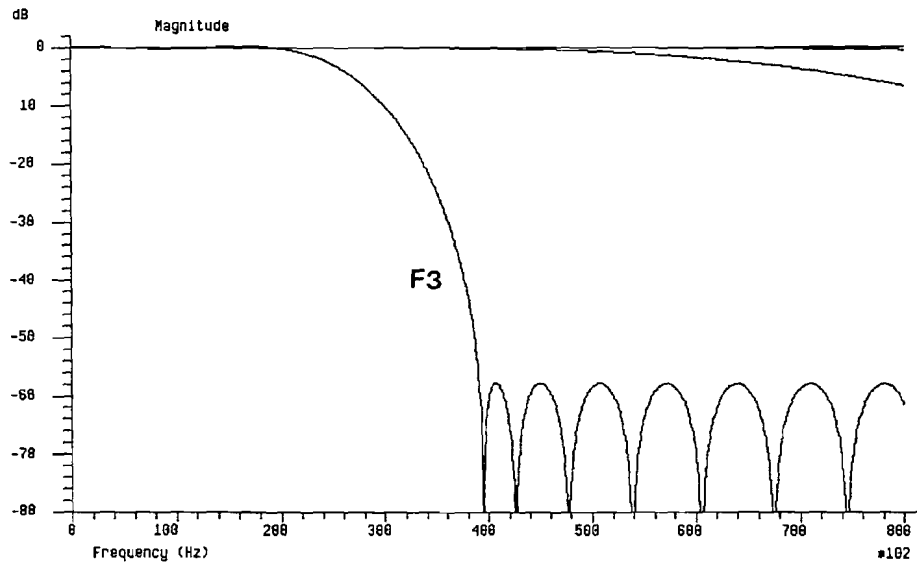
Figure 5.13: Transfer functions of FIR-filter F3 and half-band filters H1 - H7.

We now have seen that all filter sections meet the individual specifications. The use of individual FIR-filters for each band proved to be an elegant solution.

5.11 First simulation results using the sigma-delta modulator with decimating filters

With the mixed-mode level simulator MILES the ideal ADC system has been simulated. A sine generator supplies a sine wave of 10 kHz and an amplitude of 0.7447 Volt which is applied to the first-order sigma-delta loop with the decimating filter. (Maximum input voltage is 1 V so 0.7447 V is - 2.56 dB.)

A Fourier transformation is performed on the simulation results which yields the spectra of the individual outputs and the signal-to-noise ratio can be determined. The noiseband width is by definition equal to half of the actual sample frequency. Table 5.5 gives the S/N results for the 10 kHz sine wave at -2.56 dB at the various filter outputs.

filter	passband	noiseband	S/N ratio
F1	0 - 4.5 MHz	0 - 5 MHz	44.0 dB
F2	0 - 1 MHz	0 - 1.25 MHz	65.7 dB
F3	0 - 20 kHz	0 - 39 kHz	113.9 dB

Table 5.5: Simulated S/N ratios at the different decimating filter outputs. Input frequency is 10 kHz, amplitude -2.56 dB, 50 periods.

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This table must be compared with the theoretical values from section 4.4 which are :

- 5 MHz band : requested 8 bit resolution (48 dB)
  theoretical dynamic range 48.26 dB

- 1 MHz band : requested 10 bit resolution (60 dB)
  theoretical dynamic range 68.75 dB

- 20 kHz band : requested 16 bit resolution (96 dB)
  theoretical dynamic range 119.73 dB

Now we see that the simulation results differ from the theoretical values due to the gain of the filters and the input signal level. The transfer function of the filters for an input signal of 10 kHz influences the results. The gain or attenuation for 10 kHz can be determined.

band	filters	total gain at 10 kHz
4.5 MHz	F1	- 1.0 dB
1 MHz	H1 H2 F2	+ 0.315 dB
20 kHz	H1- H7 F3	- 0.007 dB

Table 5.6: Individual transfer for 10 kHz signal.

Now a recalculation of the dynamic range is performed. We add 2.56 dB extra at the simulation values due to the fact that a -2.56 dB input signal level was taken during the simulations. The recalculated values are listed in table 5.7.

S/N ratio filter out [dB]	attenuation of filters [dB]	input correction [dB]	dynamic range with filters[dB]	required S/N ratio [dB]
44.0	-1.0	2.56	47.6	48.0
65.7	+0.315	2.56	67.9	60.0
113.9	-0.007	2.56	116.4	96.0

Table 5.7: Simulated dynamic range for each individual band.

At the output of the sigma-delta loop, the S/N ratio has also been calculated. The differences found between the theoretical values and both sigma-delta output and filter output are also given. Dif 1 is the difference between theoretical and sigma-delta output and dif 2 is between theoretical and the filter output.

total S/N ratio sigma-delta_out [dB]	total S/N ratio filters_out [dB]	theoretical S/N ratio [dB]	dif 1 [dB]	dif 2 [dB]
48.36	47.6	48.26	+0.1	-0.7
68.93	67.9	68.75	+0.15	-0.8
125.76	116.4	119.73	+6.0	-3.3

Table 5.8: Comparision of the S/N ratios of theoretical model and simulations at the sigma-delta output and the filter output.

The specifications of the 4.5 MHz band are not met anymore. We now see that all S/N ratios at the decimating outputs have decreased. This is also due to the noiseband definition which gives the noiseband width to half the actual sample frequency. In the theoretical values only the signalband width was used assuming ideal low-pass filters. The results further indicate that for both the 1 MHz and 20 kHz band, the requirements are met.

5.12 Preliminary conclusions

After the first simulations the proposed filter structure seems to meet the specifications.

- The proposed filter structure is easy to expand for other bands of interest but each other band will need a special FIR filter.

- The implementation of the used half-band filters will be relatively easy. These filters have very few coefficients which contain less ones. This makes them realizable in hardware without taking too much die area.

- The FIR filter used for the 4.5 MHz band will be very hard to realize : it has a small transition band, it works at 20 MHz and contains relative much coefficients with many bits. Also the profit of noise shaping is very small due to the low oversampling factor.

- The other two FIR filters (for 1 MHz and 20 kHz) are less complex.

- The preliminary simulations yield satisfactory results for all bands except the 4.5 MHz band.

Chapter 6

Realization of the decimating filters

6.1 Introduction

In this chapter we will look in which way the designed filter structure can be implemented. In the previous chapter we have already limited the length of the filter-coefficients and now we will look at finite word length in the filters. We will design the filter sections and after completing the design, the chip area for two IC processes will be estimated. Finally the first simulation results of the to word length adapted design, will be presented.

6.2 Finite word length effects in the different filter sections

When we are realizing the filter structure, we see that the number of data bits increases very rapidly and thus we have to limit this number. In figure 6.1 we see the realization of the designed second-order half-band filter with coefficients 1/4, 1/2 and 1/4. We see that the seven bits which will come out of the multi-bit sigma-delta loop increase to nine bit at the output of this first filter section.

The next figure depicts a possible realization for the H2 filter which is a 6'th order half-band filter with coefficients - 1/32, 9/32, 1/2, 9/32 and - 1/32. We see an increase of six bits at the original number of nine. The negative filter coefficients are realized by first inverting the bits and then add a 1. (Two's complement logic) This is why an extra adder will need to be included (see figure 6.4).
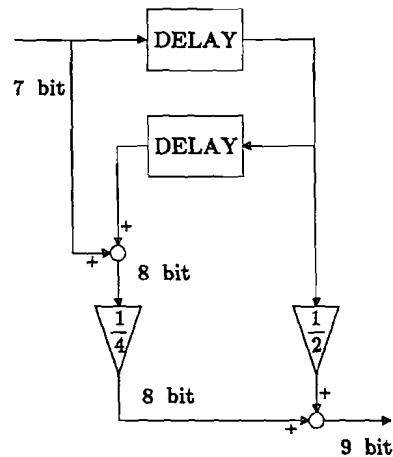
Figure 6.1: Realization of the 2nd-order half-band filter H1 with coefficients 1/4, 1/2 and 1/4. The coefficients 1/4 and 1/2 are realized by means of hard-wired bit-shifts.
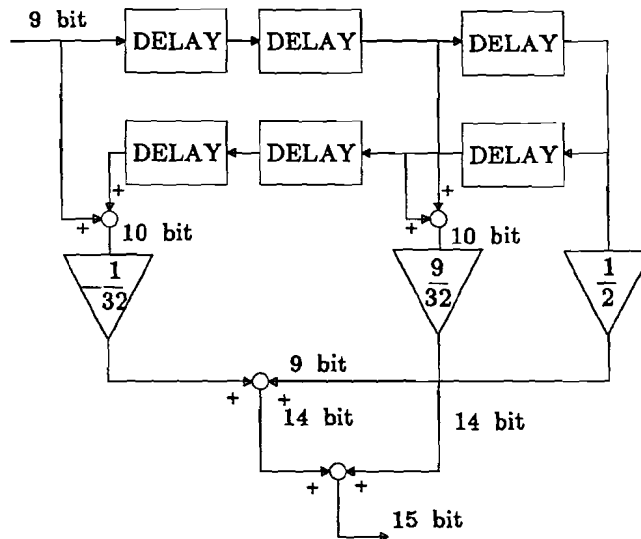

Figure 6.2: Sixth order half-band filter H2 with calculated word lengths at 9 bit input word length

When we decrease the number of bits we will also limit the number of components used in the filters. The length of the adders and registers will decrease, hence the size of the filters will be much smaller.

When we limit our word length at the filter outputs we introduce a quantization error or so called round-off noise which is depicted in figure 6.3.
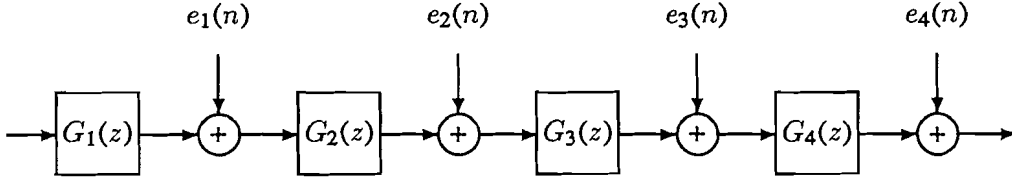
Figure 6.3: Introduction of round-off noise by truncation of the data word length in the decimating filters.

We now must calculate the influence of the round-off noise in the system. We presume uniform white noise which has a baseband power of $\frac{2f_b}{f_s}\frac{q^2}{12}$. When decimating filters are used the folded back part is suppressed with the stopband attenuation of the filter. The attenuation is always much larger than the downsampling factor so the influence of this noise can be ignored. The transfer function of each round-off noise, e_n is :

$$\varepsilon_n^2 = \frac{1}{\pi} \int_0^{\theta_1} \frac{q_{s_n}^2}{12} \prod_{j=n}^{n_{max}} G_j(\theta)\, d\theta \tag{6.1}$$

Where q_{s_n} is the number of quantization bits at filter output n and θ_1 is the normalized baseband frequency. This gives an total noise at the output of the system of :

$$\sigma_{total}^2 = \sum_{i=1}^{n_{max}} \varepsilon_i^2 = \sum_{i=1}^{n_{max}} \left(\frac{1}{\pi} \int_0^{\theta_{1_i}} \frac{q_{s_i}^2}{12} \prod_{j=i}^{n_{max}} G_j(\theta)\, d\theta \right) \tag{6.2}$$

The noise due to the round-off actions can now be calculated for each band of interest. We have to vary the transfer function for the 1 MHz and the 20 kHz band due to the different number of sections and the specific FIR-filters. For the 5 MHz band we only have one filter section so we don't round-off in the filter. Only the quantization error at the end of the filter has to be counted. Further θ varies due to the change of sample frequency. $(\theta_{1_i} = \frac{2\pi f_b}{f_{s_i}})$ Now we assume the transfer function $G_j(\theta)$ to be 1 in the baseband then equation 6.2 becomes :

$$\sigma_{total}^2 = \sum_{i=1}^{n_{max}} \frac{1}{\pi} \int_0^{\theta_{1_i}} \frac{q_{s_i}^2}{12}\, d\theta \tag{6.3}$$

This gives :

$$\sigma_{total}^2 = \sum_{i=1}^{n_{max}} \frac{1}{\pi} \frac{q_{s_i}^2}{12} \theta_{1_i} \tag{6.4}$$

When we use this for our 1 MHz band we have three contributions :

$$\sigma_{total}^2 = \left(\frac{q_{s_{F2}}^2}{12} \frac{f_{b1MHz}}{f_{s_{F2}}} + \frac{1}{2}\frac{q_{s_{H2}}^2}{12} \frac{f_{b1MHz}}{f_{s_{F2}}} + \frac{1}{4}\frac{q_{s_{H1}}^2}{12} \frac{f_{b1MHz}}{f_{s_{F2}}} \right) \tag{6.5}$$

and for our 20 kHz band :

$$\sigma_{total}^2 = \left(\frac{q_{s_{F3}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{2}\frac{q_{s_{H7}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{4}\frac{q_{s_{H6}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{8}\frac{q_{s_{H5}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} \right.$$
$$\left. + \frac{1}{16}\frac{q_{s_{H4}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{32}\frac{q_{s_{H3}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{64}\frac{q_{s_{H2}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} + \frac{1}{128}\frac{q_{s_{H1}}^2}{12} \frac{f_{b20k}}{f_{s_{F3}}} \right) \tag{6.6}$$

We now see that if we not limit the first half-band filter and further quantize half-band section H2, at 15 bit, H3 and H4 at 16 bit and H5, H6 and H7 at 17 bit, we will meet the demands. We use an overdimensioned quantizer at the last FIR-filter output of one bit more than the demanded resolution.

- 4.5 MHz band : 9 bit quantizer

- 1 MHz band : 13 bit quantizer

- 20 kHz band : 17 bit quantizer

This design which we have used, is not yet fully optimized but satisfactory for a first indication of the possibilities. Recalculations showed that the minimal required word lengths are 15 bit for H2 and H3, 16 bit for H4 and H5 and 17 bit for H6 and H7.

6.3 Simulations with word length truncation

We now have simulated the 7-bit first-order sigma-delta loop together with the designed filter structure with truncated data word length. Again an input sine wave of 10 kHz has been used at -2.56 dB input level and the number of simulated periods was 50. The results are shown in table 6.1 :

S/N ratio filter out [dB]	input correction [dB]	total S/N ratio filters_out [dB]	requested S/N ratio [dB]	difference [dB]]
42.14	3.56	45.70	48.0	-2.3
65.67	2.24	67.91	60.0	+7.9
94.34	2.56	96.90	96.0	+0.9

Table 6.1: Simulated S/N ratios at the filter outputs and comparison with requirements.

The resolution of the 20 kHz band has become 16 bit and the 1 MHz band 11 bit. This is both within the specifications. The 4.5 MHz band doesn't reach the requested 8 bit resolution. As seen in simulations with the designed filters with infinite word length, the dynamic range was 47.5 dB which was already a little bit too small.

6.4 Chip area estimation of the filter implementation

We now will look at the consequences of the word length restriction in the filters on the chip area occupied by the filters. First the number of components of each filter section will be determined. Next the size of the used components will be given and then we will give the chip area estimation.

6.4.1 Number of components

When using the H1 filter of figure 6.1 for an estimation of our number of components. We need two 7-bit registers and we need an adder for two 7-bit words. This adder is built of 1 half adder and 6 full adders. The multiplications in the filter are done by shifting bit-lines thus adding the appropriate scaled bits. We then need an adder for a 7-bit word and a shifted 8-bit word which will consist of 5 full adders and 2 half adders.

Then the total number of components equals :

- 14 registers

- 11 full adders

- 3 half adders

The universal sixth order filter, shown in figure 6.4, will use six register blocks of the incoming word and adders. The multiplications done in this section have the coefficients 1/2, 9/32 and - 1/32. To realize the negative sign multiplication we have to invert all the bits and add a 1, due to the fact that two's complement logic is used. The factor 9/32 is realized by adding the word multiplied with 1/32 and 1/4 (bit shifts).
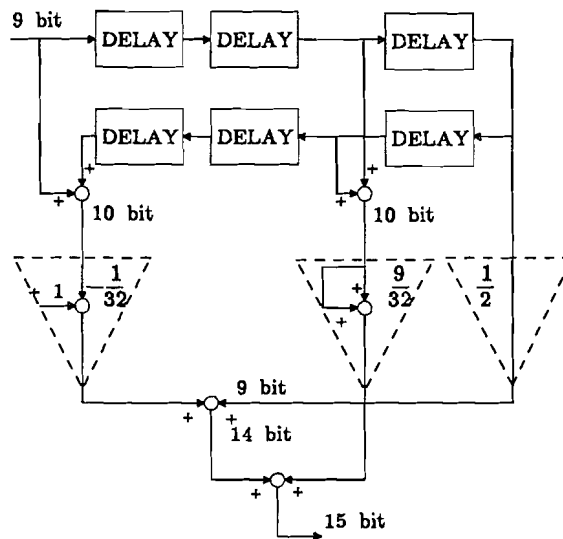
Figure 6.4: Sixth order half-band filter H2.

When looking for the first sixth order section we need in our filter structure we have a 9 bit input word. We see that we need first two nine bit adders consisting of 8 full adders and 1 half adder. To realize the factor - 1/32 we need 10 inverters and a 10 half adders. To add 1/4 and 1/32 we use 4 half adders and 6 full adders. In adding - 1/32 and 1/2 we use 4 full and 5 half adders and in the final stage we use two half adders and 12 full adders.

Then the total number of components equals :

- 54 registers

- 38 full adders

- 23 half adders

- 10 inverters

Also the other sixth order sections are calculated in this way. We have limited the word length after filter section H2 at 15 bit, after H3 and H4 at 16 bit and after H5 - H7 at 17 bit. The other estimations of the number of components are performed in appendix B.

6.4.2 Size of components

All the used components are available in our component library. The chip area sizes of the basic components in C3DM process equal :

- full adders
  117.6 * 70.4 μm

- half adders
  71.2 * 70.4 μm

- registers
  64.0 * 70.4 μm

- inverters
  19.2 * 70.4 μm

The half adders are built of one EXOR gate and one AND gate. After using the size of the components we multiply the area estimation with a factor 2 for wire routing overhead. The estimated size for each filter section equals :

Filter factor	Order and Type Filter	Size Filter
H1	2 order hb filter	0.34 mm^2
H2	6 order hb filter	1.37 mm^2
H3	6 order hb filter	2.32 mm^2
H4	6 order hb filter	2.42 mm^2
H5	6 order hb filter	2.57 mm^2
H6	6 order hb filter	2.57 mm^2
H7	10 order hb filter	5.61 mm^2
F1	15 order fir filter	6.29 mm^2
F2	22 order fir filter	19.50 mm^2
F3	20 order fir filter	11.84 mm^2

Table 6.2: Estimated sizes of the filter sections

This gives a total filter size of :

- Total filter 54.8 mm^2 process C3DM

- Total filter 21.4 mm^2 process C200

The new process C200 which was used in the second total estimation is a downscale of the C3DM process by a linear factor of 1.6 which gives a square reduction of 2.56 ! This new process will make the filter structure more attractive for realization.

6.5 Conclusions

The designed filter structure has been given a finite word length which has not been completely optimized but is sufficient to provide first simulation results and an area estimation. The first simulation results meet the specifications of the 1 MHz band and the 20 kHz band.

In the process technology C3DM the size of the filter structure is so large that the expected yield in fabrication is very low. The filter structure will be realizable in the new process C200 but will still be very large. Most of the area will be occupied by the FIR filters.

If we want to make our complete design, both sigma-delta loop and filter structure, the size will be large even in C200 process. The size of a 7-bit A/D converter and a 7-bit D/A converter and the first order filter used in the designed sigma-delta loop gives a die area of approx 6 mm^2. Thus we need 28 mm^2 in C200 process for the realization of the A/D converter.

Chapter 7

Conclusions

A system design of a 7-bit first-order sigma-delta A/D-converter has been made. This design matches all the requirements specified by the product division Test & Measurement for the 1 MHz band and the 20 kHz band. The 5 MHz band can't be realized and for used 4.5 MHz band the requirements are almost met.

In the realization of the design, the required multi-bit D/A-converter in the feedback loop has to yield at least 16 bit linearity specification which is difficult to realize.

Further a filter structure has been designed which has proved to be able to filter out different bands of interest at variable resolution. In the filter structure half-band filters with a monotonic down amplitude response have been used. These filters are ideally suited for variable resolution for they have the highest attenuation of the part of the frequency band that will fold back in the baseband. The increase of passband ripple at larger passbands contributes also to their suitability.

The use of individual FIR-filters in each last decimating filter is an elegant solution but still relative complex filters have to be used. Due to this fact the die size of these filters will become relative large, according to a first estimation which has been done. The filter structure consisting of only half-band filters is relative small. The flexibility of the structure is limited due to the specific FIR-filters.

The complete design will be large even in C200 process so further research has to be done to realize smaller FIR-filters and to the possibility of realizing filters not in hardware but in a processor architecture. The die area for that solution also has to be investigated. The realization of a 7-bit D/A-converter with 16-bit linearity is also a point of further research.

In total the main problem in the design is the fact that all heaviest requirements have to be met within all demands. The 5 MHz band requires a multi-bit quantizer which has to satisfy the linearity requirements of the 20 kHz band.

Further research has to be done to the analogue realization of the sigma-delta loop. Special attention has to be paid to noise performance, accuracy and maximum allowed non-linearities in the flash A/D.

Bibliography

[1] R.J.v.d.Plassche, *High-speed and high-resolution analogue-to-digital and digital-to-analogue converters*, Ph.D thesis, University of Technology Delft, 1989.

[2] L.R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*, Englewood Cliffs NJ: Prentice-Hall, 1975.

[3] E.F.Stikvoort, *Some remarks on the stability and performance of the noise-shaper or sigma-delta modulator*, IEEE Transactions on Communications, Vol.36, no.10, Oct. 1988.

[4] P.J.A. Naus and E.C. Dijkmans, *Low signal-level distortion in Sigma-Delta modulators*, 84th AES convention, Preprint 2584, March 1988, Paris.

[5] P.J.A. Naus and E.C. Dijkmans, *Multi-bit oversampled A/D converters as front-end for CD players*, IEEE J.Solid-State Circuits, Vol.26, No.7, July 1991.

[6] D.J. Goodman, M.J. Carey, *Nine digital filters for decimation and interpolation*, IEEE Transactions on ASSP, Vol.25, No.2, April 1977.

[7] A. v.d. Enden, N.A.M. Verhoeckx, *Digitale signaalbewerking*, Delta Press B.V., 1987

[8] P.R. Gray, R.G. Meyer, *Analysis and design of analog integrated circuits*, second edition 1984, John Wiley & Sons, Inc.

[9] B.P. Brandt, B.A. Wooley, *A CMOS Oversampling A/D converter with 12-bit resolution at conversion rates above 1 MHz*, ISSCC 1990.

[10] B.E. Boser, B.A. Wooley, *The design of sigma-delta modulation analog-to-digital converters*, J. Solid-State Circuits, Vol. SC-23, No. 6, pp. 1289–1308, Dec. 1988.

[11] M.T.W.M. Valks, *User manual for DIPRO version 3.1*, Nat. Lab. report, No. 5975, Aug. 1983.

[12] M.F.J. van Haperen, G.J.J.M. van de Ven, *MILES: mixed level simulation for analog/digital design*, Nat. Lab. report, April 1991.

Appendix A

designed FIR filter 4.5 MHz band

```
*************** INPUT SUMMARY ***********************************

        sample frequency    =         20000000.00 Hz
        filter length       =                  16
        number of bands     =                   2
        grid density        =                  16
        type of filter      = multiple pass/stopband
        impulse response    =            symmetrical
BAND 1: passband startfr.=           0.00 Hz,      gain =    0.00 dB
             stopfr. =     4500000.00 Hz,    ripple = 0.8967 dB
BAND 2: stopband startfr.=   5000000.00 Hz,
             stopfr. = 10000000.00 Hz,max. gain =   -8.00 dB
*****************************************************************

                 FINITE IMPULSE RESPONSE (FIR)
              LINEAR PHASE DIGITAL FILTER DESIGN
                  REMEZ EXCHANGE ALGORITHM

                       bandpass filter

               FILTER LENGTH =    16

            ***** IMPULSE RESPONSE *****
            h(   1) = -0.40018205E-02 = h(  16)
            h(   2) = -0.13056873E+00 = h(  15)
            h(   3) =  0.11465240E+00 = h(  14)
            h(   4) =  0.24169683E-01 = h(  13)
            h(   5) = -0.89040458E-01 = h(  12)
            h(   6) = -0.70437014E-01 = h(  11)
            h(   7) =  0.16920713E+00 = h(  10)
            h(   8) =  0.43190104E+00 = h(   9)
```

```
*****   OBTAINED PASSBAND RIPPLE OR STOPBAND GAIN IN dB      *****
** In case of freq. dependent specification in a single band, **
** the data is valid at the LOWER edge of the freq. band.     **
         BAND  1        BAND  2
         0.8926        -8.0411


EXTREMAL FREQUENCIES--MAXIMA OF THE ERROR CURVE
    0.0000000   0.0703125   0.1367187   0.1953125   0.2250000
    0.2500000   0.3007812   0.3789062   0.4609375
```

designed FIR filter 1 MHz band

```
************** INPUT SUMMARY ******************************

        sample frequency   =          5000000.00 Hz
        filter length      =               23
        number of bands    =                2
        grid density       =               16
        type of filter     = multiple pass/stopband
        impulse response   =          symmetrical
BAND 1: passband startfr.=        0.00 Hz,     gain =   0.00 dB
               stopfr. = 1000000.00 Hz,    ripple = 0.8934 dB
BAND 2: stopband startfr.= 1250000.00 Hz,
               stopfr. = 2500000.00 Hz,max. gain = -33.00 dB
*****************************************************************
                FINITE IMPULSE RESPONSE (FIR)
              LINEAR PHASE DIGITAL FILTER DESIGN
                 REMEZ EXCHANGE ALGORITHM


                    bandpass filter
                FILTER LENGTH =    23


            ***** IMPULSE RESPONSE *****
         h(    1) =   0.28506592E-01 = h(   23)
         h(    2) =   0.30267654E-01 = h(   22)
         h(    3) =  -0.15990846E-02 = h(   21)
         h(    4) =  -0.34649149E-01 = h(   20)
         h(    5) =  -0.14255858E-01 = h(   19)
         h(    6) =   0.38786065E-01 = h(   18)
         h(    7) =   0.33115633E-01 = h(   17)
         h(    8) =  -0.52540015E-01 = h(   16)
         h(    9) =  -0.90128608E-01 = h(   15)
         h(   10) =   0.53548690E-01 = h(   14)
         h(   11) =   0.30942598E+00 = h(   13)
         h(   12) =   0.43944293E+00 = h(   12)
*****  OBTAINED PASSBAND RIPPLE OR STOPBAND GAIN IN dB    ******
**  In case of freq. dependent specification in a single band,  **
**  the data is valid at the LOWER edge of the freq. band.     **
         BAND   1        BAND   2
          0.7971         -34.0405

EXTREMAL FREQUENCIES--MAXIMA OF THE ERROR CURVE
   0.0416667    0.0911458    0.1354166    0.1770834    0.2000000
   0.2500000    0.2630208    0.2942707    0.3333330    0.3723954
   0.4140619    0.4583325    0.5000000
```

designed FIR filter 20 kHz band

```
*************** INPUT SUMMARY ************************************

        sample frequency    =             156125.00 Hz
        filter length       =                    21
        number of bands     =                     2
        grid density        =                    16
        type of filter      = multiple pass/stopband
        impulse response    =              symmetrical
BAND 1: passband startfr.=          0.00 Hz,      gain =         0.00 dB
               stopfr. =    20000.00 Hz,      ripple =       0.1800 dB
BAND 2: stopband startfr.=    39062.50 Hz,
               stopfr. =    78062.50 Hz,max. gain =        -58.00 dB
****************************************************************
                FINITE IMPULSE RESPONSE (FIR)
                LINEAR PHASE DIGITAL FILTER DESIGN
                   REMEZ EXCHANGE ALGORITHM


                      bandpass filter


                  FILTER LENGTH =    21


                 ***** IMPULSE RESPONSE *****
             h(   1) = -0.22722837E-02 = h(   21)
             h(   2) = -0.68905472E-03 = h(   20)
             h(   3) =  0.96982811E-02 = h(   19)
             h(   4) =  0.21370417E-01 = h(   18)
             h(   5) =  0.11820321E-01 = h(   17)
             h(   6) = -0.27717786E-01 = h(   16)
             h(   7) = -0.60113255E-01 = h(   15)
             h(   8) = -0.19520765E-01 = h(   14)
             h(   9) =  0.11759289E+00 = h(   13)
             h(  10) =  0.28216976E+00 = h(   12)
             h(  11) =  0.35650000E+00 = h(   11)
*****   OBTAINED PASSBAND RIPPLE OR STOPBAND GAIN IN dB      ******
** In case of freq. dependent specification in a single band,  **
** the data is valid at the LOWER edge of the freq. band.      **
        BAND  1          BAND  2
         0.1820          -57.9020


EXTREMAL FREQUENCIES--MAXIMA OF THE ERROR CURVE
   0.0000000    0.0596591    0.1079545    0.1281025    0.2502002
   0.2615638    0.2871319    0.3240637    0.3666773    0.4092909
   0.4547454    0.5000000
```

Appendix B

Area estimations
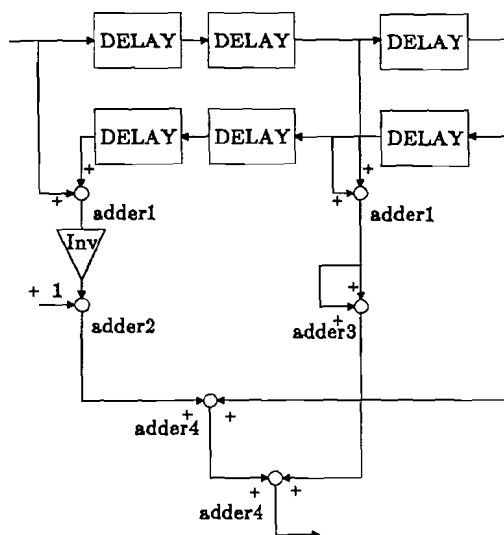
Figure 7.1: Realization a filter : adder1 symbolizes the first adding, adder2 symbolizes the adding needed after inverting, adder3 symbolizes the adding of two 1 bit shifted words, adder4 symbolizes all other addings on the maximum number of bits.

```
******  Size of the components in C3DM process  *****

          width                length
# registers        64.0          70.4
# full adders     117.6          70.4
# half adders      71.2          70.4
# inverters        19.2          70.4

( all sizes in micro meter  (10e-6 m) )
```

Half-band filter H1

```
***** 2 order half-band filter 7 bit input word *****

registers 2x 7 bit
adder1     1x          6 full 1 half
adder                  5 full 2 half
# registers     14              896.0
# full adders   11             1293.6
# half adders    3              213.6
# inverters      0
                            ---------
Total width                   2403.2
Lenght                          70.4
Routing factor                   2.0
Total area                      0.34 mm2
```

Half-band filter H2

```
***** 6 order half-band filter 9 bit input word *****
registers 6x  9 bit
adder1    2x  9 bit    8 full 1 half
inverters 1x 10 bit
adder2    1x 10 bit           1 half
adder                  6 full 4 half
adder                  4 full 5 half
adder                 12 full 2 half
# registers     54             3456.0
# full adders   38             4468.8
# half adders   23             1637.6
# inverters     10              192.0
                            ---------
Total width                   9754.4
Lenght                          70.4
Routing factor                   2.0
Total area                      1.37 mm2
```

Half-band filter H3

```
***** 6 order half-band filter 15 bit input word *****
registers 6x 15 bit
adder1     2x 15 bit  14 full 1 half
inverters 1x 16 bit
adder2     1x 16 bit         1 half
adder                  13 full 4 half
adder                  11 full 5 half
adder                  19 full 2 half
# registers        90              5760.0
# full adders      71              8349.6
# half adders      29              2064.8
# inverters        16               307.2
                                ---------
Total width                      16481.6
Lenght                              70.4
Routing factor                       2.0
Total area                          2.32 mm2
```

Half-band filter H4

```
***** 6 order half-band filter 16 bit input word *****
registers 6x 16 bit
adder1     2x 16 bit  15 full 1 half
inverters 1x 17 bit
adder2     1x 17 bit
adder                  13 full 4 half
adder                  11 full 5 half
adder                  19 full 2 half
# registers        96              6144.0
# full adders      73              8584.8
# half adders      30              2136.0
# inverters        17               326.4
                                ---------
Total width                      17191.2
Lenght                              70.4
Routing factor                       2.0
Total area                          2.42 mm2
```

Half-band filter H5

```
***** 6 order half-band filter 17 bit input word *****
registers 6x 17 bit
adder1     2x 17 bit   16 full 1 half
inverters 1x 18 bit
adder2     1x 18 bit            1 half
adder                  14 full 4 half
adder                  12 full 5 half
adder                  20 full 2 half
# registers       102            6528.0
# full adders      78            9172.8
# half adders      31            2207.2
# inverters        18             345.6
                                --------
Total width                    18253.6
Lenght                            70.4
Routing factor                     2.0
Total area                         2.57 mm2
```

Half-band filter H6

```
***** 6 order half-band filter 17 bit input word *****
registers 6x 17 bit
adder1     2x 17 bit   16 full 1 half
inverters 1x 18 bit
adder2     1x 18 bit            1 half
adder                  14 full 4 half
adder                  12 full 5 half
adder                  20 full 2 half
# registers       102            6528.0
# full adders      78            9172.8
# half adders      31            2207.2
# inverters        18             345.6
                                --------
Total width                    18253.6
Lenght                            70.4
Routing factor                     2.0
Total area                         2.57 mm2
```

Half-band filter H7

```
***** 10 order half-band filter 17 bit input word *****
registers 10x 17 bit
adder1      3x 17 bit 16 full  1 half
inverters  1x 18 bit
adder2     1x 18 bit            1 half
adder3     5x         16 full   2 half
adder4     4x         23 full   2 half
# registers        170          10880.0
# full adders      220          25872.0
# half adders       39           2776.8
# inverters         18            345.6
                               ---------
Total width                    39874.4
Lenght                            70.4
Routing factor                     2.0
Total area                         5.61 mm2
```

FIR-filter F1

```
***** 15 order FIR filter 7 bit input word *****
registers 15x  7 bit
adder1      8x  7 bit  6 full  1 half
inverters  4x  8 bit
adder2     4x  8 bit           8 half
adder3    12x          6 full   2 half
adder4    12x         12 full   2 half
# registers        105           6720.0
# full adders      264          31046.4
# half adders       88           6265.6
# inverters         32            614.4
                               ---------
Total width                    44646.4
Lenght                            70.4
Routing factor                     2.0
Total area                         6.29 mm2
```

FIR-filter F2

```
***** 22 order FIR filter 16 bit input word *****
registers 22x 16 bit
adder1      11x 16 bit 15 full  1 half
inverters  5x 17 bit
adder2       5x 17 bit          17 half
adder3      19x          15 full  2 half
adder4      19x          22 full  2 half
# registers        352            22528.0
# full adders      868           102076.8
# half adders      172            12246.4
# inverters         85             1632.0
                                  --------
Total width                      138483.2
Lenght                               70.4
Routing factor                        2.0
Total area                          19.50 mm2
```

FIR-filter F3

```
***** 20 order FIR filter 17 bit input word *****
registers 20x 17 bit
adder1      10x 17 bit 16 full  1 half
inverters  5x 18 bit
adder2       5x 18 bit          18 half
adder3      16x          16 full  2 half
adder4      16x          26 full  2 half
# registers        340            21760.0
# full adders      416            48921.6
# half adders      164            11676.8
# inverters         90             1728.0
                                  --------
Total width                       84086.4
Lenght                               70.4
Routing factor                        2.0
Total area                          11.84 mm2
```