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EINDHOVEN UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL ENGINEERING
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A DIGITAL DETECTION SYSTEM TO BE USED FOR PROPAGATION EXPERIMENTS

By H.C. van Nigtevecht

Report of the graduate work performed under the responsibility of prof. dr. ir. G. Brussaard.

Executed at: EUT, Eindhoven, the Netherlands and
ITS, Surabaya, Indonesia
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Summary

A 3-year cooperation project of the Eindhoven University of Technology and the Institute of Technology Sepuluh Nopember Surabaya, the EUT-ITS Telecommunications Project, started in January 1990. The research activities of this Project are focused on acquiring accurate information of the propagation characteristics of radio waves in the higher frequency band, Ku-band 11.7 - 12.7 GHz, in Indonesia. Measurements are performed on the Intelsat V - Surabaya down link and on a line-of-sight link between Surabaya and Madura.

A satellite beacon receiver system has been installed at ITS to receive a beacon signal from the Intelsat-V satellite. This receiver system employs an intermediate frequency phase-locked-loop receiver for the detection of the amplitude of the beacon signal. This receiver employs an analog coherent amplitude detection system.

A digital system is preferred over an analog system because of its versatility and reproducibility. At EUT a digital detector for propagation experiments using a TMS320C25 has been developed.

The objective of this graduate work is to develop a PLL receiver with digital detection to be employed in the Intelsat beacon receiver system.

To accomplish this, an analysis has been made of the accuracy requirements, and the hardware and software of the existing EUT detector has been modified. Furthermore the modified EUT detector has been interfaced to the EUT PLL receiver and tested at ITS, Indonesia. Measurements have verified the performance.

The digital detection system has a smaller detection bandwidth (0.3 Hz) than the analog detection circuit (1 Hz), which improves the signal-to-noise ratio of the detected signal.

Further digitalization of the PLL receiver is recommended.

List of symbols and abbreviations

A	amplitude of carrier
a_k	coefficient of digital filter
A_m	measured amplitude of carrier
A/D	Analog to Digital
AWGN	Additive White Gaussian Noise
b_k	coefficient of digital filter
B_n	equivalent noise bandwidth [Hz]
C	carrier power [W]
D	diameter antenna [m]
DAC	Digital to Analog Converter
DNL	Doktor Neher Laboratory
DSP	Digital Signal Processor
EPROM	Erasable Programmable Read Only Memory
EUT	Eindhoven University of Technology
f_{max}	maximal input frequency [Hz]
f_s	sampling frequency ($2\pi f_s = \omega_s$) [Hz]
f_0	carrier frequency [Hz]
FIR	Finite Impulse Response
h(n)	digital filter impulse response
H(z)	transfer function digital filter
$H(e^{-j\theta})$	transfer function digital filter
$H_{D/A}$	transfer function D/A converter
H_{det}	transfer function of detector
H_{FIR}	transfer function FIR filter
ITS	Institute of Technology Sepuluh Nopemper Surabaya
I-Q	In-phase and Quadrature
IIR	Infinite Impulse Response
INTELSAT	International Telecommunications Satellite Organization
k	integer
l	integer
LOS	Line Of Sight
LSB	Least Significant Bit
M	resolution of A/D converter
MSB	Most Significant Bit
n	integer
N	noise power [W]

NLG	Nederlandse Gulden
NUFFIC	Netherlands University Foundation for International Cooperation
PC	Personal Computer
PCB	Printed Circuit Board
PD	Phase Detector
PLL	Phase Locked Loop
q	step-size of A/D or D/A converter [V]
q_m	step-size of M-bit A/D converter [V]
R	integer
RAM	Random Access Memory
ROM	Read Only Memory
T/H	Track-Hold Amplifier
THE	Technische Hogeschool Einhoven
t_m	measuring time [s]
T_a	antenna noise temperature [K]
T_r	receiver noise temperature [K]
T_{sys}	system noise temperature [K]
T_s	sampling period [s]
VCO	Voltage Controlled Oscillator
ΔA_{dB}	amplitude resolution [dB]
Δf_0	frequency deviation from ideal frequency f_0, $f_0 = (2n + 1)/4f_s$ [Hz]
Δt	aperture uncertainty [s]
$\Delta\phi$	phase resolution [rad]
ϕ_c	phase of carrier [rad]
ϕ_{ref}	phase of reference signal [rad]
γ	ratio of rms value of noise and step-size of A/D converter
η	antenna efficiency [%]
η_0	thermal noise power density [$V^2.Hz^{-1}$]
σ_n	rms value of noise [V]
ω_s	angular sampling frequency [$rad.s^{-1}$]
θ	normalized frequency

1 Introduction

After several years of cooperation between the Eindhoven University of Technology (EUT), Eindhoven, the Netherlands and the Institute of Technology Sepuluh Nopember (ITS), Surabaya, Indonesia, a new cooperation project in the field of Telecommunications, Education and Radio Wave Propagation research has started for the period 1990 - 1992, the EUT-ITS telecommunications project. At the same time EUT and ITS are conducting a 2-year measurement contract for the International Telecommunications Satellite Organization (Intelsat) concerning beacon and radiometric measurements.

The research activities in the EUT-ITS telecommunications project will be focused on acquiring accurate information on the propagation characteristics of radio waves in the higher satellite frequency band, Ku-band 11.7 - 12.7 GHz, in Indonesia. A satellite beacon receiver has been installed at ITS to receive a beacon signal from the Intelsat-V satellite. This receiver system uses an intermediate frequency (IF) phase-locked-loop (PLL) receiver for the detection of the amplitude of the beacon signal. This PLL receiver employs an analog coherent amplitude detection circuit. The main disadvantages of the analog detection circuit are:

- Complicated tuning procedure.
- Temperature drift of analog components.
- Analog components used have nonlinear and nonidentical characteristics. This makes it difficult to realize different detectors with the same characteristics (reproducibility).

Instead of using analog detection it is possible to perform the amplitude detection digital as well at a certain IF. A digital detection system has none of the above mentioned disadvantages. An important advantage of a digital system is that different detectors using the same type of components have the same characteristics, whereas different analog detectors have not. Also with a digital system the characteristics can be easily changed by changing the software. The price to be paid for these advantages of the digital system consists of a higher power consumption, larger dimensions, and limited dynamic range due to the number of bits used.

EUT has at its disposal a digital detector, employing an in-phase and quadrature (I-Q) detection system, as developed by the Doctor Neher Laboratories (DNL, PTT), Leidschendam, The Netherlands. This DNL detector is employed in the ground station for the Olympus satellite at EUT. The disadvantage of the DNL design is that the microprocessor Z80 is used. This microprocessor is too slow to implement better filtering than the currently implemented integrate-and-dump filter.

To obtain a system with better filtering possibilities, a digital detector is developed at EUT. The new detector employs a digital signal processor (DSP) the TMS320C25. This DSP is especially designed for filtering, fast fourier transforms (FFT) etc. With this new detector it is possible to implement infinite impulse response (IIR) and finite response (FIR) filters.

The objective of this graduate work is to develop a PLL receiver with digital detection, to be employed in the Intelsat-V beacon receiver system at ITS.

This report describes the hardware and software modifications of the newly developed EUT detector to make it suitable for the Intelsat-V beacon receiver system. This detector has been made interchangeable with the DNL detector so that it can also be applied in the ground station for the Olympus satellite at EUT.

Further the interfacing of the modified EUT detector to the PLL receiver is described.

2 EUT-ITS Telecommunications Project

2.1 Introduction

The Department of Electrical Engineering of the Eindhoven University of Technology (EUT) in the Netherlands and the Department of Electrical Engineering of the Institute of Technology Sepuluh Nopember Surabaya (ITS) have been cooperating during the period 1971-1974 (THD/E/T-2 project) and 1976-1981 (THE-2 project). In the THE-2 project the following research activities were conducted:

a 50-km line-of-sight (LOS) link between Gunung Sandangan, Madura (Perumtel site), and ITS-Surabaya at 4 GHz and 7 GHz.

b 150-km troposcatter link between Situbondo and ITS-Surabaya at 4 GHz.

During the execution of this project a good relationship between EUT-ITS and Perumtel has been established.

With the financial assistance of the Netherlands University Foundation for International Cooperation (NUFFIC) a new cooperation was brought about between EUT and ITS for the period 1990-1992: The " EUT-ITS Telecommunications Project " [1], [2]. This project includes the following activities:

a Educational:
- Exchange of EUT and ITS lecturers.
- Upgrade of ITS Telecommunications curriculum.
- Seminars at ITS by EUT lecturers.

b Research:
- Execution of a satellite propagation experiment in the Ku-band (satellite receiver, radiometer, rain gauge, data acquisition system).
- LOS link between Gunung Sandangan and ITS at Ku-band, in close cooperation with Perumtel.
- Processing of all measurement results by ITS students.

c Supporting:
- Organization of workshop in Communication Electronics.
- Upgrade of library of the Telecommunications Division.

2.2 Propagation experiment

Satellite communication is vitally important in national and international telecommunications networks. The increasing demand for communication capacity and the requirement of high satellite EIRP for certain telecommunication services has urged the employment of higher satellite frequency bands, such as the Ku-band (11.7-12.7 GHz). Intelsat series V, Intelsat series VI, ECS and TV-Sat are examples of satellites that already offer telecommunication services in the Ku-band.

The Indonesian Palapa satellites, including the newly launched Palapa B2R, are equipped with transponders in the C-band only. Perumtel is taking the introduction of telecommunication services in the Ku-band into serious consideration. However, before new telecommunication services in the Ku-band can be introduced, it is necessary to know the propagation characteristics of the radio waves in a tropical monsoon country, such as Indonesia. In a tropical monsoon climate severe radio wave attenuation in the Ku-band caused by rainfall is expected. Until now neither accurate rain attenuation measurements models are available, nor have accurate attenuation measurements been conducted in tropical monsoon countries, such as Indonesia.

Therefore, it was decided that in the EUT-ITS Telecommunications Project the research activities will concentrate on acquiring accurate information on the propagation characteristics of radio waves in the Ku-band in Indonesia. A system containing a satellite beacon receiver, radiometer, rain gauge and data acquisition system has been installed at the Electrical Engineering Department (EED) of ITS. During a period of at least 2 years, attenuation induced by rain will be measured and processed.

It is expected that the final results will contribute to the improvement of the current rain attenuation models for tropical countries. Moreover, the data will be indispensable for organizations such as Perumtel and Intelsat, in defining future telecommunication systems and services in the Ku-band in Indonesia.

2.3 Measurement system

Fig. 2.1 shows the schematic diagram of the measurement system which has been installed at ITS. The system consists of:

- a Temperature sensor to measure the ambient temperature.
- b Rain gauge of the tipping bucket type, to measure rainfall up to 600 mm/h.
- c Radiometer to measure the sky noise temperature.
- d Satellite beacon receiver to measure the 11.2 GHz beacon signal from Intelsat-V F8.
- e Chart recorder to display the measured data.
- f Data acquisition system, containing an A/D converter and XT computer to collect and save the measured data. The data is stored on diskettes.

Fig. 2.2 shows the block diagram of the satellite beacon receiver. The satellite beacon signal (f=11.198 GHz) is converted to a first IF frequency of 127 MHz. The image frequency is rejected by a 11.198 GHz bandpass filter (BPF). The 127 MHz signal is converted to a second IF frequency of 10 MHz and is received by a phase-locked-loop (PLL) receiver. After DC processing, filtering and A/D conversion, the data is stored on 720 kB diskettes. The diskettes contain raw data and must be processed to obtain statistical results.

Table 2.1 shows the link budget of the beacon receiver. From this table it is shown that the dynamic range of the system is approximately 25 dB. This means that rain attenuation up to 25 dB can be measured by the system. For higher rain attenuation the PLL receiver will loose lock.

In order to collect more information on the radio wave attenuation induced by rainfall, a LOS link at a frequency of 11.3 GHz has been set up between the Perumtel site at Gunung Sandangan, Madura and ITS, Surabaya. The installation of the LOS system over a distance of 46 km has taken place in early 1991.

Fig. 2.3 shows the LOS system. A low power beacon transmitter has been installed at Gunung Sandangan, while the receiver has been placed at ITS. Additional rain information is obtained by a second rain gauge (of the tipping bucket type) at the Gunung Sandangan site. The link budget in table 2.2 shows that the LOS link offers a large dynamic range of about 84 dB. Further, ITS will discuss with Perumtel the possibility of digital data transmission in the Ku-band over the LOS.

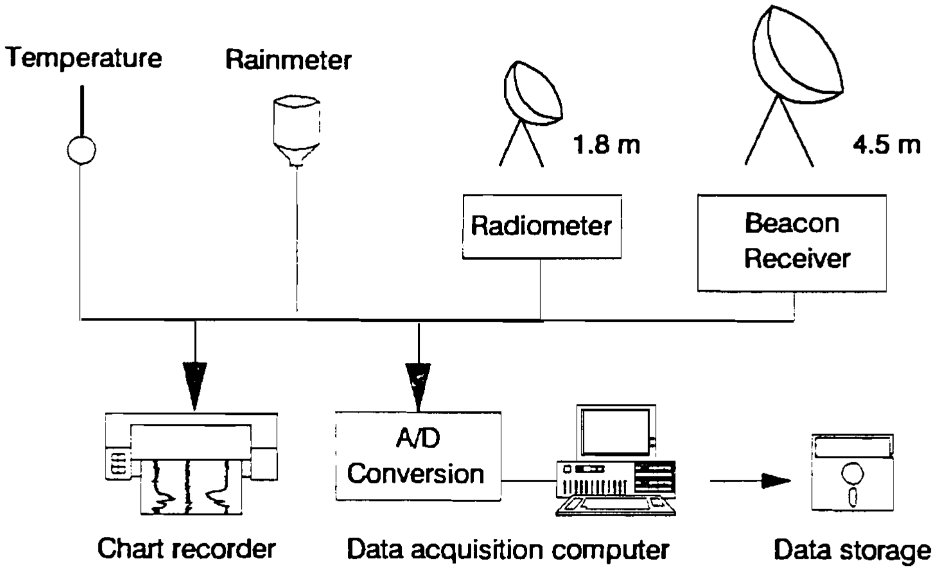


Fig. 2.1: Measurement system at ITS.

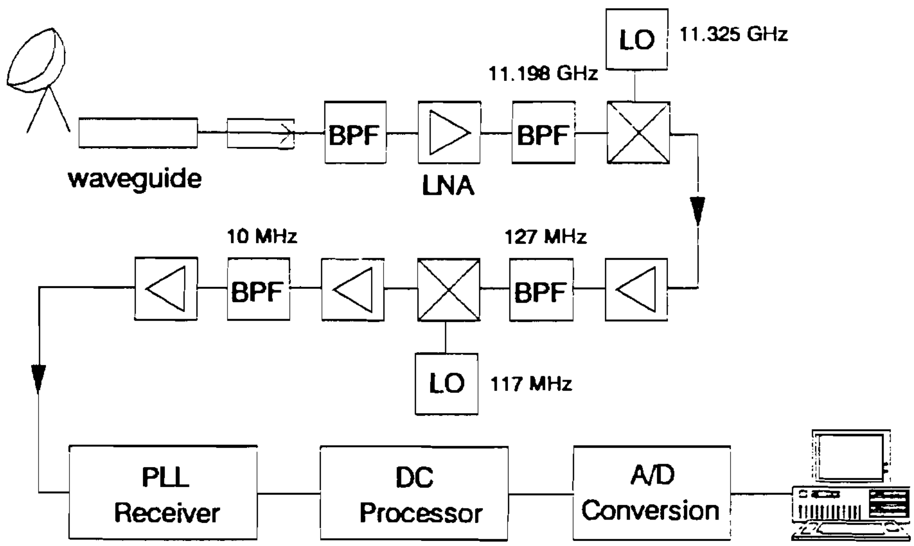


Fig. 2.2: Satellite beacon receiver.

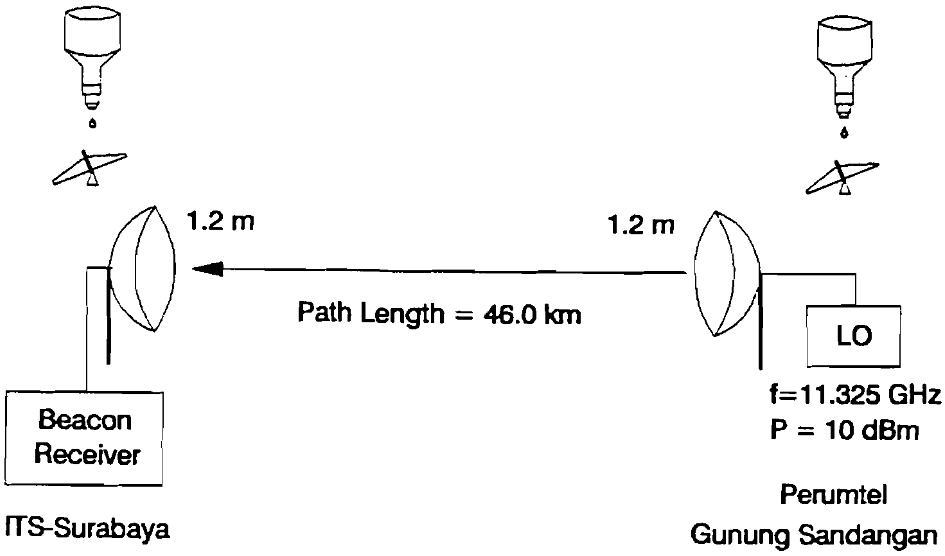


Fig. 2.3: LOS system.

Table 2.1: Beacon receiver link budget.

EIRP towards Surabaya =	9	dBW
Path Loss =	205.5	dB
Atmospheric Attenuation =	0.4	dB
Antenna Pointing Loss =	0.3	dB
Antenna Gain $\eta(\pi Df/c)^2$ =	51.0	dB
η = 55 %		
D = 4.5 m		
Power received by beacon antenna (C) =	-145.4	dBW
k (Boltzmann constant) =	-228.6	dBW/HzK
B_n (Noise Bandwidth = 100Hz) =	20.0	dBHz
T_a (Antenna Noise Temp.)	40	K
T_r (Receiver Noise Temp.)=	454	K
$T_{sys} = T_a + T_r$ =	26.6	dBK
Noise received by system N) $k.T_{sys}.B_n$ =	-182.0	dBW
C/N =	35.8	dB
C/N threshold	8.2	dB
T_{sys} degradation due to heavy rainfall (T_a = 300 K)	1.9	dB
Dynamic Range	25.7	dB

Table 2.2: LOS link budget.

EIRP towards Surabaya =	22.0	dBW
Path Loss =	146.8	dB
Atmospheric Attenuation =	0.4	dB
Antenna Pointing Loss =	0.3	dB
Antenna Gain $\eta(\pi Df/c)^2$ = η = 78 % D = 1.2 m	42.0	dB
Power received by beacon antenna (C) =	-83.5	dBW
k (Boltzmann constant) =	-228.6	dBW/HzK
B_n (Noise Bandwidth = 300 H) =	24.8	dBHz
T_a (Antenna Noise Temp.) =	200	K
T_r (Receiver Noise Temp.) =	800	K
$T_{sys} = T_a + T_r$ =	30.0	dBK
Noise received by system (N $k.T_{sys}.B_n$ =	-173.8	dBW
C/N =	90.3	dB
C/N threshold	6	dB
T_{sys} degradation due to heavy rainfall (T_a = 300 K)	0.4	dB
Dynamic Range	84	dB

3 PLL receiver for propagation experiments

3.1 PLL receiver using analog coherent detection

The block diagram of the PLL receiver, which is commonly used at EUT for propagation measurements, is shown in Fig. 3.1. This receiver is used for accurate measurement of signal level of a co- and crosspolar signal as well as the differential phase between these two signals. The receiver operates at an IF of 10 MHz and employs an analog coherent amplitude detection system.

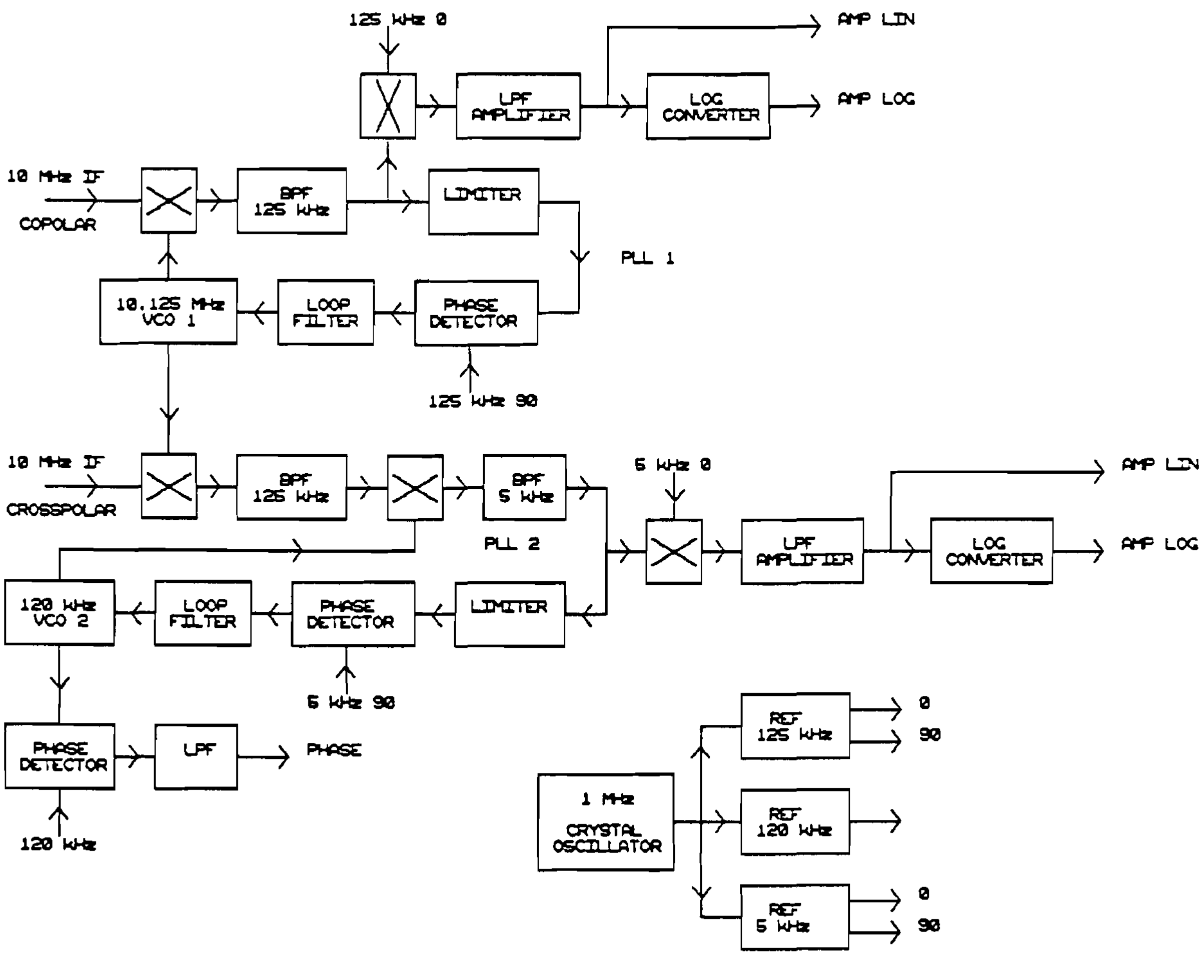


Fig. 3.1: block diagram PLL receiver using analog coherent detection.

The receiver consists of two phase-locked-loops (PLLs): The main loop PLL-1 and the sub loop PLL-2.

- Main loop PLL-1

The input signal (CP) is down converted with VCO-1 to a frequency of 125 kHz. The down converted signal is compared to a reference signal of 125 kHz. Due to PLL-1 (a heterodyning PLL) the down converted signal is locked to the 125 kHz reference signal. The phase difference of the down converted copolar signal and the reference signal is constant (90 degrees).

Coherent detection is achieved by mixing the down converted signal in the main loop with the 125 kHz reference signal, shifted 90 degrees in phase (this is called synchronous amplitude detection). A mixer is applied as a synchronous detector. The mixer is followed by a low pass filter and a logarithmic converter.

- Sub loop PLL-2

The crosspolar signal is down converted with VCO-1 to 125 kHz. Due to PLL-1 the frequency of this signal is equal to the frequency of the 125 kHz reference signal. However, the phase difference between this signal and the reference signal is not constant. The receiver is locked on the copolar signal. Due to atmospheric effects, a varying phase difference can arise between the copolar and crosspolar signal. The down converted crosspolar signal (125 kHz) is mixed with VCO-2. This down converted signal (5 kHz) is compared to a 5 kHz reference signal. Due to PLL-2 the down converted signal is locked to the 5 kHz reference signal. A low second IF frequency is chosen to make a small loop bandwidth possible. This small loop bandwidth is necessary for the detection of the crosspolar signal, which can have a small signal to noise ratio. The amplitude detection (synchronous) is performed in the same manner as in the main loop.

By mixing VCO-2 with a 120 kHz reference signal, the phase difference of the copolar and the crosspolar signal is obtained. The complete schematic diagram of the PLL receiver is given in appendix A.

3.2 Performance PLL receiver in the presence of noise

3.2.1 Requirements for stable lock condition

Additive bandpass Gaussian noise and beacon phase noise will introduce phase noise in the loop of the PLL. In the case of additive noise, the narrower the loop bandwidth the more accurate the PLL will track the beacon signal. To track out beacon phase noise, however, the loop bandwidth should be as wide as possible. The total phase error variance in the PLL will be the sum of the two component variances due to additive and phase noise. As a rule of thumb, a PLL is in lock when the phase error variance < 0.25 rad^2, in other words, when the S/N ratio in the loop > 6 dB [3].

From data concerning the fraction of total carrier power present within a prescribed noise bandwidth, an estimation of the frequency flicker noise component ($\propto f^{-3}$) of the phase noise spectrum originating from an Intelsat V beacon operating in the 11 GHz band, is determined [4]. Employing a noise bandwidth in the range 100 - 500 Hz, phase jitter due to the beacon signal will determine lock conditions of the PLL during clear sky and moderate attenuation events. During severe attenuation events thermal noise will become dominant.

The contribution of thermal noise ($\propto B_n$) as well as beacon phase noise ($\propto B_n^{-2}$) give rise to opposed constraints regarding the choice of PLL noise bandwidth B_n. This is graphically displayed in Fig. 3.2 for the case of a maximum rain attenuation event of 22 dB during which the receiver will be in lock for a value of B_n lying between 100 - 300 Hz.

An optimum can be deduced but is dependent upon carrier attenuation level. In Fig. 3.3, the operational dynamic range is plotted against noise bandwidth B_n for the cases that beacon phase jitter is absent and present.

For the Intelsat receiver, the phase error variance due to out-of-band phase noise of the Intelsat beacon, is estimated to be 0.1 rad^2 for a noise bandwidth of 100 Hz (Fig. 3.2, [4]). Therefore, loss of lock due to thermal noise inside the noise bandwidth, occurs when the phase error variance due to thermal noise is larger than 0.15 rad^2. This is equivalent to a S/N ratio of 8.2 dB within the noise bandwidth of the PLL [3].

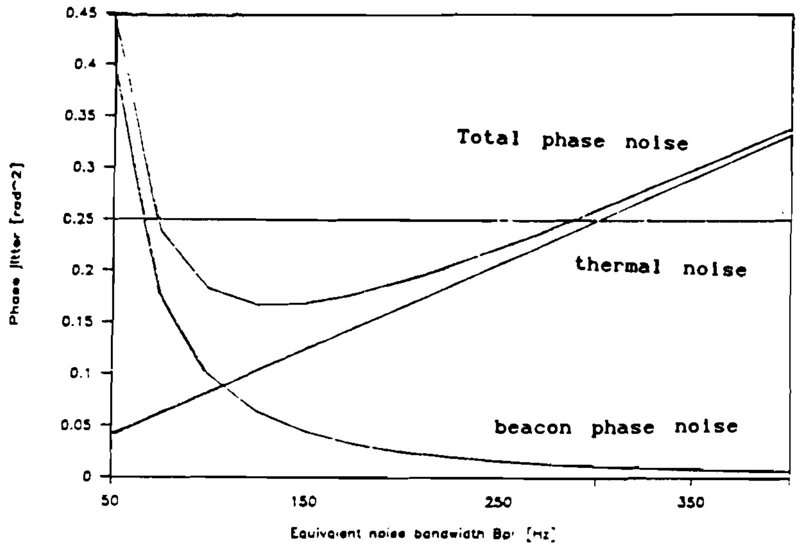


Fig. 3.2: Total phase noise during a 22 dB attenuation event versus B_n.

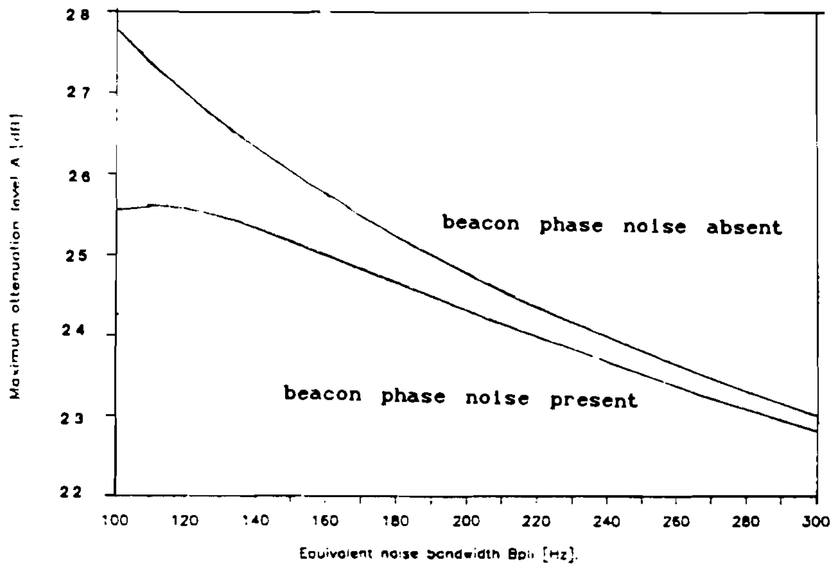


Fig. 3.3: Operational dynamic range versus B_n.

Intelsat [4] requires a minimum fade level of 22 dB. In order to meet the requirements of Intelsat and guarantee lock conditions over the entire operational dynamic range of 22 dB, a noise bandwidth in the range of 100 - 300 Hz has to be chosen. Employing a noise bandwidth of 100 Hz, an operational dynamic range of approximately 25.7 dB is available for the PLL receiver (see link budget in table 2.1).

3.2.2 Amplitude measurement errors

The down converted signal in PLL-1 is employed for coherent detection (Fig. 3.1). In an application note [3], an estimation is given for the average measured amplitude of a carrier with narrow-band noise, using coherent detection (assuming no beacon phase jitter).

$$A_m = A(1 + \sigma^2_{s1}/2) \tag{3.1}$$

where

A_m average measured carrier amplitude

A carrier amplitude

σ^2_{s1} variance of quadrature noise within the noise bandwidth of the phase-locked-loop

The average measured amplitude is an overestimation of the carrier signal A. Contrary to this, Schaffels and Vaessen [4] found an underestimation of the carrier signal. However this was due to a misconception regarding the coherent detection process.

It has been shown that thermal noise in the PLL noise bandwidth causes a measurement error. Near loss of lock a slight non-linearity can be expected. For a S/N ratio of 8.2 dB (threshold point of the Intelsat receiver) the measurement error is estimated at about 0.6 dB. Phase noise of the beacon outside the noise bandwidth, gives a constant error (for a given noise bandwidth) and does not effect attenuation measurements. The phase noise of the beacon only results in a higher S/N ratio threshold point were the PLL looses lock.

3.3 PLL receiver using digital I-Q detection

Schaffels and Vaessen [4] state that the amplitude measurement error can almost be eliminated when the receiver will be modified in order to detect the quadrature amplitude component as well (in-phase and quadrature detection, see chapter 4). However, in [3] it is demonstrated that an I-Q detection system is in essence similar to a common coherent detector (synchronous detection). Therefore an I-Q detection system will show the same error as a coherent detection system.

For the detection of a copolar and a crosspolar signal the PLL receiver employs two phase-locked-loops (main loop PLL-1 and sub loop PLL-2, see Fig. 3.1). However, if an I-Q detection system is applied only one PLL is required (main loop PLL-1). In Fig. 3.4 is shown the modified PLL receiver using I-Q detection instead of coherent detection for the detection of a copolar and a crosspolar signal. I-Q detection also produces the average phase difference between these two signals.

For the realization of the PLL receiver using I-Q detection is chosen for a digital I-Q detection system instead of an analog system because of the versatility and reproducibility which are common properties of digital techniques.

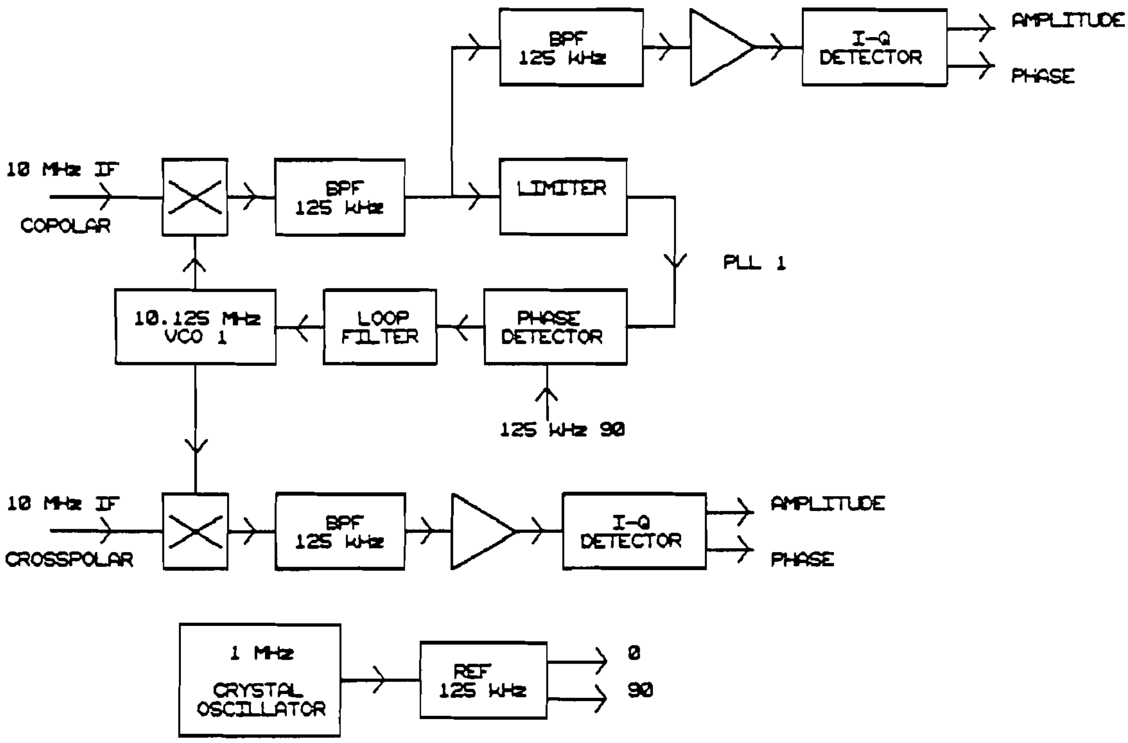


Fig. 3.4: PLL receiver using digital I-Q detection.

3.4 Recommendations for further digitalization

The PLL receiver using digital I-Q detection still has an analog circuit for the phase-locked-loop (Fig. 3.4). Further digitalization further reduces the tuning procedure and enhances the reproducibility and versatility. The analog PLL can be digitalized using a digital signal processor like the TMS320C25 as shown in Fig. 3.5 [5]. It may also be possible to implement an automatic frequency control (AFC) instead of a phase-locked-loop (PLL).

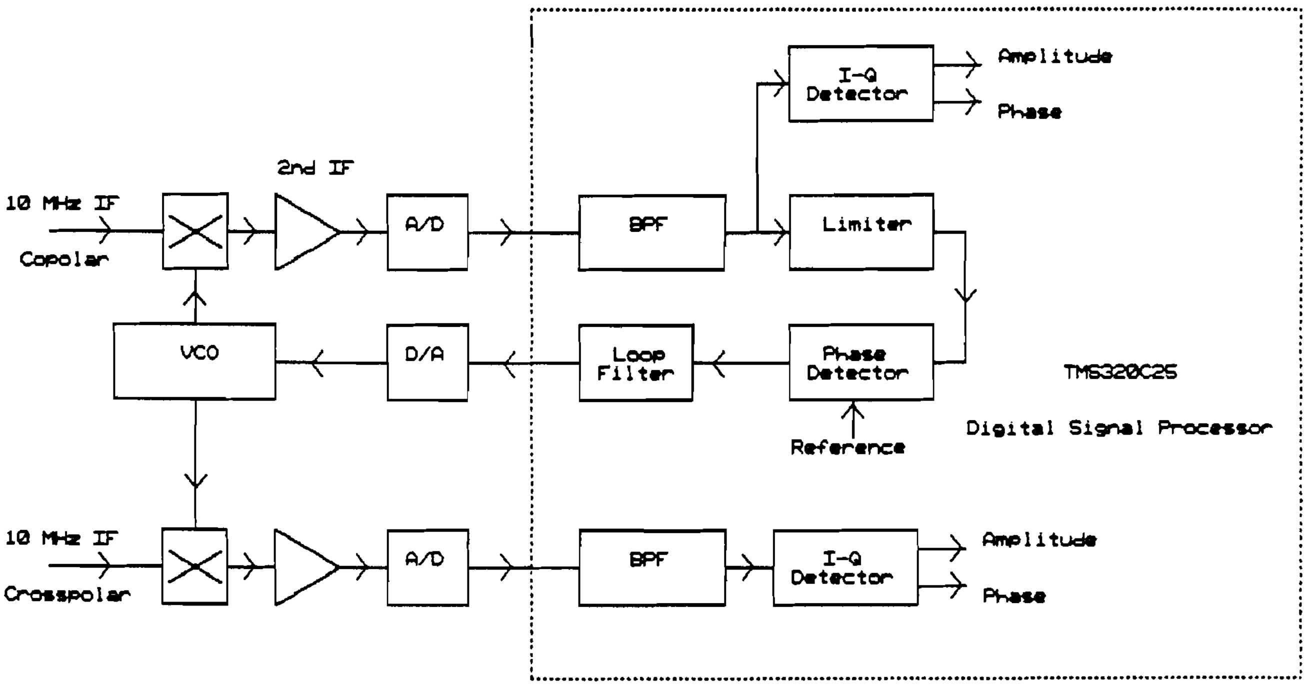


Fig. 3.5: Digital PLL receiver.

Instead of applying a down converter it might be possible to digitalize directly at the 10 MHz IF. However, the requirements of the needed A/D converter are far more stringent than when a much lower IF is applied. It may be necessary to use a lower IF to realize such a system.

4 In-phase and Quadrature detection

The digital detectors from DNL and EUT employ a digital in-phase and quadrature detection (I-Q) system. As an introduction into the digital I-Q detection system first the analog system is explained.

4.1 Analog I-Q detection

Fig. 4.1 shows the analog I-Q detection system. With this system it is possible to obtain the amplitude of an input signal and the differential phase between this signal and the local reference signal.

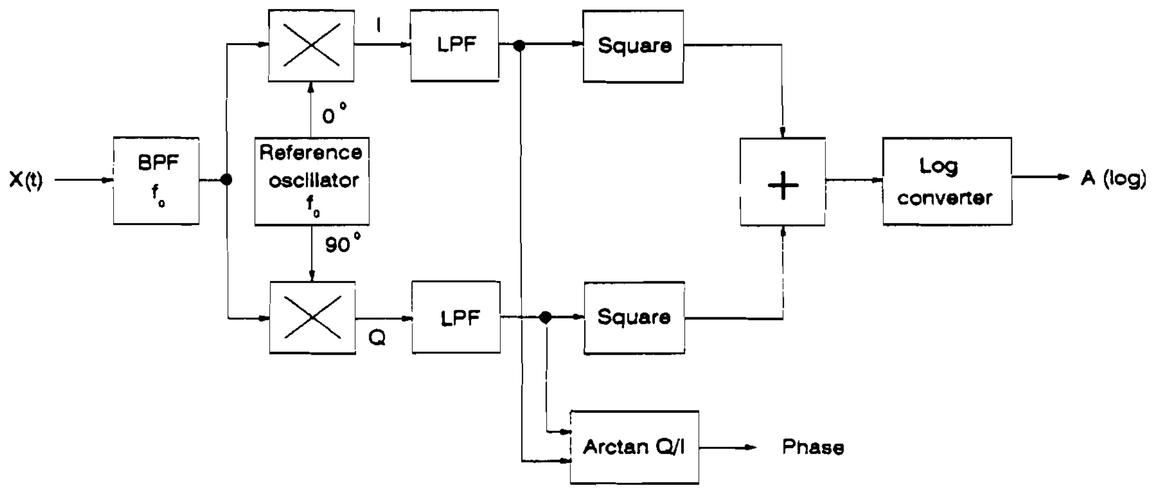


Fig. 4.1: Analog I-Q detection system.

For the explanation of the analog I-Q detection system, the input signal x(t) is assumed to be an ideal carrier without modulation and noise.

$$x(t) = A\cos(2\pi f_0 t + \phi_c) \tag{4.1}$$

The signal x(t) is split into two channels. In one channel x(t) is multiplied by $\cos(2\pi f_0 t + \phi_{ref})$ and in the other channel x(t) is multiplied by $\sin(2\pi f_0 t + \phi_{ref})$. These channels are mentioned as in-phase and quadrature channels, respectively.

$$I = A\cos(2\pi f_0 t + \phi_c)\cos(2\pi f_0 t + \phi_{ref})$$

$$= \tfrac{1}{2}A\cos(4\pi f_0 t + \phi_c + \phi_{ref}) + \tfrac{1}{2}A\cos(\phi_c - \phi_{ref}) \qquad (4.2)$$

$$Q = A\cos(2\pi f_0 t + \phi_c)\sin(2\pi f_0 t + \phi_{ref})$$

$$= \tfrac{1}{2}A\sin(4\pi f_0 t + \phi_c + \phi_{ref}) - \tfrac{1}{2}A\sin(\phi_c - \phi_{ref}) \qquad (4.3)$$

After the multiplication a lowpass filter (averaging) is employed.

$$I = \tfrac{1}{2}A\cos(\phi_c - \phi_{ref}) \qquad (4.4)$$

$$Q = -\tfrac{1}{2}A\sin(\phi_c - \phi_{ref}) \qquad (4.5)$$

These signals are squared separately and added. This results in a signal which is directly proportional to A^2.

$$I^2 + Q^2 = \frac{A^2}{4} \qquad (4.6)$$

Finally the logarithmic is taken from this signal.

$$10\mathrm{Log}(\frac{A^2}{4}) = 20\mathrm{Log}(A) - 20\mathrm{Log}(2) \qquad (4.7)$$

To obtain the phase difference $\phi_c - \phi_{ref}$ an arctangens converter is applied.

$$\arctan\left(\frac{-Q}{I}\right) = \arctan\left(\frac{\tfrac{1}{2}A\sin(\phi_c - \phi_{ref})}{\tfrac{1}{2}A\cos(\phi_c - \phi_{ref})}\right)$$

$$= \arctan(\tan(\phi_c - \phi_{ref})) = \phi_c - \phi_{ref} \qquad (4.8)$$

Thus an I-Q detection system produces the amplitude of a signal independent of the phase difference between this signal and the local reference signal ($\phi_c - \phi_{ref}$).

4.2 Digital I-Q detection

Until recently the I-Q detection system has been implemented using analog techniques. However it is difficult to construct several analog detectors with the same characteristics. Many of the used components have non-linear characteristics and are temperature dependent. The detector requires a lot of tuning which is a difficult and time consuming job. Because of these problems a digital version has been developed. However, by using digital techniques other problems are introduced, like dynamic range limitation by the amount of bits used, limitation on the resolution and nonlinearity of A/D and D/A converters. One of the main advantages of a digital detection system is the flexibility, by changing software the filter characteristics can be changed. Another important advantage is the reproducibility

Fig. 4.2 shows the digital I-Q detection system.

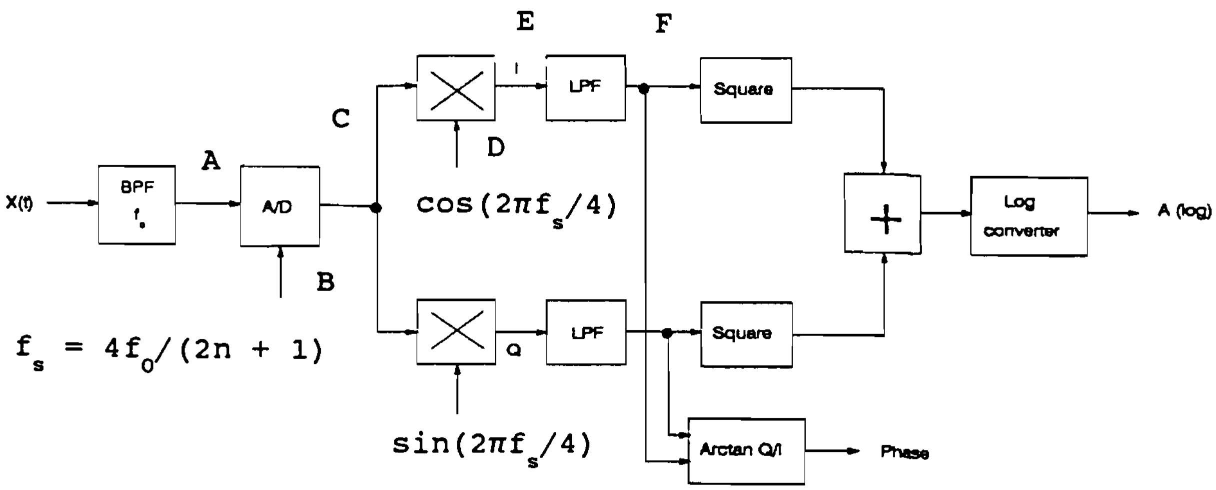


Fig. 4.2: Digital I-Q detection system.

- Frequency domain analysis

The input signal is band limited by a bandpass filter (bandwidth B_n). This filter is followed by an A/D converter. The sampling frequency should satisfy the next equations to avoid aliasing (see Fig. 4.3 for explanation). In this case, there is no overlap in the adjacent spectral components and the input signal can be completely recovered.

$$f_s \geq 2B_n \tag{4.9}$$

$$f_s = \frac{4f_0}{(2n + 1)} \qquad (n = 0,1,2,...) \tag{4.10}$$

After the A/D converter all operations are performed digital. Fig. 4.3 shows the spectra at several points in the digital detector.

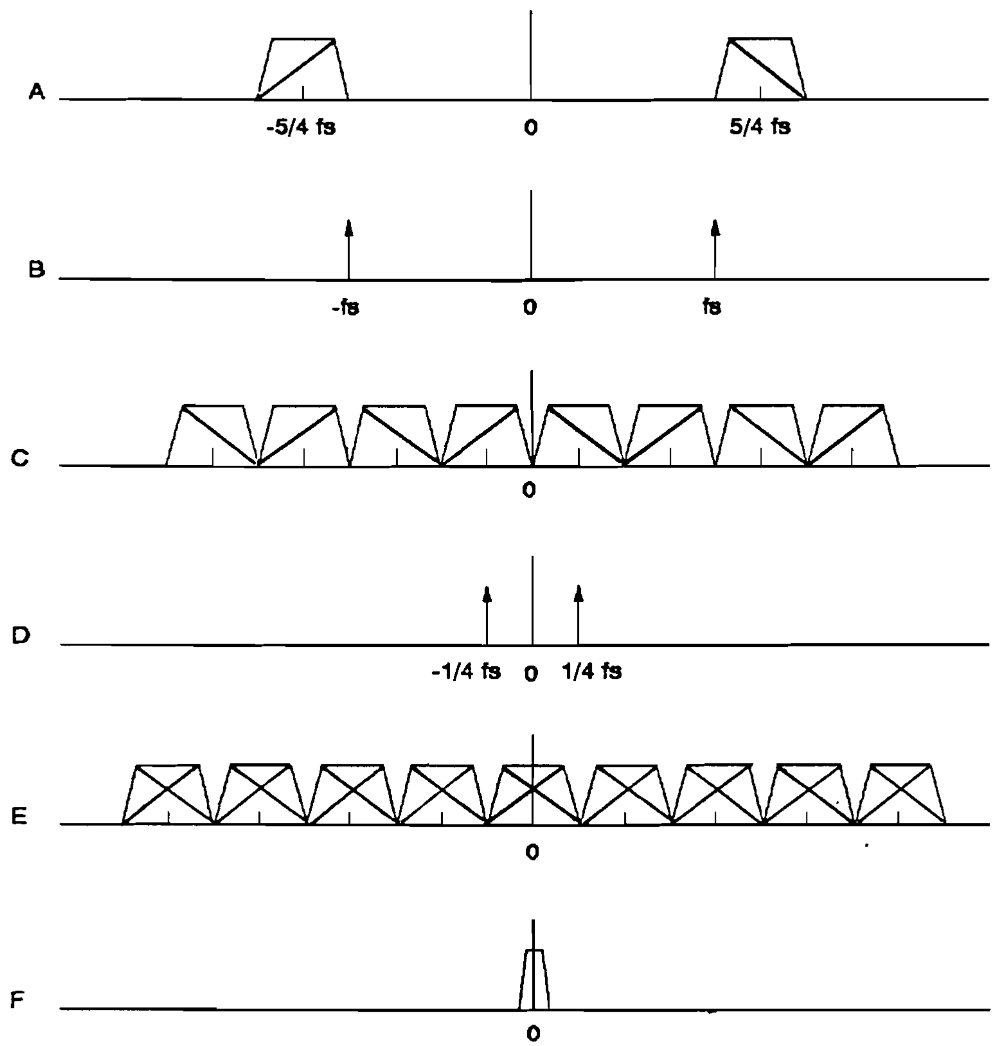


Fig. 4.3: Spectra in the digital detector, n = 2.

- Time domain analysis

For the explanation of the digital I-Q detection system the input signal x(t) is assumed to be an ideal carrier without modulation and noise.

$$x(t) = A\cos(2\pi f_0 t + \phi_c) \tag{4.11}$$

Sampling, quantization noise neglected, results in:

$$\begin{aligned} x_s(t) &= x(t)\sum_{m=-\infty}^{+\infty}\cos(2\pi m f_s) \\ &= A\sum_{m=-\infty}^{+\infty}\cos\left\{\left(\frac{2n+1}{4} - m\right)2\pi f_s t + \phi_c\right\} \end{aligned} \tag{4.12}$$

One copy of the input signal is at $\frac{1}{4}f_s$ $(m = \frac{2n}{4})$.

$$x(kT_s) = A\cos\left(\tfrac{1}{4}\omega_s kT_s + \phi_c\right) \tag{4.13}$$

To obtain a baseband signal, $x(kT_s)$ is multiplied with $\cos(\frac{1}{4}2\pi f_s kT_s)$ (I-component), and with $\sin(\frac{1}{4}2\pi f_s kT_s)$ (Q-component).

The multiplication results in:

$$\begin{aligned} I(kT_s) &= A\cos\left(\tfrac{1}{4}\omega_s kT_s + \phi_c\right)\cos\left(\tfrac{2\pi}{4}k\right) \\ &= \tfrac{1}{2}A\left(\cos\left(\tfrac{\pi}{2}k + \phi_c\right) + \cos\phi_c\right) \end{aligned} \tag{4.14}$$

$$\begin{aligned} Q(kT_s) &= A\cos\left(\tfrac{1}{4}\omega_s kT_s + \phi_c\right)\sin\left(\tfrac{2\pi}{4}k\right) \\ &= \tfrac{1}{2}A\left(\sin\left(\tfrac{\pi}{2}k + \phi_c\right) - \sin\phi_c\right) \end{aligned} \tag{4.15}$$

The lowpass filters remove the first component of Eqs. 4.14 and 4.15. The filters are implemented in software which makes a wide variety of filters possible. By changing the software, filter characteristics can be changed.

The amplitude and the phase are calculated in the same manner as in the analog I-Q detection system (see Eqs. 4.6 - 4.8).

5 Digital filters

5.1 Filter structures

For a large variety of applications, digital filters are usually based on the following relationship between the filter input sequence x(n) and the filter output sequence y(n).

$$y(n) = \sum_{k=1}^{M} a_k y(n - k) + \sum_{k=0}^{N} b_k x(n - k) \tag{5.1}$$

Eq. 5.1 is referred to as a linear constant coefficient difference equation.

Digital filters are often categorized either by the duration of their impulse response or by their structure. When a filter produces an impulse response that has an infinite duration, it is called an infinite impulse response (IIR) filter. For an IIR filter at least one of the coefficients a_k in Eq. 5.1 is nonzero. If the digital filter has an impulse response having a finite duration, then it is called a finite-impulse response (FIR) filter. For a FIR filter all of the coefficients a_k in Eq. 5.1 are zero.

Digital filter classification can also be based on the filter structure. In general, the output of a filter can be a function of future, current and past input values, as well as past output values. If the output is a function of the past outputs, a feedback, or recursive mechanism from the output must exist. Therefore, such a filter is referred to as a recursive filter. If the filter output is a function of only the input sequence values, it is called a nonrecursive filter.

To achieve an infinite-duration impulse response, some form of recursive structure is necessary. Therefore the term IIR and recursive are commonly accepted as being interchangeable. Similarly, finite-duration impulse responses are typically implemented with nonrecursive filters. Therefore FIR and nonrecursive are also usually interchangeable.

A realization of a FIR filter is shown in Fig. 5.1. This structure is referred to as a direct form of a FIR filter, because the filter coefficients can be identified directly from the difference equation.

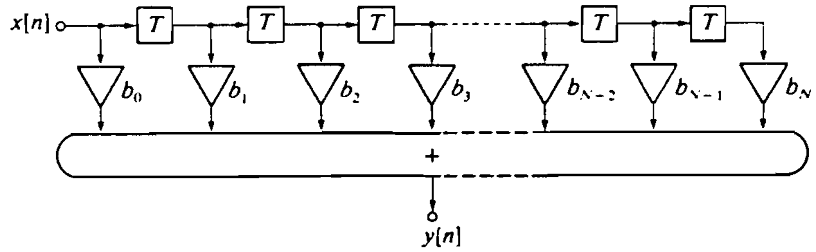


Fig. 5.1: Direct-form FIR filter.

The transfer function of a causal FIR filter is a polynomial in z^{-1}.

$$H(z) = \sum_{n=0}^{N} h(n) z^{-n} = H(e^{j\Omega}) = \sum_{n=0}^{N} b_n e^{-jn\Omega} \qquad z = e^{j\Omega} \tag{5.2}$$

A length L (L = N + 1) filter has a transfer function that has N zeros in the z-plane and has an order N pole at the origin of the z plane. A FIR filter is called an all-zero filter because it has zeros but no poles other than that at the origin.

In many applications it is desirable to design filters to have linear phase. A FIR filter can have exactly linear phase. In other words, the group delay of the filter can be a constant. For a FIR filter to have a linear-phase property, the impulse response must be symmetric or asymmetric around some point in time [6].

The required filter length L, increases when sharp transitions between frequency bands are specified, and/or large attenuations are required in the stop bands. Thus, high-performance filters with sharp cutoffs and large attenuations, are long and have a large delay.

As has been stated above for a digital filter to have a linear phase, its unit-impulse response sequence must be symmetric or asymmetric about some point in time. Since the FIR filter coefficients are identical to the elements of the impulse response, pairs of multipliers have coefficients with identical magnitudes. To save a multiplication operation, the inputs to these multipliers can be combined and then the product computed. Doing this reduces the number of multiplications by approximately one-half. Since a multiplication operation is in many situations the most time-consuming operation in a digital filter, this method can reduce the computation time significantly. However, when a digital signal processor for instance the TMS320C25 is applied, this is not necessary. A TMS320C25 contains single cycle multiply/ accumulate instruction.

A realization of a IIR filter is shown in Fig. 5.2. This structure is referred to as a direct form of a IIR filter, because the filter coefficients can be identified directly from the difference equation.

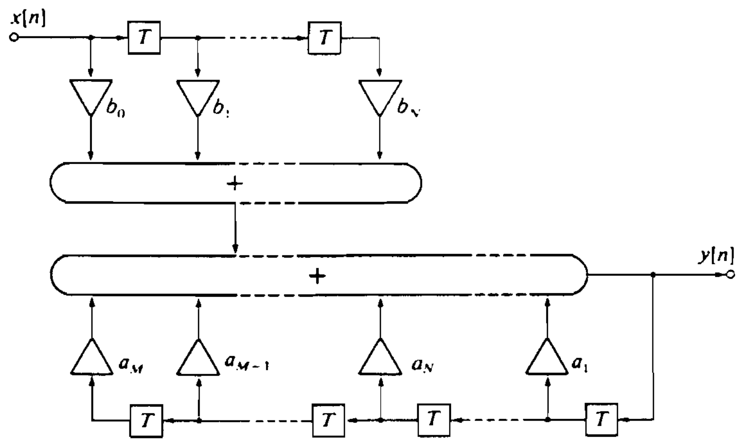


Fig. 5.2: Direct-form IIR filter.

An IIR filter has an infinite-duration impulse response. The transfer function of an IIR filter is a rational function of z^{-1}.

$$H(z) = \frac{b_0 + b_1 z^{-1} + \ldots + b_N z^{-N}}{1 + a_1 z^{-1} + \ldots + a_M z^{-M}} \tag{5.3}$$

Unlike analog filters, where the order of the numerator must be less than or equal to the order of the denominator, a digital filter can have M greater than, equal to, or less than

N. In addition to the order M-N zero or pole at the origin, the filter has N zeros and M poles in the z plane.

An IIR filter can generally achieve a sharper transition between band edges than a FIR filter with the same number of coefficients. The reason is that the IIR filter has a pole near the edge of the pass band and a nearby zero at the edge of stop band. Since the FIR filter cannot have poles (except at the origin), it cannot achieve the same sharp cutoff. The closely spaced pole and zero lead to a rapid change in group-delay for frequencies approaching the band edge.

An IIR filter has an infinite-duration impulse response that cannot be symmetric if it is causal ($h(n) = 0$ for $n < 0$). Therefore, an IIR filter cannot have exactly linear phase. Of course, an IIR filter can be designed with a good approximation to linear phase, at least over a limited band of frequencies. Minimum-phase, lowpass IIR filters with sharp transition between the pass band and stop band typically have a small group delay at zero frequency that increases rapidly at frequencies near the band edge.

Implementing IIR filters with a recursive realization in fixed-point arithmetic is much more difficult than the direct, nonrecursive implementation of an FIR filter. Much greater care must be taken in the scaling of the filter coefficients. When there is an overflow in a recursive filter, large scale oscillations can occur, which obscure any useful output from the filter.

Quantization noise can be more of a problem than in nonrecursive filters, because of the recursive nature of the calculation. The double-length product of two numbers must be quantized in order to be fed back in the recursion. The frequency response, and even the stability, as determined from the pole locations, is sensitive to quantization of the filter coefficients. This sensitivity rules against directly implementing the difference equation. Cascade or parallel connections of low-order blocks are better implementations for recursive filters.

An IIR filter has an advantage over a FIR filter in that it generally has fewer coefficients than a FIR filter with similar magnitude characteristics, so less memory is required to store the coefficients. A more significant memory saving occurs because only a few of the recent input values need to be stored, in contrast to the FIR case where L input values need to be stored for a length L filter. Even though the IIR filter has fewer coefficients than an equivalent FIR filter, it still may take less time to compute an output sample for the equivalent FIR filter. For example, with the TMS32020 signal processor, the nonrecursive calculation requires approximately one fifth of the time per coefficient of the recursive calculation. In other words, for the same computing time the FIR filter can have approximately five times as many coefficients as an IIR filter.

5.2 Moving Average filter

A special case of a FIR filter is the moving average filter [7]. The coefficients of this filter have the same value. The output signal is the moving average of the input signal. The relation between the input and output signal is given by:

$$y(n) = \frac{1}{2N+1}\sum_{k=-N}^{N} x(n-k) \qquad (5.4)$$

The impulse response of this filter is given by:

$$h(n) = \frac{1}{2N+1} \qquad \text{for} \quad -N \le n \le N \qquad (5.5)$$

$$h(n) = 0 \qquad \text{for} \quad n < -N \text{ and } n > N \qquad (5.6)$$

The impulse response is finite with a duration of 2N + 1 and is symmetric with h(n) = h(-n), which results in a linear phase response.

The transfer function of this filter is given by:

$$H(e^{j\theta}) = \frac{1}{2N + 1}\sum_{n=-N}^{N} e^{-j\theta n} = \frac{1}{2N + 1}e^{j\theta N}\sum_{n=0}^{n=2N} e^{-j\theta n}$$

$$= \frac{1}{2n + 1}\,\frac{\sin\left[(2N + 1)\frac{\theta}{2}\right]}{\sin\left(\frac{\theta}{2}\right)} \qquad \theta = \omega T_s = 2\pi f/f_s$$

$$\cong \mathrm{sinc}\left[(2N + 1)\frac{\theta}{2}\right] \qquad \text{for } f << f_s \qquad (5.7)$$

In Fig. 5.3 - 5.5 are shown the modulus of the frequency response $|H(e^{j\theta})|$ of a moving average filter, for N = 1, N = 16 and N = 32 ($|H(e^{j\theta})|$ is periodical with 2π).

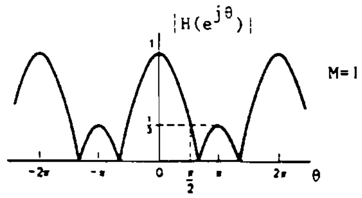


Fig. 5.3: $|H(e^{j\theta})|$ of a moving average filter, N = 1.

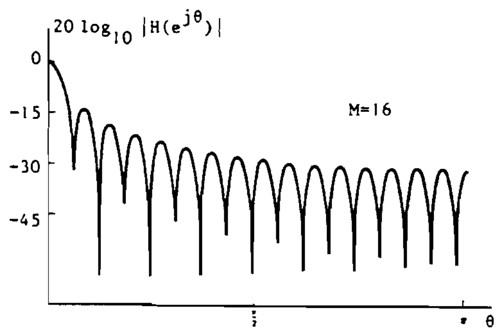


Fig. 5.4: $|H(e^{j\theta})|$ of a moving average filter, N = 16.

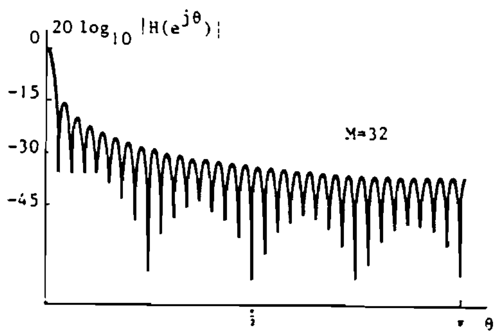


Fig. 5.5: $|H(e^{j\theta})|$ of a moving average filter, N = 32.

5.3 Decimation

In the design of digital filters it is often favorable to lower the sampling frequency. The effect of lowering the sampling frequency will be discussed in this section [6], [7].

A system that has the following relationship between input and output signal is called a decimator.

$$y(n) = x(Rn) \tag{5.8}$$

where R is a integer. The symbol for a decimator is given in Fig. 5.6.

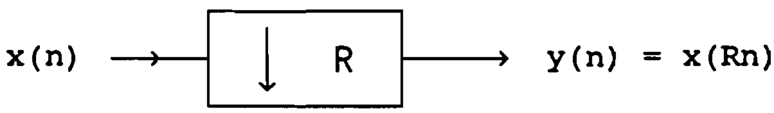


Fig. 5.6: Decimator.

In Fig. 5.7 is shown an example of the effect of a decimator.

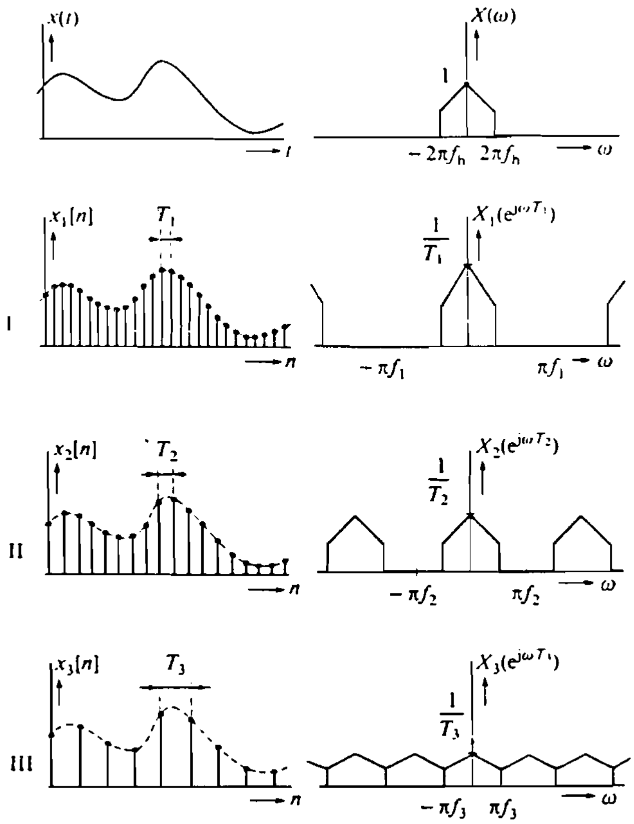


Fig. 5.7: Effect of a decimator.

Lowering the sampling frequency reduces the amount of calculations necessary in a certain time interval. The reduction is only meaningful if no information is lost. Or in other words if x(n) can be recovered from y(n).

The spectrum of the continuous time signal x(t), $X_c(j\omega)$, has to be band limited to the interval $-\pi/Tx \le \omega \le \pi/Tx$ ($f_s \ge 2f_{max}$) to prevent aliasing to occur (Nyquist criterion). The spectrum of the discreet time signal x(n) is periodical with the fundamental interval $-\pi/Tx \le \omega \le \pi/Tx$ (period f_s).

Sampling of x(n) with a sampling rate $1/Ty = R/Tx = f_s/R$ results in the sequence y(n) = x(nTy) = x(nRTx) = x(Rn). The spectrum of y(n) is periodical with the fundamental interval $-\pi/Ty \le \omega \le -\pi/Ty$ (period f_s/R).

If the highest occurring frequency component in x(t) is lower than $\pi/Ty = f_s/2R$, x(n) can be completely recovered (see Fig. 5.7).

An example where decimation is employed is an integrate and dump filter. An integrate and dump filter (used by detectors) is a moving average filter from which the output sampling frequency is lowered to reduce the total amount of calculations.

5.4 Efficient design of a lowpass filter

In Fig. 5.8 is shown an example of a multi-stage lowpass filter.

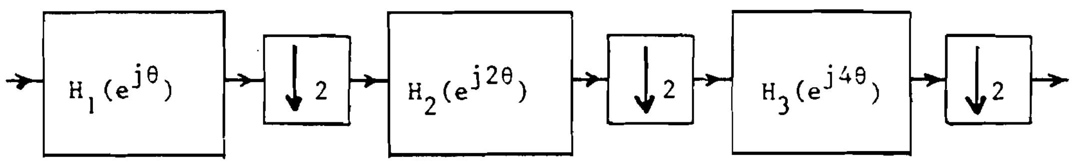


Fig. 5.8: Multi-stage lowpass filter.

Fig. 5.9 shows the spectra at different points in the multi-stage filter.

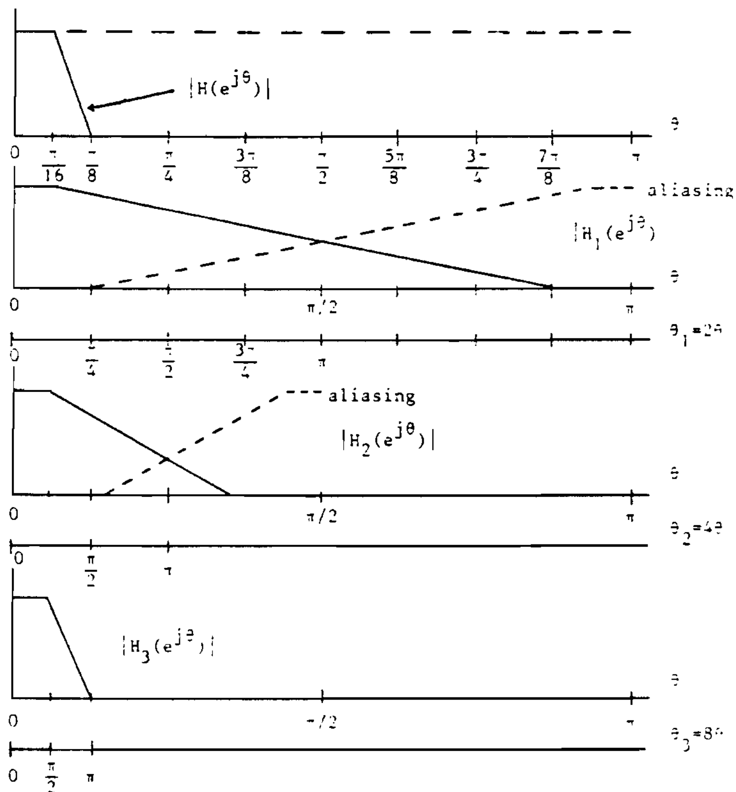


Fig. 5.9: Spectra in multi-stage lowpass filter.

As can be seen from the spectra (Fig. 5.9), aliasing occurs in the transition band of the sub-filters. However, the final spectrum contains no undesired frequency components. The transition region of $H(e^{j\theta})$ is $\pi/16 \le |\theta| \le \pi/8$. The filter is realized with 3 sub-filters, H1, H2 and H3. The transition regions of these filters are given below.

H1	$\pi/16 \le \|\theta\| \le 7\pi/8$
H2	$\pi/8 \le \|\theta\| \le 3\pi/4$
H3	$\pi/4 \le \|\theta\| \le \pi/2$

The steepness of the sub-filters is much smaller than the steepness of the total filter. With this multi-stage filter the same results can be achieved as with a single-stage filter. However the amount of calculations needed for this filter is much smaller than of a single-stage filter. Furthermore, the decimation also lowers the amount of calculations. It holds in general that it is wise to adapt the sampling frequency to the bandwidth of a signal to minimize the amount of calculations required.

6 Digital detector design

6.1 Specifications digital detector

The EUT detector to be used for the Intelsat-V beacon receiver system should at least meet the same specifications as the DNL detector ([8], [9], appendix B), which is currently used in the ground station for the Olympus satellite. The EUT design must be interchangeable with the DNL design, so that it can be applied in the Olympus measurement system as well, without modifying this system (small modifications are allowed).

The DNL detector is designed for an IF input signal of 100 kHz. To digitize the input signal the detector employs a track-hold (T/H) amplifier and a 12-bit A/D converter. A track-hold amplifier is used in conjunction with an A/D converters to track the rapidly changing analog input signal and hold this signal constant while the converter is performing a conversion. With the track-hold amplifier MN375, which is applied in the DNL design, a full power signal of about 400 kHz can be sampled with 12-bit accuracy. If the accuracy restrictions are less stringent, a much higher IF is feasible (9-bit accuracy for a 3.2 MHz input signal). More information (speed, accuracy, prices) about commercially available track-hold amplifiers is given in appendix C.

The 10 MHz PLL receiver, which is employed in the Intelsat measurement system, employs a second IF of 125 kHz. The digital detection has to take place at this IF, thus the EUT detector should be designed to operate at an IF of at least 125 kHz. In the Olympus measurement system an anti-aliasing 100 kHz bandpass filter, with a bandwidth of approximately 2 kHz, is used before the DNL detector. For the PLL receiver the same type of filter with a center frequency of 125 kHz will be applied. For an IF of 125 kHz, track-hold amplifiers are commercially available.

The sampling frequency should satisfy:

$$f_s \geq 2B_n \tag{4.9}$$

$$f_s = \frac{4}{2n + 1} f_0 \qquad n = 0, 1, 2, 3, \ldots \tag{4.10}$$

The DNL detector employs a sampling frequency of 8.163 kHz (n = 30). In fact a lower sampling frequency can be used (n = 49, f_s = 4.04 kHz) if an ideal bandpass filter is employed. However, the attenuation in the stop band of the bandpass filter employed is not very high, thus a higher sampling frequency is employed to avoid aliasing. For the EUT design a sampling frequency of 8.196 kHz (n = 30) is selected.

The DNL detector is provided with an integrate-and-dump filter, which has a sinc-characteristic. This means a large roll-off in the passband and low attenuation in the stop band. In the first developed EUT detector, the same filter is applied as in the DNL detector. However, with the EUT detector better filtering is possible. The EUT detector should have filter characteristics as follows:

Bandwidth (-3 dB)	=	0.5 Hz
Ripple in pass band	<	0.1 dB
Attenuation in stop band	>	40 dB

The output sampling frequency must be 1 Hz. This means that aliasing will occur for a bandwidth of 0.5 Hz. In the actual filter the bandwidth must be chosen smaller to prevent aliasing. Also a linear phase response in the passband is required.

For the realization of the above mentioned filter, a FIR or IIR filter can be applied. Table 6.1 shows a list of advantages and disadvantages of these two filter classes (see also chapter 5). Considering these advantages and disadvantages, a FIR filter is selected to be implemented in the EUT detector. To realize a FIR filter for real time signal processing, a fast processor is required. A TMS320C25 (appendix E), especially designed for digital signal processing, is applied in the EUT detector.

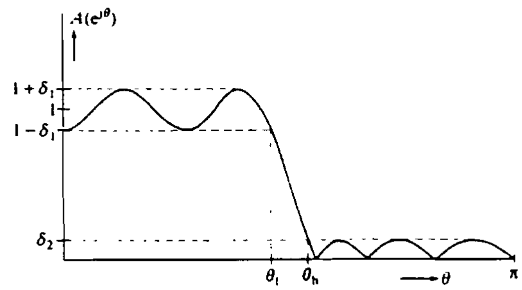
Table 6.1: Advantages and disadvantages of FIR and IIR filters.

	FIR filter	IIR filter
Phase response	can have exactly linear phase	linear phase can only be approximated
Stability	always stable	can be unstable
Quantization noise	little effect	due to quantization noise filter can be unstable
Size	large	small

The dynamic range of the DNL detector is 48 dB. For the EUT detector to be used for the Intelsat system a dynamic range of 55 dB has been selected. This is more than sufficient for the Intelsat amd Olympus system.

6.2 FIR filter design

The FIR filter for the EUT detector is developed by Kamperman [10]. The software with this filter came available during this project. The FIR filter cannot be realized with one section. To meet the specifications of the filter with one section, requires a FIR filter with more than 100.000 coefficients. The FIR filter has been developed using the method described in section 5.4. This section describes how to realize efficiently a lowpass filter using a number of sub-filters in cascade. As a result the FIR filter finally consists of 11 Kaiser window half band filters and 1 equiripple filter in cascade. The measured characteristics of the entire lowpass FIR filter are listed in table 6.2. A explanation of the filter characteristics is shown in Fig. 6.1.



$0 - \theta_1$ pass band
$\theta_1 - \theta_h$ transition band
$\theta_h - \Pi$ stop band

Fig. 6.1: Lowpass FIR filter characteristics.

Table 6.2: Measured FIR filter characteristics.

ripple in passband δ_1	0.8 dB
Attenuation in stop band δ_2	57 dB
pass band	0.0 - 0.3 Hz
transition band	0.3 - 0.4 Hz
stop band	0.4 - 0.5 Hz
decimation factor	4096
sampling frequency input signal	4081 Hz
sampling frequency output signal	0.996 Hz
(IF is 100 kHz)	

For an IF of 125 kHz the same filter can be applied, the characteristics are then slightly different. For an IF of 125 kHz the sampling frequency of the input signal of the filter is 4098 Hz. The input sampling rate of the filter is half of the sampling frequency (8198 Hz) because the sampled input signal is split into an in-phase and quadrature channel.

It would be possible, if desired, to change the number of filter sections used. Doing this the changes the bandwidth and the output sampling frequency of the filter. DIP switches could be applied for this purpose, so that software selects the number of sections used.

After the FIR filtering the digital signal is transformed to an analog signal using a D/A converter. The filter characteristics of the detector are determined by the FIR filter and the D/A converter. The D/A converter acts as a zero-order hold circuit, which has the following transfer function

$$|H_{D/A}(\omega)| = \frac{2\sin(\omega T/2)}{\omega} \tag{6.1}$$

Therefore, the transfer function of the detector using a FIR filter is given by

$$|H_{det}(\omega)| = |H_{FIR}(\omega)| \cdot |H_{D/A}(\omega)| \tag{6.2}$$

The 0.8 dB ripple in the passband of the FIR filter is probably caused by the D/A converter. To lower this ripple the output sampling rate should be raised.

6.3 A/D converter

6.3.1 Resolution of A/D converter

In [11] equations are given for the amplitude and phase resolution of a system using I-Q detection. Suppose the amplitude A of the input signal of the A/D converter is l.q, where q is the step size of the A/D converter, and l an integer. The amplitude resolution (in dB) of the system is given by:

$$\Delta A_{dB} = 10\log\left(1 + 2\frac{l\sqrt{2} + 1}{l^2}\right) \tag{6.3}$$

As can be seen from Eq. 6.3 the amplitude resolution is dependent of the level of the input signal. The smaller the input signal, the smaller the amplitude resolution.

The phase resolution is given by:

$$\Delta\phi \cong \tan\Delta\phi = \frac{q\sqrt{2}}{l.q} = \frac{\sqrt{2}}{l}\ \text{rad} = \frac{360}{2\pi}\frac{\sqrt{2}}{l}\ \text{degrees} \tag{6.4}$$

If the amplitude resolution is ΔA for a certain amplitude then the total amount of levels l needed to represent this amplitude is given by:

$$l = \frac{1 + \sqrt{10^{\Delta A/10}}}{10^{\Delta A/10} - 1}\sqrt{2} \qquad \Delta A \text{ in dB} \tag{6.5}$$

For the Intelsat measurement system a dynamic range of approximately 23 dB is wanted. Suppose an amplitude resolution of 0.1 dB is required in case of maximum attenuation. Using Eq. 6.5 results in l = 122. The phase resolution is then 0.9 degrees (using Eq. 6.4).

Maximum attenuation A_{min} = 122.q
Maximum signal (+23 dB) A_{max} = 14.122.q = 1723.q
(clear sky)

The maximum number of levels of the A/D converter must be 2 x 1723 = 3446 (taken into account a factor 2 since both positive and negative signals must be sampled). Thus at least a 12-bit A/D converter is required for the Intelsat measurement system (2^{12}= 4096).

6.3.2 Selection of A/D converter

Considering the many types of A/D converters on the market, the complex manner in which converter specifications relate to a specific system application, and the fact that prices of converters range from less than $10 to several thousands of dollars, selecting the most economical converter for an application is not an easy task.

To determine the converter performance requirements, two types of specifications should be considered: speed and accuracy. Speed-dependent specifications include conversion time, bandwidth, settling time of the input circuitry, etc. Accuracy-dependent specifications include resolution, relative accuracy, differential linearity, noise, quantization uncertainty, etc. Furthermore, for this application, the A/D converter should be easily interfaced to the TMS320C25, and the price must be reasonable.

In most systems an A/D converter is proceeded by a track-hold amplifier. The use of a track-hold amplifier increases the highest-frequency signal, of a given amplitude, that may be encoded within the resolution of the converter. When no track-hold amplifier is used, the highest-frequency signal is mainly determined by the conversion time of the A/D converter. When using a track-hold amplifier, the highest-frequency signal is mainly determined by the aperture time uncertainty of the track-hold amplifier.

The following indicates the improvement possible with a track-hold amplifier. If the input signal is a full-scale sine wave, $A\sin(2\pi ft)$, the maximum rate-of-change is at the zero-crossing, and (as can be found by differentiating with respect to t) is equal to:

$$\frac{dx}{dt} = 2\pi fA \qquad (6.6)$$

For full accuracy of the A/D converter, the change of the input signal Δx in the conversion time Δt, is to be less than 1/2 LSB.

$$\frac{q}{2\Delta t} = \frac{2^{-M}A}{\Delta t} \geq \frac{dx}{dt} = 2\pi f A \tag{6.7}$$

where

q step size of A/D converter [V]

M number of bits used for conversion

Δt conversion time [s]

The highest frequency of the input signal that can be applied to the A/D converter is:

$$f_{max} \leq \frac{2^{-M-1}}{\pi\Delta t} \tag{6.8}$$

For instance, f_{max} of a 12-bit A/D converter with a conversion time of 20 μs, is approximately 2 Hz.

Using a track-hold amplifier reduces the uncertainty in the time of measurement from the A/D converter's conversion time to the aperture jitter of the track-hold amplifier, thus effecting an improvement in f_{max} by the ratio of the conversion time to the aperture time uncertainty. Since 2 ns or better is routinely available in track-hold amplifiers designed for operation with 12-bit converters, an improvement of 10,000 : 1 is quite feasible, assuming that the track-hold amplifier has adequate bandwidth.

The requirements for the A/D converter of the digital detector are

- Input signal frequency 125 kHz
- Sampling frequency 8.196 kHz
- Resolution at least 12 bits
- Easily interfaced to TMS320C25 signal processor
- Low power consumption if possible

The DNL detector employs an A/D converter in combination with a track-hold amplifier. This track-hold amplifier has an aperture uncertainty of 100 ps. This track-hold amplifier is, when used in combination with a 12-bit A/D converter, suitable for full power signals up to 400 kHz. This system has several disadvantages: the high power consumption (typically 1.5 W) of the track-hold amplifier; two large ICs are required for the A/D conversion, which results in a larger print design. Furthermore the track-hold amplifier used, is not easily available and very expensive (400 NLG). For this application the applied track-hold amplifier exceeds the requirements.

After studying many available A/D converters and track-hold amplifiers, the AD7870 12-bit sampling A/D converter was selected (see appendix E). The AD7870 contains a 12-bit A/D converter and a track-hold amplifier. The AD7870 has a fast microprocessor interface. Data access times of 57 ns make the AD7870 compatible with modern 8- and 16-bit microprocessors and digital signal processors. The AD7870 can easily be interfaced to the TMS320C25 signal processor (see Chapter 7, section 7.4). The price of this A/D converter is reasonable: approximately 40 NLG. The power consumption of this IC is low: typically 60 mW.

The AD7870 operates from +/- 5 V power supplies, accepts bipolar input signals of +/- 3 V and can convert full-power signals up to 50 kHz to 12-bit accuracy. This seems too slow since the frequency of the input signal of the A/D converter is 100 or 125 kHz. However, if a full-power signal of 100 kHz is converted with this converter, an error occurs in the least significant bit (LSB) only. This means an error of 0.004 dB. For the Intelsat measurement system the accuracy requirements are not stringent. A 0.1 dB accuracy is wanted over a range of approximately 23 dB. This means that a much higher input frequency can be applied as long as the error $\leq$ 0.1 dB. The error is maximal for a full-power input signal. The total number of levels required for a full-power signal is 2 x 122 = 244 (see section 6.3.1). This means that only 8 bits of the 12 bits are used, and that a input frequency of 16 x 50 kHz = 800 kHz can be applied.

However, there is another restriction on the highest usable input frequency, the bandwidth of the track-hold amplifier. The bandwidth of the track-hold amplifier of the AD7870 is more than sufficient for this application. The 0.1 dB cutoff frequency occurs typically at 500 kHz.

6.3.3 Enhancement of A/D resolution

Quantization error can be reduced (resolution enhanced) when ensemble averaging will take place over a sufficient number of quantized input samples. When noise, having a uniform probability density function, is injected into a 1-bit A/D converter and ensemble averaging is carried out, this results in a perfect linear system [11]. In telecommunication systems the continuous input signal to be quantized includes zero mean additive white Gaussian noise (AWGN) with a variance proportional to the equivalent input noise bandwidth. The rms value of the AWGN must have a certain minimum value related to the quantization step-size of the A/D converter, such that a great number of the quantized samples are consecutively random scattered about several quantization levels. Averaging over a sufficient number of quantized samples will then result in an accurate estimate of the input signal with an equivalent resolution which can be much better than the physical resolution of the A/D converter. The factor γ, which gives the ratio of rms noise voltage and step-size of the A/D converter, is defined as follows

$$\gamma = \sigma_n / q_m = (\sqrt{\eta_0 B_n}\,) / q_m \tag{6.9}$$

where

γ = ratio of noise voltage and step-size A/D converter
σ_n = rms value of AWGN-process [V]
q_m = step-size of a physical M-bit A/D converter [V]
η_0 = thermal noise power density [V^2/Hz]
B_n = input equivalent noise bandwidth [Hz]

It is obvious that for large values of γ, input quantized samples are scattered about more quantized levels, and averaging has to be performed over a greater ensemble of quantized levels in order to acquire the same resolution than with small value of γ. A suitable choice for γ is 0.5 [11]. If a smaller γ is applied non-linearity will occur. However, a larger γ will result in better linearity but also results in a larger sampling frequency.

If with a M-bit A/D converter a L-bit (L > M) resolution is wanted the sampling frequency must satisfy [11]

$$f_s = \frac{4}{t_m}\left(\frac{\sigma_n}{q_m^2}\right)^2\left(\frac{2^L - 1}{2^M - 1}\right)^2 \tag{6.10}$$

where

t_m measuring time [s]

σ_n rms value of AWGN proces [V]

q_m step-size A/D converter [V]

However, the linearity of a system where the resolution is enhanced, is never better than the linearity of the applied A/D converter. Most A/D converters have a non-linearity error of 1/2 LSB. The resolution of the applied A/D converter in the EUT detector can be enhanced as has been demonstrated in [4], but the linearity will not be better than of the applied A/D converter. Only if an A/D converter is applied with a smaller non-linearity error than 1/2 LSB it is useful to enhance the resolution.

6.4 D/A converter

6.4.1 Resolution of D/A converter

The measured amplitude is converted to a logarithmic scale (in the detector software) before it enters the D/A converter. If a minimal resolution of 0.1 dB and a total dynamic range of 55 dB is wanted, a D/A converter with 550 levels is required for the amplitude output signal. This can be realized with a 10-bit D/A converter. If a phase resolution of 1 degree is needed, 360 levels are required. This can be realized with a similar 10-bit D/A converter.

6.4.2 Selection of D/A converter

Selecting a D/A converter for the detector is not as difficult as selecting the A/D converter. The requirements of the D/A converter are far less stringent than the requirements of the A/D converter.

A 10-bit D/A converter would be sufficient for the EUT detector. However, because in the future a different output scale might be wanted, a 14-bit D/A converter is selected, the AD7840. Moreover, this D/A converter is especially suitable for a digital signal processor (DSP), easily available, and low priced. The main features of the AD7840 are:

- Complete 14-bit voltage output D/A converter
- Parallel and serial interface capability
- Interfaces to high speed DSP processors
- 45 ns $\overline{WR}$ pulse width
- Low power 70 mW typ.
- Operates from ±5 V supplies
- Low price, about 20 NLG

6.5 Extraction of sampling signal from detector input signal

If the frequency of the input signal of the detector f_0 and the sampling frequency f_s are not directly related ($f_s = 4f_0/(N + 1)$, Eq. 4.10), serious measurement errors will occur as has been demonstrated in the report of Manders [11]. The measured amplitude is given by:

$$A_m = \left\{ \left(\frac{1}{N} \sum_{k=0}^{f_s t_m} A\cos(k\alpha + \phi) \right)^2 + \left(\frac{1}{N} \sum_{k=0}^{f_s t_m} A\sin(k\alpha + \phi) \right)^2 \right\}^{1/2} \qquad (6.11)$$

where $\alpha = 2\pi \frac{\Delta f_0}{f_s}$

A_m Measured amplitude
A Amplitude
N Number of samples taken for the calculation of one output sample
f_s Sampling frequency [Hz]
f_0 IF Input frequency [Hz]
Δf_0 Frequency deviation from ideal frequency $f_0 = (2n + 1)f_s/4$
t_m Averaging time [s]

The equation for the measured amplitude is determined assuming an integrate-and-dump filter is employed. In case a FIR filter is used for the lowpass filtering, then the samples are not just added, but added with different weights. However, approximately the same error will occur in the measured amplitude.

In order to keep the measurement error small, a phase-locked-loop must be used to extract the sampling signal from the input signal of the detector. In the EUT PLL receiver the 10 MHz IF signal is down converter to a 125 kHz IF. This 125 kHz signal has to be employed for the digital detection. The 125 kHz signal is locked to a 125 kHz reference oscillator. This 125 kHz reference signal is used to extract the sampling signal (see section 9.3).

7 Digital detector hardware

The recently developed EUT detector [12] has a serial output port for serial communication with a PC. However, the data-acquisition system of the Intelsat-V beacon receiver can handle analog signals only. Therefore two D/A converters are added (for amplitude and phase).

The clock frequency has been enhanced for the program containing a FIR filter. For this reason faster EPROMs are applied.

Furthermore a new print has been developed with the same connector and same print size as the DNL detector, resulting in a fully interchangeable detector.

7.1 Block diagram digital detector

The block diagram of the digital detector is shown in Fig. 7.1. The complete circuit diagram is shown in appendix D.

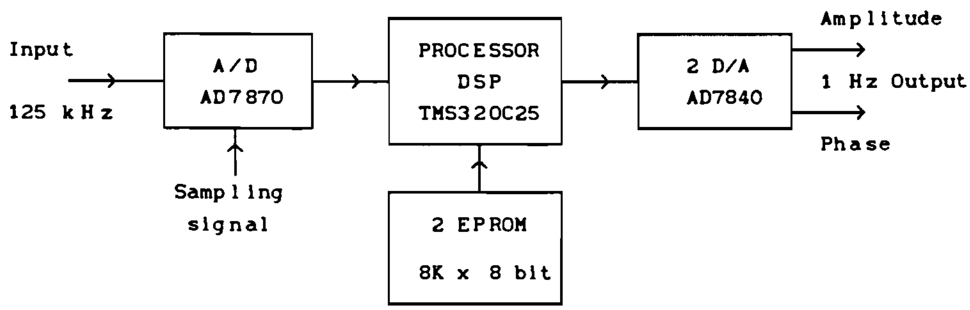


Fig. 7.1: Block diagram digital detector.

7.2 Digital signal processor TMS320C25

The detector employs the digital signal processor TMS320C25 (appendix E, [13]). This processor contains internal ROM and RAM. The ROM is for this application not useful because the system is still in development (hardware and software). In the future a version with internal EPROM (TMS320E25) will be commercially available, which makes a more compact design possible (no external EPROM necessary). The E25 is pin-compatible with the C25, thus the C25 can be replaced when the E25 will be commercially available.

The processor is provided with an address decoder 74138 (3 input, 8 output). With address lines A0 - A2 it is possible to select 8 input and 8 output peripherals. When the TMS320C25 executes an IN or OUT instruction, the peripheral address is placed on the address bus and the $\overline{\text{IS}}$ line goes low, indicating that the address on the bus corresponds to an I/O port. A low level at $\overline{\text{IS}}$ enables the address decoder 74138, and one of the outputs (Y0 - Y7), corresponding to the address on the bus, is brought low. When a output is brought low, a peripheral is selected. In this design only 3 input/output (I/O) ports are used.

The corresponding peripherals are listed below.

Port Y0: Dip switches
Port Y1: D/A converter 1 (DAC1)
Port Y2: D/A converter 2 (DAC2)

The reset circuit used, performs a power-up reset. The TMS320C25 is reset when power is applied.

Two versions of the detector are developed. One version contains an integrate and dump filter, and the other version contains a FIR filter. The version, which contains an integrate and dump filter, uses an 8 MHz clock. For the version, which contains a FIR filter, a clock of 8 MHz is not sufficient to perform all real-time calculations. Therefore a clock of 20 MHz is applied.

The circuit diagram of the processor section is shown in Fig. 7.2.

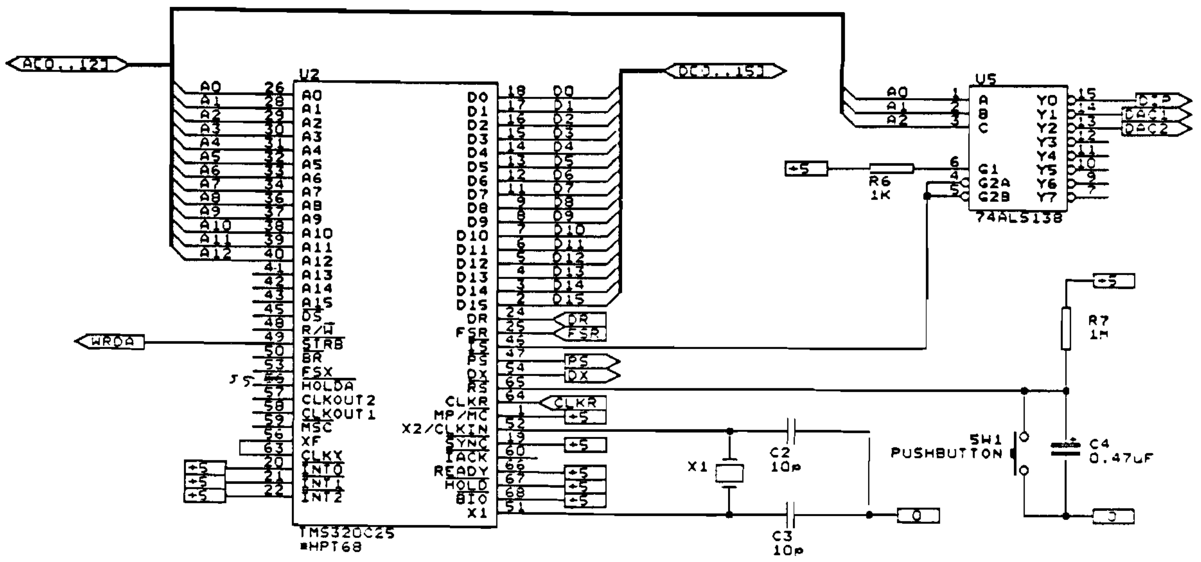


Fig. 7.2: Processor section.

The main connections of the processor section are listed below.

A0-A15, parallel address bus, A0 (LSB) through A15 (MSB).

D0-D15, parallel data bus, D0 (LSB) through D15 (MSB).

The MP/$\overline{MC}$ (microprocessor/microcomputer) pin determines the memory map of the processor [13]. This pin is set high meaning that the lower 4 K words of program memory are external, and the internal 4 K ROM is not used.

The TMS320C25 has the capability to interface to memory and peripherals that cannot be accessed in a single cycle. The number of cycles in a memory or I/O access is determined by the state of the READY input. The READY input indicates that an external device is prepared for the bus transaction to be completed. If the device is not ready (READY = 0), the processor waits one cycle and checks ready again. The automatic generation of one wait state can be accomplished by the use of the micro state complete ($\overline{MSC}$) signal. By connecting $\overline{MSC}$ with the READY input one wait state is generated.

The print is provided with a jumper to connect the READY pin to the $\overline{MSC}$ pin, to generate a wait state if necessary. Currently, the READY pin is connected to a high level, which indicates no wait states are inserted and the memory accesses are performed in a single machine cycle.

$\overline{PS}$ is used for selecting the EPROMs.

$\overline{IS}$ is used to select the address decoder IC2, 74138.

The TMS320C25 can use either its internal oscillator or an external frequency source for a clock. The internal oscillator is enabled by connecting a crystal across X1 and X2/CLKIN (Fig. 7.2). The detector employs the internal oscillator. For the detector employing an integrate and dump filter an 8 MHz crystal is applied, for the version using a FIR filter a 20 MHz crystal is applied.

7.3 EPROM

No external RAM is used, the internal RAM block (544 words) is sufficient for the integrate and dump filter and for the FIR filter. However, if in the future more RAM is required it is possible to add external RAM. It is also possible to use the latest version of the second generation signal processors, the TMS320C26. This processor is completely pin-compatible with the C25 version and contains 1.5 K internal RAM.

The external memory consists of two 8 K x 8-bit EPROMs (16-bit data-bus). There are 8 K x 16-bit EPROMs, however, these EPROMs are very expensive and hardly available. With slower EPROMs the data output turn-off can be slow, for that reason the EPROMs are connected with the data bus via a bustranceiver 74F245. When no wait states are used these bustranceivers are not necessary. The EPROMs and the bustranceivers are selected by the $\overline{PS}$ signal from the TMS320C25.

For the integrate and dump filter, two slow (cheap) 8 K x 8-bit EPROMs (27C64, access time 150 ns) are employed, the clock frequency is set to 8 MHz. A maximum of about 11 MHz is possible with these EPROMs without wait states (according to the data book [13].

For the FIR filter a 20 MHz clock is applied. Because of more real-time calculations a 8 MHz clock is not sufficient. According to the Texas Instruments data book [13], an EPROM with an access time of about 80 ns is required at a clock rate of 20 MHz. For this reason two fast and expensive (about 50 NLG) 8 K x 8-bit EPROMs (27HC64-70, access time 70 ns) are applied. These EPROMS can be used up to a clock frequency of about 21 MHz without inserting wait states. However, tests with the slow 150-ns EPROMs showed that these EPROMS also could be used with a clock frequency of 20 MHz. These EPROMs only cost about 5 NLG.

The main connections of the EPROM section are listed below.

A0-A12, parallel address bus.

D0-D15, parallel data bus.

$\overline{PS}$ (from TMS320C25) is used to select the EPROMs and the bustranceivers.

DIR is connected to +5 V to set the direction of the bidirectional bustranceiver.

The circuit diagram of the EPROM section is shown in Fig. 7.3.

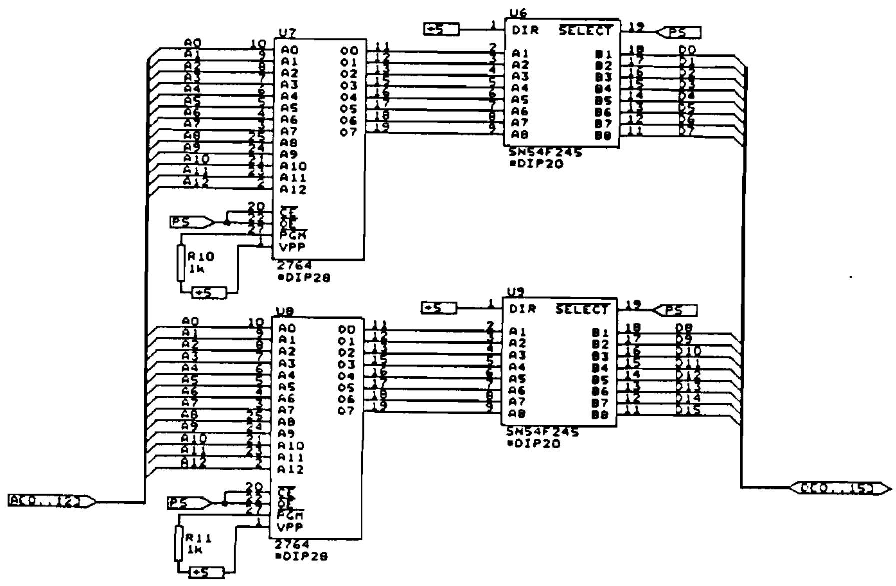


Fig. 7.3: EPROM section.

7.4 12-bit A/D converter

For sampling of the 125 kHz input signal, a 12-bit sampling A/D converter, AD7870, is employed (for specifications see appendix A).

The circuit of the 12-bit A/D converter section is shown in Fig. 7.4.

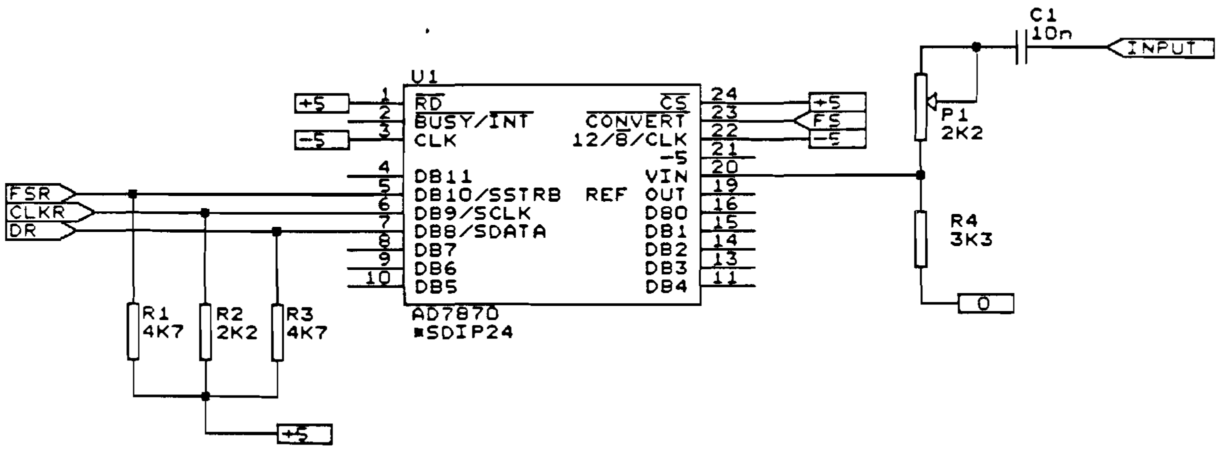


Fig. 7.4: 12-bit A/D converter section.

In this application the AD7870 is configured for serial interfacing, which means that only three lines to the processor are needed. For parallel operation much more lines are necessary, which results in a more complicated printed circuit board (PCB). For serial operation a 16-bit word (four leading zeros, followed by the 12-bit conversion result, starting with the MSB) is transmitted from the A/D converter to the processor with a baud rate of 2.5 Mbit/s. The maximum sample rate is about 100 kHz. Further, the TMS320C25 is configured for continuous clock operation. The AD7870 will not interface correctly to the TMS320C25 if the AD7870 is configured for a noncontinuous clock. Data is clocked into the data receive register (DRR) of the TMS320C25 during conversion. When a 16-bit word is received by the TMS320C25 it generates an internal interrupt to read the data from the DRR.

The main connections of the AD7870 are listed below.

SSTRB, SCLK, SDATA are connected with FSR, CLKR, DR (of TMS320C25) respectively. These signals control the serial data transfer.

$\overline{\text{CONVST}}$ is connected with the external sampling frequency of 8.196 kHz. A low to high transition on this input puts the track-hold amplifier into its hold mode and starts conversion.

V_{in} is connect with the 125 kHz input signal. A highpass filter is applied to reject DC-signals. With variable resistor P1 the input range can be changed (6 V_{pp} - 10 V_{pp}).

12/$\overline{8}$/CLK is set at -5 V to configure the AD7870 for continuous clock operation.

7.5 14-bit D/A converter

The data acquisition system requires analog input signals. For this reason the digital data (amplitude and phase) are converted to analog signals by two D/A converters.

In this system the AD7840 D/A converter is selected (data sheets see appendix E). The AD7840 is a fast, complete 14-bit voltage output D/A converter. The analog output from the AD7840 provides a bipolar range of ±3 V. Full power signals up to 20 kHz can be created. In this application only a very low output frequency is required (1-16 Hz).

In this system the parallel data bus of the AD7840 is used. The high speed operation of the AD7840 allows an interface to the TMS320C25 (at 20 MHz) with a minimum of external circuitry. If a higher clock is used (40 MHz) more circuitry is required. The address decoder 74138 (IC2) is used to decode the address of the D/A converters. When the TMS320C25 executes an OUT instruction, the DAC address is placed on the address bus and the $\overline{\text{IS}}$ line goes low (see Fig. 7.2), indicating that the address on the bus corresponds to an I/O port and not to external data or program memory. A low level at $\overline{\text{IS}}$ (from TMS320C25) enables the 74138 decoder, and the DAC1 or DAC2 output is brought low and one of the AD7840 is selected. The data appearing on the data bus is latched into the D/A converter by $\overline{\text{STRB}}$ (from TMS320C25).

The schematic diagram of the 14-bit D/A converter section is shown in Fig. 7.5.

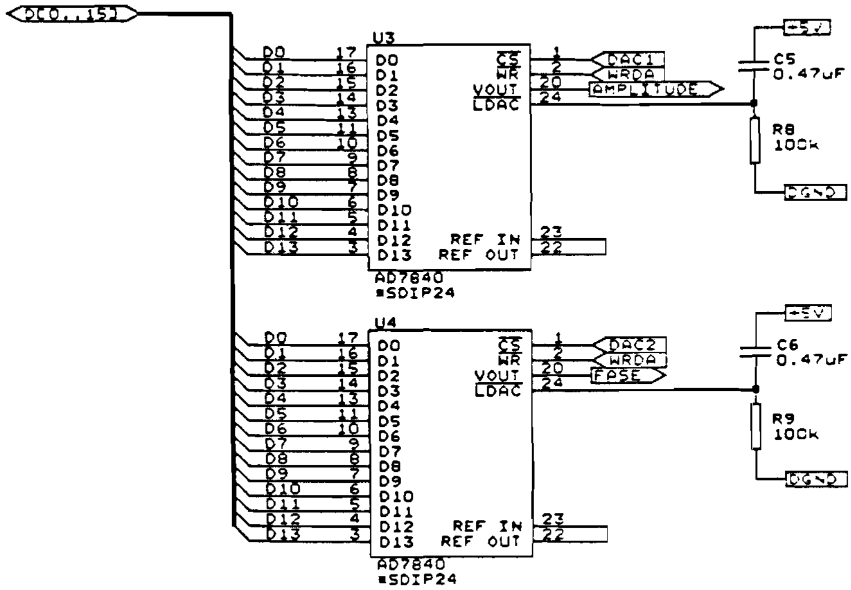


Fig. 7.5: 14-bit D/A converter section.

The main connections of the 14-bit D/A converter section are listed below.

D0-D13, parallel data bus.

$\overline{\text{CS}}$ (chip select) is connected with one output (DAC1 or DAC2) of the address decoder 74138. This is an active low logic input which is used in conjunction with $\overline{\text{WR}}$ to load data to the input latch.

$\overline{\text{WR}}$ is connected with $\overline{\text{STRB}}$ (from TMS320C25) and is used in conjunction with $\overline{\text{CS}}$ to load parallel data.

REF OUT is connected with REF IN, the AD7840 is operated with internal reference. REF OUT = 3.00 V ± 0.01 V (± 60 ppm/°C max).

V_{out} is the buffer amplifier output voltage. Bipolar output range, ±3 V with REF IN = +3 V.

$\overline{\text{LDAC}}$. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal. The AD7840 should be powered-up with $\overline{\text{LDAC}}$ high. In this application the $\overline{\text{LDAC}}$ input is hardwired low. As a result the DAC latch and analog output are updated on the rising edge of $\overline{\text{WR}}$. A single OUT instruction, therefore, loads the input latch and updates the output.

7.6 Input/Output

The print is provided with 8 dip-switches. These dip-switches are used in the integrate-and-dump filtering to set the bandwidth of the filter and the output data rate. The FIR filter software makes currently no use of the switches. They could be used to change parameters of the filter if desired. The address decoding of these switches is the same as for the D/A converters (see section 7.2).

For serial communication the TMS320C25 is provided with a serial data transmit output port (DX-pin). To convert the TTL signal of the processor to a RS232 signal, a TTL-RS232 converter, MC1488, is employed. It is possible to make a serial connection with a PC. The currently installed software makes no use of this port, however, in the past, this port has been used to test the software.

The schematic diagram of the Input/Output section is shown in Fig. 7.6. Also is shown the 64-pole (32 x 2) connector, which is mounted on the print.

The detector requires two analog power supplies (+/-) and one +5 V digital supply. The range for both analog supplies is 12 to 15 V. The -5 V required for the A/D and D/A converters is generated by a voltage regulator from the -15 V power supply input.

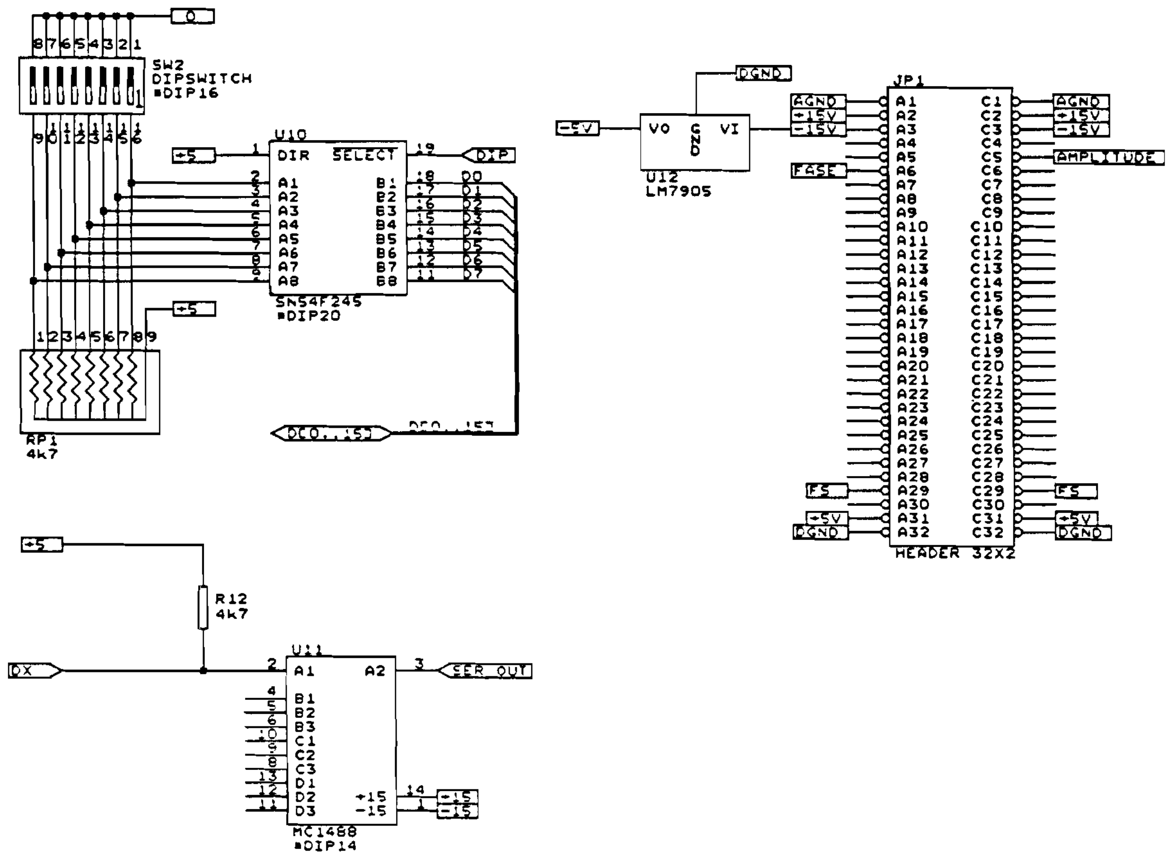


Fig. 7.6: Input/Output section.

7.7 Printed circuit board design

The printed circuit board (PCB) layout is shown in appendix D. This PCB layout has been developed as follows. First the circuit diagram is drawn using the electronic drawing program Orcad. The central technical services of EUT designed the PCB layout using this circuit drawings.

In this layout the analog and the digital ground are separated and connected at a single point. The analog lines are separated as much as possible from the digital grounds to prevent spikes on the analog lines. To the power supply connections of all the ICs bypass capacitors are connected.

8 Digital detector software

There are two versions of the modified EUT detector. One employs a modified version of the program TMSROM. TMSROM is a translated and upgraded version of the program used in the DNL detector [8], [9]. The program contains an integrate-and-dump filter, and is developed by Linsen [14], Vermeir [12], and Opdenkamp [15]. The other version uses a modified version of the program DSPFIR where a FIR filter is implemented. DSPFIR is developed by Kamperman [10]. In this chapter the basic structure of the modified versions of the programs TMSROM and DSPFIR is explained. The program DSPFIR is developed using TMSROM and basically functions in the same manner.

Both unmodified programs contain a section for serial communication with a PC. This section consumes a large part of processor time. For the Intelsat-V beacon receiver system this serial link is not needed. In the modified programs used for the Intelsat system, this software part is removed. A section for the controlling of the D/A converters is added. The listings of the modified software are given in appendix F.

8.1 I-Q detection in software

The programs TMSROM and DSPFIR employ the I-Q detection scheme as described in chapter 4. After sampling, the discrete signal is split into two channels, an I and a Q channel. The I and Q channel must be multiplied by respectively $\cos(2\pi kT_s/4)$ and $\sin(2\pi kT_s/4)$. Table 8.1 shows the values of the cos and sin at the sampling moments.

Table 8.1: $\cos(2\pi kT_s/4)$ and $\sin(2\pi kT_s/4)$ at sampling time k and n is an integer.

	k = 4n	k = 4n + 1	k = 4n + 2	k = 4n + 3
$\cos(2\pi kT_s/4)$	1	0	-1	0
$\sin(2\pi kT_s/4)$	0	1	0	-1

As can be seen from table 8.1 the multiplication can be easily realized in software (x 1, x 0, x - 1, x 0, etc). In the software using the integrate and dump filter, the multiplication and filtering has been combined using add, subtract, and divide instructions.

$$I = \frac{S(0) - S(2) + S(4) - S(6) \;....\; + S(N-3) - S(N-1)}{N/2}$$

$$Q = \frac{S(1) - S(3) + S(5) - S(7) \;....\; + S(N-2) - S(N)}{N/2} \qquad (9.1)$$

S(..) is the sample taken, and N is the amount of samples used for the averaging operation. By selecting N a power of 2, the division can easily be realized in software. If N is 2^x, division is realized by x time right shifting. Table 8.2 shows the total amount of samples necessary for the averaging for each IF and the bandwidth (this is not the 3 dB bandwidth but the first zero crossing of the filter). Rounding N results in a smaller bandwidth for an IF of 100 kHz, and a wider bandwidth for an IF of 125 kHz.

Table 8.2: Total amount of samples N for different bandwidth and IF.

Filter bandwidth (Hz)	$N = f_s/B_f$		N after rounding to a power of 2
	f_0 = 100 kHz	f_0 = 125 kHz	
16	510	512	512
8	1020	1025	1024
4	2040	2049	2048
2	4080	4098	4096
1	8160	8196	8192
0.5	16320	16392	16384
0.25	32640	32784	32768

For example for a bandwidth of 0.5 Hz, averaging should take place over a period of 2 seconds. N is chosen to be 16384 (2^{14}). If every 2 seconds the filtered amplitude is passed to the output, aliasing will occur, the decimation factor is too high. For this reason it is necessary to send the filtered signal at least 1 time a second to the output. This problem is tackled by using two blocks of 8192 samples for the filtering.

Fig. 8.1 shows which samples are used for the calculation of one output sample. As can be seen from Fig. 8.1 every block of 8192 samples is used two times (shifting of time window).

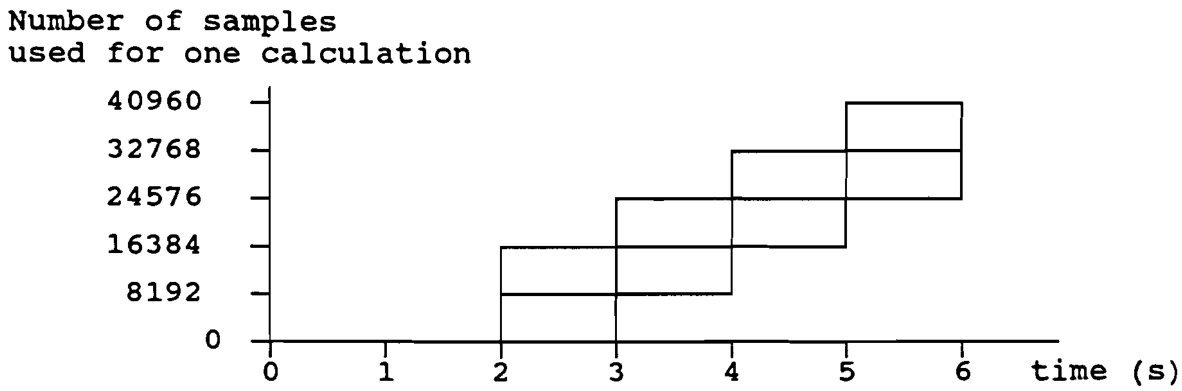


Fig. 8.1: Shift of time window to avoid aliasing,
filter bandwidth = 0.5 Hz.

The FIR filter in the program DSPFIR is much more complicated. This is described in [10].

8.2 Program structure

The programs consists basicly of the following parts

A Installation

B Main program

C Subroutines for log, cos

D Receive interrupt handler

E Tables for Bandwidth, log, cos

The sections A, B, and D are described in the following.

A Installation

Prior to the execution of the main program, it is necessary to initialize the processor. Generally, initialization takes place anytime the processor is reset.

Instructions are executed to set up operational modes, memory pointers, interrupts, and the remaining functions necessary to meet system requirements. In TMSROM the dip switches are read to set the filter bandwidth, according to table 8.3. Only 3 of the 8 switches are used in this program. In DSPFIR the dip-switches are currently not used.

Table 8.3: Function of dip switches (only for TMSROM).

filter bandwidth (Hz)	7 .. 0
16	xxxxx000
8	xxxxx001
4	xxxxx010
2	xxxxx011
1	xxxxx100
0.5	xxxxx101
0.25	xxxxx110
0.25	xxxxx111

B Main program

In this part the incoming samples are filtered and the amplitude and phase is calculated and send to the D/A converters. The flow diagram of the main program is shown in Fig. 8.2.

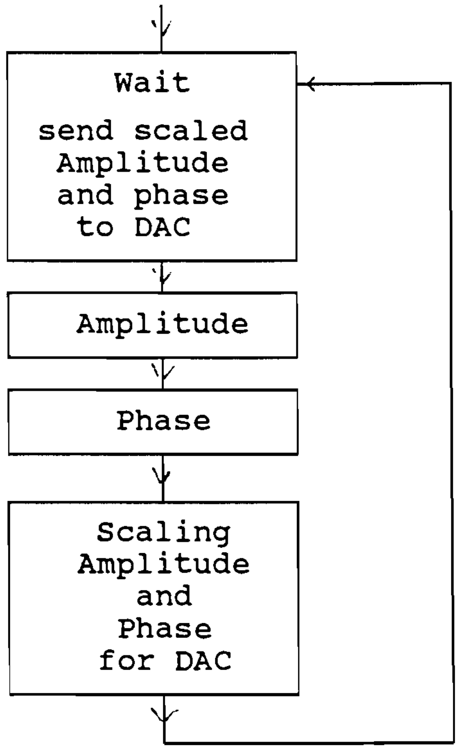


Fig. 8.2: Flow diagram main program.

Wait routine

This is an active waiting loop. The receive interrupt handler places the taken samples in the filter. In TMSROM this is an integrate and dump filter, in DSPFIR it is a FIR filter. The program leaves this routine when enough samples are collected to calculate the amplitude and phase. After the calculation of the amplitude and phase, the program returns to this routine. During the calculation of the amplitude and the phase the reading of the samples, whenever a hardware interrupt occurs, continues. This is performed by the receive interrupt handler.

At the end of this routine the scaled amplitude and phase (which are calculated in the scaling routine) are sent to the D/A converters (DAC). This is done to assure the data is sent regularly with the same time intervals (synchronized with the clock). If the data is sent immediately when the amplitude and phase are calculated the time intervals are not always the same, because the calculation time depends on the amplitude and the phase of the incoming signal (use of tables).

Amplitude routine

This routine calculates $A^2 = I^2 + Q^2$. After this the 10log of A^2 is calculated to get 20logA. A subroutine is applied for the calculation of the logarithm.

Phase routine

This routine calculates the phase of the incoming signal. The phase ϕ is the angle between the I-Q vector and the I axis.

Scaling routine

This routine scales the calculated amplitude and phase signals to an appropriate signal for the D/A converters. Table 8.4 shows the input code to output voltage relationship of the applied D/A converter AD7840. Input coding to the D/A converter is two's complement with 1 LSB = 366μV.

Table 8.4: input/output code table of D/A converter AD7840, assuming REF IN = +3 V.

DAC Latch contents (MSB ... LSB)	Analog output V_{out}(V)
0 1 1 1 1 1 1 1 1 1 1 1 1 1	+ 2.999634
0 1 1 1 1 1 1 1 1 1 1 1 1 0	+ 2.999268
0 0 0 0 0 0 0 0 0 0 0 0 0 1	+ 0.000366
0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 0.000366
1 0 0 0 0 0 0 0 0 0 0 0 0 1	- 2.999634

The output voltage can be expressed in terms of the input code N, using the following expression

$$V_{out} = \frac{2.N.REFIN}{16384} \quad - 8192 \le N \le +8191 \qquad (9.2)$$

Amplitude

The scaling routine for the D/A converter realizes an output range of approximately 55 dB. The input signal range is from about +18 dBm to -37 dBm (input A/D converter shunted with 50 ohm resistor) resulting in an output range of -3 V to +3 V. If wanted, the output range can be altered by changing the scaling routine. The minimum level for which the output signal is -3 V can be shifted, in the current program this level is at -37 dBm.

Phase

The number from the phase routine is in the range of 0 to 3600 (0 to 360 degrees). The scaling routine converts this signal to an output range of the D/A converter of -1 V to +2.6 V.

D Receive interrupt handler

The program makes use of a hardware interrupt for reading the samples and places the samples in the filter (integrate and dump or FIR filter). The samples are 12-bit two's complement binary numbers. To make a higher resolution possible than the 12 bits of the A/D converter (enhancement of A/D resolution, see section 6.3), the 12-bit two's complement number is transformed to a 16-bit two's complement number in the receive interrupt handler. The most negative and positive numbers are then respectively $2^{15} - 1 = 32767$, and $-2^{15} = -32768$.

9 Interfacing digital detector to PLL receiver

The main subject of this chapter is the interfacing of the available digital detectors to the EUT PLL receiver, whereas the conventional PLL receiver remains unmodified. In a previous research [4] this interfacing problem has already been examined theoretically. In this report is described the actual interfacing, which is not completely according to the recommendations of the former study. The PLL receiver consists of two parts: one part for receiving a copolar signal; the other part for receiving a crosspolar signal. These parts are called copolar and crosspolar receiver respectively. Because the Intelsat-V beacon receiver employs a copolar receiver only, the interfacing to the crosspolar receiver has not been performed.

9.1 Block diagram digital detector interfaced to PLL receiver

- Copolar receiver

The digital detectors (from DNL and EUT) can be interfaced to the copolar receiver as shown in Fig. 9.1 (for details see appendix A). The digital detectors operate at an IF of 125 kHz. An external 125 kHz filter/amplifier is required to prevent aliasing, and to convert the signal from the receiver to the optimum range for the A/D converter of the detector. The sampling frequency is extracted from the 125 kHz reference oscillator of the PLL receiver, and not, as has been suggested in the former study [4], from the input carrier frequency.

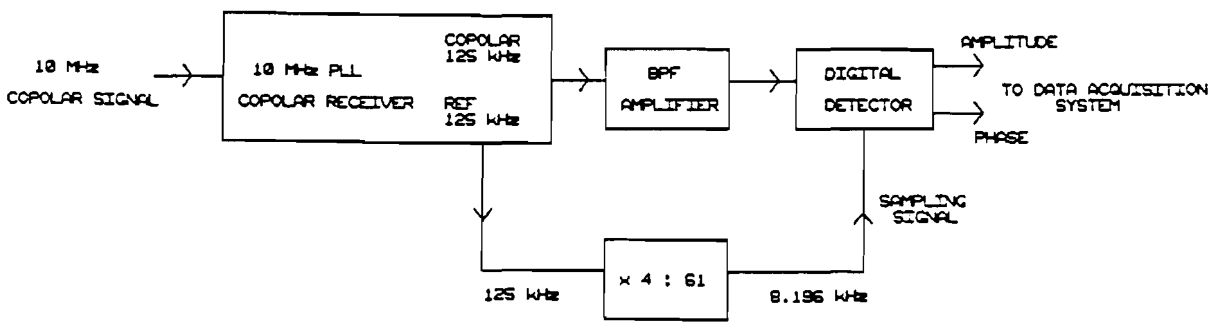


Fig. 9.1: Block diagram digital detector interfaced to the copolar receiver.

- Crosspolar receiver

For crosspolar measurements the digital detector can be interfaced to the crosspolar receiver in the same manner as to the copolar receiver (for details see appendix A). A similar 125 kHz filter/amplifier as used for the copolar receiver can be employed. The sampling signal is the same as used in the copolar receiver.

9.2 Anti-aliasing IF filter and amplifier

The schematic diagram of the anti-aliasing IF filter and amplifier is shown in Fig. 9.2. The center frequency of the filter must be tuned at 125 kHz with tuning capacitors C1 and C2. The bandwidth B_n of the filter is about 2 kHz ($B_n < f_s/2 =$ 4 kHz). The gain of the amplifier can be adjusted with P1. A limiter is included to limit the output signal to a range of approximately -8 V to +8 V. This limiter is included to prevent the A/D converter of the digital detector to be damaged.

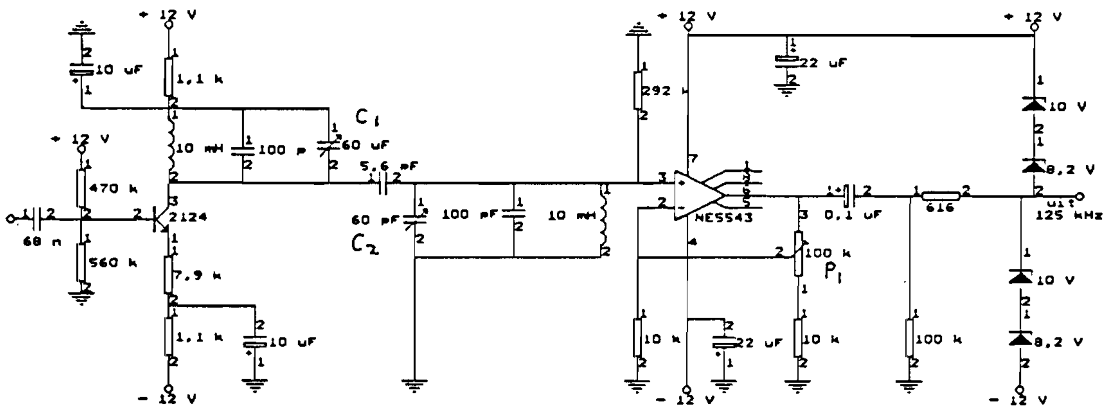


Fig. 9.2: Anti-aliasing IF filter and amplifier.

9.3 Circuit for extracting the sampling frequency

The circuit which extracts the sampling frequency is currently implemented in the PTT IF receiver system for the Olympus project at EUT as Unit 400 [16]. The block diagram of the original design is shown in Fig. 9.3. This circuit is meant to extract 8.163 kHz from a 100 kHz reference signal.

$f_s = 4f_0/(2n + 1)$, $f_0 = 100$ kHz, $n = 24$, $f_s = 8.163$ kHz.

The circuit operates as follows. A phase-locked-loop (PLL) is used to multiply the frequency of the 100 kHz input signal by a factor 8 (Fig. 9.3). Then a digital divider divides this frequency by 98 (49 x 2). Thus the frequency of the output signal is the input frequency times 4 divided by 49.

In the PLL receiver a reference signal of 125 kHz is employed. In the report of schaffels and Vaessen [4] is suggested to replace in Unit 400 the 4 MHz crystal by a 5 MHz crystal to enhance the sampling frequency by 25 % to 10.20 kHz. However, tests with the digital detector using the Z80 microprocessor showed that overflow occurs due to the higher sampling frequency. This problem can been solved by increasing the 4 MHz clock frequency of the Z80 to 5 MHz [17].

However, a few small modifications of the circuit of Unit 400, changes the sampling frequency to 8.196 kHz (f_0 = 125 kHz, n = 30, f_s = 8.196 KHz) and no overflow occurs in the digital detectors using the Z80 with a 4 MHz clock. The block diagram of the modified circuit is shown in Fig. 9.4. The complete circuit diagram of the original circuit Unit 400, and the modified version for the 125 kHz reference signal, are shown in appendix A.

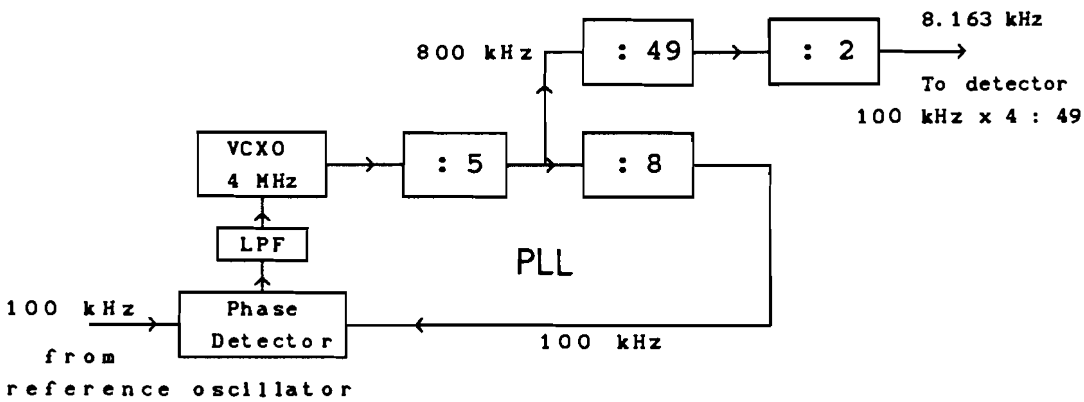


Fig. 9.3: Block diagram of Unit 400 for extracting sampling frequency out of a 100 kHz reference signal.

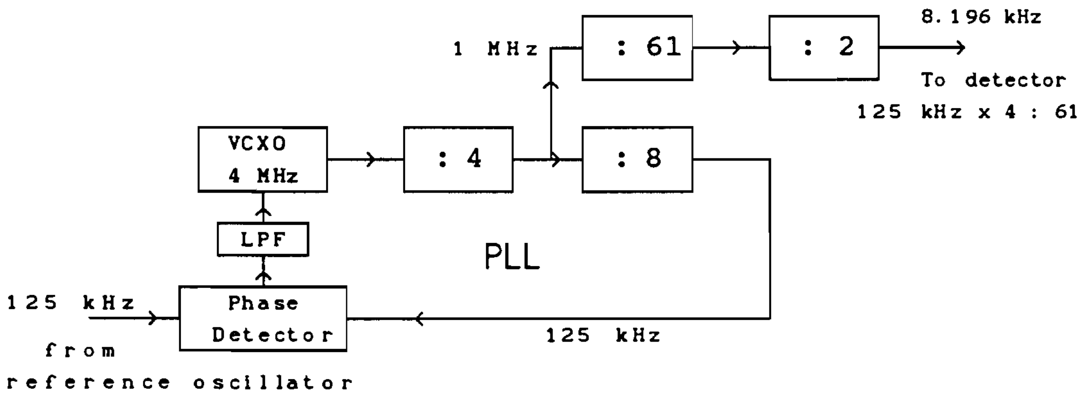


Fig. 9.4: Block diagram of modified circuit for extracting sampling frequency out of a 125 kHz reference signal.

When more PLL receivers with digital detection are used it is possible to use one circuit for extracting the sampling frequency for all the detectors. However, all the receivers should use the same external 1 MHz reference oscillator (see Fig. 3.1). The sampling frequency can then be extracted from any one of the receivers, since all have the same 125 kHz reference signal (the 125 kHz reference signal is derived from a 1 MHz crystal oscillator, internal or external, see schematic diagram in appendix A). If the sampling frequency is extracted from one receiver and no external reference oscillator is employed, large measurement errors will occur in the detectors of the other receivers (see section 6.5).

10 Measurements

10.1 Utilized processor capacity

For future developments in software and hardware of the EUT digital detector it is important to know how much of the processor capacity is needed with the currently implemented software. It is difficult to calculate the utilized processor capacity from the program. It is much easier to measure it.

The following method has been employed to determine the utilized processor capacity. During the time the processor is not performing a calculation the program is in the waiting loop to collect samples (see chapter 8). To determine the utilized capacity, an OUT statement has been added in the waiting loop. Each time the program runs through this waiting loop, output port 3 of the address decoder 74138 will be low for a short moment. When the processor is performing a calculation this output port will remain high. When no sampling signal is applied to the A/D converter the program remains in the waiting loop and at the output port of the address decoder appears a sequence of short pulses. The utilized capacity is found by measuring the frequency of the output signal of the address decoder with and without a sampling signal applied to the A/D converter. The utilized capacity is given by:

$$\text{utilized capacity} = (1 - f_1/f_2) \times 100\ \% \qquad (10.1)$$

where

f_1 frequency with sampling frequency applied

f_2 frequency without sampling frequency applied

This test has been performed with the two versions of the modified EUT detector.

- Modified EUT detector 1

Clock frequency 8 MHz
Program: modified version of TMSROM
f_1 = 227 kHz, f_2 = 285 kHz
Utilized capacity is approximately 20 %
If a clock frequency of 20 MHz is applied,
the utilized capacity is about 10 %

- Modified EUT detector 2

Clock frequency 20 MHz
Program: modified version of DSPFIR
f_1 = 410 kHz, f_2 = 715 kHz
Utilized capacity is approximately 42 %

10.2 Amplitude measurements with Modified EUT detector

Amplitude measurements have been performed with the two versions of the modified EUT detector. All amplitude measurement results given here, are performed with the modified EUT detector using the FIR filter. Both versions have the same amplitude characteristics. It has not been possible to measure the filter or phase characteristics of the detectors because at ITS the necessary equipment is not available.

The measurement setup is shown in Fig. 10.1. The amplitude measurement results of the modified EUT detector are shown in Fig. 10.2 (appendix G).

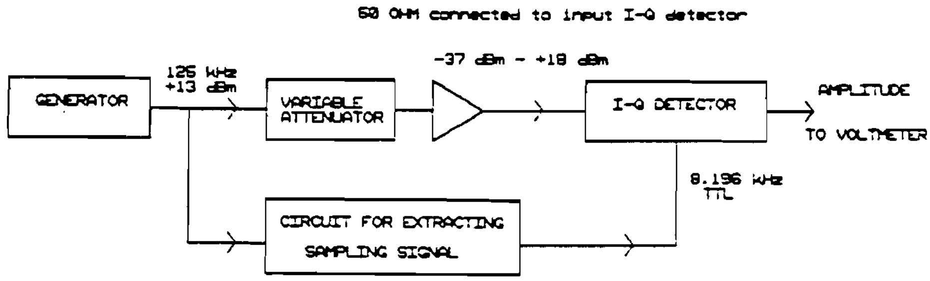


Fig. 10.1: measurement setup for amplitude measurements with modified EUT detector.

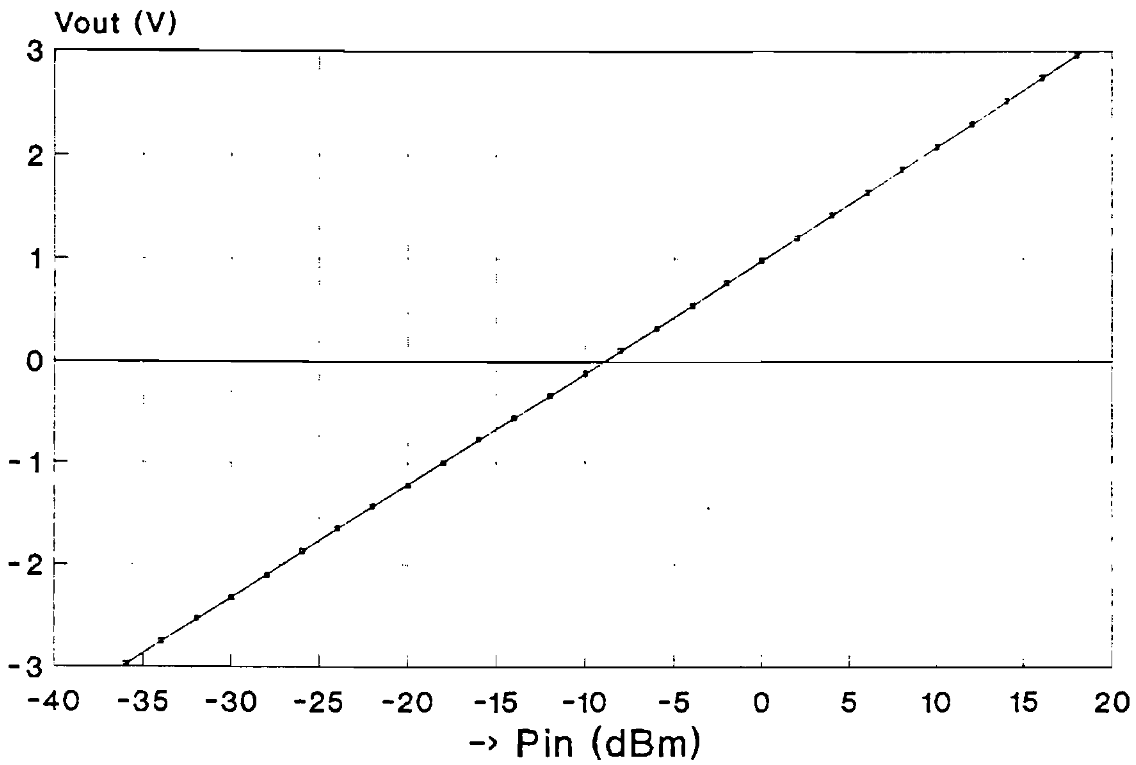


Fig. 10.2: Amplitude measurements with modified EUT detector.

Maximal non-linearity of the modified EUT detector is 0.1 dB over a range of 55 dB.

10.3 Amplitude measurements with PLL receiver using analog detection

Amplitude measurements have been performed with the EUT PLL receiver using analog detection. Before the measurements have been performed, the PLL receiver has been tuned (for tuning procedure see [18]).

The receiver has a linear and a logarithmic output port, a logarithmic converter is used for the log conversion. The measurements have been performed using a 10 dB attenuator in front of the receiver in order to realize a better match for the generator to the input of the receiver (input of receiver directly connected to mixer, see appendix A). The amplitude measurement results are shown in Fig. 10.3 and 10.4 (appendix G).

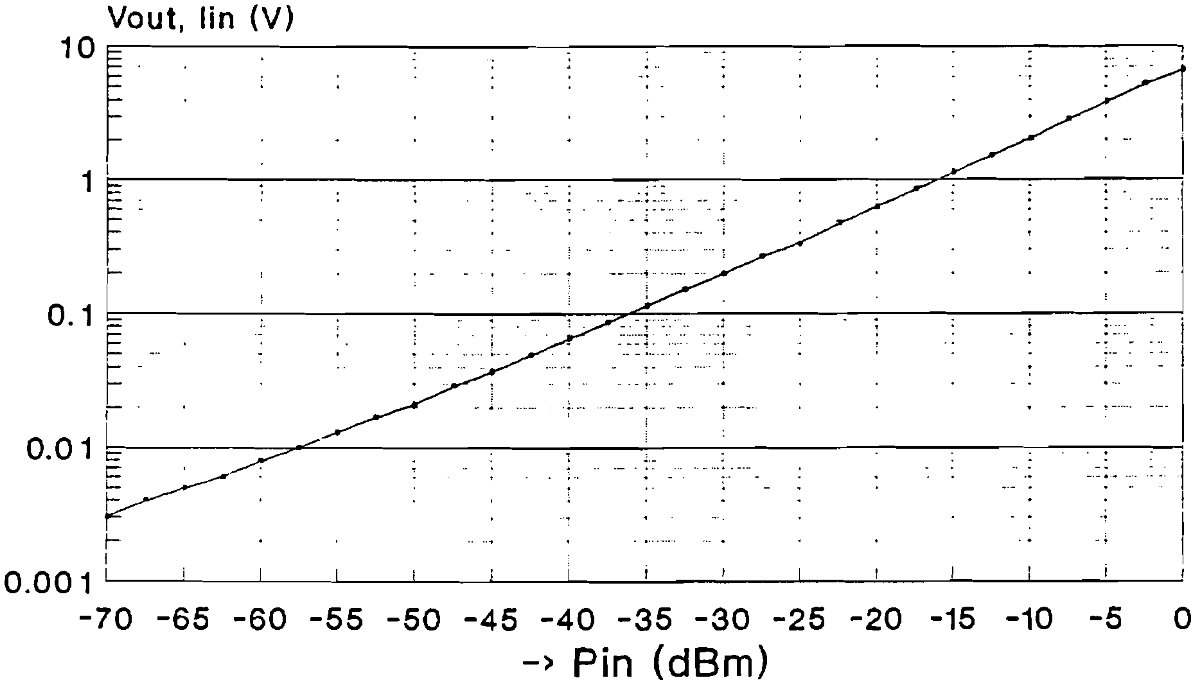


Fig. 10.3: Amplitude measurements with PLL receiver using analog detection, measured at linear output port.

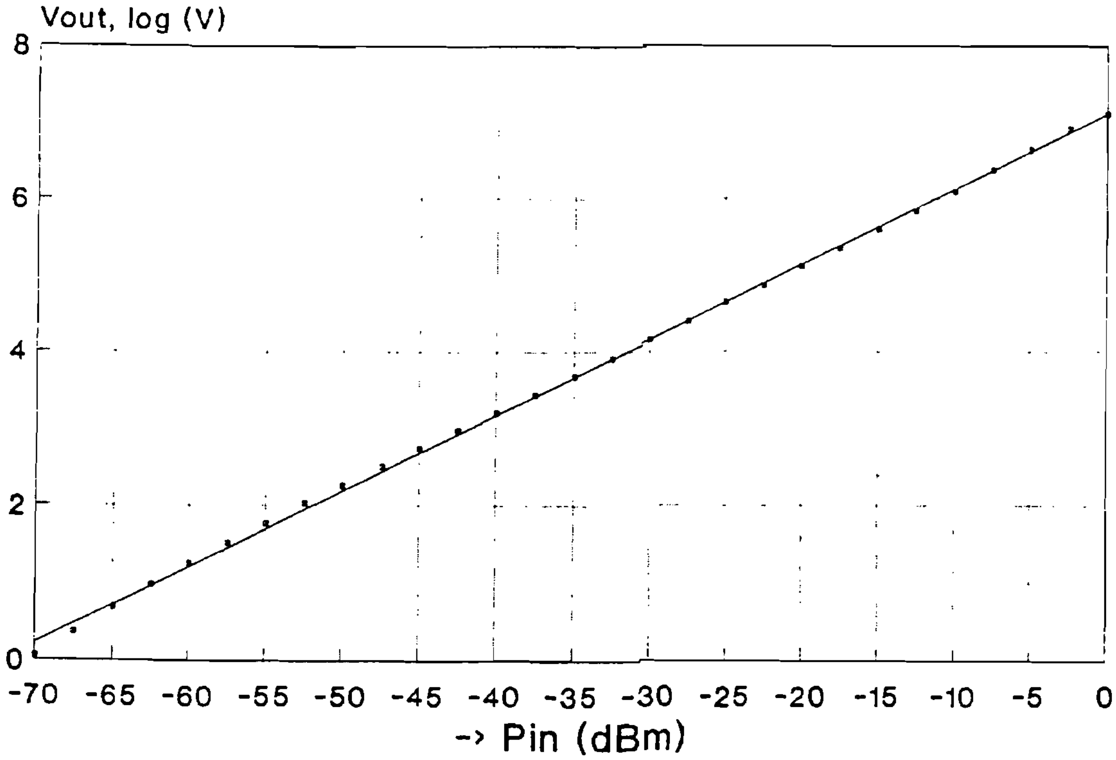


Fig. 10.4: Amplitude measurements with PLL receiver using analog detection, measured at logarithmic output port.

As can be concluded from Fig. 10.3 and 10.4, the transfer function of the system is not quite linear over the full input range. For signals higher than about -15 dBm the system is not linear. This is due to the input mixer (see circuit diagram in appendix A), above a certain input power level, compression occurs. IF the input signal is too small (< -65 dBm) also non-linearity occurs. Furthermore low level measurements are extremely sensitive for temperature drift (signals < -50 dBm).

10.4 Amplitude measurements with PLL receiver using a modified EUT detector

The modified EUT detector has been tested in combination with the PLL receiver. The measurement setup is shown in Fig. 10.5. The 125 kHz amplifier/filter has been adjusted in order to get an input range for the system using digital detection of approximately -10 to -65 dBm. Within this range the system approximates linearity best. The results are shown in Fig. 10.6 (appendix G).

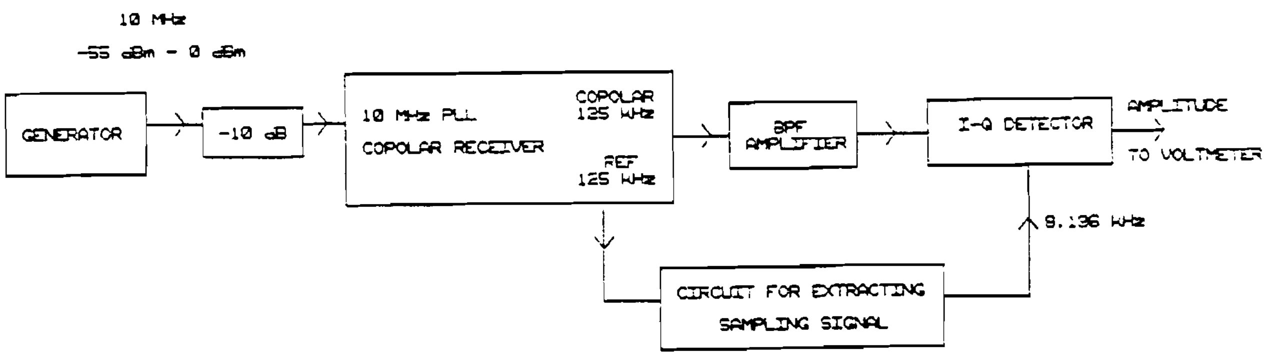


Fig. 10.5: Setup for amplitude measurements with a PLL receiver using a modified EUT detector.

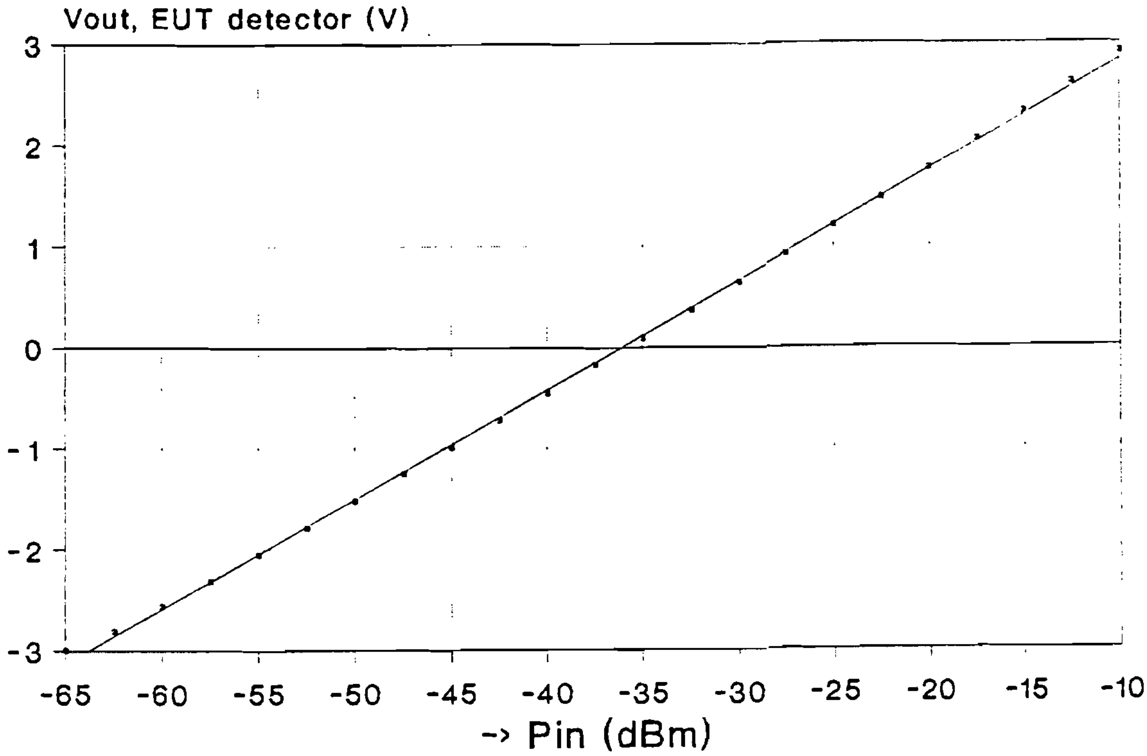


Fig. 10.6: Amplitude measurement with PLL receiver using modified EUT detector.

For the PLL receiver with modified EUT detector is found:
Input range -10 dBm to -58 dBm non-linearity ≤ 0.2 dB.
< -58 dBm nonlinearity ≤ 0.5 dB.

Signals smaller than about -58 dBm can not be measured linear. This is a result of not perfect isolation of the 125 kHz reference signal. This signal is added to the 125 kHz signal, resulting in a non-linear characteristic in the lower range of the receiver. Several points in the receiver have been tested to find the best point to interface the digital detector to the PLL receiver (see appendix A).

10.5 PLL receiver using modified EUT detector installed in Intelsat measurement system

The PLL receiver using the modified EUT detector has been installed in the Intelsat-V beacon receiver system at ITS. Measurements have been performed during clear sky. High attenuation events have been simulated by an attenuator in the front-end of the receiver. As a result a low signal to noise ratio (S/N) is obtained at the input of the PLL receiver and the receiver almost looses lock (threshold point, 25 dB attenuation). The conclusions of these measurements are stated below.

- The EUT detector using the FIR filter shows practically the same measurement results as the EUT detector with the integrate-and-dump filter (detection bandwidth about 0.3 Hz).
- The digital detection system has a smaller detection bandwidth (0.3 Hz) than the analog detection circuit (1 Hz), which improves the signal-to-noise ratio of detected signal.
- The digital I-Q detection system shows the same amplitude measurement errors as the analog coherent detection circuit for a low S/N ratio at the input of the PLL receiver. This is in accordance with the statement in section 3.3: I-Q detection is in essence similar to coherent detection.
- Contrary to theoretical considerations in section 3.2.2 the measured amplitude in the presence of noise appears to be an underestimation of the actual amplitude instead of an overestimation. In the lower input range of the PLL receiver little non-linearity occurs. If the attenuation is 25 dB (threshold point) the deviation is approximately -0.2 dB (noise bandwidth PLL = 100 Hz). Wider noise bandwidths result in more conspicuous deviations. To clarify this discrepancy further investigations are required.

11 Conclusions and recommendations

11.1 Conclusions

The software and hardware of the newly developed EUT detector have been modified to make it suitable for the Intelsat-V beacon receiver system. Two versions have been developed. One version using a readily available program with an integrate-and-dump filter. Another version has been developed using a program with a FIR filter. The superior FIR filter program became available halfway this project. The two developed detectors are interchangeable with the DNL detector so they can also be applied in the ground station for the Olympus satellite.

Both detectors have been interfaced to the PLL receiver and tested in the Intelsat system. Measurements have verified the performance.

Although the version using a FIR filter has superior filter characteristics, the actual measurements show practically no difference between the two detectors.

The digital detection system has a smaller detection bandwidth (0.3 Hz) than the analog detection circuit (1 Hz), which improves the signal-to-noise ratio of the detected signal.

11.2 Recommendations

It is possible to develop a detector for amplitude and phase measurements of two input signals. Such a dual-channel detector can be applied in the EUT PLL receiver for measurements of a copolar and a crosspolar signal. The sampling of the two channels can be performed in several ways: a multiplexer in combination with an A/D converter, or two A/D converters.

To enhance the processing capability the clock frequency can be raised to 40 MHz. This requires some hardware modifications.

For a dual-channel detector probably more data memory is needed. For this reason a TMS320C26 DSP can be applied. The TMS320C26 is pin-compatible with the TMS320C25 and contains a larger internal RAM. (TMS320C25 544 words, TMS320C26 1568 words).

Further digitalization of the PLL receiver is recommendable. The phase-locked-loop in the PLL receiver is completely analog. It might be replaced by a digital PLL using a TMS320C25.

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Appendix A: EUT PLL receiver and circuits for interfacing digital detector to PLL receiver

The block diagram of the PLL receiver is shown in Fig. A.1. The point were the 125 kHz filter/amplifier has been connected is marked with an A. At this point an emitter follower has been inserted as an interface between the PLL receiver and the amplifier (high input impedance, low output inpedance).

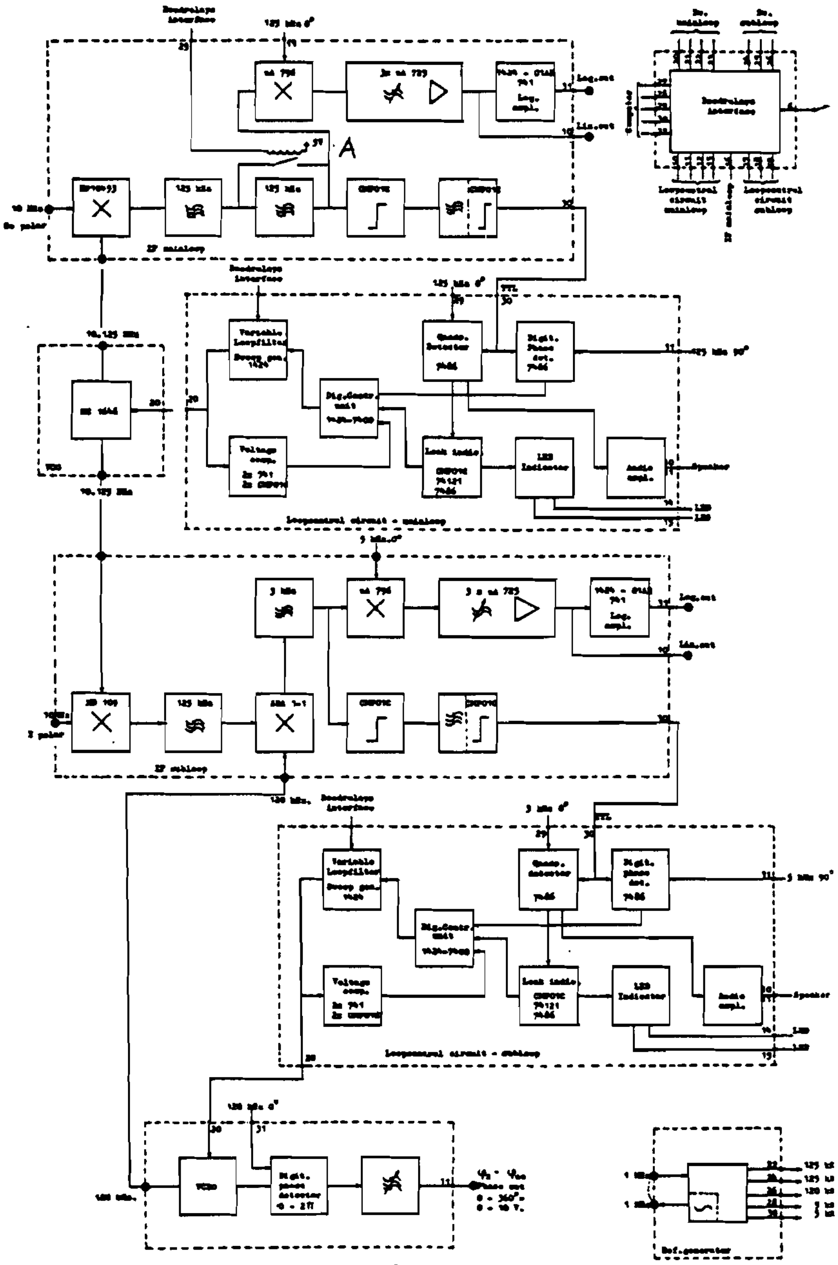
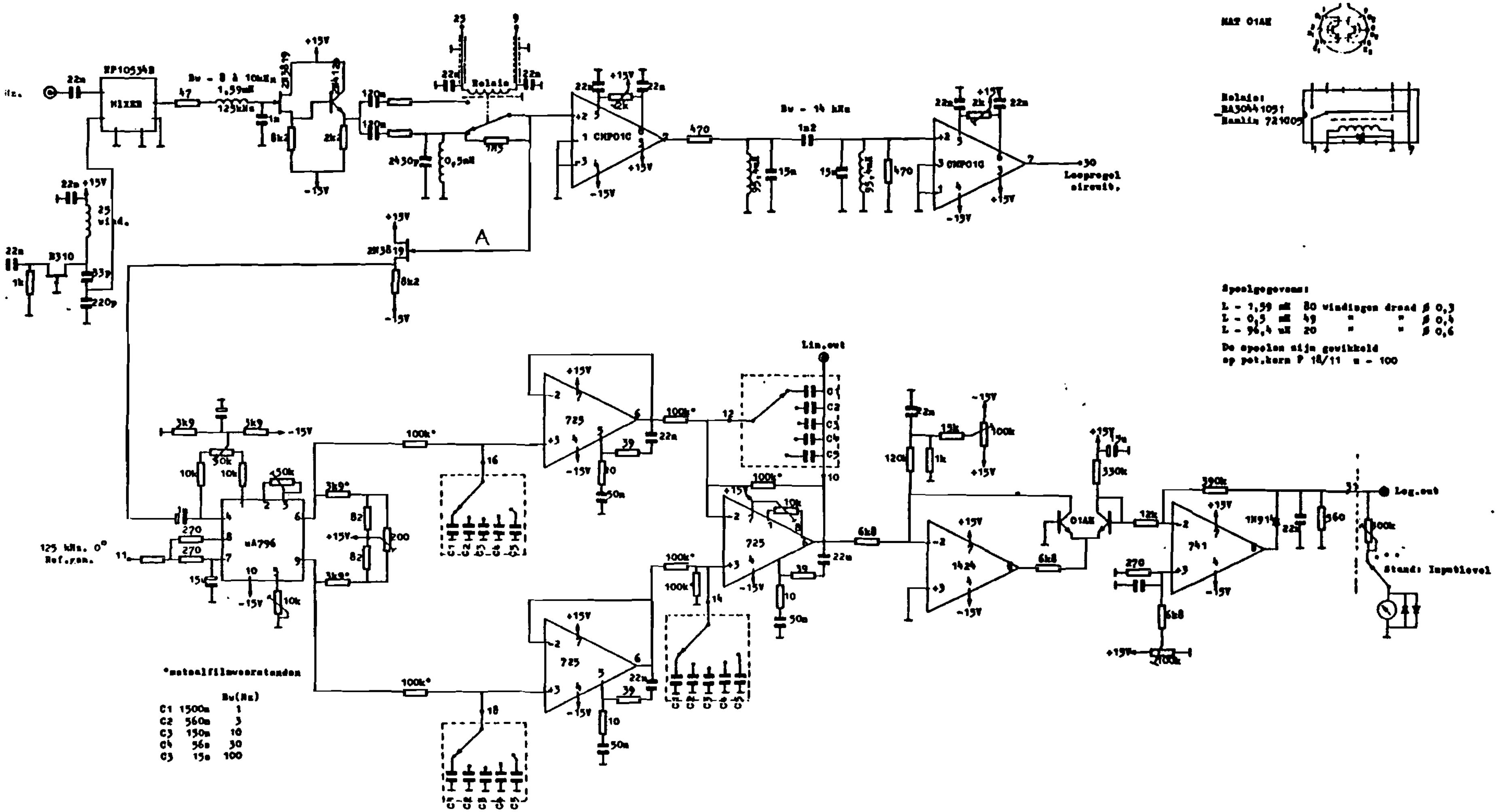
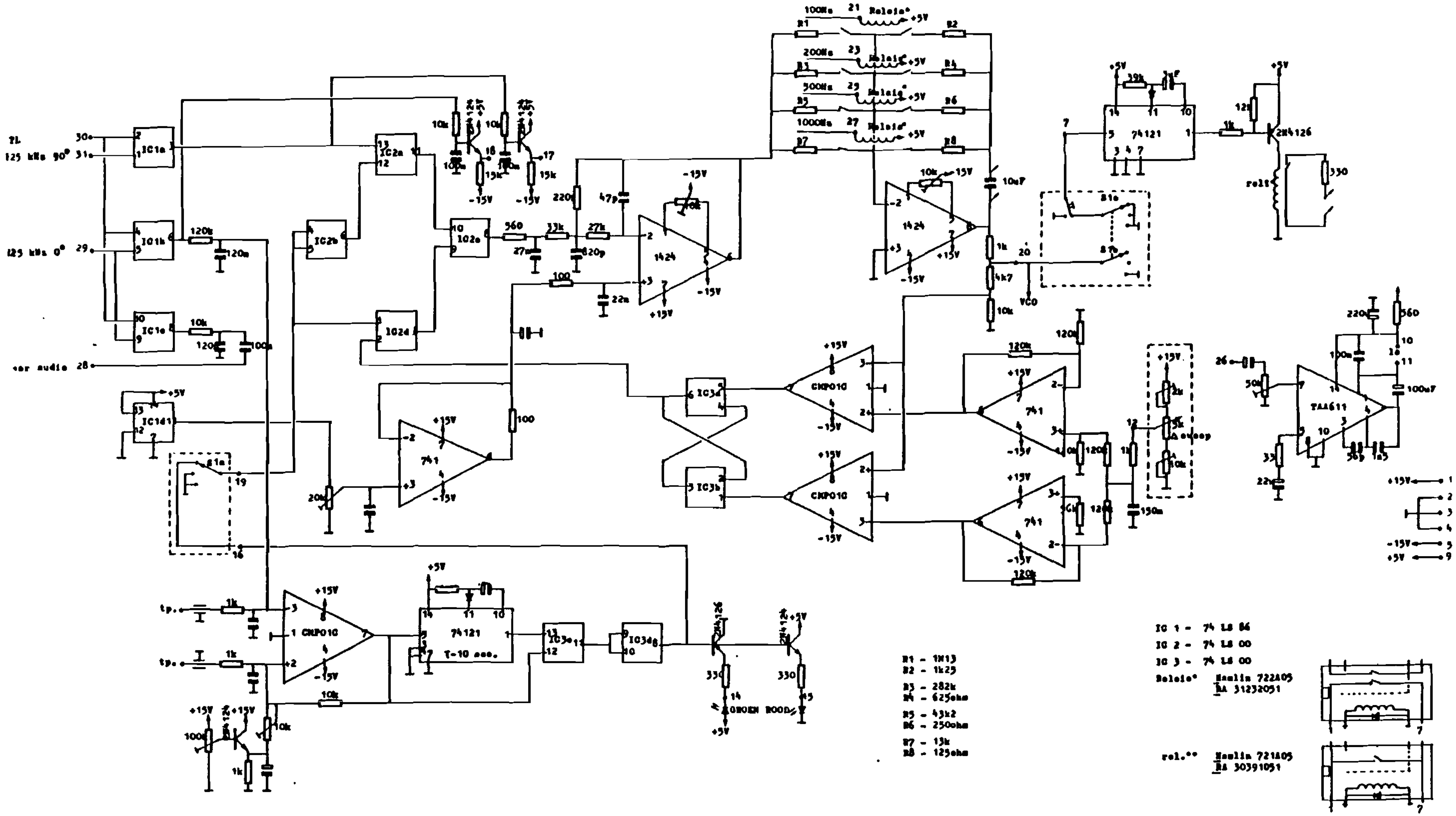


Fig. A.1: Block diagram EUT PLL receiver.

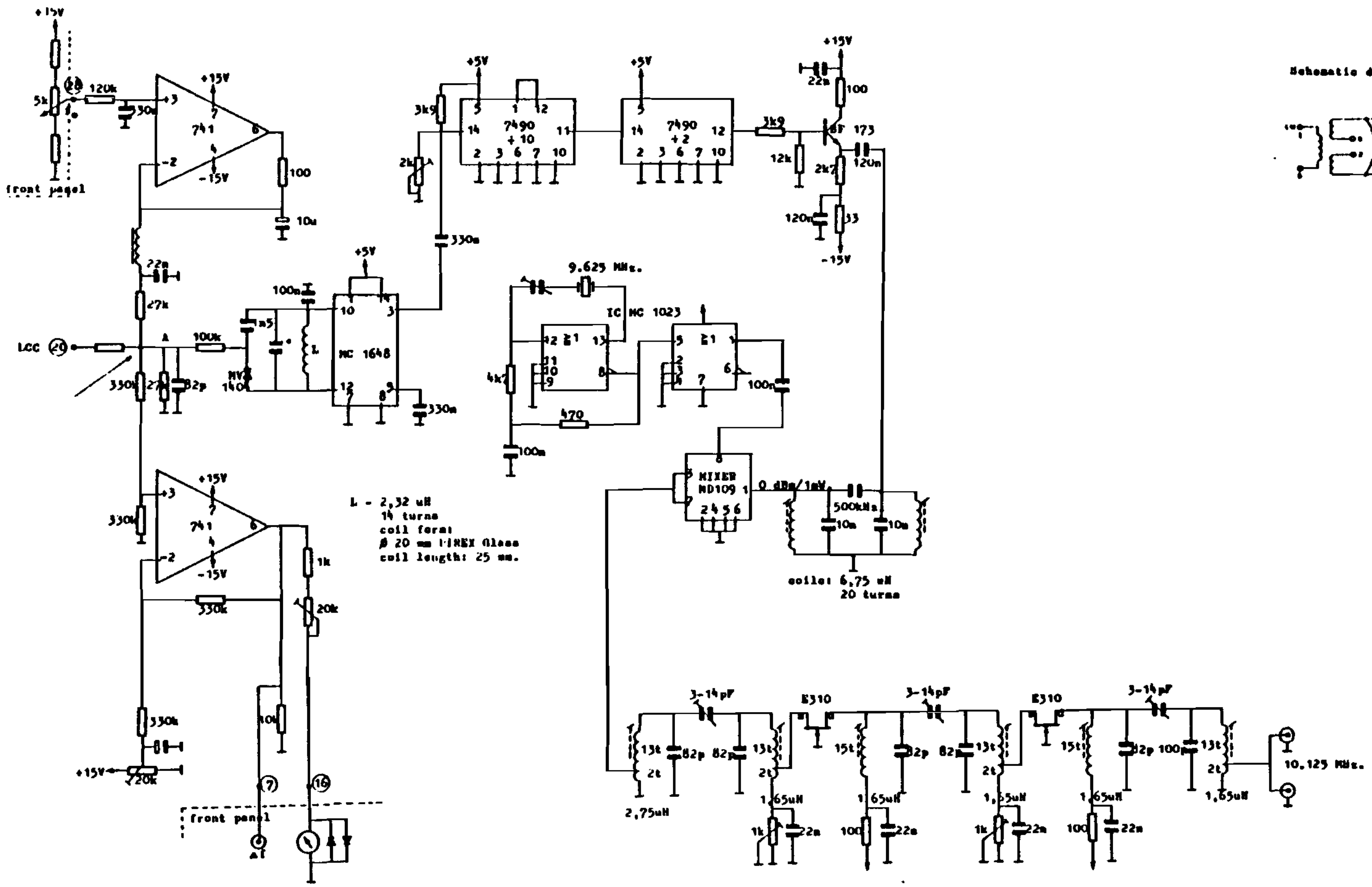


IF mainloop

– A.2 –

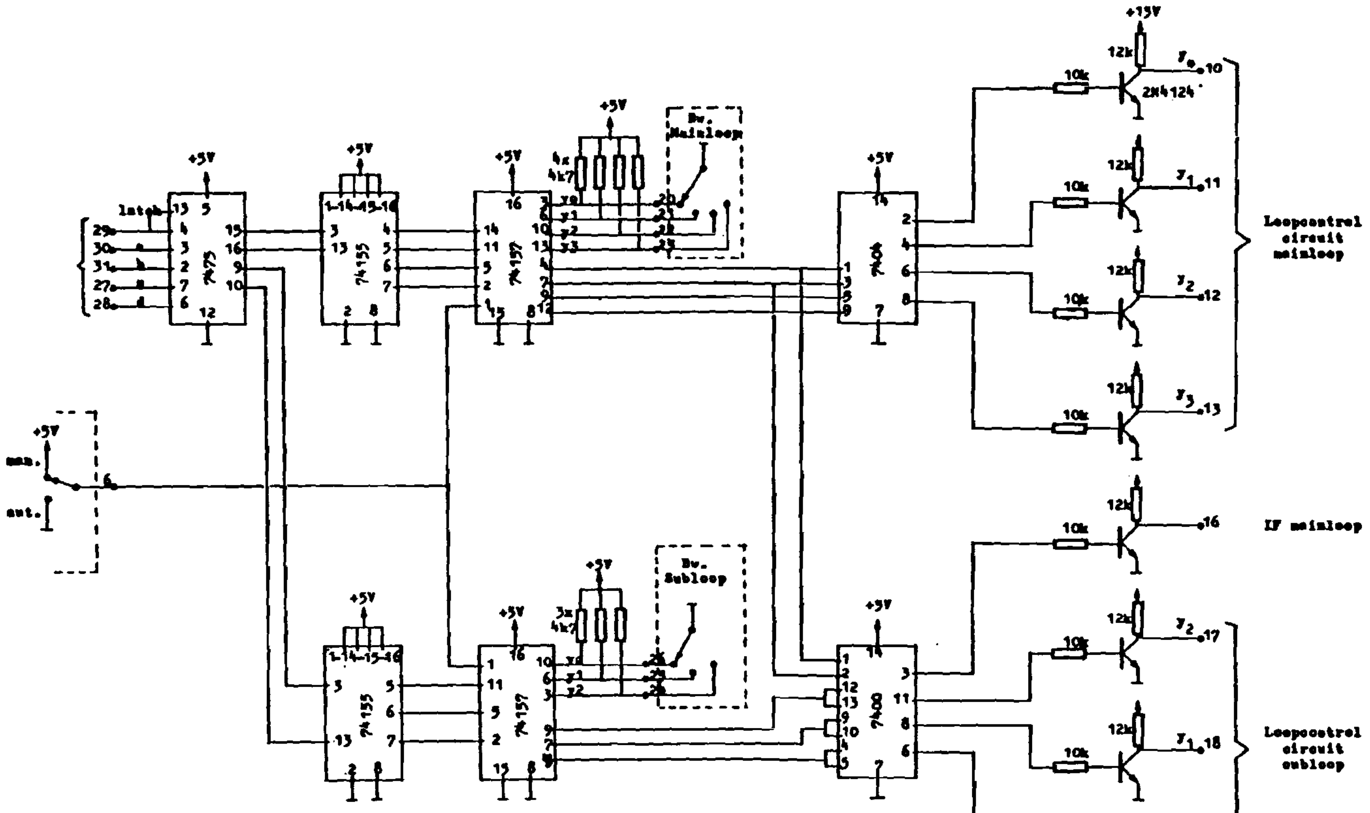


loop control circuit
(mainloop)



Schematic diagram ND 109

voltage controlled oscillator



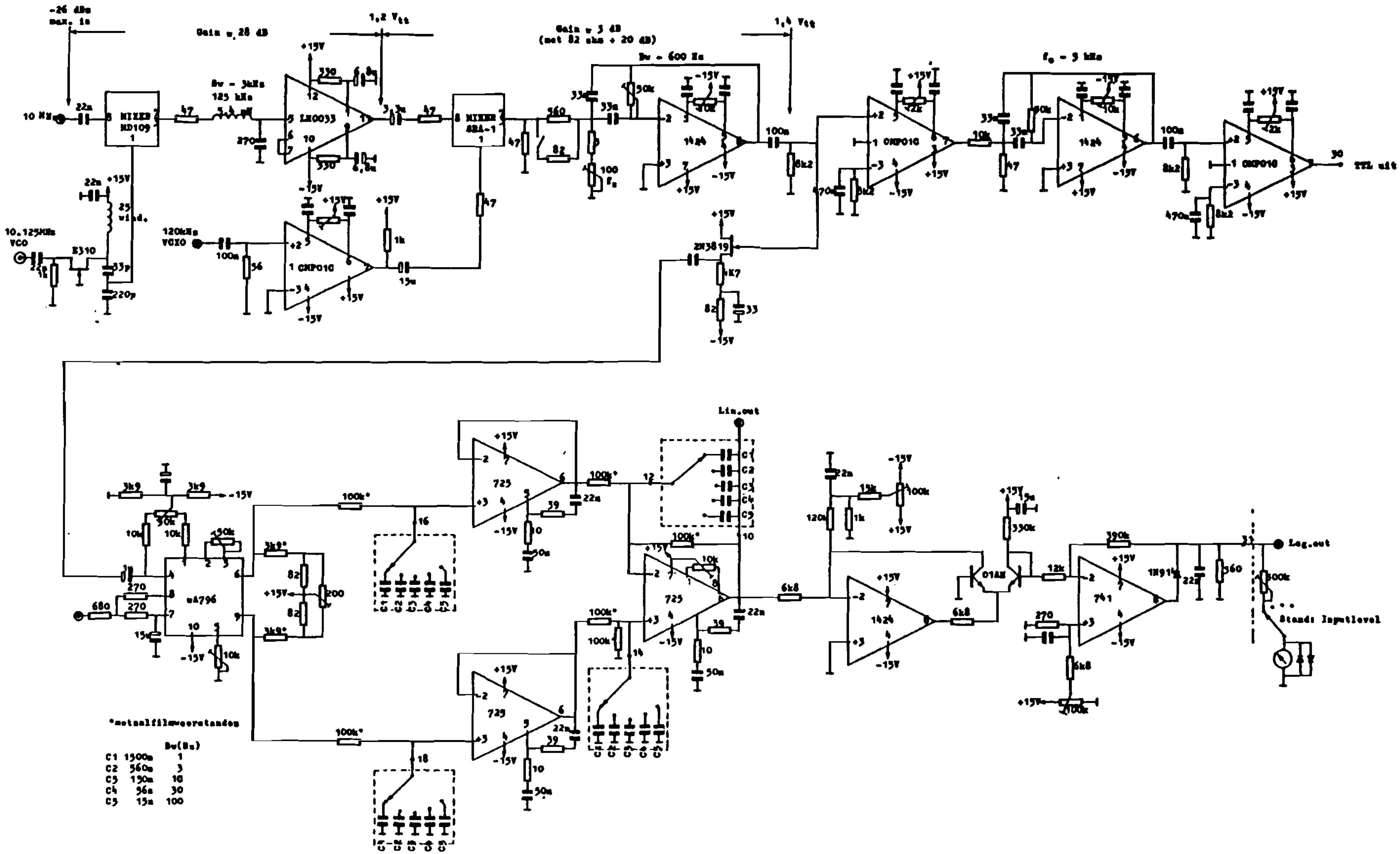
MAINLOOP

a	b	yo	y1	y2	y3	Bw. (Hz)
0	0	0	1	1	1	1000
0	1	1	0	1	1	500
1	0	1	1	0	1	200
1	1	1	1	1	0	100

SUBLOOP

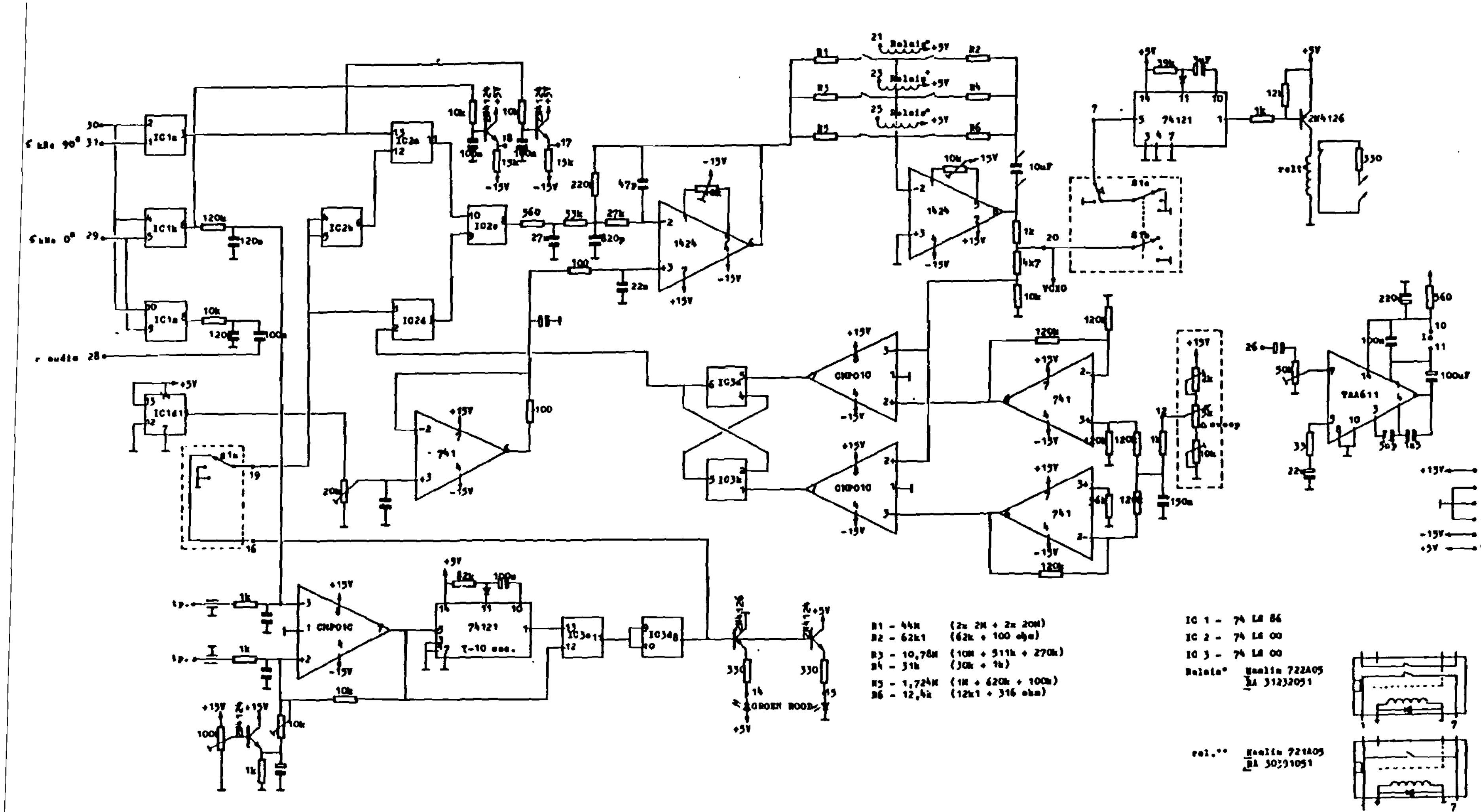
c	d	yo	y1	y2	Bw. (Hz)
0	0	0	1	1	1
0	1	1	0	1	2
1	0	1	1	0	5
1	1	x	x	x	x

reedrelais interface

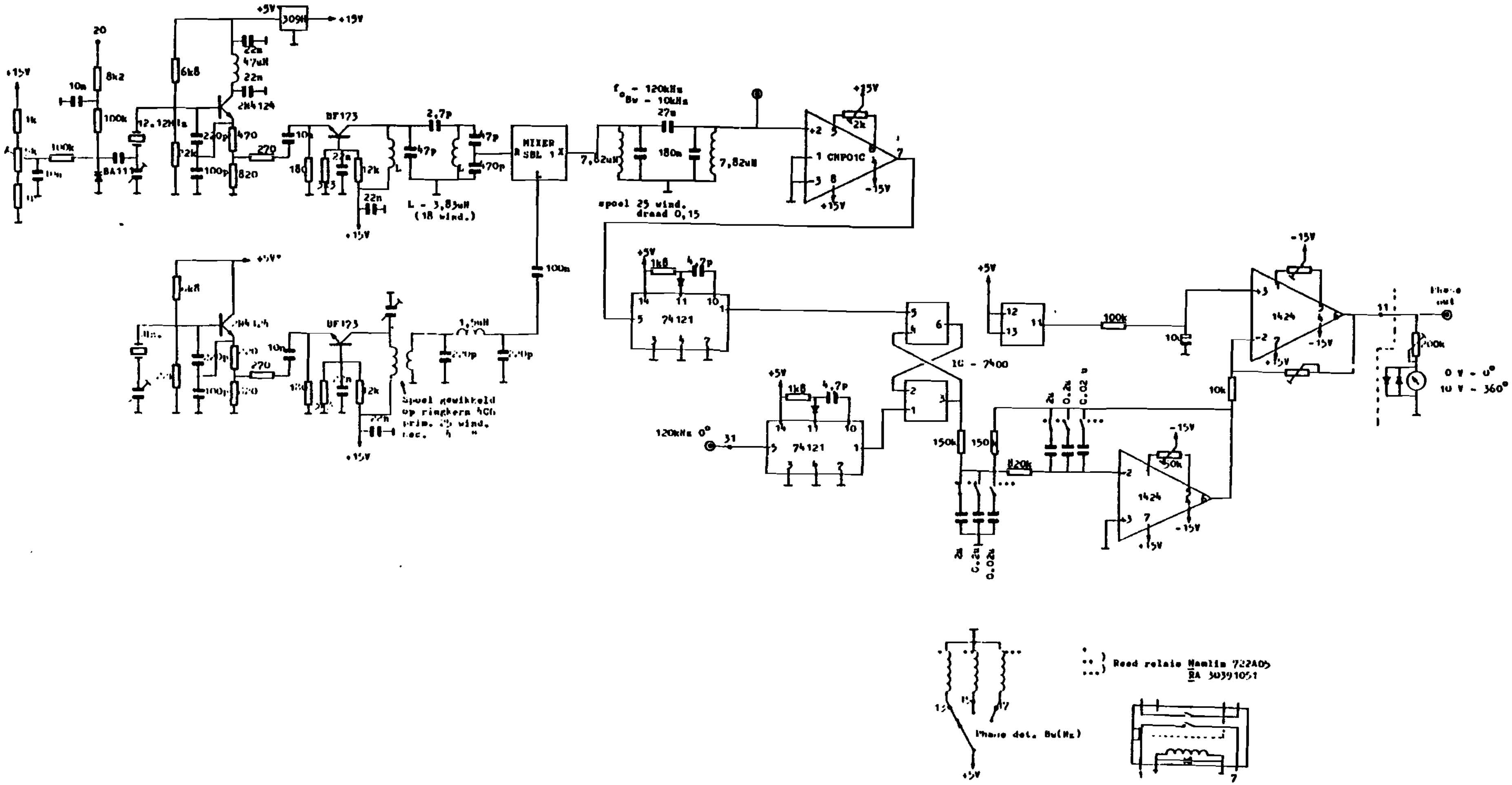


-26 dBm
max. in
Gain ≈ 28 dB
1,2 Vtt
Gain ≈ 3 dB
(met 82 ohm + 20 dB)
Bw = 600 Hz
1,4 Vtt
f0 = 5 kHz
10 MHz
MIXER MD109
LH0033
MIXER SBA-1
10.125MHz VCO
120kHz VCXO
OMP010
TTL uit
Lin.out
Log.out
Stand: Inputlevel
μA796
725
741
*metaalfilmweerstanden
Bw(Hz)
C1 1500n 1
C2 560n 3
C3 150n 10
C4 56n 30
C5 15n 100

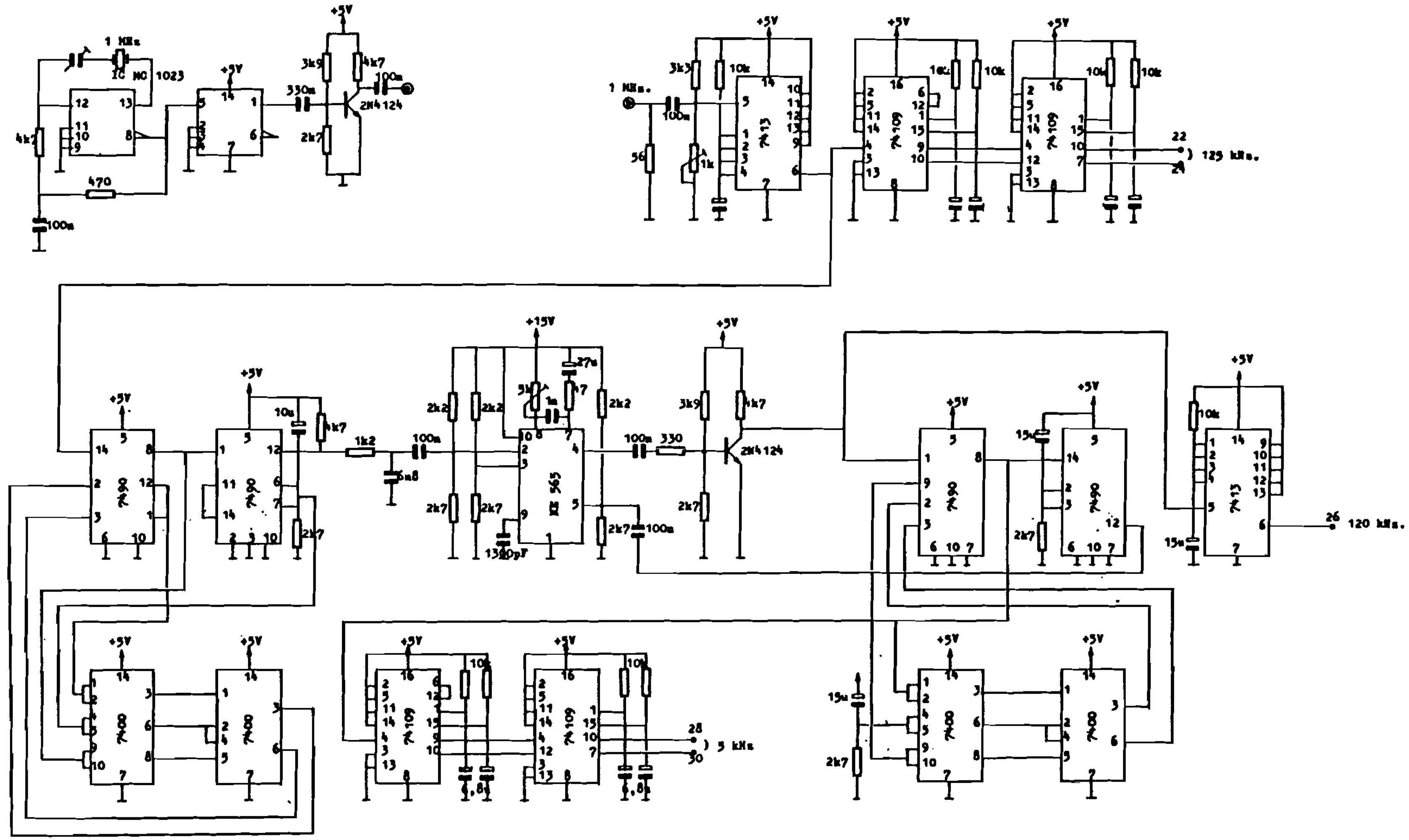
IF subloop



loop control circuit
(subloop)



voltage controlled X-tal oscillator



reference generator

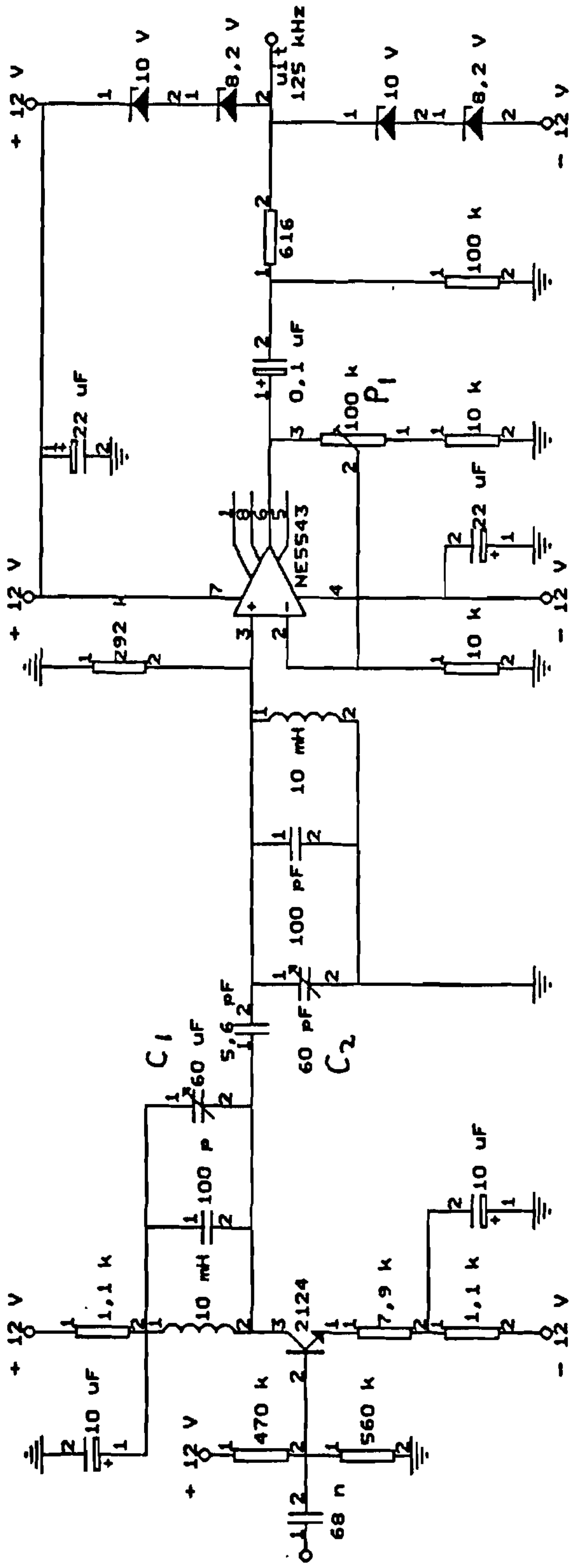
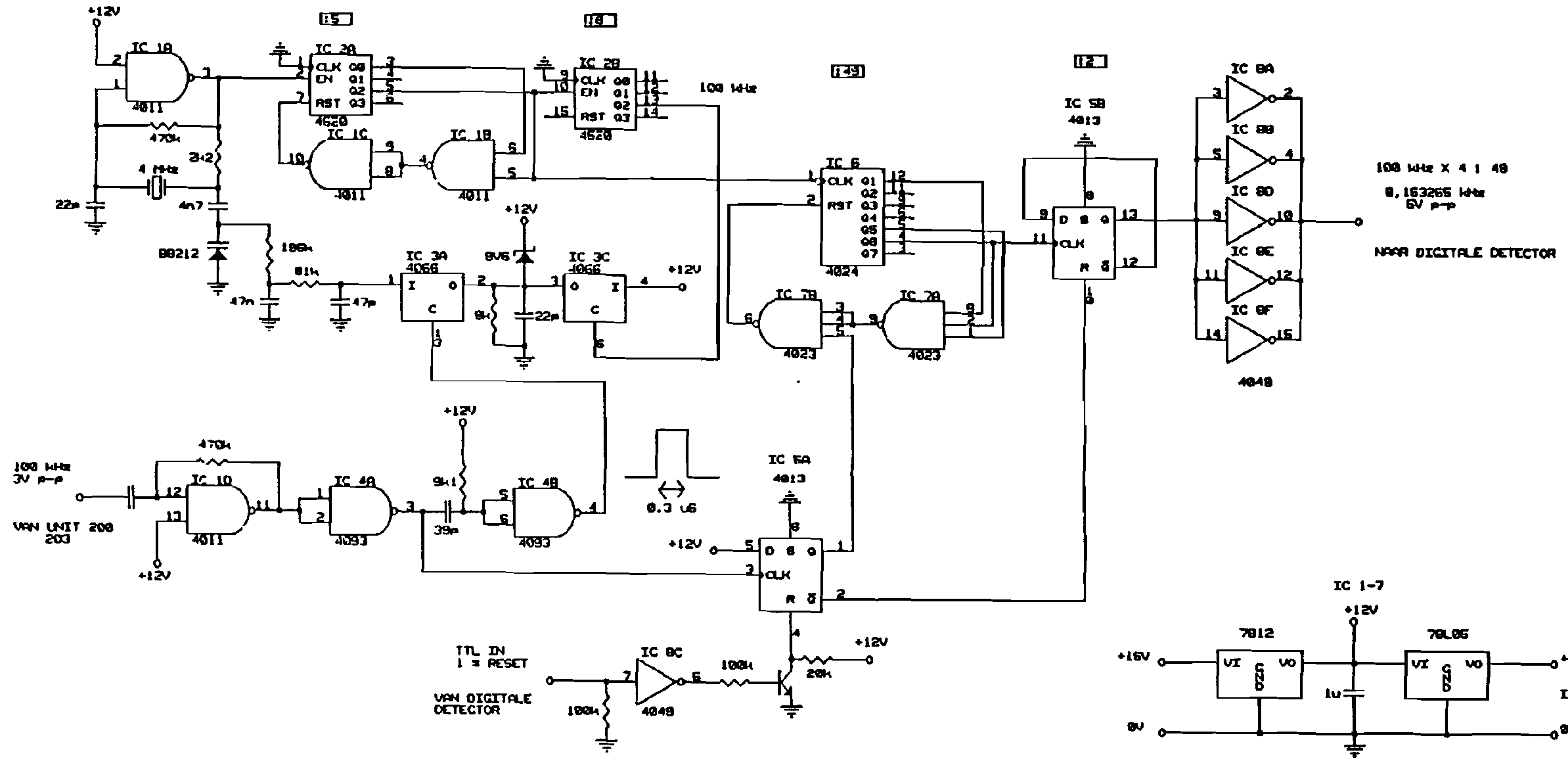


Fig. A.2: Anti-aliasing 125 kHz filter/amplifier.

Fig. A.3: Schematic diagram Unit 400.



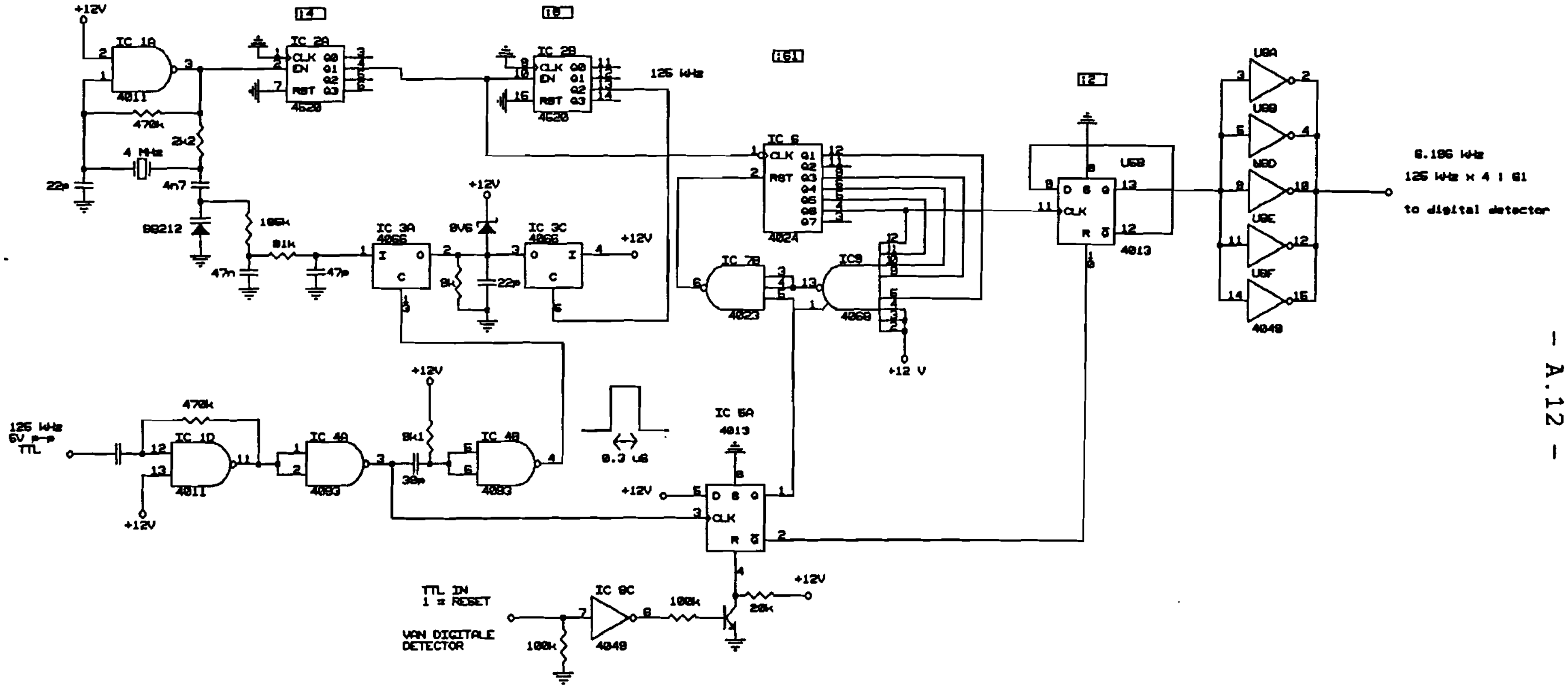


Fig. A.4: Modified version of Unit 400 for a 125 kHz input signal.

Appendix B: DNL Detector

EUT has at its disposal a digital I-Q detection system based upon the cheap Z-80 microprocessor. This system is developed by the Doctor Neher Laboratories, Leidschendam, the Netherlands. The specifications of this detector are as follows:

Z-80B microprocessor, 8-bit data bus, clock frequency 4 MHz.

Track-hold amplifier MN375.

12-bit A/D converter AD575A.

System designed for an IF of 100 kHz.

Sampling frequency 8.163 kHz, which is externally extracted and synchronized from the IF 100 kHz input signal.

Integrate-and-dump filter with selectable output sampling rate (1 Hz - 64 Hz) and bandwidth (0.5 - 4 Hz).

10-bit D/A converters NE5020 for amplitude and phase signal.

Logarithmic amplitude output, dynamic range 48 dB (-24 dBm - +24 dBm).

The schematic diagram of the DNL detector is shown in Fig. B.1.

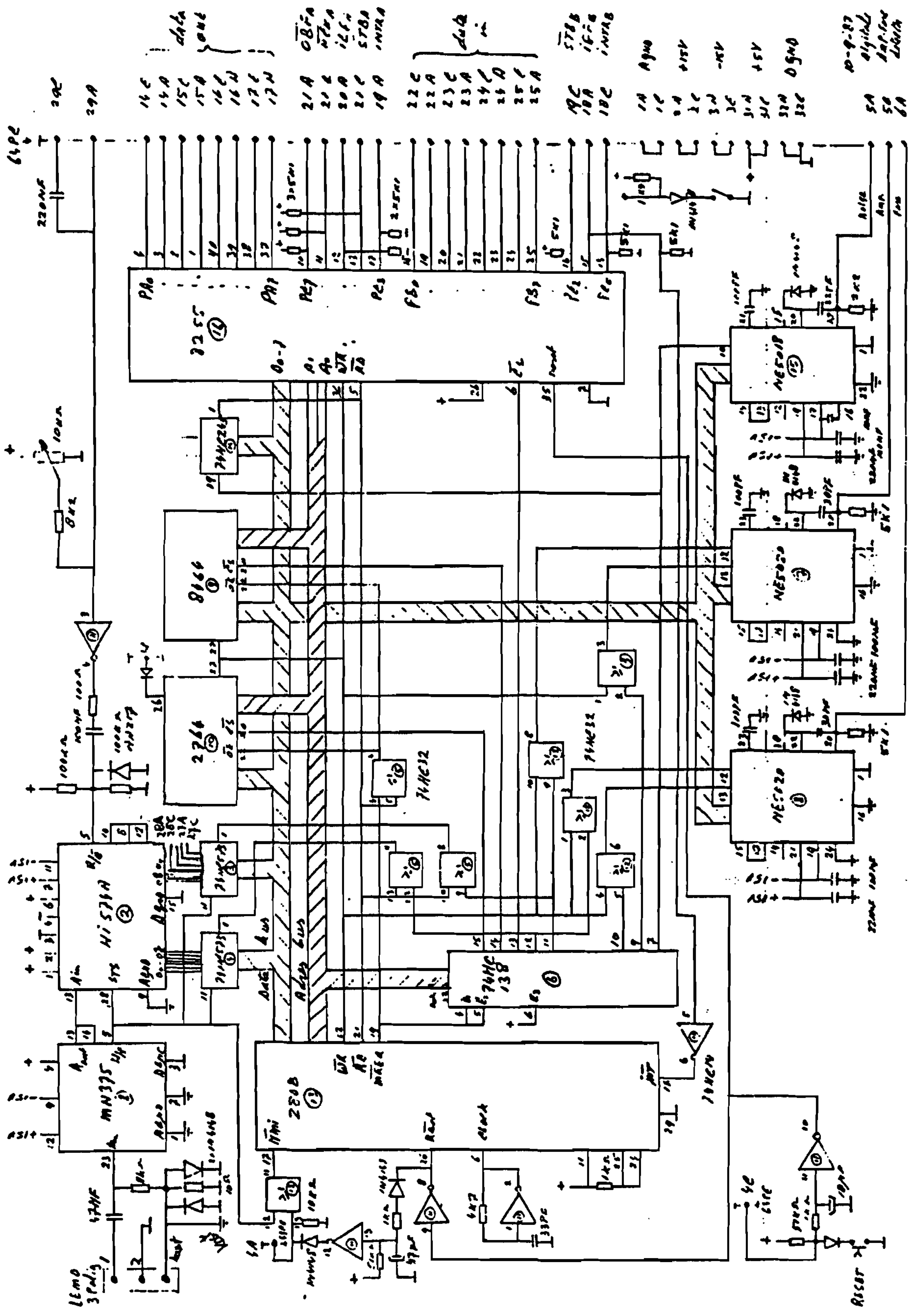


Fig. B.1: Schematic diagram DNL detector.

Appendix C: Track-hold amplifiers for high speed applications

Micro Networks

Track-Hold Amplifier Selection Guide

7-9 Bit Applications

Maximum Linearity Error (%)	Acquisition Time	Gain and Voltage Range	Model #	Specified Temp Range (°C)	Aperture Jitter (psec)	Droop Rate (µV/µs)	Power (mW)	DIP Package	Mil-Std-883 Hi-Rel Option	Page No.
±0.1	35nsec 5V Step to ±0.1%	+1, ±2.5V	MN379	0 to +70 −55 to +125	1	±500	1575	24 Pin	Yes	7-39

12-Bit Applications

Maximum Linearity Error (%)	Acquisition Time	Gain and Voltage Range	Model #	Specified Temp Range (°C)	Aperture Jitter (psec)	Droop Rate (µV/µs)	Power (mW)	DIP Package	Mil-Std-883 Hi-Rel Option	Page No.
±0.01	160nsec 10V Step to ±0.01%	−1, ±10V	MN376	0 to +70 −55 to +125	40	±0.5	730	24 Pin	Yes	7-35
±0.01	250nsec 10V Step to ±0.01%	−1, ±10V	MN9300A	0 to +70 −55 to +125	100	±5	730	24 Pin	Yes	7-5
±0.005	500nsec 10V Step to ±0.01%	−1, ±5V	MN375	0 to +70 −25 to +85	100	±0.5	1325	24 Pin	Yes	7-31
±0.01	1µsec 10V Step to ±0.01%	−1, ±10V	MN346	0 to +70 −55 to +125	400	±0.1	640	14 Pin	Yes	7-13
±0.01	1µsec 10V Step to ±0.05%	−1, ±10V	MN347	0 to +70 −55 to +125	400	±0.5	640	14 Pin	Yes	7-13
±0.01	6.5µsec 20V Step to ±0.01%	−1, ±10V	MN7130	0 to +70 −55 to +125	80 (1)	±4	900	32 Pin	Yes	8-9
±0.01	7.5µsec 10V Step to ±0.01%	−1, ±10V	MN343	0 to +70 −55 to +125	2000	±0.1	345	14 Pin	Yes	7-9
±0.01	7.5µsec 10V Step to ±0.05%	−1, ±10V	MN344	0 to +70 −55 to +125	2000	±0.4	345	14 Pin	Yes	7-9

Analog Devices

Selection Guide
Sample/Track and Hold Amplifiers

Model	Specified Accuracy %	Acquisition Time µs max	Aperture Time ns typ	Aperture Jitter ns typ	Droop Rate µV/µs max	Package Options[1]	Temp Range[2]	Page	Comments
*AD1154	0.00076	3.5	80	0.15	0.1	D	C, I	6-51	16-Bit Accurate Sample-and-Hold Amplifier
*AD386	0.00076	4.5	12	0.040	0.1	D	I, M	6-11	16-Bit Accurate Sample-and-Hold Amplifier
AD389	0.003	2.5	30	0.4	0.1	D	C, I	6-25	High Resolution Track-and-Hold Amplifier
HTC-0300A	0.01	0.1	6	0.05	0.5	D	I, M	6-57	Ultrahigh Speed Track-and-Hold Amplifier
*AD684	0.01	1.0	25	0.2	0.001	P, Q	C, I, M	6-43	Quad, Monolithic 1µs SHA
AD346	0.01	2.0	60	0.4	0.5	D	C, M	6-5	High Speed Sample-and-Hold
AD585	0.01	3.0	35	0.5	1	E, P, Q	C, I, M	6-37	High Speed, Precision. On-Board Hold Cap
AD583	0.01	5.0	50	5		D	C	6-35	5µs SHA
HTS-0010	0.01	0.014	2	0.005		D	C, I	6-61	Ultrahigh Speed Track-and-Hold Amplifier
HTS-0025	0.01	0.025	5	0.02		D	C, I	6-67	Ultrahigh Speed Track-and-Hold Amplifier
AD582	0.1	6.0	200	15		D, H	C, M	6-31	Low Cost, 15µs

[1] Package Options: D–Side-Brazed Dual-In-Line Ceramic; E–Leadless Chip Carrier; H–Round Hermetic Metal Can (Header); P–Plastic Leaded Chip Carrier (PLCC); Q–Cerdip.
[2] Temperature Ranges: C–Commercial, 0 to +70°C; I–Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M–Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product since the publication of the 1987/1988 Databooks.

Micro Networks
The MN379 track-hold amplifier can be applied to sample a full power 25 MHz signal with an accuracy of 9 bits.
MN376: full power bandwidth 8 MHz, 9-bit accuracy.
MN0300, MN375: full power bandwidth 5 MHz, 9-bit accuracy.

Analog Devices
HTS-0010: full power bandwidth 40 MHz, 9-bit accuracy
HTS-0025: full power bandwidth 20 MHz, 9-bit accuracy.
HTC-0300A: full power bandwidth 8 MHz, 9-bit accuracy.

All these very fast track-hold amplifiers are very expensive (500 - 2000 NLG). The track-hold amplifiers from Analog Devices are more easily available than of Micro Networks.

Appendix D: Modified EUT detector

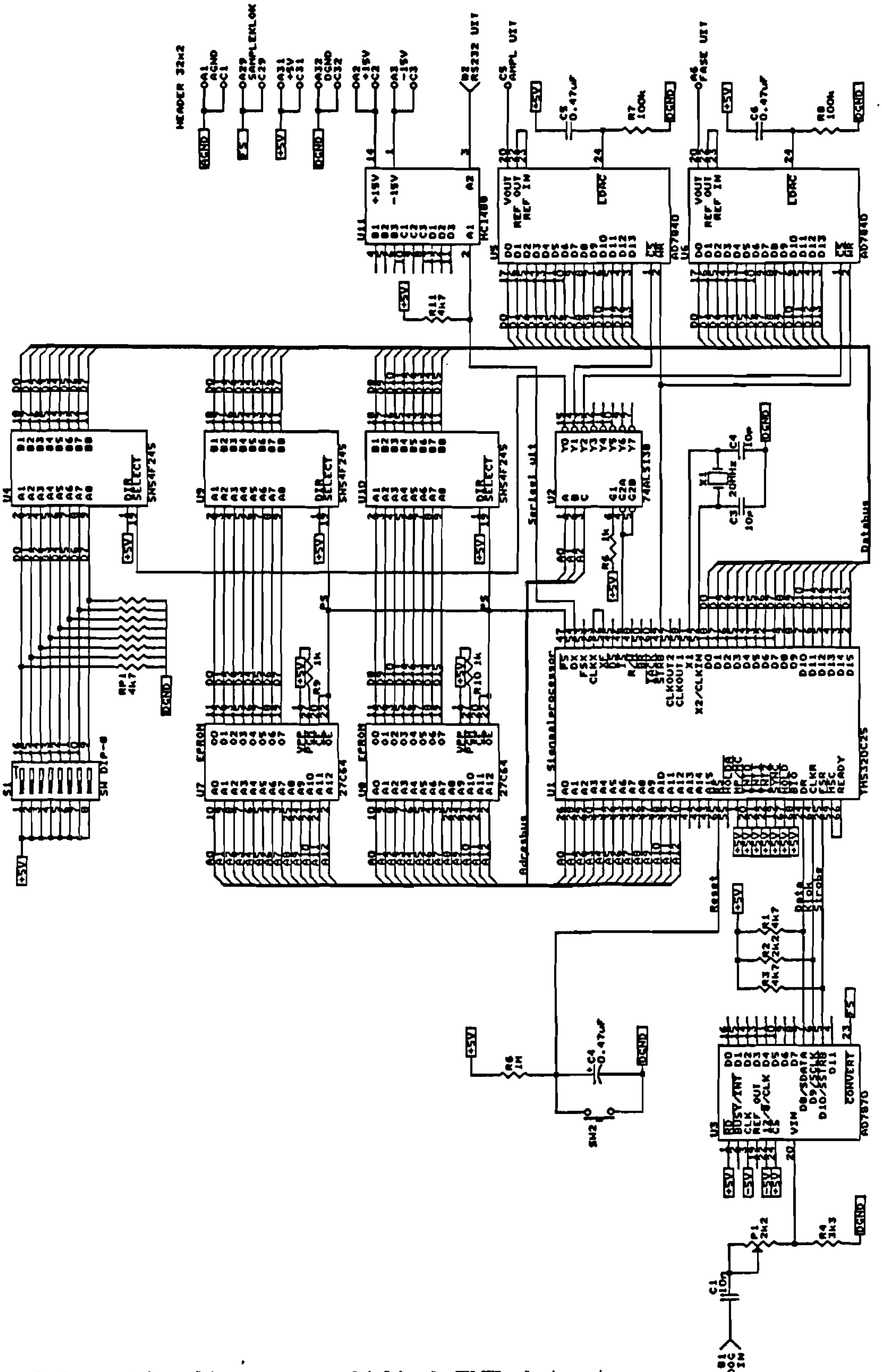


Fig. D.1: Schematic diagram modified EUT detector.

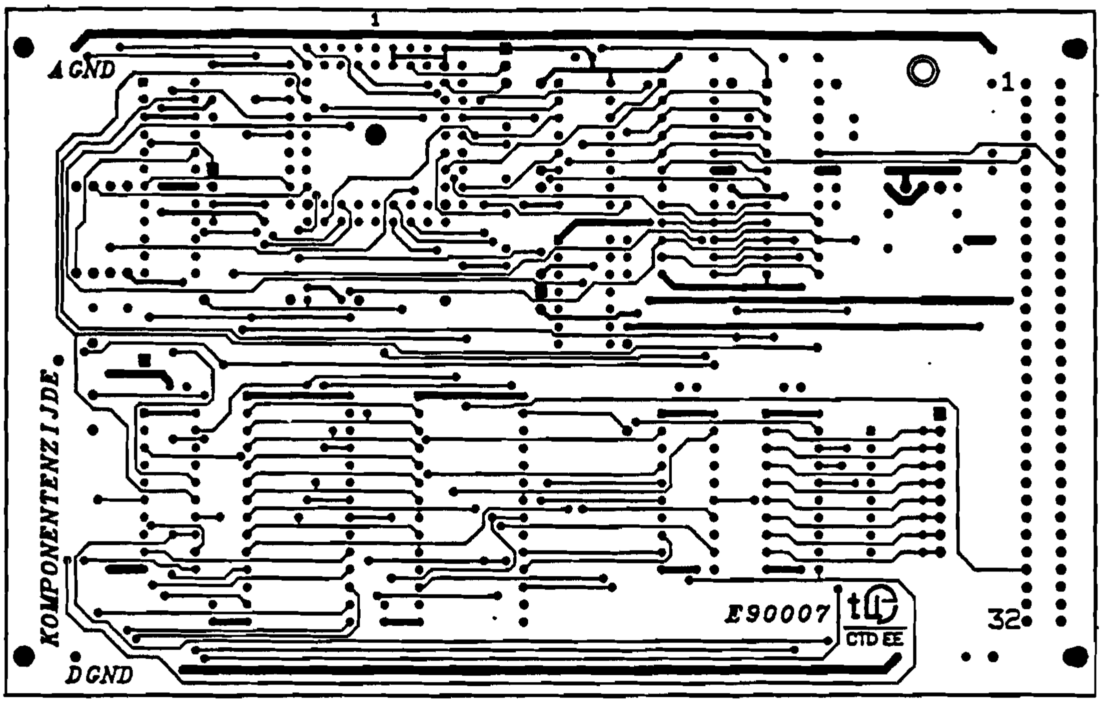


Fig. D.2: PCB component side layout.

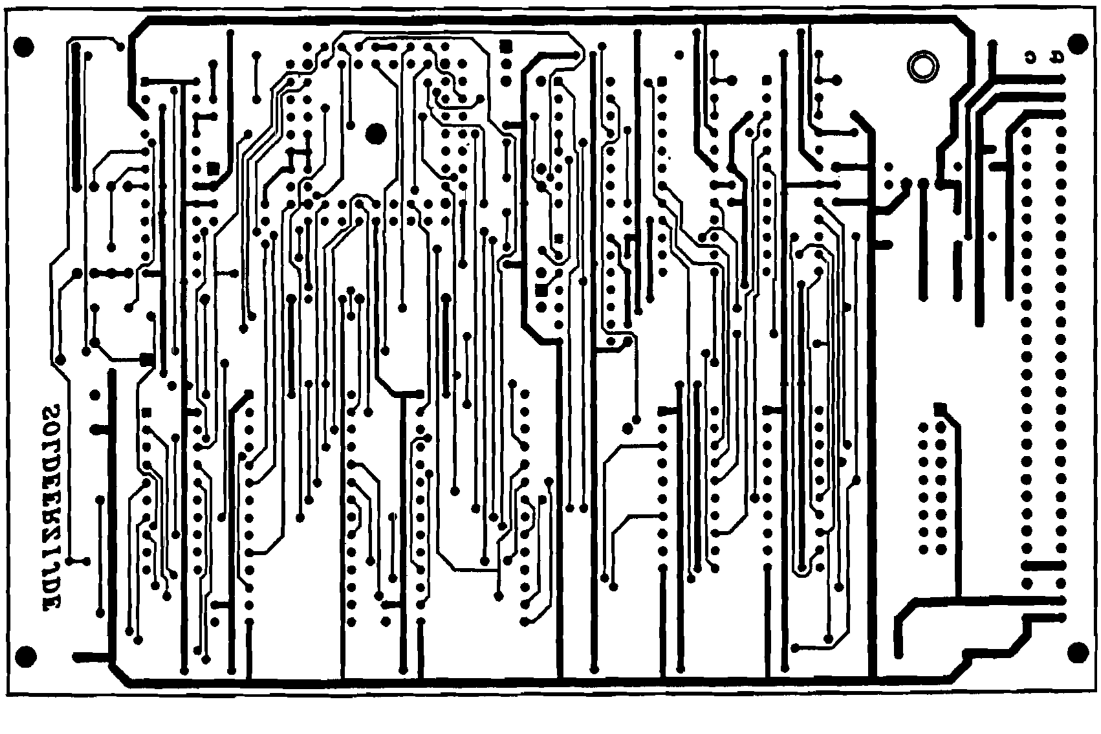


Fig. D.3: PCB solder side layout.

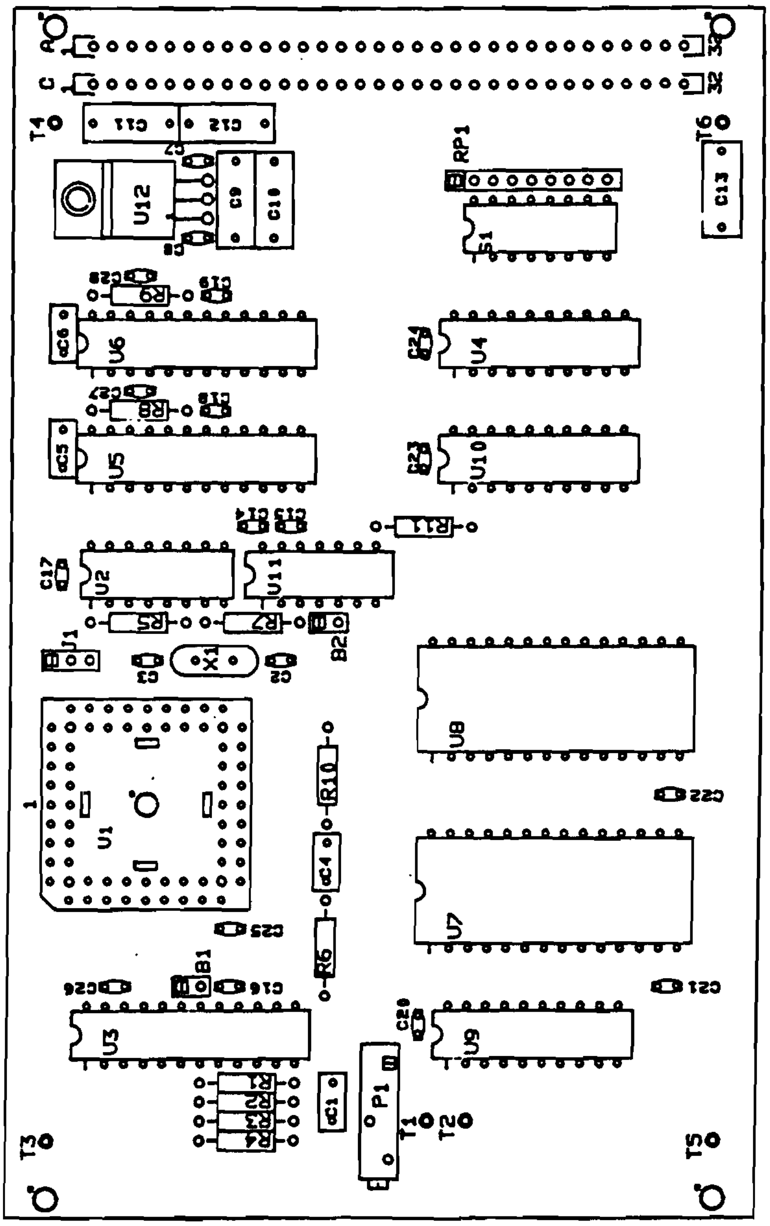


Fig. D.4: Components placement diagram.

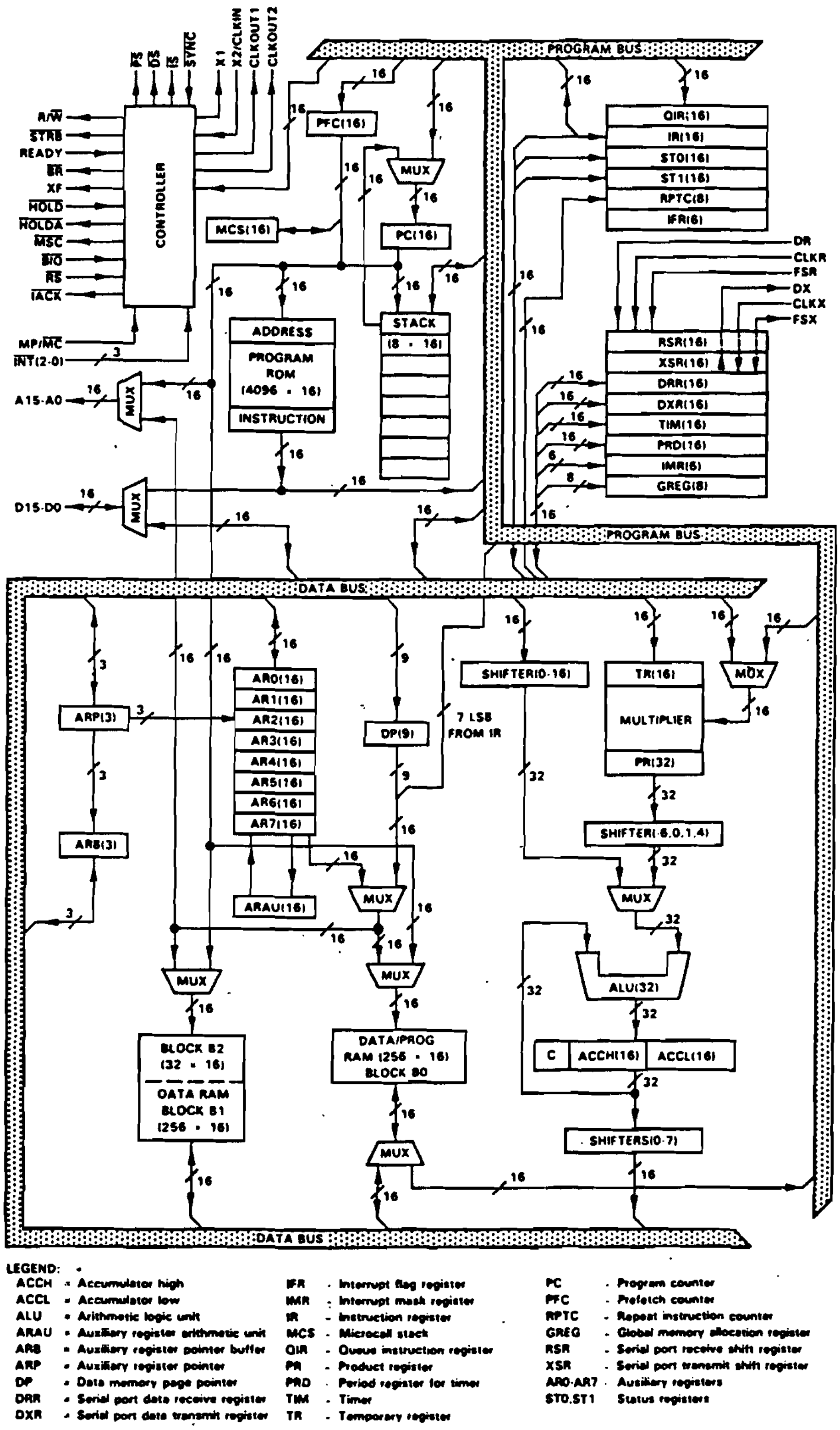
Appendix E: Data sheets components of modified EUT detector

TMS320C25, digital signal processor

the main features of the TMS320C25 are:

- 100 ns instruction cycle time
- 544-word programmable on-chip data RAM (256 words configurable as either data or program memory
- 4K x 16-bit on-chip program masked ROM
- Block moves for data/program memory
- Object-code compatible with TMS32020
- 128K words of memory space (64K words program and 64K words data)
- Repeat instructions
- Double buffered static serial port
- Sixteen input and sixteen output channels
- 16-bit parallel interface
- 32-bit ALU/accumulator
- 16 x 16-bit parallel multiplier with a 32-bit product
- Single-cycle multiply/accumulate instructions
- Eight auxiliary registers
- Eight-deep hardware stack
- On-chip clock
- Single 5-volt supply, CMOS technology, 68-pin PLCC

The block diagram of the TMS320C25 is shown in Fig. E.1.



TMS320C25 functional block diagram.

Fig. E.1: Block diagram of TMS320C25.

ANALOG DEVICES

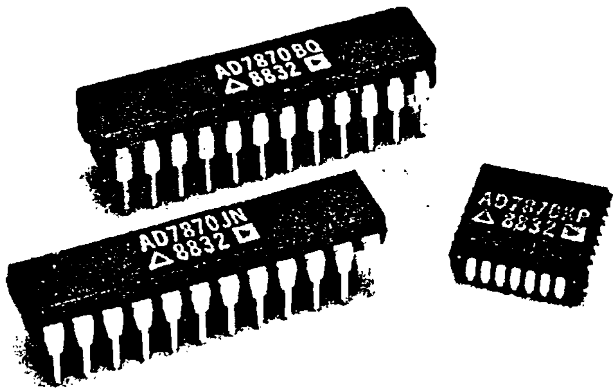
LC²MOS Complete, 12-Bit, 100kHz, Sampling ADC

AD7870

FEATURES
Complete Monolithic 12-Bit ADC with:
- **2μs Track/Hold Amplifier**
- **8μs A/D Converter**
- **On-Chip Reference**
- **Laser-Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

72dB SNR at 10kHz Input Frequency
57ns Data Access Time
Low Power – 60mW typ

APPLICATIONS
Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control



GENERAL DESCRIPTION

The AD7870 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8μs successive approximation ADC, 3V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The AD7870 offers a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

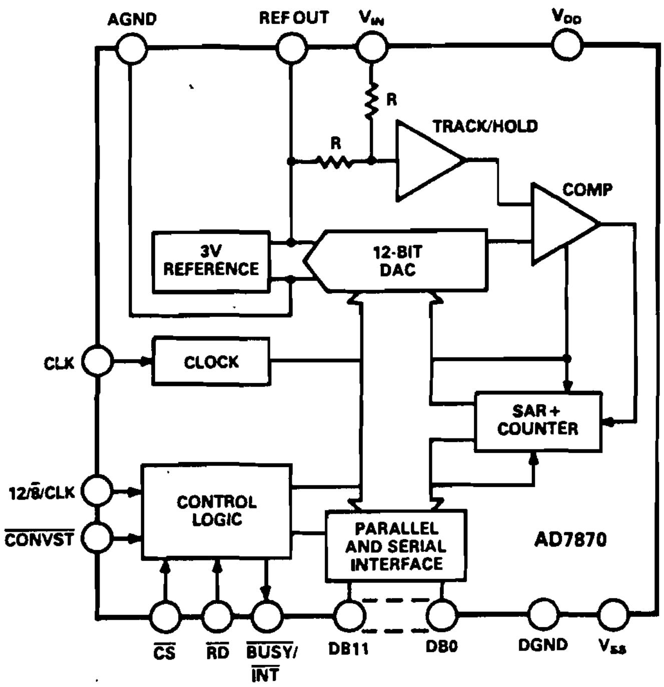
The AD7870 operates from ±5V power supplies, accepts bipolar input signals of ±3V and can convert full power signals up to 50kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7870 is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7870 is fabricated in Analog Devices' linear compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP) and in a 28-pin plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 12-bit ADC on a chip.
   The AD7870 is the most complete monolithic ADC available and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic specifications for DSP users.
   The AD7870 is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast microprocessor interface.
   Data access times of 57ns make the AD7870 compatible with modern 8- and 16-bit microprocessors and digital signal processors.



AD7870 Functional Block Diagram

SPECIFICATIONS

($V_{DD} = +5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, AGND = DGND = 0V, $f_{CLK} = 2.5MHz$ external, unless otherwise stated. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	70	70	dB min	V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz
T_{min} to T_{max}	70	70	71	70	70	dB min	Typically 71.5dB for 0 < V_{IN} < 50kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−80	−80	dB max	V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −86dB for 0 < V_{IN} < 50kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−80	−80	dB max	V_{IN} = 10kHz, f_{SAMPLE} = 100kHz Typically −86dB for 0 < V_{IN} < 50kHz
Intermodulation Distortion (IMD)							
Second Order Terms	−80	−80	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Third Order Terms	−80	−80	−80	−80	−80	dB max	fa = 9kHz, fb = 9.5kHz, f_{SAMPLE} = 50kHz
Track/Hold Acquisition Time	2	2	2	2	2	μs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	μA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0-500μA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5V ±5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	μA max	V_{IN} = 0V to V_{DD}.
Input Current (12/8/CLK Input Only)	±10	±10	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	μA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5MHz)	7.6/8	7.6/8	7.6/8	7.6/8	7.6/8	μs min/μs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	μs min/μs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8mA
I_{SS}	6	6	6	6	6	mA max	Typically 4mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60mW

NOTES

[1] Temperature ranges are as follows:
J, K, L Versions: 0 to +70°C
A, B, C Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2] V_{IN} (pk-pk) = ±3V.

[3] SNR calculation includes distortion and noise components.

[4] Measured with respect to internal reference and includes bipolar offset error.

[5] Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.
2	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the $12/\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the $12/\overline{8}$/CLK input is at −5V, then SCLK runs continuously. If $12/\overline{8}$/CLK is at 0V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7kΩ pull-up resistor is required on SDATA.
8−11	DB7/LOW–DB4/LOW	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the $12/\overline{8}$/CLK and HBEN inputs. With $12/\overline{8}$/CLK high, they are always DB7-DB4. With $12/\overline{8}$/CLK low or −5V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13−16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the $12/\overline{8}$/CLK and HBEN inputs. With/$12/\overline{8}$/CLK high, they are always DB3-DB0. With $12/\overline{8}$/CLK low or −5V, their function is controlled by HBEN (see Table I).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

Table I. Output Data for Byte Interfacing

17	V_{DD}	Positive Supply, +5V ±5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3V reference is provided at this pin. The external load capability is 500μA.
20	V_{IN}	Analog Input. The analog input range is ±3V.
21	V_{SS}	Negative Supply, −5V ±5%.
22	$12/\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5V, the output data format is 12-bit parallel only. With this pin at 0V, either byte or serial data is available and SCLK is not continuous. With this pin at −5V, byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK and independent of $\overline{CS}$ and $\overline{RD}$.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.

CONVERTER DETAILS

The AD7870 is a complete 12-bit A/D converter, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and SAR, a track/hold amplifier, a 3V buried Zener reference, a clock oscillator and control logic.

The conversion cycle normally consists of 19 clock periods, corresponding to a 7.6μs conversion time. The conversion time for both external and internal clock can vary from 19 to 20 clock cycles depending on the conversion start to ADC clock synchronization. If a conversion is initiated within 30ns prior to a rising edge of the ADC clock, the conversion time will consist of 20 clock cycles i.e., 8μs conversion time.

INTERNAL REFERENCE

The AD7870 has an on-chip temperature compensated buried Zener reference which is factory trimmed to 3V ±10mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and is capable of providing up to 500μA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50pF. If the reference is required for use external to the AD7870 it should be decoupled with a 200Ω resistor in series with a parallel combination of a 10μF tantalum capacitor and a 0.1μF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7870's internal operation.

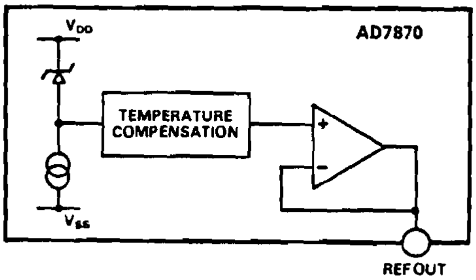


Figure 3. AD7870 Reference Circuit

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7870 allows the ADC to accurately convert an input sine wave of 6V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1dB cutoff frequency occurs typically at 500kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2μs. The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5MHz input clock the throughput rate is 10μs max.

The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. If the $\overline{CONVST}$ input is used to start conversion then the track to hold transition occurs on the rising edge of $\overline{CONVST}$. If $\overline{CS}$ starts conversion, this transition occurs on the falling edge of $\overline{CS}$.

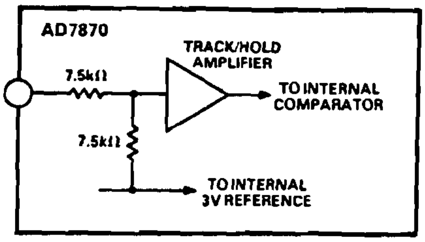


Figure 4. AD7870 Analog Input

ANALOG INPUT

Figure 4 shows the AD7870 analog input. The analog input range is ±3V into an input resistance of typically 15kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs, 5/2LSBs . . . FS−3/2LSBs). The output code is 2s complement binary with 1LSB = FS/4096 = 6V/4096 = 1.46mV. The ideal input/output transfer function is shown in Figure 5.

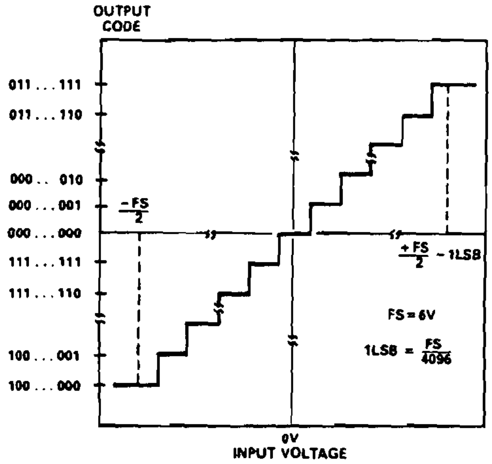


Figure 5. Bipolar Input/Output Transfer Function

BIPOLAR OFFSET AND FULL SCALE ADJUSTMEN

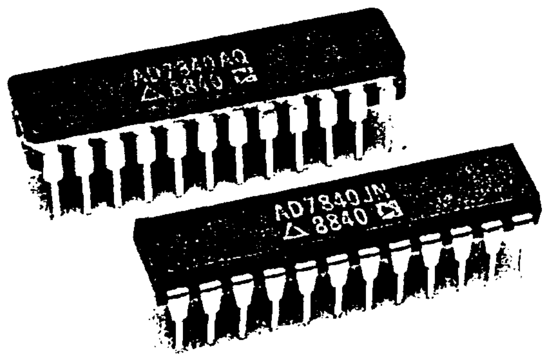
In most digital signal processing (DSP) applications, offset ar full-scale errors have little or no effect on system performanc Offset error can always be eliminated in the analog domain b ac coupling. Full-scale error effect is linear and does not cau problems as long as the input signal is within the full dynam range of the ADC. Some applications will require that the in signal span the full analog input dynamic range. In such app tions, offset and full-scale error will have to be adjusted to z

Where adjustment is required, offset error must be adjusted fore full-scale error. This is achieved by trimming the offset the op amp driving the analog input of the AD7870 while th input voltage is 1/2LSB below ground. The trim procedure follows: apply a voltage of −0.73mV(−1/2LSB) at V_1 in Fig 6 and adjust the op amp offset voltage until the ADC outpu code flickers between 1111 1111 1111 and 0000 0000 0000. error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive scale). The trim procedures for both cases are as follows (se Figure 6).

ANALOG DEVICES

LC²MOS Complete 14-Bit DAC

FEATURES
Complete 14-Bit Voltage Output DAC
Parallel and Serial Interface Capability
80dB Signal-to-Noise Ratio
Interfaces to High Speed DSP Processors
e.g., ADSP-2100, TMS32010, TMS32020
45ns min $\overline{WR}$ Pulse Width
Low Power – 70mW typ.
Operates from ±5V Supplies



GENERAL DESCRIPTION

The AD7840 is a fast, complete 14-bit voltage output D/A converter. It consists of a 14-bit DAC, 3V buried Zener reference, DAC output amplifier and high speed control logic.

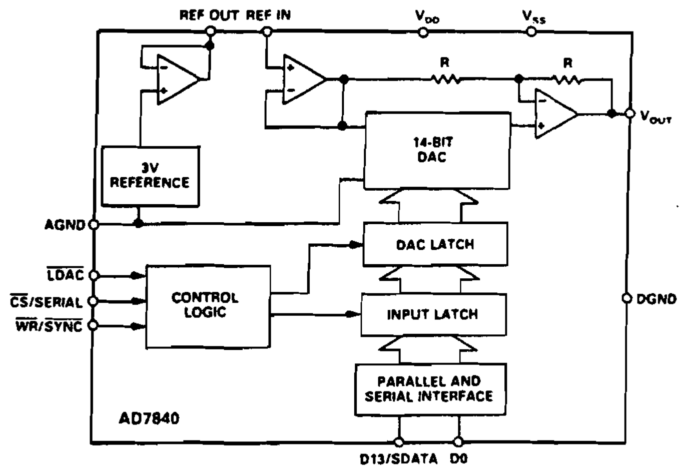
The part features double-buffered interface logic with a 14-bit input latch and 14-bit DAC latch. Data is loaded to the input latch in either of two modes, parallel or serial. This data is then transferred to the DAC latch under control of an asynchronous $\overline{LDAC}$ signal. A fast data setup time of 20ns allows direct parallel interfacing to digital signal processors and high speed 16-bit microprocessors. In the serial mode, the maximum serial data clock rate can be as high as 6MHz.

The analog output from the AD7840 provides a bipolar output range of ±3V. The AD7840 is fully specified for dynamic performance parameters such as signal-to-noise ratio and harmonic distortion as well as for traditional dc specifications. Full power output signals up to 20kHz can be created.

The AD7840 is fabricated in linear compatible CMOS (LC²MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin plastic and hermetic dual-in-line package (DIP) and is also packaged in a 28-terminal plastic leaded chip carrier (PLCC).

PRODUCT HIGHLIGHTS

1. Complete 14-Bit D/A Function
   The AD7840 provides the complete function for creating ac signals and dc voltages to 14-bit accuracy. The part features an on-chip reference, an output buffer amplifier and 14-bit D/A converter.
2. Dynamic Specifications for DSP Users
   In addition to traditional dc specifications, the AD7840 is specified for ac parameters including signal-to-noise ratio and harmonic distortion. These parameters along with important timing parameters are tested on every device.
3. Fast, Versatile Microprocessor Interface
   The AD7840 is capable of 14-bit parallel and serial interfacing. In the parallel mode, data setup times of 21ns and write pulse widths of 45ns make the AD7840 compatible with modern 16-bit microprocessors and digital signal processors. In the serial mode, the part features a high data transfer rate of 6MHz.



AD7840 Functional Block Diagram

SPECIFICATIONS (V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, AGND = DGND = 0V, REF IN = +3V, R_L = 2kΩ, C_L = 100pF. All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)	76	78	80	76	78	dB min	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically 82dB at +25°C for 0 < V_{OUT} < 20k
Total Harmonic Distortion (THD)	−78	−80	−84	−78	−80	dB max	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −84dB at +25°C for 0 < V_{OUT} < 2
Peak Harmonic or Spurious Noise	−78	−80	−84	−78	−80	dB max	V_{OUT} = 1kHz Sine Wave, f_{SAMPLE} = 100kHz Typically −84dB at +25°C for 0 < V_{OUT} < 2
DC ACCURACY							
Resolution	14	14	14	14	14	Bits	
Integral Nonlinearity	±2	±1	±1/2	±2	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic
Bipolar Zero Error	±10	±10	±5	±10	±10	LSB max	
Positive Full Scale Error[5]	±10	±10	±10	±10	±10	LSB max	
Negative Full Scale Error[5]	±10	±10	±10	±10	±10	LSB max	
REFERENCE OUTPUT[6]							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT TC	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Change (ΔREF OUT vs. ΔI)	−1	−1	−1	−1	−1	mV max	Reference Load Current Change (0-500μA)
REFERENCE INPUT							
Reference Input Range	2.85	2.85	2.85	2.85	2.85	V min	3V ±5%
	3.15	3.15	3.15	3.15	3.15	V max	
Input Current	50	50	50	50	50	μA max	
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5V ±5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5V ±5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	μA max	V_{IN} = 0V to V_{DD}
Input Current ($\overline{CS}$ Input Only)	±10	±10	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[7]	10	10	10	10	10	pF max	
ANALOG OUTPUT							
Output Voltage Range	±3	±3	±3	±3	±3	V Nom	
dc Output Impedance	0.1	0.1	0.1	0.1	0.1	Ω typ	
Short-Circuit Current	20	20	20	20	20	mA typ	
AC CHARACTERISTICS[7]							
Voltage Output Settling Time							Settling Time to within ±1/2LSB of Final V
Positive Full-Scale Change	4	4	4	4	4	μs max	Typically 2μs
Negative Full-Scale Change	4	4	4	4	4	μs max	Typically 2.5μs
Digital-to-Analog Glitch Impulse	10	10	10	10	10	nV secs typ	REF IN = 0V
Digital Feedthrough	2	2	2	2	2	nV secs typ	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	14	14	14	15	15	mA max	Output Unloaded, SCLK = +5V. Typically
I_{SS}	6	6	6	7	7	mA max	Output Unloaded, SCLK = +5V. Typically
Power Dissipation	100	100	100	110	110	mW max	Typically 70mW

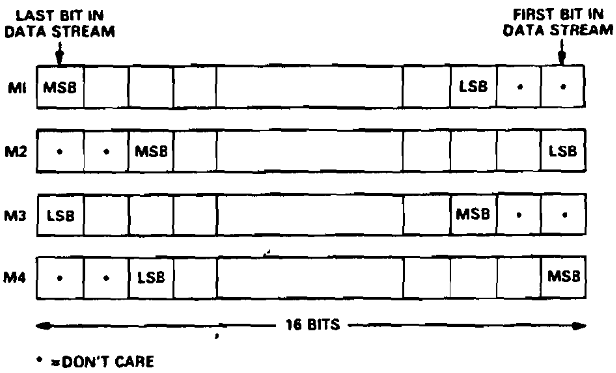
NOTES

[1]Temperature Ranges are as follows: J, K, L Versions, 0 to +70°C; A, B, C Versions, −25°C to +85°C; S, T Versions, −55°C to +125°C.
[2]V_{OUT} (pk-pk) = ±3V.
[3]SNR calculation includes distortion and noise components.
[4]Using external sample-and-hold (see Testing the AD7840).
[5]Measured with respect to REF IN and includes bipolar offset error.
[6]For capacitive loads greater than 50pF, a series resistor is required (see Internal Reference section).
[7]Sample tested @ 25°C to ensure compliance.

Specifications subject to change without notice.

PIN FUNCTION DESCRIPTION

DIP Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$/SERIAL	Chip Select/Serial Input. When driven with normal logic levels, it is an active low logic input which is used in conjunction with $\overline{WR}$ to load parallel data to the input latch. For applications where $\overline{CS}$ is permanently low, an R, C is required for correct power-up (see $\overline{LDAC}$ input). If this input is tied to V_{SS}, it defines the AD7840 for serial mode operation.
2	$\overline{WR}$/$\overline{SYNC}$	Write/Frame Synchronization Input. In the parallel data mode, it is used in conjunction with $\overline{CS}$ to load parallel data. In the serial mode of operation, this pin functions as a Frame Synchronization pulse with serial data expected after the falling edge of this signal.
3	D13/SDATA	Data Bit 13(MSB)/Serial Data. When parallel data is selected, this pin is the D13 input. In serial mode, SDATA is the serial data input which is used in conjunction with $\overline{SYNC}$ and SCLK to transfer serial data to the AD7840 input latch.
4	D12/SCLK	Data Bit 12/Serial Clock. When parallel data is selected, this pin is the D12 input. In the serial mode, it is the serial clock input. Serial data bits are latched on the falling edge of SCLK when $\overline{SYNC}$ is low.
5	D11/FORMAT	Data Bit 11/Data Format. When parallel data is selected, this pin is the D11 input. In serial mode, a logic 1 on this input indicates that the MSB is the first valid bit in the serial data stream. A logic 0 indicates that the LSB is the first valid bit (see Table I).
6	D10/JUSTIFY	Data Bit 10/Data Justification. When parallel data is selected, this pin is the D10 input. In serial mode, this input controls the serial data justification (see Table I).
7–11	D9—D5	Data Bit 9 to Data Bit 5. Parallel data inputs.
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	D4—D1	Data Bit 4 to Data Bit 1. Parallel data inputs.
17	D0	Data Bit 0 (LSB). Parallel data input.
18	V_{DD}	Positive Supply, +5V± 5%.
19	AGND	Analog Ground. Ground reference for DAC, reference and output buffer amplifier.
20	V_{OUT}	Analog Output Voltage. This is the buffer amplifier output voltage. Bipolar output range (±3V with REF IN = +3V).
21	V_{SS}	Negative Supply Voltage, −5V ±5%.
22	REF OUT	Voltage Reference Output. The internal 3V analog reference is provided at this pin. To operate the AD7840 with internal reference, REF OUT should be connected to REF IN. The external load capability of the reference is 500μA.
23	REF IN	Voltage Reference Input. The reference voltage for the DAC is applied to this pin. It is internally buffered before being applied to the DAC. The nominal reference voltage for correct operation of the AD7840 is 3V.
24	$\overline{LDAC}$	Load DAC. Logic input. A new word is loaded into the DAC latch from the input latch on the falling edge of this signal (see Interface Logic Information section). The AD7840 should be powered-up with $\overline{LDAC}$ high. For applications where $\overline{LDAC}$ is permanently low, an R, C is required for correct power-up (see Figure 19).



FORMAT	JUSTIFY	MODE
0	0	M1
0	1	M2
1	0	M3
1	1	M4

Table I. Serial Data Modes

Appendix F: Software of modified EUT detector

TMSROM version Intelsat: I-Q detection with integrate-and-dump filter.

```
*   Digital Detector Software version Intelsat
*
*
*
*   RELEASE DATE: 15-01-1991
*
*
*   This program calculates the amplitude and phase of a 125 kHz
*   IF signal using the I-Q detection method. The 20log is taken
*   of the amplitude.
*
*
*
*   Constants
*
DRR:     .equ   0          ;serial port data receive register
DXR:     .equ   1          ;serial port data transmit register
TIM:     .equ   2          ;timer register
PRD:     .equ   3          ;period register
IMR:     .equ   4          ;interrupt mask register
*
*
*   Variables
*
*   Global variables (page 0)
*
ILOW:    .equ   96         ;low word of I, used in int. handlers
IHIGH:   .equ   97         ;high word of I
QLOW:    .equ   98         ;low word of Q
QHIGH:   .equ   99         ;high word of Q
I:       .equ   100        ;variable I (two words), used in
                            main program
Q:       .equ   102        ;variable Q (two words)
SAMPLE:  .equ   104        ;data word (sample) from A/D converter
NUMSA:   .equ   105        ;number of samples for filtering
TS:      .equ   106        ;number of taken samples
HELP1:   .equ   107        ;help variable
HELP2:   .equ   108        ;help variable
HELPI:   .equ   109        ;help variable for interrupt handlers
FIRSTH:  .equ   110        ;address of first interrupt handler
AMPRES:  .equ   111        ;result of amplitude calculation
FASRES:  .equ   112        ;result of phase calculation
LOGRES:  .equ   113        ;result of log calculation (log routine)
OFFSET:  .equ   114        ;angle of zero phase
SHIFT:   .equ   115        ;number of right shifts for division
DUMMY:   .equ   116        ;dummy variable
INTADR:  .equ   117        ;address of interrupt handler
INTSAV:  .equ   118        ;status and accumulator (4 words)
*
*
*   Local variables of WINDOW (page 4)
```

```
I1HIGH: .equ   2
Q1LOW:  .equ   3          ;var Q, 1th group samples of time window
Q1HIGH: .equ   4
I2LOW:  .equ   5          ;var I, 2th group samples of time window
I2HIGH: .equ   6
Q2LOW:  .equ   7          ;var Q, 2th group samples of time window
Q2HIGH: .equ   8
*
*  Local variables of FASE (page 4)
*
COSH1:  .equ   9          ;help variable (cos routine)
COSH2:  .equ   10         ;help variable (cos routine)
STEP:   .equ   11         ;step value (cos routine)
INDEX:  .equ   12         ;index in table (cos routine)
*
*  Constants (page 4)
*
FAS180: .equ   13         ;is set to 1800 in INIT (for phase)
FAS360: .equ   14         ;is set to 3600 in INIT (for phase)
*
*  Variables for D/A converters
*
DAAMP:  .equ   15         ;amplitude data send to D/A converter
DAFASE: .equ   16         ;phase data send to D/A converter
*
*  Constants for D/A converters
*
SPAN1:  .equ   17         ;is set to 12342 in INIT
SPAN2:  .equ   18         ;is set to 1000 in INIT
*
        .sect   "Ints"
        B     INIT
        B     INIT
        B     INIT
        B     INIT
        .space 16*16
        B     RINT
        B     RINT
        B     RINT
*
*
*  Initialization
*
        .text
INIT    DINT              ;disable all interrupts
        RSXM              ;reset sign-extension mode
        LDPK  0           ;data page = 0
        LAC   IMR         ;load ACC with contents of IMR register
        ANDK  0fff0h      ;set bits 0, 1 and 2 to 0
        ORK   10h         ;set bits 3, 4 and 5 to 1
        SACL  IMR         ;store ACC in IMR register
        IN    HELP1,PA0   ;read dip-switches
        ZALS  HELP1       ;state of switches to ACC
        ANDK  07h         ;mask bits 0, 1 en 2
        ADLK  NSTAB       ;add begin address of table to offset
        TBLR  NUMSA       ;read number of samples from table
        ADDK  08h         ;shift 8 memory positions
        TBLR  SHIFT       ;read number of shifts for filtering
        LALK  SREAD1
        SACL  INTADR      ;store address of first input handler
```

```
        SACL   FIRSTH
        ZAC
        SACL   TS          ;set number of taken samples to 0
        SACL   ILOW        ;set I and Q to 0
        SACL   IHIGH
        SACL   QLOW
        SACL   QHIGH
        LDPK   4           ;data page = 4
        LALK   3600
        SACL   FAS360      ;set FAS360 to 3600
        SFR
        SACL   FAS180      ;set FAS180 to 1800
        LALK   12342
        SACL   SPAN1       ;offset for D/A converter of amplitude
        LALK   1000
        SACL   SPAN2       ;offset for D/A converter of phase
        LDPK   0           ;data page = 0
        LARK   AR2,0       ;set contents of aux. register 2 to 0
        LARP   AR0         ;AR0 is default register
        FORT   0           ;initialize 16-bits serial channel
        SFSM               ;frame sync. pulses are needed
        SPM    0           ;no shift of multiplier output
        EINT               ;interrupts are enabled
*
*
*  Main program
*
MAINP   CALL   WAIT        ;wait until enough samples taken
        CALL   FILTER      ;filtering
        CALL   AMPL        ;calculate log of amplitude
        CALL   FASE        ;calculate phase
        CALL   SCALE       ;scale AMPRES and FASRES for D/A conv.
        B      MAINP       ;return to MAINP
*
*
*  Wait loop
*
WAIT    OUT    DUMMY,PA3   ;testing utilized processor capacity
        LAC    NUMSA       ;ACC := NUMSA
        SUB    TS          ;subtract number of taken samples
        BGZ    WAIT        ;jump to WAIT if TS < NUMSA
        DINT               ;disable interrupts
        LDPK   4
        OUT    DAAMP,PA1   ;send amplitude to D/A converter
        OUT    DAFASE,PA2  ;send phase to D/A converter
        LDPK   0
        CALL   WINDOW      ;shift time window
        ZAC
        SACL   TS          ;set TS to 0
        SACL   ILOW        ;set I and Q to 0
        SACL   IHIGH
        SACL   QLOW
        SACL   QHIGH
        EINT               ;interrupts are enabled
        RET                ;return to main program MAINP
*
*
*  Filter
*
FILTER  SSXM               ;set sign-extension
```

```
        ZALH  I+1          ;load accumulator with I
        ADDS  I
        RPT   SHIFT        ;divide by 2^(SHIFT+1)
        SFR
        SACL  I            ;result to I
        ZALH  Q+1          ;Load accumulator with Q
        ADDS  Q
        RPT   SHIFT        ;divide by 2^(SHIFT+1)
        SFR
        SACL  Q            ;result to Q
        RSXM               ;reset sign-extension
        RET                ;return to main program MAINP
*
*
*  Calculate amplitude
*
AMPL    ZAC                ;set accumulator to 0
        MPYK  0            ;set P-register to 0
        SQRA  I            ;square I, P-register := I^2
        SQRA  Q            ;square Q, P-register := Q^2, ACC := I^2
        MPYA  DUMMY        ;ACC := I^2 + Q^2
        CALL  LOG          ;calculate logarithm
        SACL  AMPRES       ;store result in AMPRES
        RET                ;return to main program MAINP
*
*
*  Calculate phase
*
FASE    LALK  900          ;ACC := 900
        SACL  OFFSET       ;set OFFSET to 90 degrees
        ZAC                ;ACC := 0
        MPYK  0            ;P-register := 0
        SQRA  I            ;square I, P-register := I^2
        SQRA  Q            ;square Q, P-register := Q^2, acc := I^2
        SQRS  Q            ;ACC := I^2-Q^2, P-register := Q^2
        BGZ   FASE1        ;if I > Q, jump to FASE1
        LACK  0
        SACL  OFFSET       ;set OFFSET to 0 degrees
        SQRA  I            ;square I, P-register := I^2
FASE1   PAC                ;load accumulator with P-register
        CALL  LOG          ;calculate logarithm
        SUB   AMPRES       ;subtract log(I^2 + Q^2)
        ABS                ;make positive
        CALL  COS          ;calculate cos
        SUB   OFFSET       ;subtract OFFSET
        ABS                ;determine quadrant of the phase
        BIT   Q,0          ;test sign bit of Q
        BBZ   FASE3        ;if Q positive, jump to FASE3
        BIT   I,0          ;test sign bit of I
        BBNZ  FASE2        ;if I negative, jump to FASE2
        SACL  FASRES       ;quadrant is 1, store phase
        RET                ;return to main program MAINP
FASE2   LDPK  4            ;data page = 4
        SUB   FAS180       ;quadrant is 2, subtract 180 degrees
        ABS                ;make positive
        LDPK  0            ;data page = 0
        SACL  FASRES       ;store phase
        RET                ;return to main program MAINP
FASE3   BIT   I,0          ;quadrant is 3 or 4
        BBZ   FASE4        ;if I positive, jump to FASE4
```

```
        ADLK  1800        ;quadrant is 3, add 180 degrees
        SACL  FASRES      ;store phase
        RET               ;return to main program MAINP
FASE4   LDPK  4           ;data page = 4
        SUB   FAS360      ;quadrant is 4, subtract 360 degrees
        ABS               ;make positive
        LDPK  0           ;data page = 0
        SACL  FASRES      ;store phase
        RET               ;return to main program MAINP
*
*  Scale AMPRES and FASRES for optimum use of the D/A converters.
*  the data is sent to the DA conv. at the end of the waiting
*  routine. In this manner the transmission of data is triggered
*  with the sample clock.
*
SCALE   SOVM              ;set overflow mode
        SSXM              ;set sign-extension
        LAC   AMPRES,15   ;place AMPRES in high part of ACC (ACCH)
        SFL               ;
        SFL               ;scale with factor 2
        LDPK  4           ;data page = 4
        SUBH  SPAN1       ;subtract offset
        SACH  DAAMP       ;store ACCH in DAAMP
        RPTK  4           ;ACCH := ACCH x 6
        ADDH  DAAMP       ;
        SFR               ;scale result to 14-bit number
        SFR               ;for D/A converter
        SACH  DAAMP       ;store ACCH in DAAMP
        ROVM              ;reset overflow mode
        SPM   3           ;shift of output p register is set to 6
        LDPK  0           ;data page = 0
        LAC   FASRES      ;load ACC with FASRES (phase)
        LDPK  4           ;data page = 4
        SUB   SPAN2       ;subtract 100 degrees of phase
        SACL  DAFASE      ;store result in DAFASE
        ZAC               ;ACC := 0
        LT    DAFASE      ;multiply T-register with 349
        MPYK  349
        APAC              ;load ACC with result and
        SFR               ;divide by 64 x 2
        SACL  DAFASE      ;store result in DAFASE
        LDPK  0           ;data page = 0
        SPM   0           ;reset P-register output shift mode
        RSXM              ;reset sign-extension mode
        RET               ;return to main program MAINP
*
*
*  Subroutines.
*
*  Window routine (used by WAIT)
*
*  Shift time window
*
WINDOW  LDPK  4
        ZALH  I1HIGH      ;ACC := I1LOW/I1HIGH
        ADDS  I1LOW
        SACL  I2LOW       ;I2LOW/I2HIGH := I1LOW/I1HIGH
        SACH  I2HIGH
        ZALH  Q1HIGH      ;ACC := Q1LOW/Q1HIGH
        ADDS  Q1LOW
```

```
        SACL  Q2LOW       ;Q2LOW/Q2HIGH := Q1low/Q1HIGH
        SACH  Q2HIGH
        LDPK  0
        ZALH  IHIGH       ;ACC := ILOW/IHIGH
        ADDS  ILOW
        LDPK  4
        SACL  I1LOW       ;I1LOW/I1HIGH := ILOW/IHIGH
        SACH  I1HIGH
        LDPK  0
        ZALH  QHIGH       ;ACC := QLOW/QHIGH
        ADDS  QLOW
        LDPK  4
        SACL  Q1LOW       ;Q1LOW/Q1HIGH := QLOW/QHIGH
        SACH  Q1HIGH
        ZALH  I1HIGH      ;add I1LOW/I1HIGH with I2LOW/I2HIGH
        ADDH  I2HIGH
        ADDS  I1LOW
        ADDS  I2LOW
        LDPK  0
        SACL  I           ;store in I/I+1
        SACH  I+1
        LDPK  4
        ZALH  Q1HIGH      ;add Q1LOW/Q1HIGH with Q2LOW/Q2HIGH
        ADDH  Q2HIGH
        ADDS  Q1LOW
        ADDS  Q2LOW
        LDPK  0
        SACL  Q           ;store in Q/Q+1
        SACH  Q+1
        RET               ;return to WAIT
*
*
*  Log routine (used by AMPLITUDE)
*
*  The logarithm is calculated of the 32-bit number in ACC.
```

$$* \quad \text{32-bit number} = 2^{m}.(1 + \sum_{n=0}^{m-1} b_n.2^{(n-m)}) = \text{base x correction}$$

```
*  log(32-bit number) = log(base) + log(correction)
*  m is highest " 1 " bit. Only 9 of the 32 bits are used.
*  The auxiliary register AR1 is used.
*  The result is stored in the variable LOGRES.
*
LOG     LARK  AR1,31      ;initialize counter
        LARP  1           ;auxiliary register AR1 is active
LOG1    SFL               ;shift MSB in carry bit
        BC    LOG2        ;if carry = 1 then highest '1'-bit found
        BANZ  LOG1        ;decrease counter, if counter <> 0 cont.
        BNZ   LOG2        ;if ACC <> 0 correction must be found
        SACL  LOGRES      ;else log = 0, store result
        RET               ;return to AMPL or FASE
LOG2    RPTK  8           ;repeat next instruction 8 + 1 times
        ROL               ;rotate ACC left
        ANDK  0ffh        ;mask index: bit 0-7
        ADLK  LOGCOR      ;add start address of cor. table to index
        TBLR  LOGRES      ;copy correction to result LOGRES
        SAR   AR1,HELP1   ;copy counter (index) via variable to ACC
        ZALS  HELP1
        ADLK  LOGBAS      ;add start address of base table to index
        TBLR  HELP1       ;copy base to variable
```

```
        ZALS   HELP1        ;add base and correction
        ADDS   LOGRES
        SACL   LOGRES       ;store result in LOGRES
        RET                 ;return to AMPL or FASE
*
*
*   Cosinus-routine (used by FASE).
*
*   Angle between the I-Q-vector and the I- or Q-axis is determined
*
*   cosα = |Q|/(A)  or  -log(cosα) = log(A) - log(|Q|)
*
COS     ABS
        LDPK   4            ;data page = 4
        SACL   COSH1        ;store in COSH1
        LALK   256          ;initialize INDEX to 25.6 degrees
        SACL   INDEX
        LALK   128          ;initialize STEP to 12.8 degrees
COS1    SACL   STEP
        ZALS   INDEX        ;load ACC with INDEX
        ADLK   COSTAB       ;add start address table
        TBLR   COSH2        ;read value out table
        ZALS   COSH2        ;copy to ACC
        SUB    COSH1        ;compare with wanted phase
        BLZ    COS3         ;if wanted phase > read phase, go to COS3
        ZALS   INDEX        ;phase smaller, decrease INDEX with STEP
        SUB    STEP
COS2    SACL   INDEX        ;store new INDEX
        ZALS   STEP         ;divide STEP by 2
        SFR
        BGZ    COS1         ;INDEX > 0 try further
        ZALS   INDEX        ;ready: load ACC with result
        ADLK   450          ;add 45 degrees
        LDPK   0            ;data page = 0
        RET                 ;return to FASE
COS3    ZALS   INDEX        ;phase larger, add INDEX with STEP
        ADD    STEP
        B      COS2         ;jump to COS2
*
*
*   Handler for serial input
*
*   A sample is taken from the input register DRR and a sub handler
*   handles the input datawoord.
*   Status registers and ACC are stored in INTSAV - INTSAV+3.
*   INTADR is loaded with the address of the next sub handler
*
RINT    DINT                ;interrupts are disabled
        SST1   INTSAV       ;store status register 1
        SST    INTSAV+1     ;store status register 2
        LDPK   0            ;data page = 0
        SACL   INTSAV+2     ;store ACCL
        SACH   INTSAV+3     ;store ACCH
        SSXM                ;set sign-extension
        LAC    DRR          ;read data from input register DRR
        RPTK   3            ;multiply by 16
        SFL
        SACL   SAMPLE       ;store in SAMPLE
        BIT    SAMPLE,0     ;test sign bit
        BBZ    JUMP         ;if bit 15 = 0 jump to JUMP
```

```
        ORK     0fh           ;set 4 highest bits to 1
        SACL    SAMPLE        ;store result in SAMPLE
JUMP    LAC     INTADR        ;load address of sub handler
        BACC                  ;jump to address in accumulator
RESTOR  SACL    INTADR        ;store address next sub handler
        LAC     TS            ;copy counter to accumulator
        ADDK    1             ;subtract 1
        SACL    TS            ;copy result to TS
        ZALH    INTSAV+3      ;restore accumulator
        ADDS    INTSAV+2
        LST1    INTSAV        ;restore status register 1
        LST     INTSAV+1      ;restore status register 2
        EINT                  ;enable interrupts
        RET                   ;return to main program MAINP
*
*   Sub handlers for serial input.
*
*   SAMPLE is added or subtracted of I or Q.
*   The address of the next sub handler is stored in INTADR.
*
*   SAMPLE is added to ILOW/IHIGH.
*
SREAD1  ZALH    IHIGH         ;ACC := I
        ADDS    ILOW
        ADD     SAMPLE        ;add SAMPLE to ACC
        SACL    ILOW          ;store ACCL
        SACH    IHIGH         ;store ACCH
        LALK    SREAD2        ;address next sub handler
        B       RESTOR
*
*   SAMPLE is added to QLOW/QHIGH.
*
SREAD2  ZALH    QHIGH         ;ACC := Q
        ADDS    QLOW
        ADD     SAMPLE        ;add SAMPLE to ACC
        SACL    QLOW          ;store ACCL
        SACH    QHIGH         ;store ACCH
        LALK    SREAD3        ;address next sub handler
        B       RESTOR
*
*   SAMPLE is subtracted of ILOW/IHIGH.
*
SREAD3  ZALH    IHIGH         ;ACC := I
        ADDS    ILOW
        SUB     SAMPLE        ;subtract SAMPLE of ACC
        SACL    ILOW          ;store ACCL
        SACH    IHIGH         ;store ACCH
        LALK    SREAD4        ;address next sub handler
        B       RESTOR
*
*   SAMPLE is subtracted of QLOW/QHIGH.
*
SREAD4  ZALH    QHIGH         ;ACC := Q
        ADDS    QLOW          ;
        SUB     SAMPLE        ;subtract SAMPLE of ACC
        SACL    QLOW          ;store ACCL
        SACH    QHIGH         ;store ACCH
        LALK    SREAD1        ;address next sub handler
        B       RESTOR
*
```

```
*
*  Tables
*
*  Table with the number of samples between two calculations
*  and the number of right shifts needed for division.
*
NSTAB:   .word 256,512,1024,2048,4096,8192,16384,16384
         .word 7,8,9,10,11,12,13,13
*
*  Table with log (2^x), 0 <= x <= 31, Base
*
LOGBAS:  .word 0,301,602,903,1204,1505,1806,2107,2408,2709
         .word 3010,3311,3612,3913,4214,4515,4816,5118,5419,5720
         .word 6021,6322,6623,6924,7225,7526,7827,8128,8429,8730
         .word 9031,9332
*
*  Table with correction
*
LOGCOR:  .word 0,2,3,5,7,8,10,12,13,15
         .word 17,18,20,22,23,25,26,28,30,31
         .word 33,34,36,37,39,40,42,44,45,47
         .word 48,50,51,53,54,56,57,59,60,62
         .word 63,65,66,67,69,70,72,73,75,76
         .word 77,79,80,82,83,85,86,87,89,90
         .word 91,93,94,96,97,98,100,101,102,104
         .word 105,106,108,109,110,112,113,114,116,117
         .word 118,119,121,122,123,125,126,127,128,130
         .word 131,132,133,135,136,137,138,140,141,142
         .word 143,144,146,147,148,149,150,152,153,154
         .word 155,156,158,159,160,161,162,163,165,166
         .word 167,168,169,170,172,173,174,175,176,177
         .word 178,179,181,182,183,184,185,186,187,188
         .word 189,191,192,193,194,195,196,197,198,199
         .word 200,201,202,203,205,206,207,208,209,210
         .word 211,212,213,214,215,216,217,218,219,220
         .word 221,222,223,224,225,226,227,228,229,230
         .word 231,232,233,234,235,236,237,238,239,240
         .word 241,242,243,244,245,246,247,248,249,250
         .word 251,252,253,254,255,255,256,257,258,259
         .word 260,261,262,263,264,265,266,267,268,268
         .word 269,270,271,272,273,274,275,276,277,278
         .word 278,279,280,281,282,283,284,285,285,286
         .word 287,288,289,290,291,292,292,293,294,295
         .word 296,297,298,298,299,300
*
*  Table for cosinus routine
*
COSTAB:  .word  301,303,304,306,307,309,310,312,313,315
         .word  316,318,320,321,323,324,326,328,329,331
         .word  332,334,336,337,339,341,342,344,346,347
         .word  349,351,352,354,356,357,359,361,363,364
         .word  366,368,370,371,373,375,377,378,380,382
         .word  384,386,387,389,391,393,395,397,399,400
         .word  402,404,406,408,410,412,414,416,417,419
         .word  421,423,425,427,429,431,433,435,437,439
         .word  441,443,445,447,449,451,453,455,457,459
         .word  462,464,466,468,470,472,474,476,479,481
         .word  483,485,487,489,492,494,496,498,500,503
         .word  505,507,509,512,514,516,519,521,523,525
         .word  528,530,532,535,537,540,542,544,547,549
```

```
          .word  552,554,556,559,561,564,566,569,571,574
          .word  576,579,581,584,586,589,592,594,597,599
          .word  602,605,607,610,613,615,618,621,623,626
          .word  629,632,634,637,640,643,645,648,651,654
          .word  657,660,663,665,668,671,674,677,680,683
          .word  686,689,692,695,698,701,704,707,710,713
          .word  716,719,723,726,729,732,735,738,742,745
          .word  748,751,755,758,761,765,768,771,775,778
          .word  781,785,788,792,795,799,802,806,809,813
          .word  816,820,823,827,831,834,838,842,845,849
          .word  853,857,860,864,868,872,876,880,883,887
          .word  891,895,899,903,907,911,915,920,924,928
          .word  932,936,940,944,949,953,957,962,966,970
          .word  975,979,984,988,993,997,1002,1006,1011,1015
          .word  1020,1025,1029,1034,1039,1044,1049,1053,1058,1063
          .word  1068,1073,1078,1083,1088,1093,1098,1104,1109,1114
          .word  1119,1125,1130,1135,1141,1146,1152,1157,1163,1168
          .word  1174,1180,1185,1191,1197,1203,1209,1215,1221,1227
          .word  1233,1239,1245,1251,1257,1264,1270,1276,1283,1289
          .word  1296,1302,1309,1316,1323,1329,1336,1343,1350,1357
          .word  1364,1371,1379,1386,1393,1401,1408,1416,1423,1431
          .word  1439,1447,1455,1463,1471,1479,1487,1495,1504,1512
          .word  1521,1529,1538,1547,1556,1565,1574,1583,1592,1602
          .word  1611,1621,1631,1641,1651,1661,1671,1681,1692,1702
          .word  1713,1724,1735,1746,1757,1769,1780,1792,1804,1816
          .word  1828,1841,1853,1866,1879,1892,1906,1919,1933,1947
          .word  1962,1976,1991,2006,2021,2037,2053,2069,2085,2102
          .word  2119,2137,2155,2173,2192,2211,2230,2250,2271,2291
          .word  2313,2335,2357,2380,2404,2429,2454,2480,2506,2534
          .word  2562,2592,2622,2654,2687,2721,2756,2793,2832,2872
          .word  2914,2959,3006,3055,3108,3164,3224,3288,3358,3434
          .word  3516,3608,3710,3826,3960,4118,4312,4562,4914,5516
.word  18999,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32677
*
*
*
          .end
```

DSPFIR version Intelsat: I-Q detection with FIR filter

```
*   Digital Detection Software version Intelsat
*
*   PROPAGATION, assembler source TMS320C25
*
*   RELEASE DATE: 19 january 1991
*
*   This program calculates the amplitude and phase of a 125 kHz
*   IF signal using the I-Q detection method. The 20log is taken
*   of the amplitude. The FIR filter consists of 12 sections.
*
*   Constants
*
DRR:     .equu   0        ;serial data receive register
DXR:     .equ    1        ;serial data transmit register
TIM:     .equ    2        ;timer register
PRD:     .equ    3        ;period register
IMR:     .equ    4        ;interrupt mask register
*
*
*   Variables
*   Global (page 0)
*
BRANCH:  .equ    96       ;indicates to a branch (I/Q) for new sample
MULTI:   .equ    97       ;multiply sample in I-branch with 1 or -1
MULTQ:   .equ    98       ;multiply sample in Q-branch with 1 or -1
DATAVA:  .equ    99       ;filtered values valid
I:       .equ    100      ;variable I
Q:       .equ    101      ;variable Q
DAAMP:   .equ    102      ;data for DA-converter 1 (amplitude)
DAFASE:  .equ    103      ;data for DA-converter 2 (phase)
SAMPLE:  .equ    104      ;data word (sample) from A/D converter
HELP1:   .equ    105      ;global help variable
HELP2:   .equ    106      ;global help variable
FAS180:  .equ    107      ;offset for phase
FAS360:  .equ    108      ;offset for phase
AMPRES:  .equ    109      ;result of amplitude calculation
FASRES:  .equ    110      ;result of phase calculation
LOGRES:  .equ    111      ;result of log calculation (log routine)
OFFSET:  .equ    112      ;phase offset
DUMMY:   .equ    113      ;dummy variable
SPAN1:   .equ    114      ;offset for scaling routine amplitude
SPAN2:   .equ    115      ;offset for scaling routine phase
COSH1:   .equ    116      ;help variable (cos routine)
COSH2:   .equ    117      ;help variable (cos routine)
STEP:    .equ    118      ;step size (cos routine)
INDEX:   .equ    119      ;index in table (cos routine)
TINTSA:  .equ    120      ;status en accumulator, timer interrupt
*
*   Assembler Constants
*
BASE:    .equ    26       ;offset for start delay lines
LFIL1:   .equ    11       ;length filter 1
LFIL2:   .equ    11       ;length filter 2
LFIL3:   .equ    11       ;length filter 3
LFIL4:   .equ    11       ;length filter 4
LFIL5:   .equ    11       ;length filter 5
LFIL6:   .equ    11       ;length filter 6
```

```
LFIL7:  .equ   11        ;length filter 7
LFIL8:  .equ   11        ;length filter 8
LFIL9:  .equ   11        ;length filter 9
LFIL10: .equ   13        ;length filter 10
LFIL11: .equ   17        ;length filter 11
LFIL12: .equ   71        ;length filter 12
LPRFIL: .equ   21        ;length pre filter
*
*  Total length filters in constant TOTLEN
*
LEN1:   .equ   LFIL1+LFIL2+LFIL3+LFIL4+LFIL5+LFIL6
LEN2:   .equ   LFIL7+LFIL8+LFIL9+LFIL10+LFIL11+LFIL12
TOTLEN: .equ   LEN1+LEN2+LPRFIL
*
*  Positions of delay lines
*
*  Watch out: The delay lines for the I and Q branch
*  are on the same position in different pages !!
*  I-branch on page 4
*  Q-branch on page 6
*
*
DEL1B:  .equ   0
DEL1:   .equ   1
DEL2:   .equ   2
DEL3:   .equ   3
DEL4:   .equ   4
DEL5:   .equ   5
DEL6:   .equ   6
DEL7:   .equ   7
DEL8:   .equ   8
DEL9:   .equ   9
DEL10:  .equ   10
DEL11:  .equ   11
DEL12:  .equ   12
CNT1:   .equ   13        ;counter1 (CNT1) to counter 12 (CNT12)
CNT2:   .equ   14
CNT3:   .equ   15
CNT4:   .equ   16
CNT5:   .equ   17
CNT6:   .equ   18
CNT7:   .equ   19
CNT8:   .equ   20
CNT9:   .equ   21
CNT10:  .equ   22
CNT11:  .equ   23
CNT12:  .equ   24
DELPR:  .equ   25
*
*
        .sect  "Ints"
        B      INIT
        B      INIT
        B      INIT
        B      INIT
        .space 16*16
        B      RINT
        B      RINT
        B      RINT
*
```

```
*
*  Initialization
*
 .text
INIT    DINT                ;disable all interrupts
        RSXM                ;reset sign-extension
        LDPK  0             ;data page = 0
        LAC   IMR           ;load ACC with contents IMR register
        ANDK  0fff0h        ;set bits 0, 1, 2 and 3 to 0
        ORK   010h          ;set bit 4 to 1
        SACL  IMR           ;store ACC to IMR register
        LALK  3600
        SACL  FAS360        ;FAS360 := 3600
        SFR
        SACL  FAS180        ;FAS180 := 1800
        LALK  12342
        SACL  SPAN1         ;offset for D/A converter for amplitude
        LALK  1000
        SACL  SPAN2         ;offset for D/A converter for phase
        LARK  AR2,0         ;clear contents of auxiliary register 2
        LARP  AR0           ;AR0 is default register
        FORT  0             ;initialize 16-bits serial channel
        SFSM                ;frame-sync. pulses needed
        SPM   0             ;no shift after multiplication
*
* Initialize the stack pointer
*
        LALK  1024          ;place stack pointer at end page 7
        SACL  HELP2
        LAR   AR7,HELP2
*
* Initialize variables BRANCH, MULTI, MULTQ, DATAVA
*
        LACK  0             ;clear BRANCH, MULTI, MULTQ, DATAVA
        SACL  BRANCH
        SACL  MULTI
        SACL  MULTQ
        SACL  DATAVA
*
*****************************************************************
*  Initialize position of delay lines                           *
*                                                               *
*  In DELx the last address of the concerning                   *
*  delay lins is placed. This address contains the              *
*  old samples.                                                 *
*                                                               *
*  DEL1B contains the begin address of the 1th delay line       *
*                                                               *
*  This routine is executed 2 times. One time for the I-branch *
*  and one time for the Q-branch                                *
*****************************************************************
*
        LDPK    4             ;Initialize variables for I-branch
        LALK    4*128+BASE    ;DEL* contains positions delay lines
        CALL    DELINI        ;TEL* contains counters
        CALL    CNTSET        ;set counters CNT1 to CNT12
        LACK    0             ;clear values in all delay lines (I)
        LARP    6
        LAR     AR6,DELPR
        RPTK    TOTLEN-1
```

```
        SACL    *-
        LDPK    6               ;initialize variables for Q-branch
        LALK    6*128+BASE
        CALL    DELINI
        CALL    CNTSET          ;set counters CNT1 to CNT12
        LACK    0               ;clear values in all delay lines (Q)
        LAR AR6,DELPR
        RPTK    TOTLEN-1
        SACL    *-
        LDPK    0               ;data page = 0
        LARP    AR0             ;set auxiliary register pointer to 0
        EINT
        B       MAINP           ;Initialization finished.
*
*  Subroutines for initialization
*
DELINI  SACL    DEL1B           ;in DELx last address of delay line x
        ADDK    LFIL1-1
        SACL    DEL1
        ADDK    LFIL2
        SACL    DEL2
        ADDK    LFIL3
        SACL    DEL3
        ADDK    LFIL4
        SACL    DEL4
        ADDK    LFIL5
        SACL    DEL5
        ADDK    LFIL6
        SACL    DEL6
        ADDK    LFIL7
        SACL    DEL7
        ADDK    LFIL8
        SACL    DEL8
        ADDK    LFIL9
        SACL    DEL9
        ADDK    LFIL10
        SACL    DEL10
        ADDK    LFIL11
        SACL    DEL11
        ADDK    LFIL12
        SACL    DEL12
        ADDK    LPRFIL
        SACL    DELPR
        RET
CNTSET  LACK    1               ;set CNT1 to 1; set CNTx, x>1, to 2
        SACL    CNT1
        LACK    2
        SACL    CNT2
        SACL    CNT3
        SACL    CNT4
        SACL    CNT5
        SACL    CNT6
        SACL    CNT7
        SACL    CNT8
        SACL    CNT9
        SACL    CNT10
        SACL    CNT11
        SACL    CNT12
        RET
*
```

```
*
*  Main program
*
MAINP   CALL  WAIT        ;wait until enough samples are taken
        CALL  AMPL        ;calculate log of amplitude
        CALL  FASE        ;calculate phase
        CALL  SCALE       ;scale AMPRES and FASRES for D/A conv.
        B     MAINP       ;return to MAINP
*
*
*  Wait loop
*
WAIT    LAC   DATAVA      ;data already valid ?
        SUBK  2           ;no, wait!
        BLZ   WAIT        ;yes,
        DINT              ;disable interrupts
        ZAC               ;set DATAVA to 0
        SACL  DATAVA      ;
        EINT              ;enable interrupts
        RET               ;return to main program MAINP
*
*  Calculate amplitude
*
AMPL    ZAC               ;set accumulator to 0
        MPYK  0           ;set P-register to 0
        SQRA  I           ;square I, P-register := I^2
        SQRA  Q           ;square Q, P-register := Q^2, acc := I^2
        MPYA  DUMMY       ;ACC := I^2 + Q^2
        CALL  LOG         ;calculate logarithm
        SACL  AMPRES      ;store result in AMPRES
        RET               ;return to main program MAINP
*
*
*  Calculate phase
*
FASE    LALK  900         ;ACC := 900
        SACL  OFFSET      ;set OFFSET to 90 degrees
        ZAC               ;ACC := 0
        MPYK  0           ;P-register := 0
        SQRA  I           ;square I, P-register := I^2
        SQRA  Q           ;square Q, P-register := Q^2, acc := I^2
        SQRS  Q           ;ACC := I^2-Q^2, P-register := Q^2
        BGZ   FASE1       ;if I > Q, jump to FASE1
        LACK  0
        SACL  OFFSET      ;set OFFSET to 0 degrees
        SQRA  I           ;square I, P-register := I^2
FASE1   PAC               ;load accumulator with P-register
        CALL  LOG         ;calculate logarithm
        SUB   AMPRES      ;subtract log(I^2 + Q^2)
        ABS               ;make positive
        CALL  COS         ;calculate cos
        SUB   OFFSET      ;subtract OFFSET
        ABS               ;determine quadrant of the phase
        BIT   Q,0         ;test sign bit of Q
        BBZ   FASE3       ;if Q positive, jump to FASE3
        BIT   I,0         ;test sign bit of I
        BBNZ  FASE2       ;if I negative, jump to FASE2
        SACL  FASRES      ;quadrant is 1, store phase
        RET               ;return to main program MAINP
FASE2   LDPK  4           ;data page = 4
```

```
        SUB    FAS180       ;quadrant is 2, subtract 180 degrees
        ABS                 ;make positive
        LDPK   0            ;data page = 0
        SACL   FASRES       ;store phase
        RET                 ;return to main program MAINP
FASE3   BIT    I,0          ;quadrant is 3 or 4
        BBZ    FASE4        ;if I positive, jump to FASE4
        ADLK   1800         ;quadrant is 3, add 180 degrees
        SACL   FASRES       ;store phase
        RET                 ;return to main program MAINP
FASE4   LDPK   4            ;data page = 4
        SUB    FAS360       ;quadrant is 4, subtract 360 degrees
        ABS                 ;make positive
        LDPK   0            ;data page = 0
        SACL   FASRES       ;store phase
        RET                 ;return to main program MAINP
*
*   Scaling routine
*   Scale AMPRES and FASRES for optimum use of the D/A converters.
*   the data is sent to the DA conv. at the end of the waiting
*   routine. In this manner the transmission of data is triggered
*   with the sample clock.
*
SCALE   SOVM                ;set overflow mode
        SSXM                ;set sign-extension
        LAC    AMPRES,15    ;place AMPRES in high part of ACC (ACCH)
        SFL
        SFL                 ;scale with factor 2
        LDPK   4            ;data page = 4
        SUBH   SPAN1        ;subtract offset
        SACH   DAAMP        ;store ACCH in DAAMP
        RPTK   4            ;ACCH := ACCH x 6
        ADDH   DAAMP
        SFR                 ;scale result to 14-bit number
        SFR                 ;for D/A converter
        SACH   DAAMP        ;store ACCH in DAAMP
        ROVM                ;reset overflow mode
        SPM    3            ;shift of output p register is set to 6
        LDPK   0            ;data page = 0
        LAC    FASRES       ;load ACC with FASRES (phase)
        LDPK   4            ;data page = 4
        SUB    SPAN2        ;subtract 100 degrees of phase
        SACL   DAFASE       ;store result in DAFASE
        ZAC                 ;ACC := 0
        LT     DAFASE       ;multiply T-register with 349
        MPYK   349
        APAC                ;load ACC with result and divide by 64x2
        SFR
        SACL   DAFASE       ;store result in DAFASE
        LDPK   0            ;data page = 0
        SPM    0            ;reset P-register output shift mode
        RSXM                ;reset sign-extension mode
        RET                 ;return to main program MAINP
*
*
*   Subroutines.
*
*
*   Log routine (used by AMPLITUDE)
*
```

```
*   The logarithm is calculated of the 32-bit number in ACC
                                   m-1
*   32-bit number = 2^m.(1 + SUM  b .2^(n-m)) = base x correction
                                   n=0 n
*   log(32-bit number) = log(base) + log(correction)
*   m is highest " 1 " bit. Only 9 of the 32 bits are used.
*   The auxiliary register AR1 is used.
*   The result is stored in the variable LOGRES.
*
LOG     LARK   AR1,31      ;initialize counter
        LARP   1           ;auxiliary register AR1 is active
LOG1    SFL                ;shift MSB in carry bit
        BC     LOG2        ;if carry = 1 then highest '1'-bit found
        BANZ   LOG1        ;decrease counter, if counter <> 0 cont.
        BNZ    LOG2        ;if ACC <> 0 correction must be found
        SACL   LOGRES      ;else log = 0, store result
        RET                ;return to AMPL or FASE
LOG2    RPTK   8           ;repeat next instruction 8 + 1 times
        ROL                ;rotate ACC left
        ANDK   0ffh        ;mask index: bit 0-7
        ADLK   LOGCOR      ;add start address of cor. table to index
        TBLR   LOGRES      ;copy correction to result LOGRES
        SAR    AR1,HELP1   ;copy counter (index) via variable to ACC
        ZALS   HELP1
        ADLK   LOGBAS      ;add start address of base table to index
        TBLR   HELP1       ;copy base to variable
        ZALS   HELP1       ;add base and correction
        ADDS   LOGRES
        SACL   LOGRES      ;store result in LOGRES
        RET                ;return to AMPL or FASE
*
*
*   Cosinus-routine (used by FASE).
*
*   Angle between the I-Q-vector and the I- or Q-axis is determined.
*
*   cosα = |Q|/(A)   or   -log(cosα) = log(A) - log(|Q|)
*
COS     ABS
        LDPK   4           ;data page = 4
        SACL   COSH1       ;store in COSH1
        LALK   256         ;initialize INDEX to 25.6 degrees
        SACL   INDEX
        LALK   128         ;initialize STEP to 12.8 degrees
COS1    SACL   STEP
        ZALS   INDEX       ;load ACC with INDEX
        ADLK   COSTAB      ;add start address table
        TBLR   COSH2       ;read value out table
        ZALS   COSH2       ;copy to ACC
        SUB    COSH1       ;compare with wanted phase
        BLZ    COS3        ;if wanted phase > read phase, go to COS3
        ZALS   INDEX       ;phase smaller, decrease INDEX with STEP
        SUB    STEP
COS2    SACL   INDEX       ;store new INDEX
        ZALS   STEP        ;divide STEP by 2
        SFR
        BGZ    COS1        ;INDEX > 0 try further
        ZALS   INDEX       ;ready: load ACC with result
        ADLK   450         ;add 45 degrees
        LDPK   0           ;data page = 0
```

```
        RET                  ;return to FASE
COS3    ZALS   INDEX         ;phase larger, add INDEX with STEP
        ADD    STEP
        B      COS2          ;jump to COS2
*
*  Interrupt handler.
*
*
****************************************************************
*                                                              *
*                          INTERRUPT                           *
*                     new sample arrived                       *
*                                                              *
****************************************************************
*
RINT    DINT                 ;disable interrupts
        CALL   SAVE          ;save ST0, ST1, P, T, ACC registers
IINIT   SSXM                 ;set sign-extension mode
        SPM    1             ;set output shift mode P register to 1
        SOVM                 ;set overflow mode
        LDPK   0             ;data page = 0
SCA16   LAC    DRR           ;read sample from receive register DRR
        RPTK   3             ;scale to a 16-bit two's
        SFL                  ;complement number
        SACL   SAMPLE
        BIT    SAMPLE,0
        BBZ    SREADY
        ORK    0Fh
        SACL   SAMPLE
SREADY  LARP   6             ;this aux. register is used by FILTER
        LDPK   4             ;shift values in delay line pre filter
        CALL   SHIFT         ;of I-branch
        LDPK   6             ;shift values in delay line pre filter
        CALL   SHIFT         ;of Q-branch
        LDPK   0             ;data page = 0
*
*  DEMODULATION
*
IQSEL   LAC    BRANCH        ;select which branch must be processed
        XORK   1
        SACL   BRANCH
        BZ     QBRANCH
*
*  demodulate I-branch
*
IBRANCH LACK   0             ;place 0 in Q-branch
        LDPK   6
        LAR    AR6,DEL12
        MAR    *+
        SACL   *
        LDPK   0
        LAC    MULTI         ;Multiply sample by +1 of -1 ?
        XORK   1
        SACL   MULTI
        BZ     MIN1I
PLUS1I  LAC    SAMPLE        ;multiply by +1
        B      FILI
MIN1I   LACK   0             ;multiply by -1
        SUB    SAMPLE
```

```
*
*  filtering in  I-branch
*
FILI    LARK  AR5,I        ;output filter must to variable I
        LDPK  4            ;value in ACC, set data page
        CALL  PREFIL       ;pre filter
        CALL  FILTER       ;call filter
        B     RESTOR       ;restore registers, return from interrupt
*
*  demodulate Q-branch
*
QBRANCH LACK  0            ;place 0 in I-branch
        LDPK  4
        LAR   AR6,DEL12
        MAR   *+
        SACL  *
        LDPK  0
        LAC   MULTQ        ;multiply sample by +1 of -1 ?
        XORK  1
        SACL  MULTQ
        BZ    MIN1Q
PLUS1Q  LAC   SAMPLE       ;multiply by +1
        B     FILQ
MIN1Q   LACK  0            ;multiply by -1
        SUB   SAMPLE
*
*  filtering Q-branch
*
FILQ    LARK  AR5,Q        ;output filter must to variable Q
        LDPK  6            ;value in ACC, set data page
        CALL  PREFIL       ;pre filter
        CALL  FILTER       ;call filter
        B     RESTOR       ;restore registers, return from interrupt
*
*  Shift delays of pre filter
*
SHIFT   LAR   AR6,DELPR
        MAR   *-
        RPTK  LPRFIL-2
        DMOV  *-
        RET
*
*  Filter program pre filter
*
        LAR   AR6,DEL12    ;place value on right place in delay line
        MAR   *+
        SACL  *
        ZAC
        MPYK  0
        LAR   AR6,DELPR
        RPTK  LPRFIL-1
        MAC   CPRFIL,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        RET
```

```
*****************************************************************
*                                                               *
*                               FILTER                          *
*                                                               *
*****************************************************************
* assumptions: -New value for the first filter is in ACCL       *
*               data page 4 for I-branch                        *
*               data page 6 for Q-branch                        *
*              -auxiliary register pointer is at AR6            *
*                    -AR5 contains position for the result      *
*                                                               *
*                                                               *
* REMARKS     : ACC, AR6, T and P are changed by this routine   *
*                                                               *
*****************************************************************
*
FILTER
*
*  shift delay line 1
*
        LAR    AR6,DEL1    ;shift values in delay line filter 1
        MAR    *-          ;thus a new sample can be placed
        RPTK   LFIL1-2     ;
        DMOV   *-          ;
        LAR    AR6,DEL1B   ;place new sample in 1th delay line
        SACH   *           ;jump to right branch of the algorithm
        LAC    CNT1
        BZ     SECT1
        SUBK   1           ;CNT1:=CNT1-1
        SACL   CNT1
        LAC    CNT2
        BZ     SECT2
        LAC    CNT3
        BZ     SECT3
        LAC    CNT4
        BZ     SECT4
        LAC    CNT5
        BZ     SECT5
        LAC    CNT6
        BZ     SECT6
        LAC    CNT7
        BZ     SECT7
        LAC    CNT8
        BZ     SECT8
        LAC    CNT9
        BZ     SECT9
        LAC    CNT10
        BZ     SECT10
        LAC    CNT11
        BZ     SECT11
        LAC    CNT12
        BZ     SECT12
        RET
*
*****************************************************************
*  Sections in filter algorithm                                 *
*                                                               *
*****************************************************************
*
```

```
*  Section 1
*
SECT1    LACK   1           ;CNT1:=1
         SACL   CNT1        ;
SDEL2    LAR    AR6,DEL2    ;Shift delay line 2
         MAR    *-          ;modify current auxiliary register
         RPTK   LFIL2-2     ;
         DMOV   *-          ;
FIL1     ZAC                ;ACC := 0
         MPYK   0           ;set P-register to 0
         LAR    AR6,DEL1    ;place in AR6 last address of delay line 1
         RPTK   LFIL1-1     ;multiply the coefficients in the program
         MAC    CFIL1,*-    ;memory with the values in the delay line
         APAC               ;add the values
         RSXM               ;round number in ACC
         ADLK   32768       ;
         SSXM               ;
         LAR    AR6,DEL1    ;store calc. value in the first position
         MAR    *+          ;of delay line 2
         SACH   *           ;
         LAC    CNT2        ;CNT2:=CNT2-1
         SUBK   1           ;
         SACL   CNT2        ;
         RET                ;return to main program MAINP
*
*  Section 2
*
SECT2    LACK   2
         SACL   CNT2
SDEL3    LAR    AR6,DEL3
         MAR    *-
         RPTK   LFIL3-2
         DMOV   *-
FIL2     ZAC
         MPYK   0
         LAR    AR6,DEL2
         RPTK   LFIL2-1
         MAC    CFIL2,*-
         APAC
         RSXM
         ADLK   32768
         SSXM
         LAR    AR6,DEL2
         MAR    *+
         SACH   *
         LAC    CNT3
         SUBK   1
         SACL   CNT3
         RET
*
*  Section 3
*
SECT3    LACK   2
         SACL   CNT3
SDEL4    LAR    AR6,DEL4
         MAR    *-
         RPTK   LFIL4-2
         DMOV   *-
FIL3     ZAC
         MPYK   0
```

```
        LAR   AR6,DEL3
        RPTK  LFIL3-1
        MAC   CFIL3,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        LAR   AR6,DEL3
        MAR   *+
        SACH  *
        LAC   CNT4
        SUBK  1
        SACL  CNT4
        RET
*
*  Section 4
*
SECT4   LACK  2
        SACL  CNT4
SDEL5   LAR   AR6,DEL5
        MAR   *-
        RPTK  LFIL5-2
        DMOV  *-
FIL4    ZAC
        MPYK  0
        LAR   AR6,DEL4
        RPTK  LFIL4-1
        MAC   CFIL4,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        LAR   AR6,DEL4
        MAR   *+
        SACH  *
        LAC   CNT5
        SUBK  1
        SACL  CNT5
        RET
*
*  Section 5
*
SECT5   LACK  2
        SACL  CNT5
SDEL6   LAR   AR6,DEL6
        MAR   *-
        RPTK  LFIL6-2
        DMOV  *-
FIL5    ZAC
        MPYK  0
        LAR   AR6,DEL5
        RPTK  LFIL5-1
        MAC   CFIL5,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        LAR   AR6,DEL5
        MAR   *+
        SACH  *
```

```
         LAC    CNT6
         SUBK   1
         SACL   CNT6
         RET
*
* Section 6
*
SECT6    LACK   2
         SACL   CNT6
SDEL7    LAR    AR6,DEL7
         MAR    *-
         RPTK   LFIL7-2
         DMOV   *-
FIL6     ZAC
         MPYK   0
         LAR    AR6,DEL6
         RPTK   LFIL6-1
         MAC    CFIL6,*-
         APAC
         RSXM
         ADLK   32768
         SSXM
         LAR    AR6,DEL6
         MAR    *+
         SACH   *
         LAC    CNT7
         SUBK   1
         SACL   CNT7
         RET
*
*  Section 7
*
SECT7    LACK   2
         SACL   CNT7
SDEL8    LAR    AR6,DEL8
         MAR    *-
         RPTK   LFIL8-2
         DMOV   *-
FIL7     ZAC
         MPYK   0
         LAR    AR6,DEL7
         RPTK   LFIL7-1
         MAC    CFIL7,*-
         APAC
         RSXM
         ADLK   32768
         SSXM
         LAR    AR6,DEL7
         MAR    *+
         SACH   *
         LAC    CNT8
         SUBK   1
         SACL   CNT8
         RET
*
*  Section 8
*
SECT8    LACK   2
         SACL   CNT8
SDEL9    LAR    AR6,DEL9
```

```
        MAR     *-
        RPTK    LFIL9-2
        DMOV    *-
FIL8    ZAC
        MPYK    0
        LAR     AR6,DEL8
        RPTK    LFIL8-1
        MAC     CFIL8,*-
        APAC
        RSXM
        ADLK    32768
        SSXM
        LAR     AR6,DEL8
        MAR     *+
        SACH    *
        LAC     CNT9
        SUBK    1
        SACL    CNT9
        RET
*
*  Section 9
*
SECT9   LACK    2
        SACL    CNT9
SDEL10  LAR     AR6,DEL10
        MAR     *-
        RPTK    LFIL10-2
        DMOV    *-
FIL9    ZAC
        MPYK    0
        LAR     AR6,DEL9
        RPTK    LFIL9-1
        MAC     CFIL9,*-
        APAC
        RSXM
        ADLK    32768
        SSXM
        LAR     AR6,DEL9
        MAR     *+
        SACH    *
        LAC     CNT10
        SUBK    1
        SACL    CNT10
        RET
*
*  Section 10
*
SECT10  LACK    2
        SACL    CNT10
SDEL11  LAR     AR6,DEL11
        MAR     *-
        RPTK    LFIL11-2
        DMOV    *-
FIL10   ZAC
        MPYK    0
        LAR     AR6,DEL10
        RPTK    LFIL10-1
        MAC     CFIL10,*-
        APAC
        RSXM
```

```
        ADLK  32768
        SSXM
        LAR   AR6,DEL10
        MAR   *+
        SACH  *
        LAC   CNT11
        SUBK  1
        SACL  CNT11
        RET
*
*  Section 11
*
SECT11  LACK  2
        SACL  CNT11
SDEL12  LAR   AR6,DEL12
        MAR   *-
        RPTK  LFIL12-2
        DMOV  *-
FIL11   ZAC
        MPYK  0
        LAR   AR6,DEL11
        RPTK  LFIL11-1
        MAC   CFIL11,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        LAR   AR6,DEL11
        MAR   *+
        SACH  *
        LAC   CNT12
        SUBK  1
        SACL  CNT12
        RET
*
*  Section 12
*
SECT12  LACK  2
        SACL  CNT12
FIL12   ZAC
        MPYK  0
        LAR   AR6,DEL12
        RPTK  LFIL12-1
        MAC   CFIL12,*-
        APAC
        RSXM
        ADLK  32768
        SSXM
        LARP  AR5          ;place result of filter in address of AR5
        SACH  *            ;I or Q variable at pagina 0
        LDPK  0
        LAC   DATAVA       ;if DATAVA is 2 then the
        ADDK  1            ;WAIT routine knows I en Q  are valid
        SACL  DATAVA       ;
        OUT   DAAMP,1      ;send log of amplitude to D/A converter
        OUT   DAFASE,2     ;send phase to D/A converter
                           ;output is sync. with sample clock
        RET
```

```
*****************************************************************
*                                                               *
*                         SAVE CONTEXT                          *
*                                                               *
*                                                               *
*                                                               *
*****************************************************************
*                                                               *
* Assumptions: AR7 is used as stack pointer                     *
*                                                               *
* The 8 levels of the hardware stack are not saved              *
*                                                               *
*****************************************************************
SAVE    LARP  AR7
        MAR   *-
*  save status registers
        SST1  *-          ;ST1  -> (1023)
        SST   *-          ;ST0  -> (1022)
*  save the accumulator
        SACH  *-          ;ACCH -> (1021)
        SACL  *-          ;ACCL -> (1020)
*  save the P register
        SPM   0           ;no shift in PR output
        SPH   *-          ;PRH  -> (1019)
        SPL   *-          ;PRL  -> (1018)
*  save the T register
        MPYK  1           ;PR = TR
        SPL   *-          ;TR ->   (1017)   AR7=1016
*  save complete
        RET
*
*****************************************************************
*                                                               *
*                                 RESTORE                       *
*                                                               *
*                                                               *
*****************************************************************
*                                                               *
*    This  routine  returns  what  is  saved  by  SAVE,         *
*  enables interrupts and returns to the program                *
*                                                               *
*****************************************************************
*
RESTOR  LARP  AR7
        MAR   *+
*  restore the low P register
        MAR   *+          ;skip T register
        LT    *-          ;(1018) -> TR
        MPYK  1           ;(TR)  -> PRL
*  restore the T register
        LT    *+          ;(1017) -> TR
        MAR   *+          ;skip P register low
*  restore the high P register
        LPH   *+          ;(1019) -> PRH
*  restore the accumulator
        ZALS  *+          ;(1020) -> ACCL
        ADDH  *+          ;(1021) -> ACCH
*  restore the status registers
        LST   *+          ;(1022) -> ST0
        LST1  *+          ;(1023) -> ST1      AR7=1024
```

```
*
* restore complete
*
       EINT
 RET
*
*  Table with log (2^x), 0 <= x <= 31 Base
*
LOGBAS: .word 0,301,602,903,1204,1505,1806,2107,2408,2709
        .word 3010,3311,3612,3913,4214,4515,4816,5118,5419,5720
        .word 6021,6322,6623,6924,7225,7526,7827,8128,8429,8730
        .word 9031,9332
*
*  Correction for logarithm
*
LOGCOR: .word 0,2,3,5,7,8,10,12,13,15
        .word 17,18,20,22,23,25,26,28,30,31
        .word 33,34,36,37,39,40,42,44,45,47
        .word 48,50,51,53,54,56,57,59,60,62
        .word 63,65,66,67,69,70,72,73,75,76
        .word 77,79,80,82,83,85,86,87,89,90
        .word 91,93,94,96,97,98,100,101,102,104
        .word 105,106,108,109,110,112,113,114,116,117
        .word 118,119,121,122,123,125,126,127,128,130
        .word 131,132,133,135,136,137,138,140,141,142
        .word 143,144,146,147,148,149,150,152,153,154
        .word 155,156,158,159,160,161,162,163,165,166
        .word 167,168,169,170,172,173,174,175,176,177
        .word 178,179,181,182,183,184,185,186,187,188
        .word 189,191,192,193,194,195,196,197,198,199
        .word 200,201,202,203,205,206,207,208,209,210
        .word 211,212,213,214,215,216,217,218,219,220
        .word 221,222,223,224,225,226,227,228,229,230
        .word 231,232,233,234,235,236,237,238,239,240
        .word 241,242,243,244,245,246,247,248,249,250
        .word 251,252,253,254,255,255,256,257,258,259
        .word 260,261,262,263,264,265,266,267,268,268
        .word 269,270,271,272,273,274,275,276,277,278
        .word 278,279,280,281,282,283,284,285,285,286
        .word 287,288,289,290,291,292,292,293,294,295
        .word 296,297,298,298,299,300
*
*  Table for cosinus routine
*
COSTAB: .word  301,303,304,306,307,309,310,312,313,315
        .word  316,318,320,321,323,324,326,328,329,331
        .word  332,334,336,337,339,341,342,344,346,347
        .word  349,351,352,354,356,357,359,361,363,364
        .word  366,368,370,371,373,375,377,378,380,382
        .word  384,386,387,389,391,393,395,397,399,400
        .word  402,404,406,408,410,412,414,416,417,419
        .word  421,423,425,427,429,431,433,435,437,439
        .word  441,443,445,447,449,451,453,455,457,459
        .word  462,464,466,468,470,472,474,476,479,481
        .word  483,485,487,489,492,494,496,498,500,503
        .word  505,507,509,512,514,516,519,521,523,525
        .word  528,530,532,535,537,540,542,544,547,549
        .word  552,554,556,559,561,564,566,569,571,574
        .word  576,579,581,584,586,589,592,594,597,599
        .word  602,605,607,610,613,615,618,621,623,626
```

```
        .word  629,632,634,637,640,643,645,648,651,654
        .word  657,660,663,665,668,671,674,677,680,683
        .word  686,689,692,695,698,701,704,707,710,713
        .word  716,719,723,726,729,732,735,738,742,745
        .word  748,751,755,758,761,765,768,771,775,778
        .word  781,785,788,792,795,799,802,806,809,813
        .word  816,820,823,827,831,834,838,842,845,849
        .word  853,857,860,864,868,872,876,880,883,887
        .word  891,895,899,903,907,911,915,920,924,928
        .word  932,936,940,944,949,953,957,962,966,970
        .word  975,979,984,988,993,997,1002,1006,1011,1015
        .word  1020,1025,1029,1034,1039,1044,1049,1053,1058,1063
        .word  1068,1073,1078,1083,1088,1093,1098,1104,1109,1114
        .word  1119,1125,1130,1135,1141,1146,1152,1157,1163,1168
        .word  1174,1180,1185,1191,1197,1203,1209,1215,1221,1227
        .word  1233,1239,1245,1251,1257,1264,1270,1276,1283,1289
        .word  1296,1302,1309,1316,1323,1329,1336,1343,1350,1357
        .word  1364,1371,1379,1386,1393,1401,1408,1416,1423,1431
        .word  1439,1447,1455,1463,1471,1479,1487,1495,1504,1512
        .word  1521,1529,1538,1547,1556,1565,1574,1583,1592,1602
        .word  1611,1621,1631,1641,1651,1661,1671,1681,1692,1702
        .word  1713,1724,1735,1746,1757,1769,1780,1792,1804,1816
        .word  1828,1841,1853,1866,1879,1892,1906,1919,1933,1947
        .word  1962,1976,1991,2006,2021,2037,2053,2069,2085,2102
        .word  2119,2137,2155,2173,2192,2211,2230,2250,2271,2291
        .word  2313,2335,2357,2380,2404,2429,2454,2480,2506,2534
        .word  2562,2592,2622,2654,2687,2721,2756,2793,2832,2872
        .word  2914,2959,3006,3055,3108,3164,3224,3288,3358,3434
        .word  3516,3608,3710,3826,3960,4118,4312,4562,4914,5516
.word  18999,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32767,32767,32767,32767,32767,32767,32767,32767
.word  32767,32767,32677
*
****************************************************************
*                Coefficients of the filters                   *
****************************************************************
*
CFIL1:   .word 6,0,-815,0,8998,16384,8998,0,-815,0,6
CFIL2:   .word 6,0,-816,0,8999,16384,8999,0,-816,0,6
CFIL3:   .word 6,0,-817,0,9000,16384,9000,0,-817,0,6
CFIL4:   .word 6,0,-820,0,9003,16384,9003,0,-820,0,6
CFIL5:   .word 6,0,-825,0,9009,16384,9009,0,-825,0,6
CFIL6:   .word 6,0,-835,0,9020,16384,9020,0,-835,0,6
CFIL7:   .word 7,0,-856,0,9043,16384,9043,0,-856,0,7
CFIL8:   .word 9,0,-900,0,9088,16384,9088,0,-900,0,9
CFIL9:   .word 14,0,-994,0,9180,16384,9180,0,-994,0,14
CFIL10:  .word 0,123,0,-1459,0,9521,16384,9521,0,-1459,0,123,0
CFIL11:  .word 0,-88,0,603,0,-2293,0,9972,16384,9972,0,-2293,0,603,
CFIL12:  .word 14,-8,-24,-20,12,43,28,-35,-78,-35
         .word 73,125,32,-136,-184,-11,231,252,-41,-370
         .word -326,143,568,400,-326,-861,-467,663,1343,520
         .word -1392,-2412,-555,4175,9285
         .word 11490
         .word 9285,4175,-555,-2412,-1392
         .word 520,1343,663,-467,-861,-326,400,568,143,-326
         .word -370,-41,252,231,-11,-184,-136,32,125,73
```

```
        .word -35,-78,-35,28,43,12,-20,-24,-8,14
CPRFIL: .word 28,-62,-364,-857,-1179,-651,1373,4975,9341,12964
        .word 14375
        .word 12964,9341,4975,1373,-651,-1179,-857,-364,-62,28
*
*  End program
*
        .end
```

Appendix G: Measurement results

Table G.1: Amplitude measurement results of EUT detectors (both versions show same results)

P_{in} (dBm)	V_{out} (V)	P_{in} (dBm)	V_{out} (V)
18	2.95	-10	-0.12
16	2.74	-12	-0.34
14	2.52	-14	-0.56
12	2.30	-16	-0.78
10	2.08	-18	-1.01
8	1.86	-20	-1.23
6	1.64	-22	-1.44
4	1.42	-24	-1.66
2	1.20	-26	-1.88
0	0.98	-28	-2.11
-2	0.76	-30	-2.33
-4	0.54	-32	-2.54
-6	0.32	-34	-2.76
-8	0.10	-36	-2.98

Table G.2: Amplitude measurements with PLL receiver,
measured at linear and logarithmic output port.

P_{in}(dBm)	$V_{out,lin}$(V)	$V_{out,log}$(V)
-0.0	6.60	7.10
-2.5	5.21	6.90
-5.0	3.85	6.63
-7.5	2.82	6.37
-10.0	2.05	6.09
-12.5	1.52	5.84
-15.0	1.13	5.60
-17.5	0.84	5.35
-20.0	0.62	5.11
-23.5	0.47	4.86
-25.0	0.35	4.64
-27.5	0.266	4.39
-30.0	0.198	4.15
-32.5	0.150	3.91
-35.0	0.114	3.68
-37.5	0.086	3.44
-40.0	0.065	3.20
-42.5	0.049	2.97
-45.0	0.037	2.74
-47.5	0.029	2.50
-50.0	0.021	2.26
-52.5	0.017	2.02
-55.0	0.013	1.77
-57.5	0.010	1.52
-60.0	0.008	1.25
-62.5	0.006	0.98
-65.0	0.005	0.68
-67.5	0.004	0.36
-70.0	0.003	0.05

Table G.3: Amplitude measurements with PLL receiver, using EUT detector for the amplitude detection.

P_{in}(dBm)	$V_{out,EUT}$(V)
-10.0	2.90
-12.5	2.60
-15.0	2.32
-17.5	2.04
-20.0	1.75
-23.5	1.46
-25.0	1.19
-27.5	0.91
-30.0	0.64
-32.5	0.36
-35.0	0.09
-37.5	-0.18
-40.0	-0.46
-42.5	-0.73
-45.0	-1.00
-47.5	-1.26
-50.0	-1.53
-52.5	-1.80
-55.0	-2.06
-57.5	-2.32
-60.0	-2.57
-62.5	-2.82
-65.0	-3.00