Design of InP membrane SOA with butt-joint active passive interface

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A. Zozulia[1], V. Pogoretsky[1], P. J. van Veldhoven[1], J. Bolk[1], K. A. Williams[1], S. Rihani[2], G. Berry[2], M. Robertson[2], J. Rawsthorne[2] and Y. Jiao[1]

[1]Photonics Integration group, Eindhoven University of Technology, PO Box 513, 5600 MB Eindhoven, The Netherlands

[2]Huawei Technologies Research & Development (UK) Ltd, IP5 3RE Ipswich, UK

A butt-joint SOA design for InP on Si membrane (IMOS) platform is proposed. The new design features the butt-joint interface between the SOA and passive nanophotonic waveguide, which makes the interface a factor of 2 to 6 shorter than in the current twin-guide SOAs, with possibility to reduce it further to factor of 5-10. This makes the new SOA a promising candidate for high-speed directly modulated lasers (DML) applications, where extremely short SOAs (40-100 μm long) and short distances between reflectors are usually required.

Introduction

Indium Phosphide membrane on Silicon (IMOS) is a membrane platform for the fabrication of photonic integrated circuits (PICs), which combines membrane SOAs with ultra-compact high confinement nanophotonic waveguides [1]. This platform is promising to enable a high density of optical components and a smaller footprint of optical transceivers of the future. One of the potential bottlenecks for high-density integration on IMOS is the 50-μm-long 2-stage taper transition between the SOA building block of 1.5x2 μm in the cross-section and the passive waveguide of 0.3x0.4 μm in the cross-section [2]. Long active-passive interfaces can hinder the performance of lasers where an ultra-short cavity is desired, such as directly modulated lasers [3]. We propose a new SOA design, where a butt-joint regrowth of passive waveguides enables a 24-μm long interface, with the potential to reduce it to <10 μm.

Active-passive interface optimization

Integration of a high gain and low resistance SOA with a compact passive waveguide has always been a challenge for membrane photonics. In the previously developed twin-guide IMOS SOA, an InGaAsP optical waveguide containing 4 quantum wells (QW) is sandwiched between n- and p-doped InP contact layers [4]. The effective index of the fundamental optical mode inside the 2 μm wide SOA $n_{eff\ soa} = 3.23$. The doped layers are removed from the passive waveguide to reduce optical losses, and the waveguide dimensions are reduced to enable high optical confinement and therefore high density integration. In the 2 um wide passive InGaAsP waveguide $n_{eff\ pas} = 2.92$. The shortest active-passive interface can be achieved when an SOA is directly connected to a passive waveguide of the same width via butt-joint, but in this case Fresnel reflections, caused by effective index mismatch, will create an undesirable Fabry-Perot cavity inside the SOA. To match effective indexes, a taper is made at the top and bottom of the passive waveguide.

An SOA epitaxial layer stack was optimized for the butt-joint interface. Compared to previously specified twin-guide SOA, the separate confinement heterostructure (SCH) thickness was reduced from 500 nm to 300 nm. The p-InP contact layer thickness was

reduced from 800 nm to 600 nm. The n-contact thickness was increased from 80 nm to 200 nm. This helps to reduce diode resistance, enable more symmetric optical field distribution in the SOA, and more fabrication-tolerant surface gratings made on the n-contact side. 60 nm layers of non-intentionally doped (n.i.d.) InP was added at the top and bottom of the SCH to reduce optical losses of the mode from highly doped layers.

We optimized the interface between the updated SOA stack, which has dimensions of 1.3x2 μm^2, and passive waveguide, which has dimensions of 0.3x2 μm^2. The cross-sections are shown on Figure 1. A commercial eigenmode expansion solver (EME) is used for the simulation. The simulation setup is shown on Figure 2. The taper consists of 2 sections, which are optimized separately. The optimization parameters are section length and width of the waist between 2 sections. The taper tip width is set to 200 nm during the optimization, because this tip width is readily achievable from the fabrication point of view. The main figures of merit of the optimization are the fundamental mode power reflection and transmission coefficients ($|S11|^2$ and $|S21|^2$).

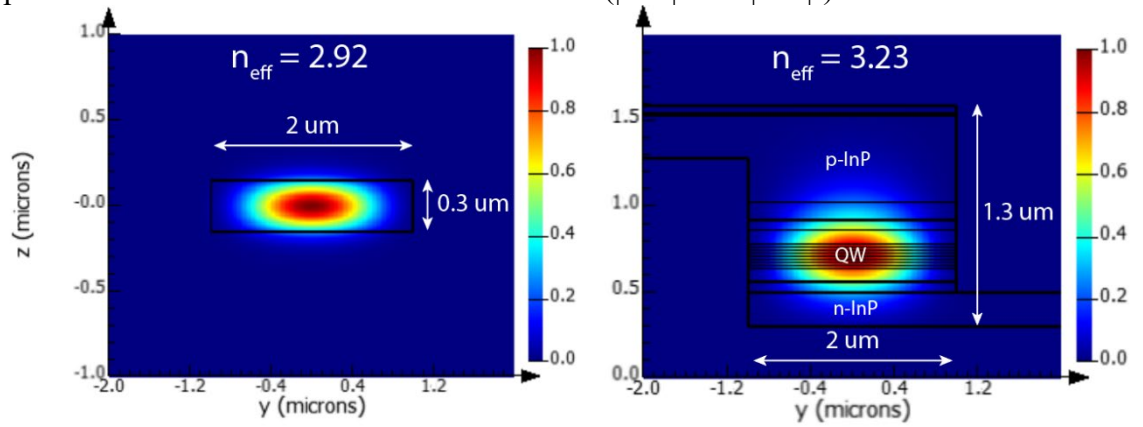

Figure 1. Left: Passive waveguide cross-section. Right: SOA building block cross-section

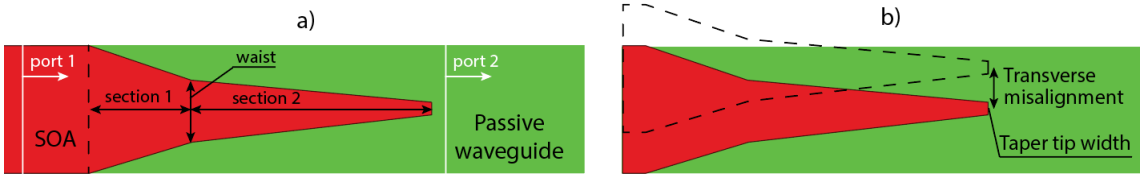

Figure 2. Schematic top view of the active-passive interface. a) Main simulation parameters. b) parameters of tolerance study

$|S21|^2$ is highly dependent on the lengths of taper sections, because for some values of the length the fundamental mode power gets converted to higher order modes at the output of the interface. By sweeping over the section length, we can identify maxima of the $|S21|^2$

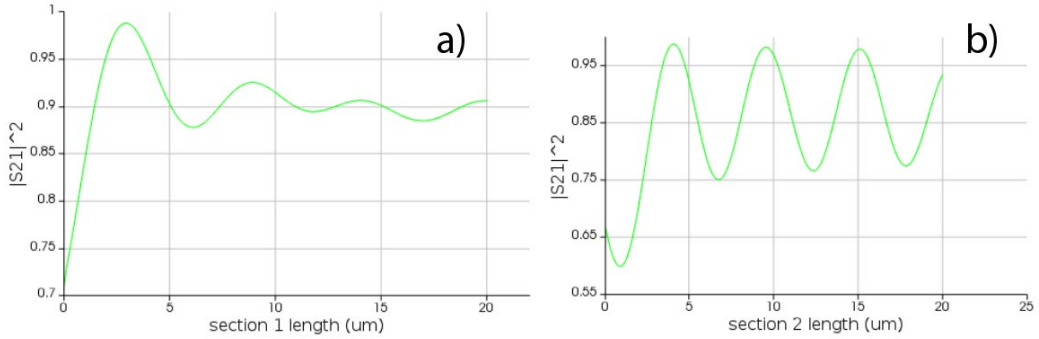

Figure 3. Interface transmission function vs a) section 1 length, b) section 2 length, when section 1 length is fixed at 3 um.

function (see Figure 3) and choose several structures with section lengths, corresponding to different maxima, to study their fabrication tolerances. We do it also for different waist widths and for taper tip widths of 200 and 300 nm.
After the optimization, 3 different designs with best performance are chosen to perform the tolerance study. The summary of parameters for selected designs is given in the Table 1. Taper 1 has a total length of 7.8 µm, the length of both sections corresponds to the first maxima of the $|S21|^2$ function. Taper 2 has a total length of 12 µm and the tip width of 0.3 µm, which is more relaxed in terms of fabrication. Taper 3 has a total length of 24.25 µm, and is a good compromise between length, performance and sensitivity to fabrication errors.

Table 1. Geometric parameters and simulated transmission and reflection of 3 selected taper designs

	Section 1, µm	Section 2, µm	Waist, µm	Tip, µm	$\|S21\|^2$	$\|S11\|^2$
Taper 1	3.5	4.3	0.7	0.2	0.989	3.7E-5
Taper 2	3.0	9.0	1.0	0.3	0.973	7.4E-5
Taper 3	9.25	15.0	0.7	0.2	0.976	3.3E-5

Figure 4 shows the change in taper performance due to deviations of the most important parameters: transverse misalignment and tip width. Taper 1 has the highest transmission in the optimal design point, however, it is less tolerant of misalignment error. A taper of 24.25 µm has the most relaxed fabrication tolerances. The reflections are -37 to -45 dB and the transmission into the fundamental mode is 94-97% in the tolerance range that we expect from the fabrication tools.

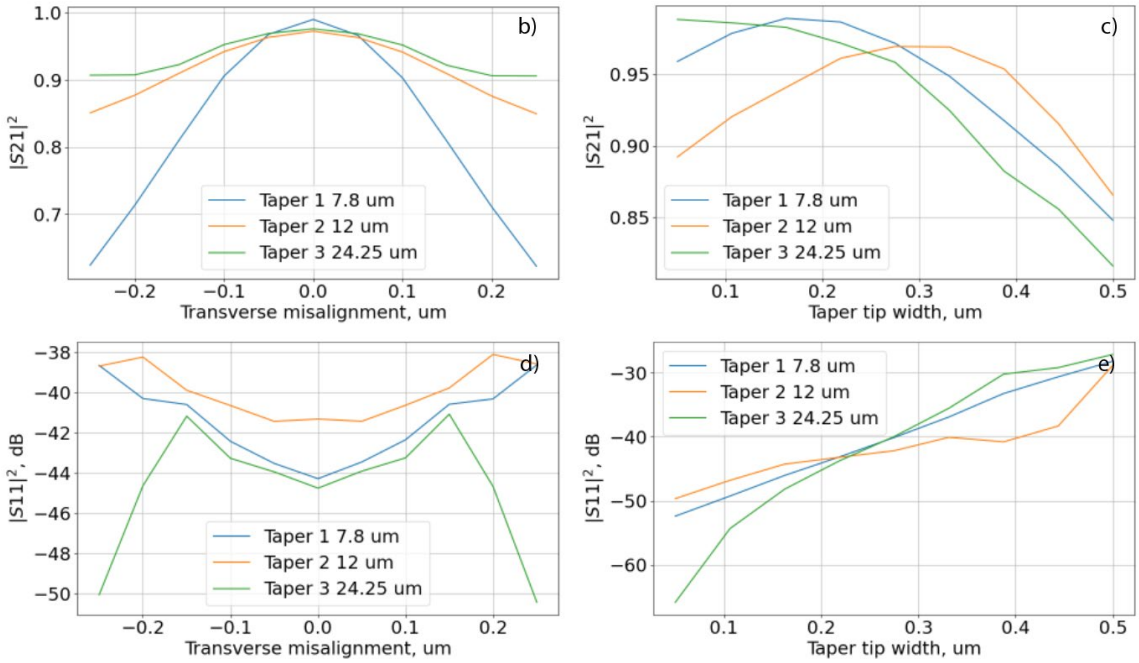

Figure 4. Tolerance comparison for 3 different taper designs. a) Tolerances in consideration. b), d): Transverse misalignment of the taper relative to the waveguide. c), e): change of the taper tip width

Experimental results

After the optimization, a taper tip width of 300 nm in the semiconductor was achieved.

This taper is expected to give < -37 dB of optical reflections. The optical performance of the taper can only be evaluated after the processing is completed. The IV curve of several fabricated diodes was measured. The series resistance of a 400 μm long diode is 2.4 Ω, for the contact area of 10800 μm^2. In previously demonstrated IMOS diodes the series resistance was 5-8 Ω for the contact area of 100000 μm^2 [4].

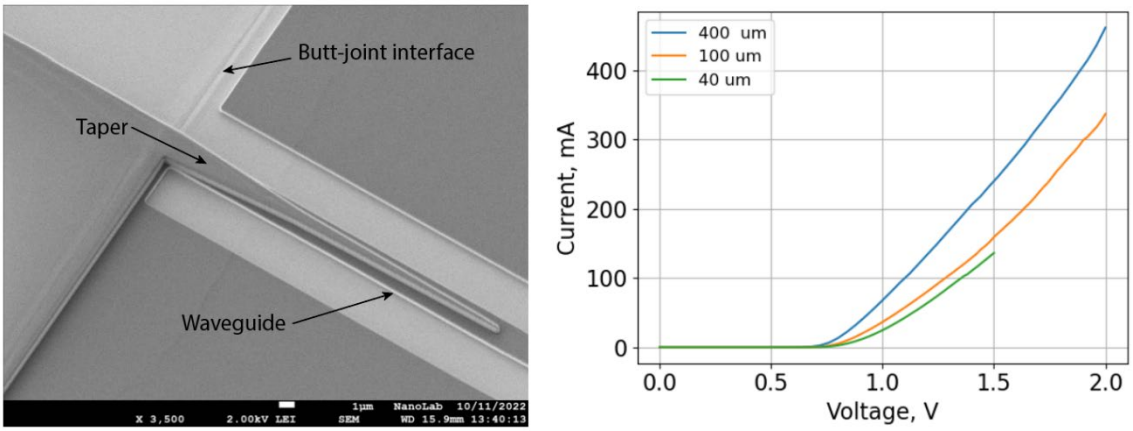

Figure 5. Left: Bird's eye view of the fabricated active-passive interface. Right: measured IV characteristics of diodes of different length.

Conclusion

A new design of a membrane SOA was proposed. The butt-joint regrowth allowed us to reduce the length of the active-passive interface to 24.25 μm with relaxed fabrication tolerances and to 7.8 μm with tight tolerances. The layer stack and the fabrication process flow were optimized to enable butt-joint regrowth and usage of optical lithography. The fabricated SOAs show good diode behavior with low series resistance.

Acknowledgements

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