Fast and Flexible, Arbitrary Waveform, 20-kV, Solid-State, Impedance-matched Marx Generator

Fast and Flexible, Arbitrary Waveform, 20-kV, Solid-State, Impedance-Matched Marx Generator

J. J. van Oorschot, *Graduate Student Member, IEEE* and T. Huiskamp, *Member, IEEE*

***Abstract*— We developed a new pulsed power supply to study the influence of the high-voltage (HV) pulse shape on the generation of plasma-activated water (PAW). This article shows the design and implementation of the generator and evaluates its performance on resistive loads. The design is an improved version of the solid-state impedance-matched Marx generator (SS-IMG) concept as previously developed at Eindhoven University of Technology. The IMG concept allows for sub-nanosecond rise time pulses, to be able to create a nonthermal plasma very efficiently. A conventional SS-Marx generator (SS-Marx) circuit is taken as the starting point, and a careful implementation is made with most electrical connections analyzed as transmission lines (TLs). All these TLs are impedance-matched to each other and the load. The implemented generator is able to generate 25 ns to μs duration pulses of 20 kV up to 10-kHz repetition rate in a 50-Ω load with about 8 ns rise time and arbitrary pulse shape. Future improvements are suggested which will increase the repetition rate and decrease the pulse rise time to the sub-nanosecond regime.**

***Index Terms*— High-voltage techniques, impedance-matched Marx generator (IMG), Marx generators, plasma generation, pulse power systems.**

I. Introduction

TRANSIENT plasmas generated by high-voltage pulses have been widely studied and used in industrial and environmental applications. Such applications include air purification, water purification, biological tissue sterilization, material surfaces modification, and many more [1], [2], [3], [4].

Another large area of research is plasma-activated water (PAW) generation, and this is the focus area for the pulsed power generator described in this work. PAW is water "activated," or treated, with plasma and can be used in various applications, such as disinfection, sterilization, and as fertilizer in agriculture [5], [6], [7]. PAW typically has a pH ranging from 2 to 4, and for each application, a different PAW composition may be optimal. This composition consists of mostly hydrogen peroxide, nitrates, nitrites, and peroxynitrite.

Manuscript received 31 October 2022; revised 8 December 2022; accepted 2 January 2023. Date of publication 18 January 2023; date of current version 24 February 2023. This work was supported by the Dutch Research Organisation Nederlandse Organisatie voor Wetenschappelijk Onderzoek (NWO) under Grant 17183. The review of this article was arranged by Senior Editor R. P. Joshi. *(Corresponding author: J. J. van Oorschot.)*

The authors are with the Electrical Energy Systems Group, Department of Electrical Engineering, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands (e-mail: j.j.v.oorschot@tue.nl; t.huiskamp@tue.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPS.2023.3235418.

Digital Object Identifier 10.1109/TPS.2023.3235418

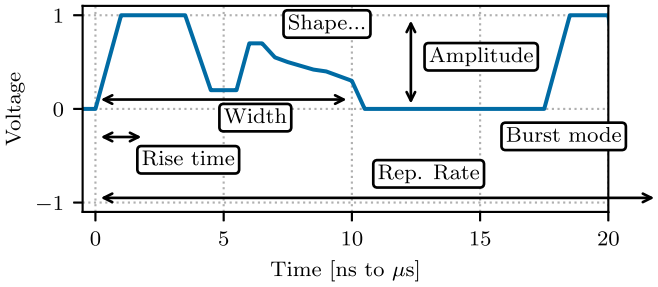

Fig. 1. Example flexible unipolar pulse shape, with many options for variations, such as pulse width, amplitude, rise time, pulse shape, repetition rate, and the possibility for burst-mode operation.

For fertilizer applications, nitrates are most important, while for disinfection hydrogen peroxide is key. PAW production is a sustainable technology, because only air, electricity, and water are used: there are no other chemicals added.

Plasma, or electrical discharges in general, can be generated from alternating voltage (AC) sources, such as radio frequency (RF), from direct current (DC), or from pulsed sources [8]. Research has shown that transient plasmas generated by short nanosecond high-voltage pulses are very efficient (electrical energy input to radical yield) in a variety of applications. More specifically, some researchers have reported that the pulse duration and rise time of the applied high-voltage pulse have a significant influence on the radical yield of the transient plasmas generated with these pulses; shorter pulses lead to higher yields [9], [10], [11].

For PAW, it was shown that the species present in PAW depend on several factors, such as the type of electrical discharge and its characteristics, gas composition, and the properties of the liquid. Researchers have studied different pulse generators and reactor designs to find an efficient way of producing PAW [6], [12], [13], [14], [15], [16], [17]. To control the PAW composition and generate PAW efficiently, the influence of the pulse shape on the PAW species has to be determined. Eventually, this could lead to a PAW production system where the desired species (nitrates, peroxides, etc.) are specified, and the optimal pulse parameters are found in a plasma "recipe." Next to the differences in the pulse width and rise time, the pulse shape can include many features as shown in Fig. 1. In addition, the repetition rate, either continuous or in bursts, has a significant influence on the plasma: when plasma species (e.g., radicals or ionized particles) of a previous pulse are still present, they influence the next pulse [18], [19]. This opens a new area of research to plasma generation [15], [20].

TABLE I
PULSE SOURCE PARAMETERS

Parameter	Design parameter	Realisation
Voltage	0–20 kV	0–20 kV
Pulse current	400 A (50 Ω)	400 A up to kA
10–90% rise time in 50 Ω	5 ns	8 ns
Pulse width	10 ns to 10 μs	25 ns to 100 μs
Continuous power transferred	1 kW	1.3 kW (best case)
Repetition rate	20 kHz	power dependent

A. HV Pulse Generation

To produce flexible, arbitrary-waveform, high-voltage pulses to study PAW, we developed a new HV pulse generator. This article shows the major design decisions and results of this generator.

Many circuits exist for generating HV pulses, but only few are suited for flexible, arbitrary-waveform pulse generation. These include the SS linear transformer driver (SS-LTD) [21], [22] and the SS-Marx [23], [24], [25]. Both the SS-LTD and SS-Marx consist of a number of modules in series: each providing a small part of the output voltage. The output voltage will be the sum of all turned-on modules at a given time. By delaying the turn-on of some modules, flexible output pulse shapes can be generated. Both the circuits can be designed for unipolar (either positive or negative) or bipolar pulses. We focus only on unipolar positive pulses to decrease complexity and focus on fast switching. While both the types of generator are capable of generating a variety of pulse shapes, typical implementations are unable to generate the fast rise times (<5 ns) we are interested in for plasma generation.

Recently, we developed an SS-IMG [26] for HV pulse generation. The IMG is similar to a normal SS-Marx, but as it uses an internal structure based on a transmission line (TL) (as suggested in [27]) the inductance is kept low and the output pulse can be of short rise time. The impedance-matched structure can be used for both the Marx and LTD with similar performance [28], and we chose to use the Marx circuit as it does not depend on magnetic cores (which could saturate at longer pulse lengths [21]). The concept and a first prototype was presented in [26] and a follow-up prototype was used for streamer discharge control with flexible pulses in [20]. This article will explain the operation principles of a significantly improved version capable of kHz repetition rate and MW power output. The IMG structure allows for very short rise times (in the nanosecond range), while the SS-Marx topology allows for flexible pulses [24]. The combination of both in SS-IMG gives us the maximum flexibility in rise time and pulse shape.

B. Requirements

The design parameters for the new IMG are summarized in Table I, as well as some realized results. Starting with pulse voltage, we need about 15 kV to reliably initiate the discharge, based on previous experience in our PAW generation setup. To have some margin and some spare stages for flexible pulses, we set the desired generator output voltage to 20 kV. The current in our plasma load will behave slightly capacitive and resistive, but is not expected to be more than a few amperes. To be able to use a 50-Ω coaxial cable as load or as connection between the load and generator, we set the minimum load impedance to 50 Ω, which results in a 400-A maximum output current. For rise time, we set the goal to 5 ns for this implementation. Through our work with gate boosting the metal–oxide–semiconductor field-effect transistor (MOSFET) switches used in the IMG [29], we know we can achieve shorter rise times for a single switch (around 2 ns), but to realize this also for the entire Marx requires very precise timing of the switches. This together with a detailed study on impedance matching (which will decrease the rise time even further) will be the topic of another article. In the current article, the focus is more on the study of the entire system, the circuits, practical design considerations, etc.

C. Article Organization

The principle of operation and design of the general IMG structure is explained in Section II followed by the design of a stage in Section III. Then, the system to recharge the IMG fast and efficiently between pulses is shown in Sections IV and V highlighting the pulse control system. Next, the results of the generator and generated plasma are shown in Section VI, followed by the discussion and conclusions in Sections VII and VIII, respectively.

II. IMG DESIGN

The IMG consists of a number of stages (like a classical Marx generator), and in our implementation the IMG is built around a coaxial structure, which will be explained in more detail. Each stage is constructed on a single printed circuit board (PCB) and consists of one or more simultaneously switched fast semiconductor switch modules (FSSMs) arranged in a cylindrical pattern to propagate pulses toward the center of the PCB. The FSSM consists of capacitive energy storage and a semiconductor switch with gate driver, along with a diode that allows the HV pulse to bypass the stage. This way, each stage can switch independently, and the output voltage is the sum of the voltages of the enabled stages.

Stages are connected together using a TL in their center, which provides a low inductance path for the HV pulse to propagate toward the load. For this design, we use a coaxial TL, but an IMG can be constructed using any TL structure. The circuit scheme is shown along with the TL in Fig. 2, and the final design is shown in Fig. 3. More on the inner TL will be described in Section II-B.

A. Sensors

At the top of the generator, the last part of the TL does not change impedance anymore. Here, a load or cable can be connected with preferably the same (characteristic) impedance as the generator output. Just below the output, a D-dot voltage sensor and Rogowski current sensor are integrated in the TL (without disturbing the coaxial structure) to measure the HV pulse. A basic summary of the sensor system can be found in Table II, and detailed information is provided in [30].

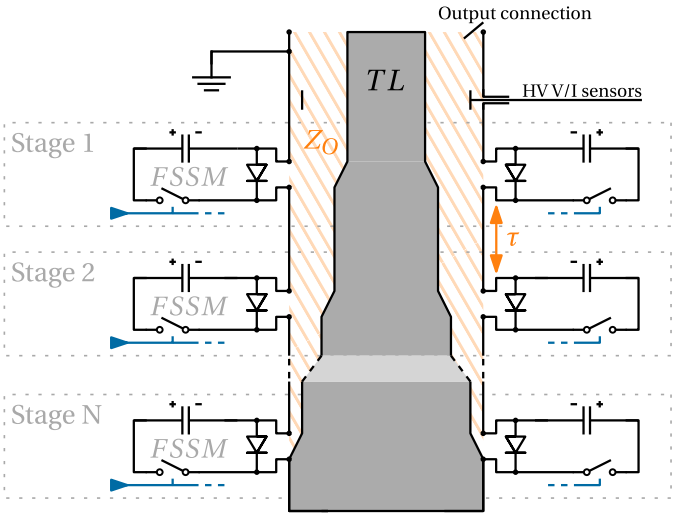

Fig. 2. Schematic drawing of the IMG circuit with two FSSMs shown per stage, showing three stages (1, 2, and N). Stages are connected together using a coaxial TL (TL). The characteristic impedance of the output is indicated as Z_O and this impedance decreases with each stage toward the bottom. The travel time of the HV output pulse between stages is indicated as τ and depends on the physical distance between the stages. Optic control connections (in blue) control the FSSM switching. Diodes in the FSSM allow a stage to be bypassed.

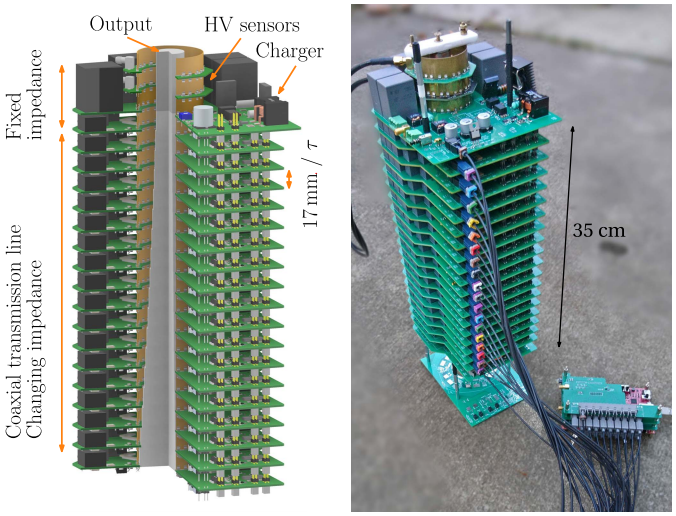

Fig. 3. 3-D model of the IMG in a three-quarter section view. The output connection on top is shown with integrated voltage and current sensors. The coaxial inner conductor of the TL changes in diameter with the Marx stages, to change the characteristic impedance (left). The TL has a fixed output impedance set by the final inner conductor diameter (50 Ω in the shown model). Stages are spaced 17 mm apart, resulting in a pulse travel time of τ (top). Picture of the implemented IMG, with the FPGA control system in the bottom-right corner, connected with optic fibers to each stage (right).

For the expected rise time of the pulse (5–8 ns), these sensors have sufficient bandwidth (rule of thumb: (0.35/5 ns) $\approx$ 70 MHz at least), but short current peaks from a load or load reflection might be in higher frequency range than can be measured by these sensors.

B. Impedance Matching

As individual stages are combined into a Marx structure, it is key to maintain the switching speed of each stage toward the output and load. This is performed using impedance matching, giving the IMG its name. This section shows just a summary. More details are available in [26].

When the three following matching conditions are met, the individual pulses of each stage will add up perfectly at the load and the IMG behaves impedance-matched.

1) All the stages (specifically, all FSSMs) match to the central IMG TL.
2) The IMG TL output impedance is matched to the load impedance.
3) All the stages switch with a specified delay, so each stages' pulse arrives simultaneous at the load. This is noted as τ in Figs. 2 and 3.

In any other case, pulse reflections will occur in the IMG, which may result in an unwanted output waveform (e.g., overshoot, undershoot, and slower rise times; see examples in [26]) or potentially even in damage to IMG components due to overvoltage at certain parts of the IMG. The first two matching conditions are explained in Sections II-B1 and II-B2 and the third one in Section V.

1) Stage Impedance: The previous section assumed that the impedance of the FSSMs of each stage will match the characteristic impedance of the central TL. This is not necessarily true. For instance, in [27] the impedance of their (spark-gap based) FSSM counterpart, a "brick" is matched to the internal TL of the impedance of all the parallel "bricks" combined. Our FSSMs are solid-state, SiC MOSFET-based and have a less defined characteristic impedance (or one could take $R_{\mathrm{ds,ON}}$ of less than 100 mΩ plus the very small inductance of the FSSM, which will result in higher currents than the device can handle). To give our FSSMs an impedance, and so to make sure the FSSMs match the inner TL, we designed a small PCB coplanar TL in [26]. A schematic representation is shown in Fig. 4. The simulations and measurements in [26] could not prove the need for this TL, while it introduces significant parasitic effects. These effects include the large capacitive coupling of FSSM TLs to nearby stages, but mostly are a source of reflection when the IMG is used in the non-matched mode, like when flexible pulses are generated.

The IMG discussed in this article should be able to operate both in matched (for single, short rise time, HV pulse) and non-matched (flexible pulses, slower rise time) modes. Instead

TABLE II
INTEGRATED HV PULSE SENSORS' SUMMARY

Sensor	Gain	Bandwidth	Response
D-dot (voltage)	$1.7{\cdot}10^{-11}$	330 MHz	400mV / 10kV
Rogowski (current)	$3.9{\cdot}10^{-10}$	129 MHz	200mv / 200A

Fig. 4. FSSM schematic, consisting of MOSFET switch, HV capacitor, and bypass diode. FSSM without TL (left) and FSSM with TL (right) to set its characteristic impedance to Z_S.

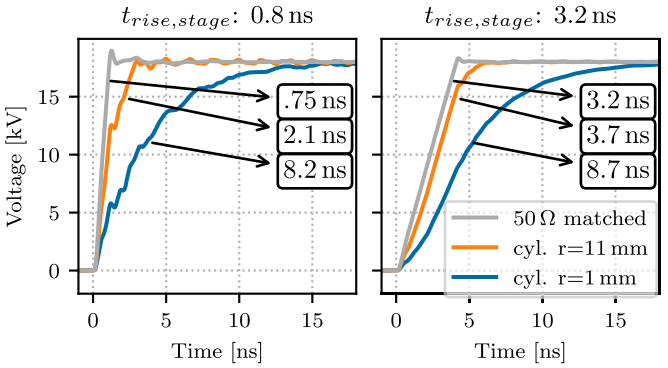

Fig. 5. CST Studio Suite simulated pulse of 18 stages with three different inner conductors with 50-Ω resistive load. An inner conductor matched to 50 Ω is used, as shown in Figs. 2 and 3, and two inner conductors of metal cylinders of 1- and 11-mm radii. 1-ns simulated turn-on time per stage (0.8 ns 10%–90% rise time) (left) and 4-ns turn-on time (3.2 ns rise time) (right) and the shown load voltage on a 50-Ω resistive load. The annotations show the 10%–90% rise times of the load voltages for all six situations. For the 50-Ω matched situation on the left, the rise time is reduced to 0.75 ns, because of the slight overshoot on the load voltage.

of using an FSSM TL, the FSSMs are placed in a ring around the central TL, as close as possible to each other and to the central TL (further explained in Section III). This way all the FSSMs on one stage operate as one single circular switch whose impedance matches to that of the central TL.

2) Central Coaxial TL: The HV central TL is used to provide a low inductance path for the HV pulse from the stage to the load, reducing the electromagnetic interference (EMI) emission and preserving the pulse shape of the individual stages. Each stage should switch the same current, while the voltage in the internal TL changes with each stage closer to the load. This results in a required characteristic impedance of (1 kV/400 A) = (50 Ω/20 stages) = 2.5 Ω per stage.

The outer structure of this TL consists of brass rings of 15-mm height and 54-mm diameter, connected to the top and bottom of a stage. The inner conductor of this TL connects the lowest stage, through all other stages, to the load at the top (see, e.g., Fig. 3). The inner conductor can be changed to match various load impedances, for example, a 50-Ω output impedance requires a 23-mm diameter inner conductor at the load side.

To prove the need for this impedance matching, a model of the IMG is made in the 3-D-EM simulation program CST Studio Suite 2021 [31] (CST) for a time-domain simulation. Using 18 stages, firing with a small delay as specified in Section II-B and each FSSM represented by a discrete port, we simulated different inner conductors at 1- and 4-ns turn-on time per stage (0–1 kV) on a 50-Ω resistive load. The effective rise time of the stage voltage (10%–90%) is then 0.8 and 3.2 ns, respectively. Three different inner conductors were used: A matched 50-Ω inner conductor (which changes diameter every stage), a cylinder of 1-mm radius, and a cylinder of 11-mm radius. This results in six outcomes, as shown in Fig. 5. We can see that the matched inner conductor results in the best waveform. When the impedance is not matched (especially so for the 1-mm inner conductor), the waveform suffers accordingly. Here, we also see that the need

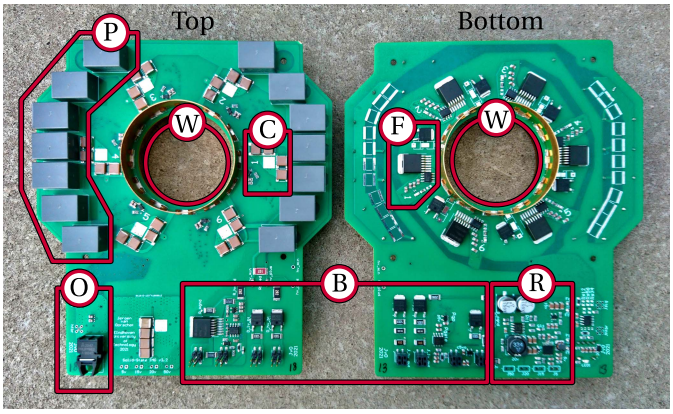

Fig. 6. Top and bottom of a stage. W = TL for HV pulse, F = FSSM, C = FSSM ceramic capacitors, P = stage plastic film capacitors, O = optic input for control signal, B = bootstrap charging circuit and stage interconnect, and R = low-voltage regulators.

for impedance matching is greatest when the rise time of the FSSMs is shortest (or more correctly, when the travel time of the pulse through the IMG structure becomes closer to the rise time of the individual stages).

III. Stage Design

This section describes the design of a single IMG stage. Such a stage consists of six FSSMs, optic control signal input, low-voltage (LV) power converters, and charge circuitry. Each stage is triggered by an AFBR 2624Z optic input, which converts the optic input into an electrical trigger for each of the six FSSMs. The layout of a stage is shown in Fig. 6.

A. Fast Semiconductor Switch Module

The first step in a fast rising output pulse is a fast switching FSSM. As in [26], we want to use a SiC MOSFET switch as these are the fastest switches available at moderately HV and current capabilities. We chose to use 1200-V rated devices, because these are widely available, and about 1-kV stage voltage is a good tradeoff between the number of stages and flexible pulse voltage step size. We want to use an surface mounted device (SMD)-type MOSFET to keep the stages compact and the package inductance low. A comparison was made between various SMD-type 1200-V SiC MOSFETs, and the fastest from our test was chosen, which is the NTBG080N120SC1 from ON semiconductors. Six FSSMs are placed in parallel on a stage for current sharing, as a lower current per MOSFET reduces switching times. Usually, MOSFETs are controlled by a gate driver with a series resistor to limit ringing on the gate. To drive MOSFETs faster, and reduce the turn-on time, special gate driving circuits can be used like gate boosting [29], [32], [33]. Because of the difficulty to implement these (e.g., large component area is needed, increased complexity, higher driving voltages), conventional gate drivers are used in our design. We use an NCP81074A driver, which was selected based on high current, fast switching capabilities, and about 10-ns shortest on-time. The implemented FSSM layout is shown in Fig. 7. Here, we took care to place the gate driver as close as possible to the MOSFET gate and used the

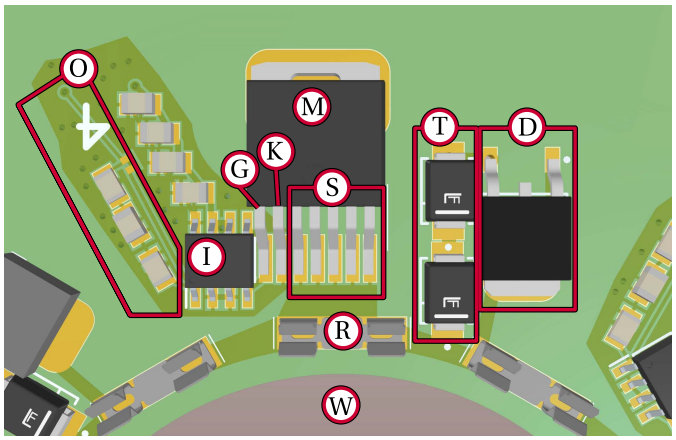

Fig. 7. One FSSM with traces visible on 3-D-render. O = signal input from the optic receiver, I = gate driver IC, M = MOSFET, G = MOSFET gate pin, K = MOSFET Kelvin source pin, S = MOSFET power source pins, R = ring connection for the outer TL, W = hole for the inner coaxial TL, T = optional TVS placement for overvoltage protection, and D = FSSM bypass diode.

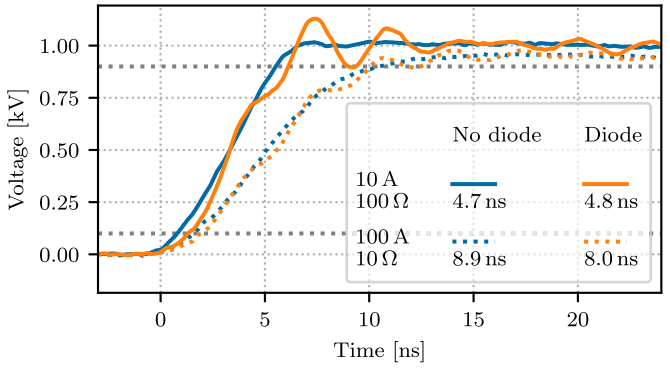

Fig. 8. FSSM-measured switching performance on MOSFET turn-on with and without HV diode placed for two loads. The diode behaves capacitively as it goes into blocking 1 kV during MOSFET turn-on. This causes some oscillations which are mostly visible at the 100-Ω load. The voltage 10%–90% rise time is calculated and averaged for 100 waveforms and shown in the legend.

Kelvin-source connection as driver ground [34]. The MOSFET and diode are placed as close as possible to the central TL ring and the HV capacitors are placed below the MOSFET to keep the power loop (top TL ring–capacitor–switch–bottom TL ring) as short as possible. Transient voltage suppressor (TVS) can be placed for overvoltage limitation but are left out of the implemented design. Ground planes are only placed where needed (around the driver) to reduce capacitive coupling to the stages below and above.

1) Diode: When not all the stages are fired, or not all at the same time, the HV pulse bypasses the inactive stages using diodes. We selected the 1200-V SiC diode IDM05G120C5 from Infineon, for its high current capability and low junction capacitance. Still, the junction capacitance will influence the pulse shape and rise time. The measured waveforms of one FSSM switching at 1 kV with 10 and 100 A, with and without diode, show this effect in Fig. 8. The diode causes ringing on MOSFET turn-on due to the diode's capacitive nature but the effect on rise time is negligible. The effect is twofold: for low current, a small increase in rise time is seen, while for a high current the rise time decreases in the situation

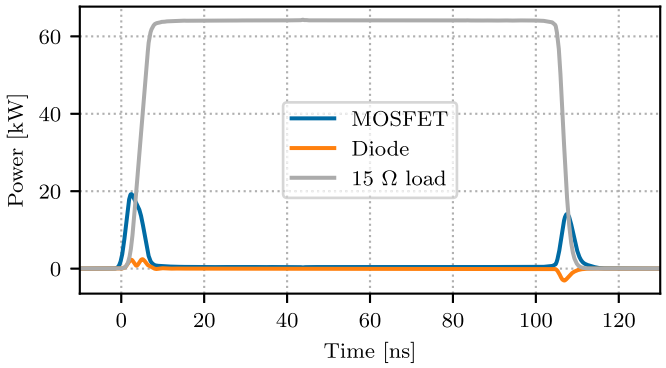

Fig. 9. Simulated power losses of one FSSM switching, using realistic MOSFET and diode models and an ideal load and source. The shown graph has a 6.5-mJ pulse in the load, 183-μJ losses in the MOSFET, and an insignificant 0.5-μJ diode losses.

with diode. The first case is mostly due to the higher capacitive load, while in the high current case the diode acts as the sharpening capacitor [35]. These diode effects are unfortunate, but unavoidable in flexible waveform Marx generators.

2) HV Energy Storage: The second important part in fast switching is the stages' energy storage. The SMD X7R-type capacitors are placed close to the MOSFET, and plastic film capacitors are placed at the edge of the stage PCB. The SMD C0G-type capacitors were considered, as these are more suitable for higher frequencies and pulsed currents, but not used as they are only available in low values and measurements did not show faster switching with these capacitors. Finally, the PCB has extra copper plane area on the HV+ and − to provide about 1.3-nF board capacitance. In total, each stage provides almost 800-nF capacitance, storing at most 400 mJ at 1000 V.

Twenty stages in series will have (at most) 40-nF capacitance, allowing a 100-ns 50-Ω pulse (20 kV, 400 A) with about 5% voltage droop.

B. Stage Power Limits

1) Stage Repetition Rate Limits: To estimate the maximum power transferred by a stage, one FSSM is simulated in LTSpice [36] with the MOSFET and diode model from the manufacturer, as shown in Fig. 9. Using a 15-Ω resistive load at 1 kV, 67-A current is switched (this corresponds to a 400-A stage current as specified before). Switching losses are about 183 μJ in the MOSFET and 0.5 μJ in the diode, compared with a load energy of 6.5 mJ in a 100-ns pulse (97% efficient). The MOSFET losses occur almost only during the switching transient, because of the low MOSFET steady-state on-resistance of about 80 mΩ. Therefore, the single pulse power loss is mostly dependent on the switch rise/fall time (which corresponds mostly to switched current) and not on the pulse length. This assumption holds even more strongly when switching capacitive behaving loads (having only output current during the switching transients), like in dielectric barrier discharge (DBD) reactors.

We can calculate the maximum pulse repetition rate based on the simulated power loss and the MOSFET datasheet specification of about 2 W of heat dissipation to ambient

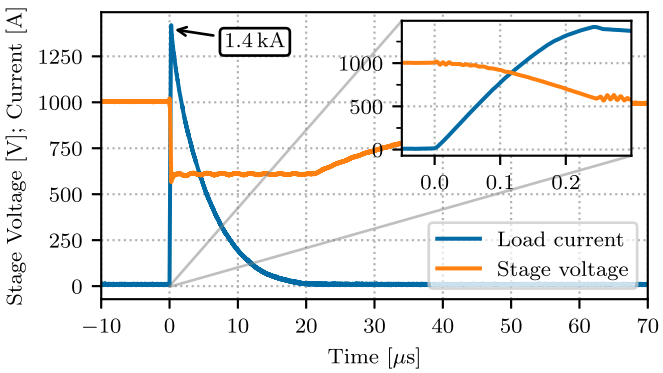

Fig. 10. Measured waveforms of one stage switching a short-circuit inductive load (about 10-cm wire). The FSSMs turn off at 250 ns when 1.4 kA is reached. Then a large current flows through the FSSM diodes for 19 μs. After some dead time, the recharge starts at $t = 20$ μs.

(without heatsink) as

$$2 \text{ W}/183 \ \mu\text{J} \approx 11 \text{ kHz}. \quad (1)$$

At lower switched currents, there are fewer losses, so a higher repetition rate is feasible.

2) Stage Current Limit: Each FSSM can handle 100 A as shown in Fig. 8, and each stage is designed for at least 400 A. Both should be able to handle occasional higher currents in the event of a short-circuit or spark in the load. One stage is tested for a single shot with an inductive short-circuit load, on a 250-ns 1-kV pulse, measured using a Bergoz CT-F0.25 current transformer and shown in Fig. 10. At the end of the pulse, the current has reached 1.4 kA which then flows through the diodes for 19 μs until all energy is dissipated. Although the MOSFET and diode currents are above the datasheet values for pulsed operation, the I^2t (maximum rating for current^2 · time) values are within the maxima and the components survive this pulse. The stage' capacitors are discharged to about 600 V in 250 ns (1.6 V/ns), which is below the rated dV/dt maximum of 6 V/ns for the plastic film capacitors on the stage.

C. Intrastage Paralleling

Each stage has six FSSMs in parallel, and they all need to switch at the same time to share the switched current in the stage. From the optic control signal input of the stage, three length-matched traces trigger two FSSMs each simultaneously. For longer pulses, MOSFETs will share current evenly due to the positive temperature coefficient. However, at the start of the pulse the current sharing depends strongly on the turn-on delay of each MOSFET. This turn-on delay is set by three factors: 1) the trace length difference between the optic receiver and the FSSM; 2) the internal delay in the MOSFET driver; and 3) the turn-on delay of the MOSFET (e.g., caused by threshold voltage differences) [37], [38], [39].

We investigated the current sharing by measuring the current in each FSSM sequentially with a LeCroy WaveRunner 9254M at 500-MHz bandwidth and plotting these together. Fig. 11 shows the first two measured delays in the top graph and the

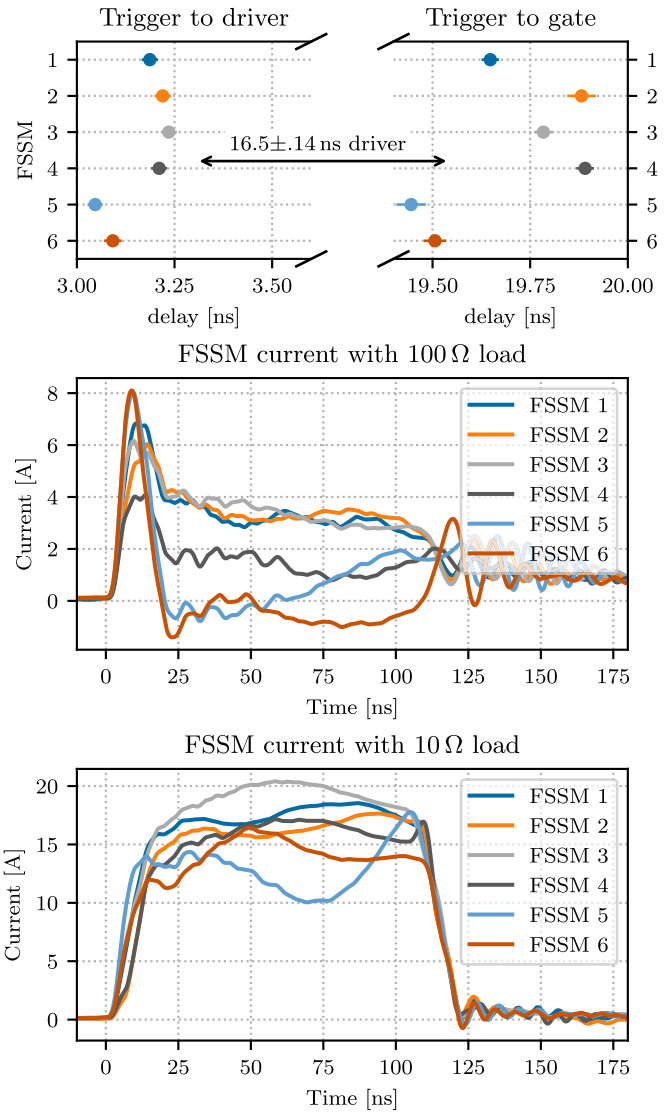

Fig. 11. Measurement results on paralleling the six FSSMs on one stage. The top graph (left side) shows the measured trace length delay from the optic receiver on the stage (trigger) to each FSSM driver input. The arrow indicates the MOSFET driver delay, of about 16.5 ns. The right side of the top graph shows the delay from trigger to gate pulse, combining the trace delay and driver delay. These delay measurements were taken at 40 GSample/s and have less than 40-ps standard deviation jitter (shown as horizontal error bar) over more than 1000 measurements. Finally, the two bottom plots show the current of each FSSM at 1 kV for 100-Ω and 10-Ω loads, respectively. A single-shot waveform is shown: the shot-to-shot difference in these waveforms is negligible.

actual FSSM current sharing for two different loads in the two graphs below.

Although the FSSMs should receive their control signal at the same time by length-matched traces, FSSMs 5 and 6 get the signal about 150 ps earlier, which can be explained by the mostly meandering traces toward these FSSMs as these are the closest to the optic control input. Next, the MOSFET gate voltage starts increasing about 16.5 ns (with at most 280-ps difference among FSSMs) after the driver input signal goes high, mostly because of the driver delay but also the differences in MOSFET gate capacitance can play a role here.

The two bottom graphs of Fig. 11 show the actual current of the six FSSMs, measured at the MOSFET drain by lifting

the drain about 1 cm from the PCB and connecting it using a small wire with a small PCB Rogowski coil around it (Rogowski coil design discussed in Appendix A of [29]). A hundred measurements were taken at 20 GSample/s (with 80-MHz low-pass filter) for each FSSM individual with the same overall output voltage and current waveform, both for 10-Ω and 100-Ω resistive loads at 1 kV. The shot-to-shot variation within these hundred measurements is negligible (e.g., less than 150 ps MOSFET turn-on time standard deviation jitter), and one measurement for each FSSM is shown.

In the 100-Ω load case (10 A switched in total), the inrush current from the parasitic capacitances in each FSSM is visible. The peak current of all the FSSMs combined is around 40 A, far above the steady-state current of 10 A. These inrush currents are mainly caused by the capacitive behavior of the FSSM diodes and to a smaller extent from the bootstrap charging components and the PCB capacitance. This inrush current is mostly carried by FSSMs 5 and 6, which is explained by their earlier turn-on. After the inrush, these two carry significantly lower current. Not all the differences can be explained by the timing offsets, like the current difference between FSSMs 2 and 4 which turn-on at the same time but carry about 3.5 and 1.8 A, respectively. When switching higher currents, as shown in the bottom graph for 100-A load current, the inrush is no longer visible and the current sharing is much better, which validates the design of the stage.

A future version of the stage could implement a variable delay to each FSSM to compensate for the turn-on delay differences, either as one-time calibration or using a feedback loop in an active gate drive system [38], possibly combined with overcurrent protection for each FSSM [40].

IV. High Repetition Rate Operation and Fast Recharging

In between pulses, the IMG is recharged using a current-limited bootstrap charger system. The stages need both LV power (LV, 20–100 V, for control signals) and HV power (HV, 0–1 kV). The HV is directly used to charge the pulse capacitors, while the LV is converted into a gate drive voltage using dc/dc converters on each stage. This power is supplied by two diode strings and the return current flows through bootstrap switches. The bootstrap circuit also discharges any remaining energy in the load, for instance, for discharging a capacitive load after the HV pulse.

Fig. 12 shows the general structure of the IMG with the bootstrap charger system. The system consists of a bootstrap switch S_{bst} (not part of an FSSM) on each stage, to connect the stage ground to the previous stage ground. This switch comprises a MOSFET and a series diode to block the body diode of the MOSFET, as the body diode is in parallel with the FSSM diodes. When the command to start charging "ch_en" is given, V_{lv} and V_{hv} power supplies are connected and optocouplers (O_1, O_2) forward the signal to each next stage to close the bootstrap switches. Next, the charge current for HV and LV flows to all the stages in parallel via diodes D_{hv1} and D_{lv1}. A second diode D_{hv2}, D_{lv2} prevents any balancing currents between stages if they are unequally discharged

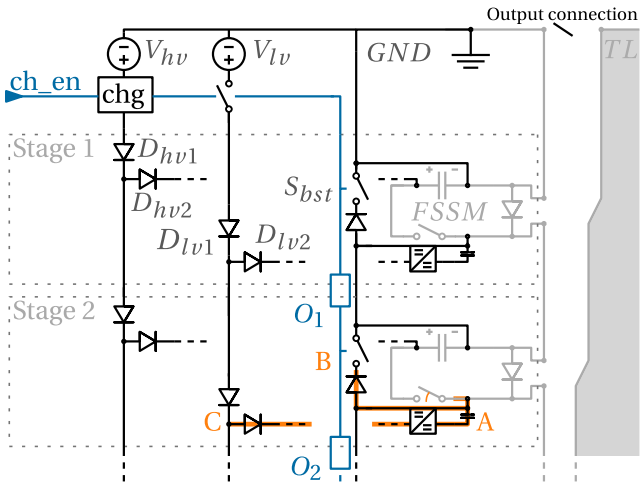

Fig. 12. Schematic of the IMG as in Fig. 2 in gray, including the bootstrap charger circuit in black. Charging is controlled by the optic input "ch_en," which controls the HV current-limited charging circuit "chg" (shown in Fig. 13), the LV charge switch, and a bootstrap MOSFET on each stage S_{bst}. Optocouplers $O_1, O_2, \ldots$ pass the ch_en signal through all the stages. The HV and LV are each recharged via two diodes on each stage (D_{hv1}, D_{hv2}, D_{lv1}, D_{lv2}). The LV voltage is downconverted to create the required voltage levels on each stage using a dc/dc converter (=/= symbol).

(which is especially important in flexible pulse operation), as suggested in [41]. It will also halve the parasitic capacitance of the diodes (limiting parasitic current) and add more margin to the voltage rating.

On the second stage in the circuit drawing of Fig. 12, one path is highlighted in orange. This path shows one of the parasitic effects that can happen in a bootstrap system like this. During the switch-on of stage 2, the LV capacitor (indicated by A), connected to the FSSM MOSFET source, is lifted by 1 kV. This results in an inrush current in the LV charging bootstrap diodes through the LV DC/DC converters. At points B and C, this could result in LC voltage-doubling, from the trace inductance in series with the diode capacitance. In addition to damaging the charging system, this inrush current stresses the FSSMs and increases the HV pulse rise time. To prevent this effect, series resistors are placed at various places in the LV charging path.

A. Current-Limited Charging

To allow high repetition rate operation, the stages have to be recharged quickly in between pulses, but to protect the charging circuit and reduce EMI, the charge current has to be limited. For the LV, this is performed using resistors on each stage. For HV, an additional current-limited charger circuit is designed for HV charging, shown as "chg" in Fig. 12. This charger circuit is shown in Fig. 13 and is integrated on a separate PCB on top of the IMG, visible in Fig. 3. The charger circuit is a buck converter which operates in self-resonance (as bang-bang converter) based on the charge current feedback. We set the maximum current to 10 A and choose a buck inductance of $L = 6.8\ \mu$H as tradeoffs between magnetic energy stored, charge switch SW switching frequency, and recharge time. The chosen inductor is 7443640680 from the Wurth WE-HCF series and is selected for its high current capability

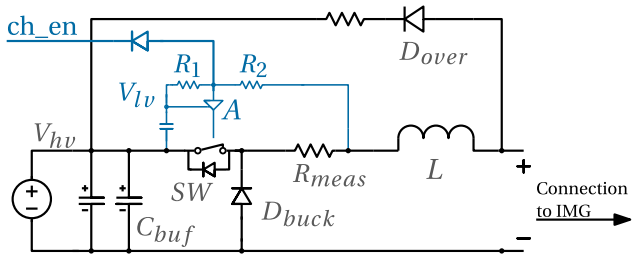

Fig. 13. Schematic of the IMG charger circuit. This is the "chg" part of Fig. 12. It is a current-controlled switched buck converter. On the left, a HV dc power supply is set to the stage voltage V_{hv}. On the right, the output is connected to the IMG. A MOSFET SW with driver A is controlled by the voltage divider R_1, R_2, and the "ch_en" enable signal. Next, a charge current will flow to the IMG through R_{meas} and L. The latter will limit the current rise rate. With increasing current, a voltage drop on R_{meas} causes the input of A to drop, which disables the switch. Current will flow via D_{buck} until the inductor L is discharged and the process will repeat until the IMG is fully charged or ch_en is pulled low. Finally, D_{over} prevents the IMG from overcharging if energy is stored in L after the last charge pulse.

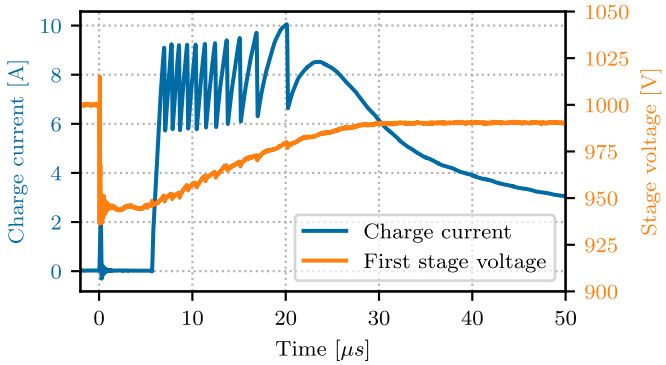

Fig. 14. Waveform of the recharging after a 70-ns pulse of about 550 mJ and the voltage of the first stage (out of 20 stages). Recharging is limited to 10 A max using the charger system. At $t = 0$, some noise is visible from the HV pulse on the charge current waveform; then after 5 μs of dead time, the charging starts. The final stage voltage is somewhat lower than the initial voltage, due to droop on the dc buffer capacitors.

of 30 A and high self-resonance frequency of 17 MHz. Fig. 14 shows the HV charge current together with the voltage of the first stage right after an example pulse of 20 kV, 400 A of 70-ns pulse length (550 mJ). After 5 μs of dead time after the pulse, recharging starts and follows a switched inductor pattern till 25 μs when the system changes to resistive charging due to some resistances in the charging path. After around 100 μs, the generator is recharged (except for some voltage droop on the input voltage buffers C_{buf}), allowing a 10-kHz repetition rate with this waveform, theoretically transferring 550 mJ $\cdot$ 10 kHz = 5.5 kW from dc to pulsed. In reality, the used switch SW, a SiC MOSFET, is power-limited and can only handle a limited number of cycles, as will be shown later on in Section VI. Therefore, the maximum pulse repetition rate is dependent on the pulse energy. We have tested this circuit, and it handles at least 1-kW power transfer from dc to Marx HV pulses at 90+% efficiency, meeting our power and repetition rate requirements.

V. FPGA Control System

With the IMG design, individual stage layout, and recharge system described, it is now up to the control system to generate the 20 pulse signals and the recharge signal.

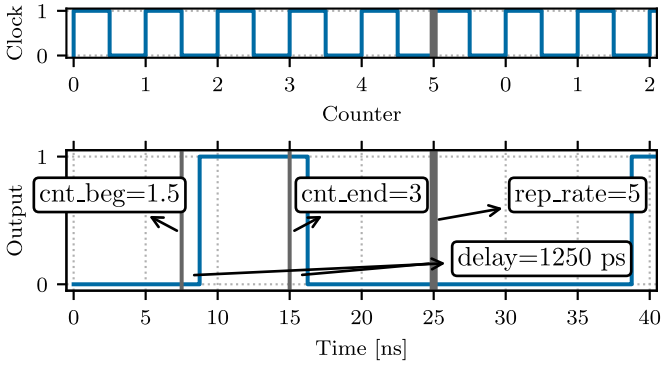

Fig. 15. FPGA clock signal and one output signal. A counter is increased with every clock cycle (of 5 ns) and reset when the (programmable) value of register "rep_rate" is reached. The output signal starts when the counter reaches the (programmable) value of "cnt_beg" and stops at value "cnt_end." Using DDR, the output can change both the rising and falling edges of the clock, giving 2.5-ns resolution. Using delay lines, the output can be delayed to have a timing precision down to 70 ps.

The field programmable gate array (FPGA) control system based on a Zynq-7000 on a PYNQ-Z2 board as shown in [26] has been improved. The FPGA generates up to 24 TTL output signals, using auxiliary boards with AFBR1624 optic transmitters, connected with plastic optic fiber (POF) to each stage. It switches each output on and off at a specified, programmable, time and repeats this with a certain repetition rate. Also, switching patterns can be repeated, which allows for burst-mode pulsing. All these parameters can be set/changed from a remote computer in millisecond timescale, allowing live reprogramming of the pulse shape. Accurate timing control is achieved using a 200-MHz clock (5-ns time step), with control on both the edges of the clock dual data rate (DDR), meaning the pulse begin time can be controlled in 2.5-ns time steps. Using tapped delay lines inside the FPGA [42], [43], we can bridge this 2.5-ns gap by delaying signals in steps of around 70 ps. An example of one output of the control system together with explanation of the programming is shown in Fig. 15.

A. Synchronous Firing and Control

To meet the last impedance matching requirement of Section II-B, the stages should fire in such sequence that the pulse from each stage arrives at the load at the same time. Theoretically, this means each stage further away from the load should be triggered 57 ps earlier than its predecessor. In practice, each stage has a slightly different turn-on delay, because of device-to-device differences in the used components. Next to component variations, the FPGA itself has some internal delay differences between its outputs. To make sure each stage switches at the right time to fulfill the matching criteria, we use an automated calibration method, where we fire each stage individually and measure when its pulse reaches the IMG output as shown in Fig. 16. This system measures the time delay, both for turn-on and turn-off, of each stage individually and this is then compensated for in the control system. The result of calibration on the HV output pulse of an 18-stage IMG is shown in Fig. 17, including the pulse rise and fall times: Without calibration, a clear bump is seen

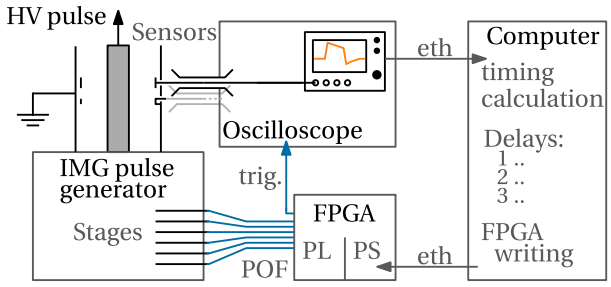

Fig. 16. Schematic overview of the control system for calibration stage timing. The FPGA controls each stage of the IMG over POF and is controlled by the computer over ethernet ("eth"). Stages are fired one-by-one and the oscilloscope measures the output pulse. The measured data are transferred to the computer over ethernet ("eth"), and the delay between the FPGA trigger ("trig") and the stage HV output pulse is measured. This results in a list of delays for each stage, which are used to compensate the stage timing afterward.

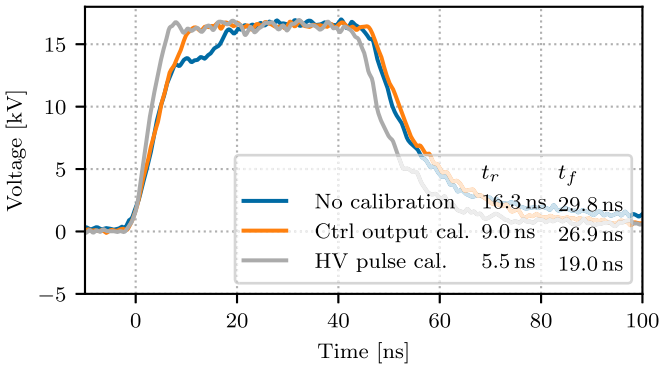

Fig. 17. Three measured waveforms of an 18-stage (17.5-kV output) IMG with different calibrations on a 120-Ω resistor load. Shown are no calibration, calibrated on the output of the FPGA control system (Ctrl output) and calibrated on the HV pulse. The rise and fall times of the 10%–90% transition are shown in the legend.

because of about 20-ns delay difference between some outputs of the FPGA. Next, the FPGA control system output delay differences are calibrated and the FPGA fires each transmitter at the exact same time, and this leads to a reasonably good result (Ctrl output cal.). Finally, the HV output pulse calibration is shown (this is calibrated using the system described before), which compensates both for FPGA delay, stage-to-stage switch delay variations and the increasing IMG pulse propagation delay with stages further from the load. As expected, the output HV pulse calibration performs best in terms of short rise and fall times, leading to 5.5 and 19 ns, respectively for the shown pulse of 18 stages switching 1 kV on a 120-Ω resistive load.

At this moment, the mentioned delay lines are implemented in only 12 outputs, so not all the stages are calibrated to the 70-ps switch timing. We are planning an upgrade of the FPGA system to calibrate delay more accurately, leading to even shorter rise times: this will be part of a future article.

VI. Results

This section evaluates the performance of the developed 20-stage IMG. The results of actual impedance matching, continuing the simulation of Section II-B, are not yet available, and these will be part of a future article. Unless noted otherwise, the output pulse waveforms are taken with the sensors developed in [30] with a LeCroy WaveRunner 620Zi (2 GHz, 10 GSample/s, 8-bit) digital storage oscilloscope. As TL inner conductor, a 100-Ω matched conductor is used for the 100-Ω load measurements and a cylindrical inner conductor of 11-mm radius for all other measurements.

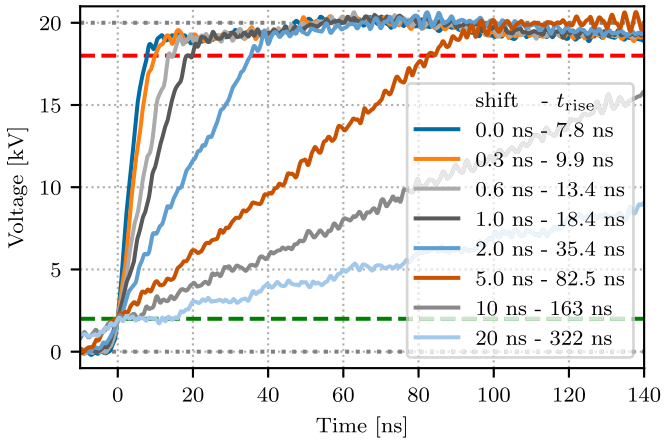

Fig. 18. Rise time variation: by changing the delays when each stage is triggered, a variable rise time can be achieved. The legend shows the delay shift of each stage and the achieved output 10%–90% rise time.

A. Rise Time

After calibration as shown in Section V-A, we can add a delay to the firing of each stage to explicitly increase the pulse rise time. A delay (shift) between subsequent stages of 0–20 ns is shown in Fig. 18 for a 20-kV pulse on a 100-Ω resistor load and the 10%–90% rise times are indicated. The shortest rise time that can be achieved is 7.8 ns (and about 8.0 ns on a 50-Ω resistive load), and by delaying each stage, longer rise times are realized. For instance, using 5-ns delay between each stage, a rise time of around 82 ns is realized. With a 20-ns delay between each stage, the steps of the delayed switching of stages in the waveform become clearly visible.

B. Flexible Pulses

Next to delaying the firing of certain stages for flexible pulses, a feature of this Marx is burst-mode pulsing, where a pulse shape is repeated more times without recharging in between. Fig. 19 shows three example flexible pulses: the shape of the letter "J" by firing four stages for a first pulse (4 kV) and 16 stages for the second pulse (15.5 kV), a burst-mode pulse of four 50-ns 17-kV (20 stages at 850 V/stage) pulses 150 ns apart, and a "tail" shape of a 70-ns pulse with a 500-ns tail at 18-kV peak (20 stages at 900 V/stage).

When not all the stages are used for pulsing, the others can be used for droop compensation on longer pulses, which is shown in Fig. 20. Here, a 1-μs pulse of 1 kV/stage is fired in a 50-Ω resistive load: 15 stages start a pulse and the five remaining turn on later to compensate the voltage droop of the capacitors.

C. Power, Repetition Rate, and Efficiency

Finally, we evaluate the continuous operation of the IMG in high-power conditions and measure its electric efficiency

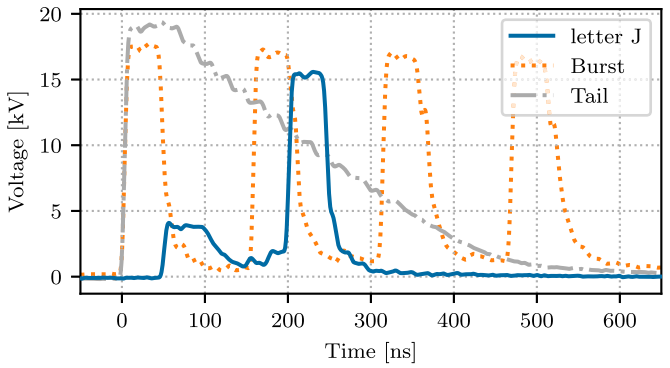

Fig. 19. Example flexible pulses on a 100-Ω resistive load. Shown are a letter "J" shape, burst mode of five pulses of 50-ns width and 150 ns between pulses, and a fast rising pulse with a long tail. The amplitudes of "J" are lower because not all the stages are fired for the second peak, and for the burst and tail the stage charge voltage was lowered to 900 and 850 V, respectively.

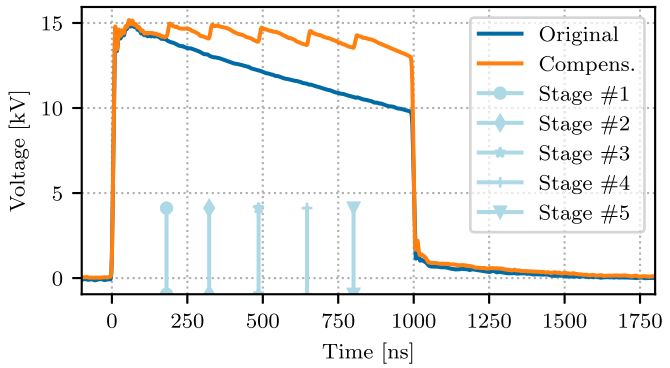

Fig. 20. 15 stages pulsing into a 50-Ω load for 1 μs. The other five stages are enabled later (at the indicated points) to compensate for the voltage droop over the resistor. Also the original (with no droop compensation) pulse is shown.

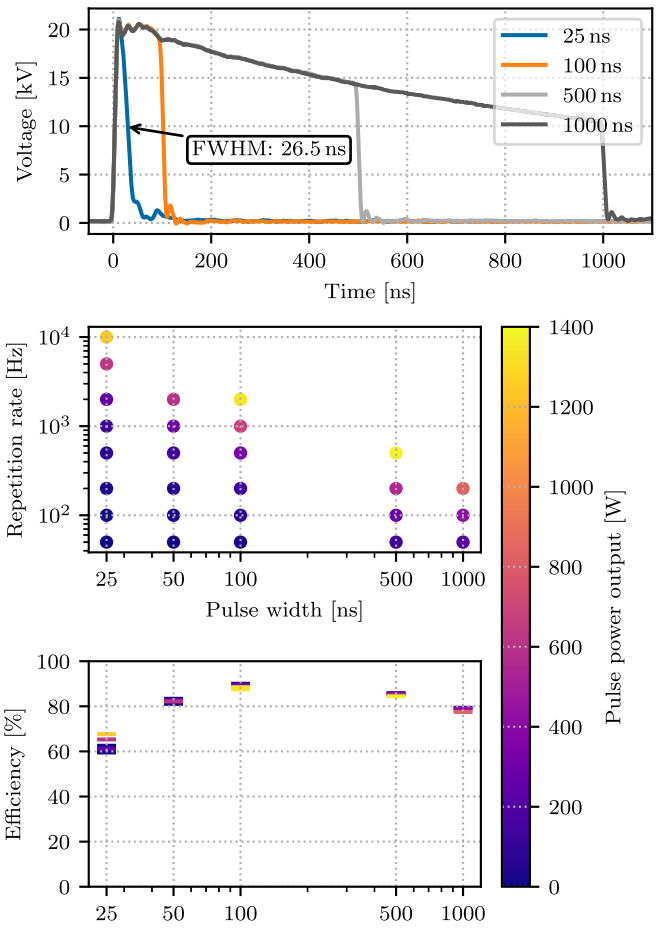

Fig. 21. Efficiency versus pulse width for powers up to 1370-W output. For low pulse widths, the efficiency and power are limited by the pulsing MOSFETs, as they are at the limit shown in Fig. 9. For longer pulses, the charging system determines the power limit and the efficiency drops because of the higher stress on the charger.

for various pulse widths and repetition rates. The conversion efficiency from 1-kV dc to 20-kV pulses by the IMG is evaluated using a high-power 50-Ω resistor as load. The integrated sensors are not suited well for μs pulses, and therefore, these measurements are taken with a Northstar PVM-1 HV probe and a Bergoz CTF-0.25 current transformer.

In the top graph of Fig. 21, we show the measured voltage waveforms; the shortest pulse of full output voltage we can reach with this type of load is about 25 ns (actual FWHM 26.5 ns) and we increase it in four steps to 1 μs, resulting in a pulse energy from 150 mJ to 4.1 J. By varying the repetition rate of these four pulse lengths, we vary the transferred power from 10 to 1370 W (max 1850-W input), as shown in the middle graph. This confirms that 10-kHz 400-A switching is feasible for 25-ns pulses, but in this operation mode the FSSMs are easily damaged by overheating (see Section III-B). For longer pulses, the maximum repetition rate is lower because of the power limit of about 1.5 kW of the charger system. Finally, the bottom graph shows the conversion efficiency from dc power input to pulsed power output for the different pulse widths and power. The efficiency is optimal at 100-ns pulse width: below 100 ns, the FSSM switching losses are significant while above 100 ns the pulse energy increases and the charger system becomes less efficient as the recharge time increases. The 25-ns width pulse has most deviation on efficiency, and this is because of larger measurement errors due to the low continuous power consumption. Efficiency for short pulses could be improved by reducing the switching losses, which can be achieved with shorter rise times. For longer pulses on resistive loads, the charging system can be improved to allow higher power transfers.

VII. Discussion on Operating Area Limits and Possible Improvements

The presented SS-IMG has a broad operating area in repetition rate, pulse width, and pulse shape. To support an even wider variety of pulses, many options exist: the output current can be easily increased by more parallel FSSM switches. A higher output voltage can be reached by adding more stages or increasing the voltage per stage. More stages give more freedom for flexible pulses, while a higher voltage per stage can reduce the total system complexity. The most important parameter in higher output voltage is the inner coaxial TL isolation distance; to support higher voltages, the TL should be made larger in diameter or an isolating material should be used as dielectric instead of air.

Repetition rate and maximum continuous power are limited by the power dissipated in the stages as switching losses, and by the charger system. When optimizing the charger system for higher power transfers, care should be taken on the large recharge currents flowing in the topmost stages. For high repetition rate combined with many stages and high power, the bootstrap system might not be the best choice and (a combination with) isolated transformers on each stage might be better.

The shortest full output voltage IMG output pulse is 26.5 ns, which is limited by the FSSM rise time and the timing synchronization of the stages. For a single stage, the shortest stage pulse is 15 ns, and this is the minimum of the used MOSFET gate driver. The rise time goes down to 8 ns for full output power, or down to 5 ns for lower output power. First, the switches are the main limit in rise time at the moment. Faster switches, like gate-boosted SiC MOSFETs [29] or gallium-nitride high-electron-mobility transistors (GaN HEMTs), could help with this. A proper design with EMI in mind will then be even more critical, as faster switches introduce more transients, while especially GaN technology is more sensitive to noise. Second, the trigger timing of the paralleled FSSMs and the control system can be even more accurate, which would result in an even shorter output voltage rise time as the synchronization becomes more optimal, which in turn allows shorter pulse widths and also more options in flexible pulses.

VIII. Conclusion

In this article, we presented a 20-kV SS-IMG for the generation of flexible, arbitrary waveform pulses with the purpose to use it for PAW generation. The presented pulse generator is suitable for fast rise time ($<$8 ns), high repetition rate ($>$10 kHz), high current ($>$400 A), rectangular, and flexible pulses at high electrical efficiencies (70%–90%). Although not all the initial requirements were met, this generator gives us ample possibilities to perform plasma research with fast and flexible pulses. The designed IMG structure is theoretically capable of nanosecond to sub-nanosecond rise time pulses from each stage to the load, but the switches in the implemented IMG are currently the bottleneck for a shorter rise time. There are still many opportunities to improve the IMG design, but a solid base is set for future IMGs. Finally, the measurement results for different inner conductors, different impedance (mis)matched conditions, are not shown, but are also expected to make a difference on the rise time. These will be part of a future research on IMG designs.

References

[1] I. Adamovich et al., "The 2017 plasma Roadmap: Low temperature plasma science and technology," *J. Phys. D: Appl. Phys.*, vol. 50, no. 32, Jul. 2017, Art. no. 323001, doi: 10.1088/1361-6463/aa76f5.

[2] A. Bogaerts et al., "The 2020 plasma catalysis roadmap," *J. Phys. D: Appl. Phys.*, vol. 53, no. 44, Aug. 2020, Art. no. 443001, doi: 10.1088/1361-6463/ab9048.

[3] S. Samukawa et al., "The 2012 plasma roadmap," *J. Phys. D: Appl. Phys.*, vol. 45, no. 25, Jun. 2012, Art. no. 253001, doi: 10.1088/0022-3727/45/25/253001.

[4] F. G. C. Ekezie, D.-W. Sun, and J.-H. Cheng, "A review on recent advances in cold plasma technology for the food industry: Current applications and future trends," *Trends Food Sci. Technol.*, vol. 69, pp. 46–58, Nov. 2017. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0924224417304582

[5] P. J. Bruggeman et al., "Plasma–liquid interactions: A review and roadmap," *Plasma Sources Sci. Technol.*, vol. 25, no. 5, Sep. 2016, Art. no. 053002, doi: 10.1088/0963-0252/25/5/053002.

[6] A. J. M. Pemen et al., "Power modulator for high-yield production of plasma-activated water," *IEEE Trans. Plasma Sci.*, vol. 45, no. 10, pp. 2725–2733, Oct. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/8014474

[7] C. Bradu, K. Kutasi, M. Magureanu, N. Puač, and S. Živković, "Reactive nitrogen species in plasma-activated water: Generation, chemistry and application in agriculture," *J. Phys. D: Appl. Phys.*, vol. 53, no. 22, May 2020, Art. no. 223001, doi: 10.1088/1361-6463/ab795a.

[8] I. Adamovich et al., "The 2022 plasma roadmap: Low temperature plasma science and technology," *J. Phys. D: Appl. Phys.*, vol. 55, no. 37, Jul. 2022, Art. no. 373001, doi: 10.1088/1361-6463/ac5e1c.

[9] T. Huiskamp, W. F. L. M. Hoeben, F. J. C. M. Beckers, E. J. M. van Heesch, and A. J. M. Pemen, "(Sub)nanosecond transient plasma for atmospheric plasma processing experiments: Application to ozone generation and NO removal," *J. Phys. D: Appl. Phys.*, vol. 50, no. 40, Oct. 2017, Art. no. 405201, doi: 10.1088/1361-6463/aa8617.

[10] T. Matsumoto, D. Wang, T. Namihira, and H. Akiyama, "Energy efficiency improvement of nitric oxide treatment using nanosecond pulsed discharge," *IEEE Trans. Plasma Sci.*, vol. 38, no. 10, pp. 2639–2643, Oct. 2010. [Online]. Available: https://ieeexplore.ieee.org/document/5447704

[11] E. J. M. Van Heesch, G. J. J. Winands, and A. J. M. Pemen, "Evaluation of pulsed streamer corona experiments to determine the O* radical yield," *J. Phys. D: Appl. Phys.*, vol. 41, no. 23, pp. 1–6, 2008, doi: 10.1088/0022-3727/41/23/234015.

[12] Y. S. Jin and C. Cho, "Generation of plasma activated water by a hybrid plasma source," *IEEE Trans. Plasma Sci.*, vol. 47, no. 10, pp. 4588–4592, Oct. 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8845777/

[13] S.-H. Song and H.-J. Ryoo, "Solid-state bipolar pulsed power modulator for high-efficiency production of plasma activated water," *IEEE Trans. Ind. Electron.*, vol. 68, no. 11, pp. 10634–10642, Nov. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9234768/

[14] T. Sugai, A. Tokuchi, and W. Jiang, "Effects of pulsed power control on plasma water treatment using LTD," *IEEE Trans. Plasma Sci.*, vol. 46, no. 10, pp. 3566–3573, Oct. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8345781

[15] J. Yang, L. Zhuang, Y. Feng, T. Sugai, and W. Jiang, "Feedback control of pulsed-power generator based on solid-state linear transformer driver," *Rev. Sci. Instrum.*, vol. 92, no. 8, Aug. 2021, Art. no. 084704, doi: 10.1063/5.0054555.

[16] K. Tachibana, R. Hanabata, T. Furuki, R. Ichiki, S. Kanazawa, and M. Kocik, "Development and evaluation of newly designed coaxial cylindrical plasma reactor with liquid flow control and post-discharge reactions for water treatment," *Energies*, vol. 15, no. 11, p. 4028, May 2022. [Online]. Available: https://www.mdpi.com/1996-1073/15/11/4028

[17] C. Man et al., "Nanosecond-pulsed microbubble plasma reactor for plasma-activated water generation and bacterial inactivation," *Plasma Processes Polym.*, vol. 19, no. 6, Mar. 2022, Art. no. 2200004, doi: 10.1002/ppap.202200004.

[18] Z. Zhao, C. Li, X. Zheng, A. Sun, and J. Li, "Periodical discharge regime transitions under long-term repetitive nanosecond pulses," *Plasma Sources Sci. Technol.*, vol. 31, no. 4, Apr. 2022, Art. no. 045005, doi: 10.1088/1361-6595/ac6050.

[19] B. Huang, C. Zhang, H. Sun, D. A. Sorokin, V. F. Tarasenko, and T. Shao, "Enhancement of hydrogen radical density in atmospheric pressure plasma jet by a burst of nanosecond pulses at 1 MHz," *Plasma Sources Sci. Technol.*, vol. 31, no. 2, Mar. 2022, Art. no. 025019, doi: 10.1088/1361-6595/ac3e3e.

[20] T. Huiskamp, C. Ton, M. Azizi, J. J. van Oorschot, and H. Höft, "Effective streamer discharge control by tailored nanosecond-pulsed high-voltage waveforms," *J. Phys. D: Appl. Phys.*, vol. 55, no. 2, Jan. 2022, Art. no. 024001, doi: 10.1088/1361-6463/ac2969.

[21] W. Jiang, H. Sugiyama, and A. Tokuchi, "Pulsed power generation by solid-state LTD," *IEEE Trans. Plasma Sci.*, vol. 42, no. 11, pp. 3603–3608, Nov. 2014. [Online]. Available: https://ieeexplore.ieee.org/document/6910281

[22] Y. Feng, T. Sugai, and W. Jiang, "Solid-state bipolar linear transformer driver using inductive energy storage," *IEEE Trans. Plasma Sci.*, vol. 49, no. 9, pp. 2887–2892, Sep. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9518374
[23] L. M. Redondo, P. Tavares, J. F. Silva, and E. Margato, "All silicon Marx-bank topology for high-voltage, high-frequency rectangular pulses," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, Jun. 2005, pp. 1170–1174. [Online]. Available: https://ieeexplore.ieee.org/document/1581777
[24] Z. Zhong, J. Rao, H. Liu, and L. M. Redondo, "Review on solid-state-based Marx generators," *IEEE Trans. Plasma Sci.*, vol. 49, no. 11, pp. 3625–3643, Nov. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9600453
[25] M. Hochberg et al., "A fast modular semiconductor-based Marx generator for driving dynamic loads," *IEEE Trans. Plasma Sci.*, vol. 47, no. 1, pp. 627–634, Jan. 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8516321
[26] T. Huiskamp and J. J. Van Oorschot, "Fast pulsed power generation with a solid-state impedance-matched Marx generator: Concept, design, and first implementation," *IEEE Trans. Plasma Sci.*, vol. 47, no. 9, pp. 4350–4360, Sep. 2019. [Online]. Available: https://ieeexplore.ieee.org/document/8812678
[27] W. A. Stygar et al., "Impedance-matched Marx generators," *Phys. Rev. A, Gen. Phys.*, vol. 20, no. 4, pp. 15–20, 2017, doi: 10.1103/PhysRevAccelBeams.20.040402.
[28] R. Risch and J. Biela, "Solid-state Marx generator vs. linear transformer driver: Comparison of parasitics and pulse waveforms for nanosecond pulsers," in *Proc. IEEE Pulsed Power Conf.*, Dec. 2021, pp. 1–12. [Online]. Available: https://ieeexplore.ieee.org/document/9733145
[29] M. Azizi, J. J. van Oorschot, and T. Huiskamp, "Ultrafast switching of SiC MOSFETs for high-voltage pulsed-power circuits," *IEEE Trans. Plasma Sci.*, vol. 48, no. 12, pp. 4262–4272, Dec. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9274514
[30] J. J. van Oorschot and T. Huiskamp, "Rogowski and D-dot sensors for nanosecond high-voltage and high-current pulse measurements in impedance-matched pulse generators," Tech. Rep., Dec. 2022.
[31] *CST Studio Suite*. Accessed: Dec. 8, 2022. [Online]. Available: https://www.cst.com/
[32] M. Hochberg, M. Sack, and G. Mueller, "Analyzing a gate-boosting circuit for fast switching," in *Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC)*, Jul. 2016, pp. 171–175. [Online]. Available: https://ieeexplore.ieee.org/document/8012918
[33] A. Del Barrio Montañés, Y. Dutheil, T. Kramer, M. Sack, and V. Senaj, "Ultra-fast generator for impact ionization triggering," in *Proc. 13th Int. Part. Accel. Conf.*, 2022, p. 3. [Online]. Available: https://jacow.org/ipac2022/doi/JACoW-IPAC2022-THPOTK044.html
[34] H. Li, S. Munk-Nielsen, X. Wang, S. Bęczkowski, S. R. Jones, and X. Dai, "Effects of auxiliary-source connections in multichip power module," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7816–7823, Oct. 2017. [Online]. Available: https://ieeexplore.ieee.org/document/7782425
[35] W. Jiang, "On pulsed power rise time dominated by circuit inductance," *IEEE Trans. Plasma Sci.*, vol. 49, no. 2, pp. 830–834, Feb. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9334439
[36] *LTSpice*. Accessed: Dec. 8, 2022. [Online]. Available: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html
[37] Y. Xue, J. Lu, Z. Wang, L. M. Tolbert, B. J. Blalock, and F. Wang, "Active current balancing for parallel-connected silicon carbide MOSFETs," *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, May 2013, pp. 1563–1569. [Online]. Available: https://ieeexplore.ieee.org/document/6646891
[38] Y. Wen, Y. Yang, and Y. Gao, "Active gate driver for improving current sharing performance of paralleled high-power SiC MOSFET modules," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1491–1505, Feb. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9130032
[39] R. Risch, A. Hu, and J. Biela, "Influence of power semiconductor device variations on pulse shape of nanosecond pulses in a solid-state linear transformer driver," in *Proc. 24th Eur. Conf. Power Electron. Appl.*, Sep. 2022, pp. 1–11. [Online]. Available: https://ieeexplore.ieee.org/document/9907478
[40] A. Rafiq and S. Pramanick, "Ultrafast protection of discrete SiC MOSFETs with PCB coil based current sensors," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1860–1870, Sep. 2022.
[41] M. Hochberg, *A High-Voltage Pulsed Power Modulator for Fast-Rising Arbitrary Waveforms* (Karlsruher Forschungsberichte aus dem Institut für Hochleistungsimpuls- und Mikrowellentechnik), vol. 14. KIT Scientific Publishing, Karlsruher Institut für Technologie (KIT), 2020, p. 170, doi: 10.5445/KSP/1000097344.
[42] R. Giordano et al., "High-resolution synthesizable digitally-controlled delay lines," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 3163–3171, Dec. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7348815
[43] A. Tontini, L. Gasparini, L. Pancheri, and R. Passerone, "Design and characterization of a low-cost FPGA-based TDC," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 2, pp. 680–690, Feb. 2018. [Online]. Available: https://ieeexplore.ieee.org/document/8249545

J. J. van Oorschot (Graduate Student Member, IEEE) was born in Lewedorp, The Netherlands, in 1994. He received the M.Sc. degree in electrical engineering from the Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, in 2019. His master's thesis was on design of a short rise time solid-state HV pulse generator.

In September 2019, he joined as a Ph.D. Researcher at the Electrical Energy Systems Group, TU/e, where his work focuses on the design of flexible, solid-state pulse generators for plasma-activated water generation.

T. Huiskamp (Member, IEEE) was born in Den Dolder, The Netherlands, in 1985. He received the M.Sc. degree (Hons.) and Ph.D. degree (Hons.) in electrical engineering from the Eindhoven University of Technology (TU/e), Eindhoven, The Netherlands, in 2011 and 2015, respectively.

He worked as a Visiting Researcher at Kumamoto University, Kumamoto, Japan, the University of Southern California, Los Angeles, CA, USA, and the Leibniz Institute for Plasma Science and Technology (INP Greifswald), Greifswald, Germany. As a Ph.D. Researcher, he worked on nanosecond pulsed-power-induced corona plasmas at the Electrical Energy Systems Group, Eindhoven University of Technology, where he is currently working as an Assistant Professor. His main area of expertise is flexible, adjustable parameter (sub)nanosecond pulse source development and their application to transient plasmas for air purification and plasma-activated water generation applications.