Digital signal processing for high-capacity indoor optical wireless communication systems

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Liuyan Chen

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绝知此事要躬行

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Summary

With the increase of connected wireless devices and the popularization of the emerging data-rate-hungry latency-sensitive applications, the future indoor network is expected to realize seamless wireless coverage with the capability to support higher connectivity density, and higher capacity with higher energy efficiency/lower power consumption, lower cost, and lower latency. However, traditional radio-based wireless communication is getting exhausted to meet the requirements of the future indoor network. In response to this, many efforts have been made to realize a fiber-wireless converged picocell-based indoor network with heterogeneous wireless access technologies including but not limited to the traditional radio and the emerging optical wireless communication (OWC) technology.

OWC is a promising supplement to the traditional radio-based wireless connectivity for indoor networks such as Wi-Fi. A concept of two-dimensional (2D) infrared (IR) beam-steering which employs high-directive narrow IR beams is proposed for developing high-capacity indoor OWC systems. It is suitable for pico-cells design to support high wireless connection densities and provides unshared intrinsically high capacity for each user device. IR beam-steering can be realized by various techniques. A.M.J.Koonen et al. have proposed a cost- and power-efficient wavelength-controlled 2D IR beam-steered OWC scheme using a pair of crossed gratings and a high port-count arrayed-waveguide grating router (AWGR), in which the beam-steering is realized by tuning the wavelength of each beam remotely. Meanwhile, the low-complexity high-efficiency DSP techniques have benefited the OWC systems since it significantly improves the spectrum efficiency and signal quality, boosting the system capacity in a cost-efficient manner. My Ph.D. research is focusing on advanced signal pro-

cessing by means of digital signal processing (DSP) techniques which take care of processing the wireless signals and preparing them for the OWC system at high connection densities and at Gigabit-per-second capacity, far beyond what current radio-based (such as Wi-Fi) systems can achieve.

In our 2D IR beam-steered OWC system, which we have realized in a laboratory demonstrator using so-called optical AWGR modules, there is a trade-off problem between the spatial resolution of the beam steering and the OWC channel capacity per beam. For larger spatial coverage and higher wireless connection densities, larger beam-steering spatial resolution is needed, but it comes at the cost of a compromised channel capacity per beam. A digital filter-aided crosstalk mitigation scheme that takes advantage of the digital Nyquist pulse shaping technique is proposed to cope with this problem. By shaping the transmitted signal for narrow spectral occupancy, the inter-channel crosstalk resulting from the imperfect AWGR filtering can be reduced, which enables using a denser AWGR grid. Also, a doubled channel capacity is attainable with the improved spectrum-efficient signal. In addition, the spectral-efficient signal reduces the bandwidth requirement of the AWGR, which allows for a low-complexity AWGR design. The proposed method is not sensitive to the wavelength misalignment between AWGRs and lasers, which relaxes the design of high wavelength-stability lasers. The proposed method has been experimentally investigated over a 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m free-space link with the 20-Gbit/s data rate OWC capacity using PAM-4 format. The experimental results show the feasibility and effectiveness of the proposed method.

As the cost of eliminating the trade-off between OWC channel capacity per beam and system spatial resolution, the introduced Nyquist pulse-shaping leads to additional complexity for the hardware implementation. The resultant doubled sample rate requirement puts higher demand for higher-speed data converters. However, high-speed data converters are complex and costly. As a solution to this, we proposed to use a non-integer oversampling approach to reduce the hardware implementation complexity and power consumption for the DSP-aided AWGR-based 2D IR beam-steered OWC system with high spatial resolution. By minimizing the oversampling of Nyquist signaling with a rational factor, the lower sample rate required relaxes the requirement of complex costly high-speed data converters, thereby reducing the hardware cost and the power consumption. We have experimentally investigated the impact of the non-integer oversampling in the 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a capacity of 20-Gbit/s data rate. The oversampling rate is

minimized to a 1.1× symbol rate (when using SRRC filter with $\beta = 0.1$) with an 11-GSa/s DAC sample rate. Compared to the 2-fold oversampling Nyquist PAM-4 system, the DAC sample rate requirement is relaxed by 55%, with a cost of a 2.3-dB power penalty at the 7% FEC limit of 1×10^{-3}.

Low-complexity DSP techniques are proven to be efficient for low-cost high-capacity OWC systems. In an effort for practical realization, we have also implemented the real-time DSP based on the FPGA platform. The speed limitation of FPGA (level of MHz) forces the parallel implementation of the FPGA-based DSP algorithms to achieve the target data rate (level of Gbit/s). However, the classical semi-parallel implementation architecture introduces severe latency due to the massive intermediate data caching, which hinders the latency-critical applications. Hence, we conduct a detailed analysis of the latency of FPGA-based DSP algorithms and further proposed to use a deeply parallel architecture that requires no massive intermediate data caching to reduce the total DSP-introduced latency. Digital adaptive equalizer (DAE) is challenging the deeply parallel implementation due to its successive input samples and the iterative adaptive update scheme. To enable the deeply parallel implementation, a new data re-allocation scheme is proposed to cope with the issue of the output dependency on the successive input samples, and a look-ahead computation approach is employed to improve the adaptive update efficiency of the DAE. In addition to the latency reduction, the deeply parallel architecture also releases the utilization of large memories and does not utilize more hardware resources in comparison to the classical parallel architecture when getting the same data throughput. An FPGA-based real-time PAM-4 receiver with deeply parallel fully-pipeline DSP implementation is demonstrated in an experimental fiber link with a 2.5-Gbit/s data rate for the performance evaluation. It reveals that the BER performance has little deterioration compared with the offline processing. The real-time PAM-4 receiver could be flexibly reconfigured for various scenarios with low-latency requirements. The proposed latency-efficient parallel approach is also feasible to be extended to the implementation of real-time low-latency high-speed communication systems with a data rate of up to 100 Gbit/s or more potentially.

In summary, this thesis concentrates on the low-complexity DSP techniques and the optimization of the 2D IR beam-steered OWC systems by using the DSP techniques. Three challenges resulting from the limitation of the AWGR-based beam-steering spatial resolution, sample rate limitation of data converters, and speed limitation of FPGA are investigated, considering the requirements of the future indoor wireless network regarding high wireless connectivity density, high

capacity, low cost, low power consumption, and low latency. Besides the offline DSP, the real-time DSP based on FPGA implementation is also explored. All the proposed solutions are experimentally investigated.

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List of Symbols and Abbreviations

$1G$	First-generation
$2D$	Two-dimensional
$2G$	Second-generation
$3G$	Third-generation
$3GPP$	3rd Generation Partnership Project
$4G$	Fourth-generation
$5G$	Fifth-generation
$6G$	Sixth-generation
$ACO-OFDM$	Asymmetrically-clipped optical OFDM
ADC	Analog-to-digital converter
$AMPS$	Advanced Mobile Phone Service
APD	Avalanche photo-diode
API	Application programming interface
AR	Augmented reality
$ASICs$	Application-specific integrated circuits

AWG	Arbitrary waveform generator
AWGN	Additive white Gaussian noise
AWGR	Arrayed-waveguide grating router
BCH − codes	Bose-Chaudhary-Hocquenhem codes
BER	Bit-error ratio
C − RNN	Cascade recurrent neural network
CAP	Carrierless amplitude-phase modulation
CCC	Central communication controller
CDMA	Code-Division Multiple Access
CDPD	Cellular Digital Packet Data
CLB	Configurable logic block
CMOS	Complementary Metal Oxide Semiconductor
CNN	Convolutional neural network
CUDA	Compute unified device architecture
D − AMPS	Digital Advanced Mobile Phone Service
DAC	Digital-to-analog converter
DAE	Digital adaptive equalizer
DCO − OFDM	DC-offset optical OFDM
DD − LMS	Decision-directed least-mean-squares
DFB − LD	Distributed feedback laser diode
DFE	Decision-feedback equalizer
DML	Directly modulated laser
DMT	Discrete multitone
DPO	Digital phosphor oscilloscope
DSP	Digital signal processing

EA	Electrical amplifier
EDFA	Erbium-Doped fiber amplifier
EDGE	Enhanced Data Rates for Global Evolution
eMBB	Enhanced Mobile Broadband
ENOB	Effective number of bits
FDE	Frequency-domain equalizer
FDM	Frequency-division multiplexing
FEC	Forward error correction
FF	Flip-flops
FFE	Feed-forward equalizer
FFTs	Fast Fourier transforms
FIR	Finite impulse response
FMC	FPGA Mezzanine card
FPGA	Field-programmable gate array
FTN	Faster-than-Nyquist
GPRS	General Packet Radio Service
GPU	Graphics processing unit
GSM	Global System for Mobile Communications
HBT	Heterojunction bipolar transistor
HEW	High-efficiency wireless local area networks
HMDs	Head-Mounted Displays
IFFT	Inverse fast Fourier transform
IIR	Infinite impulse response
$IM-DD$	Intensity-modulated direct detection
InP	Indium Phosphide

IoT	Internet of Things
IP	Internet Protocol
IR	Infrared
$IrDA$	Infrared Data Association
ISI	Inter-symbol interference
ITU	International Telecommunication Union
$LDPC$	Low-Density Parity Check
$LEDs$	Light-emitting diodes
$Li-Fi$	Light fidelity
LMS	Least mean squares
LOS	Line-of-sight
$LSTM$	Long short-term memory
$LTE-A$	Long Term Evolution-Advance
LTE	Long Term Evolution
LUT	Look-up table
$M\&A$	Multiplication and addition
$m-CAP$	Multiband carrierless amplitude-phase modulation
$MEMS$	Micro-electro-mechanical system
$MLSE$	Maximum likelihood sequence equalizer
$mMTC$	Massive Machine Type Communications
$MMWC$	Millimeter-wave communication
MZM	Mach-Zehnder modulator
NMT	Nordic Mobile Telephony
NN	Neural network
NRZ	Non-return-to-zero

OC	Optical coupler
$OFDM$	Orthogonal frequency division multiplexing
$OFDMA$	Orthogonal frequency-division multiple access
OOK	On-off keying
OSA	Optical spectrum analyzer
OWC	Optical wireless communication
OXC	Optical cross-connect
$P-DD-LMS-DAE$	Parallel DD-LMS-DAE
$P-FIR$	Parallel FIR
$PAM-4$	4-level pulse-amplitude modulation
PAM	Pulse-amplitude modulation
PBC	Polarization beam combiner
$PIN-PD$	P-type/intrinsic/n-type photodiode
$PM-PHY$	Pulse modulation physical layer
PRA	Pencil radiating antenna
$PRBS$	Pseudo-random binary sequence
PtP	Point-to-Point
QAM	Quadrature amplitude modulation
QC	Quasi-cyclic
RAN	Radio access network
RAT	Radio/optical access technology
RC	Raise-cosine
$RCPC$	Rate-compatible punctured convolution
RF	Radio frequency
$RGB-LEDs$	Red, green, blue light-emitting diodes

RLS	Recursive least squares
$RM-codes$	Reed-Muller codes
$RS-codes$	Reed-Solomon codes
RZ	Return-to-zero
$S-DD-LMS-DAE$	Serial DD-LMS-DAE
$S-FIR$	Serial FIR
SCM	Subcarrier modulation
$SiGe$	Silicon-Germanium
$SLMs$	Spatial light modulators
SMF	Single-mode fiber
SNR	Signal-to-noise ratio
$SRRC$	Square-root-raised-cosine
SVM	Support vector machine
$TD-SCDMA$	Time Division-Synchronous Code-Division Multiple Access
TDE	Time-domain equalizer
$TDMA$	Time-Division Multiple Access
THz	Terahertz
TIA	Trans-impedance amplifier
TS	Training sequence
UHD	Ultra-high definition
$URLLC$	Ultra-Reliable Low Latency Communications
UV	Ultraviolet
VCO	Voltage-controlled oscillator
VL	Visible light
VLC	Visible light communication

$VNLE$	Volterra non-linear equalizer
VOA	Variable optical attenuator
VR	Virtual reality
$W-CDMA$	Wideband direct Code-Division Multiple Access
WDM	Wavelength-division multiplexing
$Wi-Fi$	Wireless Fidelity
$WiGig$	Wireless Gigabit
$WiMAX$	Worldwide Interoperability for Microwave Access
$WLAN$	Wireless local area networks
ZF	Zero-forcing

1 Introduction

"When wireless is perfectly applied, the whole Earth will be converted into a huge brain."

— Nikola Tesla —

This chapter firstly introduces the background of indoor wireless communication, followed by an overview of the emerging optical wireless communication (OWC) technologies for indoor and the digital signal processing (DSP) techniques for indoor OWC systems. Finally, the scope and contribution of this thesis are addressed.

1.1 Indoor wireless communication

1.1.1 Growing demand for indoor wireless communication

Wireless communication has greatly benefited our daily life due to its obvious mobility advantage. Without the restriction of wires, cables, or other physical connections, we are able to move freely and stay connected to the Internet anywhere anytime, getting a better experience of working, training, entertaining, and so on. Hence, wireless communication has become our main method of Internet connection. By 2021, more than half of 17 billion connected devices are mobile and 65% of the IP traffic comes from mobile devices [1]. The number will further increase since every connection to the user for the last meters is expected to be wireless. In addition, approximately 80% of the wireless data traffic originates or terminates indoors [2].

The demand for wireless communication is growing dramatically. On the one hand, the number of wireless devices and connections is increasing rapidly driven especially by the Internet of Things (IoT) phenomenon. IoT devices will account for 50% of all networked devices by 2023 [3]. IoT refers to a variety of physical devices (e.g. smart appliances, smart light-bulb, smartwatches, smart thermostats, etc.) around the world that are now connected to the Internet, all collecting and sharing data with sensors and wireless connections intelligently, such as smart home, smart wearable, environmental monitoring, etc. There are already more connected things than people in the world. According to the IoT statistics, more than 10 billion IoT-connected devices are seen worldwide in 2021 and the estimated number of active IoT devices will surpass 25.4 billion in 2030 [4]. On the other hand, the wireless traffic volume is seeing exploding growth due to the video applications. Video contents require much higher data rates and larger traffic capacity than other content. About 76% of global wireless bandwidth will be used for video delivery by 2025, according to the new annual Ericsson Mobility Report [5]. Applications such as ultra-high definition (UHD) video services (4K video and even 8K three-dimensional video), high-quality video conferencing, augmented reality (AR), VR, holographic imaging, etc., are growing rapidly in popularity, leading to a fast increase of wireless traffic volume. Especially, the COVID-19 pandemic has sped up the popularization of video meetings and other digital behaviors by working from home. The huge scale increase in the wireless traffic volume will have an enormous impact on the wireless networks, especially the indoor wireless networks since most of the wireless data traffic is generated indoors.

To cope with the booming demand for wireless communication, wireless communication technology is evolving rapidly. However, current indoor wireless networks, which mainly depend on radio wireless communication technologies, cannot adequately meet the quickly rising demand for wireless communication for indoor scenarios (e.g. residential homes, offices, hospitals, shopping malls, meeting rooms, public transport, etc).

1.1.2 Current indoor wireless networks and future requirements

Today's wireless communication in indoor environments is mainly supported by the Wireless Local Area Networks (WLAN) such as IEEE 802.11 Wireless Fidelity (Wi-Fi) and the public mobile communication/cellular networks such as 4G long-term evolution (LTE) and 5G networks.

- Historical evolution and future requirement of Wi-Fi

  As the most popular technology of WLAN, Wi-Fi plays a dominant role in indoor wireless communication due to its simplicity, high speed, cost-efficient, and mature standardization advantage, and has been continuously evolving for faster speed, wider coverage, lower cost, higher spectrum efficiency, and lower latency. Table 1.1 summarizes the milestones of Wi-Fi evolution on the main track of faster speed and the key specifications of the main standards.

  Wi-Fi was first released for customers in 1997 when a set of standards that define communication for WLAN called IEEE 802.11 [6] was created, and was introduced for home use in 1999 with the ratification of two improved standards named IEEE 802.11b and IEEE 802.11a. The IEEE 802.11b WLAN operates in the now crowded 2.4-GHz radio frequency (RF) band with complementary code keying modulation format, and improves the maximum data rate from 2 Mbit/s to 11 Mbit/s economically with an extended coverage range to 35 m indoors in comparison to the standard IEEE 802.11. IEEE 802.11a further increased the data rate to 54 Mbit/s by introducing the orthogonal frequency division multiplexing (OFDM) technique and moving to the less crowded 5-GHz RF band. However, somewhat smaller coverage and higher cost hindered its wide deployment. In 2003, IEEE 802.11g was introduced, combining the advantages of its predecessors, achieving a high data rate of 54 Mbit/s with coverage and cost comparable to IEEE 802.11b. It also operates at the 2.4-GHz RF band and is backward compatible with IEEE 802.11b.

Table 1.1: Milestones of the radio-based Wi-Fi evolution [6, 7]

Generation*	year	IEEE standard	RF band	Max. data rate**	Channel bandwidth	milestone
(Wi-Fi 0)	1997	802.11	2.4 GHz	2 Mbit/s	20 MHz	Released for customers
(Wi-Fi 1)	1999	802.11b	2.4 GHz	11 Mbit/s	20 MHz	Introduced for home use
(Wi-Fi 2)		802.11a	5 GHz	54 Mbit/s	5/10/20 MHz	Introduce OFDM
(Wi-Fi 3)	2003	802.11g	2.4 GHz	54 Mbit/s	20 MHz	Combining the advantages of its predecessors
Wi-Fi 4	2009	802.11n	2.4/5 GHz	600 Mbit/s (4 streams)	20/40 MHz	Introduce MIMO
Wi-Fi 5	2013	802.11ac	5 GHz	6.9 Gbit/s (8 streams)	20/40/80/160 MHz	Introduce beam-forming
Wi-Fi 6	2019	802.11ax	2.4/5 GHz	9.6 Gbit/s (8 streams)	20/40/80/160 MHz	Introduce OFDMA
Wi-Fi 6E	2020		2.4/5/6 GHz			Introduce 6-GHz band
Future Wi-Fi 7	2024	802.11be	2.4/5/6 GHz	$>$ 30 Gbit/s (16 streams)	$>$ 320 MHz	Real-time communications (required latency $<$ 5ms)

* In 2018, the Wi-Fi Alliance renamed the used Wi-Fi versions for easier understanding. Wi-Fi 4 - 6 are officially labeled, Wi-Fi 0 - 3 are common usage, not an official branded numbering.

** It is the aggregate data rates, to be shared among a number of users. So the data capacity per user decreases when more users need a connection.

In 2009, a more advanced Wi-Fi standard named IEEE 802.11n or Wi-Fi 4 was introduced. It supports a theoretical maximum data rate of 600 Mbit/s by employing the MIMO technique with an antenna array (up to 4 spatial streams) and operates in both the 2.4-GHz and 5-GHz RF bands with a maximum channel bandwidth of 40 GHz.

In 2013, the currently prevalent version of Wi-Fi standard IEEE 802.11ac (Wi-Fi 5) was published with a maximum data rate up to 6.9 Gbit/s and doubled channel bandwidth up to 80 MHz and optional 160 MHz in the 5-GHz RF band, enabled by scaling up the constellation order of quadrature amplitude modulation (QAM, from 64-QAM to 256-QAM), adding more spatial streams (up to 8) and employing the beam-forming technique.

The latest more advanced IEEE 802.11ax (Wi-Fi 6) which is also labeled as a High-Efficiency WLAN (HEW) was proposed in 2019 and the 6-GHz RF band was added for Wi-Fi 6E in 2020. By collecting the state-of-art radio technologies, further upgrading 256-QAM to 1024-QAM, and introducing the orthogonal frequency-division multiple access (OFDMA) technique, the maximum data rate of Wi-Fi 6 reaches up to 9.6 Gbit/s with a 75% latency reduction in comparison to the Wi-Fi 5. Globally, 66.8% of the WLAN endpoints will be equipped with Wi-Fi 5, while Wi-Fi 6 will account for 27.4% by 2023 [3].

The future Wi-Fi 7 [7] aims at increasing the data rate to at least 30 Gbit/s for improving user experience (e.g., when watching 8K video with an uncompressed rate of 20 Gbit/s) and providing real-time communications with the required latency below 5 ms for gaming.

- Historical evolution and future requirement of Mobile communication

  Mobile communication/cellular network is offloading the heavy traffic of indoor wireless communication. Since its origination in early 1970, it is evolving rapidly and re-branding every decade, from 1G, 2G, 3G, and 4G to the upcoming 5G, and even the future 6G. Table 1.2 has summarized the timeline of the mobile communication/cellular network evolution and some key specifications.

Table 1.2: Timeline of mobile communication evolution [8, 9].

Generation	Period	Key technologies	Frequency band	Max. data rate	Bandwidth	Breakthrough
1G	1980s	NMT, AMPS, CDPD (analog)	800 MHz (analog signal)	2 Kbit/s	30 kHz	Foundation of Mobile (support voice only)
2G (& 2.5G & 2.75G)	1990s	GSM, D-AMPS, GPRS, EDGE	0.85 - 1.9 GHz	473 Kbit/s	1.25 MHz	Digital communication; Messages, simple data; International roaming
3G (&3.5G & 3.75G)	2000s	W-CDMA, CDMA 2000 TD-SCDMA	0.8 - 5.8 GHz	30 Mbit/s	10 MHz	Mobile broadband (support multimedia .ect)
4G	2010s	WiMAX LTE, LTE-A	2 -8 GHz	100 Mbit/s; 1 Gbit/s	100 MHz	Mobile ultra-broadband; All IP-based
5G	2020s	5G-NR	0.6 - 0.9 GHz 1.7 - 4.7 GHz 24 - 54 GHz	20 Gbit/s (DL) 10 Gbit/s (UL)	100 MHz 400 MHz 1 GHz	mm-Wave communication; eMBB, URLLC, mMTC; Low latency at 1-ms level; High connectivity density 10^6 devices/km^2
Future 6G	2030s			1 Tbit/s	>1 GHz	Unprecedented applications; Required latency < 0.1-ms, ×10/×100 energy efficiency, ×10 connectivity density

The first-generation (1G) mobile communication was completed in 1984, supporting basic mobile voice by analog signals with a speed of 2 Kbit/s. 1G is based on analog frequency modulation systems, including three main technologies known as Nordic Mobile Telephony (NMT), Advanced Mobile Phone Service (AMPS), and Cellular Digital Packet Data (CDPD). However, it has low capacity, bad voice links, and poor security, and it is unavailable for global roaming services.

The second-generation (2G) mobile communication started in 1991 was the first digital cellular network. It comprises systems such as Global System for Mobile Communications (GSM), digital AMPS (D-AMPS), General Packet Radio Service (GPRS), and Enhanced Data Rates for Global Evolution (EDGE), using multiplexing techniques of Time-Division Multiple Access (TDMA) and Code-Division Multiple Access (CDMA). By replacing analog technology with digital communication, 2G offers improved sound quality, better security, and the capability of international roaming. In addition to the traditional voice services, it also provides services such as text messaging, picture messaging, and simple Web browsing, but the achieved data rate is smaller than 0.5 Mbit/s.

The third-generation (3G) mobile communication is based on the International Telecommunication Union (ITU) family of standards under the International Mobile Telecommunications program, IMT-2000. It is a CDMA-based generation with key technologies known as wideband direct CDMA (W-CDMA), CDMA 2000, and Time Division-Synchronous CDMA (TD-SCDMA). 3G provides a higher data rate of up to 30 Mbit/s and supports multimedia applications (e.g. full-motion video, video conferencing, and internet access).

The current fourth-generation (4G) mobile communication is a collection of wireless standards, including key technologies such as Worldwide Interoperability for Microwave Access (WiMAX)/802.16m standardized by the IEEE, Long Term Evolution (LTE), and LTE-advance (LTE-A) standardized by the 3rd Generation Partnership Project (3GPP). A 4G system is based on an all-IP (Internet Protocol) packet-switched network and provides capabilities defined by ITU in IMT Advanced, aiming at peak data rates of up to approximately 100 Mbit/s for high mobility and up to approximately 1 Gbit/s for low mobility, and supporting applications such as amended mobile web access, IP telephony, gaming services, high-definition mobile TV, video conferencing, and 3D television.

The latest fifth-generation (5G) mobile communication provides a new approach giving ubiquitous connectivity and a far more outstanding performance than the previous generations of mobile communication. In addition to the sub - 6 GHz frequency band, 5G technologies introduce the millimeter-wave (24 - 54 GHz) for a larger bandwidth. Unlike the previous generations, 5G expands traditional mobile broadband to a variety of services such as Industry 4.0, VR, and IoT. To support applications categorized as Enhanced Mobile Broadband (eMBB), Ultra-Reliable Low Latency Communications (URLLC), and Massive Machine Type Communications (mMTC), 5G networks are expected to achieve a high data rate of up to 20 Gbit/s for downlink and 10-Gbit/s for up-link, ultra-low user plane latency in the 1-ms level, high-density connectivity of 10 to 100 times more connected devices (capability to support up to 1 million devices per square kilometer (km^2)), and a low energy-consumption of $> 90\%$ reduction in comparison to the 4G networks [10].

The future sixth-generation (6G) mobile communication is planned for many unprecedented application scenarios such as holographic-type communication, extended reality, tactile Internet, multi-sense experience, digital twin, pervasive intelligence, intelligent transport logistics, and enhanced onboard communications in 2030 and beyond. More stringent requirements are foreseen for the 6G networks. For example, 6G is expected to achieve a peak data rate up to 1 Tbit/s, a reduced latency at the 100-μs level, 10 times higher connectivity density, and improved energy efficiency of 10 to 100 times in comparison to the 5G networks [9].

To conclude, the data rate of the radio-based Wi-Fi witnessed a dramatic increase from 2 Mbit/s to almost 10 Gbit/s, benefiting from wider channels and higher spectrum efficiency with the adoption of advanced modulation schemes, spatial multiplexing such as MIMO, beam-forming techniques, etc. It is notable that these Wi-Fi data rates are aggregated data rates, to be shared among a number of users. So the data capacity per user will decrease when more users need a connection. More than 30 user devices will be connected to an access point in a high-density environment [11]. The mobile communication/cellular network is also evolving every decade for higher capacity from sub-Mbit/s to the maximum 20 Gbit/s and expands the mobile communication services from simple phone calls to a variety of services such as Industry 4.0, VR, and IoT. Also, the 5G cellular network is capable to support a high connectivity density of up to 1 million connected devices per square kilometer (km^2). Moreover, the 5G

cellular network has achieved convergence with Wi-Fi which was not completed in the 4G cellular network. Future Wi-Fi 7 is planned to improve user experience (e.g., when watching 8K video with an uncompressed rate of 20 Gbit/s, and real-time communications with the latency below 5 ms for gaming) [7] and future 6G mobile communication will realize many unprecedented user scenarios (e.g., holographic-type communication, extended reality, tactile Internet, multisense experience, digital twin, pervasive intelligence, intelligent transport logistics, and enhanced onboard communications) [9]. Thus, more stringent technical requirements regarding higher data rate, lower latency, higher connectivity density, higher energy efficiency, etc., are proposed for the future indoor wireless networks.

However, the future requirements are challenging traditional radio wireless communication. The intrinsically limited radio spectrum is getting more and more congested driven by the ongoing growth of wireless traffic, and the interference issues are reducing the total throughput. In addition, real-time traffic is very sensitive to congestion and interference, which can increase delays in the network. Moreover, the required higher connectivity density put high demand for smaller wireless cells. Therefore, advanced technologies are needed to support the stringent requirements of indoor wireless networks.

1.1.3 Future indoor wireless networks with advanced technologies

Various promising technologies have been suggested. One of the powerful solutions to catch up with the exponentially growing wireless traffic and tackle the exhausting spectrum problem of traditional radio wireless communication is to open up new spectra with enormous bandwidth. New radio spectrum such as millimeter-wave (from 30 GHz to 300 GHz) has been exploited for providing high-capacity links. Millimeter-wave communication (MMWC) has been applied in 5G mobile cellular networks [12] and WLAN such as Wireless Gigabit (WiGig, e.g. 60-GHz based IEEE 802.11ad - 2012) [13]. However, because of the higher propagation loss, millimeter-waves (e.g. 60-GHz band, for indoor use) have a more limited range, requiring many small cells for the coverage of a certain area. Also, they can be impeded or blocked by materials in walls or windows, hence, MMWC is mainly for the short-reach direct line-of-sight (LOS) scenarios. Moving away from the RF region, Terahertz (THz, from 0.1 THz to 10 THz, which is known as the "terahertz tap") carriers are also being investigated for broadband wireless communication, however, significant challenges still exist both from the device and communication perspectives [14]. Exceeding the THz bands, the

optical spectra including the visible light (VL) and infrared (IR) regions offer hundreds of THz unregulated bandwidth. It will undoubtedly provide a promising alternative to combat the bandwidth crisis in the radio spectrum. As stated by the Friis equation, higher radio frequencies also require more directive antennas to achieve a certain link power budget. Directive (optical) antennas are much easier to realize in beam-steered OWC, by means of passive optics. Optical wireless communication (OWC) technologies are being investigated widely. Visible light communication (VLC) has taken advantage of the light-emitting diodes (LEDs)-illumination systems and has been applied in the network known as light fidelity (Li-Fi) [15] with already commercialized VLC products, while IR OWC can take advantage of the available devices developed for the optical fiber systems and benefit from the fiber indoor backbone network. In particular, IR beam-steered OWC technology is foreseen to provide ultra-high capacity to individual users, which is a powerful solution for wireless traffic explosion. More details about the OWC technologies for indoors are introduced in the next subsection.

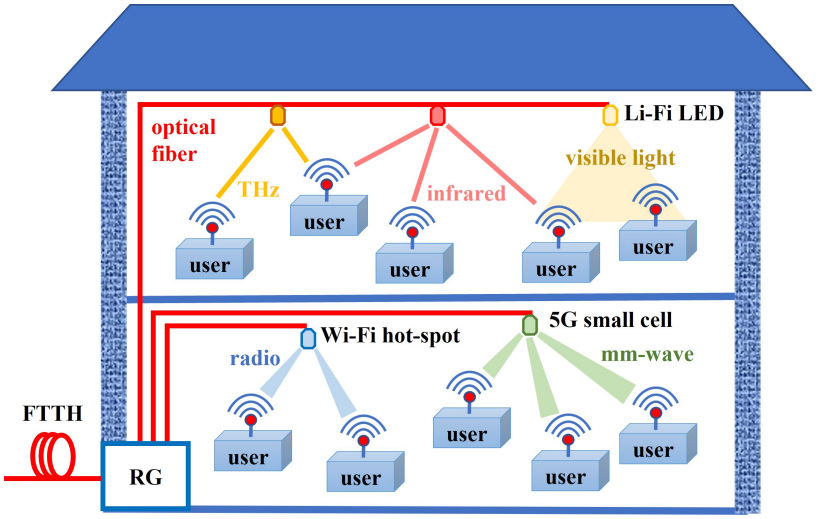

Figure 1.1: Future converged fiber-wireless indoor network with advanced technologies. FTTH: Fiber to the home; RG: residential gateway.

Hence, the future indoor wireless networks will inevitably take advantage of the technologies based on the high-frequency bands (millimeter-wave, THz, optical spectrum), which brings abundant bandwidth, providing ultra-high capacity. However, similar to MMWC, THz communications and OWC also suffer from

high path loss and LOS-dependency, thus providing limited coverage. Consequently, the emerging advanced technologies will not replace traditional radio wireless communication, but will be a powerful supplement to offload the heavy broadband traffic loads from the exhausted radio spectrum. Therefore, the future indoor wireless networks will provide a good capability of heterogeneous radio/optical access technology (RAT), where the legacy RAT with low radio frequencies and the LOS-dependent RATs (MMWC, THz, IR OWC, and VLC) can co-exist well, as shown in Figure 1.1. Similar to the introduction of millimeter-wave in the 5G networks, THz, IR OWC, and VLC may construct a new layer in the hierarchical radio access network (RAN) architecture (e.g., picocells), where heterogeneous cells with different RAT are overlaying each other [9]. The picocells architecture can be effectively supported by the converged fiber-wireless network solution with a central site (e.g. the residential gateway) in a cost-efficient way [16].

1.2 Optical wireless communication technologies for indoor

Optical wireless communication (OWC) is attracting a lot of interest as a supplement to the traditional radio wireless connection for the indoor network, since 1) it can provide a wealth of license-free spectrum which offers hundreds of THz bandwidth; 2) it does not cause electric-magnetic interference and thus can be used in RF-restricted areas such as hospitals; 3) it features enhanced privacy and security as light does not penetrate walls; 4) it is suitable for creating smaller cells which enables higher-density spectrum reuse, etc. However, OWC also has limitations such as 1) it covers a relatively short range, usually a few meters with a single access point; and 2) it is susceptible to connectivity loss due to obstructions. Thus, it is intended for short-reach and LOS links. Consequently, OWC will not replace radio wireless communication, but will be a powerful supplement offloading the heavy broadband traffic loads from the congested radio-based indoor wireless networks.

OWC refers to wireless communication technologies which utilize optical carriers in the ultraviolet (UV), visible light (VL), or infrared (IR) region of the electric-magnetic spectrum. The optical spectrum window is illustrated in Figure 1.2. UV is rarely used in indoor scenarios due to eye safety issues and a lack of suitable sources and detectors. Thus, indoor OWC mainly contains two categories: visible light communication (VLC) and IR OWC.

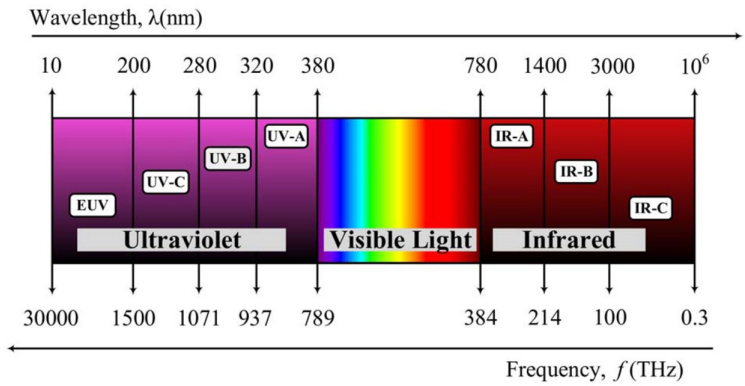

Figure 1.2: Optical spectrum window [17].

1.2.1 Visible light communication

VLC uses visible light as the carrier for information streams. The spectrum of visible light spans a range from 380 nm to 780 nm, offering a huge bandwidth up to 400 THz. From the historical perspective, visible light was used for communication from ancient times by using beacon fires, smoke signals, or reflected sunlight for transmitting messages. The prototype of the modern VLC system originated in 1880 when the first VLC device known as the photophone [18] was invented by Alexander Graham Bell using various lamps as light sources. However, VLC started progressing more significantly only after the invention of compact LEDs in the 1960s [19]. The idea of illumination and data transmission simultaneously by using white-LED was first proposed for the wireless home link in 2000 [20]. Thenceforth, VLC gained more interest and became sufficiently mature to be standardized by IEEE 802.15.7 working group in 2011. The networked version of VLC is known as Li-Fi [15], for which standardization has been started by IEEE 802.11 LC study group, aiming for higher capacity.

VLC works by switching the current to the LEDs off and on at a very high speed, fast enough to be imperceptible by the human eyes. In the VLC systems, phosphor-based white LEDs or red, green, blue LEDs (RGB LEDs) are used as data transmitters, while a p-type/intrinsic/n-type (PIN) diode, avalanche photo-diode (APD), or optical camera can be utilized as optical receivers.

As the LEDs are increasingly being used for illumination, the VLC systems can make use of the LED illumination infrastructure, which is cost-efficient. However, VLC requires the illumination system to be switched on when unnecessary (e.g. daytime), which costs extra energy. Moreover, the white LED used in

illumination systems has intrinsically limited bandwidth. Advanced spectrum-efficient modulation techniques are needed to achieve data rates beyond 1 Gbit/s. A peak data rate of 9.5 Gbit/s was achieved over 1 m in a multi-color LED VLC system by using orthogonal frequency division multiplexing (OFDM) and wavelength-division multiplexing (WDM) techniques [21].

1.2.2 Infrared optical wireless communication

IR OWC commonly utilizes the infrared spectrum centered at 850 nm (353 THz), 1310 nm (229 THz), and 1550 nm (193 THz), in a Point-to-Point (PtP) configuration. Infrared light communication has already proven its huge potential in optical fiber networks which mainly utilize the infrared spectrum roughly from 1460 nm to 1625 nm (S+C+L bands, 20.9-THz bandwidth). Free-space IR OWC may take advantage of the treasure of mature high-speed optical devices (laser diodes, photo-detectors, optical modulators, etc.) already developed by optical fiber systems, which is cost-efficient. In addition, the IR OWC is inherently compatible with the converged fiber-wireless network solution, as the modulated optical signals can be delivered to remote optical access points via fiber and directly transmitted to users through free space. Different from optical fiber communication, free-space IR beams do not experience wave-guiding, hence can offer a higher bandwidth together with a 50% lower latency than silica fiber [22].

IR OWC was first proposed for short-reach wireless communication more than four decades ago. In 1979, F.R.Gfeller and U.Bapst proposed in-house infrared communication via a diffuse beam operating at 950 nm and achieved 1 Mbit/s [23]. The concept was further explored for in-building applications [24]. The achieved data rates remain in the order of Mbit/s until the early 90's and broke through 1 Gbit/s successfully in 1996 by BT Labs [25]. The Infrared Data Association (IrDA) standard [26] was formed in 1993, providing specifications for a complete set of protocols for wireless infrared communications over the "last one meter". The standard was then widely adopted for short-reach infrared wireless communication.

In comparison to the LED-based VLC, IR OWC has a larger link budget according to the eye safety regulations. The eye safety standards (e.g. IEC 60825 and ANSI Z136) allow free-space infrared optical beams at wavelengths beyond 1400 nm to carry power up to 10 mW, whereas only a few tenths of mW is allowed for visible light [27]. Moreover, the infrared light can be easier confined to narrow beams which are suitable to establish pico-cells to provide unshared connections with inherently better privacy, exclusive high capacity,

and high-efficiency power consumption [22].

- High-capacity 2D IR beam-steered OWC system

  By means of optical elements such as lenses and mirrors, infrared beams can be collimated into small cross-sections and stay narrow over a long reach. By using beam steering techniques, the narrow infrared beams can be directed only to the intended destination and serve the individual user device (such as your laptop, phone, or smart TV) when needed. Thus, you can enjoy the high-speed dedicated lane for video streaming, internet browsing, and file exchange without congestion and privacy disclosure. Also, it is power-efficient since the infrared beam directs its power only to the intended destination without power spoiling elsewhere. In addition, the high directivity results in a better signal-to-noise ratio (SNR) since a significantly large fraction of the signal power emitted by the transmitter is received by the users. Consequently, the link with narrow beams can carry a significantly high capacity [22] due to the increased SNR and high bandwidth of the infrared wireless link, according to the Shannon's Law which concludes the maximum attainable capacity of a power-constrained bandwidth-limited continuous-time additive white Gaussian noise (AWGN) channel as $C = B \cdot \log_2(1 + SNR)$ where B is the channel bandwidth [28]. Different from the Wi-Fi router whose capacity is shared among all the wireless devices in the covered rooms, the high capacity of the IR beam-steered OWC system is unshared for only one dedicated user device. Once the user device is connected, there is no competition for capacity with other devices.

  In order to address the user devices, accurate agile two-dimensional (2D) beam steering is proposed. 2D IR beam-steered systems have been developed with actively controlled devices such as micro-electro-mechanical system (MEMS)-based mirrors [29], and spatial light modulators (SLMs) [30, 31]. Each beam can carry >10 Gbit/s data with both solutions. However, scaling up for multiple beam systems is complex and challenging by using MEMS- or SLM-based steerers since each beam requires an active steering element with separate control signals.

  To address this problem, passive steering elements are employed. Recently, a wavelength-controlled 2D beam-steered scheme using passive crossed diffractive elements based on two orthogonal gratings was proposed and experimentally demonstrated [32, 33]. The beam steering was achieved

by just tuning the wavelength of each beam remotely. The system can be easily scaled up to many beams only by adding wavelengths in the remote central controller. Thus, the beam-steerer on the local side can be more compact, power-efficient, and reliable. By using discrete multitone (DMT) modulation, the system achieved more than 42 Gbit/s per beam [34]. Another alternative passive beam steering module based on a high port-count arrayed waveguide grating router (AWGR) was also proposed for the wavelength-controlled 2D IR beam-steered system [35]. More details about the AWGR-based 2D IR beam-steered system are introduced in Chapter 3. The AWGR-based beam steering is easier for assembling and requires less alignment effort. It has been experimentally demonstrated with a data capacity of up to 112 Gbit/s per beam by using 4-level pulse-amplitude modulation (PAM-4) modulation format and DSP techniques [36]. More details about DSP are introduced in the next subsection.

1.3 Digital signal processing techniques for indoor OWC

Low-complexity high-efficiency DSP plays an important role in indoor OWC systems [21, 34, 36, 37] since it significantly improves the spectrum efficiency and signal quality, which further boosts the system capacity at a cost-efficient manner. DSP techniques permit spectrum-efficient digital modulations (e.g. PAM-4, DMT, OFDM, etc.) which significantly reduce the signal bandwidth and provide compensation for various kinds of distortions caused by bandwidth-limited channels (e.g. the low-frequency response of LEDs, the capacitance of large area photo-diodes), relaxing the requirements for expensive high-bandwidth optoelectronic devices, thus reduce the overall cost.

1.3.1 Digital signal processing algorithms

DSP techniques have been widely used in traditional radio wireless communication, but it was introduced into optical communication until high-speed data converters commensurate with the optical line rate emerged. The first commercial deployment of DSP for optical communication was the pre-equalization of chromatic dispersion and non-linearity at a 10-Gbit/s intensity-modulated direct detection (IM-DD) transceiver for a fiber transmission system in 2005 [38]. After that, 40-Gbit/s coherent transceivers were developed with phase and polarization tracking realized in the digital domain [39], which is now standard for long-haul fiber transmission systems. In terms of short-reach OWC systems for

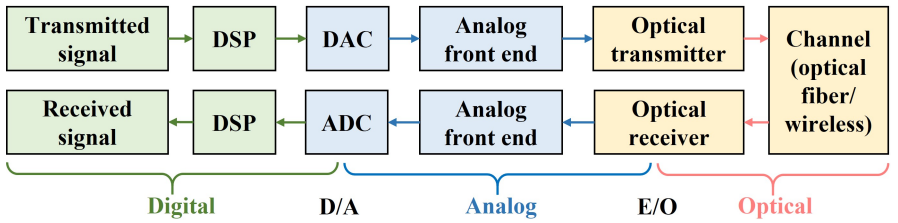

Figure 1.3: Block diagram of an optical communication system with DSP. DSP: Digital signal processing; DAC: digital-to-analog converters; ADC: analog-to-digital converters.

cost- and power-sensitive indoor networks, the IM-DD scheme is more appealing due to the lower cost and complexity [40].

High-speed data converters including digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) are the gateway for introducing DSP to optical communication systems. As Figure 1.3 shows, the transmitted data bits are processed digitally and converted into analog signals by using DACs, then the analog signals are processed and modulated onto the optical carriers before being transmitted to the optical fiber or optical wireless systems. The receiver is mirroring the operation of the transmitter. After the optical to electrical conversion, the electrical signals are processed and converted into digital signals by using ADCs.

The state-of-the-art DACs and ADCs have a bandwidth lower than the nowadays optoelectronic devices and a sample rate lower than the optical line rate. To avoid complicated interfaces, Complementary Metal Oxide Semiconductor (CMOS)-based data converters are preferred since DSP algorithms are normally implemented in CMOS technology. In 2021, a state-of-the-art DAC fabricated in 28-nm CMOS technology was reported. It achieves a 10-GSa/s sample rate with a 5-GHz bandwidth and a 14-bit resolution [41]. Also, a state-of-the-art ADC implemented in the 40-nm CMOS technology and features a 5-GSa/s sample rate 360-MHz bandwidth is reported in 2022 [42]. However, the indoor OWC systems have moved from 10-GBaud/s IM-DD OOK system [43] to 56-GBaud/s IM-DD PAM-4 system [36], and the next-generation optical transceivers are even evolving toward 200 Gbit/s per lane IM-DD system [44]. The efficient techniques enabling the utilization of DACs and ADCs in optical communication are time-interleaving and frequency-interleaving/spectral slicing using multiple sub-DACs or sub-ADCs. By using these techniques, current high-speed CMOS data converters fabricated in the 16-nm FinFET process technology can achieve sample

rates of up to 128 GSa/s with 8-bit nominal resolution at an average effective number of bits (ENOB) of 5.5 bits [45]. These techniques have also been used in the high-end arbitrary waveform generator and real-time oscilloscopes for the experimental investigation of optical communication.

DSP mainly takes charge of coding, digital modulation, pulse shaping, equalization, and synchronization.

- Coding

  Coding mainly contains source coding, channel coding, and line coding. Source coding (data compression) removes unwanted redundancy of the raw data for higher bandwidth efficiency, while channel coding (error control coding) adds redundancy to the transmitted data for error detection and correction. Forward error correction (FEC) coding is one of the most widely used error control techniques. There has been a lot of effort in the research of FEC coding techniques, aiming to improve communication reliability with fewer transmission errors. FEC codes not only detect the errors but also correct the errors. Generally, the FEC codes can be categorized into block codes that encode information bits into blocks (e.g. Hamming codes, Reed-Muller (RM) codes, Reed-Solomon (RS) codes, and Bose-Chaudhary-Hocquenhem (BCH) codes), convolutional codes which are not encoded in blocks but are encoded relying on a linear combination of previous bits, and a concatenation of these codes. Remarkably, state-of-the-art techniques are mainly based on the turbo codes developed by parallel concatenating convolutional code blocks and the Low-Density Parity Check (LDPC) codes which is a class of linear block codes with a sparse parity-check matrix. They have better error-correction performance but high complexity. Recently, polar codes which have lower complexity attract lots of attention [46, 47, 48]. The LDPC codes and polar codes have been adopted in the 5G cellular networks as the coding scheme of user data and control link, respectively [49]. Many advanced coding schemes based on the modified FEC techniques have been proposed for indoor OWC systems. As a VLC system also takes charge of illumination, the FEC coding schemes need to adapt to the changing SNR that results from dimming, and to take care of the burst errors that results from flickering, for which large numbers of advanced FEC codes such as modified RM codes, rate-compatible punctured convolution (RCPC) codes, and quasi-cyclic (QC) LDPC codes are proposed [50]. Whereas, the IR OWC does not need the dimming control. The FEC coding schemes improve the communication

reliability at the cost of lower spectral efficiency, for which the coded modulation techniques were proposed. Coded modulation combines the FEC coding and higher-order modulation, enabling a spectral-efficient robust transmission system.

Line coding converts the binary data into digital signals suitable for transmission, providing bit clock recovery possibility and error detection capability. With line coding, the binary '0' and '1' are represented in various serial-bit signaling formats, including two major basic categories: return-to-zero (RZ) and non-return-to-zero (NRZ). Based on the signal levels assigning regulation, line coding can be further classified as unipolar signaling, polar signaling, bipolar signaling, Manchester signaling, and differential signaling. Line coding is also a kind of digital baseband modulation. The unipolar NRZ signal is also known as the widely used on-off keying (OOK) in indoor OWC systems. An efficient and practical line coding technique is nBmB which encodes a group of binary data (of length n) into another group (of length m) of binary data, and nBmT which encodes a group of binary data (of length n) into another group (of length m) of ternary data, where $m > n$. For example, 8B10B line coding has been adopted in the current pulse modulation physical layer (PM-PHY) for OWC, as defined in the IEEE P802.15.13 task group [51]. 64B67B line coding was also proposed as an optional high-speed mode to the PM-PHY specification in IEEE P802.15.13 [52].

- Digital modulation

  Digital modulation provides the possibility of using high-order modulation formats which enables tremendous capacity growth by introducing multiple dimensions for carrying information. By using high-order modulation formats, more information bits can be coded into the electrical signal waveform before being modulated onto the optical carriers. Digital modulation for indoor OWC mainly includes single-carrier modulations and multi-carrier modulations. Different from the optical fiber and RF systems, the modulation formats suitable for indoor OWC systems should be power-efficient because of the transmission power restriction due to the eye safety regulations, thus single-carrier modulations attract more interest. Pulse amplitude modulation (PAM) is a simple modulation technique widely used in indoor OWC systems [36, 31], in which OOK is the simplest type of PAM. The more spectrum-efficient modulation formats such as quadrature amplitude modulation (QAM), carrierless amplitude-phase

modulation (CAP), and DMT are other promising modulation formats that can be employed in indoor OWC systems [53, 54, 34, 55]. Multi-carrier modulation such as subcarrier modulation (SCM) and OFDM has also been applied in indoor OWC systems for higher data rate but are less power-efficient [56, 21]. More details about the modulation format including PAM, QAM, CAP, DMT, SCM, and OFDM are explained in Chapter 2.

- Pulse shaping

  Pulse shaping controls the spectrum of transmitted signals to improve spectral efficiency and reduce inter-symbol interference (ISI). Signals transmitted through bandwidth-limited channels get smeared out in the time domain, resulting in ISI which degrades the performance of a communication system. Pulse shaping based on the Nyquist zero-ISI criterion can achieve ISI-free transmission ideally. In addition, the pulse-shaped signals have a narrower spectrum occupation with a high out-of-band suppression, reducing the adjacent channel crosstalk of multiplex systems. Pulse shaping is realized by specially-designed spectral masks (Nyquist filters). The widely used practical Nyquist filters are the raise-cosine (RC) filter and square-root-raise-cosine (SRRC) filter pairs which consist of a pulse-shaping filter on the transmitter side and a matched filter on the receiver side. The Nyquist pulse shaping technique is explained in Chapter 3 in detail.

- Equalization

  Digital equalization, including pre-equalization in the transmitter and post-equalization in the receiver, compensates for the impairments in the channel. The channel impairments of the indoor OWC systems are mostly caused by 1) bandwidth-limited devices for high-speed transmission, 2) multipath propagation in diffuse links, 3) background radiations from non-signal free-space light, 4) LOS blocking, etc. Equalization in the digital domain avoids the utilization of costly optical compensating modules. In the simplest case, digital equalization is based on filters that have the inverse characteristics of the channel response. It can be static filters depending on the pre-estimated channel response, or adaptive filters that can track and calibrate the channel variations in real-time. An overview of the equalization techniques is given in Chapter 2.

- Synchronization

Synchronization ensures the clock of transmitter and receiver operating at the same rate, reduces the sampling timing errors, and makes clear where the information units start which is essential to recover the transmitted digital signals. Three basic types of synchronization for digital communications are carrier synchronization, symbol/bit synchronization, and frame synchronization. Different synchronization techniques are required according to the employed modulation schemes.

1.3.2 Hardware implementation of DSP algorithms

DSP algorithms are usually employed for experimental investigation in an offline way. Offline DSP is normally performed with Matlab simulation, which is convenient for algorithm development and customization for specific channels. However, offline processing does not consider the feasibility and limitation of the speed/throughput, latency, precision, resource/area utilization, and power consumption for hardware implementation of DSP algorithms. Therefore, real-time DSP based on hardware implementation is developed for feasibility verification, performance estimation, and experimental investigation/real-time demonstration, which is also an important step toward commercial roll-out.

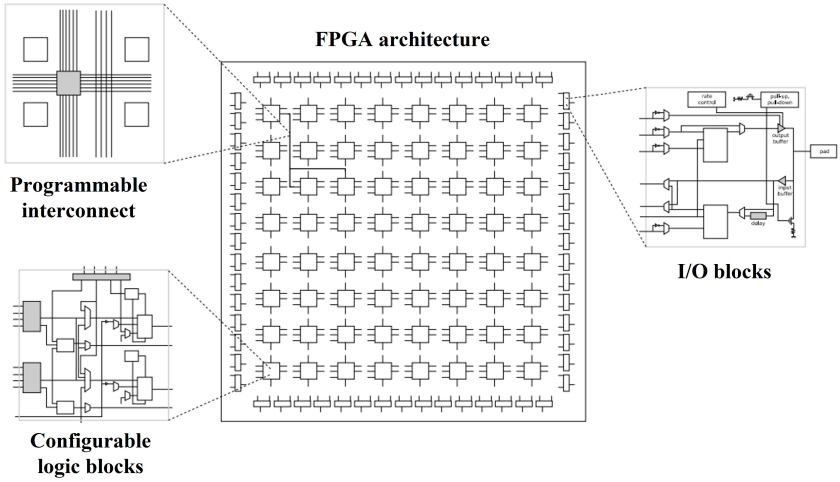

Figure 1.4: Simplified FPGA architecture.

Commercial application-specific integrated circuits (ASICs) with DSP capabilities are now available for high-capacity optical transmission systems, but the ASIC-based DSP algorithms cannot be customized dynamically for the optical

Table 1.3: Comparison of three real-time DSP implementation methods.

Platform	ASIC	FPGA	GPU
Parallel processing	Support	Support	Support
Power efficiency	High	Low	Low
Flexibility for reconfiguration	Low	High	High
Flexibility for possible circuits	High	Medium	Low
Development effort & cost	High	Medium	Low
Development time	Long	Medium	Short
Possibility for fully-integration	High	Medium	Low

transmission systems with various requirements. DSP implemented based on ASIC has the advantages of superior power efficiency and the possibility of developing fully-integrated cost-efficient compact products. However, the ASIC design suffers from prohibitively high development effort, high fabrication cost, and long development time, which is not suited for research. Therefore, many real-time DSP for optical transmission demonstrations are based on the field-programmable gate array (FPGA) design [57, 58, 59, 60, 61]. FPGA is suitable for research since it is flexibly reconfigurable for DSP algorithms customization, relatively cost-efficient, and time-efficient for DSP algorithms implementation. Different from ASIC which draws the circuits permanently into silicon, FPGA makes the functional circuits by connecting the configurable logic blocks (CLBs) with programmable interconnect, as shown in Figure 1.4. In recent years, the general-purpose graphics processing unit (GPU) is becoming another real-time implementation method of DSP algorithms for optical transmission systems [62, 63, 64, 65] due to its enhanced parallel processing and high throughput capabilities. GPU-based real-time DSP development requires relatively shorter development times since it can be implemented using compute unified device architecture (CUDA) which is a $C++$ application programming interface (API) and provides many pre-defined routines such as fast Fourier Transforms (FFTs), facilitating the DSP implementation. Also, GPU-based DSP implementation does not require stringent timing constraints and hardware resource management which are important for the FPGA-based DSP implementation. However, GPU has relatively less flexibility than FPGA because FPGAs consist of plenty of logic blocks that can perform any digital implementation desired by the developer, whereas the GPU reprogramming capabilities are restricted by the software-determined data flow. Both FPGA and GPU platforms can be

used for real-time demonstrations, but FPGA design is more compatible with ASIC design for fully integration as they both use hardware design languages. DSP algorithms are normally tested and optimized on the FPGA platform before the expensive and unchangeable ASIC implementation. A comparison of these three real-time DSP implementation methods is summarized in Table 1.3. FPGA is utilized for real-time DSP implementation in this thesis. More details are addressed in Chapter 5.

1.4 Scope and contribution of this thesis

The future indoor wireless networks will be fiber-wireless converged picocell-based with heterogeneous wireless access technologies including but not limited to the traditional RF and the emerging OWC technology. It is expected to realize seamless wireless coverage with the capability to meet the following requirements [16, 22]:

- **High connectivity density**. The number of wireless devices and connections is increasing rapidly driven by the popularization of smartphones and the IoT phenomenon. 5G network is capable to support a high connectivity density of up to 1 million connected devices per square kilometer (km^2) [10], and a 6G network is expected to support 10 times higher connectivity density [9]. Smaller wireless cells are required to achieve higher connectivity density.

- **High capacity**. To cope with the booming wireless data traffic caused by the increase of connected wireless devices and the popularization of the emerging data-rate-hungry applications such as UHD video services, VR/AR, and holography imaging, the indoor wireless networks are expected to have higher and higher data capacity/data rate. For example, a typical modern Head-Mounted Displays (HMDs), for instance, Oculus Rift CV1, has a resolution of 1080 × 1200 (1,296,000) per eye and a refresh rate of 90 Hz, resulting in an uncompressed data rate of about 5.3 Gbit/s [66]. Moreover, as reported in [67], the data rate demand of a hologram system will even exceed 1 Tbit/s. Pursuing higher capacity is the leitmotiv of technology evolution. New spectra with enormous bandwidth resources and higher spectrum efficiency are required to achieve higher capacity.

- **Low cost**. Different from the operator-owned outdoor networks, many access wireless networks installed indoors are personally owned and the costs

are borne by a single household. Moreover, a large number of access points are required due to the picocell approaches. Thus, low cost is another important consideration.

- **High power efficiency**. With the dramatic increase in wireless connectivity density, the power consumption of future indoor wireless networks will be enormous, thus high power efficiency is required. High power efficiency is especially desired in portable battery-powered equipment in order to ensure longer usage time. Also, high power efficiency is important for indoor OWC systems since the average transmit optical power is limited due to the eye safety regulations.

- **Low latency**. Latency is particularly important for machine-to-machine communications such as Industry 4.0 settings, and for real-time applications such as video conferencing, VR, gaming, and remote equipment control which require real-time synchronous visual-haptic feedback. Excessive latency will degrade the user experience. For example, users may feel dizzy or lose patience with glitchy videos, laggy games, and dilatory machine interfaces. Therefore, low latency is required for future indoor wireless networks to support and improve the user experience of the latency-sensitive user scenarios.

My Ph.D. research is focusing on advanced signal processing by means of DSP techniques and preparing them for the indoor OWC systems at high connection densities and at a Gigabit-per-second capacity, far beyond what current radio-based systems can achieve. This thesis concentrates on the optimization of the 2D IR beam-steered OWC system introduced in Section 1.2.2 by using DSP techniques, with consideration of the above requirements. Three challenges resulting from the limitation of the AWGR beam-steerer, data converters, and FPGA are investigated in this thesis. The three problem-oriented research questions and proposed solutions are summarized as:

- Capacity improvement for the high spatial resolution AWGR-based 2D IR beam-steered OWC system

  In our 2D IR beam-steered OWC system, which we have realized in a laboratory demonstrator using the AWGR beam-steerer [35], there is a trade-off between the spatial resolution of the beam steering and the OWC channel capacity per beam. We proposed to take advantage of the digital Nyquist filtering technique for crosstalk mitigation and spectrum efficiency

improvement of the AWGR-based 2D IR beam-steered OWC system, resolving the compromise between the system spatial resolution and channel capacity per beam. By shaping the transmitted signal for narrow spectral occupancy, the inter-channel crosstalk resulting from the imperfect AWGR filtering can be reduced, which enables using a denser AWGR grid. Also, the capacity is increased by squeezing more data into the limited bandwidth. In addition, the spectral-efficient signal reduces the bandwidth requirement of the AWGR, which allows a low-complexity AWGR design. Thirdly, the proposed method is less sensitive to the wavelength misalignment between AWGRs and lasers, which relaxes the design of high wavelength stability lasers. The proposed method is cost-efficient and has been experimentally verified in a 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a 20-Gbit/s data rate OWC capacity using PAM-4 modulation format. More details are presented in Chapter 3.

- Complexity reduction for the DSP-aided high spatial resolution AWGR-based 2D IR beam-steered OWC system

  In our digital Nyquist filter-aided 2D IR beam-steered OWC system, the two samples/symbol oversampling of the Nyquist signaling doubles the sample rate requirement of data converters, which increases the hardware implementation complexity since high-speed data converters are complex and costly. We proposed to use the non-integer oversampling method to minimize the required sample rate of data converters to efficiently make use of the available relatively low-cost data converters, thus reducing the implementation complexity and power consumption. The performance impact of non-integer oversampling is experimentally investigated in the 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a 20-Gbit/s data rate OWC capacity using PAM-4 modulation format as well. The oversampling rate is minimized to 1.1 samples/symbol (when using SRRC filter with $\beta = 0.1$) with a DAC sample rate of 11 GSa/s. More details are presented in Chapter 4.

- Latency reduction for the FPGA-based DSP implementation

  For the FPGA implementation of DSP algorithms, a parallel implementation is necessary because the commonly-used FPGA operation frequency (level of MHz) is much smaller than our targeted data rate (level of Gbps). The classical straightforward-parallel implementation requires large mem-

ory for intermediate data caching, which introduces additional latency problems in the DSP. We proposed to use a deeply parallel method for the DSP algorithms implementation to avoid data caching with large memory in FPGA, reducing the DSP latency significantly. To enable the deeply parallel implementation, a data re-allocation scheme is proposed to cope with the issue of the dependency of the FIR output on the successive input samples, and a look-ahead computation approach is employed to improve the adaptive update efficiency of the digital adaptive equalization. An FPGA-based real-time digital PAM-4 receiver is implemented in the deeply parallel architecture and experimentally demonstrated in a fiber link with a 2.5-Gbit/s data rate for the performance evaluation. More details are presented in Chapter 5.

The organization of this thesis is shown in Figure 1.5. The key DSP techniques investigated in this thesis are explained in Chapter 2. The problem statements, proposed solutions, and experimental results for the above three research questions are presented in Chapter 3, Chapter 4, and Chapter 5. After the three problem-oriented chapters, the conclusions are drawn and the future outlook is discussed in Chapter 6.

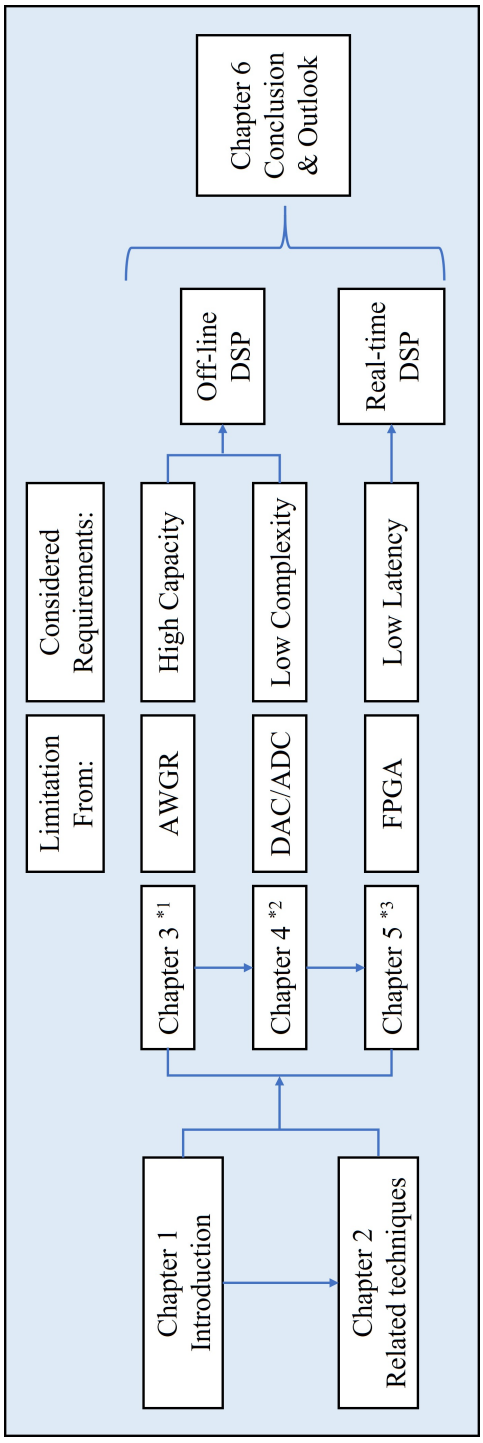

Figure 1.5: Organization of this thesis.
∗1. Chapter 3 is adjusted from the publication 1 [68];
∗2. Chapter 4 is adjusted from the publication 2 [69];
∗3. Chapter 5 is adjusted from the publication 3 [70];

2

Related DSP techniques

"You cannot force ideas. Successful ideas are the result of slow growth. Ideas do not reach perfection in a day, no matter how much study is put upon them."

— Alexander Graham Bell —

Low-complexity high-efficiency DSP plays a vital role in indoor OWC systems since it significantly improves the spectrum efficiency and signal quality, boosting the system capacity in a cost-efficient manner. This chapter briefly explains the key DSP techniques employed in this thesis. The IM-DD scheme is first introduced. Then the popular digital high-order modulation formats such as PAM, QAM, CAP, SCM, OFDM, and DMT are introduced, among which PAM-4 is utilized for investigation in the work of the subsequent chapters. After that, the digital equalization technique for the IM-DD PAM-4 system is introduced in detail. The conclusions are drawn finally.

2.1 IM-DD scheme

The IM-DD scheme is employed in the short-reach IR OWC systems for cost- and power consumption-sensitive indoor networks due to its low-complexity advantage. The simplified diagram of an IM-DD link for IR OWC is presented in Figure 2.1. Generally, the construction of the IR OWC system is similar to the construction of an optical fiber communication system, except that the fiber channel is replaced by the free space channel. The fiber channel suffers from attenuation loss and dispersion effects, while the free space channel also has losses but dispersion is negligible. In the transmitter, IM is achieved by modulating the transmitted waveform onto the instantaneous power of the optical carrier. The modulation can be achieved by direct current modulation which directly varies the driving current of laser sources or external modulation which relies on external modulators. Direct current modulation is more cost-efficient but offers a data rate of only a few Gbit/s and suffers from non-linear distortion and chirp problems, while external modulation is more complex but supports a higher data rate of up to tens of Gbit/s with better performance. The modulated signals are then transmitted to the receiver via the free-space channel with the help of optical components. DD is the simplest way to detect an intensity-modulated signal, in which a photo-detector produces a current proportional to the received instantaneous power. PIN and APD are the most popular photo-detectors for IR OWC systems. The PIN is widely used for indoor applications, in which economy is the priority. APD features higher sensitivity but at a higher cost in terms of price and high operating voltage. A simple description for the IM-DD channel is given:

$$y(t) = R \cdot x(t) \otimes h(t) + R \cdot n(t) \tag{2.1}$$

where $y(t)$ is the instantaneous photo current received, R is the photo-detector responsivity, $x(t)$ is the instantaneous transmitted power, t is the absolute time, $\otimes$ represents convolution operation, $h(t)$ is the channel impulse response, and $n(t)$ is the background noise, which is modeled as white Gaussian noise and is independent of the received signal [71].

2.2 Digital high-order modulation formats

The IR beam-steered OWC provides intrinsically high data capacity due to the enormous unregulated bandwidth of the IR spectrum and the better SNR of the high-directivity narrow-beam-steering link. The free space channel theo-

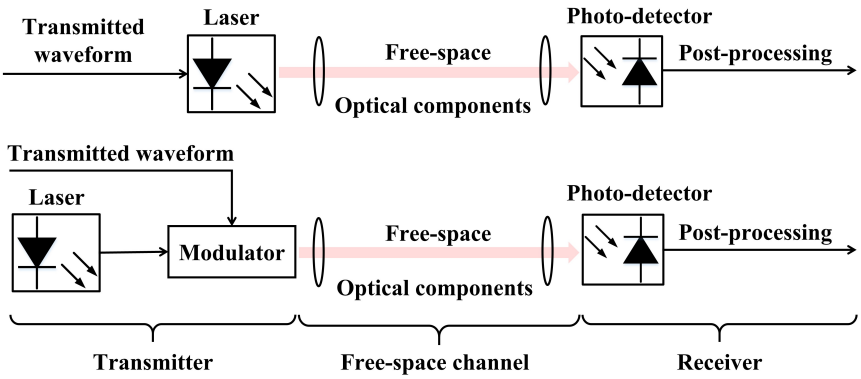

Figure 2.1: Simplified diagram of an IM-DD link for IR OWC.

retically can be considered to have unlimited bandwidth, but the electrical and optical components in the transmitter and receiver nodes are bandwidth-limited. Therefore, spectrum-efficient digital high-order modulation which squeezes more data into the limited channel bandwidth is required in order to achieve higher capacity per beam.

By introducing multiple dimensions for carrying information, more information bits can be coded into the transmitted signal waveform before being modulated onto the optical carriers. The popular spectrum-efficient modulation formats employed in the OWC systems include but are not limited to pulse amplitude modulation (PAM), quadrature amplitude modulation (QAM), carrierless amplitude phase (CAP) modulation, discrete multitone (DMT) modulation, subcarrier modulation (SCM), and orthogonal frequency division multiplexing (OFDM).

- **PAM** is one-dimension baseband modulation using only the amplitude to carry the information. Basically, the on-off-keying (OOK) non-return-to-zero (NRZ) signal is transmitted in the OWC system. The OOK NRZ signal has two levels, which are the on-level when there is light and the off-level when there is no (or little) light. It is a binary unipolar signal that represents 1 bit/symbol. In order to transmit more than 1 bit/symbol, 2^n-level PAM (PAM-L, where $L = 2^n$) can be used. PAM-L signal is a multi-level signal that represents n bits/symbol. For example, the PAM-4 signal carries 2 bits/symbol, as shown in Figure 2.2. The OOK NRZ signal is a PAM-2 modulation format. The waveform of a PAM signal can

Figure 2.2: Example of constellation diagrams for (a) OOK, (b) PAM-4.

be represented as:

$$x_{PAM}(t) = \sum_i b_i \cdot p(t - i \cdot T_P) \tag{2.2}$$

where $b_i = \{0, 1, 2, ..., (L-1)\}$ is selected to represent the input symbols, $p(t)$ is the pulse shaping filter and T_P is the pulse period (i.e., $T_p = 1/R_S$, R_S is the symbol rate). For a given bit rate, the bandwidth requirement of the PAM-L signal is reduced by $1/n$ in comparison to the OOK NRZ signal, which is more spectrum-efficient albeit at the cost of lower power efficiency. The PAM-L signal requires better system linearity and higher DAC/ADC resolution when L grows, and the smaller Euclidean distance of the constellation points of higher order PAM modulation (larger L) increases the sensitivity to noise and signal corruption.

- **QAM** is a two-dimensional modulation format that combines two carriers whose amplitudes are modulated independently with the same frequency but a phase difference of 90 degrees from each other. The QAM signal is complex including in-phase (I) and quadrature (Q) components. It can be represented as:

$$x_{QAM}(t) = I(t) \cdot \cos(2\pi f_c t) + Q(t) \cdot \sin(2\pi f_c t) \tag{2.3}$$

where f_c is the carrier frequency, the I and Q components are given as:

$$\begin{aligned} I(t) &= \sum_i b_I(i) \cdot p(t - i \cdot T_P) \\ Q(t) &= \sum_i b_Q(i) \cdot p(t - i \cdot T_P) \end{aligned} \tag{2.4}$$

In comparison to the PAM signal, 2^n-level QAM also represents n bits/symbol, but the constellation points of the QAM signal at the same order have a larger Euclidean distance for easier discrimination after the channel impairment. The QAM constellation points are usually arranged on a square grid, with the same vertical and horizontal spacing, for easier implementation. The example of constellation diagrams for the 4-QAM and 16-QAM

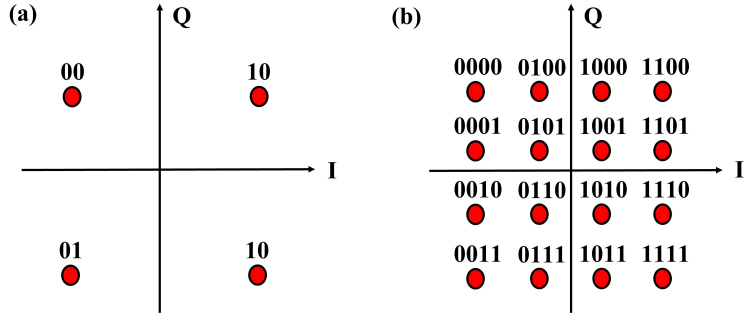

Figure 2.3: Example of constellation diagrams for (a) 4-QAM, (b) 16-QAM.

signal with a square grid is depicted in Figure 2.3. At the receiver, both the I and Q components must be extracted separately through quadrature demodulation, which increases the complexity of post signal processing to recover the transmitted data. For the IM-DD link, the QAM format is enabled by electrical sub-carriers modulation.

- **CAP** is a variant of QAM. Instead of modulating the amplitude of two sub-carriers, CAP generates a QAM signal by combining two PAM signals through two orthogonal pulse shaping filters whose impulse responses form a Hilbert transform pair (have the same amplitude spectrum but the phase spectrum differs by 90^o) [55]. The CAP signal can be expressed as:

$$x_{CAP}(t) = \sum_i \left[b_I(i) \cdot p_I(t - i \cdot T_P) + b_Q(i) \cdot p_Q(t - i \cdot T_P) \right] \tag{2.5}$$

where the orthogonal pulse shaping filters are given as:

$$\begin{aligned} p_I(t) &= p(t) \cdot \cos(2\pi f_p t) \\ p_Q(t) &= p(t) \cdot \sin(2\pi f_p t) \end{aligned} \tag{2.6}$$

where f_p is the center frequency of the CAP signal. Figure 2.4 shows the block diagrams of QAM and CAP modulation. The advantage of CAP over QAM is the simpler implementation. The up-conversion of the baseband PAM signal with the quadrature carriers is not necessary with CAP because the orthogonality is realized in the transmit pulses, thus the name 'carrierless'. At the receiver, the received signal is demodulated after matched filtering with the delayed mirrored version of the transmit orthogonal pulse shaping filters. It is possible to subdivide the CAP signal

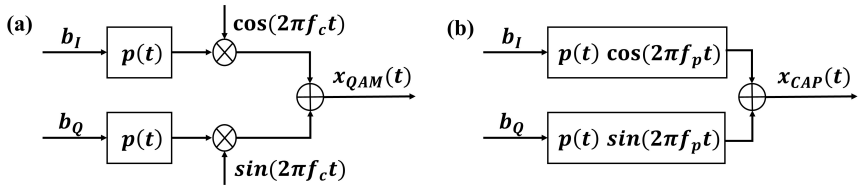

Figure 2.4: Block diagrams of (a) QAM, (b) CAP modulation.

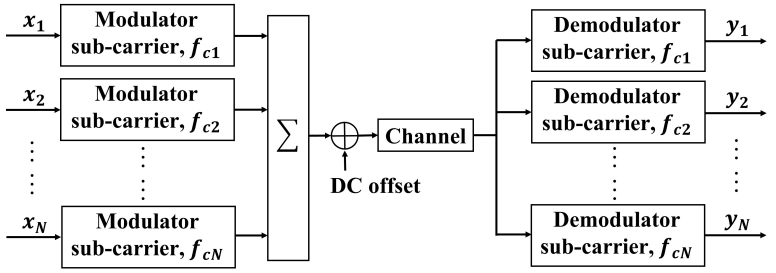

Figure 2.5: Block diagram of SCM scheme.

into a number of non-orthogonal frequency-division multiplexing (FDM) sub-carriers, known as multiband-CAP (m-CAP) [72, 73].

- **SCM** is a multi-carrier modulation format. It encodes information data onto multiple electrical sub-carriers before being modulated onto the optical carrier. The block diagram of the SCM scheme is presented in Figure 2.5. The available signal bandwidth is divided into a number of narrow bandwidth slots (sub-carriers), and each sub-carrier carries data based on the adopted modulation format. Then the multiple sub-carriers are combined for transmission. At the receiver, multiple bandpass demodulators are used to recover the individual data streams. It provides better immunity to inter-symbol interference (ISI) and background light-induced noise, and offers an opportunity of multiplexing multiple user data onto a single optical carrier. However, it has poor average power efficiency due to the required DC-offset. A sufficient DC-offset should be added with the electrical sub-carriers which have both negative and positive parts since the input signal for the optical intensity modulation must be non-negative. The amount of required DC-offset increases as the number of sub-carriers increases, thus the power efficiency decreases when increasing the sub-carriers number [40]. SCM can also be implemented with the sub-carrier signals made orthogonal to one another to achieve OFDM.

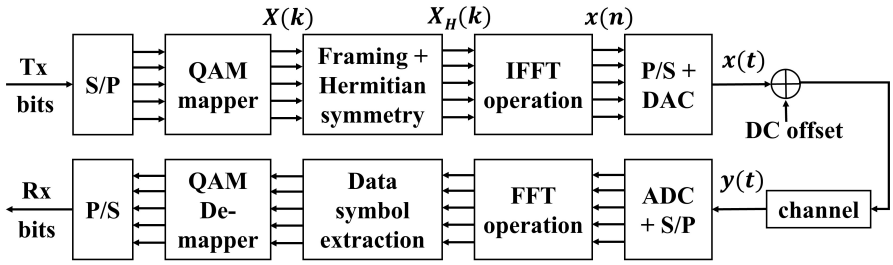

Figure 2.6: Block diagram of DCO-OFDM. S/P: serial-to-parallel converter, P/S: parallel-to-serial converter [40].

- **OFDM**, a special class of FDM, is a widely-used multi-carrier modulation format. The higher-speed serial information bit stream is divided into lower-speed parallel steams and transmitted in parallel over a number of sub-channels associated with a set of sub-carriers. The main difference between OFDM and FDM is that OFDM sub-channels can overlap in the frequency domain with no inter-channel interference due to orthogonality. The data streams for each sub-carrier are encoded with the adopted modulation format such as QAM at a lower symbol rate, then the data rate is increased by densely spacing the sub-carriers thanks to the guard-band-free sub-channels. The multiple sub-carriers modulation and de-modulation are efficiently implemented based on the fast Fourier transform (FFT) algorithm. In terms of OWC systems, the input signal for intensity modulation must be positive and real-valued. By adding a suitable DC offset, the signal can be made positive and unipolar. The real value is enabled by imposing Hermitian symmetry prior to the inverse fast Fourier transform (IFFT) operation. This results in the well-known DC-offset optical OFDM (DCO-OFDM), and its block diagram is depicted in Figure 2.6. A representation of the signal that results from the Hermitian operation on signal $X(k)$ is represented by:

$$X_H(k) = \left[1, X(k), 0, \underbrace{0,...,0}_{N(L-1)/2}, 0, \underbrace{0,...,0}_{N(L-1)/2}, X^*(NL-k)\right], \tag{2.7}$$

where $X^*(.)$ represents the complex conjugate of $X(.)$, $k = 0,1,...N_s - 1$, N_s is the number of sub-carriers, $N = 2(1 + N_s)$, L is the oversampling factor of the time-domain signal, and $X_H(k)$ is the resultant signal before

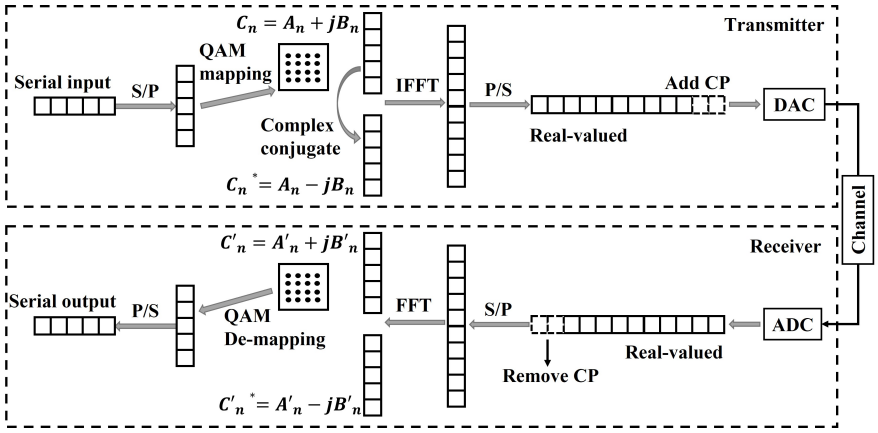

Figure 2.7: Principle of DMT. S/P: serial-to-parallel converter, P/S: parallel-to-serial converter, CP: cyclic prefix [76].

being modulated onto the sub-carriers by the NL-points IFFT block [40]. There are also variants of optical OFDM without the need for DC-offset such as asymmetrically-clipped optical OFDM (ACO-OFDM) [74, 75]. In ACO-OFDM, the bipolar real OFDM signal is clipped at the zero value and only the positive parts are transmitted.

- **DMT** is a baseband implementation version of OFDM. The principle of DMT is presented in Figure 2.7. Similar to the OFDM, the high-speed serial bit sequence is firstly divided into lower-speed parallel bit streams and mapped onto the QAM constellation. The complex QAM signal is then multiplied with its conjugate satisfying the Hermitian symmetry for real-valued IFFT output. IFFT is performed to modulate the complex signals and their conjugates on different sub-carriers which are mutually orthogonal. Then the parallel data streams are converted into a serial data stream for transmission. An inverse operation is performed on the receiver side. With DMT the number of bits per sub-carrier can be adjusted depending on the available SNR, which is the so-called bit-loading function. This is achieved by selecting the corresponding constellation size of each sub-carrier according to the allocated number of bits. The bit-loading algorithms include two categories: rate-adaptive bit-loading which maximizes the bit rate for a fixed bit-error ratio (BER), and margin-adaptive bit-loading which minimizes the BER for a fixed bit rate. In addition, the power for each sub-carrier can be allocated based on the water-filling

method, which is known as power-loading. Similar to ACO-OFDM, PAM-DMT is a variant of DMT that requires no DC-bias, and allows asymmetric clipping at zero value and transmission of only the positive parts. Unlike ACO-OFDM in which only the odd sub-carriers are data carrying, PAM-DMT utilizes all sub-carriers to carry data, thus allowing for full use of the bit-loading and power-loading techniques [76].

In general, multi-carrier modulation provides better spectrum efficiency, but is less power-efficient, and requires higher implementation complexity than single-carrier modulation. Hence, single-carrier modulation is preferred for indoor OWC applications where power-efficient and cost-efficient are the most important criterion. In terms of our IR beam-steered OWC system, both PAM-4 and DMT have been applied for experimental demonstration [36, 34]. In this thesis, the modulation format being investigated for the indoor IR OWC is the PAM-4 modulation due to the lower complexity with no need for complex signal processing, FFT operations, carrier and phase estimation, etc.

PAM-4 has been widely used in short-reach optical fiber links and has already been ratified by IEEE 802.3 bs for 400 Gbit/s Ethernet transmission [77]. Unlike multi-carrier modulation which has better tolerance to ISI resulting from the larger symbol duration of each sub-carriers, single-carrier modulation suffers from larger ISI problems for transmission of the same data rate. Thus an equalization technique is needed for the PAM-4 systems. The equalization technique is explained in the next subsection.

2.3 Digital equalization techniques

Digital equalization is normally utilized for channel distortion compensation and ISI mitigation for high-speed transmission in a cost-efficient way. Unlike optical fiber which suffers from attenuation loss and dispersion effects such as chromatic dispersion and waveguide dispersion, the free-space channel has attenuation loss but negligible dispersion. Therefore, the channel distortion of the IM-DD free-space link mainly comes from the high-frequency attenuation and distortion of the bandwidth-limited electrical and optical components. Digital equalization enables the utilization of relatively low-cost components with limited bandwidth and avoids the utilization of costly optical compensating modules, which realizes high-speed transmission in a cost-efficient way. In addition, the high data rate represents a short symbol duration for the single-carrier system, leading to higher sensitivity to ISI caused by channel impairments (e.g. bandwidth-limited com-

ponents, multipath propagation, background noise from non-signal free-space light, etc). Equalization minimizes the ISI for better BER performance.

In the simplest case, digital equalization is based on filters that have the inverse characteristics of the channel response. Based on the channel noise characteristics and practical system requirements, the equalization is sometimes partitioned between a pre-equalizer in the transmitter and a post-equalizer in the receiver. Pre-equalizer is usually implemented with static filters depending on the pre-estimated channel response, while a post-equalizer can be implemented using static filters based on the pre-estimated channel response or adaptive filters which can track and calibrate the channel variations in real-time. The filter structure can be Infinite Impulse Response (IIR)-based or Finite Impulse Response (FIR)-based, as depicted in Figure 2.8. The FIR-based structure has better linearity and stability, and is more practical for implementation than the IIR-based structure. Therefore, the FIR-based filter structure is widely used in digital equalization.

Digital equalization can be implemented in both the time domain and frequency domain. When the equalization filter length is large, the frequency-domain equalizer (FDE) has less computational complexity than the time-domain equalizer (TDE) since the FDE only relies on a single-tap multiplication. However, the time-to-frequency domain and frequency-to-time domain conversion which is realized by using the FFT and IFFT blocks also spend hardware resources, so the FDE may be less cost-efficient than the TDE. Also, the FDE is less latency-efficient since the FFT-based operation adds intrinsic latency. In [78], a comparison between the TDE and FDE is performed in the Faster-than-Nyquist (FTN) system where the ISI problem is severe. It came to a conclusion

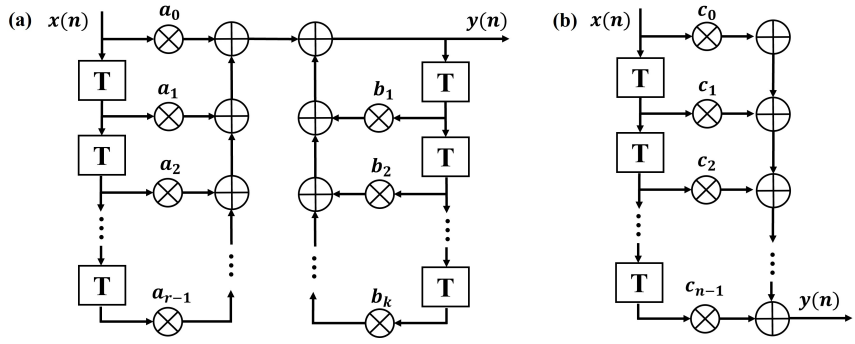

Figure 2.8: Direct-form filter structures: (a) IIR and (b) FIR.

that the TDE outperforms the FDE with better BER performance and robustness. Many digital equalization techniques have been developed for short-reach IM-DD PAM-4 systems. Some popular digital equalization techniques are summarized in Figure 2.10 according to various classifications.

2.3.1 Digital equalization techniques for linear impairments

The FIR-based feed-forward equalizer (FFE) is a very popular and efficient equalization technique to cope with the linear impairments for the short-reach PAM-4 IM-DD link. The FFE can boost the power of high-frequency components that suffer from attenuation due to the system bandwidth limitation. The basic component of an FFE is the FIR filter, as shown in Figure 2.8 (b). For a specific channel, the channel distortion can be pre-estimated and the inverse of the channel response is stored as the tap weights (filter coefficients) of the static FFE. For a time-varying channel, adaptive equalization is needed to track and calibrate the channel distortion in real time. The block diagram of an adaptive FFE is shown in Figure 2.9. The tap weights (filter coefficients) of both the static and adaptive FFE can be pre-calculated or adaptive updated using zero-forcing (ZF) algorithms, least mean squares (LMS) algorithms, recursive least squares (RLS) algorithms, and so on. Different adaptation algorithms have different convergence speeds to obtain the optimal weights (filter coefficients), among which LMS is widely utilized due to its robust and low-complexity advantage. When the FFE operates at symbol rate sampling (1 sample/symbol, the FFE inputs are delayed by T where T is the symbol duration), it is called symbol-spaced FFE. When the FFE operates at higher symbol rate sampling (m samples/symbol, the FFE inputs are delayed by T/m), it is called the fractionally-spaced FFE. In comparison to the symbol-spaced FFE, fractionally-spaced FFE has a lower residual error [79], but at the cost of higher computational complexity.

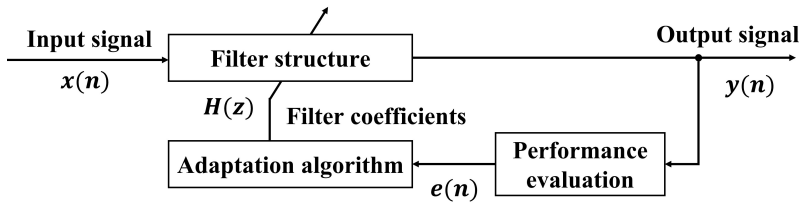

Figure 2.9: Block diagram of an adaptive FFE.

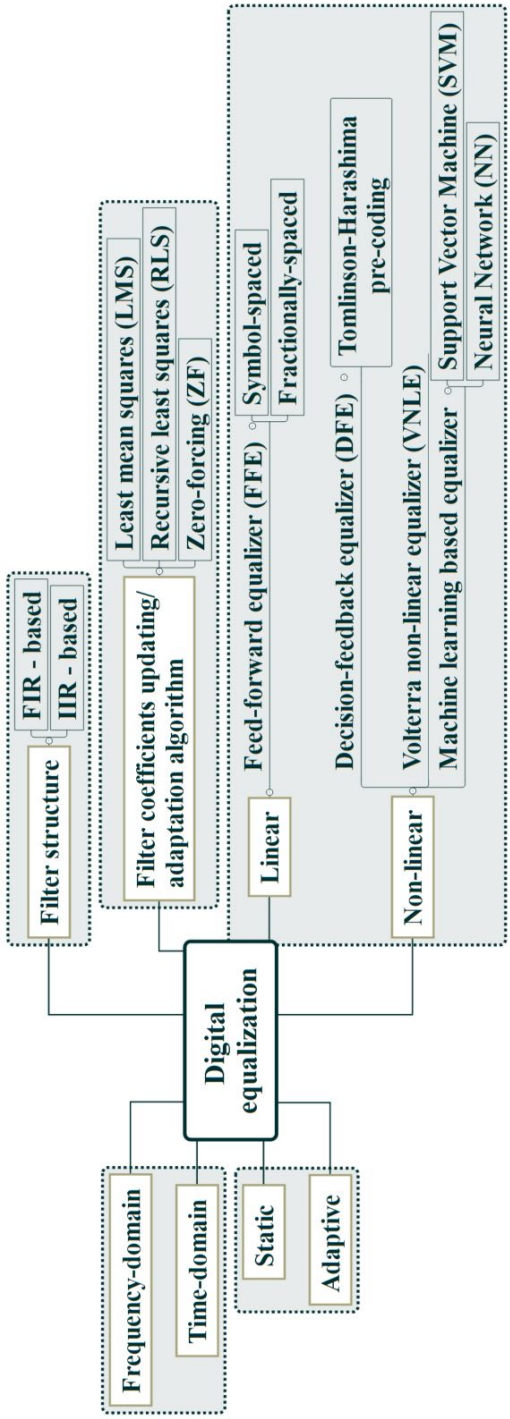

Figure 2.10: Popular digital equalization techniques.

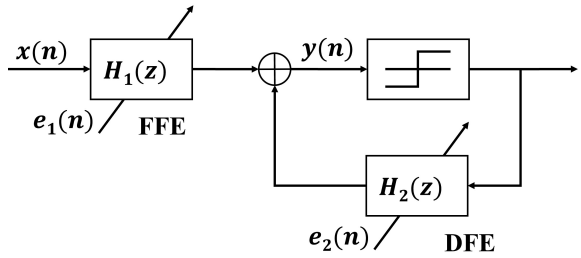

Figure 2.11: Block diagram of a cascaded FFE and DFE.

Decision-feedback equalizer (DFE) is another widely-used equalization technique in the short-reach IM-DD PAM-4 systems. The interaction between fiber chromatic dispersion and direct detection will lead to a power-fading effect. The detected signal may contain frequency notches after several kilometers transmission at a high symbol rate [80, 81, 82]. The frequency notches are unable to be compensated for easily by FFE but can be mitigated by DFE. However, DFE uses the signal after the decision as input, which may cause error propagation and is unstable due to the decision feedback scheme. Therefore, DFE is not used independently but always together with FFE, as shown in Figure 2.11. Recently, the Tomlinson-Harashima pre-coding technique has also been proposed to cope with the DFE error propagation problem [80, 83, 84, 85]. DFE can be considered as a nonlinear device due to the decision-feedback operation although most of the DFE structures are based on linear filters. Many novel equalizers based on the conventional FFE/DFE are proposed to deal with the practical system implementation problems [86, 87, 88].

In terms of the short-reach IR OWC system, the power-fading effect caused by the fiber chromatic dispersion can be neglected. Therefore, FFE is efficient to compensate for linear impairments. In the experimental setup investigated in Chapter 3, the main channel impairment comes from the bandwidth-limited AWGR, which can be efficiently compensated for by using only the time-domain symbol-spaced FIR- and LMS-based FFE.

2.3.2 Digital equalization techniques for non-linear impairments

High-order PAM systems require high system linearity. Without consideration of the fiber dispersion, the non-linear impairments of an IR OWC IM-DD link are mainly caused by the non-linearity of devices (e.g. directly modulated laser (DML), RF amplifiers or drivers, and square-law detection). The non-linear

impairments are non-negligible for a high-speed PAM-4 transmission system. The nonlinear intensity/power input-output relationships will result in unequal eye openings for the PAM-4 signals with different amplitude levels, and the intensity/power-dependent delay will lead to an amplitude-dependent skew in the overall PAM waveform [89, 90].

Volterra non-linear equalizer (VNLE) is a popular equalization technique to compensate for non-linear impairments. VNLE can be FFE-based or DFE-based. The main difference between VNLE and FFE/DFE is that the basic components of the VNLE are high-order filters but not linear filters. The output of the m-th sample from a K-th order VNLE with memory length L_k for each $k = \{1, 2, ..., K\}$ order can be described as [91, 90]

$$y(m) = \sum_{k=1}^{K} \sum_{n_1=0}^{L_k-1} \sum_{n_2=0}^{n_1} ... \sum_{n_k=0}^{n_k-1} \{w_k(n_1, n_2, ..., n_k) \cdot x(m-n_1)x(m-n_2)...x(m-n_k)\}, \tag{2.8}$$

where x represents the real-valued VNLE inputs and $w_k(n_1, n_2, ..., n_k)$ are the tap weights (filter coefficients) for the K-th order. When $K = 1$, it is the linear equalizer. Similarly, the VNLE can be adaptive updated using the adaptation algorithms. The main drawback of the VNLE is its high computational complexity. The computational complexity of a VNLE grows dramatically with the VLNE order for a fully-connected VNLE, which is not practical for the hardware implementation. The computational complexity of Eq. (2.8) in terms of the number of real multiplications is given by [91, 90]

$$CC_{VNLE}(K, L) = \sum_{k=1}^{K} \frac{(L_k - 1 + k)!}{(k-1)!(L_k - 1)!}, \tag{2.9}$$

where $L = [L_1, L_2, ..., L_k]$ is a vector that includes all memory lengths and $(\cdot)!$ denotes the factorial operation. Fortunately, the computational complexity can be reduced by pruning the unnecessary kernels. A sparse VNLE or a VNLE order of up to 2 or 3 is sufficient for equalizing most of the nonlinear impairments [90, 92, 93, 94, 95], improving the feasibility of the VNLE.

More advanced equalization techniques based on machine learning including support vector machine (SVM) and neural network (NN) have also been proposed and investigated [96, 97, 98, 99] to cope with the non-linear impairments. In [99], an optimized 2nd-order VNLE with the tap weights updated by using the SVM trainer is proposed to enable an 80-Gbit/s DML-based IM-DD PAM-4 20-km fiber transmission utilizing 10-Gbit/s-class optics. Various variants of the

NNs such as convolutional NN (CNN) [100], long short-term memory (LSTM) networks [101], and cascade recurrent NN (C-RNN) [102, 103] have been demonstrated. A 100-Gbit/s PAM-4 15-km fiber transmission using 16-GHz DML is achievable in [102, 103] by using the C-RNN-based equalization technique. To reduce the computational complexity of the NN-based equalization, the insignificant weights can be cut off. A sparsely-connected C-RNN is proposed in [104], which depicted that a 21.66% reduction of the C-RNN connections causes almost no performance degradation.

2.4 Conclusion

In this chapter, the key DSP techniques related to the work of this thesis are explained in detail. Six popular digital high-order modulation formats including PAM, QAM, CAP, SCM, OFDM, and DMT have been described to give a general overview of the digital high-order modulation techniques. Considering the dominant requirements of power-efficient and cost-efficient for the indoor IR OWC applications, the IM-DD scheme and PAM-4 format are chosen for further investigation in this thesis. Digital equalization techniques are necessary for the high-speed PAM-4 systems which are sensitive to the ISI resulting from the reduced symbol duration for higher required data rate. Thus an overview of a variety of digital equalization techniques is given finally. In the work of the subsequent chapters, the symbol-spaced LMS-updated FIR-based adaptive FFE is efficient for channel impairments compensation.

3

Capacity improvement for the high spatial resolution AWGR-based 2D IR beam-steered OWC system

"If the only tool you have is a hammer, you tend to see every problem as a nail."

— Abraham Maslow —

This chapter concentrates on the tradeoff problem of the system spatial resolution and OWC channel capacity per beam for the AWGR-based 2D IR beam-steered OWC system. A digital filter-aided crosstalk mitigation scheme which takes advantage of the digital Nyquist pulse shaping technique is proposed to cope with this problem. By shaping the transmitted signal for narrow spectral occupancy, the inter-channel crosstalk resulting from the imperfect AWGR filtering can be reduced, which enables using a denser AWGR grid. Also, a doubled channel capacity is attainable with the improved spectrum-efficient signal. The proposed method has been experimentally investigated over a 6-GHz bandwidth-limited 12.5-GHz channel-spaced AWGR-based 1.1-m free-space link with the 20-Gbit/s OWC capacity using PAM-4 format [68].

3.1 AWGR-based 2D IR beam-steered OWC system

The 2D IR beam-steered OWC using highly directive narrow beams which has been introduced in Section 1.2.2 is a promising solution for high-speed indoor wireless connectivity. Different from the broadcast-based VLC, the IR beams can be easily confined as narrow beams and directed only to the intended destination and serves the individual user device when needed. The highly directional narrow-beam-steered scheme is power-efficient and provides intrinsically high capacity per beam since most of the emitted signal power can be received by the user devices with little power spoiling elsewhere. The high capacity per beam is fully used for only one user device without competition to other user devices. The unshared link provides better privacy protection and avoids congestion issues.

The beam-steering can be realized with actively controlled devices such as MEMS-based mirrors and SLMs, or with passive steering elements such as diffraction gratings and AWGRs. More beam-steering techniques are presented in [105]. The passive beam-steering techniques outperform the active beam-steering techniques with the benefits of passive maintenance-free, easy scaling, and fast steering response. Passive beam-steering is achieved by just tuning the wavelength of each beam remotely with no need for mechanical movement and local powering. Thus, it is easy to scale up for multiple beams system only by adding wavelengths in the remote central controller, and the beam steerer on the local side can be more compact, power-efficient, and reliable. Also, the steering response time is reduced from microseconds-level to nanoseconds-level thanks to the fast wavelength tuning speed of laser diodes. Both the grating-based and the AWGR-based beam-steering techniques have been utilized for realizing high-capacity 2D IR beam-steered OWC systems [32, 33, 35]. In comparison to the grating-based solution, the AWGR-based solution can make use of the AWGR modules which are readily available commercially, and is easier for assembling and requires less alignment effort. Also, it is not impacted by polarization state fluctuations in the optical input signal which may cause signal intensity fluctuations in the grating-based solution [22].

The first concept of AWGR-based 2D IR beam-steered OWC was proposed by A.M.J.Koonen et al. from the Eindhoven University of Technology in 2016 [106]. A 10-Gbit/s data transfer over a 2.4-m free-space distance is achieved by using the OOK signal and a C-band 80-ports AWGR-based beam steerer features a 50-GHz channel spacing, providing the possibility of serving 80 users simultaneously and independently with a free-space transmission capacity per user at 10 Gbit/s

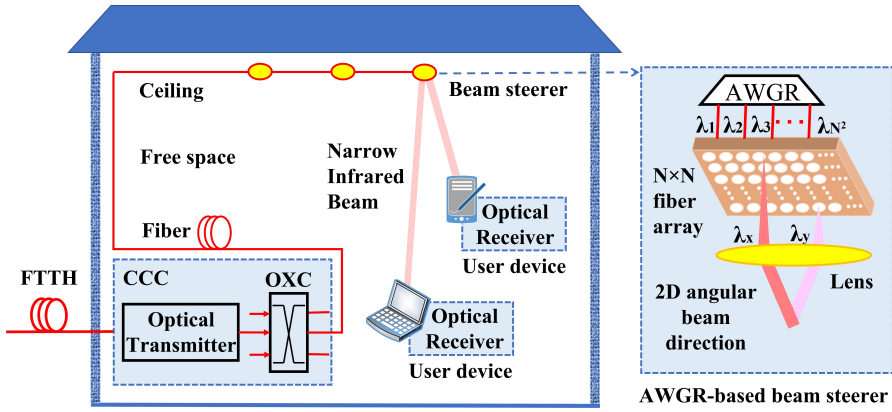

Figure 3.1: Indoor OWC down-link with AWGR-based 2D IR beam steering. FTTH: Fiber to the home; CCC: central communication controller; OXC: optical cross-connect; AWGR: arrayed waveguide grating router.

[43]. The system performance is further improved with a capacity per beam increasing from 10 Gbit/s to 35 Gbit/s (OOK signal) [107] and further to 112 Gbit/s (PAM-4 signal) [36] over 2.5-m reach, implying a potential aggregate system capacity of 80 beams $\times$112 Gbit/s/beam = 8.96 Tbit/s. This concept has been implemented in a laboratory demonstrator setup with simultaneous delivery of two beams carrying independent real-time high-definition video streams over 10-GbE protocol, showing the feasibility for practical applications [108]. The demonstrator setup utilizes an upgraded C+L band AWGR-based beam steerer (PRA, which is short for pencil radiating antenna) to support 129 beams for 129 OWC cells. In this demonstrator setup, the user localization and the upstream communication are done by means of 60-GHz RF techniques. A defocusing approach is also proposed to reduce the size of the beam steerer and achieve a better filling of the covered area [35].

Figure 3.1 shows a simplified indoor OWC down-link with AWGR-based 2D IR beam steering. The beam-steering is realized by just tuning the wavelength of each beam remotely in the central communication controller (CCC). The CCC is the interface between the public access network and the indoor network. The AWGR-based beam steerers are mounted on the ceiling, and multiple beam steerers will be installed in a room to cope with the LOS blocking issues. The transmitted signal is modulated onto the optical carrier with the optical transmitter, then switched and fed to the desired beam steerer through an optical cross-connect (OXC) and fibers. The signal is λ-splitted after the filtering at

the AWGR. The output ports of the AWGR are regrouped into a 2D fiber array and this fiber array is placed in the focal plane of a lens. The position of the fiber in the focal plane of the lens determines the angular direction of the collimated beam after the lens. In order words, each wavelength fitting on the grid of the AWGR maps to a specific 2D angular beam direction for an individual user device. The wavelength is tuned remotely in the CCC and the number of beams is limited by the number of output ports of the AWGR. Each beam is narrow covering only a certain area and is steered step-wise in both the 2D directions. In order to cover the user devices anywhere in the room and support a higher wireless connectivity density, a high spatial resolution of the beam-steering is needed, resulting in the requirement of AWGR with a higher port count.

3.2 Trade-off problem between AWGR-based system spatial resolution and OWC channel capacity per beam

In this wavelength-controlled AWGR-based 2D IR beam-steered OWC system, the spatial resolution is compromised with the channel capacity per beam. Based on the above discussion, each wavelength that fits on the grid of the AWGR maps to a specific 2D angular beam direction (each beam covers a certain area). Thus, the spatial resolution of the AWGR-based 2D IR beam-steered system depends on the grid of the AWGR (port count of the AWGR). A higher spatial resolution requires a higher port-count AWGR. For a limited available spectral range, a direct way of adding port count is to reduce the channel spacing, as shown in Figure 3.2 (b). However, the reduced channel spacing causes larger inter-channel crosstalk. To avoid the crosstalk caused by the reduced channel spacing, a larger spectral guard band should be inserted between adjacent AWGR channels, which leads to a compromised channel bandwidth, thus smaller channel capacity.

Take C-band (1530 nm to 1565 nm) as an example, the possible AWGR port-counts can be increased by 4 times if the channel spacing is reduced from 50 GHz (maximum of 87 ports theoretically) to 12.5 GHz (maximum of 350 ports theoretically) when tuning over C-band. However, the 3-dB bandwidth of the AWGR channel shrinks as the decrease of channel spacing. For example, the Gaussian-shaped commercial 50-GHz channel-spaced AWGR features 24-GHz 3-dB bandwidth, while the 3-dB bandwidth of the 12.5-GHz channel-spaced AWGR is only 6 GHz [109]. Therefore, the achievable OWC channel capacity per beam is compromised when the AWGR port count is increased.

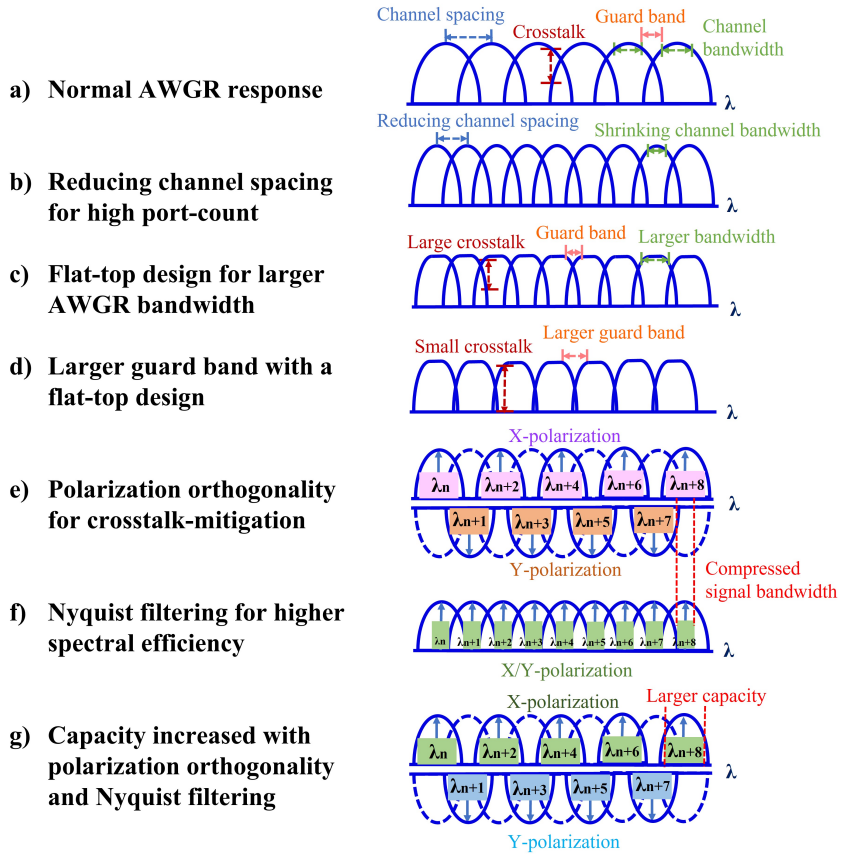

Figure 3.2: AWGR responses and techniques for increasing the channel capacity per beam for the AWGR-based 2D IR beam-steered system with high spatial resolution.

3.3 Reported solutions

In order to increase the channel capacity per beam for the AWGR-based 2D IR beam-steered system with high spatial resolution, one solution is to develop AWGRs with both high port count and high channel bandwidth. To get a high channel bandwidth with a dense channel grid, the channel response of the AWGR can be shaped from 'Gaussian' to 'Flat-top' [110], as shown in Figure 3.2 (c), the 1-dB bandwidth can get a >30% extension. Nevertheless, this 'Flat-top' design leads to larger crosstalk which requires a larger guard band for crosstalk mitigation as shown in Figure 3.2 (d), thus the bandwidth improvement is offset.

Another solution is to feed the high port-count AWGRs with a specially-

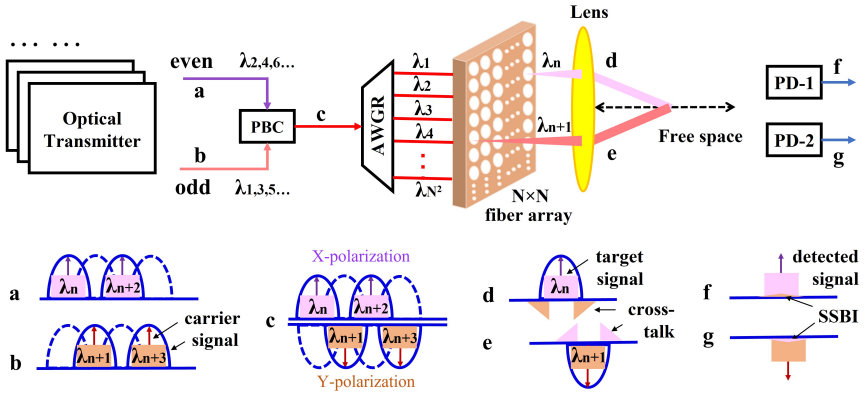

Figure 3.3: The operational principle of the crosstalk-mitigation solution for the AWGR-based 2D IR beam-steered OWC system by using polarization orthogonality [111]. (a) The input optical spectrum of the PBC even channels; (b) the input optical spectrum of the PBC odd channels; (c) the combined optical spectrum after PBC; (d)-(e) the optical spectrum of channel n and channel $n+1$ after AWGR; (f)-(g) the electrical spectra of the detected signal. PBC: Polarization beam combiner; PD: photo-diode; SSBI: signal-to-signal beat interference.

designed signal which causes little crosstalk between adjacent AWGR channels. A guard-band-free crosstalk-mitigation scheme was proposed for the AWGR-based 2D IR beam-steered system in [111]. By creating polarization orthogonality between the adjacent AWGR channels, the crosstalk between adjacent channels in the user plane is mitigated, which allows some spectral overlap between adjacent channels, as shown in Figure 3.2 (e). The operational principle of the polarization orthogonality for crosstalk mitigation is presented in Figure 3.3. The input signal is split into two groups (even and odd) as shown in Figure 3.3 (a) and (b) which are planned to feed into the even and odd channels of the AWGR. The polarization states of these two groups of signals are set orthogonal by using a polarization beam combiner (PBC). As Figure 3.3 (c) shows, the combined signals are polarization-orthogonal after the PBC. After the filtering of AWGR, the signal spectral of the n-th AWGR channel (λ_n) and $(n+1)$-th AWGR channel (λ_{n+1}) are presented in Figure 3.3 (d) and (e), including the targeted signal and the crosstalk from the adjacent channels. The signal of interest is polarization-orthogonal to the crosstalk from the adjacent channels and the two orthogonal polarization states do not affect each other upon detection. In the detected photocurrent, the electrical crosstalk items are small enough to be neglected in comparison to the signal of interest, so little crosstalk remains. Hence,

the number of AWGRs port counts can be doubled, with some spectral overlapping between the adjacent AWGR channels. Also, this technique releases the tight constraint on high wavelength stability laser sources design since it allows some wavelength misalignment between the laser and the AWGR channel. In addition, this technique enables a low-complexity high port-count AWGR design, which is implemented simply by reducing the on-chip spatial gap between output waveguides. However, it requires extra components for polarization-orthogonal signals design. More importantly, it is difficult to further scale up the channel capacity per beam for the bandwidth-limited high spatial resolution AWGR-based 2D IR beam-steered system by using the polarization-orthogonality technique. Crosstalk remains between the even channels or odd channels which stay at the same polarization state when the signal bandwidth is further scaled up for a larger channel capacity.

3.4 Proposed solution

In this chapter, a new crosstalk-mitigation scheme employing the digital Nyquist pulse shaping technique is proposed for the AWGR-based 2D IR beam-steered system to mitigate the inter-channel crosstalk and further increase the channel capacity per beam. As shown in Figure 3.2 (f), the signals fed to the AWGRs are specially shaped for narrow spectral occupancy, which releases the bandwidth requirement of AWGR, and enables using a denser AWGR grid with no need for a large guard band for crosstalk mitigation. Also, we can make use of the mature digital signal processing (DSP) techniques without additional optical components. In addition, the proposed method can also get rid of the strict constraint on wavelength-stable laser sources design since it allows some wavelength misalignment between the laser and the AWGR channel. In addition, a higher data rate is attainable with a low-cost low-complexity AWGR. Moreover, by combining the proposed solution with the polarization-orthogonal technique in [111], a larger channel capacity per beam is attainable resulting from the improved spectral efficiency, as shown in Figure 3.2 (g). Table 3.1 has summarized the pros and cons of the mentioned techniques.

Table 3.1: Summary of the pros and cons of the reported solutions and the proposed solution.

Techniques		Advantages	Disadvantages
'Flat-top' AWGR		Higher channel bandwidth	Larger crosstalk requires larger guard band
'Gaussian' AWGR	Polarization orthogonality	1) Crosstalk-free between adjacent channels 2) Allow the spectral overlap between adjacent channels 3) Enable low-complexity high port-count (HPC) AWGRs design 4) Get rid of the strict constraint on wavelength-stable laser sources design	1) Require extra optical components for polarization-orthogonal signals design 2) Difficult to further scale up the channel capacity per beam for the bandwidth-limited system 3) Crosstalk remains between even or odd channels that stay at the same polarization state
	Proposed Nyquist filtering	1) Crosstalk-free between adjacent channels 2) Higher spectral efficiency 3) Lower bandwidth requirement of AWGR 4) Require no additional optical components 5) Enable low-complexity HPC AWGRs design 6) Get rid of the strict constraint on wavelength-stable laser sources design	Increase the complexity of DSP implementation
	Proposed Nyquist filtering + Polarization orthogonality	Further doubled channel capacity per beam is attainable	1) Require extra optical components for polarization-orthogonal signals design 2) Increase the complexity of DSP implementation

3.4.1 Digital Nyquist pulse shaping technique

By introducing the digital Nyquist pulse shaping technique, the spectrum efficiency of a PAM-4 system can be further improved. Nyquist PAM-4 which takes advantage of the Nyquist pulse shaping technique can achieve enhanced spectrum efficiency similar to DMT [112] but with lower implementation complexity. Also, the Nyquist pulse shaping can achieve ISI-free transmission ideally according to the Nyquist zero-ISI criterion. In addition, the Nyquist pulse-shaped signals have a narrower spectrum occupation with a high out-of-band suppression, reducing the adjacent channel crosstalk of multiplex systems.

Generally, in order to avoid ISI, the digital sequence is converted into an analog signal employing a time-domain rectangular pulse. However, an ideal rectangular pulse in the time domain consumes infinite bandwidth in the frequency domain, as shown in Figures. 3.4 (a) and (b). When the signal with unlimited bandwidth is transmitted through a bandwidth-limited channel, the truncation of the spectrum leads to energy leakage in the time domain, resulting in ISI again. Nyquist pulse shaping technique is widely used for ISI mitigation in the conventional digital single-carrier communication systems [113, 114, 28]. By shaping the transmitted signal with specially-designed spectral masks (Nyquist filters), the signal bandwidth can be compressed without introducing ISI. A Nyquist filter is a filter with impulse response $h(t)$ satisfying the Nyquist zero-ISI criterion: only gets a 'one' at the desired moment and hits zero crossings at other symbol sampling instants, as shown in Eq. (3.1), where T_S is the symbol duration. The corresponding Fourier transform $H(f)$ satisfies Eq. (3.2), the frequency-shifted replicas of $H(f)$ should add up to a constant value.

$$\textit{Time domain}: \quad h(nT_S) = \begin{cases} 1, & n = 0 \\ 0, & n \neq 0. \end{cases} \tag{3.1}$$

$$\textit{Frequency domain}: \quad \sum_{k=-\infty}^{\infty} H\left(f + k/T_S\right) = T_S. \tag{3.2}$$

A commonly used practical Nyquist filter is using a pair of square-root raised-cosine (SRRC) filters. The Nyquist filtering is equally split between the pulse-shaping filter on the transmitter side and matched filter on the receiver side. The pulse-shaping filter determines the spectral mask, while the matched filter is introduced to maximize the signal-to-noise ratio (SNR) at the receiver. The impulse response of the SRRC pulse-shaping filter is given by Eq. (3.3), where

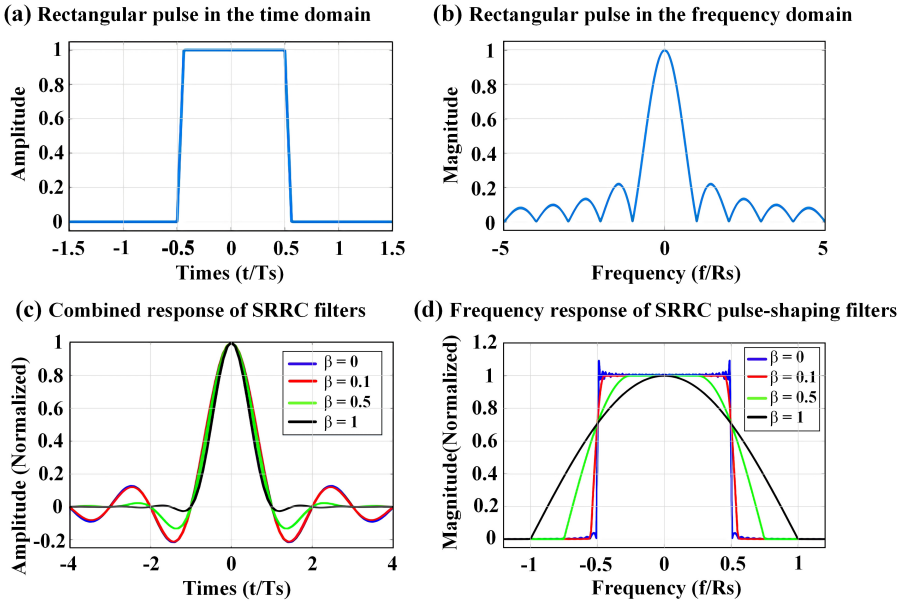

Figure 3.4: Pulse responses.

β is the roll-off factor that determines the pulse tail decaying. The impulse response of the SRRC matched filter is the delayed mirrored copy of $h_{SRRC}(t)$. The combined response of the SRRC filters satisfies the Nyquist zero-ISI criterion, as shown in Figure 3.4 (c). The corresponding frequency response of the SRRC filter is expressed and plotted in Eq. (3.4) and Figure 3.4 (d), respectively. The stopband frequency of the SRRC filters can be adjusted between $R_S/2$ and R_S by β, where R_S is the symbol rate.

$$h_{SRRC}(t) = \frac{1}{\sqrt{T_S}} \frac{\sin\left[(1-\beta)\frac{\pi t}{T_S}\right] + 4\beta\frac{t}{T_S}\cos\left[(1+\beta)\frac{\pi t}{T_S}\right]}{\frac{\pi t}{T_S}\left[1-(4\beta\frac{t}{T_S})^2\right]}. \tag{3.3}$$

$$H_{SRRC}(f) = \begin{cases} \sqrt{T_S}, & 0 \le |f| \le \frac{(1-\beta)R_S}{2} \\ \sqrt{\frac{T_S}{2}\left\{1+\cos\left[\frac{\pi T_S}{\beta}\left(|f|-\frac{1-\beta}{2T_S}\right)\right]\right\}}, & \frac{(1-\beta)R_S}{2} \le |f| \le \frac{(1+\beta)R_S}{2} \\ 0, & |f| \ge \frac{(1+\beta)R_S}{2} \end{cases}. \tag{3.4}$$

Therefore, by shaping the transmitted signal with SRRC filters, the signal bandwidth (main lobe width) can be compressed by $0.5(1+\beta)$, and the side

lobe is suppressed sufficiently. When the channel distortion and the receiver timing jitters are negligible, adjacent symbols do not cause interference to the interested symbol since they all pass through zero at the sampling instant theoretically. However, in practical systems, the channel distortion and the receiver timing jitters are non-negligible, so ISI remains and equalization is needed for ISI cancellation.

3.4.2 Crosstalk mitigation

Without the digital Nyquist pulse shaping, the transmitted signal is normally generated with the time-domain rectangular pulse, and the signal spectra mainly rely on the DAC and analog front-end hardware responses. The signal transmitted using the time-domain rectangular pulse consumes a frequency-domain infinite bandwidth with decaying side-lobes, as shown in Figure 3.5 (blue). When the AWGR channels become denser, the infinitely extending frequency response spills to the adjacent channels due to the imperfect AWGR filtering, resulting in inter-channel crosstalk. The Digital Nyquist pulse shaping technique allows precise control of the desired spectral shape of the transmitted signal. By shaping the transmitted signal with SRRC filters whose impulse response and frequency response are given by Eq. (3.3) and Eq. (3.4), the signal bandwidth (main lobe width) can be compressed by $0.5(1+\beta)$ where β is the roll-off factor and ranges from 0 to 1, and the side lobe is suppressed sufficiently, as shown in Figure 3.5 (red). When feeding the SRRC-shaped spectral-efficient signal to the AWGR, the AWGR channel spacing can be reduced with little inter-channel crosstalk, enabling the employment of AWGR with a higher port count.

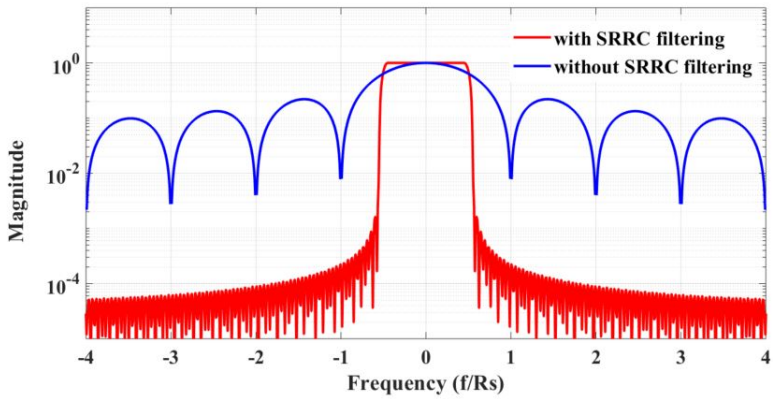

Figure 3.5: Frequency responses of the rectangular pulse and SRRC pulse.

For example, when the Gaussian-shaped AWGR [109] is employed and the PAM-4 signal with 20-Gbit/s channel capacity is transmitted, the transmitted signal features a 20-GHz double-sideband main lobe bandwidth. By using the AWGR with a channel spacing of 50 GHz, there is a large guard band that will not cause inter-channel crosstalk, as shown in Figure 3.6 (a). However, to transmit the 10-GBaud/s PAM-4 signal with 20-GHz double-sideband main lobe bandwidth by using the AWGR with 12.5-GHz channel spacing, the signal spectra are overlapping. The energy leakage from adjacent channels caused by imperfect AWGR filtering inevitably leads to signal crosstalk.

By using the polarization-orthogonal technique, the inter-channel crosstalk can be avoided thanks to the polarization-orthogonal adjacent channels, as shown in Figure 3.6 (c). The signals of polarization-orthogonal adjacent channels will not affect each other in the signal detection. The even channels or odd channels still stay at the same polarization state, but the channel spacing between the even channels or odd channels is 25 GHz, which is large enough to avoid inter-channel crosstalk.

By introducing the SRRC filtering, the 20-Gbit/s PAM-4 signal bandwidth (double-sideband main lobe bandwidth) can be compressed to 11 GHz (when $\beta = 0.1$, a small β leads to a narrow signal bandwidth), and the side lobe is suppressed sufficiently. There is still a 1.5-GHz guard band when the AWGR channel spacing is 12.5 GHz, as shown in Figure 3.6 (e). So, the inter-channel crosstalk can be avoided when the 12.5-GHz spaced channels are at the same polarization state.

3.4.3 Capacity improvement

To further scale up the PAM-4 signal bandwidth for a channel capacity of 40 Gbit/s, the signal bandwidth (double-sideband main lobe bandwidth) becomes 40 GHz. As mentioned above, the 3-dB bandwidth of the AWGR channel shrinks with the decrease of the channel spacing. For example, the Gaussian-shaped commercial 50-GHz channel-spaced AWGR features 24-GHz 3-dB bandwidth, while the 3-dB bandwidth of the 12.5-GHz channel-spaced AWGR is only 6 GHz [109]. As shown in Figure 3.6 (b), the 40 Gbit/s capacity is attainable for the 50-GHz channel-spaced AWGR with channel compensations. However, it is a challenge for the 12.5-GHz channel-spaced AWGR.

As shown in Figure 3.6 (d), most of the signal spectra are truncated by the 6-GHz AWGR bandwidth, leading to severe signal impairment. The signals may be recovered by using advanced equalization algorithms, but it will result in very complex digital signal processing. Moreover, even if the signals are possible to transmit over this bandwidth-limited channel, heavy spectra overlap will occur between odd channels or even channels that are 25-GHz channel-spaced. If the adjacent channels are polarization-orthogonal, the even channels or odd channels remain at the same polarization state, leading to the signal crosstalk. Thus, the crosstalk-mitigation scheme of using polarization-orthogonal channels does not work for further scaling up the channel capacity.

By combining the SRRC filtering and polarization orthogonality, a channel capacity of 40 Gbit/s is attainable for this bandwidth-limited high spatial resolution AWGR-based 2D IR beam-steered system. To transmit 40-Gbit/s data, the compressed signal bandwidth (double-sideband main lobe bandwidth) is 22 GHz (when $\beta = 0.1$), as shown in Figure 3.6 (f). This is equivalent to double the channel capacity with approximately halved signal bandwidth, which is acceptable for the bandwidth-limited channel. The crosstalk between adjacent channels (12.5-GHz spaced) is mitigated by polarization-orthogonality, and the crosstalk between even channels or odd channels (25-GHz spaced) is avoided by the 3-GHz guard band. Thus, 40-Gbit/s data transmission per beam is attainable by combining the proposed signal bandwidth compression method and the orthogonal-polarization design.

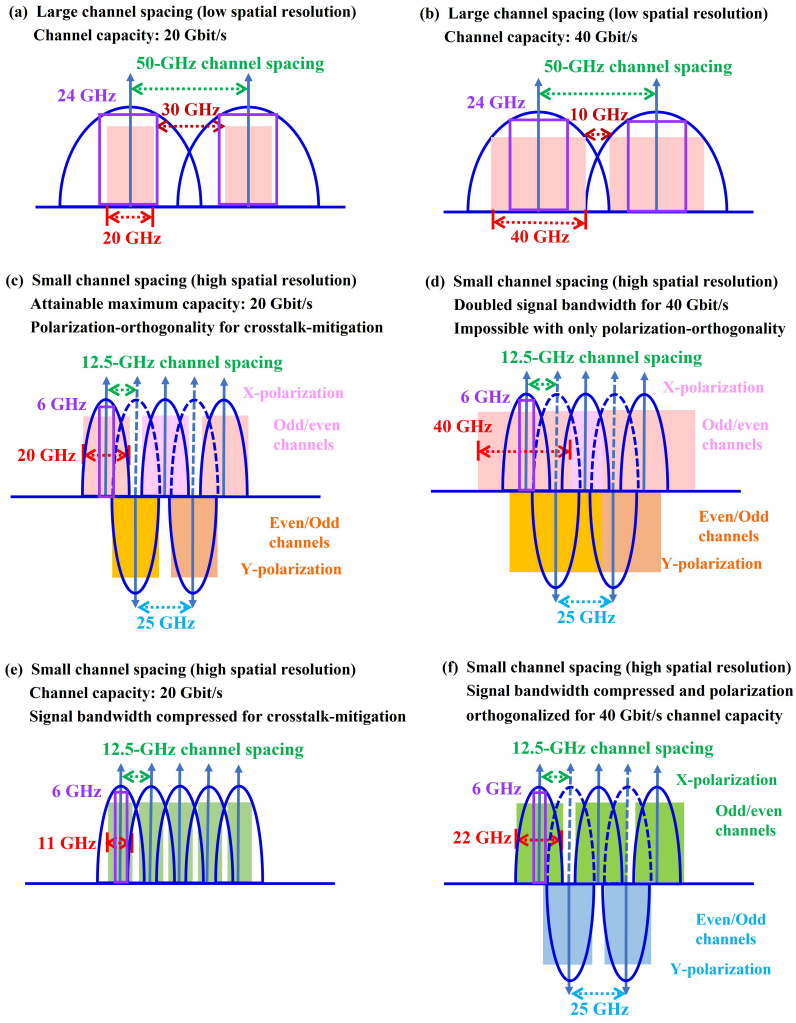

Figure 3.6: Principle of crosstalk mitigation and scaling up the channel capacity per beam for the high spatial resolution AWGR-based 2D IR beam-steered system.

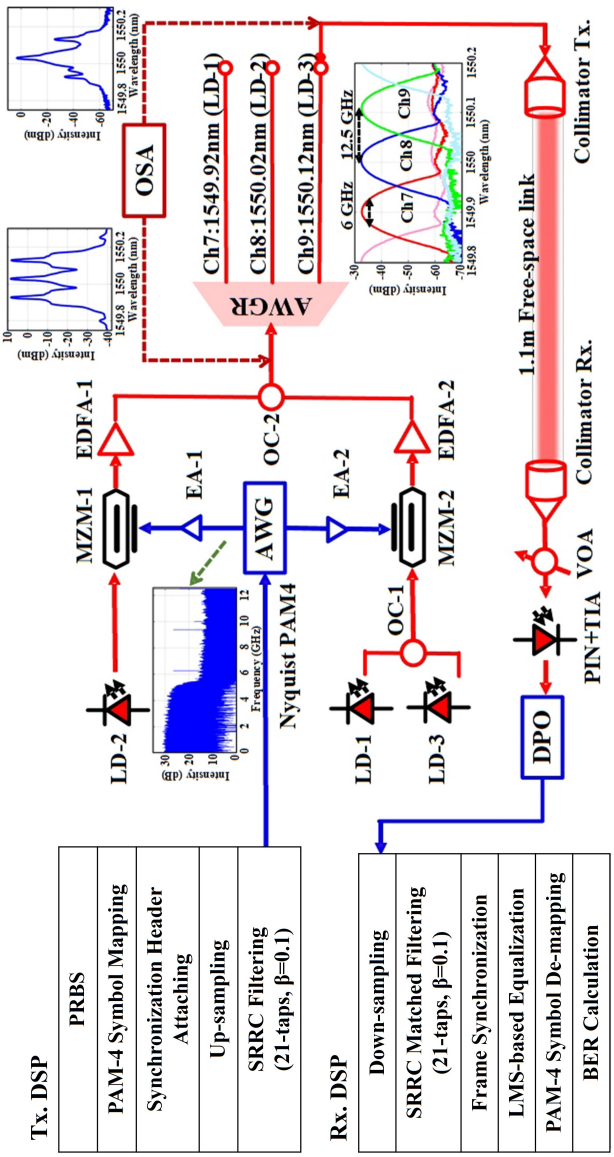

Figure 3.7: Experimental setup. Tx: transmitter; Rx: receiver; DSP: digital signal processing; PRBS: pseudo-random binary sequence; PAM-4: 4-level pulse amplitude modulation; SRRC: square-root raised-cosine; LMS: least mean square; BER: bit error rate; LD: tunable laser; MZM: Mach-Zehnder modulator; AWG: arbitrary waveform generator; EA: electrical amplifier; OC: optical coupler; EDFA: erbium-doped fiber amplifier; AWGR: arrayed waveguide grating router; OSA: optical spectrum analyzer; VOA: variable optical attenuator; PIN: pin-photodiode; TIA: trans-impedance amplifier; DPO: digital phosphor oscilloscope.

3.5 Experimental setup

For the experimental demonstration of the proposed method, a Gaussian-shaped commercial AWGR [115] featuring a 6-GHz 3-dB bandwidth and 12.5-GHz channel spacing is adopted, and the PAM-4 signal is used. Figure 3.7 presents the experimental setup. Three adjacent AWGR channels (1549.92 nm, 1550.02 nm, 1550.12 nm) labeled as Ch7, Ch8, and Ch9 are utilized, in which Ch8 is investigated in detail. The inset shows the response of the selected channels. The optical carriers are set at the center of the corresponding AWGR channels using three independently tunable lasers (LD-1, LD-2, LD-3) provided by the Keysight N7714A four-port tunable laser system source. On the digital transmitter side, a pseudo-random binary sequence (PRBS) with a periodicity of $2^{23} - 1$ is generated and mapped on the PAM-4 symbols. After attaching the synchronization header (a PRBS of a $2^{11} - 1$ periodicity with zero padding before and after the PRBS), the PAM-4 symbol stream is up-sampled by 2 times and digitally filtered by the Nyquist filter before being uploaded to an arbitrary waveform generator (AWG, Tektronix, AWG7122B). The Nyquist filter we used here is the SRRC filter with a length of 21-taps and a roll-off factor of 0.1. (Small roll-off factor is used since the spectrum efficiency has the higher priority here and the signal quality can be improved by the equalization. Taking into account the implementation complexity, a filter length of 21-taps and a roll-off factor of 0.1 is utilized since a larger filter length and a smaller roll-off factor bring little performance improvement according to the experimental investigation.) The inset presents the electrical spectrum of the filtered PAM-4 signal. The filtered PAM-4 signal generated by the AWG is amplified by electrical amplifiers (EAs, SHF 100APP), and modulated onto the three optical carriers via two individual Mach-Zehnder modulators (MZM). Individual MZMs are utilized to de-correlate the adjacent signals. To simplify the hardware utilization, the two side channels (Ch7 and Ch9) share one MZM (MZM-2, Fujitsu, FTM7937EZ/204) which is implemented by combining LD-1 and LD-3 with an optical coupler (OC), while the central channel (Ch8) enjoys the dedicated MZM (MZM-1, SUMITOMO, T.MXH1.5-10PD-ADC-S). The three modulated signals are amplified by two EDFAs (Amonics AEDFA-PM-DWDM-23-B-FA and Highlight EDFA) and then combined by an OC. After being filtered by the AWGR, the λ-split signal is transmitted to a 1.1-m free-space link ($\sim$3.5-dB loss including the collimators) via a collimator (Thorlabs TC18FC-1550 with a beam diameter of $\sim$3.4 mm at 1.1 m [116]). An optical spectrum analyzer (OSA, Advantest Q8384) is utilized for measuring the optical spectra before and after the AWGR. The

two insets show the optical spectra of the transmitted modulated PAM-4 signals with digital Nyquist filters before and after AWGR. The receiver consists of a collimator (Thorlabs F810APC-1550) followed by a commercial photo-detector (DSC-R402PIN) which includes a 10-GHz pin-photodiode (PIN-PD) and a trans-impedance amplifier (TIA). A variable optical attenuator (VOA) is used for adjusting the received optical power, for performance measurements. The detected signal is sampled by a digital phosphor oscilloscope (DPO, Tektronix, DPO72304DX) at a sampling rate of 50 GSa/s and post-processed digitally. The digital signal processing at the receiver side mainly contains down-sampling, SRRC matched filtering, frame synchronization, least mean square (LMS)-based equalization, PAM-4 symbol de-mapping, and BER calculation.

3.6 Experimental results and discussions

3.6.1 Electrical spectra, optical spectra, and crosstalk

The electrical spectra of the transmitted signals are presented in Figure 3.8 (a). Due to hardware limitations in the lab, the transmission data rate was targeted at 20 Gbit/s (10-GBaud/s PAM-4) for this experimental investigation. A PAM-4 signal without digital Nyquist filtering is plotted as a reference (red), the single-sideband main lobe bandwidth is 10 GHz and the first side lobe level is just about -10 dB below the main lobe. Whereas by employing the digital Nyquist filter (blue), the main lobe bandwidth is compressed to around 5.5 GHz (the 3-dB bandwidth is about 4.7 GHz) and the side lobe is efficiently suppressed to nearly 10 dB which is mainly noise floor caused by the DPO.

The optical spectra of the modulated signals before AWGR is shown in Figure 3.8 (b), the digitally filtered PAM-4 signal (blue) occupies narrower spectra than the signal without digital Nyquist filters (red). As shown in Figure 3.8 (c), the AWGR has a 12.5-GHz channel spacing, and the measured crosstalk into Ch8 from optical carriers of adjacent channels is -34 dB and -27 dB from Ch7 and Ch9, respectively. The optical spectra of the modulated signals (dotted line) and the crosstalk strength (solid line) after AWGR (Ch8) are presented in Figure 3.8 (d), which is measured by switching LD-2 on and off. The strength of carrier leakage from Ch7 and Ch9 is -35 dB and -27 dB, respectively, resulting from the AWGR response. The crosstalk of the PAM-4 signal (red) is mainly caused by the main lobe and first side lobe, which is almost mitigated by using digital Nyquist filters (blue).

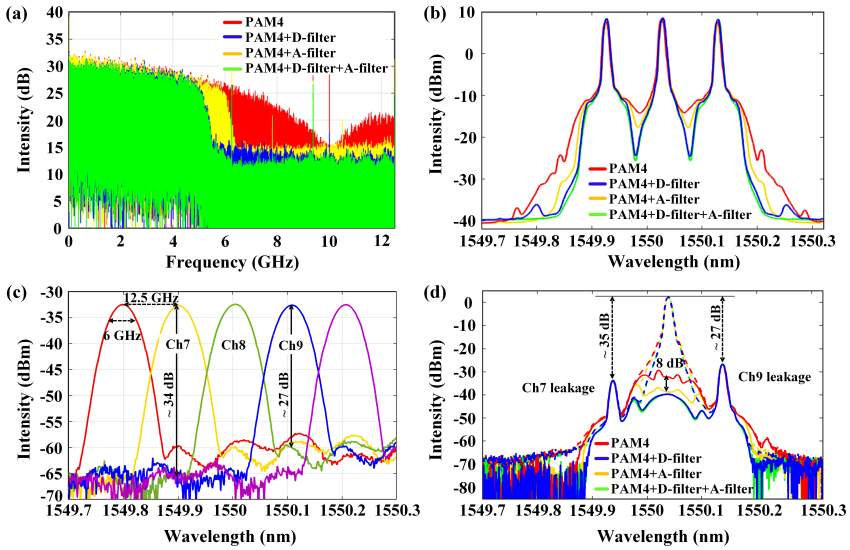

Figure 3.8: (a) Electrical spectra of the transmitted signals (D-filter: digital Nyquist filtering; A-filter: analog filtering); (b) optical spectra of the transmitted modulated signals before AWGR; (c) AWGR response; (d) optical spectra of the transmitted modulated signals (dotted line) and the crosstalk strength (solid line) after AWGR (Ch8).

3.6.2 Channel performance

Prior to investigating the crosstalk impact in the experimental demonstration, we have investigated the impact of the channel limitation and the impact of the signal shaped by the digital Nyquist filter. By turning LD-2 on, LD-1 and LD-3 off, the performance of the single-channel (Ch8) link with no crosstalk is investigated. We measure the bit error rate (BER) versus received optical power curves to evaluate the system performance. As shown in Figure 3.8 (c), the 3-dB bandwidth of the AWGR is 6 GHz, which is the bottleneck of this system. Figure 3.9 (a) shows the BER performance without (square) and with (circle) AWGR. Without the AWGR, the channel bandwidth is limited to about 10 GHz (double-sideband), and the BER performance (receiver sensitivity at the 7% FEC limit of 1×10^{-3}) of the PAM-4 signal with digital Nyquist filter (5.5-GHz single-sideband main lobe bandwidth, blue square) is 1.2 dB worse than that of the PAM-4 signal without digital Nyquist filter (10-GHz single-sideband main lobe bandwidth, red square). The impact of the channel bandwidth limitation is weaker, so the difference is mainly the impact of signal bandwidth compression

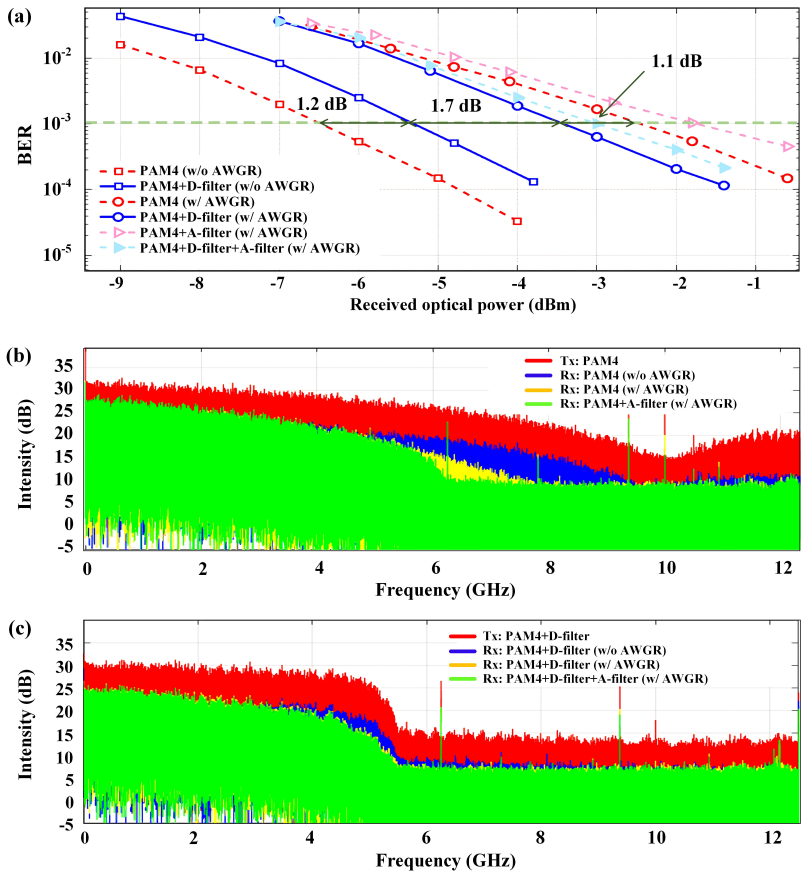

Figure 3.9: Channel performance (central channel, without side channels): (a) measured BER versus received optical power curves; (b) electrical spectra of the transmitted PAM-4 signal and received signals without digital Nyquist filter; (c) electrical spectra of the transmitted PAM-4 signal and received signals with digital Nyquist filter. D-filter: digital Nyquist filtering; A-filter: analog filtering.

by using the digital Nyquist filter. With the AWGR, the channel bandwidth is limited to about 6 GHz (double-sideband). The BER performance of the PAM-4 signal (red) deteriorates significantly ($\sim$ 4-dB at the 7% FEC limit of 1×10^{-3}) due to the heavy spectrum truncation by the AWGR, while the performance deterioration of the case with the digital Nyquist filter (blue) is 2.3-dB smaller since most of the compressed spectrum is within the passband of the AWGR. Hence, a 1.1-dB improvement of receiver sensitivity at the 7% FEC limit of

1×10^{-3} is obtained by using the digital Nyquist filter for this 6-GHz bandwidth-limited AWGR-based 2D IR beam-steered system.

The electrical spectra of the received signal without and with digital Nyquist filters are also plotted in Figure 3.9 (b) and (c), respectively.

3.6.3 Impact of crosstalk

By turning all the lasers (LD-1, LD-2, LD-3) on, the impact of crosstalk from adjacent channels (Ch7, Ch9) is evaluated. A polarization controller is inserted after EDFA-2 to maximize the crosstalk by tuning all the channels to the same polarization state, so we measure the worst case. The crosstalk is visualized in the electrical spectra by turning off the signal for Ch8, as shown in Figure 3.10 (b). Strong crosstalk is observed when transmitting the PAM-4 signals (red), which causes performance deterioration. The crosstalk only remains a little when the digital Nyquist filters are employed (blue). As depicted in Figure 3.10 (a), there is an apparent error floor in the curve (red) and the BER is maintained at a high level when the digital Nyquist filters are absent. By using the digital Nyquist filters (blue), the BER is improved to $\sim 2 \times 10^{-4}$, which allows 20-Gbit/s data transmission.

Different transmission data rates (10-GBaud/s, 9-GBaud/s, 8-GBaud/s) are explored as well. As shown in Figure 3.11, the BER performance improves as the data rate decreases since the signal is less affected by the AWGR filtering.

3.6.4 Evaluation of digital Nyquist filtering versus analog filtering

Two 5.5-GHz (passband, loss $<$ 2 dB) electrical analog filters (Mini-Circuits VLF-5500+) are also introduced before the electrical amplifiers for comparison. The electrical spectra of the transmitted signals after analog filtering are also presented in Figure 3.8 (a). The PAM-4 signal is directly truncated with the analog filter (yellow), so the side lobes are reduced and part of the main lobe is cut off. 8-dB reduction of the inter-channel crosstalk is achieved by using analog filters, as shown in Figure 3.8 (d) (yellow). The BER performance of the single-channel link with the analog filter is slightly deteriorated due to the filtering (dot red triangle in Figure 3.9 (a)), and the BER is improved to $\sim 3 \times 10^{-3}$ when considering the crosstalks from adjacent channels (dot red triangle in Figure 3.10 (a)). Nevertheless, the improvement is weaker than the method using digital Nyquist filters (blue in Figure 3.10 (a)). If we cascade the analog filter with the digital Nyquist filter, little impact is foreseen on the spectra (green in Figure 3.8 (a) and (b)) since the digitally filtered signal is within the passband of the

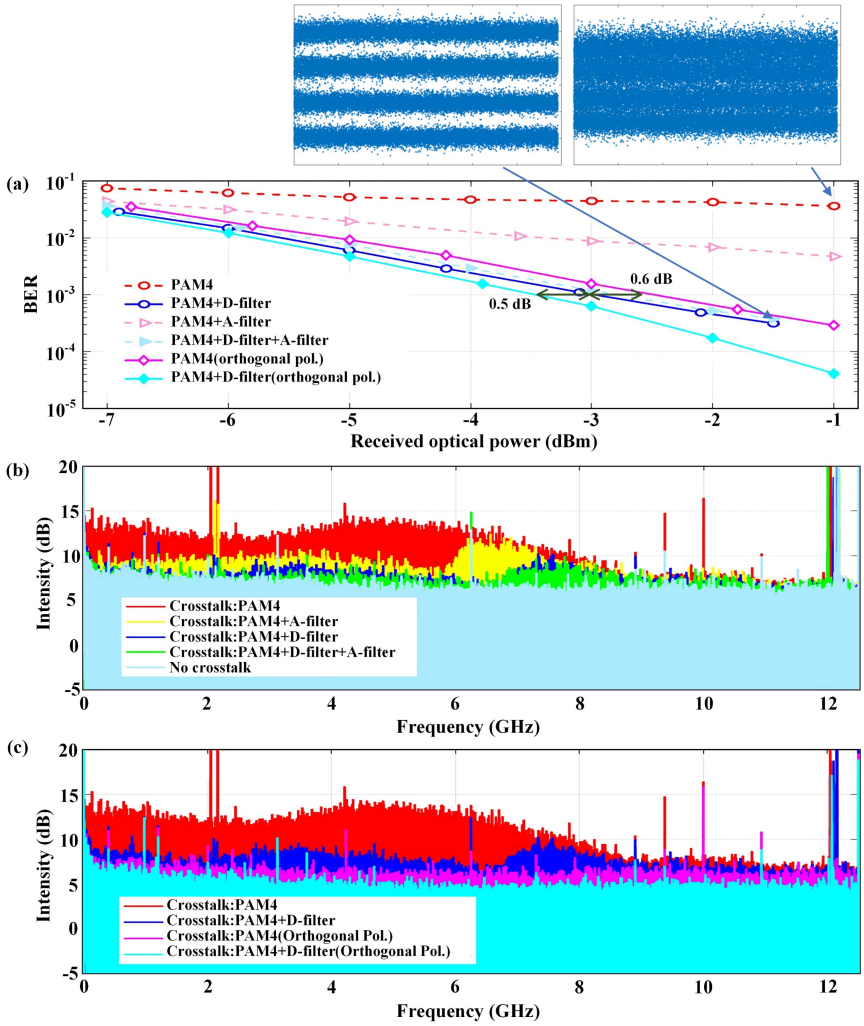

Figure 3.10: Impact of crosstalk (with side channels): (a) measured BER versus received optical power curves; (b) electrical spectra of the crosstalk for various cases of signals with same polarization; (c) electrical spectra of the crosstalk comparison between signals with same polarization and signals with orthogonal polarization. D-filter: digital Nyquist filtering; A-filter: analog filtering; Orthogonal Pol: orthogonal polarization.

analog filter, so the BER performance maintains (dot blue triangle in Figure 3.10 (a)). Thus, the proposed method using digital Nyquist filters performs better than that using analog filters. It is unnecessary to introduce extra analog filters, which meet the cost-efficient requirement of this system.

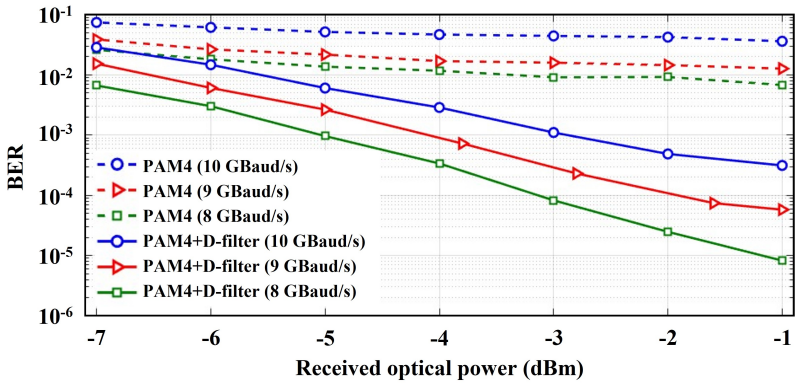

Figure 3.11: Measured BER versus received optical power curves for different transmission data rates (with side channels). D-filter: Digital Nyquist filtering.

3.6.5 Evaluation of digital Nyquist filtering versus polarization-orthogonal channels

We also compare the proposed method with the crosstalk-mitigation technique in [111] which uses polarization-orthogonal signals in adjacent AWGR channels. By replacing OC-2 with a polarization beam combiner (PBC), the polarization of the adjacent signals can be set as the orthogonal state. Two polarization controllers are also inserted before two input ports of the PBC to minimize the power loss of signals at the corresponding polarization state. It has been proven effective for crosstalk mitigation. As shown in Figure 3.10 (c), nearly zero crosstalk remains (magenta). Thus, the BER performance of polarization-orthogonal channels (magenta and cyan in Figure 3.10 (a)) remains almost the same as the case of single-channel performance without crosstalk (dot red circle and blue circle in Figure 3.9 (a)). The receiver sensitivity of the single-channel with a digital Nyquist filter (blue circle in Figure 3.9 (a)) has a 1.1-dB improvement compared to the case without a digital Nyquist filter (dot red circle in Figure 3.9 (a)), but the receiver sensitivity of the triple-channels with digital Nyquist filter and same polarization (blue circle in Figure 3.10 (a)) is only about 0.6 dB (not 1.1 dB) better than the case of using polarization-orthogonal signals (without digital Nyquist filter, magenta in Figure 3.10 (a)) since there is still residual crosstalk (blue in Figure 3.10 (c)) with the same polarization. By combining the proposed solution of using the digital Nyquist filtering and polarization-orthogonal channels, the additional 0.5-dB improvement of receiver sensitivity at the 7% FEC limit of 1×10^{-3} (cyan in Figure 3.10 (a)) is obtained since

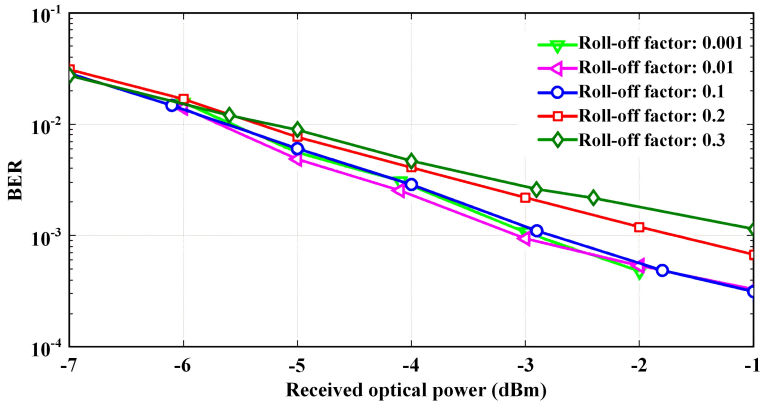

Figure 3.12: Measured BER versus received optical power curves with different roll-off factors of the SRRC filters.

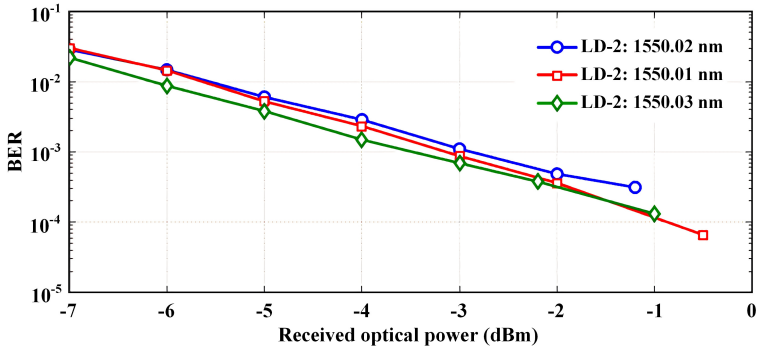

Figure 3.13: Measured BER versus received optical power curves with wavelength shift of laser sources.

the residual crosstalk (blue in Figure 3.10 (c)) is mitigated with polarization-orthogonal channels (cyan in Figure 3.10 (c)).

3.6.6 Impact of SRRC filtering roll-off factors

Figure 3.12 compares the BER performance of the digital Nyquist filter-aided system with different roll-off factors, β. The receiver sensitivity diminishes as β increases because the less compressed signal bandwidth causes more crosstalk to the adjacent channels. When β is smaller than 0.1, there is no significant performance improvement, except that the implementation complexity increases. Thus, an optimum roll-off factor for our experimental demonstration is 0.1.

3.6.7 Impact of wavelength misalignment

In addition, the impact of wavelength misalignment among the laser sources and AWGR channels is evaluated. As shown in Figure 3.13, the BER performance improves slightly when the wavelength of LD-2 is shifted by 0.01 nm. Thus, the proposed method has a good tolerance of wavelength misalignment between the laser sources and AWGR channels, which releases the strict design constraint of wavelength stable lasers and precise AWGRs.

3.7 Conclusion

In the AWGR-based 2D IR beam-steered system, a trade-off between the system spatial resolution and the channel capacity per beam should be considered. To increase the channel capacity for this system with a high spatial resolution, we proposed to take advantage of the Nyquist pulse shaping technique in this chapter. By shaping the transmitted signal for narrow spectral occupancy, the inter-channel crosstalk resulting from the imperfect AWGR filtering can be reduced, which enables using a denser AWGR grid. In addition, the spectral-efficient signal reduces the bandwidth requirement of the AWGR, which allows for a low-complexity AWGR design. The proposed method is not sensitive to the wavelength misalignment between AWGRs and lasers, which relaxes the design of high wavelength-stability lasers. Moreover, the proposed method is cost-efficient as we can make use of the mature DSP technique without requiring additional optical components. The proposed method has been experimentally investigated over a 6-GHz bandwidth-limited AWGR-based 1.1-m free-space link with the 20-Gbit/s data rate OWC capacity using PAM-4 format. The experimental results show the feasibility and effectiveness of the proposed method. By combining our proposed method with the polarization orthogonality technique in [111], a promising capacity per beam of 40 Gbit/s is potentially attainable.

As the cost of eliminating the trade-off between channel capacity per beam and system spatial resolution of the AWGR-based 2D IR beam-steered system, the introduced Nyquist pulse-shaping filter and matched filter lead to additional complexity for the DSP implementation. However, the combined filter length of our employed pulse-shaping filter and matched filter is only 21, resulting in a rather small additional implementation complexity. Whereas, the doubled sample rate requirement results from the employment of the digital Nyquist pulse shaping increases non-negligible complexity, which will be discussed in the next chapter.

4

Complexity reduction for the DSP-aided high spatial resolution AWGR-based 2D IR beam-steered OWC system

"Nothing in life is to be feared, it is only to be understood."

— Marie Curie —

This chapter focuses on the complexity reduction for the DSP-aided high spatial resolution AWGR-based 2D IR beam-steered OWC system. The digital Nyquist pulse shaping technique benefits our AWGR-based 2D IR beam-steered OWC system [68]. However, the doubled sample rate of the Nyquist pulse-shaped signal significantly increases the implementation complexity, for which we proposed to use the non-integer oversampling approach for complexity reduction. By minimizing the required sample rate with a rational oversampling factor (e.g. $1.1\times$ symbol rate when using SRRC filter with $\beta = 0.1$), the requirement of complex costly high-speed data converters is relaxed, thereby reducing the hardware cost and the power consumption. We have experimentally investigated its impact in the 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a 20-Gbit/s capacity and a minimum 11-GSa/s DAC sample rate [69].

4.1 DSP-aided high spatial resolution AWGR-based 2D IR beam-steered OWC system

The wavelength-controlled 2D IR beam-steered OWC system using the passive high port-count AWGR provides intrinsically high capacity and is cost- and power-efficient [35]. In this system, beam-steering is realized by just tuning the wavelength of each beam remotely. Each wavelength fitting on the grid of the AWGR maps to a specific 2D angular beam direction for an individual user device. In order to get a larger spatial coverage and support higher wireless connectivity density, beam steering with a higher spatial resolution is needed, resulting in the requirement of higher port-count AWGRs with dense grids. However, the channel capacity per beam is compromised by the spatial resolution of the AWGR-based beam-steering. By introducing the high-order modulation format and Nyquist pulse shaping technique, a larger channel capacity per beam with crosstalk-free dense-spaced AWGR channels is attainable. More details are given in Chapter 3.

4.2 Limitation from the sample rate of data converters

The employment of digital Nyquist pulse shaping usually increases the complexity of the hardware implementation. For example, a 2-fold oversampling is required for generating Nyquist pulse-shaped signals (two samples are generated for each transmitted symbol), leading to a doubled sampling rate requirement for the DAC and ADC. Unfortunately, high-speed data converters (DAC and ADC) with a high sample rate above 10 GSa/s are complex and costly. Taking advantage of Silicon-Germanium (SiGe) bipolar or Indium Phosphide (InP) Heterojunction Bipolar Transistor (HBT) technologies, sampling rates of tens of GSa/s are attainable [117, 118, 119, 120]. However, sophisticated high-speed interfaces are required since DSP is normally implemented in CMOS technology. CMOS data converters can benefit from the advanced process technology nodes (e.g. from 65 nm to 40 nm to 28 nm) and ride Moore's Law to higher speeds. However, the lower supply voltages of the advanced process technology nodes limit the signal swings of the analog circuits, leading to an increased speed at the price of a reduced dynamic range [121]. By utilizing parallel approaches such as time-interleaving and frequency-interleaving/spectral slicing techniques, CMOS data converters with sample rates approaching or above 100 GSa/s come within reach [122, 123]. However, complex calibration is required to compensate for the mismatch (e.g. gain mismatch, timing mismatch) between the parallel

sub-channels. In addition, the resolution of the data converters is compromised by the speed. Current high-speed CMOS data converters fabricated in the 16-nm FinFET process technology can achieve sample rates of up to 128 GSa/s with 8-bit nominal resolution at an average ENOB of 5.5 bits [45]. However, data converters fabricated in advanced process technology are extremely costly, and the limited resolution of the data converters decreases the precision of the digital Nyquist pulse-shaped signal.

4.3 Proposed solution

In this chapter, we propose to use a non-integer oversampling method [124, 125] to lower the sample rate requirement of the data converters, reducing the implementation complexity and power consumption of our digital Nyquist filtered AWGR-based 2D IR beam-steered OWC system. In order to efficiently make use of the available relatively low-cost data converters, the sample rates are minimized as close as possible to the symbol rates.

4.3.1 Digital Nyquist filtering with non-integer oversampling

Nyquist pulse-shaped signals offer an optimum spectral efficiency close to a theoretical limit and feature a high out-of-band suppression [113, 114, 28]. The signal bandwidth can be halved theoretically and exhibits a rectangular spectrum by using ideal Nyquist filters. However, the abrupt transition of the rectangular spectrum results in long pulse tails in the time domain, and ideal "brick wall" filters with infinite filter lengths are non-realizable. A widely-used Nyquist filter is the SRRC filter pair which features a smoother roll-off shaped spectrum. The SRRC filtering is equally split between the pulse-shaping filter on the transmitter side and matched filter on the receiver side. The symmetrical filter pair is preferred in order to maximize the SNR at the receiver. The signal bandwidth with SRRC pulse shape depends on the roll-off factor, β. The stopband frequency of the SRRC filtered signal is $0.5(1+\beta)R_S$, where R_S is the symbol rate and β ranges from 0 to 1.

According to the Nyquist sampling theorem, the minimum sampling rate is 2-fold of the signal bandwidth, which is $(1+\beta)R_S$ for the SRRC pulse-shaped signal theoretically. As shown in Figure 4.1, the spectra of the signal measured at the DAC outputs contain both the spectrum of interest and the so-called image spectra that repeat infinitely for an ideal DAC. The image spectra can be removed by electrical low-pass filters. To sample at the symbol rate would

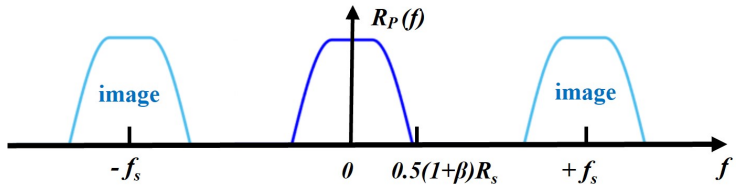

Figure 4.1: Electrical spectra of the transmitted Nyquist signal with oversampling/interpolation. R_S is the symbol rate, β is the roll-off factor which ranges from 0 to 1, and f_S is the sampling rate.

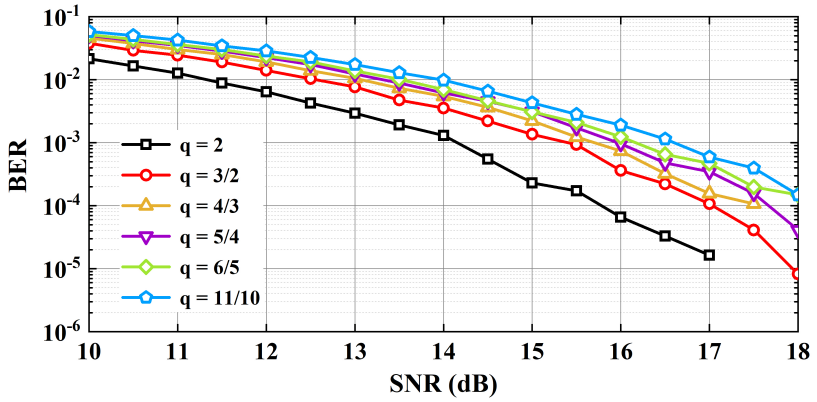

Figure 4.2: Simulated waterfall curves for various oversampling rates (SRRC-pulse-shaped PAM-4 signals with $\beta = 0.1$) in the AWGN channel. q: Oversampling factor.

call for non-realizable "brick wall" filters, thus oversampling is required. To avoid aliasing between the spectrum of interest and the image spectra, the minimum sample rate of the SRRC pulse-shaped signal is $(1+\beta)R_S$. The SRRC pulse-shaped signal gets a maximum spectra occupation when β is 1 and the minimum sample rate is 2-fold of R_S. The integer oversampling is normally utilized since the hardware implementation is straightforward, therefore, at least 2-fold oversampling is usually used in the SRRC pulse-shaping. By using non-integer oversampling, an oversampling factor smaller than 2 is attainable when β is smaller than 1. The simulated waterfall curves for various oversampling rates (q) based on the SRRC ($\beta = 0.1$, 21-taps) pulse-shaped PAM-4 signals which is the same scenario as the one addressed in Chapter 3, AWGN channel, and the same equalizer (LMS-updated FIR-based FFE with 151-tap and $\mu = 0.01$ where μ is the adaptive update step) are presented in Figure 4.2, where q

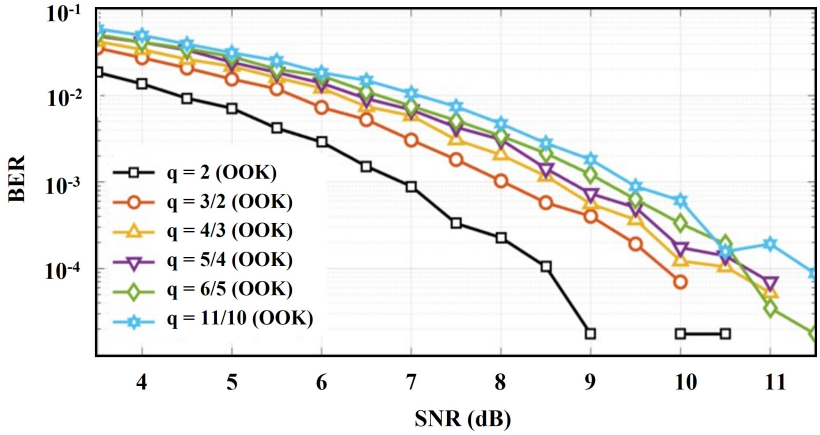

Figure 4.3: Simulated waterfall curves for various oversampling rates (SRRC-pulse-shaped OOK signals with $\beta = 0.1$) in the AWGN channel. q: Oversampling factor.

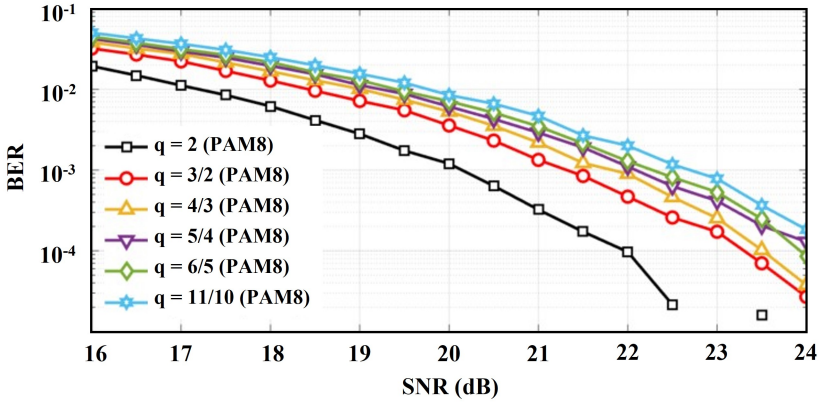

Figure 4.4: Simulated waterfall curves for various oversampling rates (SRRC-pulse-shaped PAM-8 signals with $\beta = 0.1$) in the AWGN channel. q: Oversampling factor.

is the oversampling factor defined by Eq. (4.1) and a minimum value is $1 + \beta$. It shows that a 2.3-dB larger SNR is required to achieve the 7% FEC limit of 1×10^{-3} if q is reduced from 2 to 1.1. The simulation results of the Nyquist OOK system and Nyquist PAM-8 system under the same assumptions (except that the adaptive update step of the equalizer is $\mu = 0.005$ for the Nyquist OOK system) are also presented in Figure 4.3 and Figure 4.4, respectively.

$$q = \frac{sample\ rate\ f_S}{symbol\ rate\ R_S}. \tag{4.1}$$

4.3.2 Complexity analysis

At a given technology node, DACs and ADCs may be combined in parallel to augment their sample rate and bandwidth. Figure 4.5 and Figure 4.6 exhibit the architectures which can double the DAC effective sample rate and ADC

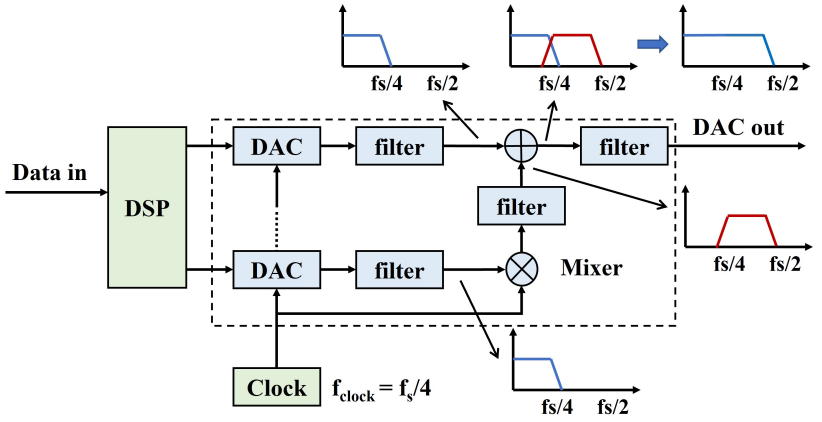

Figure 4.5: Architecture for extending DAC sample rate [120]. f_S: Sample rate of combined DAC outputs.

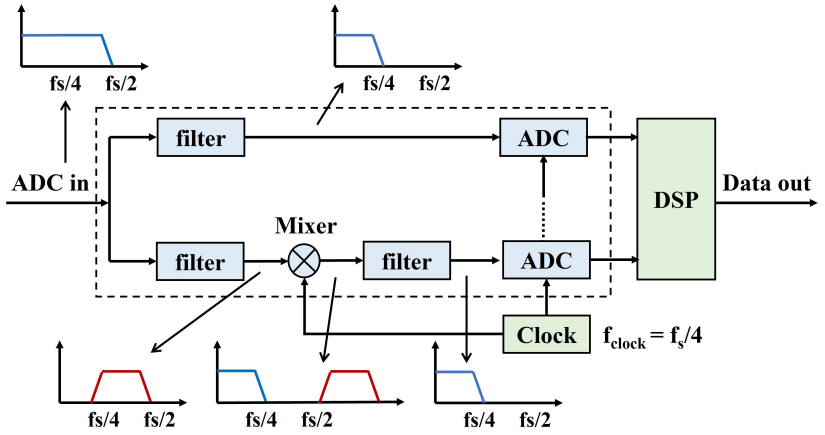

Figure 4.6: Architecture for extending ADC sampling rate [120]. f_S: Sampling rate of combined ADC inputs.

effective sampling rate, respectively [120]. The combination of multiple DACs and ADCs increases the hardware cost and power consumption. Instead, non-integer oversampling minimizes the required sample rate as close as possible to the symbol rate, which allows making use of the available relatively low-cost data converters (DAC and ADC), thereby reducing the implementation complexity and power consumption for our DSP-aided AWGR-based 2D IR beam-steered OWC system at a given symbol rate.

Non-integer oversampling not only relaxes the sampling rate requirement of the data converters but also reduces the computational effort of the DSP implementation. For the pulse-shaping with an integer oversampling factor $q = p$, $p \times R_S$ samples should be calculated. For the non-integer oversampling with a factor of $q = k/l$, only $k/l \times R_S$ samples are calculated.

In terms of the digital pulse shaping implementation with integer oversampling, the transmitted symbols are interpolated and convoluted with the pulse-shaped filter coefficients directly. Take $q = p = 2$ as an example, the operation is presented in Figure 4.7. All the 21 points (assume that the pulse shaping filter length is 21) are used for the calculation and need to be summed up for generating 2 samples per symbol.

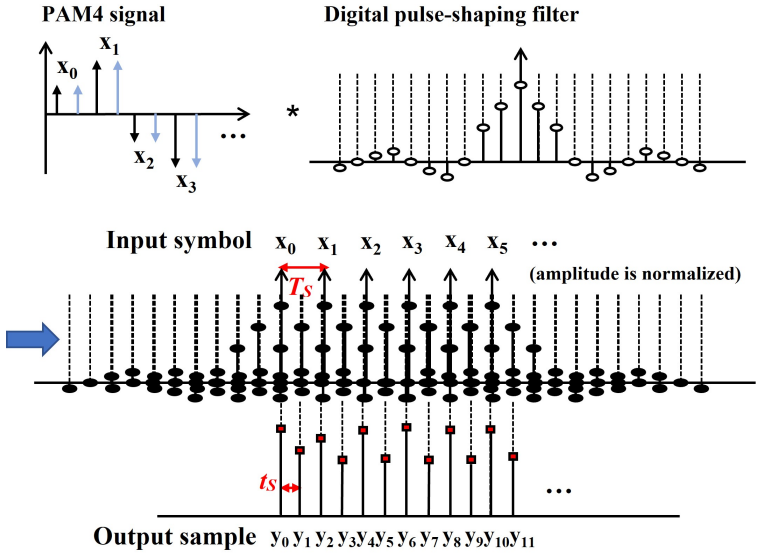

Figure 4.7: Example of digital pulse shaping with integer oversampling, $q = 2$. T_s: Symbol period with interpolation; t_s: sample period.

As for the digital pulse shaping implementation with non-integer oversam-

pling, take $q = k/l = 4/3$ as an example, the operation is presented in Figure 4.8. Normally, $4/3$-fold oversampling means we need to interpolate 3 samples for each symbol first, then operate convolution with pulse-shaped filter coefficients (amplitude is normalized in Figure 4.8). After that, we only need the results every 3 samples (2 samples are skipped) for generating the output waveform. The results which are not finally used waste some computational efforts, hence we can skip the calculation of those useless results which do not contribute to the output waveform. We only need to calculate and sum up the solid points in Figure 4.8 (a) for generating the output waveform (4 output samples per 3 input symbols). It should be noted, as the sample period t_s is a fraction of the symbol period T_s, the useful samples are located at different positions in each symbol period T_s, distributed unevenly for each symbol (2 samples come from the same symbol, the other 2 samples come from the other 2 symbols), and repeated periodically every $l = 3$ symbols. As shown in Figure 4.8 (b), the position of each symbol period (with interpolation of 3 samples, so 1 symbol period is represented by 4 samples duration) is labeled as A, B, C, D. The useful samples are located in 'A, D' of 'symbol x_0', 'C' of 'symbol x_1', 'B' of 'symbol x_2', then 'A, D' of 'symbol x_3', 'C' of 'symbol x_4', 'B' of 'symbol x_5'. The position repeats every 3 symbols. The repetition of every 3 symbols will benefit the implementation, it is equivalent to that 3 different pulses (black, green, and red in Figure 4.8 (c)) are needed for the calculation. For each symbol, the convolution of filter length is reduced (only 7 solid points of the total 21 points are used for the calculation). The calculation of each solid point can be multiplication or obtained from the look-up table (LUT). Then the solid points are summed up at the same sample instant to generate the output waveform.

The solid points of both the Figure 4.7 and Figure 4.8 (a) can be pre-calculated with the given symbol values and the SRRC filter coefficients. Hence, the main computation here is, to sum up the solid points. Therefore, the DSP computational effort is relaxed by $\frac{k}{l \cdot p}$, reducing the complexity of hardware implementation.

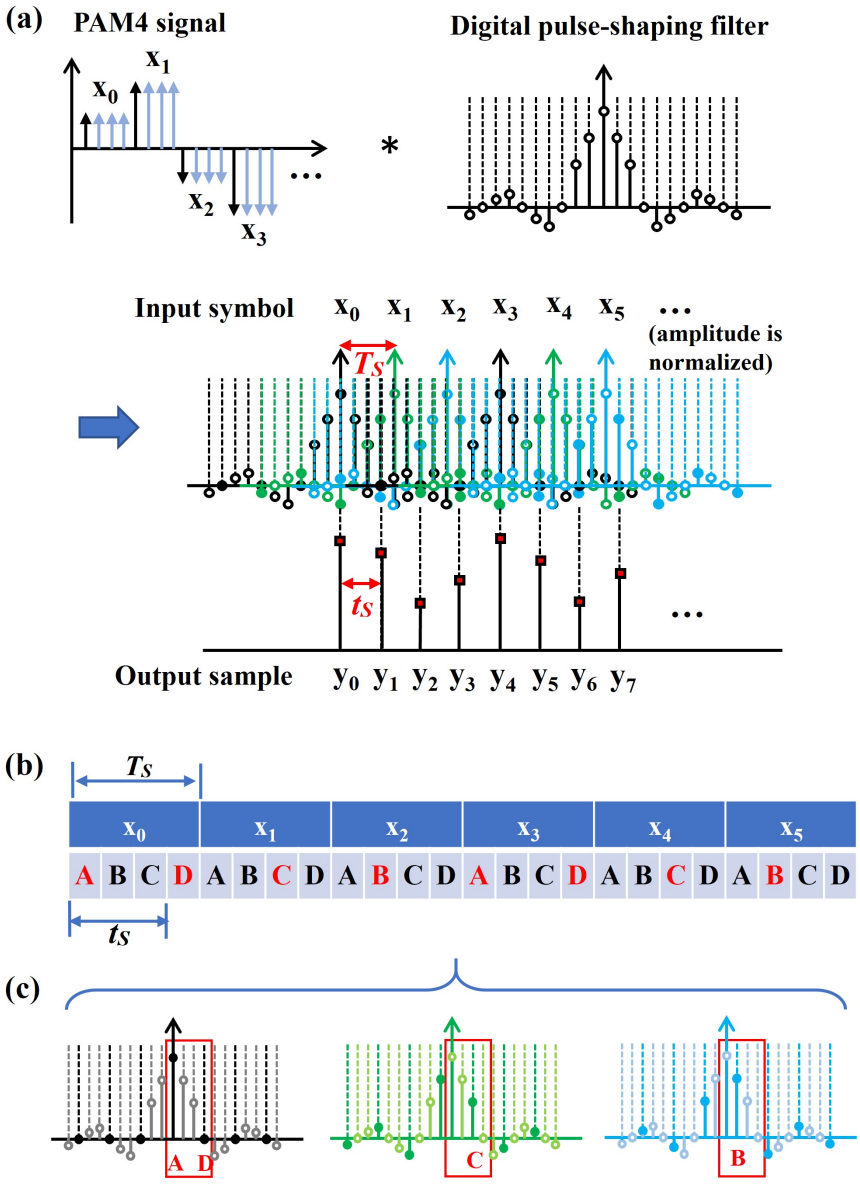

Figure 4.8: Example of digital pulse shaping with non-integer oversampling, $q = 4/3$. (a) Only the solid points need to be summed up for generating the output waveform, the circle ones are skipped. (b) Position of the useful samples repeats periodically every 3 symbols. (c) Equivalent 3 different pulses with only 1/3 filter length. T_s: Symbol period with interpolation; t_s: sample period.

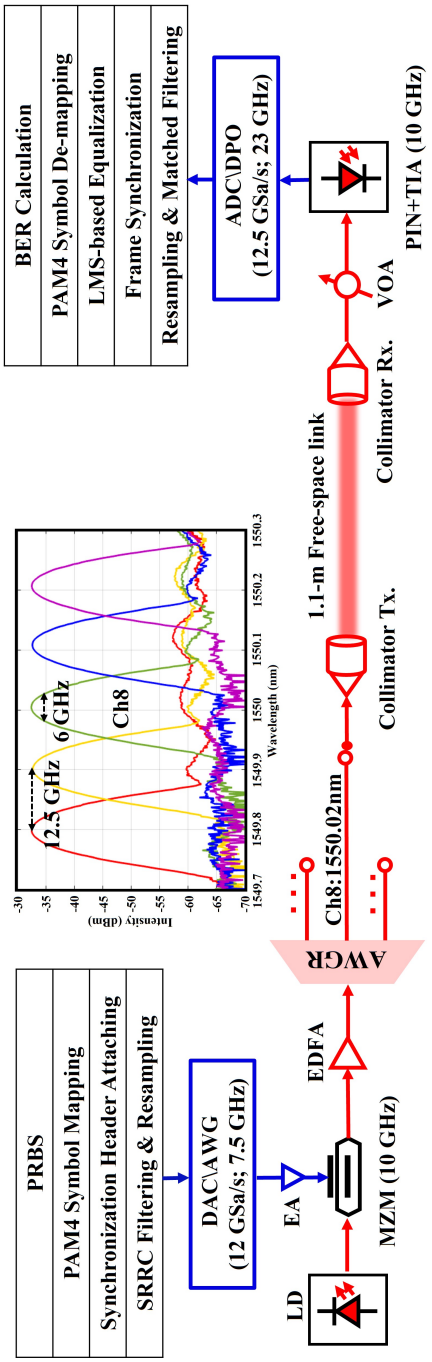

Figure 4.9: Experimental setup. Tx: transmitter; Rx: receiver; PRBS: pseudo-random binary sequence; PAM-4: 4-level pulse amplitude modulation; SRRC: square-root raised-cosine; LMS: least mean square; BER: bit error rate; LD: tunable laser; MZM: Mach-Zehnder modulator; DAC: digital to analog converter; AWG: arbitrary waveform generator; EA: electrical amplifier; OC: optical coupler; EDFA: Erbium-Doped fiber amplifier; AWGR: arrayed waveguide grating router; VOA: variable optical attenuator; PIN: pin-photodiode; TIA: trans-impedance amplifier; ADC: analog to digital converter; DPO: digital phosphor oscilloscope.

4.4 Experimental setup

The experimental setup is presented in Figure 4.9. A C-band Gaussian-shaped commercial 16-ports AWGR [115] with 6-GHz 3-dB bandwidth and 12.5-GHz channel spacing is adopted in this experimental investigation, which is the same as the one addressed in Chapter 3. The inset shows part of the AWGR response (Ch6 - Ch10). Multiple optical carriers of various wavelengths (1549.3 nm - 1550.8 nm) can be fed to the AWGR, and the optical carrier with a wavelength fitting the corresponding AWGR channel will be received. Here, the AWGR channel labeled as Ch8 is investigated and the optical carrier is set at the center of the Ch8 (1550.02 nm) using a tunable laser. Due to the hardware limitation in the lab, we make use of an AWG (Tektronix, AWG7122B) as the DAC and take a DPO (Tektronix, DPO72304DX) to act as the ADC. The PAM-4 signal is used in this experimental investigation. On the digital transmitter side, a PRBS with a periodicity of $2^{23}-1$ is generated and mapped on the PAM-4 symbols. After attaching the synchronization header (a PRBS of a $2^{11}-1$ periodicity with zero padding before and after the PRBS), the PAM-4 symbol stream is pulse shaped by the SRRC filter with a length of 21 taps and a roll-off factor of 0.1. Then the filtered PAM-4 signal is re-sampled and uploaded to the AWG featuring a maximum sample rate of 12 GSa/s, 7.5-GHz output bandwidth, and 10-bit resolution. The PAM-4 signal generated by the AWG is amplified by an EA (SHF 100APP), and modulated onto the optical carrier via a 10-GHz MZM (SUMITOMO, 214 T.MXH1.5-10PD-ADC-S). An EDFA is utilized to provide enough power budget (about 20 dB from the laser to the photo-detector) for the transmission link. After being filtered by the AWGR, the λ-split signal is transmitted and received over a 1.1-m free-space link (about 3.5-dB loss from collimator Tx. to collimator Rx.) via a pair of collimators (Thorlabs TC18FC and Thorlabs F810APC-1550). The received signal is detected by a commercial photo-detector which includes a 10-GHz PIN-PD and a TIA. A VOA is used for adjusting the received optical power, for performance measurements. The detected signal is sampled by the 23-GHz DPO at 12.5 GSa/s and post-processed digitally. The digital signal processing at the receiver side mainly contains resampling, SRRC matched filtering, auto-correlation-based frame synchronization, LMS-based equalization, PAM-4 symbol de-mapping, and BER calculation.

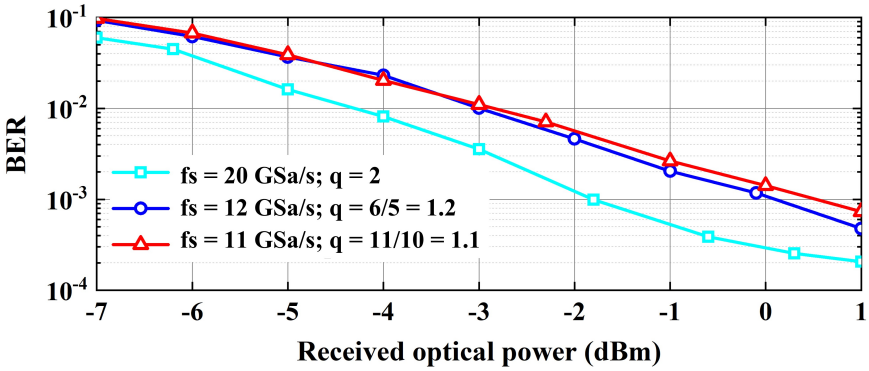

Figure 4.10: Measured BER versus received optical power curves with different DAC sample rates (f_s) for a transmission symbol rate of 10 GBaud/s and an SRRC filter length of 21, $\beta = 0.1$. q: Oversampling factor.

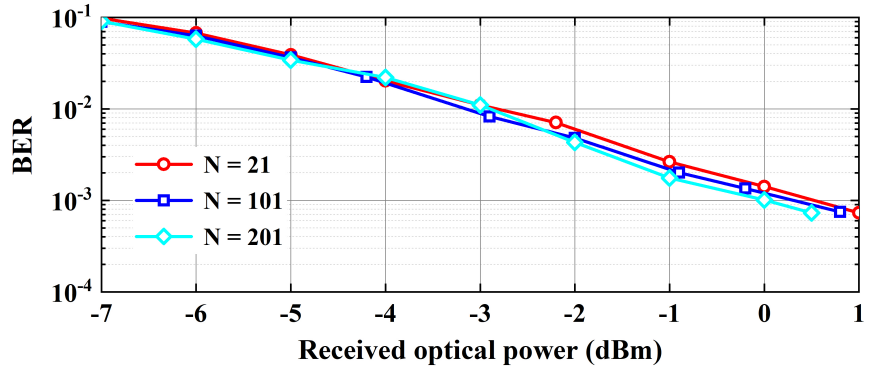

Figure 4.11: Measured BER versus received optical power curves with different SRRC filter lengths, N, with $\beta = 0.1$ for a transmission symbol rate of 10 GBaud/s, an DAC sample rate of 11 GSa/s, and $q = 1.1$.

4.5 Experimental results and discussions

The BER curves across the received optical power (input power of the photodetector) are measured for the system performance evaluation. We have firstly verified the feasibility of non-integer oversampling with an oversampling factor of 1.1 and 1.2 for the 10-GBaud/s Nyquist PAM-4 signal transmission when the AWG/DAC operates at 11 GSa/s and 12 GSa/s. As depicted in Figure 4.10 (triangle and circle), the receiver sensitivity is 0.5 dBm (1.1-fold) and 0.2 dBm (1.2-fold) at the 7% FEC limit of 1×10^{-3}, respectively. By using the interleaving option which enables a DAC sample rate of 20 GSa/s, we also measured the

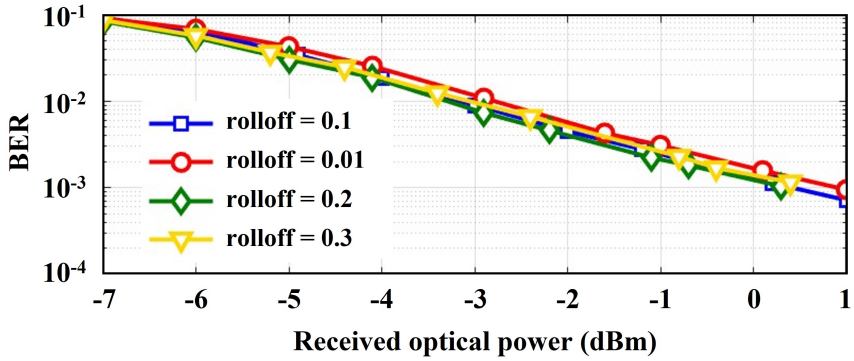

Figure 4.12: Measured BER versus received optical power curves with different SRRC roll-off factors and a 21-taps SRRC filter length for a transmission symbol rate of 10 GBaud/s, an DAC sample rate of 11 GSa/s, and $q = 1.1$.

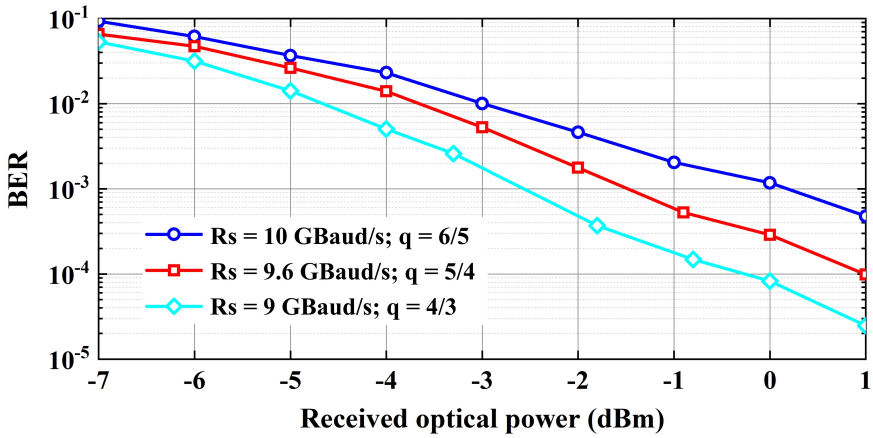

Figure 4.13: Measured BER versus received optical power curves with different transmission symbol rates (R_s) at an DAC sample rate of 12 GSa/s and an SRRC filter length of 21, $\beta = 0.1$. q: Oversampling factor.

BER performance of the 2-fold oversampling for the 10-GBaud/s Nyquist PAM-4 signal transmission, as shown in Figure 4.10 (square). A 25-GSa/s DPO/ADC sampling rate is required when the DAC sample rate is 20 GSa/s. The 25-GSa/s DPO sampling rate results in higher noise suppression, leading to a better BER performance. Compared to the 2-fold oversampling, a 2.3-dB power penalty is observed for the 1.1-fold oversampling at the 7% FEC limit of 1×10^{-3}, which is the cost of the complexity reduction.

Figure 4.11 compares the BER performance with different SRRC filter lengths

at $\beta = 0.1$ for a transmission symbol rate of 10 GBaud/s, DAC sample rates of 11 GSa/s ($q = 1.1$). It can be seen that a larger SRRC filter length causes little improvement of the signal quality. Thus, a small filter length (e.g. $N = 21$) can be used for low computational complexity. The BER performance with different SRRC roll-off factors and a 21-taps filter length under the same assumption is also investigated, as shown in Figure 4.12.

By adjusting the oversampling factor, the transmission symbol rate can be flexibly adjusted with a fixed sample rate. The BER performance of 10-GBaud/s ($q = 6/5$), 9.6-GBaud/s ($q = 5/4$) and 9-GBaud/s ($q = 4/3$) data transmission with 12-GSa/s DAC sample rate are presented in Figure 4.13. The BER performance improves as the data rate decreases since the signal is less affected by the 6-GHz AWGR filtering.

4.6 Conclusion

In this chapter, we have proposed to use a non-integer oversampling method to reduce the hardware implementation complexity and power consumption for our DSP-aided AWGR-based 2D IR beam-steered OWC system with high spatial resolution. By minimizing the oversampling of Nyquist signaling with a rational factor, the lower sample rate required relaxes the requirement of complex and costly high-speed data converters, and the power consumption is reduced. Also, the computational effort of the digital Nyquist signal implementation is reduced. We have experimentally investigated the impact of the non-integer oversampling approach in the 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a capacity of 20-Gbit/s data rate. The oversampling rate is minimized to $1.1 \times R_S$ (when using SRRC filter with $\beta = 0.1$) with a DAC sample rate of 11 GSa/s. Compared to the 2-fold oversampling Nyquist PAM-4 system, the DAC sample rate requirement is relaxed by 55%, with a cost of a 2.3-dB power penalty at the 7% FEC limit of 1×10^{-3}.

5

Latency reduction for the FPGA-based DSP implementation

"I just wondered how things were put together."

— Claude Shannon —

Low-complexity DSP techniques are efficient for low-cost high-capacity indoor OWC systems. In an effort for practical realization, this chapter focuses on the FPGA-based real-time DSP implementation. The speed limitation of FPGA forces the parallel implementation of the FPGA-based DSP algorithms. However, the classical semi-parallel implementation architecture introduces severe latency due to the massive intermediate data caching, which hinders the latency-critical applications. Hence, we propose to use a deeply parallel architecture, which does not require massive intermediate data caching, to reduce the total DSP-introduced latency. To enable the deeply parallel implementation, a new data re-allocation scheme is proposed to cope with the dependency of the FIR output on the successive input samples, and a look-ahead computation approach is employed to improve the adaptive update efficiency of the digital adaptive equalizer. An FPGA-based real-time digital PAM-4 receiver with deep-parallel DSP implementation is demonstrated in an experimental fiber link with a 2.5-Gbit/s data rate for the performance evaluation [70].

5.1 FPGA implementation of DSP algorithms

DSP techniques are proven to be efficient for low-cost high-capacity indoor OWC systems. However, the DSP algorithms are commonly experimentally demonstrated in an offline way which is convenient for algorithm development and customization. The offline DSP only provides the upper bound of the achievable system performance but does not consider the feasibility and limitation of the speed/throughput, latency, precision, resource/area utilization, and power consumption for hardware implementation. Not all offline DSP algorithms are suitable and efficient for hardware implementation. For example, offline DSP algorithms are usually utilized based on the assumption of one-symbol loop latency for the feedback loops, which is unattainable for practical implementation. Also, offline processing usually uses the full accuracy double precision (64-bit) floating-point data type while the fixed-point data type with limited precision is normally used for practical implementation, which may cause performance degradation. To further investigate the DSP algorithms constraints and estimate the performance for practical implementation, DSP algorithms are implemented on a FPGA platform which provides a cost-efficient manner for algorithm verification, performance estimation, and real-time/online demonstration. FPGA platform is also usually used to test and optimize the DSP algorithms before the expensive and unchangeable ASIC implementation.

An FPGA platform is composed of a finite number of predefined resources with programmable interconnects. FPGA resources are grouped in the so-called slices, which contain look-up tables (LUT), flip-flops (FF), multiplexers, and registers. The slices are connected via wide busses and switching nodes to create configurable logic blocks (CLB). Besides, the FPGA platform also offers a number of dedicated functional blocks or IP cores such as DSP, memory, clock managers, and gigabit transceivers. In the current commercial market, more advanced FPGA has also integrated high-speed PAM-4 transceivers. For example, Intel Stratix 10 TX FPGA [126] integrates 58-Gbit/s PAM-4 transceivers with advanced DSP including the linear equalizer, DFE, hardened FEC, etc. Xilinx has also integrated 58-Gbit/s PAM-4 transceivers into its 16-nm FinFET+ Virtex UltraScale+ FPGA family [127]. This chapter concentrates on the DSP implementation based on the regular FPGA platforms instead of using the gigabit PAM-4 transceivers on the advanced FPGA platforms. We take the implementation of the PAM-4 system as an example to acquire expertise in the hardware implementation of DSP algorithms. The implementation does not rely on a specific FPGA platform and the approaches are applicable to be extended

to other modulation formats and DSP algorithms.

There are also many reported works about the FPGA-based PAM-4 DSP implementation for optical transmission demonstrations. [128] has demonstrated a C-band 56-Gbit/s PAM-4 25-km fiber transmission in inter-data center network with FPGA-based real-time DSP including the LDPC coding, DFE, maximum likelihood sequence equalizer (MLSE), etc. In [129], K. Maragos et al. proposed a high-speed flexible FPGA-based FFE based on a custom multi-level parallel approach for optical interconnects up to 112 Gbit/s (56 GBaud/s with PAM-4 modulation). In [130], an FPGA-based FFE reconfigurable in baud-rate and modulation format is also demonstrated and investigated in both the 35-45-56 Gbit/s NRZ and 32-40 GBaud/s PAM-4 fiber transmission for data center networks. In this chapter, we concentrate on the implementation, latency analysis, and latency reduction of the low-complexity DSP algorithms for cost- and latency-sensitive applications.

5.1.1 DSP algorithms of a PAM-4 system

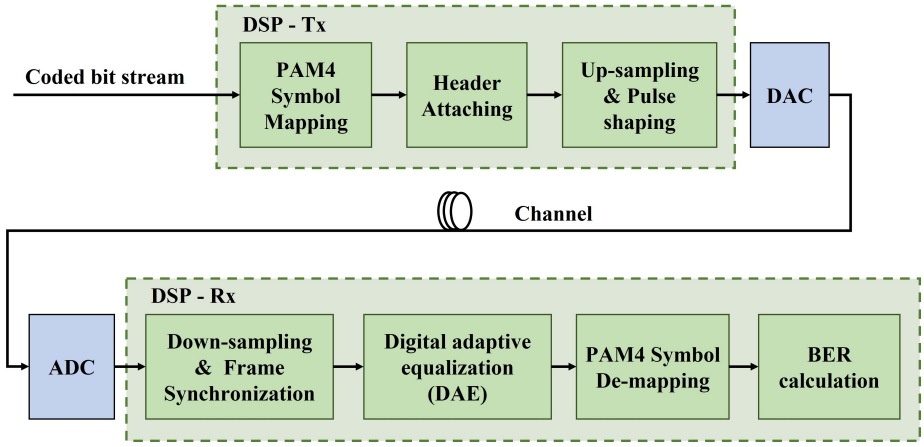

Figure 5.1: Block diagram of a digital PAM-4 transmission system. DAC: digital-to-analog converter, ADC: analog-to-digital converter.

The general block diagram of a digital PAM-4 system is shown in Figure 5.1. At the transmitter side, the coded bit stream is firstly mapped to PAM-4 symbol. Then synchronization header and training sequence are attached at the beginning of the symbol stream. After up-sampling and pulse shaping, the data stream is converted to an analog signal using a digital to analog converter (DAC). As for the receiver side, an analog to digital converter (ADC) is firstly used to

sample and quantize the received analog signal to digital signal. After down-sampling, frame synchronization is performed to get the start of the symbol stream. Then digital adaptive equalization (DAE) is used to track the variance of the channel and reduce ISI in real-time. Finally, the equalized and recovered symbol stream is de-mapped to the bit stream for error counting.

5.1.2 Limitation from the FPGA clock frequency

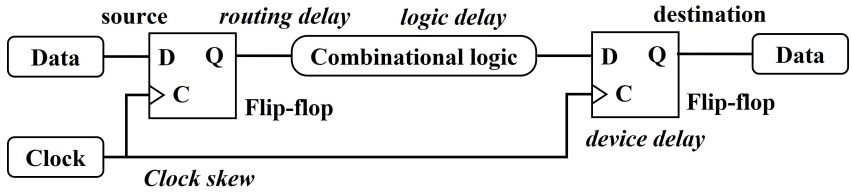

Figure 5.2: Example of a data path on FPGA.

One major limitation of FPGA is that its operation frequency (maximum clock frequency) is intrinsically limited to a few hundred MHz [131, 132]. The achievable clock frequency is limited by the data path delay. Figure 5.2 shows an example of a data path on FPGA. For the FPGA synchronous circuits, latching data into the FFs are synchronized by a set of clocks. When the data is transmitted from the source FF to the destination FF, the data path delay should be shorter than the clock period, otherwise, the destination clock can not capture the correct data which leads to the so-called timing issue. The data path delay consists of the logic delay, routing delay, and device delay. The achievable clock frequency depends on the critical data path of the design. To increase the clock frequency, the critical data path delay should be reduced with a well-designed timing. Normally, 200 MHz is achievable when using the Xilinx VC707 evaluation board featured with a Virtex-7 XC7VX485T-2FFG1761 device [133].

However, the OWC systems achieve a high data rate, in the order of tens of Gbit/s, which is far beyond the operation frequency of FPGA. Therefore, parallel implementation of the DSP algorithms is necessary to increase the data throughput for the OWC data rate (data rate = data throughput $\times$ clock frequency). The block diagram of parallel implementation is shown in Figure 5.3. The parallel implementation utilizes more resources, and the maximum number of parallel lanes is limited by the available FPGA resources.

Another limitation of FPGA is that FPGA with integrating high-speed data

converters [134] is expensive. Hence, external high-speed data converters are required.

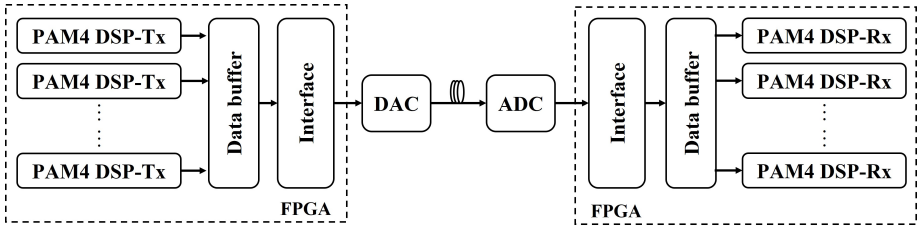

Figure 5.3: Block diagram of parallel implementation.

5.1.3 Parallel implementation architectures

In terms of parallel implementation, algorithm parallelism can be realized on different levels, as shown in Figure 5.4. For a classical straightforward parallel architecture, parallelism is only implemented on the top level, while parallelism from top to down is performed in the proposed deeply parallel architecture.

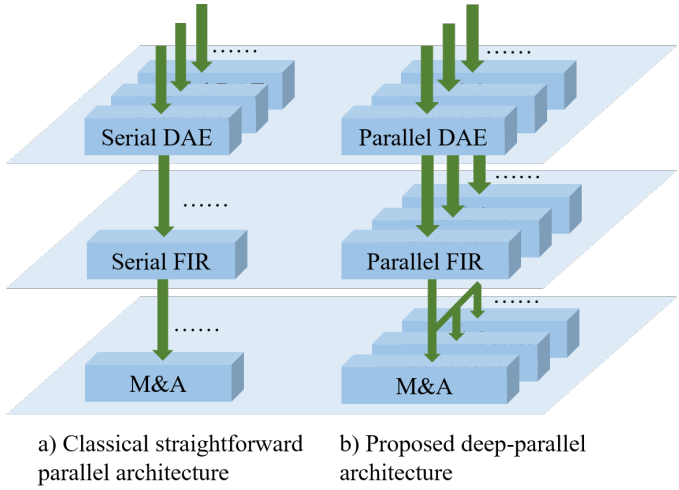

Figure 5.4: Parallelism of algorithms (e.g. DAE) with different depths. DAE: Digital adaptive equalization, FIR: finite impulse response filter, M&A: multiplication and addition operation.

Classical straightforward parallel architecture: pros and cons

The straightforward parallel architecture utilizes serial processing algorithms which are easier for implementation and require less computational hardware (e.g. multiplier and adder). However, parallel to serial conversion is required to enable serial processing algorithms in a parallel processing structure. It means that the incoming data with parallel streams should be written into a large memory column by column, then read out for serial processing row by row. This allows frames of data to be processed in a serial way, with no need for parallelizable algorithms. However, it requires large memory for the data caching and the data caching significantly increases the total latency. Also, the discontinuities need to be resolved at the start of each serial-processing block. To solve this, an overlap is needed between the serial processing blocks which further increases complexity, or a frame-based data structure with a training sequence is needed at the beginning of each serial processing block.

Proposed deeply parallel architecture: pros and cons

The deeply parallel architecture utilizes parallel processing algorithms which consume more computational hardware (e.g. multiplier and adder) and require parallelizable algorithms. Despite this drawback, it brings some benefits. As the incoming data with parallel streams can be processed continuously by the parallel processing algorithms, large memory is not required for intermediate data caching and the total latency is reduced significantly.

To enable the deeply parallel implementation, the algorithms should be parallelizable. A data re-allocation scheme is proposed and a look-ahead computation technique is employed to cope with the problems of the parallelism of the DAE algorithm. The problems are stated in Subsection 5.2, and the proposed solutions are explained in Subsection 5.4. In Subsections 5.3 and 5.4, a step-by-step description of the hardware implementation of the digital PAM-4 receiver is provided in detail by using both these two parallel architectures.

5.2 Challenges of deep-parallel implementation

The parallelizable algorithms should provide the possibility to make the processing modules work independently from each other. For example, the FIR filter structure is a more appropriate choice than the IIR filter structure for parallel implementation. This is because each output of the IIR filter depends on the calculated results at the same time in other parallel modules, which is a barrier

to independent processing module design. Although the output signal of FIR depends on the information provided by several parallel modules, it does not depend on the results of the same calculations performed in these modules. Hence, the FIR filter structure is possible for parallel processing.

In the digital PAM-4 system, the DAE algorithm is the main bottleneck for deeply parallel implementation. FIR-based DAE is chosen for investigation in this work. The operation of FIR-based DAE is described as

$$y(n) = \sum_{i=0}^{N-1} c_i \cdot x(n-i), 0 \leq i \leq N-1 \tag{5.1}$$

where $y(n)$ is the output signal. $x(n)$ is the input signal. N and c_i are the filter length and the filter coefficient of the i-th tap. The filter coefficients are updated adaptively by the LMS algorithm benefiting from its simplicity, computational efficiency, and good performance under a variety of operating conditions [135]. The adaptive updating scheme of LMS is expressed as

$$c(n+1) = c(n) + 2 \cdot \mu \cdot e(n) \cdot x^*(n) \tag{5.2}$$

$$e(n) = d(n) - y(n) \tag{5.3}$$

where μ is the updating step, which affects the updating speed and converging accuracy. It is worth noting that, the conjugate operation is added here to represent a more general case including complex-valued processing, but it can be removed for the PAM-4 system due to the real-valued processing. $e(n)$ is the error between the equalized output signal and the reference signal $d(n)$. From another perspective, the error signal indicates the distance vector from the current result toward the desired optimal point. In the error calculation procedure, the reference signal $d(n)$ is set as the training sequence initially and then switched to the recovered symbol stream when the error is smaller than a designed threshold. A training sequence (TS) is used to assist the pre-convergence of the algorithm at startup, and then a decision-directed LMS (DD-LMS) method is employed to track the remaining error. To implement the DD-LMS-DAE algorithm in parallel, two challenges need to be addressed.

5.2.1 Problem of output dependency resulting from the successive input

Based on Eq. (5.1), each output signal is calculated based on N successive input signals. It means that every output signal depends on the information of other parallel modules in direct parallel implementation. For example, assuming

that 4 lanes are paralleled and 3 taps are used for equalization, then $y(n)$ relies on not only the signal $x(n)$, but also the signals $x(n-1)$ and $x(n-2)$ from neighboring parallel modules. Consequently, in order to maintain the calculation continuity, the successive input signals should not be directly separated and fed to the independent parallel processing modules. Hence, the first challenge for parallel implementation of the DD-LMS-DAE is how to make the processing modules work independently for parallel processing without breaking the calculation continuity.

A common parallel technique for the FIR filter is the poly-phase decomposition [136, 137]. The key point of this technique is to decompose an N-taps FIR filter into a set of P sub-filters with N/P-taps for parallel processing, as shown in Figure 5.5. In contrast to this theoretical approach, we proposed a more practical and flexible solution for deep-parallelism to cope with this problem by using a data re-allocated scheme, which is explained in Section 5.4.

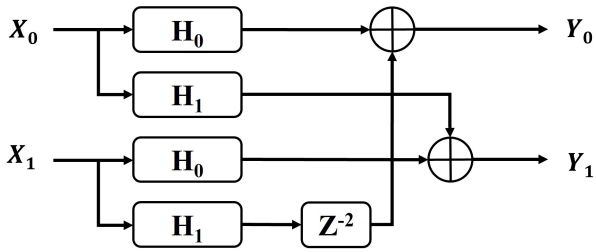

Figure 5.5: Poly-phase decomposition (e.g. $P = 2$).

5.2.2 Problem of iterative adaptive updating scheme

According to Eqs. (5.2) and (5.3), the filter coefficients are updated step by step. Each new set of coefficients at time $n+1$ relies on the information of signal $e(n)$ at time n. However, for direct parallel implementation, the updating interval between the new set of coefficients and the old ones could not maintain 1, since several parallel error signals $e(n)$ are generated at one moment and predicted several different distant vectors toward the optimal point simultaneously. A large updating interval makes the updating procedure less efficient. For example, if 4 parallel error signals $e(n)$ are generated at time n and only one could be used to predict the new set of coefficients at time $n+1$. Then, the updating interval is 4, and the valid information of the other 3 error signals is neglected, which could lead to a slower convergence. Therefore, the second challenge for parallel

implementation of the DD-LMS-DAE is how to update the coefficients efficiently in parallel. To deal with this problem, we proposed to introduce a look-ahead computation technique [138][139], which is explained in Section 5.4.

5.3 Classical straightforward parallel architecture

The classical parallel architecture is based on serial-FIR (S-FIR), which is a straightforward and hardware-efficient method for bottom-level hardware implementation. In this architecture, parallelism is only addressed on the top level.

5.3.1 Serial FIR (S-FIR)

A fundamental S-FIR architecture is shown in Figure 5.6 (a). It includes a shift register for caching N input signals, a ROM for storing all filter coefficients, a control logic block for synchronizing the shift register and ROM, a multiplier, and an adder for arithmetic calculation. The input signals are flowed into the S-FIR sequentially at a speed of one sample per N clock cycles since N multiplication and addition (M&A) operations are required for each convolution. With a controller, the data stream flows and caches in the shift register, and are calculated together with the corresponding filter coefficient simultaneously. The output signals are generated sequentially cycling one time at every N clock cycles.

5.3.2 Serial DD-LMS-DAE (S-DD-LMS-DAE)

In terms of the FIR-based DD-LMS-DAE, the coefficients of the FIR filter are not learned in advance and updated adaptively. A feedback loop is employed to calculate the inverse response of the channel step by step. As shown in Figure 5.6 (b), a DD-LMS-DAE includes an FIR filter for equalization, an adder (subtraction) for calculating the distance vector between the equalized output signal and the reference signal, a symbol recovery block for direct decision, a ROM for storing the training sequence, a control logic block for selecting the reference signal and synchronizing the calculation, a shift register for caching the input signals, a delay block for balancing the path latency, registers for saving the old filter coefficients, a conjunction block, a multiplier, a shifter, and an adder for LMS updating. The input signals are fed into the DAE at the speed of one sample per N clock cycles. The output signals of DAE are generated at one sample per N clock cycles.

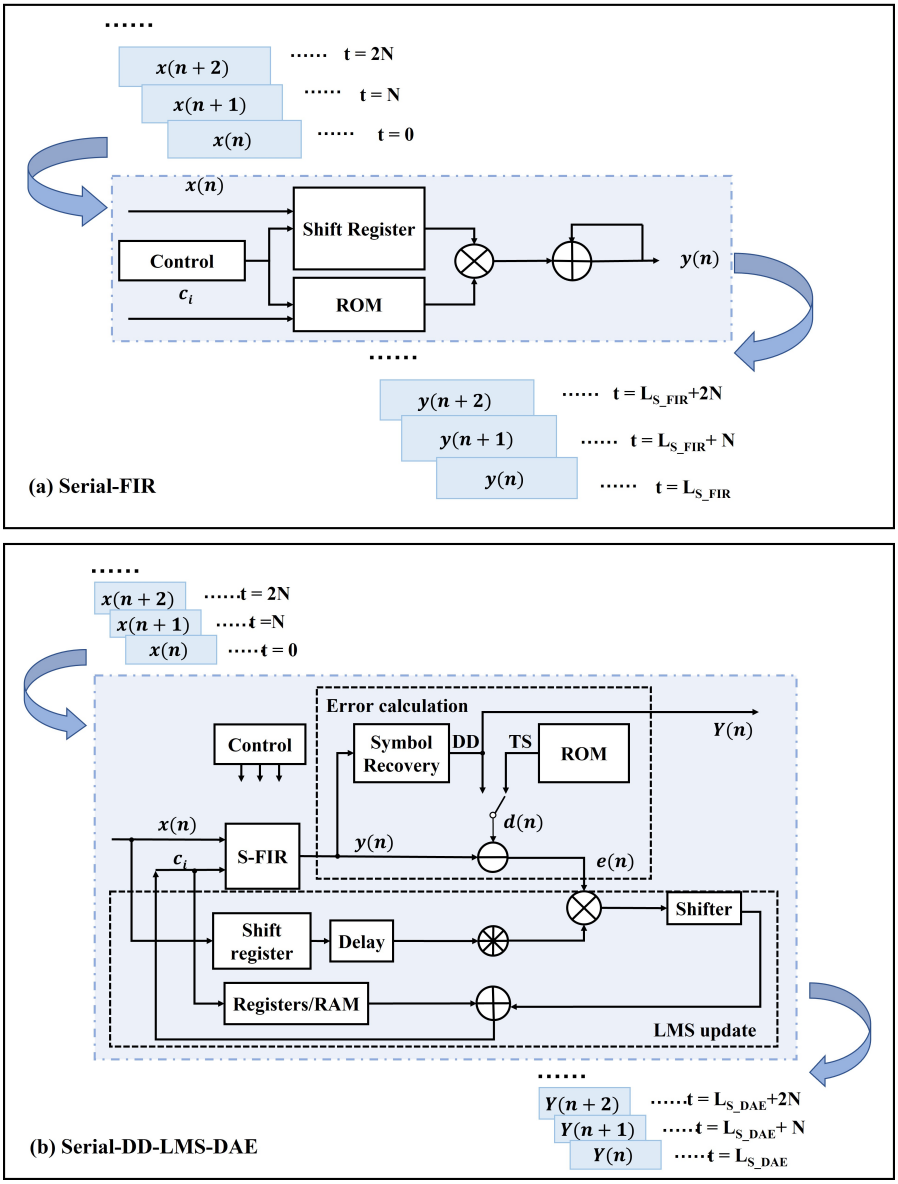

Figure 5.6: Hardware implementation: (a) Serial-FIR and (b) Serial-DD-LMS-DAE.

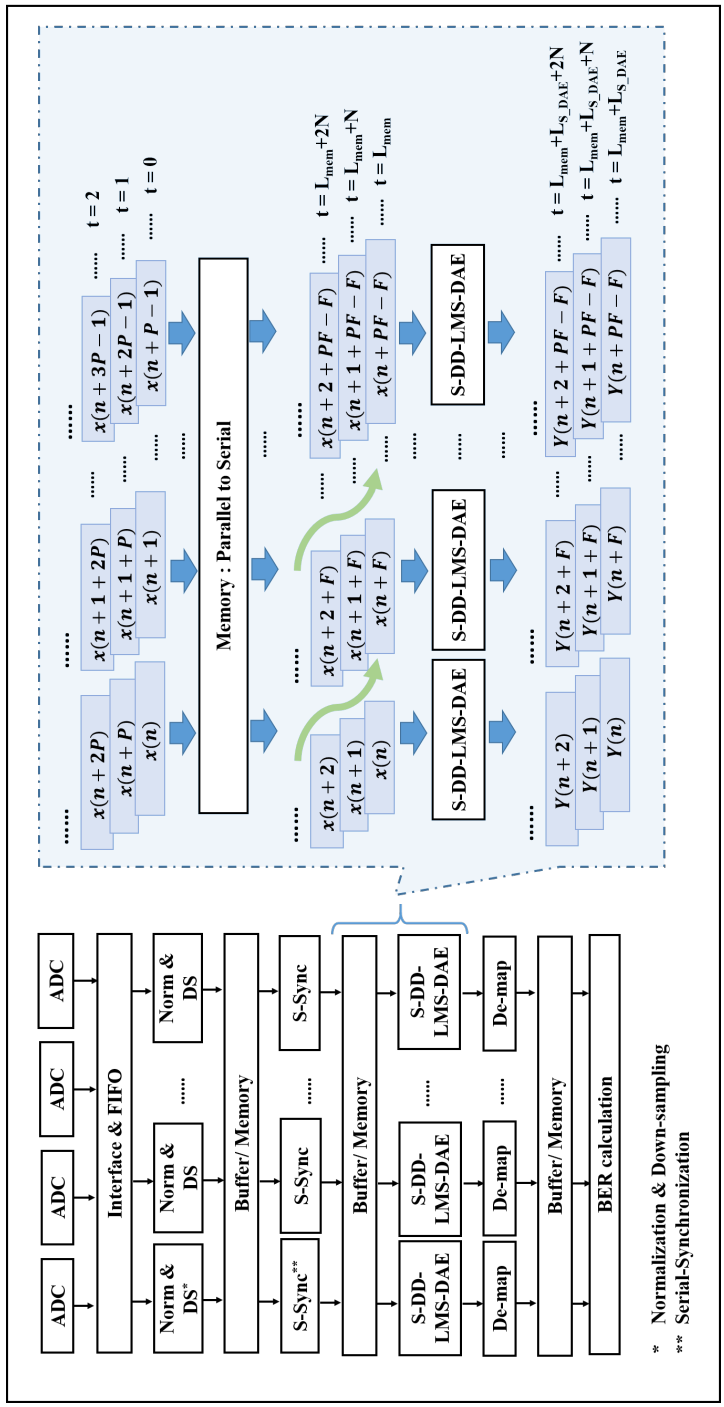

Figure 5.7: Parallel of algorithms only on the top level (Latency-costly parallel architecture).

5.3.3 Top-level parallel of algorithms

As mentioned in Section 5.1, in order to balance the transmission data rate and FPGA-based signal processing rate, the algorithms should be implemented in parallel. However, algorithms like DD-LMS-DAE require consecutive calculations due to the output dependency caused by the successive input samples. To maintain the calculation continuity, the incoming high-speed data stream should be written into a large memory for caching and then read out for processing frame by frame. Figure 5.7 shows the top-level parallel architecture and the data flow of parallelism with parallel S-DD-LMS-DAEs. As presented in Figure 5.7, memory is an important element to transform the parallel data streams into serial data streams (e.g. $x(n), x(n+1), x(n+2), ...$, and $x(n+F), x(n+1+F), x(n+2+F), ...$) to be processed by the processing modules (e.g. S-DD-LMS-DAE). Moreover, to cope with the discontinuities at the start of each individual S-DD-LMS-DAE, a data overlap between adjacent processing modules and a training sequence at the beginning of each frame is required.

Apart from the DD-LMS-DAE, frame synchronization based on autocorrelation also needs sequential calculation implemented with the FIR structure. Hence, the throughput of the frame synchronization is one sample every N clock cycles as well. Finally, the receiver can process data at a throughput of P samples every N clock cycles.

5.3.4 Latency analysis

Normally, a complex multiplication introduces a latency of 3 clock cycles while a real multiplication has a latency of 1 clock cycle on FPGA when the pipeline registers are irrespective. Other arithmetic operations like complex addition/real addition result in a latency of 1 clock cycle, while logic operation introduces zero latency. Each data registration occupies a latency of 1 clock cycle. For example, in DAE, the input signals flowing into a serial FIR are supposed to pass through a shift register (1 clock cycle), a multiplier (1 clock cycle), and an adder (1 clock cycle). N arithmetic calculations are required to generate one output signal. Thus, the latency of a real-valued S-FIR filter is at least $3N$ clock cycles. Similarly, a real-valued S-DD-LMS-DAE results in a latency of $3N+2$ clock cycles conservatively. The latency caused by the receiver DSP algorithms is analyzed and listed in Table 5.1.

The latency of the whole digital receiver is accumulated by all the algorithms

and memories, and is expressed as

$$L_{Total} = L_{Process} + L_{Cache} \tag{5.4}$$

where $L_{Process}$ is the latency of all the algorithms for signal processing. L_{Cache} represents the latency caused by caching. The significant latency contribution of this architecture comes from the caching for parallel-to-serial transformation. The incoming parallel data stream is stored in a memory and read out in a serial way. A latency of $\lceil (P-1) \times F/P \rceil$ is introduced for caching, where P is the number of parallel lanes and F is the frame length. Generally, the value of F is usually larger than 10 thousand symbols, leading to a large caching latency in comparison to the processing latency. Regardless of pipeline registering, the total DSP-introduced latency in this case is $(9 + 3S + 3N + \lceil \log_2(P) \rceil + 3 \times \lceil (P-1) \times F/P \rceil)$ clock cycles, where S is the length of the synchronization header. For example, F is 10000 symbols, S is 128 symbols, N is 4 taps and P is 8 lanes. The generated latency is 26658 clock cycles, which approximately equals 133.29 μs when FPGA operates at 200 MHz. It is composed of signal processing latency (2.04 μs) and caching latency (131.25 μs). So, the caching latency is the main contributor to the total latency.

Table 5.1: Latency of algorithms in the digital PAM-4 Receiver

$L_{Processing}$*							$L_{Caching}$
Cases \ Algorithms		Norm +DS	Synchroni-zation	DD-LMS -DAE	De-map	BER Calculation	Memories/ Re-allocation
A	*Real***	3	$3 \times S$	$3 \times N + 2$	1	$3 + \lceil \log_2 P \rceil$	$3 \times \lceil (P-1) \times F/P \rceil$
	*Complex****	5	$5 \times S$	$5 \times N + 2$	1	$3 + \lceil \log_2 P \rceil$	
B	*Real***	3	$1 + \lceil \log_2 S \rceil$	$4 + \lceil \log_2 N \rceil$	1	$3 + \lceil \log_2 P \rceil$	$\left\lceil \frac{P+S+2\times N-3}{P} \right\rceil + 1$
	*Complex****	5	$3 + \lceil \log_2 S \rceil$	$6 + \lceil \log_2 N \rceil$	1	$3 + \lceil \log_2 P \rceil$	
*without pipeline registers; **data for processing is real value; ***data for processing is complex value. S: Length of synchronization header; N: number of filter coefficients; P: number of parallel lanes; F: frame length.							

5.4 Proposed deeply parallel architecture

Different from the straightforward parallel architecture as discussed in Section 5.3, all the algorithms are implemented in parallel from top to bottom level in the latency-efficient parallel architecture. It is based on the parallel FIR (P-FIR) structure, which unfolds the convolution operation and calculates the M&As in parallel within one clock cycle using dedicated hardware rather than shared hardware. It reduces the latency and improves the throughput at the expense of more hardware resources. In this part, a deep-parallel (parallelism from top to down) receiver architecture based on a thorough P-FIR is discussed.

5.4.1 Parallel FIR (P-FIR)

In contrast to an S-FIR architecture, a thorough P-FIR architecture uses N multipliers and a $log_2(N)$ depth adder tree to conduct the N arithmetic calculations simultaneously, as shown in Figure 5.8 (a). In addition, pipeline registers are inserted to cache the intermediate results of each step for throughput optimization. Consequently, it can receive, process, and output the data stream at a throughput of one sample per clock cycle.

5.4.2 Parallel DD-LMS-DAE (P-DD-LMS-DAE)

The P-DD-LMS-DAE is developed based on the S-DD-LMS-DAE. As displayed in Figure 5.8 (b), P-FIR is used instead of S-FIR, and N times of hardware are employed for LMS updating. It is worth noting that the delay compensation should be re-designed to adjust the timing of the feedback loop in order to guarantee the calculation synchronization. Moreover, a fully-pipeline technique is employed, enabling the DAE to achieve the maximum throughput at one sample per clock cycle.

5.4.3 Deeply parallel algorithms

For a high-speed data stream, large memory is required to process the stream in the straightforward parallel architecture, since P samples are possible to arrive at the digital receiver simultaneously. However, going back and forth to the memory is expensive for FPGA design. To avoid visiting dedicated large memory, a deep-parallel architecture is developed based on the enhanced P-DD-LMS-DAE.

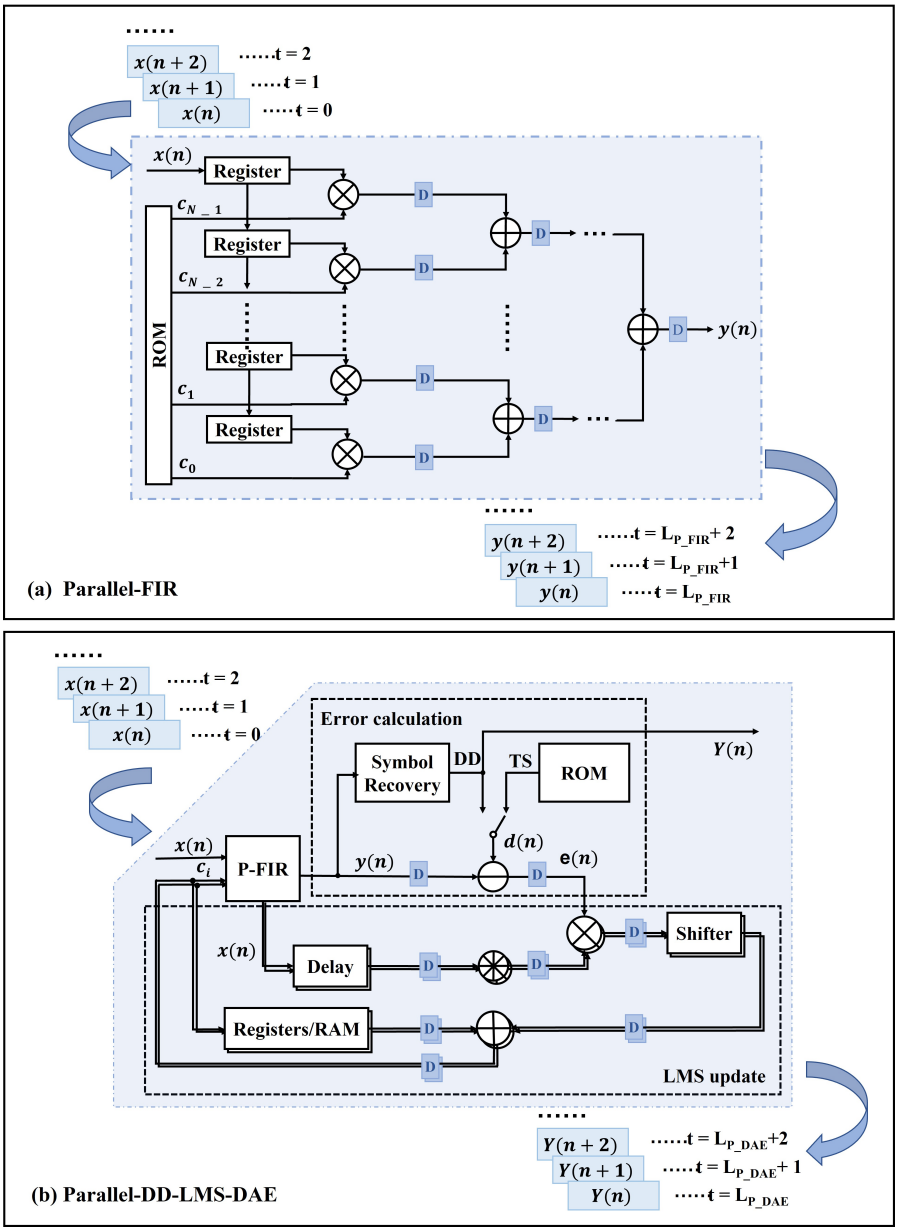

Figure 5.8: Hardware implementation: (a) Parallel-FIR and (b) Parallel-DD-LMS-DAE.

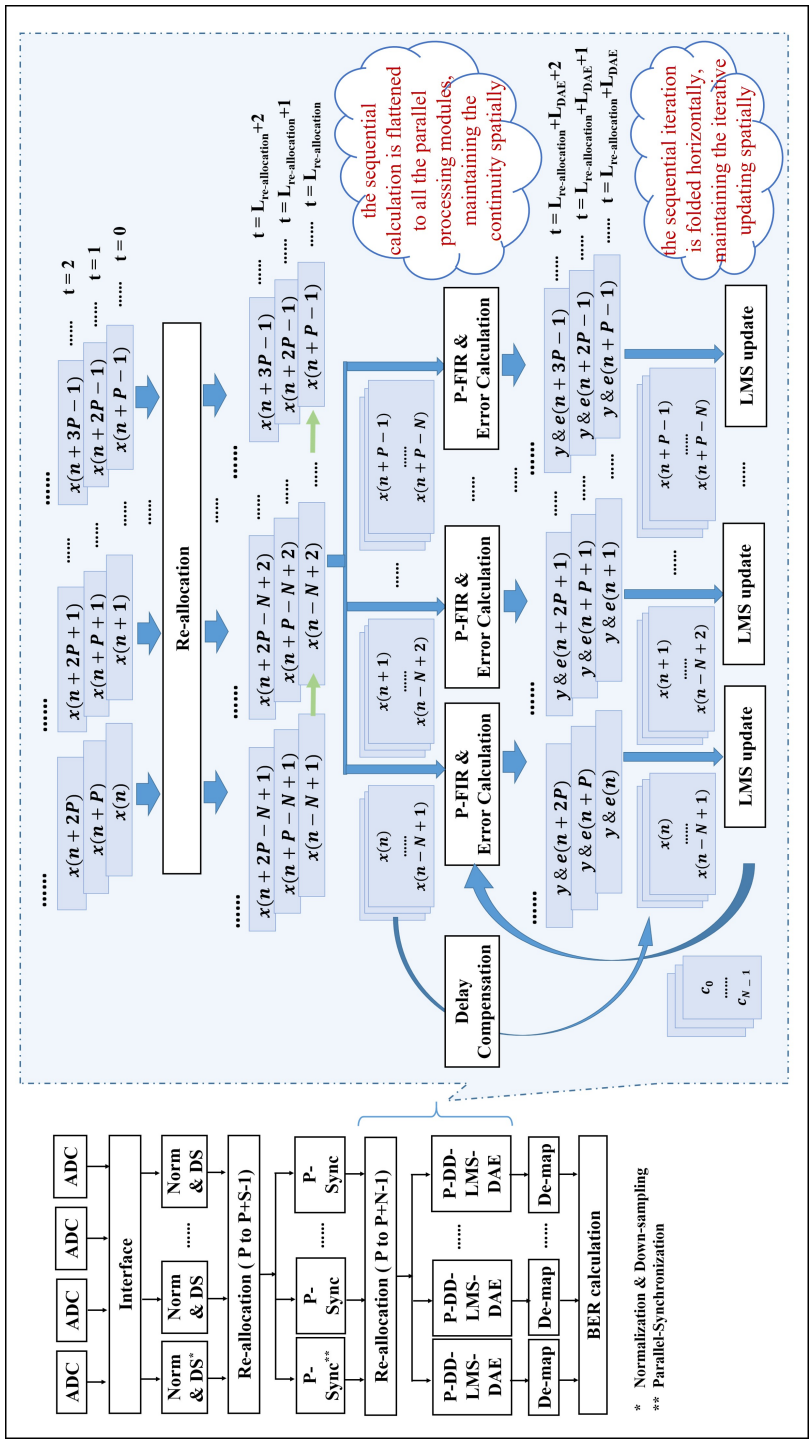

Figure 5.9: Deep-parallel of algorithms (Latency-efficient parallel architecture). The successive input samples and iterative updating scheme are both flattened to the spatial domain.

Data re-allocated scheme

As described in Section 5.2, two challenges are existing in the DD-LMS-DAE parallel implementation. In order to deal with the challenge of output dependency resulting from the successive input, a data re-allocation scheme is proposed. As shown in Figure 5.9, P parallel input signals are re-allocated as $P+N-1$ parallel input signals, and then broadcasted to P parallel P-DD-LMS-DAE modules at the same clock cycle. It is worth noting that the re-allocation implementation only needs several registers to eliminate the penalties from large memory access directly in the straightforward parallel architecture. In this way, all the parallel P-DD-LMS-DAE modules could get the required successive input signals for calculation at one clock cycle. Therefore, the dependency of parallel P-DD-LMS-DAE modules is de-correlated and the operations are conducted independently. The spatial continuity of the input signals is still preserved. In other words, the sequential calculation is flattened to all the parallel processing modules. Benefiting from the re-allocation scheme, there are no discontinuities between adjacent processing modules in this architecture since all the input signals are ultimately processed by all processing modules. Therefore, only a short zero-padding and one training sequence at the beginning are required for the data transmission.

Look-ahead computation approach

To cope with the iterative adaptive update challenge, a look-ahead computation technique is introduced. Intrinsically, the filter coefficients are updated at intervals since the P parallel error signals $e_k(n)$ are available at the same time. Whereas, all the P error signals $e_k(n)$ contain valid information for updating the filter coefficients. Each estimated error signal refers to a distinct distance vector towards the optimal point. Applying the look-ahead computation technique, all the information of P distance vectors is combined to generate the new set of filter coefficients. Notably, the update process maintained spatial iterative, which means the sequential iteration is folded horizontally. Assuming P is 3 lanes, the LMS updating procedure with look-ahead computation technique is expressed as

$$\begin{aligned} c_{k=1}(n) &= c_{k=0}(n) + 2 \cdot \mu \cdot e_{k=0}(n) \cdot {x_{k=0}}^*(n) \\ c_{k=2}(n) &= c_{k=1}(n) + 2 \cdot \mu \cdot e_{k=1}(n) \cdot {x_{k=1}}^*(n) \\ c_{k=3}(n) &= c_{k=2}(n) + 2 \cdot \mu \cdot e_{k=2}(n) \cdot {x_{k=2}}^*(n) \\ c(n+1) &= c_{k=3}(n), c(n) = c_{k=0}(n) \end{aligned} \tag{5.5}$$

Thanks to the look-ahead computation technique, the adaptive updating ef-

ficiency is enhanced, and the length of the training sequence is shortened by P times. Combining the look-ahead computation technique and parallel technique, Eqs. (5.1) - (5.3) are turned into

$$y_k(n) = \sum_{i=0}^{N-1} c(n-D)_i \cdot x_k(n-i), k = 0, 1, ..., P-1 \tag{5.6}$$

$$c(n+1)_i = c(n)_i + 2 \cdot \mu \cdot \sum_{k=0}^{P-1} e_k(n-D) \cdot {x_k}^*(n-D-i) \tag{5.7}$$

$$e_k(n) = d_k(n) - y_k(n) \tag{5.8}$$

where D is the feedback loop delay. According to Eqs. (5.6) - (5.8), a deep-parallel fully-pipeline DD-LMS-DAE is built, in which the successive input samples and iterative updating scheme are both flattened to the spatial domain. The data flow has been demonstrated in Figure 5.9 in detail. In addition, a deep-parallel fully-pipeline auto-correlation-based frame synchronization is also realized with the help of the data re-allocation scheme. All the algorithms at the receiver are implemented in parallel from the top level to the bottom level, enabling the data stream to flow smoothly through the processing modules with no need for caching. Therefore, the receiver can receive, process, and output data at a throughput of P samples per clock cycle.

5.4.4 Latency analysis

Generally, an adder tree with N input data has a latency of $\lceil \log_2(N) \rceil$ clock cycles. So the latency of a real-valued P-FIR is $1 + \lceil \log_2(N) \rceil$ clock cycles and a real-valued P-DD-LMS-DAE is $4 + \lceil \log_2(N) \rceil$ clock cycles. As for the latency of other algorithms, the details are listed in Table 5.1. Furthermore, the latency of fundamental calculating elements is doubled for fully-pipeline since every intermediate result is registered. Hence, a fully-pipeline real-valued P-DD-LMS-DAE occupies a latency of $8 + 2 \times \lceil \log_2(N) \rceil$ clock cycles.

Compared with the straightforward parallel architecture, the main latency caused by caching in large memories is removed. In this architecture, only several registers are used to re-allocate P parallel input signals to $P + N - 1$ parallel input signals for deeply parallel processing in the DD-LMS-DAE. Similarly, P parallel input signals are also re-allocated to $P + S - 1$ parallel input signals for frame synchronization. To optimize the hardware utilization efficiency, only one data re-allocation block is employed for the whole digital receiver. $P + N + S - 2$

parallel input signals are simultaneously generated and shared by both the frame synchronization and DD-LMS-DAE. Consequently, the caching latency of this architecture is $\lceil (P+S+2\times N-3)/P \rceil + 1$ clock cycles in total. The total latency of the real-valued digital receiver is summation of the re-allocation block and algorithms except for frame synchronization, $12+\lceil \log 2(N) \rceil + \lceil \log 2(P) \rceil + \lceil (P+S+2\times N-3)/P \rceil$ clock cycles. Here, the latency caused by the pipeline registers is ignored.

5.5 Latency reduction

5.5.1 Latency comparison of the two parallel architectures

A comparison of the calculated latency between the straightforward parallel architecture (case A) and the deeply parallel architecture (case B) is shown in Figure 5.10. The charts are made based on the assumption of zero pipeline registers, 10000 symbols frame length (F), 128 symbols synchronization header length (S), 8 parallel lanes (P) when N grows, and 4 taps (N) when P increases. In case A, caching latency is the dominant proportion and grows obviously with P increment, while processing latency rises slightly with the increment of both N and P. In case B, caching latency grows with the increment of N, but decreases as P increases. As for the processing latency, it has a tiny increment with both N and P as well. As shown in Figure 5.10, the total latency of case B is much smaller than case A. Under the condition that P is 8 lanes and N is 4 taps, the total latency of case B is 35 clock cycles, which is just 0.13% of 26658 clock cycles for case A. Considering an FPGA operation frequency of 200 MHz, the total DSP-introduced latency of case A exceeds 75 μs (15000 clock cycles). Whereas, the latency of case B is only around 0.2 μs (40 clock cycles) which is much more latency-efficient. Therefore, the deeply parallel architecture reduces the latency significantly, which better meets the requirements of latency-sensitive user cases.

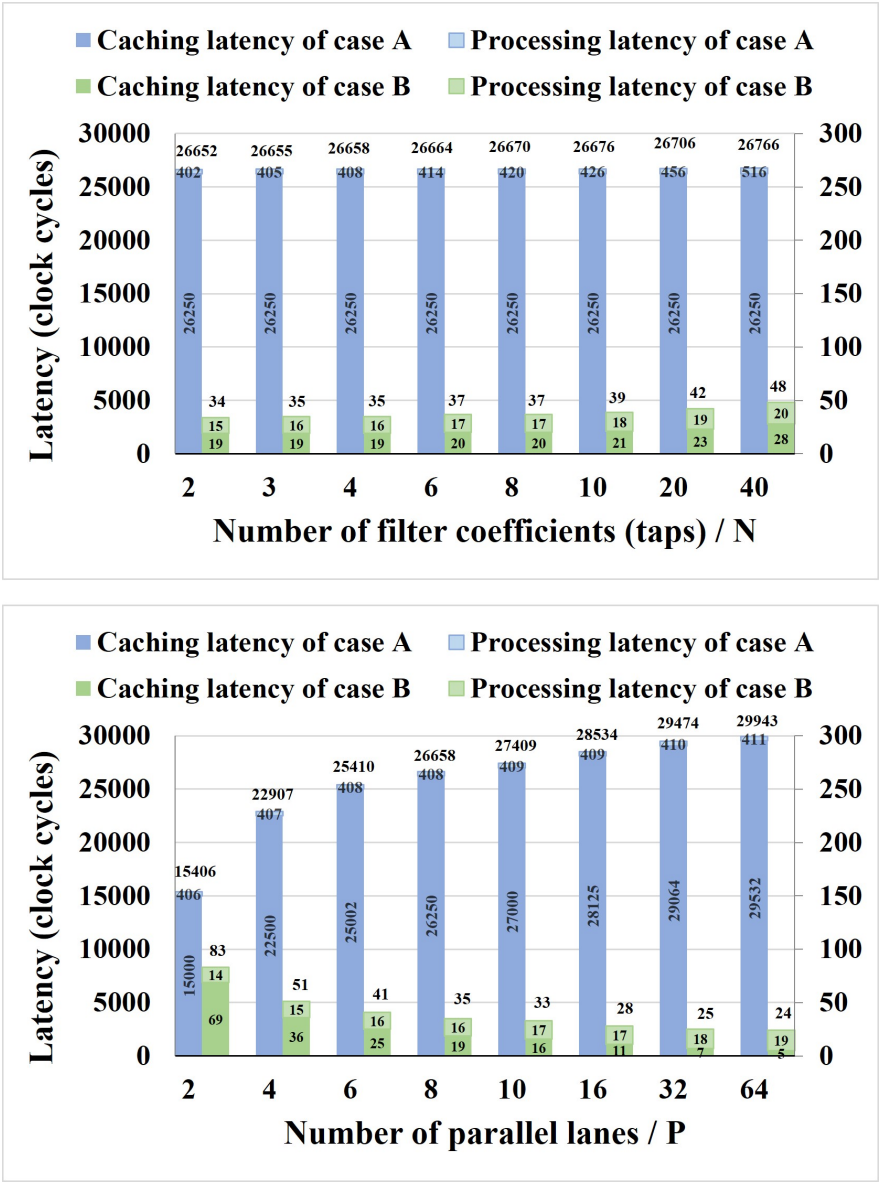

Figure 5.10: Calculated latency comparison between latency-costly parallel architecture (case A) and latency-efficient parallel architecture (case B).

5.5.2 Impact of latency reduction

We proposed to use a deep-parallel scheme in our design to reduce the real-time system latency. The parallel implementation is necessary when the required transmission data rate is much higher than the operating frequency of FPGA. Straightforward parallel architecture is latency-costly (as shown in case A of Figure 5.10), while deeply parallel architecture is much more latency-efficient (as shown in case B of Figure 5.10).

System cost is another consideration factor when designing a real-time system. The main difference between the straightforward parallel implementation and the deeply parallel implementation is the bottom-level realization. Serial-FIR is used for straightforward parallel, while parallel-FIR is used for deeply parallel. Parallel-FIR needs more hardware resources than serial-FIR. For example, N times of multipliers and $log_2(N)$ times of adders are needed for parallel-FIR in comparison to the serial-FIR. However, deeply parallel architecture does not need large memories for data caching. Moreover, as the data throughput of serial-DD-LMS-DAE is one sample per N clock cycles, N paralleling serial-DD-LMS-DAEs are required to generate a data throughput of one sample per clock cycle. Whereas, the data throughput of a parallel-DD-LMS-DAE is one sample per clock cycle. Hence, N serial-FIRs (N multipliers and N adders) are needed while one parallel-FIR (N multipliers and $log_2(N)$ adders) is required to get the same data throughput. Therefore, the deeply parallel architecture reduces the latency and does not increase the hardware resource utilization when getting the same data throughput.

As for the BER performance of the real-time transmission system, it will not be affected by the parallel architecture, it is related to the resolution of the data converters and the FPGA internal signal processing precision.

5.6 Experimental setup

The developed deeply parallel fully-pipeline FPGA-based PAM-4 receiver is investigated in an optical fiber link. The experimental setup is shown in Figure 5.11. At the transmitter side, a digital baseband PAM-4 signal with synchronization header and training sequence is generated in the FPGA and stored as a text file. The length of the repeating data stream is 80000 symbols, including 128 symbols for synchronization and 8000 symbols for start-up training. Then, the digital baseband signal is sent to an AWG to generate a 1.25-GBaud/s analog PAM-4 signal, yielding a bit rate of 2.5 Gbit/s. After that, the output signal from AWG is amplified by an electrical amplifier and combined with the bias current (DC) via a bias-T, which is used to drive an off-the-shelf C-band distributed feedback laser diode (DFB-LD). The optimal values of DC and input voltage are 50 mA and 3.5 V, respectively. After the DFB-LD, the modulated optical signal is transmitted through a span of single-mode fiber (SMF). In comparison to the performance of a short (1m-2m) SMF link, there is negligible or minimal impact on the performance of an indoor PtP IR OWC link, which has been verified in [105]. Therefore, in this experiment, we investigate the link performance using a short SMF link (which would have a similar performance as the indoor PtP IR OWC link). On the receiver side, an off-the-shelf optical-to-electrical converter, including a PIN-PD and a TIA, is used for signal detection. A VOA is placed at the front of the PD to adjust the received optical power. Then, the detected electrical analog signal arrived at our developed FPGA-based real-time receiver for signal processing. On the FPGA evaluation board (Xilinx VC707 evaluation board featured with a Virtex-7 XC7VX485T-2FFG1761 device), a commercial FPGA Mezzanine Card (FMC) carrying a 10-bit quad ADC (E2V-EV10AQ190) [140] is used for analog to digital signal conversion. The high-speed data stream is sampled by four interleaved 1.25-GSa/s ADC cores running at the aggregate maximum sampling rate of 5 GSa/s. These four interleaved digital signals are transformed into 32 parallel signals with the help of the high-speed interface. After down-sampling by 4 times, the digital signals are parallel processed with 8 lanes at a clock frequency of 156.25 MHz on FPGA. The ADC is operating at a clock frequency of 2.5 GHz provided by the FMC on-board voltage-controlled oscillator (VCO). The FMC clock architecture is designed to provide a sampling clock with minimum jitter and phased noise. The FPGA clock is provided by the FMC internal clock. The DSP-introduced latency and BER performances can be measured with ChipScope from Xilinx, which is the virtual probe for internal signals debugging on FPGA.

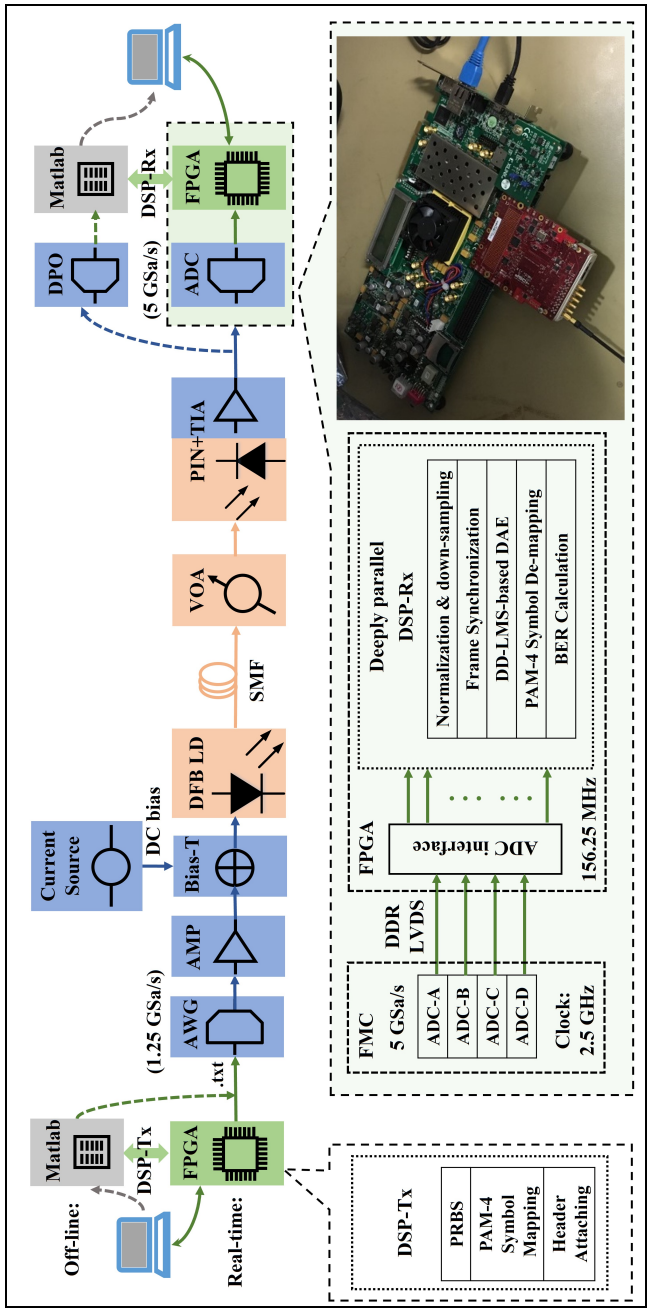

Figure 5.11: Experimental setup of the optical transmission system. FPGA: field programmable gate array; AWG: arbitrary waveform generator; AMP: amplifier; DFB LD: distributed feedback laser diode; DC: direct current; SMF: single mode fiber; VOA: variable optical attenuator; TIA: trans-impedance amplifier; ADC: analog-to-digital converter; DPO: digital phosphor oscilloscope; FMC: FPGA Mezzanine Card FMC; DDR: double data rate; LVDS: low-voltage differential signaling.

5.7 Experimental results and discussions

Before the real-time BER measurement, offline experiments are carried out for performance estimation and comparison. As displayed in Figure 5.11, the experimental setup is a little different from the real-time version: at the transmitter, the digital PAM-4 signal is generated by Matlab and then sent to the AWG for the analog signal generation; at the receiver, the detected analog signal is captured by a DPO and processed with Matlab. According to the offline processing, a 4-tap symbol-space (T-space) DAE with the main cursor positioned at 1 is adequate to compensate for the distortion in the transmission link, as shown in Figure 5.12 of the red curve. The calculated BER values across the received optical power range from -8 dBm to -3 dBm by 1 dBm step.

Then the real-time experiment is demonstrated based on the DAE parameters specified in the offline experiment. The real-time BER performance as a function of received optical power is presented in Figure 5.12. Considering the 7% FEC limit of 1×10^{-3}, the receiver sensitivity of the real-time receiver with equalization (blue curve in Figure 5.12) is about –5.5 dBm, which is consistent with the value of the offline experiment. The case of the real-time receiver without equalization is also shown in Figure 5.12, where the error floor occurs. Therefore, the feasibility of the FPGA-based PAM-4 receiver with equalization is verified.

In the real-time experiment, the DSP-introduced latency is 0.3904 μs (61 clock cycles) in total, in which 0.3072 μs (35 clock cycles) is consistent with the former calculation in Section 5.4. The additional 0.1088 μs (17 clock cycles) is caused by the pipeline registering and 0.0576 μs (9 clock cycles) is introduced by signal reset and control. The training latency is not included in the total DSP-introduced latency above. For both offline and real-time experiments, a training sequence with 8000 symbols and an LMS updating step of 0.004 are applied to help the DAE tap weights converge to the targeted point. Benefiting from parallel implementation, the latency for training is shortened by the number of parallel lanes, leading to a latency of 6.4 μs (1000 clock cycles).

In this work, the used FPGA is the Xilinx VC707 evaluation board featured with a Virtex-7 XC7VX485T-2FFG1761 device, and the ADC we used is FMC126 with E2V-EV10AQ190 chip. The ADC sampling resolution is 10-bit and the FPGA internal signal processing precision is 16-bit. The resource utilization of the implemented PAM-4 receiver is listed in Table 5.2. Figure 5.13 shows the power consumption (according to the implemented netlist) of the implemented PAM-4 receiver, which consumes a total power of 3.308 W. It is worth mentioning that the proposed deep-parallel method is potentially effective for

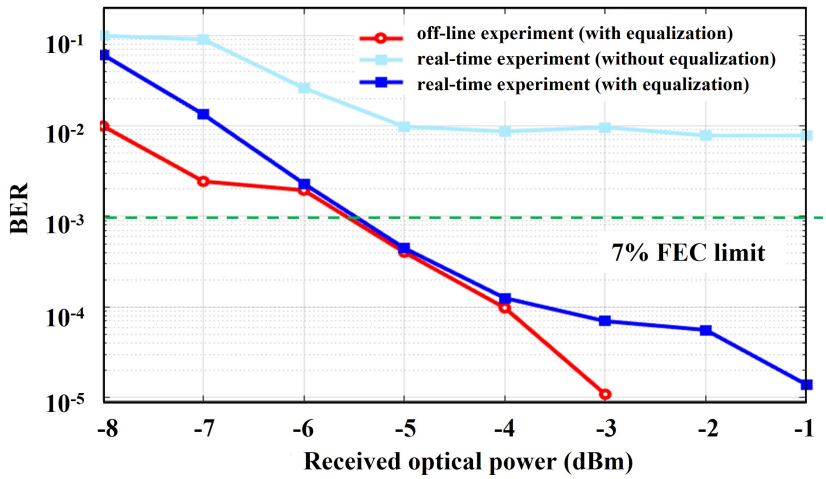

Figure 5.12: BER performance as a function of received optical power for 2.5-Gbit/s PAM-4 signal transmission.

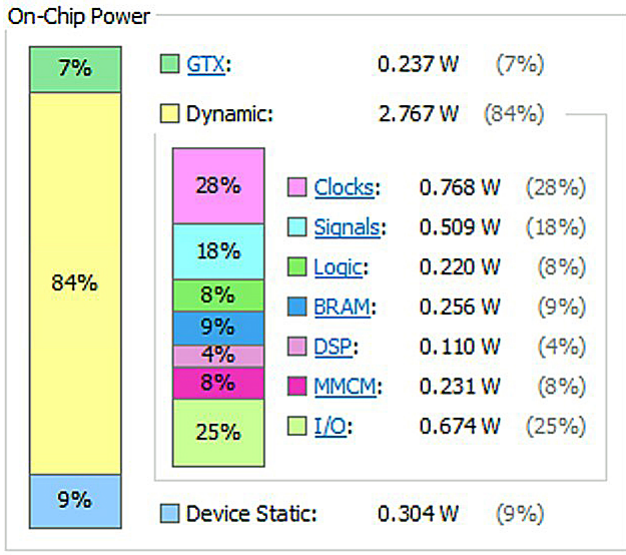

Figure 5.13: Power consumption of the implemented PAM-4 receiver.

100 Gbit/s or higher transmission. In our demonstration, the data rate is limited by the employed hardware device (e.g. the available ADC has a maximum sample rate of 5 GSa/s), not the proposed method. When the transmission data

rate increases, the number of parallel lanes and hardware utilization increase. For 100 Gbit/s or higher data rates, ASIC with abundant hardware resources can be used for our proposed deep-parallel method to reduce the latency. For ASIC implementation, the number of parallel lanes can be reduced significantly since the operating frequency of ASIC is much higher than FPGA. Generally, the operating frequency of FPGA is around 200 MHz [131, 132] (the specific speed depends on the critical-path delay of the design), while about 700 MHz is attainable with ASIC implementation [141]. Moreover, for FPGA implementation, structured logic blocks are utilized, leading to the waste of some unnecessary areas in layout design. ASIC implementation is more flexible in the optimization of the layout design. This leads to reduced costs due to the reduced chip area required. Thus, the proposed method is effective to be extended to ASIC implementation for >100 Gbit/s direct detection or coherent detection systems with reduced latency and cost.

Table 5.2: Resource utilization of the implemented PAM-4 receiver

Resource	Slice LUTs (303600)	Slice Registers (607200)	Slice (75900)	LUT as Logic (303600)	LUT Flip Flop Pairs (303600)	Block RAM Tile (1030)	DSPs (2800)
ADC interface	2.62%	1.47%	4.26%	2.59%	1.24%	3.93%	0%
DSP-RX	8.8%	15.94%	26.88%	8.47%	7.96%	17.52%	38.86%
DAE	0.72%	1.72%	2.84%	0.72%	0.63%	0.05%	2.28%

5.8 Conclusion

DSP techniques have been proven efficient for the low-cost high-capacity indoor OWC systems, but the experimental demonstrations are mainly based on the offline DSP which does not consider the limitation of hardware implementation. In this chapter, the DSP algorithms are implemented on the FPGA platform. Whereas, the speed limit of FPGA forces the parallel implementation of the FPGA-based DSP algorithms. However, the classical parallel implementation architecture introduces severe latency, which hinders the latency-critical applications. Hence, we conduct a detailed analysis of the latency of hardware-realized DSP algorithms and further propose to use a deeply parallel architecture to reduce the total DSP-introduced latency. The step-by-step hardware implementation of the two parallel implementation architectures is described, followed by a detailed latency analysis. DAE is challenging the deeply parallel implementation due to its successive input samples and the iterative adaptive update scheme. To enable the deeply parallel implementation, a novel data reallocation scheme is proposed to cope with the issue of the output dependency on the successive input samples, and a look-ahead computation approach is employed to improve the adaptive update efficiency of the DAE. In addition to the latency reduction, the deeply parallel architecture also releases the utilization of large memories and does not utilize more hardware resource in comparison to the classical straightforward parallel architecture when getting the same data throughput. An FPGA-based real-time PAM-4 receiver with deep-parallel fully-pipeline DSP implementation is demonstrated in an experimental fiber link with a 2.5-Gbit/s data rate for the performance evaluation. It reveals that the BER performance has little deterioration compared with the offline processing. The real-time PAM-4 receiver could be flexibly reconfigured for various scenarios with low-latency requirements. The proposed latency-efficient parallel approach is also feasible to be extended to the implementation of real-time low-latency high-speed communication systems with a data rate of up to 100 Gbit/s or more potentially.

6

Conclusions and Future outlook

"The only limit to our realization of tomorrow will be our doubts of today."

— Franklin D. Roosevelt —

6.1 Conclusions

The increase of connected wireless devices and the popularization of emerging bandwidth-hungry latency-sensitive applications are challenging traditional radio-based indoor wireless networks. Spectrum-efficient modulation schemes and multiplexing techniques have been adopted to improve the transmission capacity, but the limited spectrum is getting exhausted inevitably due to the increasing growth of wireless data traffic. The emerging OWC technology employing license-free optical spectrum is becoming a promising supplement to the traditional radio-based technologies to tackle the exhaust spectrum problem. Future indoor networks will be fiber-wireless converged picocell-based with heterogeneous wireless access technologies including but not limited to the traditional radio and the emerging OWC technology. It is expected to realize seamless wireless coverage with the capability to meet the requirements of high connection density, high capacity, low power consumption, low cost, and low latency.

OWC mainly contains two categories: VLC and IR OWC. Different from the broadcast-based VLC, the IR beam-steered OWC using high-directive narrow beams is more power-efficient, more suitable to establish pico-cells, and provides intrinsically high capacity per beam. The narrow beams can be steered only to the intended destination and serve the individual user device when needed, providing better privacy protection and avoiding congestion issues. IR beam-steering can be realized by various techniques. A.M.J.Koonen et al. have proposed a cost- and power-efficient wavelength-controlled 2D IR beam-steered OWC scheme using a pair of crossed gratings and a high port-count AWGR. The beam-steering is realized by tuning the wavelength of each beam remotely. Meanwhile, the low-complexity high-efficiency DSP technique has benefited the OWC systems since it significantly improves the spectrum efficiency and signal quality, boosting the system capacity in a cost-efficient manner.

This thesis concentrates on the low-complexity DSP techniques and the optimization of the 2D IR beam-steered OWC systems by using the DSP techniques. Three challenges resulting from the limitation of the AWGR-based beam-steering spatial resolution, sample rate limitation of data converters, and speed limitation of FPGA are investigated, considering the above requirements of the future indoor wireless network. Besides the offline DSP, the real-time DSP based on FPGA implementation is also explored. All the proposed solutions are experimentally investigated.

In Chapter 2, the key DSP techniques investigated in this thesis are explained in detail. The popular digital high-order modulation formats including PAM,

QAM, CAP, SCM, OFDM, and DMT have been described to give a general overview of the digital high-order modulation techniques. Considering the dominant requirements of power-efficient and cost-efficient for the indoor IR OWC applications, the IM-DD scheme, and PAM-4 format are chosen for further investigation in this thesis. Digital equalization techniques are necessary for the high-speed PAM-4 systems which are sensitive to the ISI resulting from the reduced symbol duration for higher required data rate. Thus an overview of a variety of digital equalization techniques is given finally.

Chapter 3 concentrates on the trade-off problem of the system spatial resolution and OWC channel capacity per beam for the AWGR-based 2D IR beam-steered OWC system. Large spatial coverage is required regarding a realistic OWC application. However, the OWC capacity per beam is compromised by the high spatial resolution AWGR-based beam-steering. A digital filter-aided crosstalk mitigation scheme that takes advantage of the digital Nyquist pulse shaping technique is proposed to cope with this problem. By shaping the transmitted signal for narrow spectral occupancy, the inter-channel crosstalk resulting from the imperfect AWGR filtering can be reduced, which enables using a denser AWGR grid. Also, a doubled channel capacity is attainable with the improved spectrum-efficient signal. In addition, the spectral-efficient signal reduces the bandwidth requirement of the AWGR, which allows for a low-complexity AWGR design. The proposed method is not sensitive to the wavelength misalignment between AWGRs and lasers, which relaxes the design of high wavelength-stability lasers. The proposed method has been experimentally investigated over a 6-GHz bandwidth-limited AWGR-based 1.1-m free-space link with the 20-Gbit/s data rate OWC capacity using PAM-4 format. The experimental results show the feasibility and effectiveness of the proposed method. As the cost of eliminating the trade-off between OWC channel capacity and system spatial resolution, the introduced Nyquist pulse-shaping filter and matched filter lead to additional complexity for the DSP implementation. However, the combined filter length of our employed pulse-shaping filter and matched filter is only 21, resulting in a rather small additional implementation complexity. Whereas, the doubled sample rate requirement results from the employment of the digital Nyquist filtering increases non-negligible complexity, which is discussed in Chapter 4.

In Chapter 4, we have proposed to use a non-integer oversampling approach to reduce the hardware implementation complexity and power consumption for our DSP-aided AWGR-based 2D IR beam-steered OWC system with high spatial resolution. By minimizing the oversampling of Nyquist signaling with a ratio-

nal factor, the lower sample rate required relaxes the requirement of complex costly high-speed data converters, thereby reducing the hardware cost and the power consumption. Also, the computational effort of the digital Nyquist signal implementation is reduced. We have experimentally investigated the impact of the non-integer oversampling approach in the 12.5-GHz channel-spaced 6-GHz bandwidth-limited AWGR-based 1.1-m OWC link with a capacity of 20-Gbit/s data rate. The oversampling rate is minimized to a $1.1\times$ symbol rate (when using SRRC filter with $\beta = 0.1$) with an 11-GSa/s DAC sample rate. Compared to the 2-fold oversampling Nyquist PAM-4 system, the DAC sample rate requirement is relaxed by 55%, with a cost of a 2.3-dB power penalty at the 7% FEC limit of 1×10^{-3}.

In an effort for practical realization, Chapter 5 focuses on the real-time DSP based on the FPGA implementation. The speed limitation of FPGA forces the parallel implementation of the FPGA-based DSP algorithms. However, the classical parallel implementation architecture introduces severe latency, which hinders the latency-critical applications. Hence, we conduct a detailed analysis of the latency of hardware-realized DSP algorithms and further propose to use a deeply parallel architecture to reduce the total DSP-introduced latency. The step-by-step hardware implementation of the two parallel implementation architectures is described, followed by a detailed latency analysis. Digital adaptive equalizer (DAE) is challenging the deeply parallel implementation due to its successive input samples and the iterative adaptive update scheme. To enable the deeply parallel implementation, a novel data re-allocation scheme is proposed to cope with the issue of the output dependency on the successive input samples, and a look-ahead computation approach is employed to improve the adaptive update efficiency of the DAE. In addition to the latency reduction, the deeply parallel architecture also releases the utilization of large memories and does not utilize more hardware resource in comparison to the classical straightforward parallel architecture when getting the same data throughput. An FPGA-based real-time PAM-4 receiver with deep-parallel fully-pipeline DSP implementation is demonstrated in an experimental fiber link with a 2.5-Gbit/s data rate for the performance evaluation. It reveals that the BER performance has little deterioration compared with the offline processing. The real-time PAM-4 receiver could be flexibly reconfigured for various scenarios with low-latency requirements. The proposed latency-efficient parallel approach is also feasible to be extended to the implementation of real-time low-latency high-speed communication systems with a data rate of up to 100 Gbit/s or more potentially.

6.2 Future outlook

In the future, the following topics could be explored:

- Higher-order PAM

  PAM-4 modulation is efficient for doubling the capacity of the cost- and power-efficient indoor OWC systems, but the OWC capacity has an upper bound when using the relatively low-cost electrical and optical components due to the relatively low spectral efficiency (2 bits/symbol) of the PAM-4 system. To achieve a higher data rate, higher-order PAM such as PAM-6 and PAM-8 can be used. However, it comes at a cost of higher required SNR to distinguish the larger number of amplitude levels with smaller spaced constellation points. And higher-order PAM requires better system linearity and DAC/ADC performance. Therefore, the trade-off between the modulation order and resultant performance can be explored.

- Low-complexity non-linear equalizer

  As the data rate further scales up, the non-linear impairments caused by the non-linearity of electrical and optical components such as MZM driver and square-law detection of the photo-diode are non-negligible. They can be compensated by the advanced equalizer such as Volterra non-linear equalizer (VNLE). However, the computational complexity of VNLE grows exponentially with the equalizer order for a fully-connected VNLE, which is not practical for the hardware implementation. Therefore, the complexity reduction of VNLE can be explored concerning the requirement of a specific channel.

- Low-complexity faster-than-Nyquist signaling

  Faster-than-Nyquist (FTN) signaling has attracted lots of attention due to its enhanced spectral efficiency. Different from Nyquist signaling which emphasizes the orthogonality to avoid ISI, FTN signaling allows ISI with non-orthogonal signals, squeezing more data into the same bandwidth. FTN systems can be regarded as a subset of partial response systems [142]. The main difference is the introduction of a time compression factor τ. By introducing the time compression factor into Eq. (2.2), the transmitted signal is expressed as

$$x_{FTN}(t) = \sum_i b_i \cdot p(t - i \cdot \tau \cdot T_P) \tag{6.1}$$

When τ is smaller than 1, the pulse duration is reduced equivalently which represents a higher data rate ($1/(\tau \cdot T_P) > R_S$). For example, 22% data rate improvement is attainable when $\tau = 0.82$, and the BER performance will not increase until τ falls below 0.802 for binary signaling over AWGN channels [143]. However, the introduced severe ISI of the FTN system requires complicated data recovery techniques which increase the implementation complexity of both the transmitter and receiver. Therefore, efficient solutions with low complexity for the FTN system can be explored.

- Multi-dimensional multiplexing

  The digital Nyquist PAM-4 system can be further extended to the CAP system and Nyquist SCM system in conjunction with spatial multiplexing and frequency band multiplexing for larger OWC capacity.

- ASIC implementation

  The FPGA-based DSP algorithms and the extended data converters can be realized on-chip as ASIC for cost-efficient, power-efficient, and compact products. On the one hand, the integration of data converters and DSP algorithms will relax the high-speed interface design. On the other hand, ASIC implementation can achieve higher operating frequency, smaller area utilization and power consumption than the FPGA implementation of the DSP algorithms. Generally, the operating frequency of FPGA is around 200 MHz [131, 132] (the specific speed depends on the critical-path delay of the design), while about 700 MHz is attainable with ASIC implementation [141]. So the number of parallel lanes can be reduced significantly to achieve the same targeted data rate in the ASIC implementation. The reduction of parallel lanes results in less resource utilization, thus smaller area and power consumption. Moreover, the chip area and power consumption of ASIC implementation is intrinsically smaller than the FPGA implementation. Take the comparison between the 90-nm CMOS FPGA and the 90-nm CMOS standard-cell ASIC implementation as an example [144], the ratio of the critical-path delay (which limits the operating frequency), is roughly three to four times smaller from FPGA to ASIC, which means a three to four higher frequency than FPGA is attainable for ASIC implementation. The ratio of the chip area is on average 35:1 from FPGA to ASIC when the circuits are implemented using only the logic resources. When the ”hard” blocks such as multiplier/accumulators, DSP blocks, and block memories are utilized, the area gap ratio is reduced and can be be-

low five. The gap ratio of dynamic power consumption between the FPGA and an equivalent ASIC implementation is approximately 14:1 on average. The utilization of the ”hard” blocks also enables a substantial reduction in the gap of power consumption between the FPGA and ASIC implementation. To conclude, higher operating frequency, smaller chip area, and lower power consumption can be expected in regard to ASIC implementation of DSP algorithms.

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Biography

Liuyan Chen was born on November 23, 1991, in Guangdong, China. She received her B.Eng. Degree in Microelectronics (2013) and her M. Eng. Degree in Microelectronics and Solid-state Electronics (2016) from Sun Yat-Sen University, Guangzhou, China. During her bachelor's and master's studies, she has four-year research experience in Analog Integrated Circuit (IC) design including low-power smart temperature sensors, fully integrated power management ICs, and micro Organic Light Emitting Diode (OLED) drivers. After her graduate school education, she worked in All Winner Technology, Zhuhai, China as an analog IC designer (2016). Since November 2016, she was a Ph.D. candidate in the Electro-Optical Communication (ECO) group at the Eindhoven University of Technology (TU/e), Eindhoven, the Netherlands, granted by the Guangzhou Elite Project. Her current research topics include digital signal processing, optical wireless communications, and Field-Programmable Gate Array (FPGA) implementation.

List of Publications

Within the scope of this thesis:

1. Chen, L., Oh, C.W., Lee, J., Zhang, X., Cao, Z., and Koonen, A.M.J., 2022. Digital-filter-aided crosstalk-mitigation for high spatial resolution AWGR-based 2D IR beam-steered indoor optical wireless communication system. Optics Express, Mar. 2022.

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3. Chen, L., Li, C., Oh, C.W. and Koonen, A.M.J., 2021. A low-latency real-time PAM-4 receiver enabled by deep-parallel technique. Optics Communications, volume 508, p.127836.

Out of the scope of this thesis:

1. Sun, K., Chen, L., Guo, J., Teng, D. and Liu, L., 2016. A LTPS-TFT pixel circuit for active matrix organic light emitting diode based on improved current mirror. Displays, 44, pp.1-4.

2. Chen, L., Cheng, Q., Guo, J. and Chen, M., 2015, September. High-PSR CMOS LDO with embedded ripple feedforward and energy-efficient bandwidth extension. In 2015 28th IEEE International System-on-Chip Conference (SOCC) (pp. 384-389). IEEE.

3. Cheng, Q., Chen, L.. and Guo, J., 2014, November. A fully integrated AC-DC regulator over wide frequency range for implantable bio-medical

devices. In 2014 International SoC Design Conference (ISOCC) (pp. 44-45). IEEE.