Interference Suppression Techniques for RF Receivers

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Kuangyuan Ying

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Introduction

1.1 Background

There has been more than a hundred years of history for the development of wireless radio communication. On December 12, 1901, the reception of the first transatlantic radio transmission, was received by Guglielmo Marconi, using a 500-foot (150m) kite-supported antenna [1], to hear the faint clicks of Morse code for the letter "s". Nowadays, radio communication has become essential for people's daily life. With mobile devices small enough to fit in a pocket, people can communicate over distance, watch media and acquire the latest happenings in the world by just moving fingers. The heavy usage of mobile devices and various applications also reflect the dramatic increase of data rate over the years. Fig. 1.1 shows the observation of the data rate of shorts links, LAN and cellular communication. It follows the prediction of Edholm's Law that the increase of wireless communication data rate follows exactly the Moore's Law rate: doubling every 18 months [2, 3]. While radio communication keeps developing for higher data rate and heavier usage, it poses tough requirement for different wireless devices to co-exist with each other. Interference is no doubt a major challenge in the scenario that multiple devices operate simultaneously in close proximity.

It is also a major challenge while we develop next-generation wireless communication systems for higher data rate and spectral efficiency. One of the ideal features for next-generation wireless system is enhanced flexibility, by using a single mobile radio to cover a wide frequency range and support many different applications. Take an example of today's mobile phones. Multiple

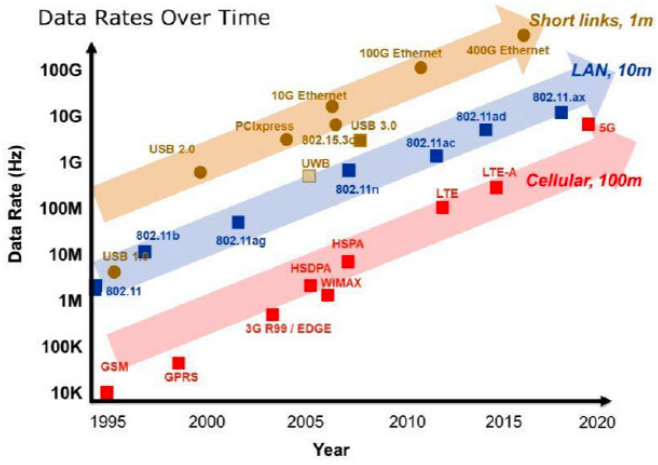

Figure 1.1.: Edholm's law: the wireless communication data rate doubles every 18 months [2, 3].

Table 1.1.: Wireless communication related IC chips inside a Xiaomi Mi 10© mobile phone.

	IC	Module	Frequency
Qualcomm	SDX55	5G Modem	
Qualcomm	QET6100	Envelope Tracking IC	
Qualcomm	QET5100	Envelope Tracking IC	
Qualcomm	SDR865	RF Transceiver	
Qualcomm	QCA6391	Wi-Fi 6 / BT SOC	
Qorvo	QM77040	FEM	band n41, n3
Qorvo	QM77032	FEM	2G, B26, B8, B12, B20
Qorvo	QM42391	FEM	WLAN 2.4G
Qorvo	QM45391	FEM	WLAN 5G
Qualcomm	QDM2310	FEM	
Qualcomm	QPM6585	PAM	band n41
Qualcomm	QPM6577	PAM	band n77/78
Qualcomm	QPM6579	PAM	band n79

standards are supported simultaneously, such as LTE, WiFi, GPS, Bluetooth, NFC, etc, mostly operating in the sub-6GHz frequency. In order to avoid the unwanted interference from different radios and corruption to the signal quality, multiple narrow-band radio front-ends are typically used to provide RF filtering. These front-ends are typically composed of filters and amplifiers, which add to the cost and size of the PCB. Table 1.1 [4] summarizes IC chips on the PCB inside a Xiaomi Mi 10© mobile phone that are related to wireless communication. Alternative to multiple narrow-band radio paths, a single wideband receiver, such as software-defined radios (SDR), can cover the sub-6GHz range. It has much less complexity and provides higher flexibility, however due to the absence of RF filtering, it must be able to tolerate interferers to avoid unwanted effects such as desensitization, cross modulation, reciprocal mixing, insufficient image rejection and harmonic rejection, etc.

Full duplex wireless is another hot research topic of wireless systems to pursue high data rate and spectral efficiency. More specifically, same frequency full duplex wireless is the focus here that it allows the simultaneous transmission and reception at the same frequency, ideally doubling the spectral efficiency compared to a time-division duplexing (TDD) or a frequency-division duplexing (FDD) system. This is very much needed for the development of wireless systems considering that the available bandwidth, especially in the sub-6GHz is very rare to find. The major challenge on the PHY layer of a full duplex system is the suppression of self-interference from the transmitter, which falls directly in the bandwidth of the receiver. On one hand, this self-interference can not be filtered by traditional frequency-domain filtering. On the other hand, the amount of suppression needed is huge to be below

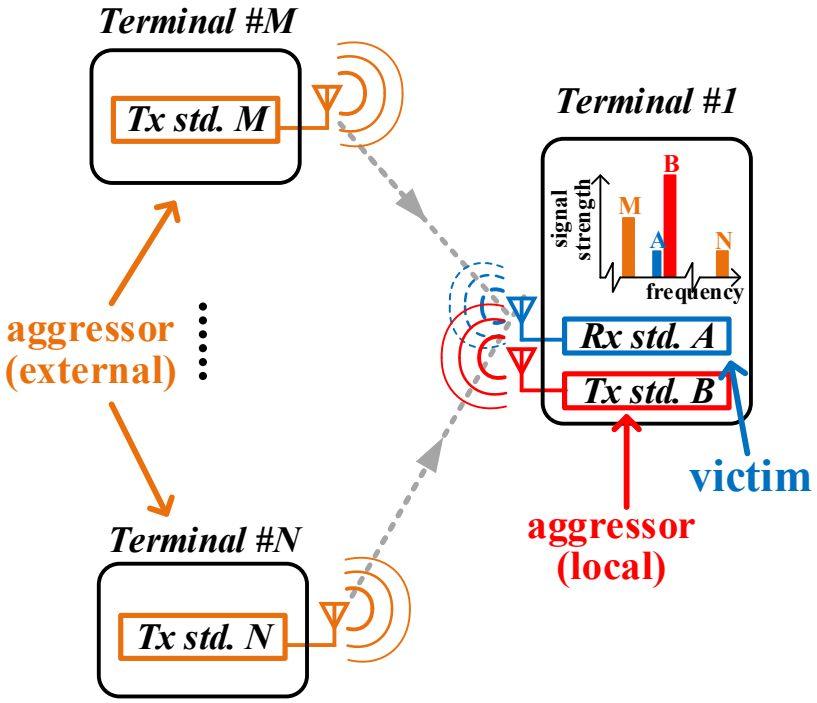

Figure 1.2.: The interference scenario that the receiver of standard A in terminal #1 is plagued by the strong signals transmitted by terminal #1, terminal #M, or terminal #N.

the receiver noise floor, which can be as large as 100dB [5]. The ability of self-interference suppression is essential for a compact and low cost on-chip integration.

To conclude, interference suppression is a major challenge in the development of wireless communication today and in the future. In this thesis, we will be investigating interference suppression techniques suitable for multi-radio coexistence and future spectral-efficient wireless systems.

1.2 Aim and Scope of the Thesis

The interference scenario within the scope of the thesis is shown in Fig. 1.2. There are three wireless terminals in Fig. 1.2. Terminal #1 is a multi-radio device. Terminal #M and terminal #N are single-radio devices. The receiver in terminal #1 is receiving information with wireless standard A, while the transmitter in terminal #1 is transmitting with wireless standard B. Terminal #M and terminal #N are transmitting information through wireless standard M and N, respectively. In this case, the receiver in terminal #1 is plagued by

the transmitting signal from either the transmitter in terminal #1, terminal #M, or terminal #N. In this scenario, the term 'victim' is used for the receiver in terminal #1, and the term 'aggressor' is used for transmitters in terminal #1, terminal #M and terminal #N. The input spectrum at the receiver antenna in terminal #1 is shown accordingly. Due to the difference of wireless standards and coupling paths, the interference signals received at the receiver antenna are different in frequency and power. The interference signal from the colocated transmitter in the same device (Terminal #1) is usually much stronger because of the small size of a handset device.

The aim of the thesis is to investigate interference suppression techniques that are suitable to deal with multi-radio coexistence scenario and interference problems in future wireless systems such as software-defined radios or full duplex systems. The appropriate technique should deal with both interference generated locally within the device and externally outside the device. The internal interference may be coming from other radios in the same device, such as terminal #1, or TX leakage from the same radio transceiver. In this case, the interferer could be stronger and the information of the interferer is known. For the external interference, the information of the interferer is unknown but it's usually smaller in power.

The appropriate technique should also be able to deal with interference within a wide frequency range and independent of the offset frequency between interference and the desired signal. In such way, the radio receiver can cover a wide RF bandwidth and suppress the interferers fall in the band. It is also suitable to work with either TDD, FDD or full duplex systems as the interferer suppression is independent on the offset frequency.

The appropriate technique should suppress the interference and at the mean time keep the other system performance uncompromised, such as sensitivity, linearity, power efficiency, etc. As will be analyzed in Chapter 2, insufficient interferer suppression will cause problems such as desensitization, cross-modulation and intermodulation distortion, reciprocal mixing, insufficient harmonic rejection and image rejection, etc, that lead to signal corruption. The most straightforward way to deal with strong interferer is to increase the dynamic range by using more current consumption. However with appropriate techniques, such design trade-off between system performance and power efficiency can be avoided.

1.3 Own Contributions

To address the interference problem in wireless RF receivers, a nonlinear transfer function based technique was studied, implemented in a test chip and later measured which suppresses larger interferer and enhances receiver performance in terms of linearity, noise figure, signal-to-interference ratio and power efficiency.

We studied and analyzed the consequences of the proposed technique on the interferer and wanted signal. We extended the nonlinear transfer specific behavior analysis to the calculation of NF. Different from the system in [6] which aims to tackle local interference only, this thesis also aims to tackle external interference of which the envelop information is unknown. Therefore we studied the accuracy requirement on the envelope extraction path to avoid system level performance degradation.

The envelope detector and the nonlinear transfer based receiver was implemented in a 40nm CMOS technology. The envelope detector was designed to cover the sub-6GHz and achieve low delay and high accuracy simultaneously by using a 2nd harmonic cancellation technique. The receiver was characterized in both linear mode and nonlinear mode, for different receiver performance parameters like NF, gain, linearity, etc, with and without the presence of strong blockers. The measurement results agreed well with the analysis presented in this thesis and we demonstrate the advantage of the proposed technique on system performance through the comparison between linear mode and nonlinear mode operation.

1.4 Thesis Overview

The rest of the thesis is organized as follows:

Chapter 2 discusses the interference scenarios of interest in this thesis, with a classification on interference power and offset frequency. The problems related to interference are desensitization, intermodulation, reciprocal mixing, channel selection and increase of power consumption. The state-of-the-art approaches regarding interference suppression or tolerance are discussed. Further information and supporting material for this chapter could be found in Paper A.

Then, in Chapter 3, the mechanism of our proposed nonlinear-transfer based interference suppression technique is revisited. We analyzed the different consequences for the unwanted large interferer and the wanted signal mathematically. The receiver system based on this method is proposed to suppress interference generated both locally and externally. The system-level performance and requirement are analyzed. Further information and supporting material for this chapter could be found in Paper A.

Next, Chapter 4 presents the design and implementation of the envelope detector, which is used to extract the large interferer envelop amplitude in the receiver system. We showed by using quadrature signal generation and 2nd harmonic cancellation, the design trade-off between detection speed and accuracy can be overcome. Further information and supporting material for this chapter could be found in Paper B.

Chapter 5 presents the work of a wideband blocker-resilient receiver based on the nonlinear interference suppression technique presented in Chapter 3 in

a 40nm CMOS technology. The measurement results proved the theory developed in previous chapters and demonstrated superb receiver performance with the presence of strong blocker. Compared with linear mode operation, the receiver operates in nonlinear mode and achieves 78.5dB SIR improvement with no extra power consumption under a 5.3dBm blocker signal. Further information and supporting material for this chapter could be found in Paper C and Paper D.

Finally, Chapter 6 presents the conclusion and the recommendations for future work.

2

Coexistence Issues and State-of-the-Art

2.1 Coexistence scenarios

The simplified diagram of multi-radio coexistence is shown in Fig. 1.2. In this section, the interferers in a multi-radio coexistence scenario are classified into different categories based on their frequency and amplitude.

2.1.1 Interference due to crowded spectrum

In a mobile phone nowadays, there are several wireless standards supported and operating at the same time. Fig. 2.1 shows the frequency allocation of different standards supported in mobile devices, in the frequency range from 1800 MHz to 2900 MHz. In this frequency range, there are several highly-used wireless communication standards, such as FDD LTE, TDD LTE [7], WiFi [8, 9], Bluetooth [10], WiMAX [11], etc. The frequency spectrum is allocated differently for different countries and regions [12, 13]. The main observation is that the spectrum is very crowded. Several key points are:

1) The frequency separation between TX and RX band in several cellu-

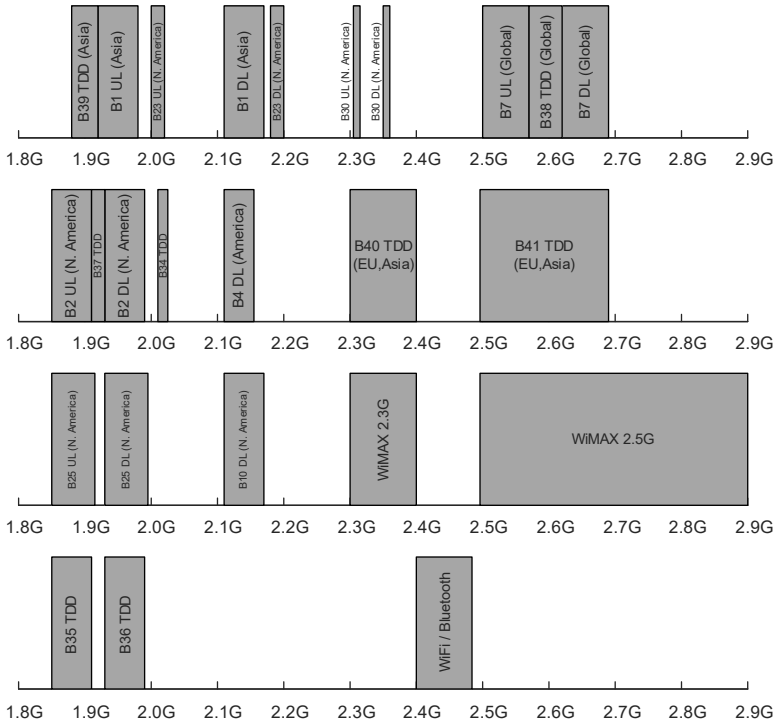

Figure 2.1.: Frequency allocation of different wireless standards supported in mobile phones, in the frequency range from 1800MHz to 2900MHz.

lar FDD bands is very small. The frequency separation is 15MHz and 20MHz, in GSM900 band and DCS1800 band, respectively.

2) The smallest frequency separation between WiFi and LTE is 12 MHz.

3) FDD LTE, TDD LTE, WiFi, Bluetooth and WiMAX share a large frequency spectrum.

More importantly, the trend of the frequency gap between different standards is towards even closer because of increasing over-allocation of the frequency spectrum. Therefore, for the multi-radio coexistence in this frequency range, and for future operation with even more crowded spectrum, it requires filtering for interferers located very close to the desired signal in frequency domain.

2.1.2 Interference due to physical proximity

The interference scenarios can be divided into two classes in terms of physical distance, namely colocation and proximity. The collocation scenario refers to a case when multiple radios are placed in the same physical unit and the interferers are thus generated locally, i.e., inside the device.

As an example, the location of different antennas inside a Samsung S8© mobile phone is shown Fig. 2.2 [14, 15]. There are 7 antennas related to WiFi and Cellular wireless communication placed at different locations inside the phone. The transmitting power of LTE user equipment is 24 dBm [13]. According to [16], the physical dimension of the S8 is 148.9mm by 68.1mm by 8mm. In such dimension, the antennas are in the near field and coupling is really present between different antennas. The isolation between different signal paths depends on the stopband attenuation of off-chip SAW filters. There are other possible ways to increase the isolation, such as by using different antenna types, different polarization, etc, though the limitation from the small physical dimension needs also to be considered.

The proximity scenario happens when multiple devices are placed physically very close to each other. The transmitting signal from one device becomes interference for the receivers in other devices. This type of interferers are generated externally. They could be coming from LTE small cell access points or WiFi routers [17]. The typical transmit power of an access point is around 20 to 30 dBm. The free space loss at 2.4 GHz for a distance of 0.5 m is 34 dB. Therefore, for both scenarios, the interference power at the input of the victim receiver can be as strong as several dBm.

2.1.3 Interference scenarios of interest in this thesis

The interference scenarios of interest can be summarized into three cases:

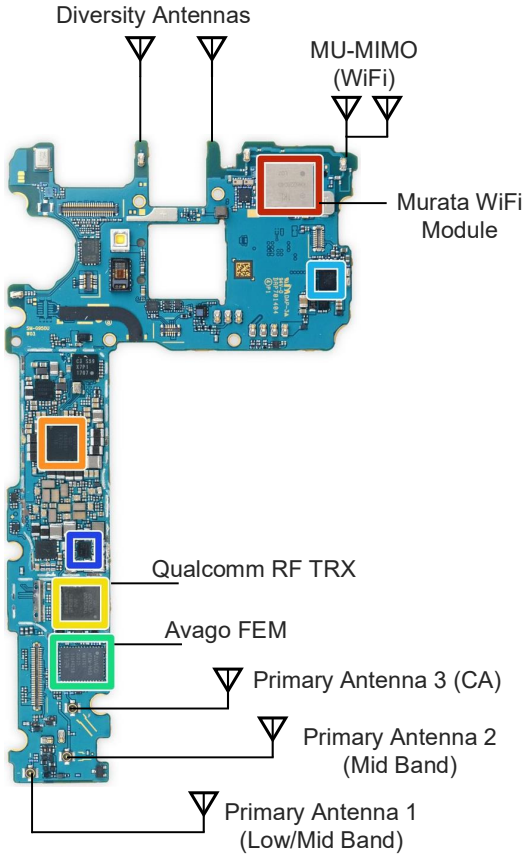

Figure 2.2.: Different signal path and antenna location related to WiFi and LTE wireless communication on the PCB board in a Samsung S8© mobile phone [14, 15].

1) *Out-of-band (OOB) interferers*
They are coming from different standards and are located far away in frequency.

2) *Interferers from other standards and at small frequency offsets (tens of MHz), e.g. the WiFi and LTE coexistence scenario*
This category includes local interference due to antenna coupling and external interference from other devices. In both casaes, the amplitude of interferers can be several dBm.

3) *Interferers from the same standard: in-band (IB) interference, e.g. the coexistence between WiFi and WiFi, LTE and LTE, FDD LTE transmitter and receiver*
This category includes local interference due to TX leakage in frequency division duplex (FDD) or full duplex (FD) systems, and external inter-

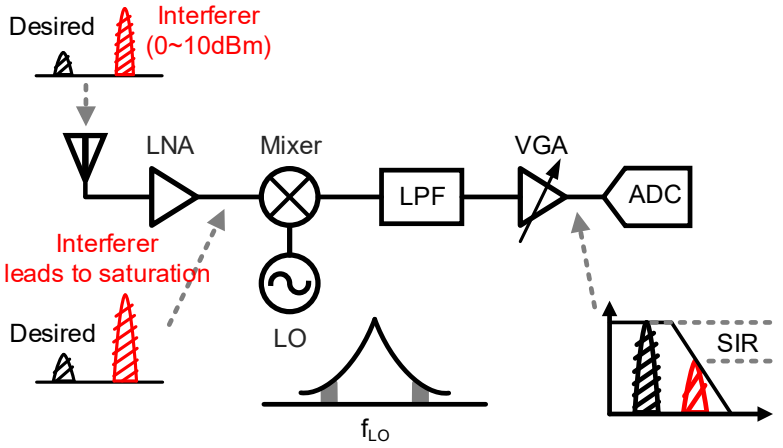

Figure 2.3.: General overview of receiver design challenges when a strong interferer is present at the receiver input. The challenges include saturation, desensitization, reciprocal mixing, output SIR degradation and power consumption.

ference from other devices. The TX leakage depends on the isolation provided by the duplexer. Both interference power can be as strong as several dBm.

2.2 Related problems

Radio receivers need to deliver good performance to maintain a reliable wireless link at a certain data rate. The key performance parameters are NF, linearity, power consumption, etc. The presence of interference adds extra difficulties in the receiver design. The problems related to interference signals include desensitization, reciprocal mixing, harmonic mixing, intermodulation, cross-modulation, insufficient image rejection, etc. In order to tolerate a large interferer, extra power consumption might be needed for increasing the linearity of the receiver. These problems are more severe if the interferer power is large or the offset frequency between the interferer and the wanted signal is small.

Fig. 2.3 gives a general overview of these challenges. Suppose the input is composed of a weak desired signal and a large interferer. According to the interferer categorization in previous subsection, the large interferer power could be as high as 0 to 10dBm. Firstly, assuming the LNA has 20dB gain, the interferer could be as high as 20 to 30dBm at the LNA output, already saturating the receiver. Secondly, after the LNA, the interferer mixes with LO phase noise, thereby increasing the noise in the receiver band. Thirdly, in order to handle a large interferer, the linear receiver typically needs to have a large dynamic range, which would increase the receiver's power consumption.

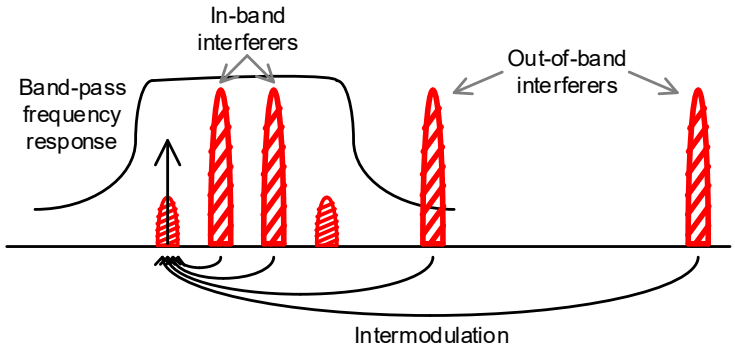

Figure 2.4.: Third-order intermodulation product from two in-band or out-of-band interferers that falls on top of the desired signal.

2.2.1 Desensitization

Due to the compressive characteristics [18] of a typical nonlinear system[1], the gain experienced by the wanted signal at the input becomes smaller as the input power becomes larger. This effect is quantified by the 1-dB compression point, P_{1dB}, defined as the input signal level that causes the gain to drop by 1dB from the ideal gain observed at very low input signal levels. This is a large-signal linearity parameter. With the presence of large interference, it causes another effect that the small wanted signal experiences gain compression due to the large excursions produced by the strong interferer. This is often called blocker desensitization and quantified by blocker 1-dB compression point, B_{1dB}. Both phenomenons lower the signal-to-noise (SNR) ratio at the receiver output. If the blocker is too large, it could cause the wanted signal to be below the noise floor, or the receiver to be saturated.

2.2.2 Intermodulation

Desensitization is a phenomenon that characterizes large-signal linearity involving a wanted signal accompanied by a large interferer. Another phenomenon characterizes the small-signal linearity performance when the wanted signal is accompanied by two interferers. This phenomenon is very likely to happen in a multi-radio coexistence scenario as in Fig. 1.2, where multiple radios are transmitting signals in different standards and frequencies. The interferers could be either in-band or out-of-band, while the intermodulation product could be generated in-band and falling on top of a wanted signal, as shown in Fig. 2.4.

[1] All these considerations are based on the polynomial model of the transfer characteristic of the system, i.e. $y = a_1 x + a_3 x^3 + ...$, as explained in [18].

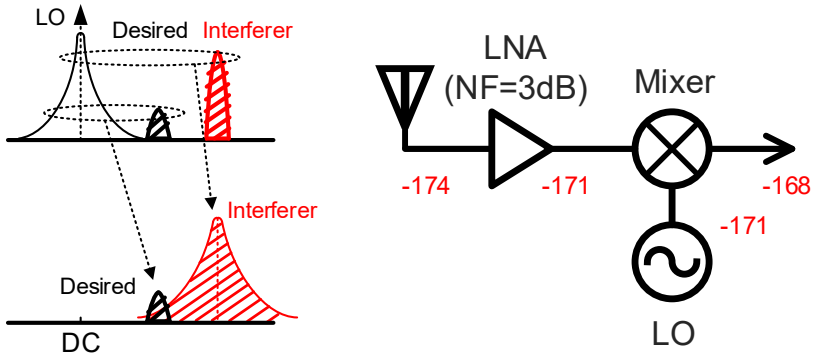

Figure 2.5.: Left: Reciprocal mixing, down-conversion of a desired signal accompanies by a strong blocker with a noisy LO. The reciprocal-mixing product adds corruption to the desired signal due to the additional noise.
Right: Example of reciprocal mixing of the noise floor at each stage of the receiver that could cause a 3dB noise figure degradation when a 0dBm blocker is present at the input.

Third intercept point, IP_3, is used to characterized the intermodulation product in a two-tone test. The amplitude of each tone is called the input third intercept point, IIP_3, which is an extrapolated result of the plots of the fundamental tone amplitude and the intermodulation product amplitude versus amplitude of each input tone. For accurate extrapolation, the input amplitude is kept small, i.e., higher than the noise floor, but well below compression, in the range where the rule of 3dB increase in the intermodulation product for every 1dB increase in input amplitude holds. Therefore it is a small-signal linearity performance parameter.

2.2.3 Reciprocal mixing

Fig. 2.5 illustrates the problem of reciprocal mixing with the down-converted frequency spectrum on the left and the receiver front diagram on the right. During down-conversion, the desired signal and the large interferer are convolved with a noisy LO signal. The down-converted interferer has a broadened spectrum of noise skirt due to its high power level and the phase noise of the LO. The noise skirt falls on top of the down-converted desired signal. It degrades the signal-to-noise (SNR) ratio at the output of the mixer.

To quantify the reciprocal mixing problem, the noise level at each stage of the receiver front-end is shown in Fig. 2.5. The thermal noise floor density at the input of the system is -174dBm/Hz. We will assume that the LNA has a noise figure of 3dB. Furthermore, we will assume the LNA has unity gain for simplicity, as the desired signal, the interferer and the noise floor are all amplified. The noise floor at the LNA output is -171dBm/Hz. Assuming the

interferer is 0dBm after the LNA and at an offset frequency from the LO signal of which its phase noise, when mixed with the interferer, corresponds to a -171dBm/Hz input-referred noise signal. Hence the noise floor at the IF output has an additonal 3dB degradation. Thus 50% of the total 6dB SNR degradation is coming from the receiver signal path and 50% of it is coming from reciprocal mixing.

Two observations need to be noted here. Firstly, the LO phase noise is assumed to be -171dBc/Hz, which is a very ideal and unrealistic number. For example, [19] reports a phase noise of -131dBc/Hz at 1MHz offset and -153dBc/Hz at a 10MHz offset from a 3.7GHz LO frequency. Imagining with a 0dBm blocker at 10MHz and a LO phase noise of -153dBc/Hz, the SNR degradation due to reciprocal mixing is 18dB and dominating the SNR degradation.

Secondly, the reciprocal mixing is more severe if the blocker power is stronger or if the offset frequency from the wanted signal is smaller. This phenomenon puts difficult requirement in the design of a low-phase-noise oscillator, calling for very low phase noise levels at small offsets. It also puts difficult to the requirement of the tolerance or filtering capability of large interferers, especially when the offset between the wanted signal and the interferer is small. This scenario will happen very likely in a multi-radio coexistence scenario or in the operation of software-defined radios.

2.2.4 Channel selection

With the ever increasing wireless standards and applications, there's a trend nowadays to use a single radio device, such as wideband radios [20–23] or software-defined radios [24–29]. It saves the complexity of multiple radio paths and reduces the number of off-chip components required for different paths. The off-chip components are often bulky and add to the PCB bill-of-material (BOM). Besides, this approach also tightens the NF specification of integrated on-chip receiver.

Without the off-chip filters, the radio receiver has to integrate the band-select function and the ability to filter out-of-band interferers on chip. The former one is usually implemented as a current-mode mixer and baseband TIA stage [add citation], where the mixer up-converts the low-pass frequency response to RF frequency to form a band-pass frequency response. The latter one is also important as it could avoid the problems mentioned previously such as reciprocal mixing, harmonic mixing and receiver desensitization.

2.2.5 Power consumption

In order to handle a large interferer, the linear receiver needs to have a large dynamic range. The power dissipation will scale with the dynamic range, and therefore the blocker level. Thus, every 10dB extra blocker level will result in

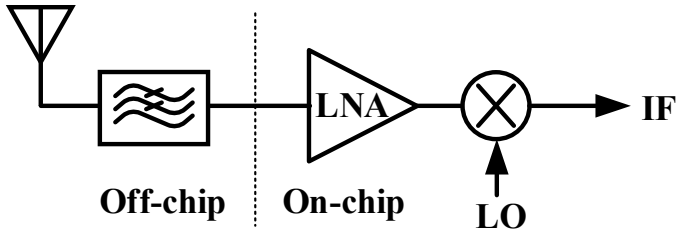

Figure 2.6.: Simplified system architecture of a conventional narrowband receiver with off-chip SAW filters.

10 times higher power dissipation of the circuits. However if some interference suppression can be provided at an earlier stage of the receiver chain, the power consumption for the following circuit blocks can be reduced.

2.3 State-of-the-art

There have always been needs for interference filtering in modern wireless receivers. Conventionally, as shown in Fig. 2.6, this is provided by an off-chip filter component, typically a surface acoustic wave (SAW) filter, which enables high-Q filtering to suppress out-of-band interferers. Lately, the development of software-defined radio or full duplex systems aims to use the frequency spectrum more efficiently and more flexibly. There are several approaches for achieving on-chip interference filtering, which have been heavily investigated in the recent years, and they are reviewed here.

2.3.1 N-path mixer

N-path filtering [30, 31] technique is widely implemented on-chip to suppress out-of-band interferers. The main idea is to use passive switches with non-overlapping multi-phase LO signals to translate the baseband low-pass frequency response to a band-pass frequency response around the LO frequency. This idea is used as up- or down-conversion mixer together with baseband circuits or as tunable bandpass or notch filters, as will be discussed here. Besides, they are also used in circulator design [32], or in beamforming arrays [33].

The mixer-first architecture uses N-path passive mixers directly after the antenna without an LNA [31, 34–40]. CMOS switches benefit from technology scaling with smaller on resistance and parasitic off-state capacitance. The architecture is shown in Fig. 2.7. It delivers good linearity due to the usage of passive mixer and no RF gain. However due to the switch resistance, the NF and the out-of-band filter rejection are degraded. The work described in [31] reports a NF of 6.5dB and an IIP3 of 11dBm. Some techniques have been used to lower NF and harmonic re-radiation such as using 8-phase mixing in-

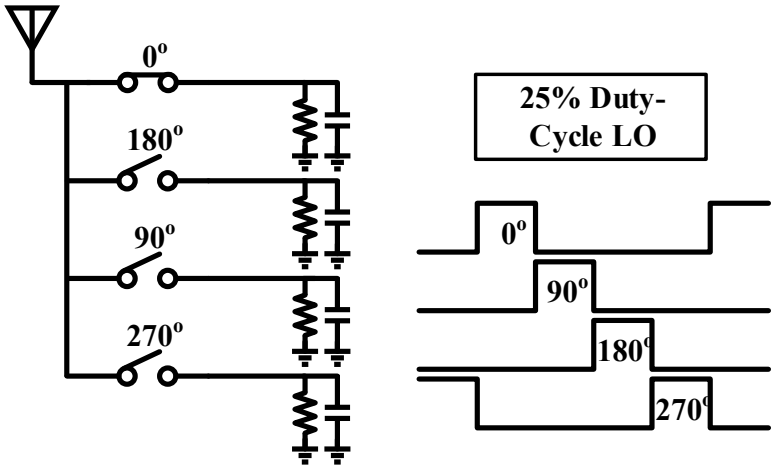

Figure 2.7.: Model of 4-phase passive mixer with baseband RC and 25% duty cycle LO waveforms.

stead of 4-phase [37, 41–43]. Other techniques on baseband amplifiers such as complex feedback [35, 37], passive switch connection and higher-order filtering response [44–47] are used to improve out-of-band linearity parameters such as IIP3 and B1dB. With these techniques applied, the mixer-first receivers could achieve below 3dB NF [43, 47], blocker 1dB compression point (B1dB) of -20dBm at 5MHz offset and 15dBm at 30MHz offset [48], and out-of-band IIP3 of 44dBm [46].

Several LNA-first architectures also deploy N-path mixers to provide filtering to out-of-band interferers [49–57]. The existence of an LNA further reduces the receiver NF and re-radiation with more isolation between antenna and N-path mixer. In order to avoid saturation by LNA gain, current-mode LNTA are used so that the voltage swing at the LNA output is reduced to have a better linearity. Furthermore, noise cancelling is deployed with a Gm cell in combination with an N-path mixer at the axillary path to cancel the noise of the mixer-first architecture at the main path [27, 58], as shown in Fig. 2.8. With these techniques applied, the LNTA-Mixer receivers could achieve better NF at 2dB [27], at the cost of compromised linearity with out-of-band B1dB of around 0dBm, and out-of-band IIP3 of 10 to 20 dBm [27, 56, 57].

The receiver blocker NF measured in the above literature assumes the usage of an ideal external LO signal. However with an LO on chip, the reciprocal mixing with strong blocker will degrade the blocker NF severely. The design in [59] deals with the reciprocal mixing by using an auxiliary path to create a replica of the in-band reciprocal mixing and then subtracts it from the main path. It reports a 7dB noise figure for a blocker power of -15dBm at 20MHz away. [29] extends the phase noise cancellation (PNC) idea to deal with mod-

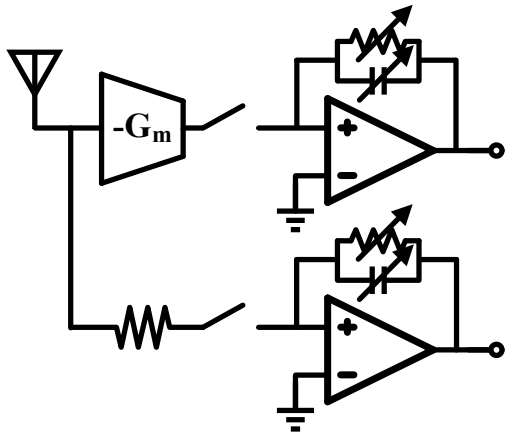

Figure 2.8.: Simplified system architecture of the frequency-translational noise-cancelling receiver in [27].

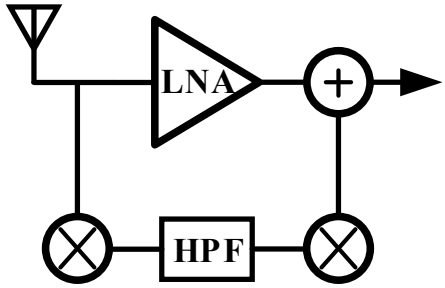

Figure 2.9.: Simplified system architecture of a two-path feedforward receiver front-end with a notch filter on the axillary path [60].

ulated blockers and improves linearity. It reports a 0dBm blocker NF of 13.5 dB with PNC on, compared with 32 dB with PNC off while the PNC block consumes 11 mW.

2.3.2 N-Path Filter

N-path RC circuitry can also be used as filter blocks with tunable center frequency. It can be used as a single stage band-pass filter [61, 62] or notch filter [60, 63, 64], or multi-stage filters [65]. High-Q filtering can be achieved if the RC pole frequency is on the order of MHz with the RF center frequency at GHz ranges. However, the dynamic power consumption is proportional to the center frequency and the number of stages. The design in [64] reports an 18 dB filtering capability at 6 MHz offset. The filtering capability is mostly limited by the switch resistance and accuracy of the LO duty-cycle. The design

in [65] reports a 59 dB filtering capability at 100 MHz offset. The filtering is improved with 3 cascaded filter stages, however the LO generation sees bigger capacitance and consumes a significant power of 43mW while operating at 1.2GHz.

2.3.3 TX Leakage Cancellation

The interference cancellation techniques dealing with specific TX leakage are described in several papers. They use active [5, 66–68] or passive circuits [69] to create a replica of transmitting signal with the right amount of delay to cancel the TX leakage on the receiver path. This cancellation could happen either before or after the mixer.

An active cancellation of TX leakage is described in [5]. It repurposes the CG device of a noise-cancelling LNTA by applying a properly scaled TX leakage replica at the gate of the CG device so that the TX leakage is eliminated at the LNTA input. However the TX leakage current is still flowing down the CG path, therefore a replica current of the TX leakage is injected at the output of the CS device in the LNTA so that it can be cancelled at the baseband output. Another active cancellation of TX leakage is described in [68] with the similar noise-cancelling two-path receiver topology. The difference is that is the TX replica is created and injected directly at the input of the LNTA, so that TX leakage is eliminated at the input and not flowing into the down-conversion path.

The main limitation of the two approaches comes from the creation of the TX replica. As the TX leakage is cancelled at RF, the TX replica needs to be created with a small delay that matches the TX-RX leakage path. This limits the bandwidth of the cancellation to 4MHz in [68]. In [68], with a 0dBm blocker at TX output and -20dB of TX-to-RX coupling, the NF degradation is 0.6dB. For stronger TX leakage power, the two approaches would still suffer from reciprocal mixing induced NF degradation.

Another topology of self-interference canceler is described in [69] that adopts a passive mixer-first receiver. The TX replica is created by a vector modulator and injected at the baseband of the receiver path. The cancelling path consumes 10mW. The TX leakage power at 1dB RX compression is 1.5dBm with 27dB cancellation. The cancellation is limited by the resolution of the vector modulator. Also due to the mixer-first receiver topology and the loading from the canceler path to the baseband path, the receiver NF is more than 10dB with the canceling path enabled.

2.3.4 Duplexer

Duplexer is a key building block for frequency-division duplexing (FDD) systems and provides isolation between TX and RX signal path at RF. [70] presents

an integrated tunable electrical-balance (EB) duplexer that achieves more than 50dB TX-to-RX isolation and a TX-to-Antenna IIP3 of over 70dBm. However it introduces loss on the TX and RX path, which is 3.7dB and 3.9dB respectively. This leads to an increase of receiver noise figure and a reduction of TX output power. Besides, as it is based on passive components like transformers and inductors, it also takes a large onchip area of $1.75mm^2$.

2.3.5 Nonlinear Interference Suppression

A completely different approach of TX leakage cancellation is first implemented in [6] and later also used as an interference-resilient technique in a low power receiver [71]. The key idea is to exploit the property that nonlinear transfer function does not obey the rule of superposition. Therefore a small wanted signal is amplified while a large interferer is simultaneously suppressed, if they are passed together through a specifically tailored nonlinear transfer function. The filtering is based on the amplitude discrimination between a desired small signal and a large interferer, and essentially independent on the frequency offset between them. In [6] the nonlinear transfer is created by combining the transfer function of a linear amplifier and a clipping amplifier, thus creating a sort of zig-zag transfer function. By adjusting the bias current of the clipping amplifier, the nonlinear transfer is adjusted accordingly to the instantaneous interferer amplitude in such a way that the interferer gets canceled. The circuit achieves more than 30dB suppression of blockers in the range from 0 to 11dBm.

However, the implementation in [6], as shown in Fig. 2.10, has several limitations. Firstly, the power consumption of the clipping amplifier is directly proportional to the interference power. The circuit consumes 35mW in total for a blocker power of 11dBm. Secondly, it uses a resonant tank at the load which limits its operating bandwidth. Although the nonlinear interference suppression idea is frequency independent, the design in [6] only suppresses interference in a relatively small bandwidth around 1.8GHz. Thirdly, the nonlinear interference suppression idea is implemented as an RF stage amplifier providing good suppression. However its effect on reciprocal mixing and linearity performance in a receiver including down-conversion and baseband stages is not proven. Finally, another important limitation of [6] is that it works only in the case of self-generated interference, because knowledge on the envelope of the interferer is needed for dynamically adapting the nonlinear transfer function.

This last technique of providing interference suppression in the amplitude domain by using nonlinear transfer function is essentially frequency-independent, which makes it very promising for dealing with strong interference at small offset. This technique will be further discussed in detail in the following chapter.

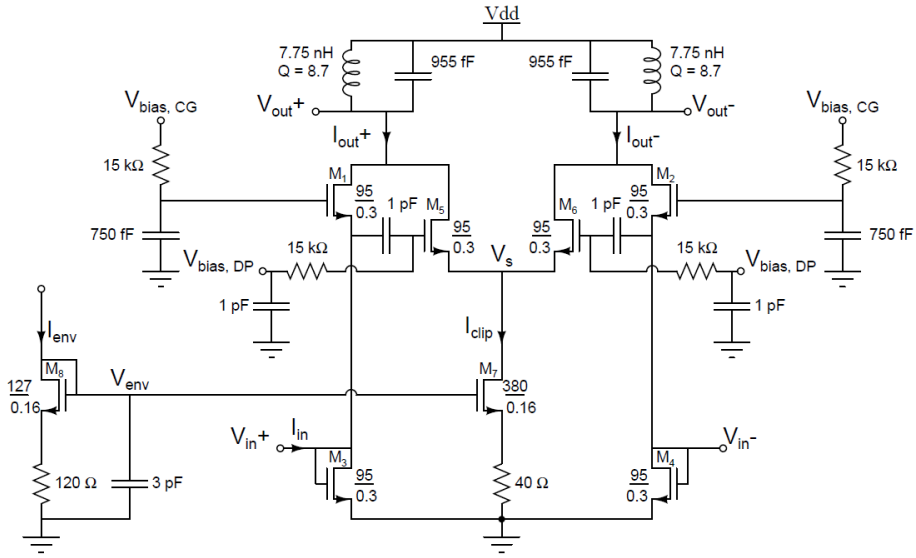

Figure 2.10.: The schematic of NIS core circuit described in [6]. It consists of a linear amplifier with transistors M_{1-4} and a clipping amplifier with transistors M_{5-7}. The nonlinear transfer function is created by combining the current at the output.

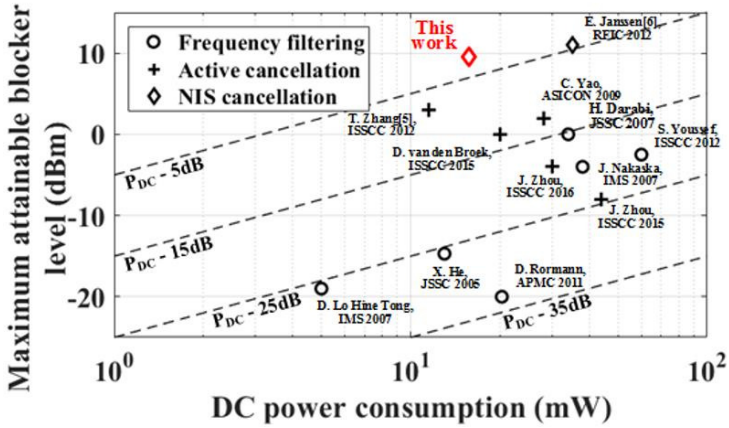

Figure 2.11.: Maximum attainable blocker level versus power consumption. The 1dB compression point is used in case a maximum level is not specified.

2.3.6 Benchmark of the Interference Suppression Techniques

In the previous subsections, the pros and cons of different interference suppression techniques have been analyzed on the capability of interference sup-

pression while simultaneously maintaining the other receiver performance such as noise, linearity and power consumption. To illustrate the comparison of power efficiency between the different techniques, Fig. 2.11 summarizes the reported performance on the maximum attainable blocker power against the DC power consumption of the RF circuitry. The 1dB compression point is used in case a maximum attainable blocker power is not specified. It indicates that only the NIS cancellation technique exceeds the 'PDC-5dB' line. Compared with [6], the proposed NIS circuit maintains the maximal attainable blocker level at around 10 dBm while the power consumption is halved.

3

Mechanism and System Level Analysis of Nonlinear Interference Suppression

3.1 Mechanism behind Nonlinear Interference Suppression

3.1.1 Time- and Frequency-Domain Behavior for Different Transfer Functions

Nonlinear transfer functions behave fundamentally different from linear transfer functions. The nonlinear transfer function does not obey the rule of superposition. The signals passing through a nonlinear system can undergo different operations. Also, nonlinear systems do not necessarily require a large power consumption to handle a large signal. The fundamentals of a nonlinear system make it a possible candidate to deal with interference tolerance.

The input and output signals in frequency and time domain for various transfer functions are illustrated in Fig. 3.1. When a large signal is passing through an ideal linear system as shown in Fig. 3.1(a), the signal is amplified linearly at the output. When the same input signal is passing through a conventional compressive nonlinear system as shown in Fig. 3.1(b), the signal gets distorted at the output and 3rd order harmonic is generated[1]. Fig. 3.1(c) shows a specially-tailored nonlinear system with a third-order polynomial transfer function. When the large signal pass through, the fundamental tone of the large signal is completely removed at the output, while a 3rd harmonic is created.

A combination of a strong interferer and a much weaker desired signal passing together through the nonlinear system is illustrated in Fig. 3.1(d). At the output, the large signal at the fundamental frequency is suppressed completely, while the fundamental tone of the weak signal is amplified. The 3rd harmonics are generated for both the interferer and the desired signal. Besides, an intermodulation (IM) term arises with the same power as the output of the fundamental tone of the weak signal. The intermodulation term is the result of nonlinearity and convolution between the input signals, and introduces noise folding into the signal band.

3.1.2 Nonlinear Transfer function

In Section A.3, a simple 3rd order polynomial, $y(t) = c_1x(t) + c_3x^3(t)$ was used to give an example of how nonlinear transfer function can be used to remove large interferer at the fundamental frequency. We assume here that the input signal is a strong sinusoidal signal given by $y(t) = A_{LS}sin(\omega_{LS}t)$ with amplitude A_{LS} and frequency ω_{LS}. By ensuring $c_3 = -\frac{4c_1}{3A_{LS}^2}$, the output at the nonlinear transfer function becomes $y(t) = -c_1\frac{A_{LS}}{3}sin(3\omega_{LS}t)$. The nonlinear transfer adapts to the envelop of the amplitude A_{LS} of the large interferer and

[1]This holds when the transfer function is modeled as $y = a_1x + a_3x^3$. In gerenal, nonlinearity can contain any order terms, so the even order harmonic, such as 2nd, 4th, etc, will also appear at the output.

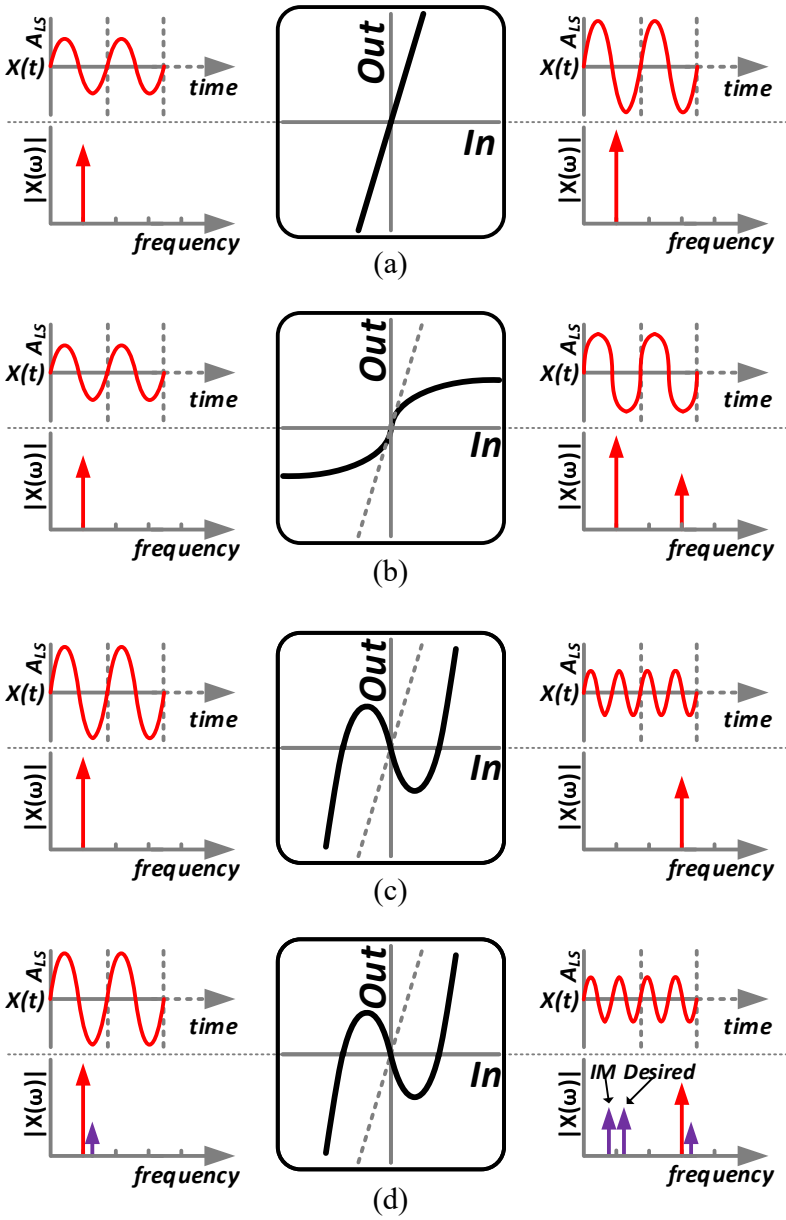

Figure 3.1.: Input and output of a large (single-tone) signal in frequency and time domain when passing through a (a) ideal linear system (b) conventional nonlinear system (c) proposed nonlinear system (d) proposed nonlinear system together with a weak signal.

the fundamental at the output is removed. Therefore for modulated interferers, the nonlinear transfer function can be altered accordingly to maintain the suppression.

Fourier analysis can be applied to the output spectrum as shown in Fig. 3.1(c) so that the requirements of a transfer function with interference suppression can be understood more clearly. As shown in Eqn. (A.8), the effective gain of the fundamental component of the strong signal G_{LS} can be expressed as:

$$G_{LS} = \frac{1}{A_{LS} \cdot \pi} \int_{-\pi}^{\pi} f(A_{LS} sin\theta) \cdot sin\theta d\theta \tag{3.1}$$

For Eqn. (3.1) to be zero, transfer function f(x) must be an odd function and have at least three zero crossing in the interval of $x \in (-A_{LS}, A_{LS})$.

Similarly, the equivalent gain of the small signal is given in Eqn. (A.11)

$$G_{SS} = \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot PDF_{sine}(x) dx \tag{3.2}$$

The small signal gain, G_{SS} is a function of large interferer amplitude A_{LS}, the derivative of the transfer function f(x) and the probability density function (PDF) of the large interferer. From Eqn. (3.1) and (3.2), both G_{LS} and G_{SS} depends on the amplitude of large interferer and transfer function y=f(x), while the phase or the frequency of large interferer and the small wanted signal are irrelevant.

3.1.3 Transfer-Specific Characteristics

Chebyshev polynomials with different orders are found to fulfill the requirement for such nonlinear transfer functions to provide large signal suppression [72]. Zig-zag function, as shown in Fig. 3.2 is created by high order Chebyshev polynomials and is used here to analyze the transfer-specific characteristics. The zig-zag transfer function can be expressed as

$$f(x) = \begin{cases} G_{lin} \cdot x + A_{clip}, & \text{if } x < -a \\ (G_{lin} - \frac{A_{clip}}{a}) \cdot x, & \text{if } -a \leqslant x \leqslant a \\ G_{lin} \cdot x - A_{clip}, & \text{if } x > a \end{cases} \tag{3.3}$$

where G_{lin} is the slope of the function in region 1 and 3. By limiting a to 0, transfer function $f(x)$ exhibits an abrupt transition in region 2, for $x \in [-a, a]$. For complete suppression of an interferer with amplitude A_{LS}, based on Eqn.

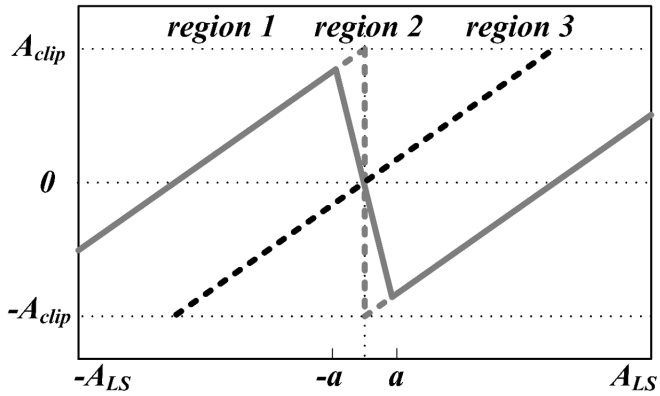

Figure 3.2.: The zig-zag transfer function shown in Eqn. (3.3). The slope in region 1 and 3 is G_{lin} and the clipping on the y-axis when a is approaching zero is A_{clip}.

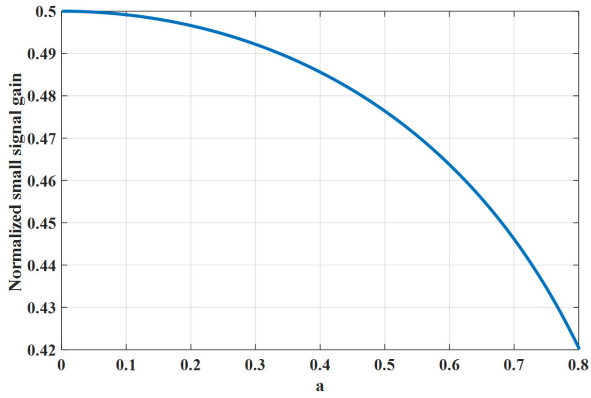

Figure 3.3.: The influence of the width of zero-transition region, a, on normalized small signal gain G_{SS} using zig-zag transfer function for nonlinear interference suppression.

(3.1), the transfer has to fulfill that

$$G_{LS} = G_{lin} - \frac{4A_{clip}}{\pi A_{LS}}, \quad A_{clip,supp} = \frac{\pi}{4} A_{LS} G_{lin} \tag{3.4}$$

The dependence of G_{SS} on the value a of the zero-transition region 2 in the zig-zag function is shown in Fig. 3.3. The normalized small signal gain varies little with change of value a, which can be explained by the weighting function of the PDF of the sinusoidal input waveform in Eqn. (3.2). Because the PDF of a sinusoidal waveform is high near the edges and low in the center, the circuit

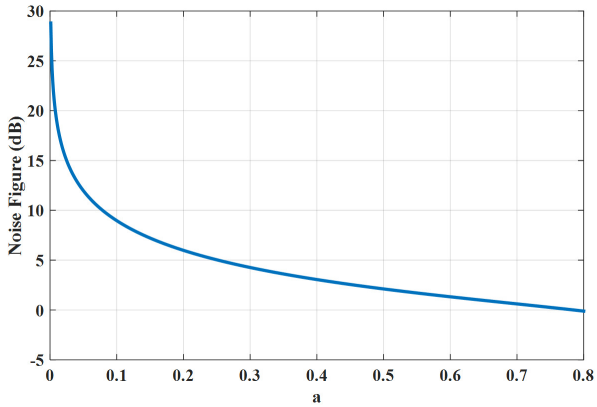

Figure 3.4.: The influence of the width of zero-transition region, a, on noise figure (NF) using zig-zag transfer function for nonlinear interference suppression.

is forced to operate mostly near the edges in large signal operation. So the derivative of the zig-zag function in region 1 and 3 plays a bigger role on G_{SS}. Therefore the weak desired signal will experience amplification if $G_{lin} > 2$ and Eqn. (3.4) is satisfied. However, the large signal suppression is decreasing with increasing a since the zig-zag function deviates more from the original setting.

The noise figure of a noiseless zig-zag transfer function over the zero-transition region 2 is shown in Fig. 3.4. By decreasing a, the NF increases steadily. This is because by decreasing a, the nonlinear zig-zag function has sharper zero transition in region 2, introducing more noise from high frequency components folding onto the signal frequency. By increasing a, the NF keeps decreasing as fewer high frequency noise components fold to the desired signal band. The NF almost decreases to zero at large values of a. However this result is meaningless since the transfer function at larger values of a is totally different from an ideal zig-zag function and Eqn. (3.4) is no longer satisfied.

3.2 System Level Requirement and Performance Analysis

3.2.1 NIS system for general interference suppression

Different from the receiver architecture described in [73], the receiver architecture proposed here aims to deal with both interference generated locally and interference generated from external devices. The difference is that the envelope amplitude of an external interference is unknown. Therefore, an envelope extraction path is needed to extract the instantaneous amplitude of the interferer so that the nonlinear transfer function could be adjusted accordingly to achieve maximum suppression.

The system architecture for general large interference suppression is shown

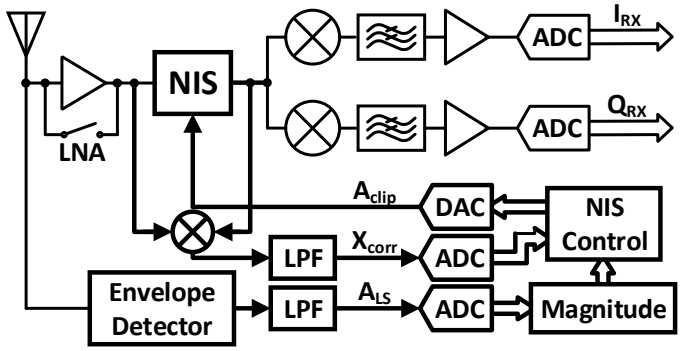

Figure 3.5.: The system diagram of the proposed NIS operation for general interference suppression.

in Fig. 3.5. The key sub-blocks in the nonlinear receiver system are highlighted: NIS, cross-correlation mixer, LPF, envelope extraction, ADC, DAC, Magnitude and NIS Control sub-blocks.The feedforward path starts from the receiving antenna and consists of the envelope extraction sub-block followed by the LPF and serves to to derive the amplitude information. The extracted envelope contains noise received by the antenna, the envelope information of the desired signal and the envelope information of interferer. However as the focus of this work is the coexistence of large interferer and weak desired signal, the envelope of the wanted signal behaves as noise and small disturbance to the control signal A_{clip}. This path can be recognized as a feedforward path which gives the correct control signal with accuracy and speed.

On the other hand, a feedback path is also needed to model the environmental changes, such as variations in the coupling between the transmitter antenna and the receiver antenna. Therefore, a mixer is placed around the NIS sub-block to provide cross-correlation between the input and output of the NIS sub-block. Assuming the interferer is the dominant signal, the cross-correlation measures how much the residue interference remains after nonlinear suppression, representing the errors in control signal A_{clip}. The cross correlation signal is fed back to the NIS control sub-block to form a feedback path. The feedback path only requires low speed to track environmental changes, while the feedforward path should be fast enough to update the control signal according to the variations of the envelope of the interferer, e.g. a blocker with strong PAPR or large bandwidth.

3.2.2 System Performance and Limitations

The nonlinear receiver system is modeled in Advanced Design System (ADS). The NIS, cross-correlation mixer, NIS Control, Magnitude sub-blocks are modeled with symbolically defined devices. The down-conversion mixer uses an

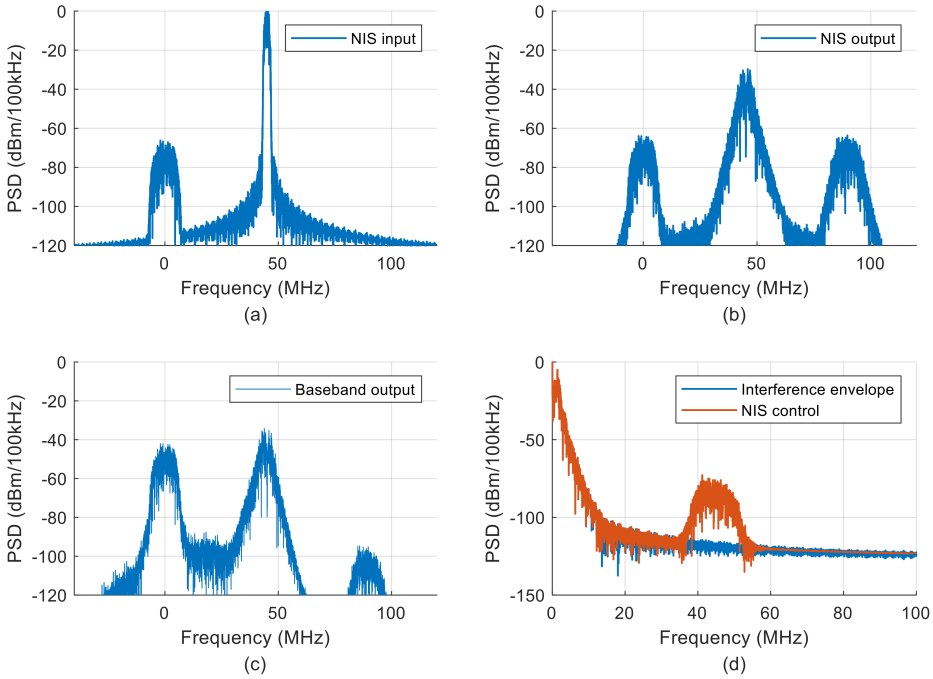

Figure 3.6.: The frequency spectrum of (a) input at receiver antenna (b) output of NIS sub-block (c) baseband output (d) envelope of the interferer (blue) and control signal for NIS sub-block (red).

ideal mixer component with ideal I/Q demodulation. The baseband filter is set as a 4th order Butterworth filter with a bandwidth determined by the data rate of the wanted signal. The amplifier is set as an ideal, i.e. linear and noiseless, 30dB wideband amplifier.

The desired signal is assumed to be a 16-QAM modulated signal with raised cosine pulse shaping and a roll-off factor of 0.5. The baseband I and Q signals have a data rate of 10 Mbps. The interference is a QPSK signal with the same pulse shaping, and a data rate of 2.5 Mbps for the baseband I and Q signals. The weak desired signal lies at 1.825 GHz with -50 dBm power and the strong interferer at 1.870 GHz with 10 dBm power. The input spectrum of the nonlinear receiver is shown in Fig. 3.6(a).

The output spectrum of the NIS sub-block is shown in Fig. 3.6(b). The fundamental component of the weak signal remains, while the interference signal is partially suppressed, by about 40 dB. After passing the baseband circuitry, the desired signal is amplified, while the intermodulation term is further suppressed, as shown in Fig. 3.6(c).The EVM at the baseband output is 5.4%, which corresponds to an SNR of 25 dB.

There are two major limitations for the level of suppression of larger in-

Table 3.1.: Interference Suppression Limitations

Interference Power (dBm)	Interference suppression at RF (dB)	EVM (%)	SNR (dB)
-30	20	14.4	17
-20	42	3.7	29
-10	56	1.9	34
0	66	1.9	34
10	80	2.9	31

terferers. Firstly, the mechanism of interference suppression by the nonlinear transfer is based on the amplitude discrimination between the interferer and the wanted signal. To illustrate this point, the weak desired signal is kept the same while the interferer power is swept from -30 dBm to 10 dBm. The resulting suppression, EVM and SNR at the baseband output are shown in Table 3.1. For an increasing interference power, larger interference suppression is achieved with better EVM and SNR. When the relative power ratio between the interferer and the desired signal is decreasing to 20dB or less, the nonlinear system will gradually become incapable to distinguish one from the other, thus leading to limited suppression of the interferer and excessive distortion of the desired signal.

Secondly, the limited suppression also comes from the inaccuracy of the extracted interference envelope amplitude. Fig. 3.6(d) shows the comparison of frequency spectrum between the interferer envelope and the control signal for the NIS sub-block. The spectrum of the control signal has an intermodulation term at Δf, due to convolution between the input signals. LPF is needed to filter out the intermodulation term. However there is a tradeoff between the filtering of the intermodulation term and the delay introduced by the filter. The filter bandwidth could be set small to filter out the intermodulation term completely, but then it will introduce a big delay on the control signal. On the other hand, if the filter bandwidth is set large so that there's little delay introduced, the residue of the intermodulation term brings error to the control signal.

The amount of interference suppression versus LPF bandwidth (BW_{LPF}) is summarized in Table 3.2. With larger BW_{LPF}, smaller delay is introduced and the interference suppression is better. To compensate the delay of the control signal, a delay block can be added before the input of the NIS sub-block. With the corresponding delay compensated, the interference suppression is decreasing when BW_{LPF} is increasing, as more intermodulation error is allowed to the control signal. Nevertheless, the delay block is not easy to implement at RF frequencies, and especially for a wideband operation.

Table 3.2.: Trade-off of BW_{LPF} on Interference Suppression

F_{LPF} (MHz)	Intermodulation (dBm)	Delay (ns)	Suppression wo. delay (dB)	Suppression wi. delay (dB)
5	-90	36	30	52
10	-69	18	38	50
20	-60	8	46	45

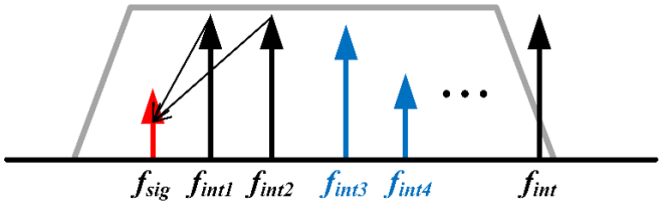

Figure 3.7.: Illustration of NIS operation principle with multiple large interferers accompanying weak desired signal (red). The interferers includes local interferers (black) and external interferers (blue).

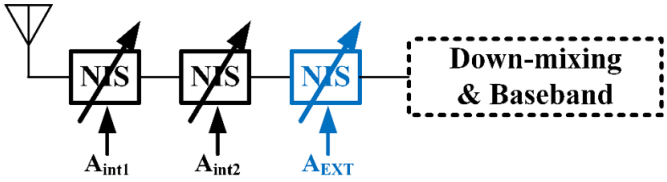

Figure 3.8.: llustration of NIS operation principle with NIS blocks for each local large interferer.

3.2.3 NIS System Operation with Multiple Large Interferers

In this section, we will consider the interference scenario with multiple large interferers, either locally or externally generated, as shown in Fig. 3.7. The weak desired signal is shown in red. The local interferers (1, 2) are shown in black and usually are the dominant signals. External interferers are shown in blue (3, 4). The grey line indicates the RF bandwidth of the NIS receiver system. In this case, the worst scenario is that the two large local interferers (1, 2) saturate the receiver, and the 3rd intermodulation (IM3) product between them is exactly located on the desired signal frequency.

The NIS operation principle with multiple interferers is illustrated in Fig. 3.8. The local interferers are dominant interferers so they should be filtered out first. Since the local interference envelope is prior-known, one NIS circuit block can be enabled for suppressing each corresponding local interferer. Therefore the NIS operation prevents the receiver from saturation. Note that for closely

spaced interferers, they can be also suppressed in one NIS block by following their combined envelope.

The influence of IM3 product on signal distortion is not alleviated as it happens before the large interferers are suppressed. Based on Eqn. (A.18), the nonlinear zig-zag transfer function based receiver has an IIP3 10 dB higher than the interferer envelope amplitude A_{LS}, which help lower the IM3 product. Besides, frequency-translational filtering techniques can be implemented as in Fig. A.5 and A.6. That helps the IM3 problem, depending on the frequency spacing between the wanted signal and interferers.

The final NIS circuit block can be enabled if there is still large external interferer existing. The envelope extraction circuit block will extract the envelope of the dominant external interferer, and feed it to the NIS circuit block to partially suppress the external interferer. In this way, the influences of large interferers are largely alleviated.

4

Design Example of the Envelope Detector

4.1 Design Goal

Envelope detectors are widely used circuit blocks in modern wireless communications, where the envelope information of the signal is required. For example in smartphones, they are used with power amplifiers (PA) to reduce power consumption and improve efficiency.

In the design here, an envelope detector is used in the system architecture as shown in Fig. 3.5, which uses nonlinear transfer to suppress large interference that is generated either locally or externally. The envelope detector tracks the envelope of the interferer and adjust the nonlinear transfer accordingly for maximum suppression of the interferer, which may be a constant-envelope or amplitude-modulated interferer. As shown in Fig. B.2 and Table 3.2, the keys requirements are high accuracy and low delay, in order to enable the system to achieve maximum suppression. At the same time, it should cover a wide carrier frequency range as the NIS-based receiver targets at wideband operation. It also should be fast enough to track rapid variations of the envelope of a wideband interferer [13, 74]. So its detection bandwidth extends from 0Hz (constant-envelope interferer) up to hundreds of MHz (fast envelope-varying interferer.

Envelope detector circuits are mostly composed of a rectifier stage and a low-pass filter (LPF) stage. The LPF are placed at the output to filter out the harmonic components either at ω_{RF} or ω_{2RF}, depending on if it's a half-wave rectifier or full-wave rectifier. The choice of the LPF cutoff frequency brings a trade-off between detection speed and accuracy. A small bandwidth provides better harmonic filtering, but it allows only a low-speed detection and introduces a large delay. A large bandwidth however introduces more error due to the lack of harmonic filtering. To overcome this trade-off, a new envelope detector topology with quadrature signal generation and 2nd harmonic cancellation is proposed in the next section.

4.2 Envelope Detector Topology

The key idea behind the 2nd harmonic cancellation topology is the well-known Pythagorean identity that $sin^2\theta + cos^2\theta = 1$. However, the process that cancels the 2nd harmonic is not obvious just by looking at the equation. This will be explained as follows in Eqn. (4.1) - (4.4) and Fig. 4.1.

Let's start by assuming an input signal given by $x(t) = Acos\theta, \theta = \omega t$. This signal can be expressed as

$$Acos\omega t = \frac{A}{2}(e^{j\omega t} + e^{-j\omega t}) \tag{4.1}$$

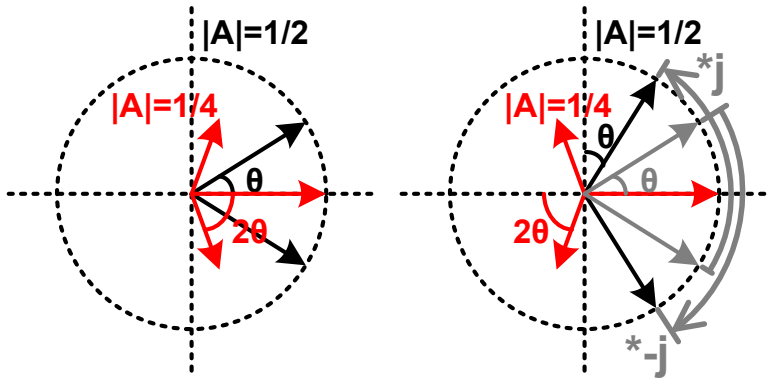

Figure 4.1.: Explanation of 2nd harmonic rejection ($sin^2\theta + cos^2\theta$) in complex plane. Left represents $cos\theta$ in black and $cos^2\theta$ in red. Right represents $cos\theta$ in grey, the transformation from $cos\theta$ to $sin\theta$ in black, and the $sin^2\theta$ in red.

By squaring the signal, we obtain

$$A^2 cos^2 \omega t = \frac{A^2}{2} + \frac{A^2}{4}(e^{j2\omega t} + e^{-j2\omega t}) \tag{4.2}$$

which contains components at DC and $\pm 2\omega t$.

The quadrature input signal can be expressed as

$$Acos(\omega t - \frac{\pi}{2}) = \frac{A}{2j}\left(e^{j\omega t} - e^{-j\omega t}\right) = Asin\omega t \tag{4.3}$$

And the quadrature square term is

$$\begin{aligned} A^2 cos^2(\omega t - \frac{\pi}{2}) &= \frac{A^2}{2} - \frac{A^2}{4}\left(e^{j2\omega t} + e^{-j2\omega t}\right) \\ &= \frac{A^2}{2} + \frac{A^2}{4}\left(e^{j(\pi+2\omega t)} + e^{(\pi - j2\omega t)}\right) = A^2 sin^2 \omega t \end{aligned} \tag{4.4}$$

After combining Eqn. (4.2) and (4.4) together, only the components at DC get added as A^2, while the components at $\pm 2\omega t$ get cancelled out. This process is also illustrated in Fig. 4.1. Only the vector at 0^o is additive, while the other vectors with 2θ to the x-axis get cancelled out.

The system diagram of the proposed envelope detector topology is shown in Fig. 4.2. The non-quadrature (I) and quadrature (Q) versions of the input RF signal are generated and passed to the square operation. The two paths are summed together before the LPF stage. Since the harmonics are cancelled out before the LPF, the filtering requirement for the LPF is relaxed. Therefore, the optimization for delay (or speed) and accuracy can be achieved at the same

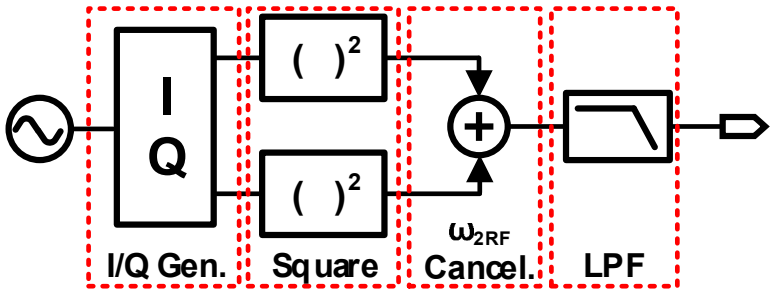

Figure 4.2.: The proposed envelope detector topology.

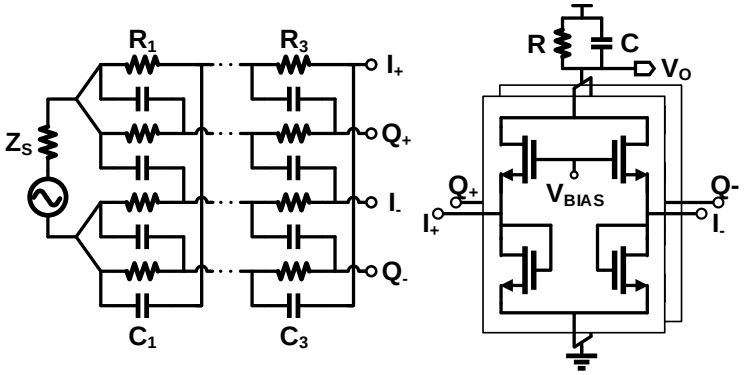

Figure 4.3.: The schematic of the proposed envelope detector topology with quadrature generation and 2nd harmonic rejection.

time. The squaring operation, or the rectifier circuit, can be designed to achieve the linearity specification.

4.3 Design and Implementation

The complete schematic of the proposed envelope detector with 2nd harmonic cancellation is shown in Fig. 4.3. The circuit consists of a Type-II polyphase filter (PPF) for I/Q signal generation, a full-wave rectifier on each path, and a RC LPF at the output.

4.3.1 Full-Wave Rectifier Circuit

The full-wave rectifier is a differential input, single-ended output circuit. The schematic is shown in Fig. B.5(a). Transistors M_2 and M_3 are biased in weak

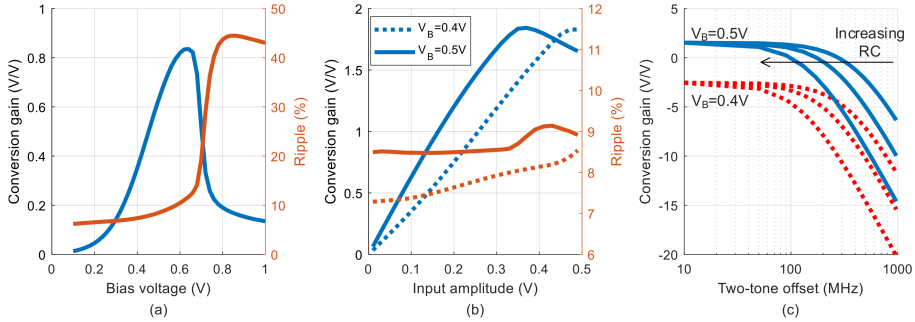

Figure 4.4.: (a) Conversion gain and ripple versus bias voltage of $M_{2,3}$ with 100mV input signal at 2GHz. (b) Conversion gain and ripple as a function of input amplitude. (c) Two-tone tests with different bias and RC settings.

inversion in order to rectify the input signal. The output is related to the 2nd order term of the power series expansion of the drain current of $M_{2,3}$ in weak inversion [75, 76], as denoted in Eqn. (B.4, B.5). Applying a single-tone $v_i^+(t) = (A/2)sin(2\pi f_{in}t)$, the output is given by

$$i_{2nd} = \frac{I_Q A^2}{8V_T^2}\left[1 + cos(2\pi(2f_{in})t)\right] \tag{4.5}$$

where $I_Q = I_0 e^{\frac{V_G - V_{th}}{nV_T}} e^{\frac{-V_S}{V_T}}$ denotes the quiescent current and V_T the thermodynamic voltage kT/q [75].

We can now define the single-tone conversion gain and ripple as

$$G_{conv}(A) = \frac{i_{2nd\,DC} \cdot R}{A} = \frac{I_Q A R}{8V_T^2} \tag{4.6}$$

$$Ripple = \frac{i_{2nd\,2\omega} \cdot H_{LPF}(\omega)}{i_{2nd\,DC} \cdot R} = \frac{H_{LPF}}{R} \tag{4.7}$$

where G_{conv} is a function of the input amplitude and ripple purely depends on the LPF transfer.

The relation of G_{conv} and Ripple versus bias point are shown in Fig. 4.4(a). For reasonable G_{conv} and small Ripple, the transistor should be biased in the weak inversion region. The relation of G_{conv} and Ripple on the input amplitude is shown in Fig. 4.4(b) for biasing voltages of 0.4V and 0.5V. The choice of the biasing voltage depends on the target dynamic range. Two-tone simulation results for detection speed are shown in Fig. 4.4(c).

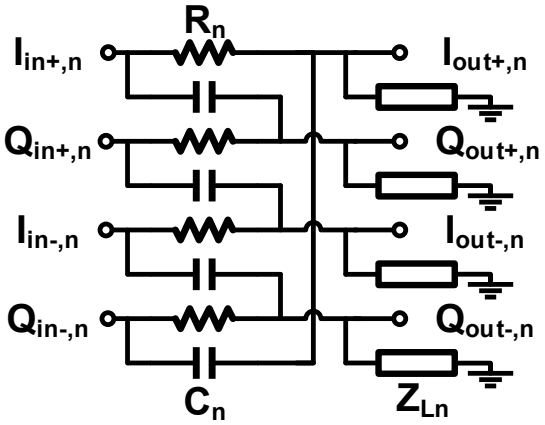

Figure 4.5.: An n^{th} PPF stage with load impedance Z_{in} of the following circuitry.

4.3.2 Quadrature Signal Generation

An n^{th} PPF stage is shown in Fig. 4.5. The difference between Type-I and Type-II PPFs is in the input configuration. Supposing Fig. 4.5 shows the first stage of the PPF, the differential inputs are connected to I_{in+} and I_{in-} in Type-I configuration. On the other hand, in Type-II configuration, each differential input is connected to both I_{in} and Q_{in}. The different input configuration also causes different output I and Q response [75]. Type-I PPFs have ideal phase balance at all frequencies and amplitude balance is unity at each RC pole frequency given by $\omega_n = 1/R_nC_n$. Type-II PPFs always have unity amplitude balance at all frequencies and the phase is 90 only at each RC pole frequencies given by $\omega_n = 1/R_nC_n$.

Fig. B.8(a)-(c) plots the frequency response of PFFs with different configurations. Type-II PPFs have less loss compared with Type-I PPFs. PPFs with unequal pole frequencies have less loss compared with equal pole frequency. Fig. B.8(c) plots the sum of squared magnitudes of the output responses, i.e., $|I|^2 + |Q|^2$. Similar conclusions are drawn that PPFs with unequal pole frequencies have bigger output responses.

In addition to loss, another parameter that is important here in the PPF design is the image rejection ratio (IRR), which will limit the ability of 2nd harmonic rejection to reduce the ripple. Fig. B.9(a) compares the IRR of a single stage PPF, a two-stage PPF with equal pole frequency ω_C and a two-stage PPF with unequal pole frequency $\omega_C = \sqrt{\omega_1\omega_2}$. The two-stage PPF has a larger bandwidth than the single-stage PPF. Furthermore, the two-stage PPF with unequal pole frequencies has larger bandwidth than that with equal pole frequency.

Combining PPF losses and IRR, we can define the ideal conversion gain

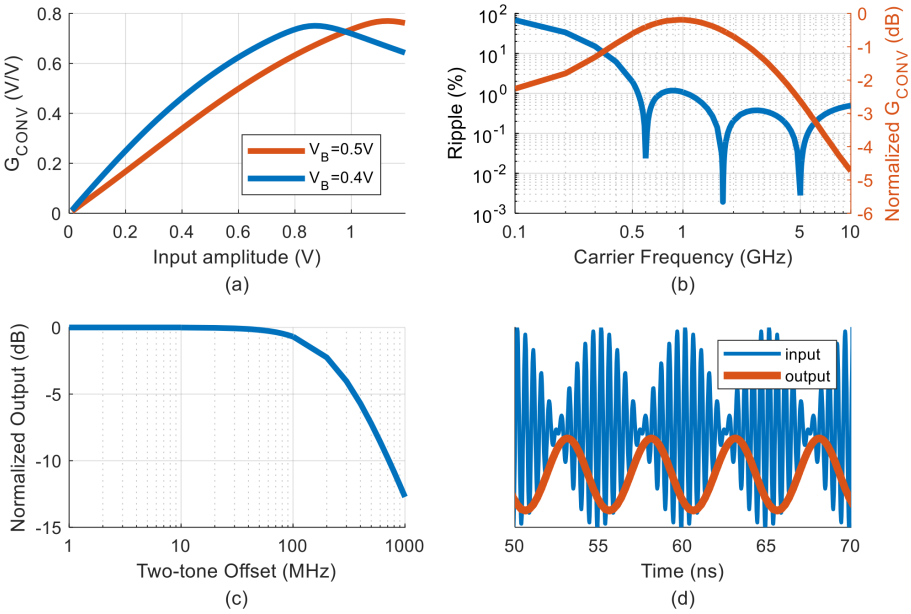

Figure 4.6.: Simulation results: (a) Conversion gain versus input amplitude with bias voltage of 0.5V and 0.4V. (b) Normalized conversion gain (red) and simulated ripple with an input voltage of 100mV (blue). (c) Simulated output magnitude (normalized) in a two-tone test. The input was 100mV for each tone. (d) Simulated input and output waveforms of the proposed envelope detector topology.

and 2nd harmonic rejection of a PPF-based envelope detector with the ideal rectifier circuit, as in Eqn. (B.8). Type-II PPF is chosen here for its smaller loss. The simulation results are shown in Fig. B.9(b)(c). The results for $HR_{2\omega}$ are similar as IRR and the results for $G_{conv,PPF}$ are the same as $I^2 + Q^2$ plotted in Fig. B.8(a)-(c) (dash yellow).

Therefore, a two-stage Type-II PPF configuration with unequal pole frequencies is desired to have a less loss and better IRR at a wider bandwidth. Also note that the actual source and load impedance will influence the PPF behavior.

4.4 Simulation Results

The proposed envelope detector was implemented in a 40nm CMOS technology. The layout is shown in Fig. B.11 with an area of 180 um by 88 um. The power consumption is 76.9 uW.

Fig. 4.6 shows the simulated results. The conversion gain over input amplitude is shown in Fig. 4.6(a). The gain compresses at 0.8V and 1V input ampli-

tude for the biasing voltage of 0.5V and 0.4V respectively, which corresponds to an input power of 8 and 10 dBm in a 50 Ohm impedance environment. Fig. 4.6(b) shows the frequency response of the ripple and conversion gain. The 3dB operating frequency reaches 6GHz. The ripple is below 2% starting from 500MHz. Fig. 4.6(c) shows a detection bandwidth of around 250MHz, set by the LPF bandwidth. Fig. 4.6(d) shows the time-domain waveform of the input and output signal. The input is a two-tone signal at 2GHz with each amplitude of 200mV and a spacing of 200MHz. The simulated delay is 0.64ns.

4.5 Conclusions

An envelope detector was designed in a 40nm CMOS technology. Based on quadrature signal generation and 2nd harmonic cancellation, the circuit achieves 2% ripple from 500MHz to 6GHz and only 0.64ns delay for a two-tone signal with 200MHz spacing. The detector consumes 76.9 uW from a 1.1V power supply. By employing it in the NIS receiver, more than 25 dB of interference suppression can be achieved.

5

Design Example of the Receiver with Nonlinear Interference Suppression

5.1 Design Goal

The idea of nonlinear interference suppression and the mathematic analysis have been presented in Chapter 3. In this chapter, we will be focusing on the implementation of the nonlinear interference suppression idea in a wideband receiver design. The design goals of this chip are as follows:

The first goal is to compare the receiver performance in linear mode operation and nonlinear mode operation when a strong blocker is present. As discussed previously, in the presence of a strong blocker, a linear receiver needs to increase the power consumption so that the dynamic range is increased to tolerate the blocker while maintaining the receiver performance such as NF, SIR, etc. However, in this design, the strong blocker is suppressed by using a nonlinear transfer function at the RF stage. Since the blocker is removed at an early stage of the receiver, we shall see how this technique improves the receiver performance while avoids sacrificing power efficiency.

The second goal is to provide good blocker suppression and receiver linearity even if the blocker is located close in frequency or even in channel. As discussed in the literature review in Chapter 3, the approaches using frequency domain filtering have the limitation of the offset frequency between the blocker and the wanted signal. As the idea of nonlinear interference suppression enables filtering in the amplitude domain, the idea is inherently frequency-independent. Therefore it could provide good receiver performance independent of the blocker frequency.

The third goal is to improve the implementation and performance of the circuit blocks based on the NIS idea. One previous prototype based on this NIS idea was proposed in [6] to deal with locally generated TX self interference. It achieves more than 30dB suppression to a 0-11dBm blocker and consumes 7-35mW. In this paper, we present a new wideband receiver with the NIS technique implemented at the RF stage. It improves the amount of blocker suppression over a larger power range while consuming less power.

5.2 Design of NIS Transconductance Amplifier

5.2.1 Schematic

The requirement and behavior of the nonlinear transfer function for simultaneous interference suppression and simultaneous amplification of the weak desired signal have been analysed in Chapter 3. In order to create such nonlinear transfer functions, we can make use of multiple differential pairs either in series, parallel or hybrid connection.

For a differential pair with a bias voltage offset of $2V_C$ as shown in Fig. 5.1(a), its V-I input-output transfer function is shifted along the x-axis towards negative input values by $2V_C$. A Gilbert-cell combining structure is shown in

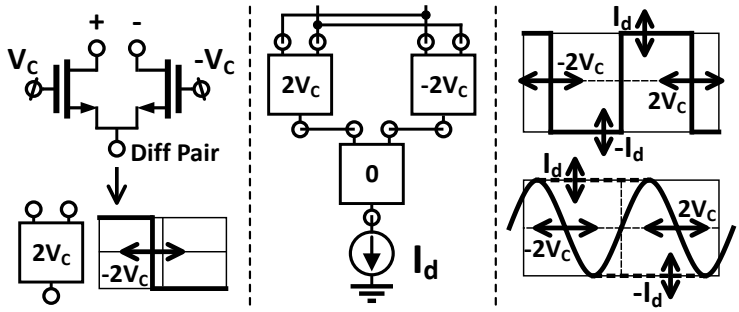

Figure 5.1.: (a) Differential pair with a bias voltage offset of $2V_C$ and its V-I transfer function, (b) Gilbert-cell structure of combining three differential pair with bias voltage offset of 0, $2V_C$ and $-2V_C$, (c) the created nonlinear transfer in ideal (top) and implementation (bottom).

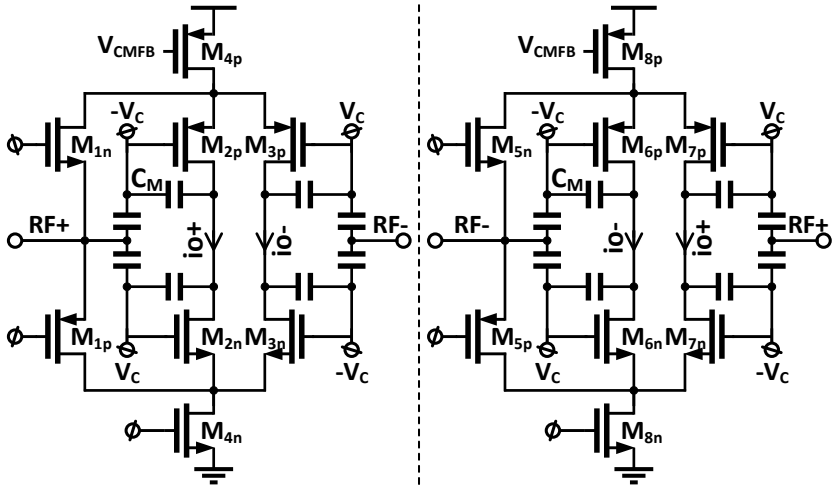

Figure 5.2.: Schematic of the proposed NIS transconductance amplifier.

Fig. 5.1(b) with three differential pairs with bias offset of 0, $2V_C$ and $-2V_C$, respectively, and a tail current source I_d. Its transfer function is shown in Fig. 5.1(c) for the ideal case and for real implementation. The nonlinear transfer can be adjusted by both V_C and I_d.

The proposed NIS transconductance amplifier is shown in Fig. 5.2, using a differential and complementary folded Gilbert-cell structure. The CG transistors M_{1p}, M_{1n} form the first differential pair with no bias offset. The second and third differential pairs are composed of M_{2p}, M_{3p} and M_{2n}, M_{3n}, with a bias offset of $-2V_C$ and $2V_C$, respectively. M_{4p}, M_{4n} are variable current

sources. Transistors M_{5-8} make up the other differential part of the circuit. Capacitor C_M is used to compensate the pole introduced at the drain of the current sources to maximize suppression. In nonlinear mode, V_C and I_d are updated according to the blocker power. In linear mode, V_C is set negative so that the out-of-phase branches, M_{2p} and M_{6p}, are switched off.

In [6], the NIS circuit is realized by combining the outputs of a linear amplifier and a clipping amplifier. The current of the clipping amplifier is adjusted according to the instantaneous interferer amplitude. Compared with [6], the proposed circuit has three advantages. Firstly, the power consumption under different blocker power is well defined by the current source I_d. Secondly, there are two degrees of freedom, V_C and I_d, in the circuit. It helps to achieve an optimum performance between suppression and noise figure for different blocker power. Thirdly, there is no need to create two amplified copies of interferer that are then cancelled out. This makes the circuit more power-efficient and allows for a lower noise figure.

5.2.2 Nonlinear Transfer and Equivalent G_{LS},G_{SS}

An example of the nonlinear transfer and its derivative is shown in Fig. 5.3 (a)(b) with setting I_d=4mA and V_C=170mV. The zero crossings are at 0 and around $\pm 2V_C$. The center region of the transfer is determined by the CG devices and the regions around $\pm 2V_C$ are determined by the differential pairs. The equivalent G_{LS}, and G_{SS} are calculated using Eqn. (3.1) and (3.2) and the results over A_{LS} are shown in Fig. 5.3(c).

For very small A_{LS}, the circuit operates in the CG region. In this region of operation, G_{LS} and G_{SS} are the same and are determined by the g_m of the CG devices. When the interference amplitude starts to increase, the circuit enters the nonlinear region of operation and G_{LS}, G_{SS} start to behave differently. According to Eqn. (3.1), G_{LS}=0 happens when the integral over the CG region and the diff-pair regions equal to zero. This happens at $A_{LS} = 385mV$ in Fig. 5.3(c). For $A_{LS} > 385mV$, G_{LS} increases again as the integral result is now more dominant by the differential-pair region.

On the other hand, according to Eqn. (3.2), G_{SS} is related to the convolution of the output transconductance Gm_{NIS} and the PDF of the large signal within $[-A_{LS}, A_{LS}]$. Thus G_{SS} is largely dependent on the Gm_{NIS} around $\pm A_{LS}$. As shown in Fig. 5.3(c), G_{SS} first decreases faster than G_{LS}, then follows the change of Gm_{NIS} in the differential-pair region. Therefore, the behavior of the differential-pair decides the equivalent gain for the small signal G_{SS} and blocker 1dB compression point B_{1dB}. For this particular transfer function, maximum suppression happens at a blocker amplitude $A_{LS} = 385mV$ and the small signal transconductance gain G_{SS} is 15mS.

Here the nonlinear transfer function and the analysis on G_{LS} and G_{SS} is only shown for one setting on I_d and V_C. As discussed, the nonlinear transfer can

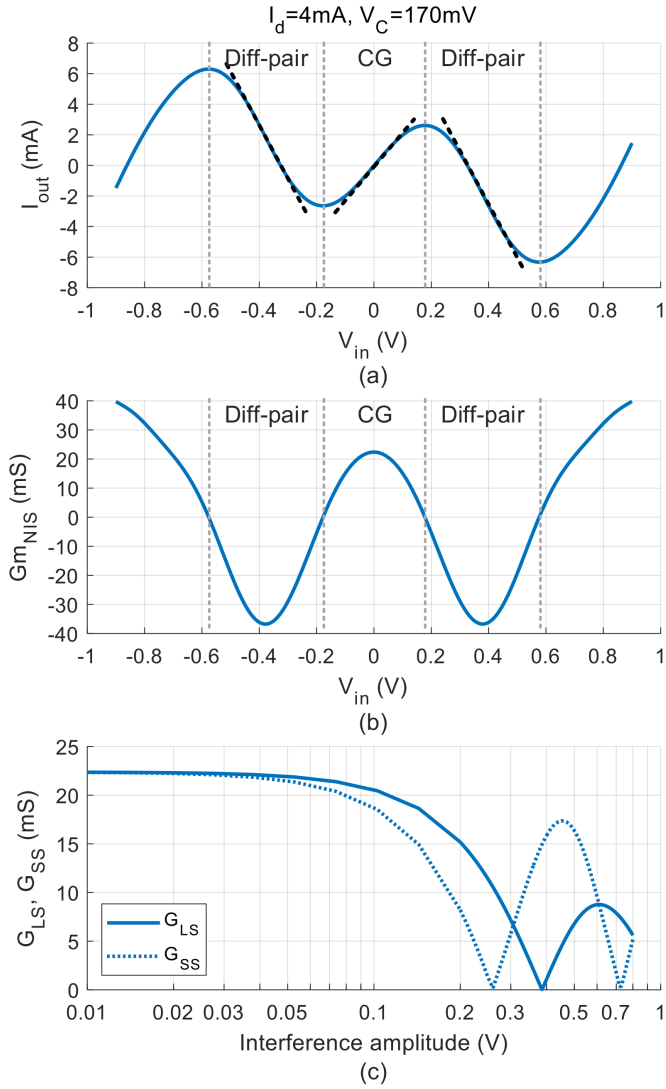

Figure 5.3.: (a) The V-I transfer function with I_d=4mA and V_C=170mV, (b) the derivative, Gm_{NIS}, of the transfer function, (c) G_{LS} and G_{SS} as a function of the interference amplitude A_{LS}.

be adjusted by different settings of I_d and V_C in order to achieve suppression on different blocker power. For more details on the reconfigurability of the nonlinear transfer and the corresponding analysis on G_{LS} and G_{SS}, the reader is referred to Paper D.

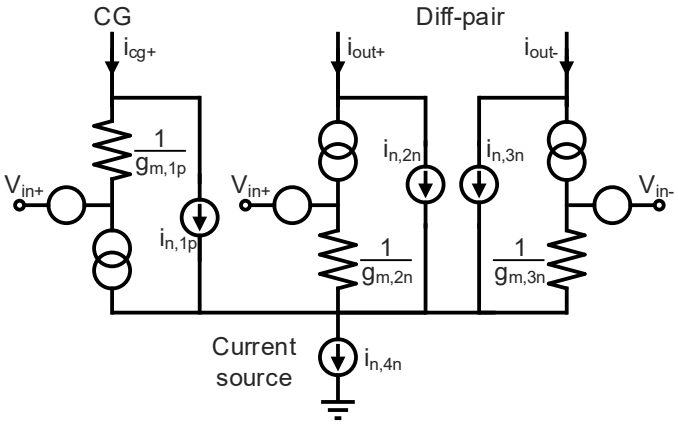

Figure 5.4.: The 1/4 schematic with noise sources of CG, diff-pair and current sources.

5.2.3 Noise Figure

In the presence of a large blocker, the transconductance of the CG and differential pair devices are changing periodically. Therefore, we must use Fourier analysis to analyze the noise contribution from each noise source within a period of the large blocker. Fig. 5.4 shows the different noise sources from a quarter of the schematic, namely $i_{n_{1p}}$, $i_{n_{2n}}$, $i_{n_{3n}}$, $i_{n_{4n}}$. Besides, there is also noise from the source, $i_{n_{SRC}}$.

The noise transfer from each noise sources to the output is described in Paper D in details. Here we focus on the final result of the modeled noise power from each noise source and the overall noise figure when a blocker is present. An example of the nonlinear transfer and its derivative is shown in Fig. 5.5 (a)(b) with setting I_d=4mA and V_C=200mV. The current output noise power from different noise sources are shown in Fig. 5.5(c).

From Fig. 5.5(c), the two big contributors are the noise power due to the current sources and CG devices. This is because unlike the noise of differential pair, the noise due to the current sources and CG devices directly appears at one of the outputs for a large part of the period. The g_m of the CG devices are also limited by the input matching requirement. The gm of current sources are relatively big due to the limited voltage headroom. The noise power of the source considering spectrum mirroring basically follows the change of $G_{m_{NIS}}$ and has two notches. Each notch happens at the position shortly after $G_{m_{NIS}}$ changes sign.

The noise factor is equal to total noise at the output divided by the noise at the output due to the source considering spectrum mirroring, as expressed in

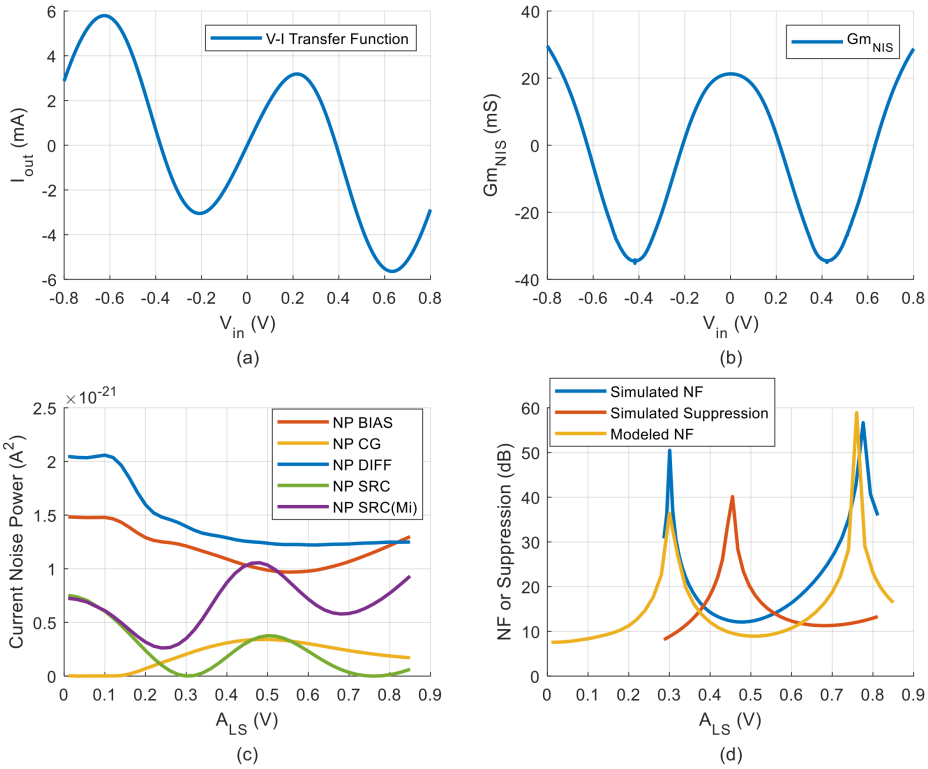

Figure 5.5.: (a) The V-I transfer function with Id=4mA and Vc=200mV, (b) its derivative Gm_{NIS}, (c) the current noise power from each noise sources, (d) comparison between modeled NF and simulated NF, and simulated blocker suppression..

Eqn. (5.1).

$$F_{NIS} = \frac{NP_{circuit}}{NP_{src,mirror}} \tag{5.1}$$

The modeled NF using Eqn. (5.1) is compared with the simulated NF and shown in Fig. 5.5(d), along with the simulated blocker suppression. The modeled NF and simulated NF are matched quite well. They both have two peaks at the A_{LS} where the noise power due to the source, NP_{src}, is equal to zero. The minimum noise figure is achieved when NP_{src} is at its peak value, which is in the diff-pair region. Therefore for noise consideration, it is desirable to extend the diff-pair region so that the two NF peaks are further away. Thus a smaller NF can be achieved over a wider range of A_{LS}. This can be tuned by changing the bias voltage at the gate of the diff-pairs at the cost of smaller G_{SS}.

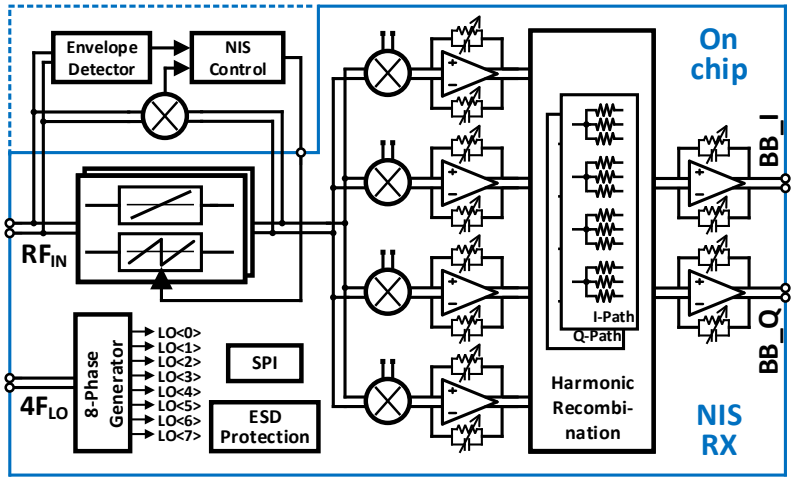

Figure 5.6.: The system diagram of the proposed NIS-based receiver.

In Fig. 5.5(d), there's still a gap between modeled NF and simulated NF. There are several possible reasons. Firstly, it can be the noise coefficient γ between modelling and simulation. $\gamma = 1.5$ is used in modeling. Secondly, the noise sources in the modeled NF only cover channel noise, while it does not cover other noise sources such as gate, source or drain resistance, or flicker noise. The diff pair is excited by a large blocker similarly to the operation of a mixer or an oscillator. The flicker noise of the current sources will be upconverted to the blocker frequency ω_{LS}, which can be very close to ω_{SS}. Unlike in oscillator designs, a capacitor to ground is not appropriate here as a high impedance node is desired.

5.3 Complete Receiver

5.3.1 Receiver Topology

The block diagram of the proposed NIS-based receiver is shown in Fig. 5.6. The on-chip part consists of the RF signal path and the LO path, while the NIS control path is placed off-chip. The signal path uses current-mode circuit to maximize large signal linearity. The RF stage is an NIS-based transconductance amplifier that has two operation modes. In linear mode, it is operated as an amplifier. The nonlinear mode is enabled when a strong blocker is present, and the circuit will then perform simultaneous frequency independent blocker suppression and weak signal amplification. The circuit is designed for wideband operation. It suppresses large blockers that fall in the bandwidth from 0.5GHz to 3GHz, independent of the offset frequency between the blocker and the wanted signal.

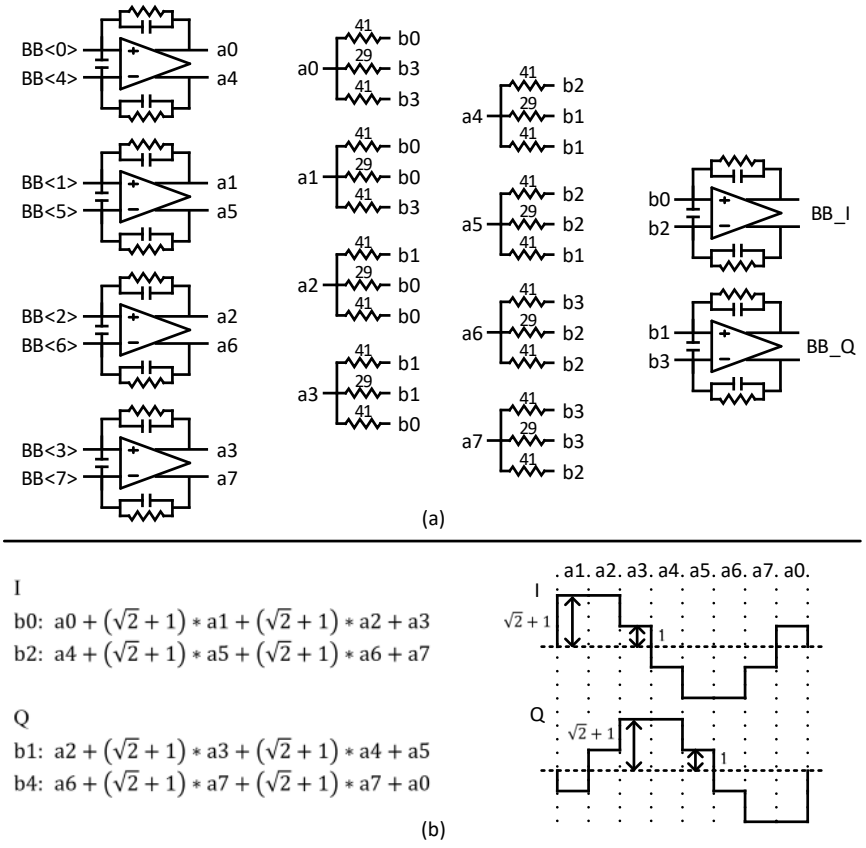

Figure 5.7.: (a) Diagram of the baseband TIA and resistive harmonic recombination circuit, (b) the equivalent LO waveform to cancel 3rd and 5th harmonic.

5.3.2 Clock Generation and Harmonic Rejection

As a result of the nonlinear transfer, the output signal contains strong 3rd and 5th harmonics. An 8-phase passive mixer with 12.5% duty cycle clock is used here to avoid downconversion of the 3rd and 5th harmonic. The 12.5% duty cycle LO signals are created by performing AND function on three 50% duty cycle waveforms at $4f_{LO}$, $2f_{LO}$ and f_{LO} [77]. The dynamic power consumption at $f_{LO} = 1.5GHz$ is 12mW. The divide-by-4 circuit works up to 11GHz input frequency and achieves -155dBc/Hz at 20MHz offset. Note this phase noise will degrade the blocker NF for a receiver with little filtering capability.

The baseband harmonic recombination circuit is shown in Fig. 5.7, by using resistive networks with a ratio of 41:29:41 to mimic the weighting ratio of $1 : \sqrt{2} : 1$. In order to alleviate the influence by resistor mismatch to the accuracy of weighting factors, the outputs of the first TIA are connected to

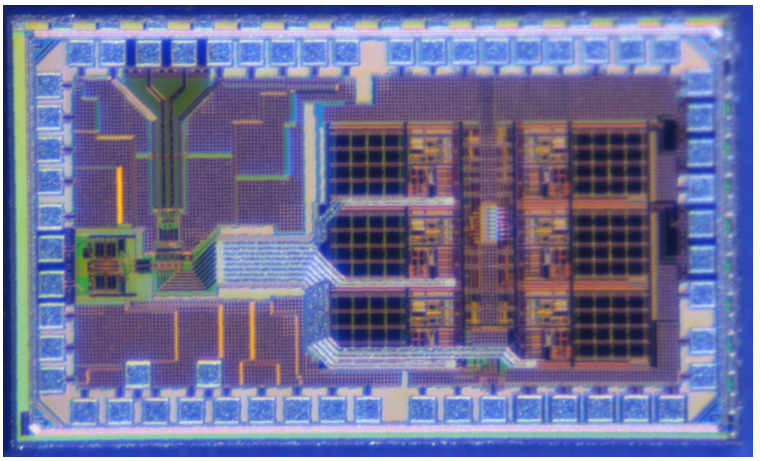

Figure 5.8.: Die photo.

multiple paths to average out the mismatch between different resistors. They are summed up at the input of the second TIA to achieve harmonic rejection.

5.4 Measurement Results

In this section, we will mainly focus on the performance of the NIS-based RX when the strong blocker is present at the input. We shall see how the nonlinear mode operation helps improve receiver linearity, noise figure and SIR compared with traditional linear mode operation. The proposed NIS-based Receiver was implemented in a 40nm CMOS technology. The die photo is shown in Fig. 5.8. The total area is $1.67mm^2$ including bonding pads. The dynamic power consumption of the divider is 12mW at 1.5GHz LO frequency. The baseband TIAs consumes 16.2mW from a 1.1V supply.

5.4.1 Nonlinear Mode G_{LS} and G_{SS}

Fig. 5.9 shows the measured G_{LS} and G_{SS} for different nonlinear transfer settings. The frequency setup for the LO, blocker and small signal are 2GHz, 2.01GHz and 2.0001GHz, respectively. The measured results are very similar to the simulation results shown in Fig. 5.3. Fig. 5.9(a) shows the notch filter behavior on the amplitude domain, at blocker power of 0.2dBm and 3.9dBm. Fig. 5.9(b) shows the small signal gain as a function of blocker power. Fig. 5.9(c) shows the 1dB compression point P1dB with blocker present is around -16dBm or +8.7dBm OP1dB. The P1dB is mostly set by the nonlinear transfer and TIA output swing.

For a linear receiver, we use OP_{1dB}/P_{DC} as a figure-of-merit to characterize

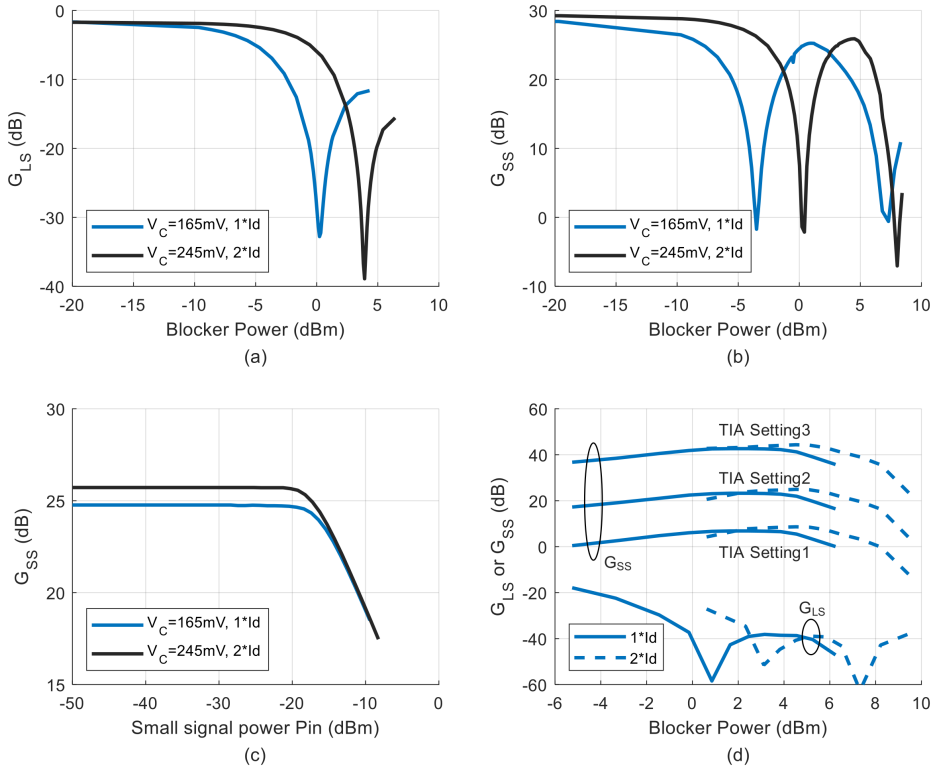

Figure 5.9.: Measured (a) blocker suppression G_{LS} and (b) mall signal gain at different Vc and Id. (c) small signal gain G_{SS} over small signal input power, measured under the blocker power at min G_{LS} in (a). (d) measured blocker suppression G_{LS} by RF NIS block and the small signal conversion gain G_{SS} with the blocker at 10MHz offset.

linearity over power efficiency. For the nonlinear mode, we can use a virtual OP_{1dB} that equals $P_{blocker} \cdot G_{SS}$, which is what a linear receiver needs when the blocker is present. This FOM would be smaller than 1 in a linear receiver but could be higher than 1 in this nonlinear receiver. In this work, this FOM is -2dB in linear mode and 11dB/14.6dB in nonlinear mode as shown in Fig. 5.9.

Fig. 5.9(d) summarizes G_{LS} and G_{SS} over different V_C and I_d settings. The measured blocker suppression is more than 38dB for blocker power within [0, 9.6] dBm, or more than 20dB for blocker power within [-4.4, 9.6] dBm. The NIS block power consumption is 8.7mW at low current setting (1*Id) or 15.7mW at high current setting (2*Id).

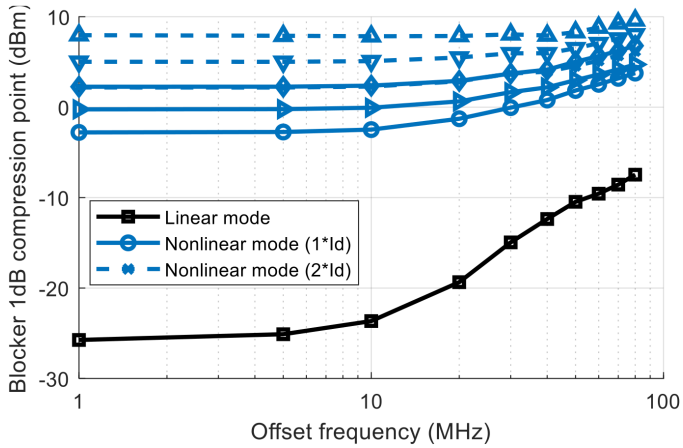

Figure 5.10.: Measured Blocker 1dB compression point (B_{1dB}) with TIA setting2.

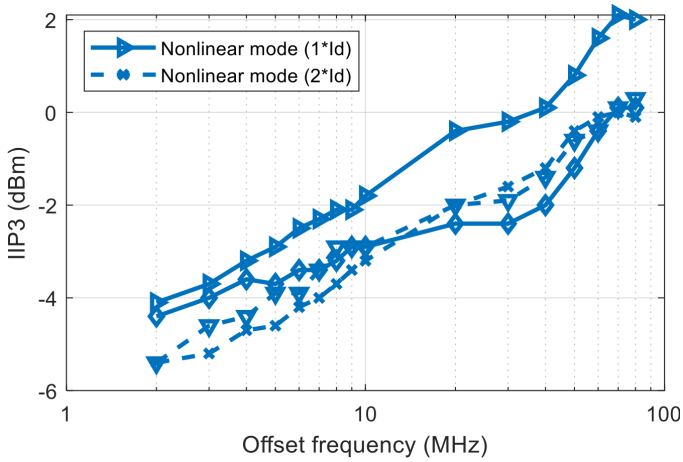

Figure 5.11.: Measured IB-IIP3 in nonlinear mode over the blocker offset frequency.

5.4.2 Linearity Improvement

Fig. 5.10 shows the measured blocker 1dB compression point (B_{1dB}) in linear mode and nonlinear mode over the blocker offset frequency, using TIA setting 2. In linear mode, the IB-B1dB at 1MHz offset is -25.7dBm. The OB-B1dB at 80MHz offset improves to -7.5dBm as a result of baseband filtering. In nonlinear mode, the IB-B1dB at 1MHz offset ranges from -2.8 to 8 dBm for different settings. The OB-B1dB at 80MHz offset ranges from 4.6 to 9.6 dBm. Compared with linear mode operation, the IB-B1dB in nonlinear mode improves around 30dB as a result of the frequency-independent blocker suppression by the NIS

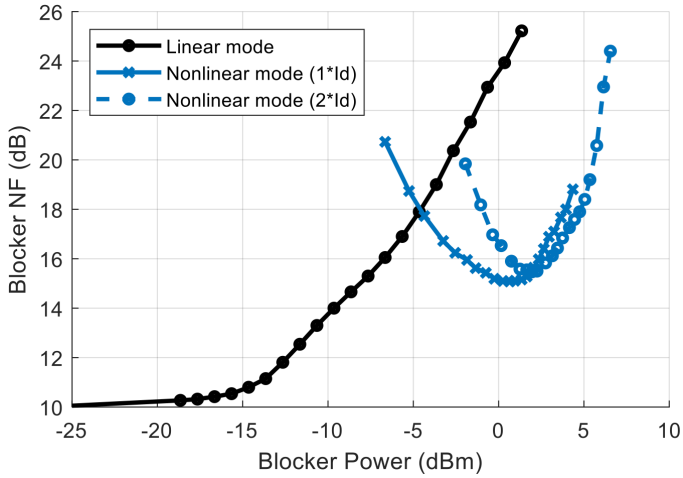

Figure 5.12.: Measured blocker NF over blocker power in linear mode and nonlinear mode.

block.

Fig. 5.11 shows the IB-IIP3 measurement results over blocker offset in nonlinear mode at different V_C and I_d settings. The IIP3 test here is different: besides the two small tones, the strong blocker is also present at the input. The blocker power is as noted in Fig. 5.9(d) for different V_C and I_d settings. The measurement was made with LO=1.5GHz, 1st tone at 1.501GHz and 2nd tone at 1.5012GHz so that IM3 falls in-band at 800kHz. The blocker offset is swept from 2MHz to 80MHz. The measured IB-IIP3 is around -4dBm with a strong blocker at 2MHz and 2dBm with the strong blocker at 90MHz. These results suggest that with large amount of blocker suppression, the circuit operates linearly for the small signal. As the blocker suppression is frequency-independent, the IB-IIP3 variation over blocker offset is small.

5.4.3 Noise Figure

Fig. 5.12 shows the measured blocker noise figure with the blocker located at 51MHz offset. Note the simulated divider phase noise is -155dBc/Hz at 20MHz offset at 2GHz. In linear mode, the noise figure degrades quickly with increasing blocker power. In nonlinear mode, the noise figure is measured at different V_C and I_d settings to cover the blocker power range. For blocker power larger than -4.3dBm, the noise figure is smaller than the noise figure in linear mode. Because of the blocker suppression, the noise figure is determined by the NIS block and degradation due to reciprocal mixing is reduced. The blocker noise figure is 15.1dB or 15.5dB under a 0.65dBm or 1.95dBm, respectively.

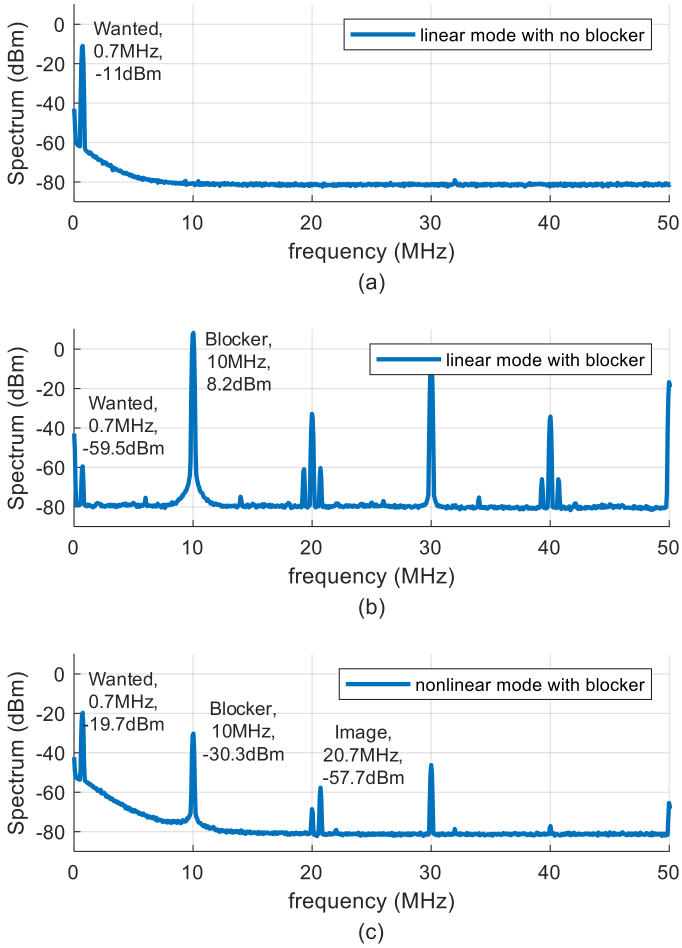

Figure 5.13.: The measured down-converted output spectrum (a) with a -54dBm input small signal in linear mode, (b) with a 5.3dBm blocker at 10.7MHz offset in linear mode, (c) with the blocker in nonlinear mode.

This nonlinear receiver can be placed after an external LNA to reduce NF in applications where blocker power larger than 0dBm will not be encountered. Assuming an LNA of 3dB noise figure and 10dB gain, the receiver will have a total NF of 4.6dB in linear mode and 8.4dB in nonlinear mode with the presence of a -9.35dBm blocker power at 51MHz offset.

5.4.4 SIR Improvement

Fig. 5.13 shows the signal-to-interference ratio (SIR) comparison in linear mode and nonlinear mode. The measurement was made with LO at 1.5GHz,

a 5.3dBm blocker at 1.49GHz and a -54dBm wanted signal at 1.5007GHz. The RF circuit consumes 14mW in linear mode and 8.7mW in nonlinear mode.

In Fig. 5.13(a) without the blocker, the linear circuit provides 43dB gain and the small signal output is at -11dBm. In Fig. 5.13(b) with the blocker, the receiver in linear mode is saturated by the large blocker. The blocker output is 8.2dBm. The small signal is attenuated by 5.5dB, at -59.5dBm. The SIR is around -68dB. The baseband harmonics are clearly seen in the spectrum. In nonlinear mode as in Fig. 5.13(c), compared with linear mode, the blocker is suppressed by 38.5 dB. At the same time, the small signal is amplified by 40dB. The SIR is now +10.5dB. Therefore 78.5dB SIR improvement is achieved with even less power consumption.

5.4.5 Comparison to State-of-the-Art

Table 5.1 summarizes and compares the performance with other recently published wideband blocker-resilient receivers. Compared with [6], the frequency-independent blocker suppression is improved to more than 38dB for block power from 0dBm to 9.6dBm. For blocker NF, the result in this work is comparable with the result in [29] with PNC on, while consuming less power consumption. This work offers the best receiver performance when a strong blocker is present. In nonlinear mode, the receiver achieves more than 13dB OP_{1dB}/P_{DC} improvement, more than 30dB B_{1dB} improvement, and 78.5dB SIR improvement compared with in linear mode when the blocker is present.

5.5 Conclusion

A new wideband blocker-resilient receiver is introduced that utilizes nonlinear transfer function for simultaneous blocker suppression and weak signal amplification. This technique suppresses the strong blocker in the amplitude domain, independent of the offset frequency between the blocker and the wanted signal. Accordingly, it breaks the trade-off between blocker offset and receiver performance such as linearity, blocker NF, SIR and power consumption.

A prototype has been fabricated in a 40nm CMOS technology. More than 38dB blocker suppression is achieved for blocker power from 0 to 9.6dBm. 78.5dB SIR improvement with no extra power consumption under a 5.3dBm blocker is achieved in nonlinear mode operation compared with conventional linear mode operation.

Table 5.1.: Comparison with Other State-of-the-Art Blocker-Resilient Receivers

		JSSC'18 [45]	JSSC'12 [78]	JSSC'11 [51]	ESSCIRC'17 [68]	ISSCC'15 [29]	RFIC'12 [6]		This work	
Topology		Mixer-First	Noise Cancelling	LNA + N-Path Mixer	Adaptive Filter	Phase and Noise Cancelling	RF NIS		RF NIS + N-Path Mixer	
LO Generation		External	External	Integrated	Integrated	Integrated	N.A.		External	
CMOS Technology		45nm SOI	40nm	40nm	40nm	28nm	0.18um		40nm	
RF Frequency (GHz)		0.2 - 8	0.08 - 2.7	0.4 - 6	1.7 - 2.2	0.2 - 3	1.85		0.5 - 2.7	
Blocker suppression (dB) / Blocker power (dBm)		N.A.	N.A.	N.A.	N.A.	N.A.	30 / (0 $\sim$ 11dBm) 20 / ($-3 \sim$ 11dBm)		38 / (0 $\sim$ 9.6dBm) 20 / ($-4.4 \sim$ 9.6dBm)	
Blocker NF (dB), 0dBm blocker, $\Delta f = 80MHz$	Ideal LO, -174 dBc/Hz	4.7	4.1	13 (Δf=20MHz)	N.A.	5.5	12.8 $P_{blocker}$=2dBm		NL mode: 15.1 (0.65dBm) 15.47 (1.95dBm) (-155dBc/Hz @20MHz**)	
	Non-ideal LO, -141 dBc/Hz	32*			N.A.	32 (PNC off) 13.5 (PNC on)	N.A.			
Gain (dB)		22	70	70	20 - 36	60	17(L), 9.4(NL)		17 - 53	
IF BW (MHz		20	N.A.	0.5 - 30	N.A.	N.A.	N.A.		1 - 27	
Mode		N.A.					Linear	Nonlinear	Linear	Nonlinear
OB-B1dB (dBm) @100MHz		12.5	-0.5	N.A.	N.A.	-2.5	-1.9	N.A.	-7.5	4.6 $\sim$ 9.6
IB-B1dB (dBm) @1MHz		-10	-6 @30MHz	-20 @20MHz	3	N.A.			-25.7	$-2.8 \sim 8$
IB-IIP3 (dBm) @1MHz		5	-2.5	6	N.A.	N.A.	6.6	> 4	N.A.	$-4 \sim 2$***
OP_{1dB} / P_{DC} (dB)		N.A.	N.A.	N.A.	N.A.	N.A.	-6.7	4.6#	-2	14.6#
SIR improvement (dB) nonlinear vs. linear mode		N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	+78.5 $P_{blocker}$=5.3dBm
Power (mW)		56 - 290	32 (ex. LO)	30 - 55 (ex. PLL)	11 (RF) 11.5 (canceller)	12 (RF), 23 (BB) 11 (PNC)	3 (RF)	7 - 35 (RF)	14 (RF)	8.7 $\sim$ 15.7 (RF)
									16 (BB)	

*Estimated and/or interpreted form plots, figures and/or reported numbers. Summarized in [29].

**Post-layout simulation results of on-chip divider-by-4 at 20MHz offset.

***The setup of the IIP3 test here includes a strong blocker at the input besides two small tones.

#In nonlinear mode, virtual OP_{1dB} / P_{DC} = $P_{blocker} \cdot G_{SS}/P_{DC}$.

6

Conclusions

6.1 Conclusions

The key conclusions from this thesis are summarized as the following:

1) The limitation that was found in the NIS circuit implementation in [6] for power dissipation vs. P1dB was not fundamental.

2) By using circuit topologies that avoid this non-fundamental limitation, a very large improvement over previous state-of-the-art can be achieved.

3) The limitation of previous work in [6, 73] that only deals with self-generated blockers is not fundamental and the advantages of NIS can therefore be extended to deal with external interferers and blockers.

4) The NF performance of NIS can be strongly improved by a preceding LNA but noise folding seems to be a fundamental limitation resulting in a NF > 3 independent of preceding gain.

5) NIS can provide filtering for signals that are so close or even overlapping in the frequency domain that frequency selectivity is not possible or practical.

6) NIS is orthogonal to frequency selectivity and therefore a combination of frequency selectivity (such as N-path) with NIS would offer even better and more universal robustness against interferers and blockers.

7) The NF degradation due to reciprocal mixing is alleviated with NIS implemented before the mixer. No extra circuit or power dissipation is needed for LO phase noise improvement or cancellation.

6.2 Recommendations for Future Work

The NIS receiver circuitry can be further optimized for better NF performance. Firstly, the linear mode NF is on the high side as the circuit is not optimized for linear mode operation. We could completely bypass the NIS if there's no strong interferer. Secondly, we see a lot of noise contribution from the input CG transistors and current sources in nonlinear mode operation. This is limited by input matching of the CG devices and the limited voltage headroom for the current mirrors. Potentially other circuit techniques can be investigated to improve the NF, such as using CS rather than CG input configuration or other noise reduction techniques. Thirdly, as shown in Fig. 5.5, there is some discrepancy in noise figure over blocker amplitude between modeling and simulation results. Further investigation could be made to check the hypotheses in modeling, simulation of transfer function, etc.

In order to show the reduction on the effect of reciprocal mixing in the NIS receiver, a /4 divider is implemented on-chip to mimic a realistic phase noise

performance from a real synthesizer. However, it would be more convincing if the synthesizer, or at least the oscillator, is implemented on-chip. A second prototype has actually been made with an on-chip oscillator, however due to unexpected chip bonding issues, the complete performance characterization is unfortunately unavailable. Another recommendation could be to fix the bonding issue and evaluate the complete chip performance.

The envelope extraction path has not been integrated on this NIS receiver prototype. If this loop can be closed on the chip, or on the PCB, it would be great for the demonstration of suppression to a modulated interferer, also as a stand-alone module. However, some additional digital signal processing hardware and algorithm would be required. Once this path is established, it would be also interesting to see how its accuracy and speed would affect the amount of suppression to interferers with different modulation and bandwidth.

While this work mainly focused on the receiver implementation, there are other interesting aspects to explore on the higher level of the system. One thing is the inversion of the spectrum mirroring side-effect from the NIS concept, which could lower the NF by 3dB. Another thing is to develop an automated algorithm to auto switch from linear mode and nonlinear mode operation based on the envelope amplitude extracted at the antenna. As long as the extracted amplitude is small, there is no strong interferer present and the system can work in linear mode with low NF. When a large amplitude is extracted, the system switches to nonlinear mode automatically. It could also be challenging to extend this algorithm to work in a scenario with multiple strong interferers.

II Papers

A

A Nonlinear Transfer Function Based Receiver for Wideband Interference Suppression

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Abstract - Wideband receivers for multi-standards operation can simplify the system and lower the cost. In a wideband receiver, the tolerance of large interference signal within the operating band is important. Traditional frequency domain filtering suffers from lacking of filtering capability for in-band interference signals. This paper describes a receiver system exploiting nonlinear transfer function. Based on the fundamental nonlinear theory, the receiver with nonlinear method can provide frequency-independent filtering for large blockers and linear amplification for weak desired signals simultaneously. The interference suppression performance depends on the amplitude discrimination between the envelope of the large and small signal. The operation of the nonlinear receiver is based on the amplitude of the interferer envelope. A feedforward path is designed to extract the envelope information of the interferer and a feedback path is added to keep track of the environment. With frequency-independent filtering, the nonlinear receiver system enhances both in-band and out-of-band linearity, thus enabling wideband multi-mode operation.

A.1 Introduction

Wireless communication systems are developing to provide higher speed with reliability under the increasing amount of daily usage [7]. In a mobile handset device, several wireless communication standards are supported, such as 2G/3G/4G, Bluetooth, Wifi, GPS, NFC etc [79]. In general there are two solutions for multiple standards operation. One is narrowband solution and another is wideband solution. In the narrowband solution, multiple narrowband receiver front-ends and off-chip surface-acoustic-wave (SAW) filters are required. In the wideband solution, a single wideband receiver covers the spectrum of interest. The wideband solution is widely applied in the design of software-defined radios (SDR) [25–28, 80, 81] and reconfigurable receivers [20–23]. However, the wideband operation introduces wideband interference problems. The interference comes from the simultaneous operation of multiple radios with multiple standards. The transmitted signal generates interference through the poor isolation between transmitter and receiver in the same device. Also, the transmitted signal generates interference for other devices if they have active receivers operating at the same time.

The multi-radio coexistence scenario [82, 83] is shown in Fig. A.1. In Fig. A.1, there are three wireless terminals. Terminal #1 is a multi-radio device. Terminal #M and terminal #N are single-radio devices. Terminal #1 has both a receiver and a transmitter. The receiver in terminal #1 is receiving information with wireless standard A, while the transmitter in terminal #1 is transmitting with wireless standard B. Terminal #M and terminal #N are transmitting information through wireless standard M and N, respectively. In this case, the receiver in terminal #1 is plagued by the transmitting signal from either the transmitter in terminal #1, terminal #M, or terminal #N. In this scenario, the term 'victim' is used for the receiver in terminal #1, and the term 'aggressor' for transmitters in terminal #1, terminal #M and terminal #N. The input spectrum at the receiver antenna in terminal #1 is shown accordingly. Due to the difference of wireless standards and coupling paths, the interference signals received at the receiver antenna are different in frequencies and power. The interference signal from the collocated transmitter in the same device (Terminal #1) is usually much stronger because of the small size of a handset device.

The lack of RF filtering after antenna generates problems for wideband operation. The problems can be divided into three categories: distortion, phase noise and power consumption. It can be extremely harmful if the strong interferer is located close to the desired signal, or at harmonic frequency of the desired signal. Firstly, if the interferer is too large, it leads to desensitization of the receiver. Secondly, when the interferer mixes with LO phase noise, it poses additional noise in the receiver band. That noise is proportional to the interferer power [28, 81]. The receiver's blocker NF under reciprocal mixing can be expressed as:

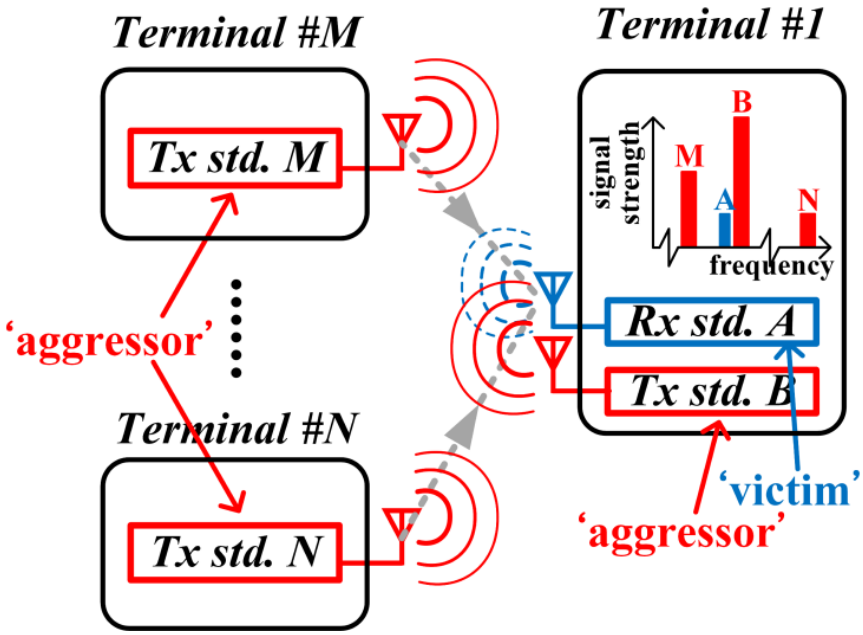

Figure A.1.: Multi-radio coexistence scenario. The receiver of standard A in terminal #1 is plagued by the strong signal transmitting by either terminal #1, terminal #M, or terminal #N.

$$\mathrm{NF}_{\mathrm{blocker}} \approx -174[\mathrm{dBm/Hz}] + \mathrm{P_b}[\mathrm{dBm}] + \mathrm{L}_{\omega}(\Delta\omega)[\mathrm{dBm/Hz}] \tag{A.1}$$

where $\mathrm{L}_{\omega}(\Delta\omega)$ is the LO phase noise at the interferer offset $\Delta\omega$ and $\mathrm{P_b}$ is the interferer power. Thirdly, in order to handle a large interferer, the linear receiver should have a large dynamic range, which would increase the receiver's power consumption. However if some interference suppression can be provided at the RF stage, all three problems are alleviated.

This paper presents a nonlinear receiver topology with frequency-independent interference tolerance. Based on the information of envelope amplitude of the interferer, the receiver is able to provide suppression at RF frequency for large interferers. It can achieve both good IB and OOB linearity, thus making it suitable for the multi-radio coexistence scenario. The suppression at RF frequency also alleviates the requirements for the following receiver circuit blocks and saves the overall power consumption. The paper is organized as follows. Section A.2 classifies different interference cases and reviews prior works. The fundamental theory of the nonlinear concept is presented in section A.3. The system modeling and analysis of nonlinear interference suppression for local

interference are carried out in section A.4. Section A.5 discusses the nonlinear interference suppression for general interference by extracting envelope information. The nonlinear receiver system operation under multiple large interferers is discussed in section A.6. Conclusions are drawn in section A.7.

A.2 Interference Cases and Reivew of Prior Works

A.2.1 Interference Scenarios and Cases

There are several wireless standards operating in a mobile handset device. Fig. A.2 illustrates the frequency allocation of different standards supported in mobile devices, starting from 1800 MHz to 2700 MHz. In this frequency range, there are several dominant communication standards, which are FDD LTE, TDD LTE, WiFi, Bluetooth and WiMAX, etc. The frequency spectrum is allocated differently for different countries and regions [7–10]. Several key points are observed here. Firstly, the smallest frequency separation between uplink and downlink of FDD LTE is 20 MHz. Secondly, the smallest frequency separation between WiFi and LTE is 12 MHz. Thirdly, FDD LTE, TDD LTE, WiFi, Bluetooth and WiMAX share a large frequency spectrum. Therefore the multi-radio coexistence in this frequency range requires filtering for interferers located very close to the desired signal in frequency domain.

The interference scenarios can be divided into two classes in terms of physical distance, namely collocation and proximity. The collocation scenario refers to that multiple radios are placed in the same physical unit that the interferers are generated locally inside the device. The transmitting power of LTE user equipment is 24 dBm. The measured antenna coupling for collocated 915 MHz patch antennas is roughly 20 dB in worst case [82].

The proximity scenario happens when multiple devices are placed very close. The transmitting signal from device #A generates interference for receivers in other devices. Therefore, the interferers are generated externally, e.g. from the use of LTE small cell access points and low-power WiFi routers [17]. The typical transmit power of an access point is around 20 to 30 dBm. The free space loss at 2.4 GHz for a distance of 0.5 m is 34 dB. Therefore, for both scenarios, the interference power can as strong as several dBm.

The interference scenarios of interest can be summarized into three cases:

1) *Out-of-band (OOB) interferers*
   From different standards and far away in frequency, as outof-band (OOB) interferers.

2) *Interferers from other standards and close frequency (tens of MHz), e.g. WiFi and LTE coexistence*
   Including local interference due to antenna coupling and external interference from other devices. Both interference power can be several dBm.

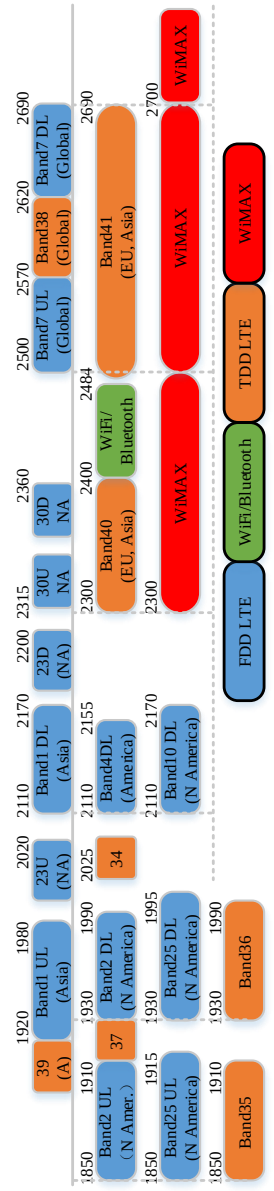

Figure A.2.: Frequency allocation of different wireless standards from 1800 MHz to 2700 MHz.

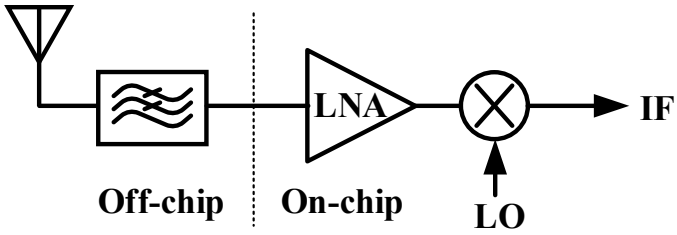

Figure A.3.: Simplified system architecture of a conventional narrowband receiver.

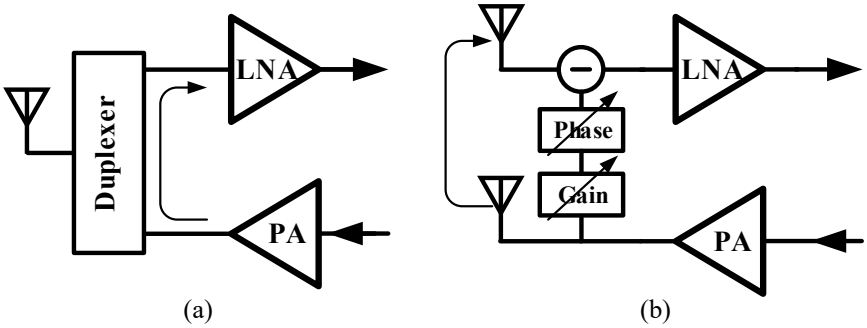

Figure A.4.: Simplified system architecture of (a) a FDD system with duplexer (b) an analog cancellation method of local interferer.

3) *Interferers from the same standard, in-band (IB) interference, e.g. WiFi/WiFi, LTE/LTE, FDD LTE UP/DN*
Including local interference due to TX leakage of FDD/FD systems and external interference from other devices. The TX leakage depends on the isolation provided by duplexer. Both interference power can be as strong as several dBm.

A.2.2 Interference Cancelling/Filtering Methods

In a conventional narrowband receiver as shown in Fig. A.3, RF signals and interference are bandpass-filtered by an off-chip SAW filter after the receiver antenna. In this way, the unwanted OOB interferers are filtered out. When the SAW-based filters are omitted after the receiver antenna, the receiver needs to provide blocker filtering and harmonic rejection function to meet the target of wireless communication specifications.

In FDD communication systems shown in Fig. A.4(a), a duplexer [84] is placed after the single antenna to allow bidirectional communication of receiving and transmitting signals. The functions of the duplexer are to provide matching, band selection, and to attenuate the transmitter leakage at the receiver input for avoiding desensitization of the receiver. The duplexer relies on

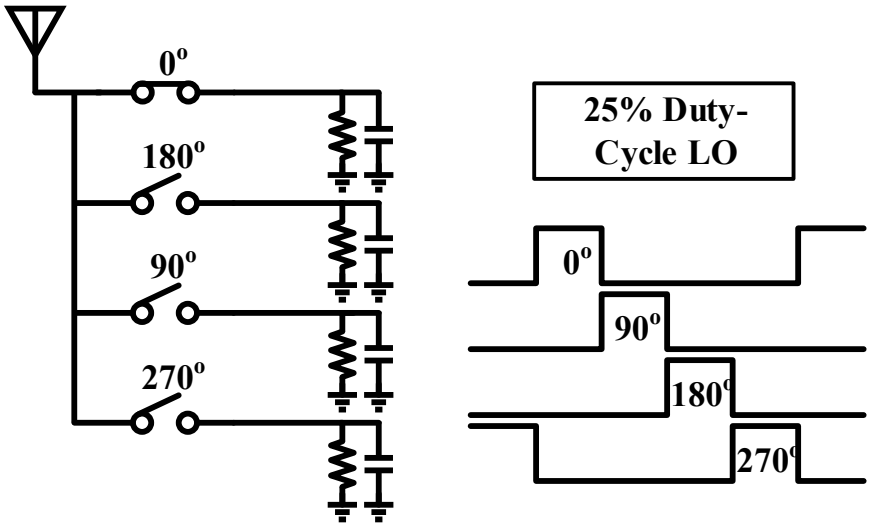

Figure A.5.: Model of 4-phase passive mixer with sampling capacitor, load resistor and LO driving waveforms.

frequency-selective filters for isolation and band selection, which often means high-Q and off-chip.

Fig. A.4(b) shows an analog cancellation technique [85] for locally generated interference signals. Based on prior known information of the transmitting signal and modeling of the coupling path, a replica interference signal can be subtracted at the input of the receiver, while the desired signal remains unaffected. However the technique fails to deal with unknown interference signals. The adaption of modeling of the coupling path can also be power hungry at RF frequency.

Instead of the conventional LNA-first approach, recent works [25, 86] suggest directly connecting the receiver antenna to a CMOS passive mixer. This approach is referred to as Mixer-first approach and is shown in Fig. A.5. There are four CMOS switch paths after the antenna, followed by RC lowpass filters (LPF). The switches are controlled by four path non-overlapping 25% duty-cycle LO signals. The CMOS switches are favored for its high linearity, wide tuning range, and bidirectional response-translational property. The LPF at baseband is translated to a bandpass filter (BPF) at RF frequency and it can achieve much higher quality factor at RF than by using on-chip LC components. However the interference filtering is limited by the switch resistance, accuracy of duty-cycle of LO signals, and the baseband filter order. It also suffers from limited isolation between RF and LO ports.

The simplified system architecture of a two-path feedforward cancellation receiver [87, 88] is shown in Fig. A.6(a). It is based on the up-conversion of

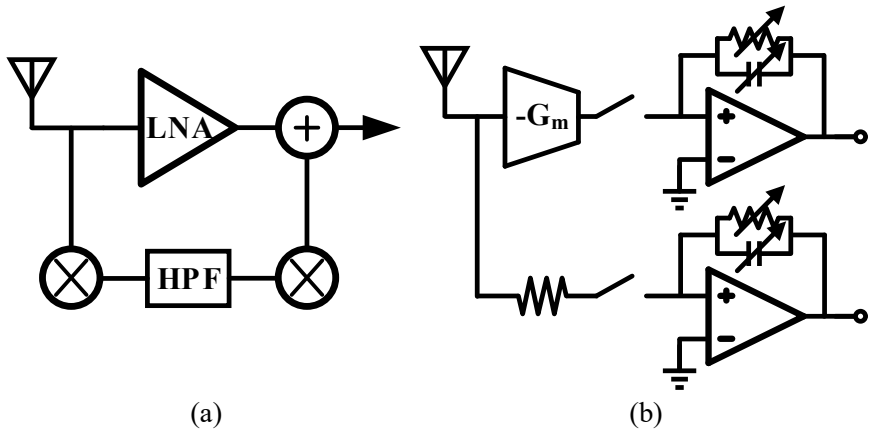

Figure A.6.: Simplified system architecture of (a) a two-path feedforward receiver (b) a frequency-translational noise-cancelling receiver.

baseband filters. In the main path, both desired signal and unwanted interferer are amplified. In the auxiliary path after down-conversion, the desired signal lies at DC and is filtered out by passing through a highpass filter. The interferer is up-converted again and subtracted at the output of the LNA. The auxiliary path is identical to a high-Q notch filter centered at the desired signal frequency. This approach has a better input matching and better isolation between RF and LO port. However, the LNA linearity becomes a bottleneck for the tolerance of large interferers.

The simplified system architecture of a frequency-translational noise-cancelling receiver [27] is shown in Fig. A.6(b). The receiver consists of two separate passive-mixer-based down-conversion paths. The passive mixer down-converts the RF current to baseband. A transimpedance amplifier (TIA) then converts the in-band current back to voltage. Therefore the voltage gain is avoided at RF until baseband filtering is provided. The 3dB noise figure brought by the matching resistor in the main path now can be cancelled by the auxiliary path. The Gm block is implemented as a CMOS inverter with small load impedance in order to handle large swings at the input. The frequency-translational noise-cancelling receiver achieves to provide blocker tolerance, good OOB linearity, input matching, and low noise at the same time. However the system's interference filtering is limited in the same way as in mixer-first approaches and also the IB linearity is poor in the presence of a large in-band blocker.

A.3 Fundamental of Nonlinear Interference Suppression

Nonlinear transfer functions [6, 89–91] behave fundamentally different from linear transfer functions. The nonlinear transfer function does not obey the rule of superposition. The signals passing through a nonlinear system can undergo different operations. Also, nonlinear systems do not necessarily require a large power consumption to handle a large signal. The fundamentals of a nonlinear system make it a possible candidate to deal with interference tolerance.

A.3.1 Time- and Frequency-domain behavior analysis

The input and output signals in frequency and time domain for various conditions are illustrated in Fig. A.7. When a large signal (single-tone) is passing through an ideal linear system as shown in Fig. A.7(a), the signal is amplified linearly at the output. When the same input signal is passing through a conventional compressive nonlinear system as shown in Fig. A.7(b), the signal gets distorted at the output and 3rd order harmonic is generated. Fig. A.7(c) shows a specially-tailored nonlinear system with a third-order polynomial transfer function. When the large signal pass through, the fundamental tone of the large signal is completely removed at the output, while a 3rd harmonic is created. The process can be described using the following mathematical Eqn. (A.2) - (A.6). The nonlinear transfer function is described as:

$$y(t) = c_1 x(t) + c_3 x^3(t) \tag{A.2}$$

The input signal is defined as a strong sinusoidal signal with amplitude A_{LS} and frequency ω_{LS}:

$$x(t) = A_{LS} sin(\omega_{LS} t) \tag{A.3}$$

The output signal y(t) equals to:

$$y(t) = \left[c_1 A_{LS} + c_3 \frac{3A_{LS}^3}{4} \right] sin(\omega_{LS} t) + c_3 \frac{3A_{LS}^3}{4} sin(3\omega_{LS} t) \tag{A.4}$$

If choosing

$$c_3 = -\frac{4c_1}{3A_{LS}^2} \tag{A.5}$$

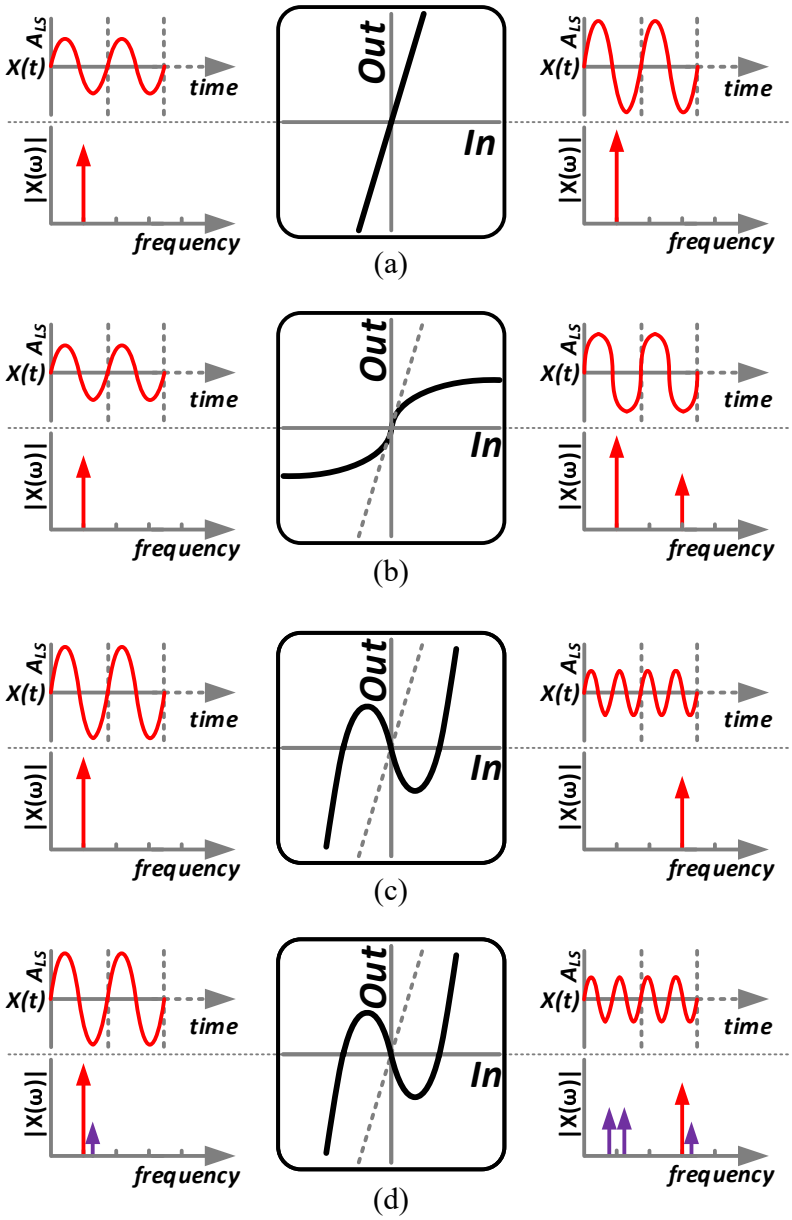

Figure A.7.: Input and output of a large (single-tone) signal in frequency and time domain when passing through a (a) ideal linear system (b) conventional nonlinear system (c) proposed nonlinear system (d) proposed nonlinear system in accompany with a weak signal.

the output becomes:

$$y(t) = -c_1 \frac{A_{LS}}{3} sin(3\omega_{LS}t) \tag{A.6}$$

Furthermore, the nonlinear transfer function does not obey the rule of superposition. Therefore, the large signal in accompany with a (much weaker) signal passing through the nonlinear system can undergo different operations. The situation is illustrated in Fig. A.7(d). At the output, the large signal at fundamental frequency is suppressed completely, while the fundamental tone of the weak signal is amplified. 3rd harmonics are generated for both large signal and weak signal. Besides, an intermodulation (IM) term arises with the same power as the output of the fundamental tone of the weak signal. The intermodulation term is the result of nonlinearity and convolution between input signals, and introduces noise folding into the signal band [6], which will be discussed later.

Therefore based on the envelope amplitude of the large interferer, the specially-tailored nonlinear transfer function enables large interference suppression. When the amplitude of the large interferer changes, e.g. modulated interferers, the nonlinear transfer function should be altered correspondingly to maintain the suppression. The nonlinear interference suppression can be considered as a notch filter in amplitude domain. The adaption of the nonlinear transfer function in amplitude domain is equivalent to the adaption of a frequency domain notch filter. When the interferer amplitude is similar to or smaller than the wanted signal, the transfer function can be switched to a linear one.

The adaption is shown in Fig. A.8. The nonlinear interference suppression relies on the amplitude discrimination between the strong signal and the weak signal. This is similar to frequency domain filtering that relies on the relative frequency difference between input signals. In this way, the nonlinear interference suppression method enables frequency-independent filtering.

A.3.2 Nonlinear Transfer Characteristics for Large Interference Suppression

To derive the general requirements of a nonlinear transfer function for interference suppression, the input signal x(t) is defined here:

$$\begin{aligned} x(t) &= Int(t) + s(t) \\ Int(t) &= A_{LS}(t) sin[\omega_{LS}t + \varphi_{LS}(t)] \\ s(t) &= A_{SS}(t) sin[\omega_{SS}t + \varphi_{SS}(t)] \\ A_{SS} &<< A_{LS} \end{aligned} \tag{A.7}$$

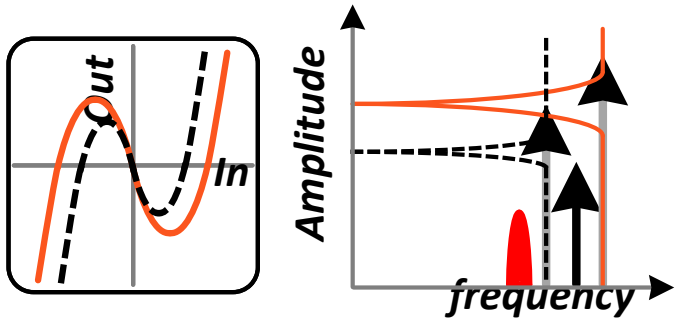

Figure A.8.: The adaption of nonlinear transfer function to maintain large signal suppression when the amplitude of large signal changes.

which consists of a strong interference signal Int(t) and a much weaker desired signal s(t), with their corresponding amplitude, frequency and phase information. The input is fed to a memoryless nonlinear system with transfer function y=f(x). By applying Fourier analysis to the output signal, the effective gain of the fundamental component of the strong signal G_{LS} can be expressed as:

$$G_{LS} = \frac{1}{A_{LS} \cdot \pi} \int_{-\pi}^{\pi} f(A_{LS} sin\theta) \cdot sin\theta d\theta \tag{A.8}$$

The transfer function y=f(x) can be expressed as the sum of odd and even functions:

$$f(x) = f_{odd}(x) + f_{even}(x) \tag{A.9}$$

For Eqn. (A.8) to equal to 0, the transfer function can only consist of odd-order terms. Eqn. (A.8) becomes:

$$G_{LS} = \frac{2}{A_{LS} \cdot \pi} \int_{0}^{\pi} f_{odd}(A_{LS} sin\theta) \cdot sin\theta d\theta \tag{A.10}$$

For the entire integration interval $\theta \in [0, \pi]$, $sin\theta \geqslant$ always exists, which means $f_{odd}(A_{LS} sin\theta)$ must change sign in this interval. Therefore the transfer function y=f(x) must have at least one zero crossing in each interval $x \in [-A_{LS}, 0)$ and $x \in (0, A_{LS})$. The third zero crossing is at the origin because of odd-order symmetry. Chebyshev polynomials are found to fulfill the requirement for such nonlinear transfer functions to provide large signal suppression [72]. It is also clear that the transfer function f(x) is also a function of A_{LS} and y=f(x,A_{LS}). If the input interference has varying envelope amplitude, e.g. modulated interferer, the transfer function should be adapted accordingly to the instantaneous value of the interferer envelope amplitude.

A.3.3 Consequence for Weak Desired Signal

The effective gain of the fundamental component of the weak signal G_{SS} can be expressed as

$$G_{SS} = \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot PDF_{sine}(x)dx \tag{A.11}$$

From Eqn. (A.11), G_{SS} is a function of A_{LS}, probability density function (PDF) of the sinusoidal Int(t) and f(x). Both G_{LS} an G_{SS} depends on the amplitude of Int(t) and transfer function y=f(x), while the phase or frequency of Int(t) and s(t) is irrelevant. In case there is no large interference or only small interference exists, the system transfer function can be switched to a linear one, resulting in conventional compressive receiver behavior.

Given the expression of effective gain of strong signal and weak signal, the output of the nonlinear transfer function using method described in [92] becomes:

$$\begin{aligned} y(t) = G_{LS} \cdot Int(t) + \frac{1}{2}\left[A_{LS} \cdot \frac{\partial G_{LS}}{\partial A_{LS}} + G_{LS}\right] \cdot s(t) \\ + \frac{1}{2}\left[A_{LS} \cdot \frac{\partial G_{LS}}{\partial A_{LS}} - G_{LS}\right] \cdot IM(t) \end{aligned} \tag{A.12}$$

in which the first term is the remaining residue of strong interference, the second term is the desired signal output and the third term is the intermodulation (IM) product between the strong and weak signal. The IM product is given by:

$$IM(t) = A_{SS}(t)sin\left[(2\omega_{LS} - \omega_{SS})t + 2\varphi_{LS}(t) - \varphi_{SS}(t)\right] \tag{A.13}$$

With complete interference suppression, G_{LS}=0, the desired signal output and the IM term have the same magnitude, which explains the frequency domain behavior in Fig. A.7(d). When the nonlinear transfer function is set for full suppression at amplitude A_{LS}, the weak signal at ω_{SS} is mirrored to the frequency component at $2\omega_{LS} - \omega_{SS}$. On the other hand, the noise at $2\omega_{LS} - \omega_{SS}$ is folded to the desired signal frequency. If the frequency difference between strong signal and small signal $|\omega_{LS} - \omega_{SS}|$ is small, the cross-talk introduces noise penalty of 3 dB. If the frequency difference is large and the circuit is narrowband, the noise penalty is less than 3 dB.

A.3.4 Transfer-Specific Characteristics

To further analyze the nonlinear operation and consequences, a specific nonlinear transfer function is chosen here. As shown in Fig. A.9, the zig-zag function is created by high order Chebyshev polynomials. By limiting a to 0, it has infinite slope in the zero-transition region 2. The mathematic expression

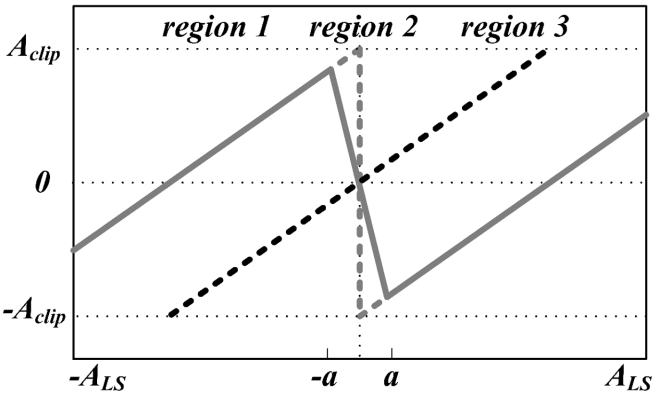

Figure A.9.: Zig-zag transfer function (grey) for an interferer with envelope amplitude of A_{LS}. By limiting a to zero, the zig-zag function has an infinite slope in the zero-transition region 2. The creation of the zig-zag transfer function can be considered as shifting the linear transfer (black) in the y-axis in opposite directions in region 1 and 3.

of the zig-zag function is:

$$f(x) = \begin{cases} G_{lin} \cdot x + A_{clip}, & \text{if } x < -a \\ (G_{lin} - \frac{A_{clip}}{a}) \cdot x, & \text{if } -a \leqslant x \leqslant a \\ G_{lin} \cdot x - A_{clip}, & \text{if } x > a \end{cases} \tag{A.14}$$

where G_{lin} is the slope of the function in region 1 and 3. For complete suppression at amplitude A_{LS}, based on Eqn. (A.8),

$$G_{LS} = G_{lin} - \frac{4A_{clip}}{\pi A_{LS}}, \quad A_{clip,supp} = \frac{\pi}{4} A_{LS} G_{lin} \tag{A.15}$$

Based on Eqn. (A.11), assuming a unity amplitude interferer for simplicity, the first order small signal gain $G_{SS,1}$ becomes:

$$\begin{aligned} G_{SS,1} &= \int_{-1}^{-a} G_{lin} \cdot \frac{dx}{\pi\sqrt{1-x^2}} + \int_{-a}^{a} \left(G_{lin} - \frac{A_{clip}}{a} \right) \cdot \frac{dx}{\pi\sqrt{1-x^2}} \\ &\quad + \int_{a}^{1} G_{lin} \cdot \frac{dx}{\pi\sqrt{1-x^2}} \\ &= \frac{G_{lin}}{\pi} \left[\pi - \frac{2\pi}{4a} arcsin(a) \right] \end{aligned} \tag{A.16}$$

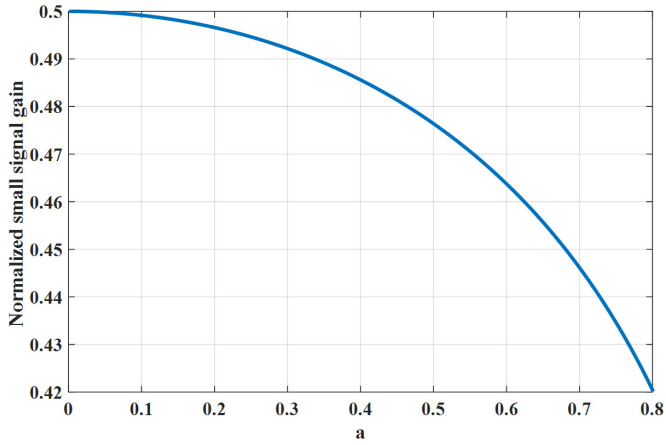

Figure A.10.: The influence of zero-transition region a on normalized small signal gain $G_{SS,1}$ using zig-zag transfer function for nonlinear interference suppression.

$$\lim_{a \to 0} G_{SS,1} = \frac{G_{lin}}{2}$$

The dependence of $G_{SS,1}$ on the value a of the zero-transition region 2 in the zig-zag function is shown in Fig. A.10. The normalized small signal gain varies little with change of value a, which can be explained by the weighting function of the PDF of the sinusoidal input waveform in Eqn. (A.11). Because the PDF of a sinusoidal waveform is high near the edges and low in the center, the circuit is forced to operate mostly near the edges in large signal operation. So the derivative of the zig-zag function in region 1 and 3 plays a bigger role on $G_{SS,1}$. Therefore the weak desired signal will experience amplification if G_{lin}>2 and Eqn. (A.15) is satisfied. However the large signal suppression is decreasing with increasing a since the zig-zag function deviates more from the original setting.

The third order small signal gain $G_{SS,3}$, assuming a is approaching zero, can be calculated using:

$$\lim_{a \to 0} G_{SS,3} = \int_{-A_{LS}}^{A_{LS}} \frac{\partial^3 f(x)}{\partial^3 x} \cdot \frac{dx}{\pi\sqrt{1-x^2}} = -\frac{G_{lin}}{16 A_{LS}^2} \tag{A.17}$$

leading to:

$$V_{IIP3} = \sqrt{\left|\frac{4G_{SS,1}}{3G_{SS,3}}\right|} = \sqrt{\frac{32}{3}} \cdot A_{LS} \tag{A.18}$$

So, the IIP3 of the nonlinear system using the ideal zig-zag transfer function is approximately 10dB higher than the amplitude of strong interferer signal.

A.3.5 Noise Properties of Noiseless Nonlinear Transfers

Based on Eqn. (A.11), the output signal power can be calculated as:

$$\begin{aligned}\text{Output signal power} &= |A_{SS} \cdot G_{SS}|^2 \\ &= |A_{SS}|^2 \cdot \left| \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \right|^2 \end{aligned} \tag{A.19}$$

As shown in Fig. A.9, the derivative of the zig-zag transfer function changes sign between different regions, resulting from the requirement for three zero crossings. The circuit will experience constructive behavior in region 1 and 3, and destructive behavior in region 2.

However for output noise power, all regions lead to additive behavior because the noise is white. So the output noise power can be calculated by:

$$\text{Output noise power} = \int_{-A_{LS}}^{A_{LS}} \left| \frac{\partial f(x)}{\partial x} \cdot v_n \right|^2 \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \tag{A.20}$$

where v_n is the standard deviation of the Gaussian noise voltage.

Based on Eqn. (A.19) and (A.20), the noise folding penalty brought by the nonlinear transfer function can be calculated by Eqn. (21), in which the numerator is the output noise power and the denominator is the output signal power when the input signal is equivalent to noise voltage:

$$\begin{aligned}\mathrm{F} &= \frac{\text{Output noise power}}{\text{Output signal power}|_{A_{SS}=v_n}} \\ &= \frac{|v_n|^2 \cdot \int_{-A_{LS}}^{A_{LS}} \left| \frac{\partial f(x)}{\partial x} \right|^2 \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}}}{|A_{SS}|^2 \cdot \left| \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \right|^2} \end{aligned} \tag{A.21}$$

If the transfer function y=f(x) is a noiseless linear function, i.e. $f(x) = c_1 x$, Eqn. (A.21) becomes:

$$\mathrm{F}_{\text{linear}} = \frac{\int_{-A_{LS}}^{A_{LS}} |c_1|^2 \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}}}{\left| \int_{-A_{LS}}^{A_{LS}} c_1 \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \right|^2} = 1 \tag{A.22}$$

since there's no spectrum mirroring and high frequency terms in a linear transfer function. If the transfer function is a noiseless 3rd Chebyshev polynomial as shown in Eqn. (A.2) and (A.5), Eqn. (A.21) becomes:

$$\mathrm{F_{3rd}} = \frac{\int_{-A_{LS}}^{A_{LS}} \left|c_1 - 4c_1x^2\right|^2 \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}}}{\left|\int_{-A_{LS}}^{A_{LS}} (c_1 - 4c_1x^2) \cdot \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}}\right|^2} = 3 \tag{A.23}$$

That equals to a noise figure (NF) of 4.77 dB, resulting from the noise folding from the mirroring product and 3rd harmonic component.

If the transfer function is a noiseless zig-zag nonlinear function as shown in Eqn. (A.14) and (A.15), and shown in Fig. A.9, assuming a unity amplitude interferer for simplicity, the numerator in Eqn. (A.21) becomes:

$$\begin{aligned}\text{Numerator} &= \int_{-1}^{-a} |G_{lin}|^2 \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} + \int_{-a}^{a} |G_{lin} - \frac{\pi \cdot G_{lin}}{4a}|^2 \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \\ &+ \int_{a}^{1} |G_{lin}|^2 \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \\ &= |G_{lin}|^2 \cdot \left[1 + \left(\frac{\pi}{8a^2} - \frac{1}{a}\right) \cdot arcsin(a)\right]\end{aligned} \tag{A.24}$$

The denominator in Eqn. (A.21) becomes:

$$\begin{aligned}\text{Denominator} &= \Big| \int_{-1}^{-a} G_{lin} \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} + \int_{-a}^{a} \left(G_{lin} - \frac{\pi \cdot G_{lin}}{4a}\right) \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \\ &+ \int_{a}^{1} G_{lin} \frac{dx}{\pi\sqrt{A_{LS}^2 - x^2}} \Big|^2 \\ &= |G_{lin}|^2 \cdot \left[1 - \frac{arcsin(a)}{2a}\right]^2\end{aligned} \tag{A.25}$$

The noise factor of a noiseless zig-zag transfer function becomes:

$$\mathrm{F_{zig-zag}} = \frac{1 + \left(\frac{\pi}{8a^2} - \frac{1}{a}\right) \cdot arcsin(a)}{1 - \frac{arcsin(a)}{2a}} \tag{A.26}$$

Eqn. (A.26) is plotted in dB scale in Fig. A.11. By decreasing a, the NF increases steadily. This is because by decreasing a, the nonlinear zig-zag function has sharper zero transition in region 2, introducing more noise from high frequency components folding onto the signal frequency. By increasing a, NF

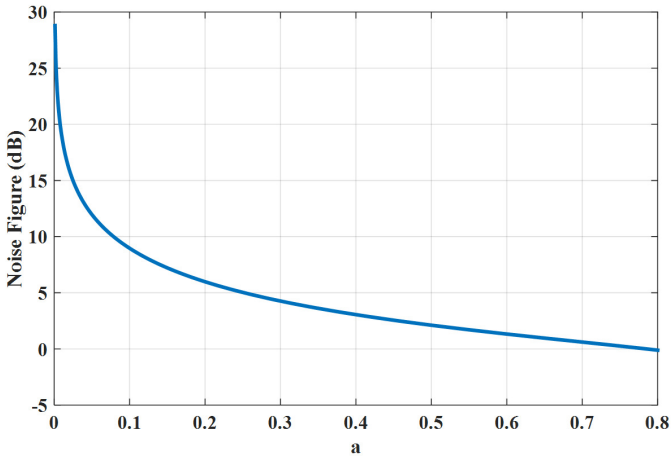

Figure A.11.: The influence of zero-transition region a on noise figure (NF) using zigzag transfer function for nonlinear interference suppression.

keeps decreasing as fewer high frequency noise components folds to the signal band. The NF almost decreases to zero at large a value. However this result is meaningless since the transfer function at larger a value is totally different from an ideal zigzag function and Eqn. (A.15) is no longer satisfied.

A.4 Nonlinear System Modelling and Analysis

A.4.1 System Architecture

A 1.8 GHz RF amplifier with linear mode and nonlinear mode operation was implemented in a 140 nm CMOS technology. The nonlinear mode operation is enabled for frequency-independent interference suppression, while the linear mode is for linear amplification when no large interference is present. In the presence of a 0 to 11 dBm interferer, the interferer is suppressed by more than 39 dB [6]. The PCB including the nonlinear RF amplifier IC implementation is shown in Fig. A.12.

Fig. A.13(a) shows the system diagram of applying the nonlinear method to the multi-radio coexistence in the same device. The highlighted are the key sub-blocks in the nonlinear receiver system, including NIS, cross-correlation mixer, LPF, ADC, DAC, Magnitude, NIS Control sub-blocks. To derive the exact amplitude information of the interferer, the baseband I and Q signal from the transmitter are fed to the Magnitude subblock. The Magnitude sub-block models the path loss between transmitter baseband and receiver antenna and is connected to a sub-block named NIS Control. The NIS Control sub-block interfaces a DAC that steers the control signal A_{clip} to the NIS sub-block,

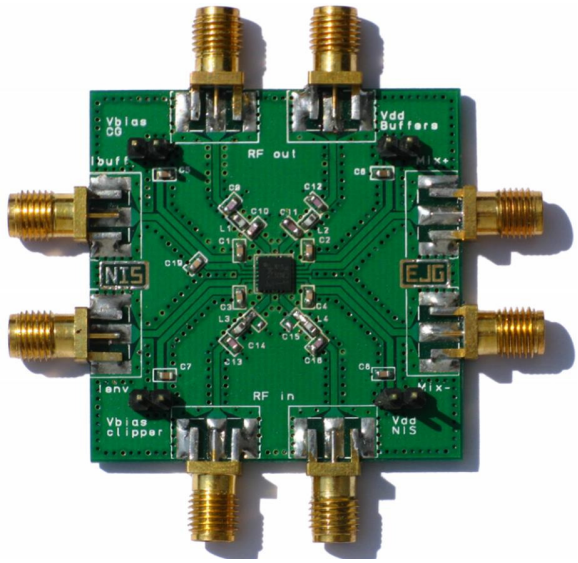

Figure A.12.: PCB including the Nonlinear Interference Suppression (NIS) IC implementation.

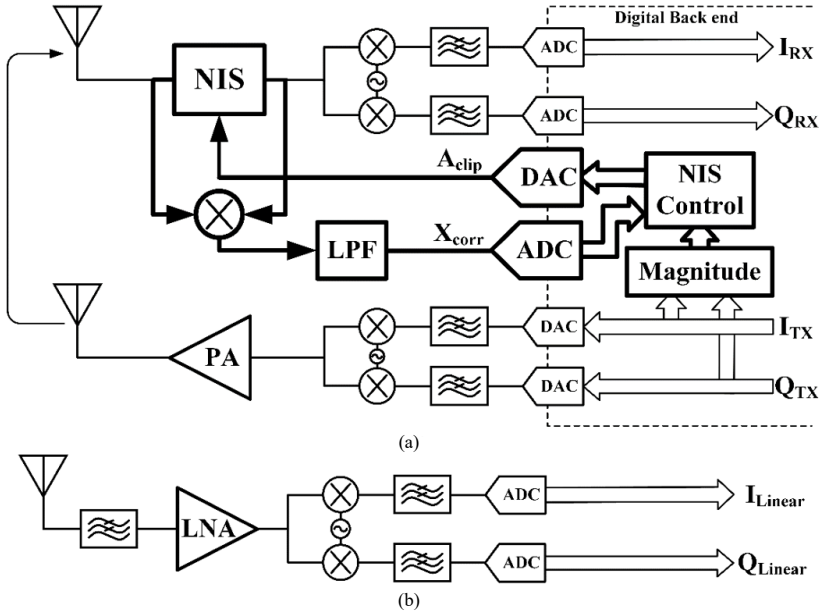

Figure A.13.: The system diagram of (a) the proposed NIS operation in a multi-radio platform (b) a conventional narrowband receiver with off-chip SAW filter.

where the nonlinear suppression is performed. This path can be recognized as a feedforward path. Based on the interferer information from transmitter baseband, the feedforward path gives the correct control signal with accuracy and speed.

On the other hand, a feedback path is also needed to model the coupling changes between the transmitter antenna and the receiver antenna. Therefore, a mixer is placed around the NIS sub-block to provide cross-correlation between the input and output of the NIS sub-block. Assuming the interferer is the dominant signal, the cross-correlation measures how much the residue interference remains after nonlinear suppression, representing the errors in control signal A_{clip}. The cross-correlation signal is fed back to the NIS control sub-block to form a feedback path. The feedback path only requires low speed because environment changes slowly, while the feedforward path should be fast enough to update the control signal with the changes of the interferer envelope amplitude.

A conventional narrowband receiver with off-chip SAW filter is shown in Fig. A.13(b) for a comparison of interference tolerance with the nonlinear receiver system in a later section. Both receivers are assumed with direct conversion architecture.

A.4.2 NIS Modelling and Analysis

The nonlinear receiver system is modeled in Advanced Design System (ADS). The NIS, cross-correlation mixer, NIS Control, Magnitude sub-blocks are modeled with symbolically defined devices. The down-conversion mixer uses ideal mixer component with ideal I/Q demodulation. The baseband filter is set as a 4th order Butterworth filter with a bandwidth determined by the data rate of the wanted signal. The amplifier is set as ideal 30 dB gain broadband amplifier.

16-QAM modulation scheme is used for both the interferer and the desired signal with raised cosine pulse shaping and a roll-off factor of 0.5. The baseband I and Q of both signals have a data rate of 20 Mbps. The weak signal lies at 1.825 GHz (fs) with -50 dBm power and the strong signal at 1.870 GHz (fi) with 10 dBm power. The frequency separation Δf between the input signals is 15 MHz. The input spectrum is shown in Fig. A.14(a).

The output spectrum of the NIS sub-block is shown in Fig. A.14(b). As shown in Fig. A.14(b), the fundamental tone of the weak signal remains, while the fundamental tone of the interferer is totally suppressed. The intermodulation terms lies at $2f_i$-f_s and its bandwidth depends on the convolution of the wanted signal and the interferer. The interference suppression by NIS sub-block is about 80 dB. After passing to the baseband, the signal is amplified by 1000 times, while the interferer residue and intermodulation term is further suppressed, as shown in Fig. A.14(c). The constellation diagram of the baseband output is shown in Fig. A.15. The corresponding error vector magnitude

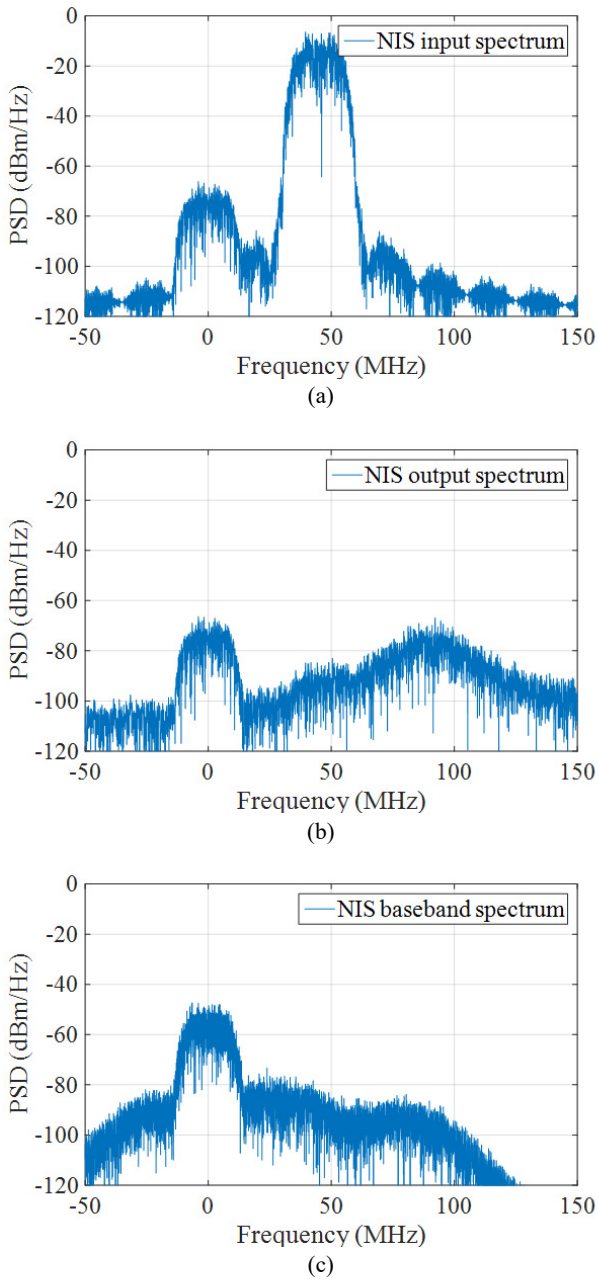

Figure A.14.: The frequency spectrum of (a) input at receiving antenna (b) output of NIS sub-block (c) baseband output.

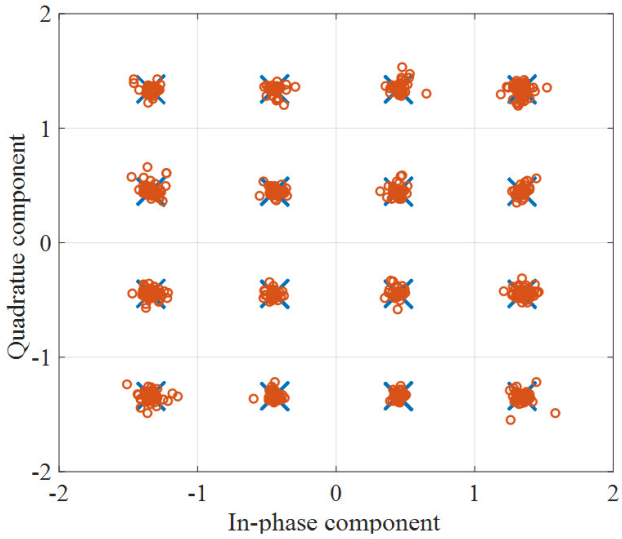

Figure A.15.: Baseband output constellation diagram of the nonlinear receiver system.

Table A.1.: Interference Suppression Limitations

Interference Power (dBm)	Interference suppression at RF (dB)	EVM (%)	SNR (dB)
-30	20	14.4	17
-20	42	3.7	29
-10	56	1.9	34
0	66	1.9	34
10	80	2.9	31

(EVM) is 2.82%, which corresponds to a signal-to-noise ratio (SNR) of 31 dB. 16-QAM modulation requires a SNR of 17.6 dB to achieve a symbol-to-error ratio (SER) of 10^{-3} [93], which is achieved here.

As pointed out before, the interference suppression at RF stage by nonlinear transfer function is based on the amplitude discrimination between the interferer and the wanted signal. To illustrate the influence of the relative power ratio, the input si gnals are kept the same except the interferer power is swept from -30 dBm to 10 dBm. The result of RF suppression, EVM and SNR at baseband output are shown in Table A.1. For an increasing interference power, larger interference suppression at RF is achieved with a better EVM and SNR at baseband output.

The probability densify function (PDF) of the instantaneous power of the modulated interferers for input power and the PDF of the wanted signal are shown in Fig. A.16. It is observed that when the relative power ratio between

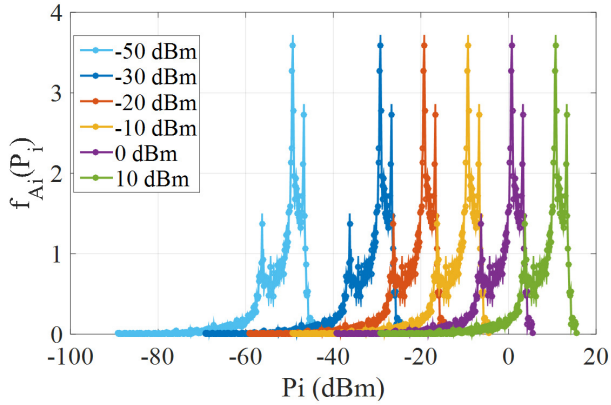

Figure A.16.: Probability density function of the instantaneous power of the interferer with from -30 dBm to 10 dBm and probability density function of the instantaneous power of the wanted signal with -50 dBm power (light blue).

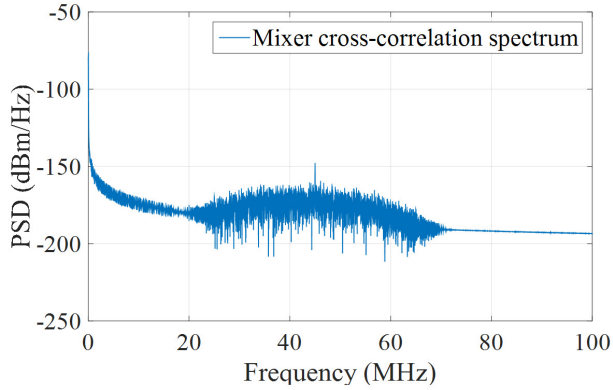

Figure A.17.: The frequency spectrum of cross-correlation mixer output.

the interferer and the wanted signal is as low as 20 dB, the PDF of the instantaneous power of the interferer overlaps with that of the wanted signal. Therefore the nonlinear system is incapable to distinguish one from another, thus leading to the limited suppression performance of the interferer and distortion of the desired signal. When the relative power is even lower, the NIS sub-block output is completely flooded by noise and distortion.

The limitation for complete interference suppression also comes from baseband filtering for signals outside the baseband bandwidth. The baseband filtering is determined by the baseband filter design such as order and power.

The cross-correlation mixer output spectrum is shown in Fig. A.17. The output spectrum has convolution products at DC and intermodulation frequency.

As the interferer is totally suppressed in this case, the output spectrum at DC and intermodulation frequency is low. If the interferer is only partially suppressed, the mixer output at DC will reflect the error in the control signal. The intermodulation term would also be bigger but discarded because the speed of the feedback path is slow.

For simplicity the 3rd order harmonic generated by the nonlinear receiver with nonlinear transfer function is not shown here. It can be removed by frequency-domain filters and harmonic rejection mixers to avoid harmonic mixing.

A.4.3 Comparison of Linear and Nonlinear Receiver

The system diagrams of a nonlinear receiver system with proposed nonlinear interference suppression and a conventional narrowband linear receiver are shown previously in Fig. A.13(b). The down-conversion mixer and baseband circuitry are set as exactly the same for a fair comparison on interference tolerance. The low noise amplifier (LNA) in the conventional linear narrowband receiver is configured as ideal component and unit gain. That is same for the setting of nonlinear transfer function to provide unit gain for the desired signal. Therefore, in the modeling of the conventional linear narrowband receiver in ADS, the LNA is simply removed. The SAW filter after the antenna is set with a center frequency at the signal frequency, a passband bandwidth of 200 MHz and a stopband bandwidth of 220 MHz with 40 dB attenuation. Again the same input signals are used here, a 16-QAM interferer with 10 dBm power and a 16-QAM weak wanted signal with -50 dBm power.

The signal-to-interference ratio (SIR) is used here to characterize the interference tolerance and influences on the linear and nonlinear receiver. Initially the SIR at the input of the receiver is -60 dB. The SIR at the input of baseband ADCs should be at least higher than zero, so that the signal is amplified while the interferer is largely suppressed. The suppression of interference signal before ADC is beneficial since it alleviates signal aliasing. Besides, the residue interference also needs extra ADC resolution bits to quantize the total input at baseband A DCs. According to [93], one additional ADC bit should be added for every 6 dB decrement of SIR, which will leads to a huge increase in ADC power consumption.

The comparison of SIR at baseband output of the linear receiver and the nonlinear receiver versus frequency separation between large interference and wanted signal is shown in Fig. A.18. The SIR of the linear receiver is achieved completely by the SAW filter and baseband 4th order LPF. Between the edge of the passband and stopband of the SAW filter, the SIR of the linear receiver increase sharply as the interference falls outside the SAW filter passband. The SIR of the nonlinear receiver is achieved with the help of nonlinear interference suppression. The SIR of the nonlinear receiver has a positive value and

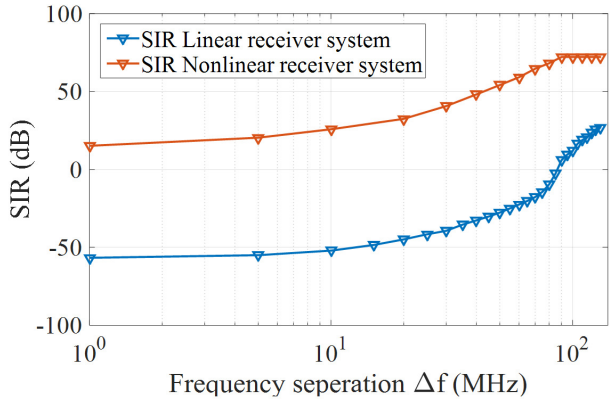

Figure A.18.: SIR of baseband output of the linear receiver (blue) and the nonlinear receiver (red) versus the frequency separation between input signals.

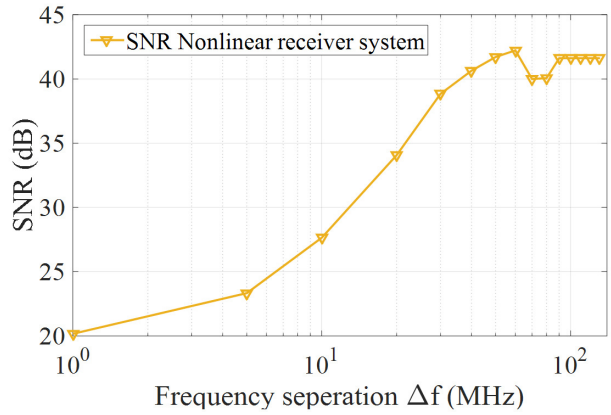

Figure A.19.: SNR of baseband output of the nonlinear receiver versus the frequency separation.

is higher than the SIR of the linear receiver. Since the nonlinear interference suppression is frequency independent, the increase of SIR curve of the nonlinear receiver is similar to that of the linear receiver. However, since both input signals have 20 MHz bandwidth, both SIR do not increase exactly like a 4th transfer function. As the frequency separation Δf between the input signals increases, the available suppression provided by the baseband filter is limited by the noise floor, which leads to a saturated value of SIR for the nonlinear receiver. The SNR at the baseband output of the nonlinear receiver system is shown in Fig. A.19. The SNR is 20.2 dB at Δf of 1 MHz and converges to 42 dB when Δf increases.

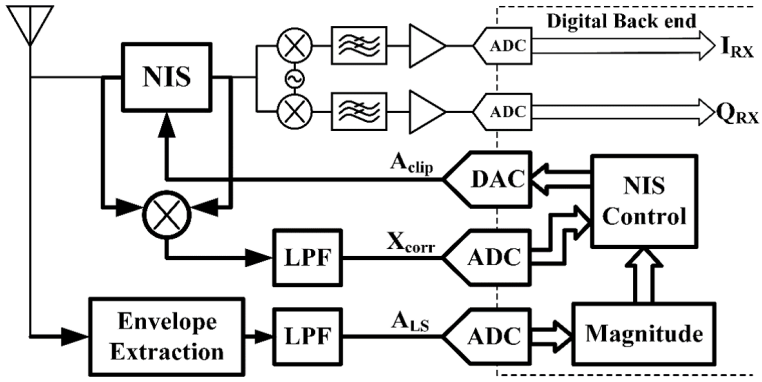

Figure A.20.: The system diagram of the proposed NIS operation for general interference suppression.

A.5 NIS Modelling for General Interference

A.5.1 System Architecture for General Interference Suppression

To extend the nonlinear method to the suppression of general large interference, the envelope amplitude of the interference needs to be extracted. The system architecture for general large interference suppression is shown in Fig. A.20.

The feedforward path starts from the receiving antenna and consists of an Envelope Extraction sub-block followed by LPF to derive the amplitude information. The Envelope Extraction sub-block can be implemented as self-mixing mixers or diodes. The extracted envelope contains noise received by antenna, the envelope information of the desired signal and the envelope information of interferer. However as the focus of this work is the coexistence of large interferer and weak desired signal, the envelope of the wanted signal behaves as noise and small disturbance to the control signal A_{clip}.

A.5.2 NIS modelling and Analysis

Here the desired signal is assumed as a 16-QAM modulated signal with raised cosine pulse shaping and a roll-off factor of 0.5. The baseband I and Q signals have a data rate of 10 Mbps. The interference is a QPSK signal with same pulse shaping, and a data rate of 2.5 Mbps for baseband I and Q. The weak signal lies at 1.825 GHz (f_s) with -50 dBm power and the strong signal at 1. 870 GHz (f_i) with 10 dBm power. The input spectrum of the nonlinear receiver is shown in Fig. A.21(a).

The output spectrum of NIS sub-block is shown in Fig. A.21(b). It is observed that the fundamental component of the weak signal remains, while

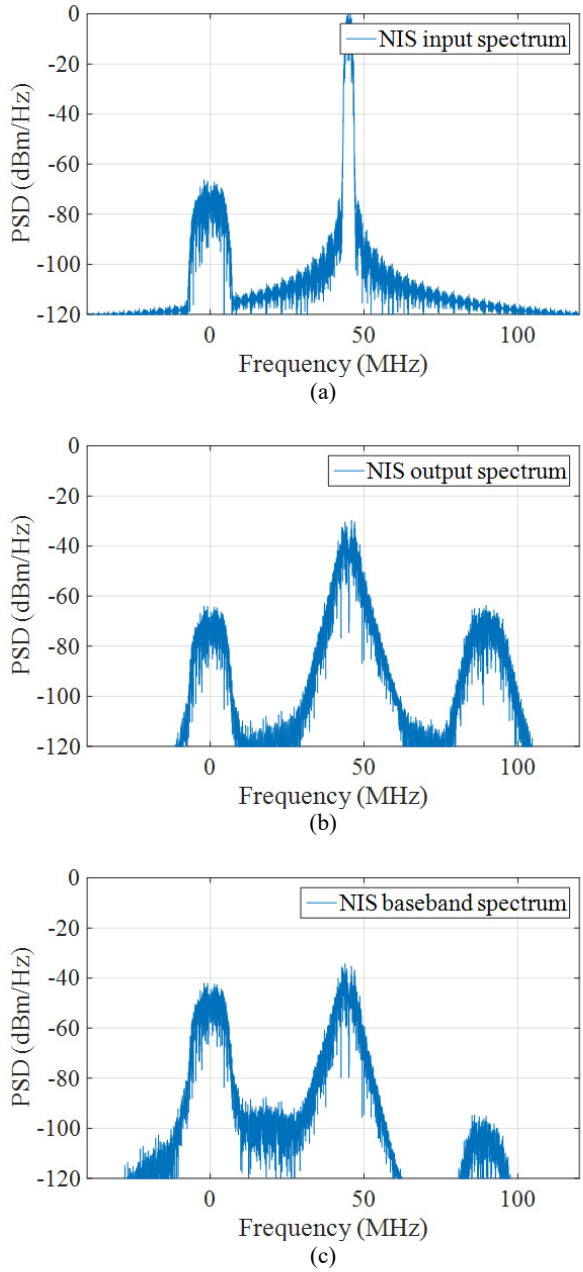

Figure A.21.: The frequency spectrum of (a) input at receiver antenna (b) output of NIS sub-block (c) baseband output.

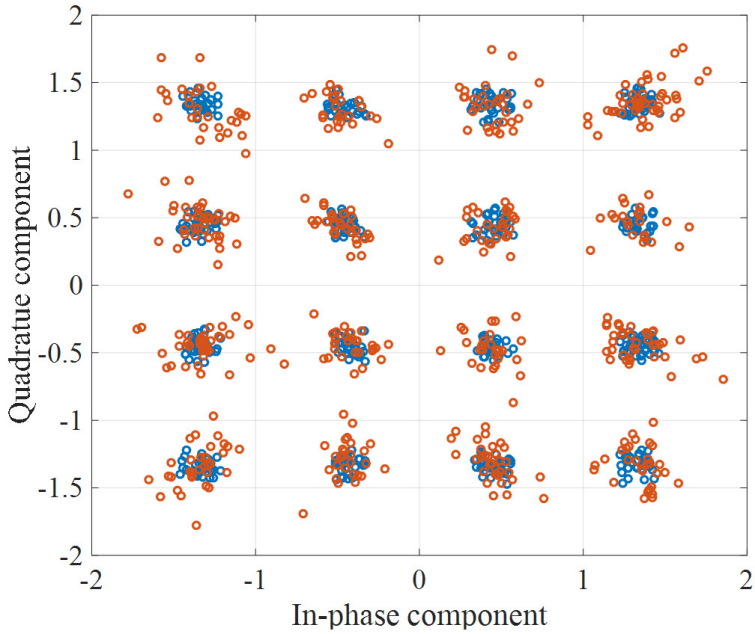

Figure A.22.: Baseband output constellation diagram of the nonlinear receiver system for general large interference suppression.

the interference signal is only partially suppressed. The nonlinear interference suppression at RF is about 40 dB. Therefore more filtering at baseband is need. The baseband filter order is increased to 6th order. After passing the baseband circuitry, the signal is amplifier by 30 dB, while the interference residue and the intermodulation term is further suppressed, as shown in Fig. A.21(c). The constellation diagram of the baseband output is shown in Fig. A.22. The EVM at the baseband output is 5.4%, which corresponds to a SNR of 25 dB.

The limited suppression at RF is a result of inaccuracy of the extracted interference envelope. Fig. A.23 shows the comparison of frequency spectrum between the input interferer envelope and the control signal for NIS sub-block. The spectrum of the control signal is quite the same at DC compared to the interferer envelope spectrum. However there is an intermodulation term at Δf. The intermodulation term is the result of convolution between the input signals in frequency domain. Thus a LPF is needed after the Envelope Extraction sub-block to filter out the intermodulation term. However there is a tradeoff between the filtering of the intermodulation term and the delay introduced by the filter. The filter bandwidth could be set small to filter out the intermodulation term completely, while it will introduces a big delay on the control signal. On the other hand, if the filter bandwidth is set large so that there's little delay introduced, the residue of the intermodulation term brings error to the control

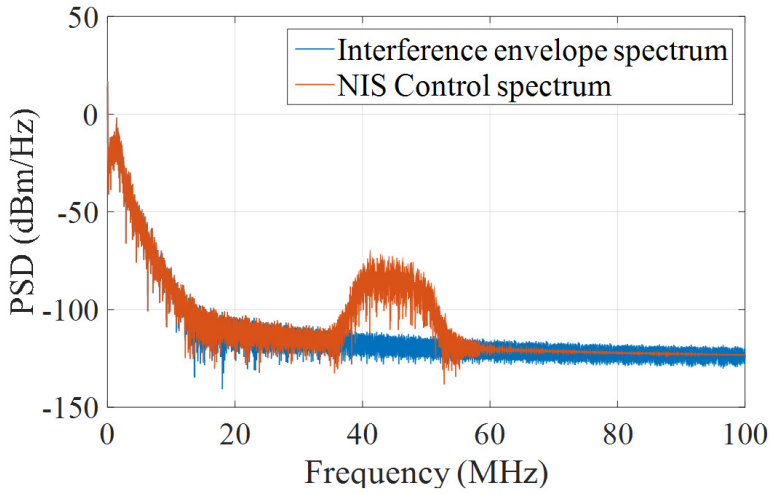

Figure A.23.: The frequency spectrum of envelope of the interferer (blue) and control signal for NIS sub-block (red).

Table A.2.: Trade-off of F_{LPF} on Interference Suppression

F_{LPF} (MHz)	Intermodulation (dBm)	Delay (ns)	Suppression wo. delay (dB)	Suppression wi. delay (dB)
5	-90	36	30	52
10	-69	18	38	50
20	-60	8	46	45

signal.

The amount of interference suppression versus LPF bandwidth (FLPF) is summarized in Table A.2. With larger FLPF, smaller delay is introduced, and the interference suppression is increasing. To compensate the delay of the control signal, a delay block can be added before the input of NIS sub-block. With the corresponding delay compensated, the interference suppression is decreasing when FLPF is increasing, as more intermodulation error is allowed to the control signal. Nevertheless, the delay block is not easy to implement at RF frequency for a wideband operation. Therefore, the main limitation of interference suppression is still the amplitude discrimination between the large interferer and the weak signal.

A.6 NIS Operation under Multiple Large Interferers

In section A.4 and section A.5, the working principle of NIS is modeled and analyzed if one local large interferer or one external large interferer is present.

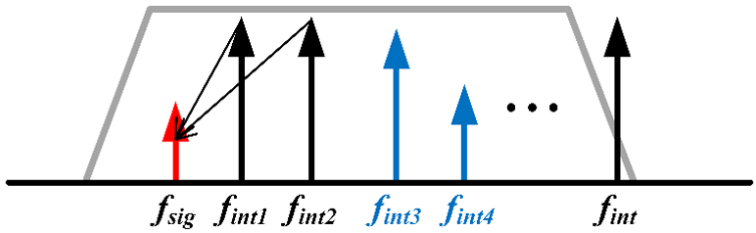

Figure A.24.: Illustration of NIS operation principle with multiple large interferers accompanying weak desired signal (red). The interferers includes local interferers (black) and external interferers (blue).

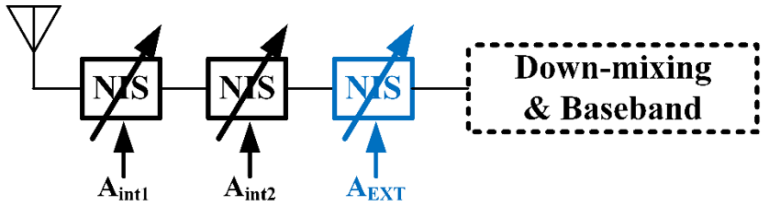

Figure A.25.: Illustration of NIS operation principle with NIS blocks for each local large interferer.

In this section, the interference scenario that multiple large interferers, either locally or externally generated, is encountered. The working principle of NIS under such interference scenario is discussed here.

The interference scenario is shown in Fig. 24, in which multiple interferers are present. The weak desired signal is shown in red (f_{sig}), the local interferers are shown in black and usually are the dominant signal (f_{int1} and f_{int2}), and external interferers are shown in blue (f_{int3} and f_{int4}). The grey line indicates the RF bandwidth of a NIS receiver system. In this case, the worst scenario is that the two large local interferers INT1 and INT2 saturate the receiver, and the 3rd intermodulation (IM3) product between them is exactly located on the desired signal frequency. Besides, although external interferers INT3 and INT4 are not as powerful as local interferers, they may also saturates the receiver chain.

The NIS operation principle under multiple interferers is illustrated in Fig. 25. The local interferers are dominant interferers so they should be filtered out first. Since the local interference envelope is prior-known information, one NIS circuit block can be enabled for suppressing each corresponding local interferer. Therefore the NIS operation prevents the receiver from saturation.

The influence of IM3 product on signal distortion is not alleviated as it happens before the large interferers are suppressed and the NIS operation relies on nonlinear transfer function. On the other hand, for receiver or RF circuit,

once the IIP3 is known, the IM3 at any other power level can be calculated. For every 1-dB increase of the IIP3 point, the corresponding IM3 product drops by 3 dB [18]. Based on Eqn. (A.18), the nonlinear zig-zag transfer function based receiver has an IIP3 10 dB higher than the interferer envelope amplitude A_{LS}, which should help lower the IM3 product amplitude.

Besides, the nonlinear receiver can implement frequency-translational filtering techniques at mixer and baseband stage, as shown in Fig.A.5 and Fig.A.6. Therefore, besides amplitude-domain filtering at the RF stage, the receiver also has frequency-domain filtering at mixer and baseband stage. The frequency selectivity at the RF input depends on LO frequency sweeping range and baseband filtering order. That helps alleviate the IM3 problem, depending on the frequency spacing between the wanted signal and interferers.

A final NIS circuit block can be enabled if there are still large external interferers exist. Since the external interferers are usually smaller in power compared with the local ones, it is only necessary to deal with the dominant external interferer. The envelope extraction circuit block will extract the envelope of the dominant external interferer, and feed it to the NIS circuit block to partially suppress the external interferer, as discussed in section A.5. In this way, the influences of large interferers are largely alleviated.

A.7 Conclusion

The nonlinear receiver with adaptive nonlinear transfer function has been proposed for multi-radio coexistence problems in wideband receivers. It relies on the amplitude information of the interference signal and enables frequency-independent filtering, thus improving in-band and out-of-band linearity for wideband operation. With the nonlinear method, the interference suppression is achieved at the RF stage, which relieves the requirement and power consumption for the following circuitry in the receiver chain. With this method, the interference envelope should be tracked continuously to adjust the nonlinear transfer function accordingly. An adaption method for envelope extraction is proposed and co-simulated with the RF receiver. The limitations for interference suppression are identified. From the analysis, the main limitation of interference suppression is the amplitude discrimination between large and weak signals. In the situation of external interference suppression, the accuracy of the extracted envelope is affected by the LPF filter. Therefore the input frequency separation and bandwidth limit the performance of interference suppression. From system level simulation, a large interference suppression is achieved, and positive SIR can be achieved at the input of baseband ADCs. Therefore the ADC resolution requirement is relaxed and the aliasing product is alleviated.

Competing Interests

The authors declare that there are no competing interests.

Acknowledgment

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B

A Wideband Envelope Detector with Low Ripple and High Detection Speed

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Abstract - In this paper, a new envelope detector design in a 40nm CMOS technology is presented. The design employs quadrature signal generation and 2nd harmonic cancellation to reduce output ripple while achieving high detection speed at the same time. The envelope detector operates from 500MHz to 6GHz with a detection speed of 250 MHz. It achieves less than 2% ripple, 0.64 ns delay and consumes 76.9 uW. With the achieved results, it is suitable for use in a nonlinear interference suppression receiver, enabling more than 25 dB of suppression.

Keywords - envelope detector, quadrature generation, harmonic rejection, interference suppression.

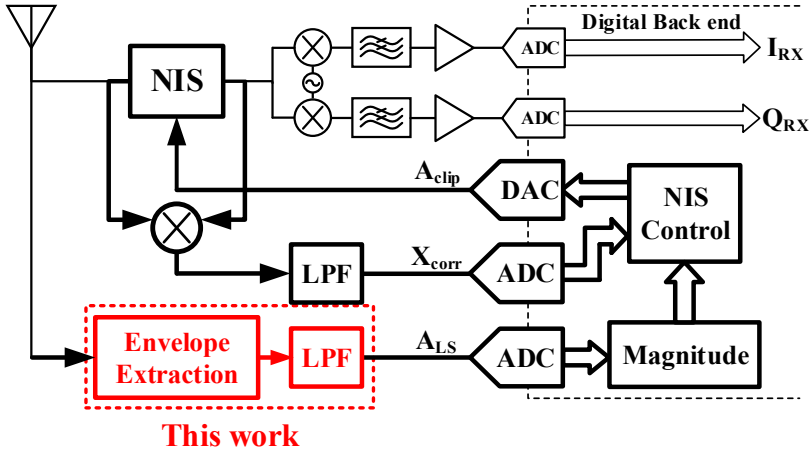

Figure B.1.: System architecture of the NIS receiver.

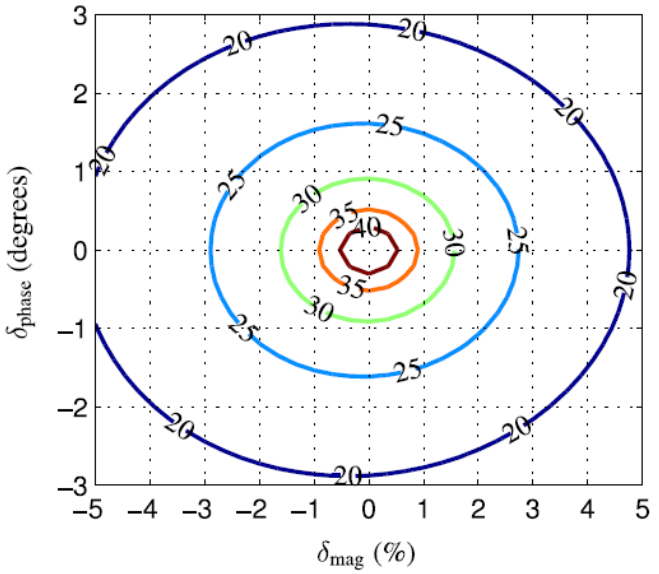

Figure B.2.: Strong-signal suppression versus error in A_{clip}.

B.1 Introduction

Wireless communication systems are continuously developing to increase data rate with high reliability. Envelope detectors used in applications such as radio frequency (RF) transceivers and pre-distortion techniques should meet the bandwidth requirement to track wide-bandwidth modulated signals.

Fig. B.1 shows a nonlinear interference suppression (NIS) receiver architec-

ture [94] aimed for RF coexistence. The NIS receiver makes use of a nonlinear circuit [6] to suppress strong undesired signals and amplify the weak desired signals. The envelope of the strong interferers is tracked so that interferers with varying envelope amplitude can be suppressed. The strong signal suppression versus error in the extracted envelope is shown in Fig. B.2. Therefore for this application, the envelope detector should provide as small phase and amplitude error as possible, i.e., high accuracy and low delay.

Envelope detector circuits are mostly composed of a rectifier stage and a low-pass filter (LPF) stage [76, 95–97]. The transistors are biased in weak inversion to exploit the exponential transfer. LPFs are placed at the output to filter out the harmonic components either at ω_{RF} or ω_{2RF}. The choice of the LPF cutoff frequency brings a trade-off between detection speed and accuracy. Small bandwidth provides better harmonic filtering, while the speed is low. Large bandwidth however introduces more error since the lack of harmonic filtering. To overcome this trade-off, a new envelope detector topology with quadrature signal generation and 2nd harmonic cancellation is proposed in this paper.

The paper is organized as follows. Section B.2 presents the proposed envelope detector topology and circuits. Simulation results and comparison to state of the art are shown in section B.3. Finally, conclusions are given in section B.4.

B.2 Envelope Detector Topologies

B.2.1 Proposed Envelope Detector with 2nd Harmonic Cancellation

The proposed envelope detector topology is shown in Fig. B.3. It is composed of quadrature signal generation, square operation, 2nd harmonic cancellation and a LPF stage. When a signal is applied at the input, the quadrature signal generation creates two replica signals with a 90^o phase difference. The I and Q signals pass through the square operation. Then, the two signal paths are combined at the output with 2nd harmonics cancelled out and fed to the filter. Because the 2nd harmonic component is removed, the requirement for the LPF bandwidth is relaxed. Therefore, the optimization for detection speed and accuracy can be achieved at the same time.

The proposed topology shown in Fig. B.4 utilizes Pythagorean Identity that $sin^2\theta + cos^2\theta = 1$. First, assume an input signal, $Acos(\omega t)$, $A = 1$ for simplicity and assign $\theta = \omega t$. Thus the input signal and its square term can be expressed as

$$\begin{cases} cos\theta & = \frac{1}{2}(e^{j\theta} + e^{-j\theta}) \\ cos^2\theta & = \frac{1}{2} + \frac{1}{4}(e^{j2\theta} + e^{-j2\theta}) \end{cases} \tag{B.1}$$

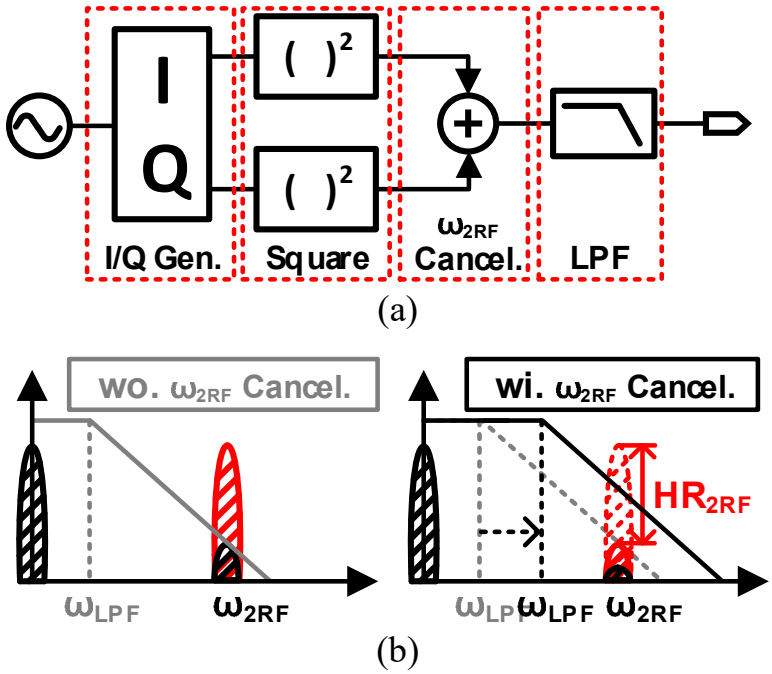

Figure B.3.: (a) Proposed new envelope detector topology with quadrature generation, square operation, and 2nd harmonic cancellation and LPF. (b) Output spectrum comparison between conventional and proposed topology.

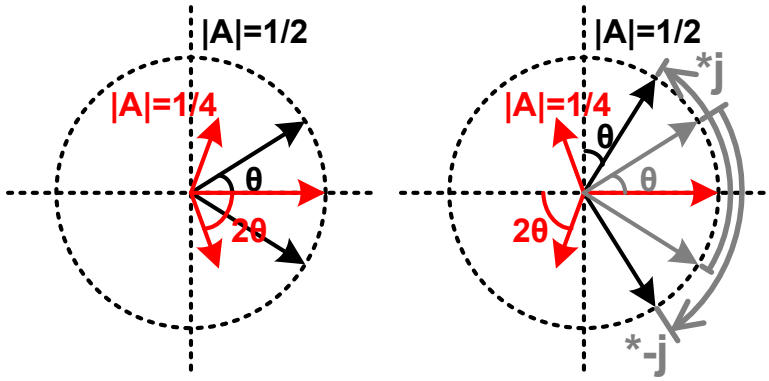

Figure B.4.: Explanation of 2nd harmonic rejection ($sin^2\theta + cos^2\theta$) in complex plane.

The square output contains component at 0^o and $\pm 2\theta$. The quadrature signal

is achieved by multiplying $e^{j\theta}$ by and $e^{-j\theta}$ by -j,

$$\begin{aligned} cos(\theta - 90^o) &= \frac{1}{2}\left(e^{j(\theta-90)} - e^{-j(\theta-90)}\right) \\ &= \frac{1}{2j}\left(e^{j\theta} - e^{-j\theta}\right) = sin\theta \end{aligned} \tag{B.2}$$

And the quadrature square term is

$$\begin{aligned} cos^2(\theta - 90^o) &= \frac{1}{2} - \frac{1}{4}\left(e^{j2\theta} + e^{-j2\theta}\right) \\ &= \frac{1}{2} + \frac{1}{4}\left(e^{j(\pi+2\theta)} + e^{(\pi-j2\theta)}\right) = sin^2\theta \end{aligned} \tag{B.3}$$

After combining the two square terms, only the components at 0^o get doubled while the components at $\pm 2\theta$ get cancelled out. Therefore, the square sum of input $Acos(\omega t)$ and its quadrature signal only contains DC component (envelope amplitude), while 2nd harmonics at 2ω are cancelled out.

B.2.2 Full-wave Rectifier Circuit

Fig. B.5(a) presents the proposed differential rectifier circuit. Transistor M_2 and M_3 are biased in weak inversion to rectify the input signal. Transistor M_0 and M_1 are diode-connected to provide a relatively low input impedance.

The drain current of M_2 biased in weak inversion is

$$I_{d,M2} = I_0 e^{\frac{V_G - V_{th}}{nV_T}} \left(e^{\frac{-V_S}{V_T}} e^{\frac{-v_i^+}{V_T}} - e^{\frac{-V_D}{V_T}} \right) \xrightarrow{small-signal} I_Q e^{\frac{-v_i^+}{V_T}} \tag{B.4}$$

where $I_Q = I_0 e^{\frac{V_G - V_{th}}{nV_T}} e^{\frac{-V_S}{V_T}}$ denotes the quiescent current, V_T the thermodynamic voltage kT/q, V_{th} the threshold voltage and n is the slope factor [75].

The 2nd order term of the power series expansion of Eqn. (B.4) is [76]

$$i_{2nd} = \frac{I_Q {v_i^+}^2}{2V_T^2} \tag{B.5}$$

Applying a single-tone $v_i^+(t) = (A/2)sin(2\pi f_{in} t)$, the output is given by,

$$i_{2nd} = \frac{I_Q A^2}{8V_T^2}\left[1 + cos(2\pi(2f_{in})t)\right] \tag{B.6}$$

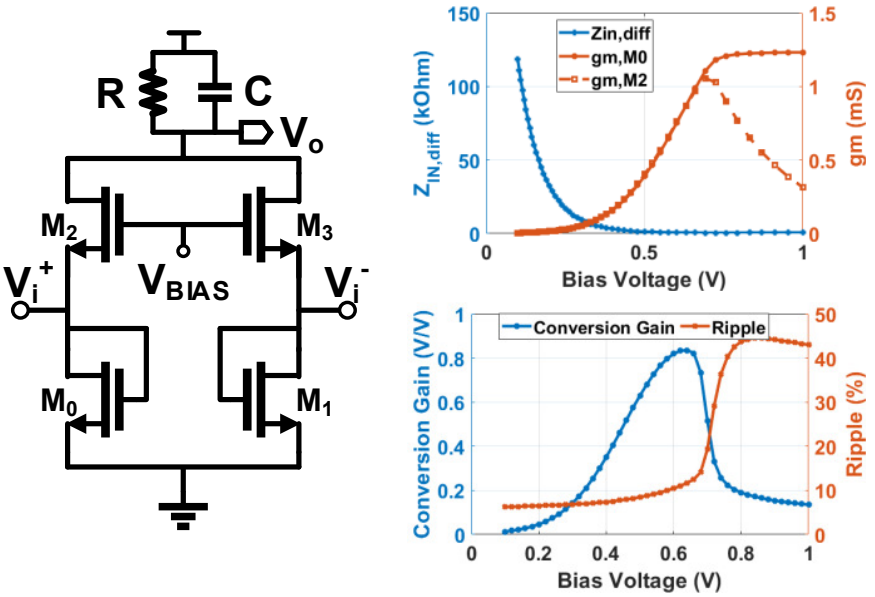

Figure B.5.: (a) The schematic of proposed full wave rectifier circuit. (b) $g_{m,M0}$, $g_{m,M2}$ and differential input impedance, conversion gain and ripple versus bias voltage of $M_{2,3}$ with 100mV input signal at 2GHz.

We can define single-tone conversion gain and ripple that

$$G_{conv}(A) = \frac{I_Q A R}{8 V_T^2}$$
$$Ripple = \frac{i_{2nd2\omega} \cdot H_{LPF}(\omega)}{i_{2ndDC} \cdot R} \tag{B.7}$$

where G_{conv} is a function of input amplitude and ripple purely depends on LPF transfer.

The relation of input impedance and transistor g_m, G_{conv}, Ripple versus bias point are shown in Fig. B.5(b). For reasonable G_{conv} and small Ripple, the transistor should be biased in weak inversion region.

The relation of G_{conv} and Ripple on input amplitude is shown in Fig. B.6(a) for different biasing voltage. The biasing voltage depends on the targeting dynamic range. Two tone simulation results on detection speed are shown in Fig. B.6(b).

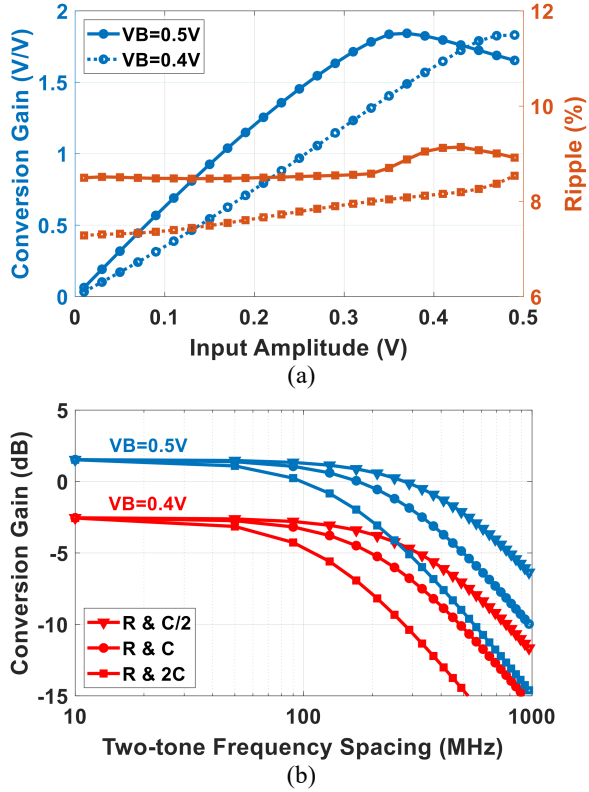

Figure B.6.: (a) Conversion gain and ripple as a function of input amplitude. (b) Two-tone tests with different RC configuration.

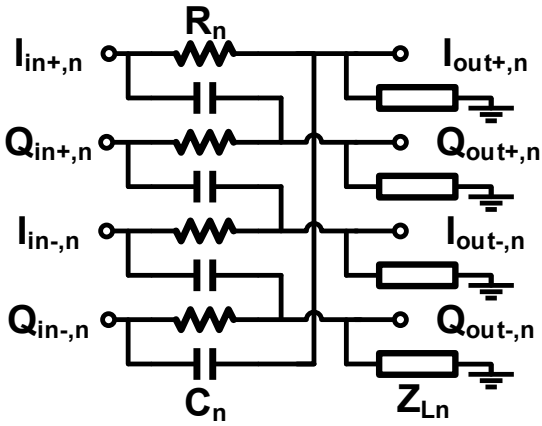

Figure B.7.: An n^{th} PPF stage with load impedance Z_{in} of the following circuitry.

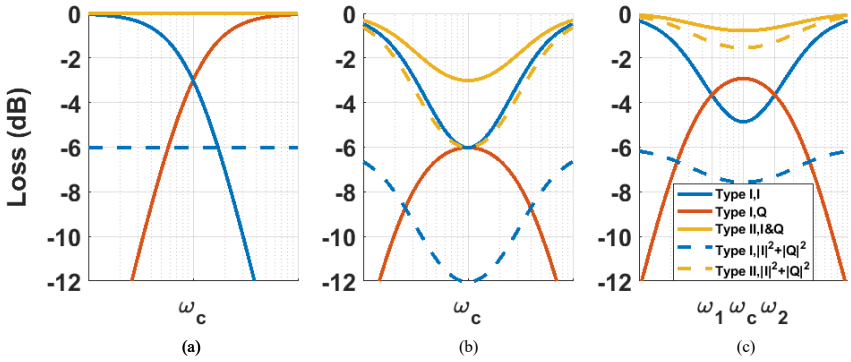

Figure B.8.: Loss of Type I/II (a) a single stage PPF (b) a two-stage PPF with equal pole frequency ω_C (c) a two-stage PFF with unequal pole frequency ω_1 and ω_1, $\omega_C = \sqrt{\omega_1\omega_2}$ (assuming zero source impedance and infinite load impedance).

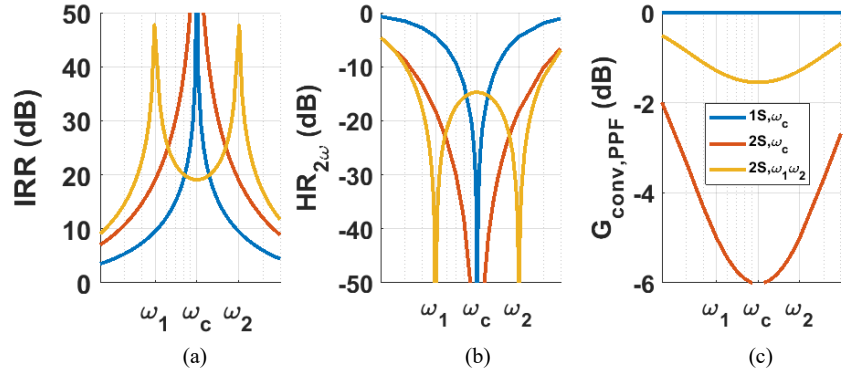

Figure B.9.: Comparison between single stage (blue), two-stage with equal pole frequency ω_C (red) and two-stage with unequal pole frequency ω_1 and ω_2 (yellow) of Type II PPF on (a) HRR (b) $HR_{2\omega}$ (c) $G_{conv,PPF}$.

B.2.3 Quadrature Signal Generation

Polyphase filters (PPF) [75] are used for quadrature signal generation in the proposed envelope detector topology. An n^{th} PPF stage is shown in Fig. B.7.

The frequency response of outputs of PFFs with different configurations are plotted in Fig. B.8(a)-(c). Type-II PPFs have less loss compared with Type-I PPFs. PPFs with unequal pole frequencies have less loss compared with equal pole frequency.

The sum of square of the magnitude of the output responses, $|I|^2 + |Q|^2$ are also shown in Fig. B.8(a)-(c), dash blue for Type-I and dash yellow for Type-II. Similar conclusions are drawn.

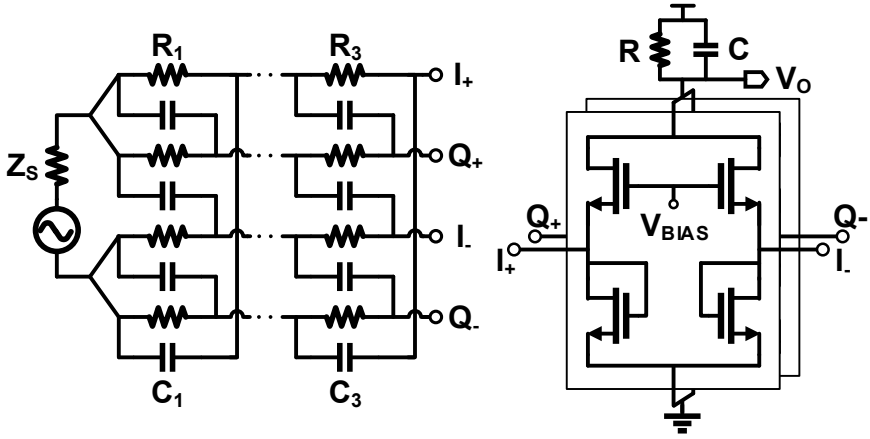

Figure B.10.: The schematic of the proposed envelope detector topology with quadrature generation and 2nd harmonic rejection.

The image rejection ratio (IRR) of different PPFs are shown in Fig. B.9(a) (equal for Type-I/II). It is observed that the bandwidth of a two-stage PPF is larger than single-stage PPF. The bandwidth of two-stage PPF with unequal pole frequencies is wider than that with equal pole frequency.

$$\Delta V_{Iout,ns}^{II}{}^2 + \Delta V_{Qout,ns}^{II}{}^2 = \begin{cases} \frac{|H_{I,ns}^{II}(j\omega)|^2+|H_{Q,ns}^{II}(j\omega)|^2}{2}, & DC \\ \frac{[H_{I,ns}^{II}(j\omega)]^2+[H_{Q,ns}^{II}(j\omega)]^2}{2}, & 2\omega \end{cases} \tag{B.8}$$

$$\Delta V_{Iout,ns}^{II}{}^2 + \Delta V_{Qout,ns}^{II}{}^2 = 2\left(\Delta V_{Iout,ns}^{I}{}^2 + \Delta V_{Qout,ns}^{I}{}^2\right) \tag{B.9}$$

The output of the proposed envelope detector, assuming an ideal rectifier, can be expressed by the sum of square of the output responses, $I^2 + Q^2$ in (B.8)(B.9). The DC component represents the conversion gain and the 2nd harmonic residue can be defined as $HR_{2\omega}$. The simulation results are shown in Fig. B.9(b)(c), respectively. The results for $HR_{2\omega}$ are similar as IRR and the results for $G_{conv,PPF}$ are the same as $I^2 + Q^2$ plotted in Fig. B.8(a)-(c) (dash yellow).

Therefore the influences of PPF choices on $HR_{2\omega}$ and $G_{conv,PPF}$ can be characterized by IRR and I,Q output responses. Also note that the actual source and load impedance will greatly influence the PPF behavior [75].

B.2.4 2nd Harmonic Cancellation

The complete envelope detector circuit is shown in Fig. B.10. It consists of a three-stage Type-II PPF and two replica of full-wave rectifier circuits for I and

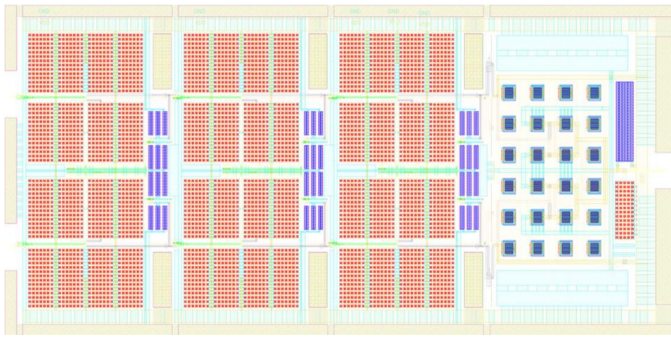

Figure B.11.: The layout of the proposed envelope detector.

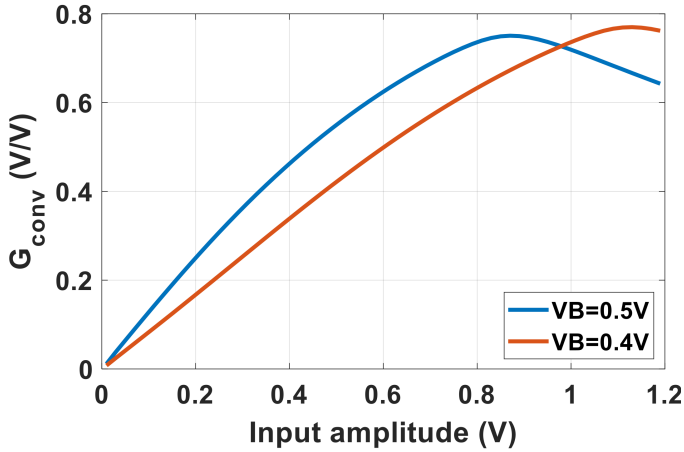

Figure B.12.: Conversion gain versus input amplitude with bias voltage of 0.5V and 0.4V.

Q path. The 2nd harmonic cancellation happens when the current outputs of I and Q path rectifiers are combined. A pole splitting factor of 2.88 was used in the PPF to provide more than 20 dB of in band $HR_{2\omega}$.

B.3 Simulation Results

The proposed envelope detector circuit was implemented in a 40nm CMOS technology. The layout is shown in Fig. B.11. It occupies 180 um by 88 um. The power consumption of the envelope detector is 76.9 uW.

Fig. B.12 shows the simulated conversion gain of the envelope detector when driven with a constant envelope signal. The conversion gain increases linearly and compresses at 0.8V and 1V input amplitude for biasing voltage of 0.5V and 0.4V respectively, which corresponds to an input power of 8 and 10

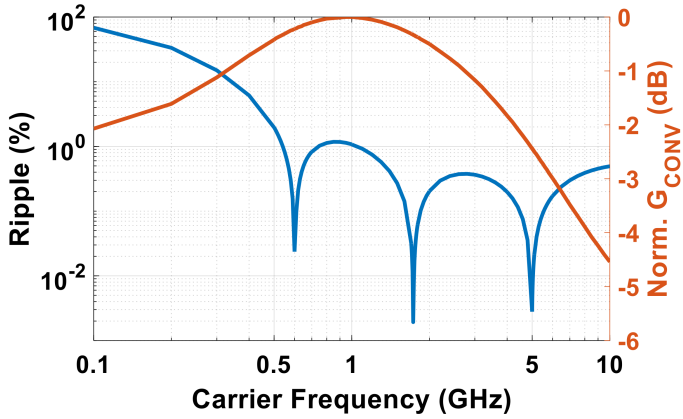

Figure B.13.: Normalized conversion gain (red) and simulated ripple with an input voltage of 100mV (blue).

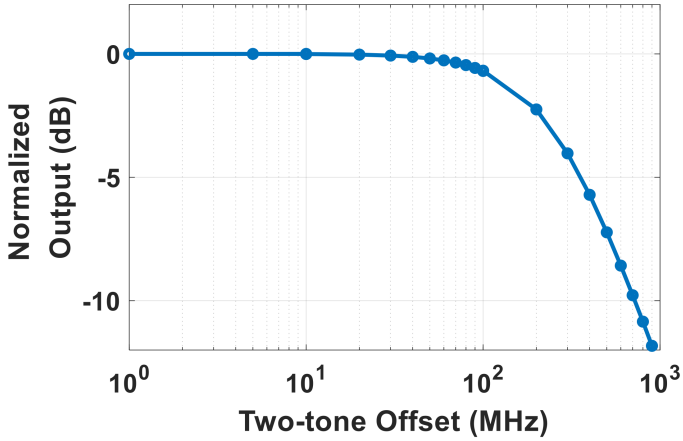

Figure B.14.: Simulated output magnitude (normalized) in a two-tone test. The input was 100mV for each tone.

dBm in a 50 Ohm impedance environment.

Fig. B.13 illustrates the normalized frequency response and ripple for an input amplitude of 100mV. The upper limit of 3dB operating frequency reaches 6GHz . The lower limit is set by the requirement of ripple, which is below 2% starting from 500MHz and below 1% from 1GHz, limited by $HR_{2\omega}$.

The normalized magnitude of the output voltages versus offset frequencies is shown in Fig. B.14. It was simulated with a two-tone input signal, with 100mV amplitude for each tone. The detection bandwidth is around 250MHz, which is close to the designed LPF bandwidth and meets the bandwidth requirement of most communication standards.

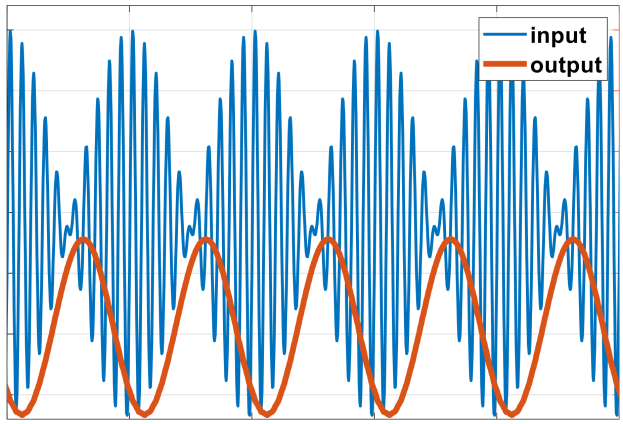

Figure B.15.: Simulated input and output waveforms of the proposed envelope detector topology.

Table B.1.: Summary and Comparison with Other Works

Ref.	[95]	[96]	[76]	[97]	This work
Technology	0.18um	0.18um	90nm	0.13um	40nm
Carrier Frequency	100Hz - 1.6GHz	1GHz - 6GHz	2.4GHz	0.2GHz - 4.2GHz	0.5GHz - 6GHz
Ripple	N.A.	N.A.	N.A.	1dB*	2%
Detection Speed	5kHz	5MHz	5MHz	190MHz	250MHz
Delay	N.A.	N.A.	N.A.	N.A.	0.64ns
Power	6.3mW	1.8mW	3uW	25mW	76.9uW

*The paper reports a ± 1 dB of detection error within the dynamic range, which includes ripple at the output and the nonlinearity of conversion gain.

Finally, the input and output waveforms of the envelope detector are shown in Fig. B.15. The input is a two-tone signal of 200mV amplitude for each tone and an offset frequency of 200 MHz at 2GHz carrier frequency. The delay is 0.64 ns. With the achieved results of the proposed envelope detector, the NIS receiver could provide more than 25 dB of suppression to large interferers. The performance of the proposed envelope detector and comparison with state of the art are summarized in Table B.1.

B.4 Conclusion

An envelope detector with quadrature signal generation and 2nd harmonic cancellation has been designed in a 40 nm CMOS technology. The envelope detector operates from 500MHz to 6GHz and achieves less than 2% ripple and

0.64 ns delay. It consumes 76.9 uW power consumption from a 1.1V power supply. By applying it to the NIS receiver, more than 25 dB of interference suppression can be achieved.

C

A Reconfigurable Receiver with 38 dB Frequency-Independent Blocker Suppression

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Abstract - This paper presents a reconfigurable receiver with frequency-independent blocker suppression in a 40nm CMOS technology. In linear mode, the receiver achieves an in-band B1dB of -25.7 dBm at 1MHz offset with 34 dB gain setting. In nonlinear mode, blocker suppression is achieved by dynamically adapting a nonlinear transfer function according to the blocker amplitude. In the presence of a 0 to 9.6 dBm blocker, the receiver provides more than 38 dB of frequency-independent suppression, while consuming 8.7-15.7 mW in the RF stage. The maximum attainable blocker level exceeds PDC-5dB. The measured in-band B_{1dB} is from -2.8 to 8 dBm at 1MHz offset for different settings. The measured blocker NF is 15.47 dB with a 1.95 dBm blocker.

Keywords - Full duplex, in-band linearity, reconfigurable receiver, nonlinear interference suppression.

C.1 Introduction

The sub-6GHz RF spectrum has become increasingly crowded with wireless standards for higher data rate and link capacity. This development has led research efforts to explore spectral-efficient wireless systems such as software-defined radios (SDR), reconfigurable receivers and full duplex (FD). However, a major challenge in these systems is the lack of RF filtering, especially for strong in-band (IB) interferers, such as transmitter (TX) leakage and external IB interferers. These interferers bring problems such as RX desensitization, noise figure (NF) degradation and reciprocal mixing. Therefore, the tolerance of strong IB interference requires large IB linearity, which typically demands a large power consumption.

Frequency translational filtering techniques have been proposed for suppressing out-of-band (OOB) interferers [98, 99]. Furthermore, thermal noise [27] and phase noise cancellation [29] techniques were adopted to lower the NF. However, these frequency-domain approaches fail at in-band interferers, due to the limited achievable quality factor.

In [100], an active canceller circuit provides suppression to TX leakage, but the cancellation bandwidth is limited. In [6], a unique RF amplifier with nonlinear interference suppression (NIS) technique was proposed. It enables frequency-independent filtering by dynamic adaption of a nonlinear transfer function according to interferer amplitude. However, these active techniques only deal with self-generated interferers.

In this paper, a reconfigurable wideband receiver is proposed that enables frequency-independent filtering with more than 38 dB suppression for a 0 – 9.6 dBm blocker, an in-band blocker 1dB compression point (B_{1dB}) of -2.8 – 8 dBm at 1MHz offset, while consuming only 8.7 – 15.7 mW in the RF stage. Compared with [6], this NIS technique is here extended and applied to a folded Gilbert structure for achieving blocker suppression over a larger power range with lower power consumption. The maximum attainable blocker level exceeds PDC-5dB. Since the suppression is performed at RF, NF degradation due to reciprocal mixing is alleviated. It exhibits 15.47 dB NF with a 1.95 dBm blocker, together with a phase noise of -155 dBc/Hz at 20 MHz offset from the on-chip divider. The RX system is developed to suppress strong self-generated and external interferers based on the amplitude extracted at the antenna.

The paper is organized as follows. In section C.2, the nonlinear interference suppression concept is introduced and the proposed receiver system is described. The circuit implementation is presented in Section C.3. Measurement results are provided in section C.4. Conclusions are drawn in Section C.5.

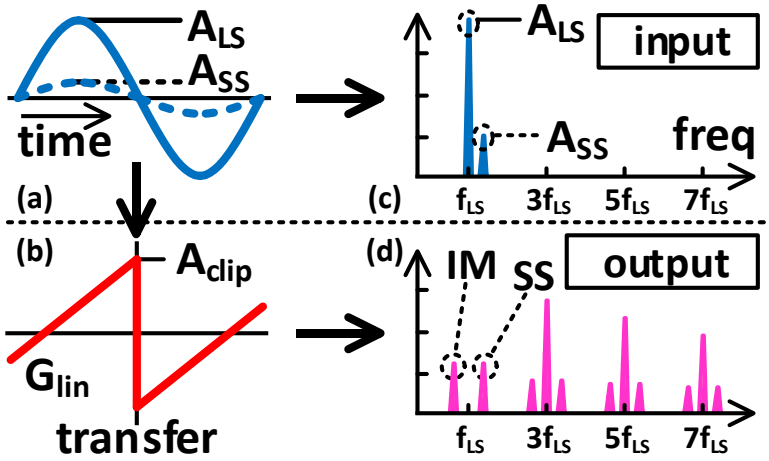

Figure C.1.: The zig-zag nonlinear transfer function (b) and its effect on the combination of a strong and weak signal (a) in frequency domain (c, d).

C.2 Nonlinear Interference Suppression System

C.2.1 Nonlinear Interference Suppression (NIS) Concept

Since nonlinear transfers do not obey the principle of superposition, a weak desired signal and strong interference at the input can undergo different operations simultaneously [94].

An illustration of the concept is shown in Fig. C.1. The input is a combination of a strong interference with amplitude A_{LS} and a weak desired signal with significantly smaller amplitude A_{SS}. The input signal is passing through a zig-zag transfer function, where A_{clip} is the clipping amplitude and G_{lin} is the slope of the linear region. The fundamental output of the strong interference is completely suppressed if the clipping amplitude A_{clip} fulfills

$$A_{clip} = \frac{\pi}{4} A_{LS} G_{lin} \tag{C.1}$$

The weak desired signal experiences a linear gain equal to $G_{lin}/2$. Due to strong nonlinearity of the zig-zag function, the output spectrum contains intermodulation products and harmonics of the input signals, which can be filtered by the following down-conversion and baseband circuitry.

The clipping amplitude Aclip must be dynamically adjusted when the envelope of the strong interference is changing, i.e. in the case of amplitude-modulated interferers.

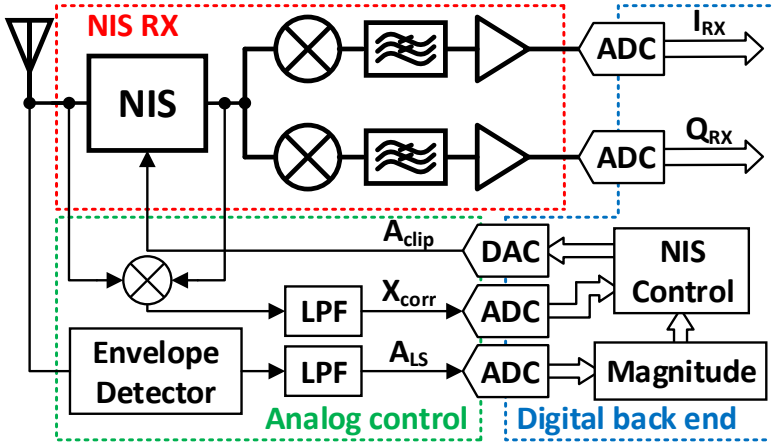

Figure C.2.: NIS-based RX system architecture for general interference suppression at the receiver input.

C.2.2 NIS-Based Receiver System Architecture

In Fig. C.2, the NIS-based receiver system is proposed to deal with strong self-generated and external interference at the receiver input. The system consists of the LNA, NIS RX, Analog Control and Digital Back End.

The system operation can be separated into small- and largesignal operation modes. For small-signal operation, the NIS RX works in linear mode and the LNA is switched on for lower NF. For large-signal operation when strong blocker is present, the LNA is switched off and the NIS RX operates in nonlinear mode. The Analog Control and Digital Back End adapt the NIS transfer according to the blocker amplitude while the NIS RX performs strong interference suppression and desired weak signal amplification.

The Analog Control part consists of a feedforward path and a feedback path. The feedforward path provides the envelope amplitude information extracted at the antenna by the envelope detector with a detection speed of hundreds of MHz [101]. Since it contains both the envelope of the wanted signal and the interferer, complete suppression only applies when the interferer is much stronger than the wanted signal.

The feedback path provides cross-correlation between the input and output of the NIS sub-block by a mixer. This path has two functions. First, it corrects the error introduced by the feed-forward path. Second, it makes sure that the large signal is suppressed. A minimal cross-correlation is ensured through iterative adjustment of the NIS transfer via A_{clip}.

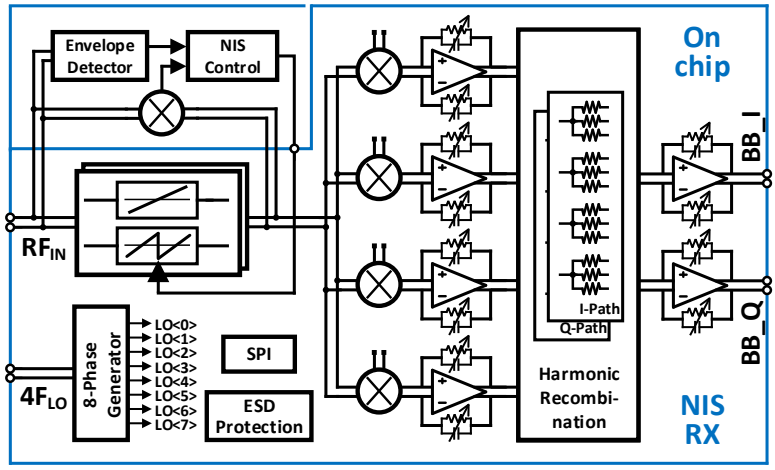

Figure C.3.: Simplified block diagram of the NIS-based RX, 8-path mixer, transimpedance amplifier (TIA) and harmonic recombination.

C.3 System Implementation

C.3.1 Receiver Diagram

The simplified block diagram of the proposed NIS RX is shown in Fig. C.3. The receiver is designed to utilize current-mode circuit. The RF stage is an NIS-based transconductance amplifier that has two operation modes, linear mode as a variable gain amplifier and nonlinear mode for interference suppression. The nonlinear mode is enabled when strong blocker is present so that the circuit will perform simultaneous frequencyindependent blocker suppression and weak signal amplification.

As shown in Fig. C.1, the nonlinear transfer output contains strong 3rd and 5th harmonics. An 8-phase passive mixer is used here to avoid noise folding from the harmonics. Harmonic recombination is enabled at baseband using resistive networks with a ratio of 29:41:29. The feedback capacitors and resistors of the transimpedance amplifiers (TIA) are reconfigurable for tuning gain and IF bandwidth.

C.3.2 NIS-based RF Transconductance Amplifier

The nonlinear transfer should be symmetric and have at least three zero crossings for the desired NIS function [94]. Differential pairs can be utilized to create such transfers, as shown in Fig. C.4(a). With a bias difference of $2V_C$ at the input, the transition is shifted towards negative by $2V_C$. For different connections of three differential pairs with bias differences of zero, $2V_C$ and

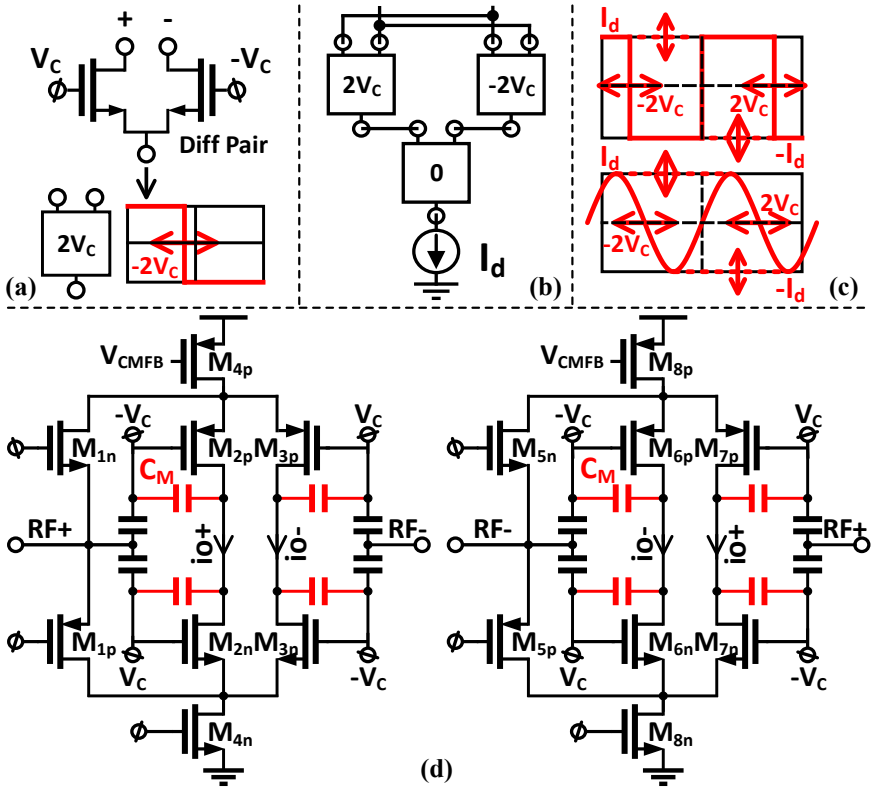

Figure C.4.: (a) Differential pair and its transfer, (b) a Gilbert-cell topology with V_C and I_d and (c) corresponding transfer in ideal (top) and implementation (bottom), (d) proposed NIS-based RF transconductance amplifier.

$-2V_C$, a nonlinear transfer can be created as required.

The Gilbert-cell structure with a tail current source I_d is shown in Fig. C.4(b). The power consumption is reduced by current reuse. Furthermore, the nonlinear transfer function can be adjusted by both V_C and I_d for different blocker power to achieve optimum performance of blocker suppression, small signal gain, NF, and power efficiency at the same time. The corresponding transfer function is shown in Fig. C.4(c) for the ideal case and for real implementation.

The proposed NIS-based RF transconductance amplifier is shown in Fig. C.4(d), using a differential and complementary folded Gilbert-cell structure. Transistors M_{1p} and M_{1n} make up a common gate (CG) input stage to provide wideband matching and convert the input voltage to current. M_{4p} and M_{4n} are variable current sources and provide high impedance nodes. The input ac current is then fed into two differential pairs composed of M_{2p} and M_{3p}, M_{2n} and M_{3n} with a bias difference of $-2V_C$ and $2V_C$, respectively. Transistors

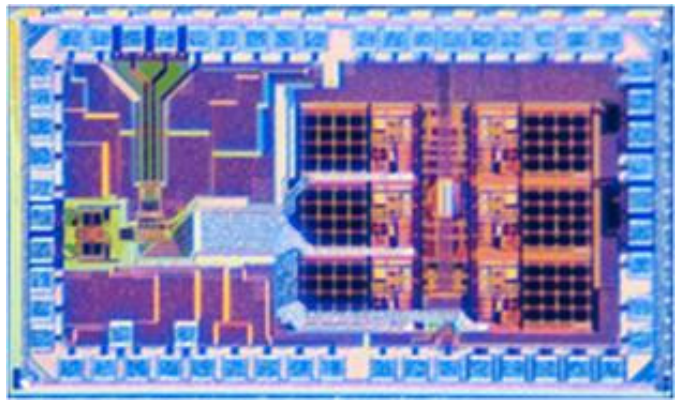

Figure C.5.: Die photo of the fabricated NIS RX using a 40nm CMOS technology.

M_{5-8} make up the other differential part of the circuit. Capacitor C_M is used to compensate the pole introduced at the drain of the current sources. Therefore, the ac current at source, and the input voltage at the gate of the differential pairs are matched so that maximum suppression can be achieved.

In the nonlinear mode, V_C is positive so that the nonlinear transfer can be created as required. The current sources $M_{4,8}(I_d)$ has two current settings. The values of V_C and I_d are updated according to the blocker power for an optimum overall performance. In the linear mode, V_C is assigned negative so that the out-of-phase branches (M_{2p} and M_{6p}) are switched off with negligible gain reduction and noise contribution to the circuit.

C.4 Measurement Results

The NIS RX chip is fabricated in a 40nm CMOS technology and the die photograph is shown in Fig. C.5. The total area including bond pads is 1.67 mm^2. The on-chip divider-by-4 works up to 11 GHz input frequency and achieves -155 dBc/Hz at 20 MHz offset. The dynamic power consumption of the divider is 12 mW at fLO=1.5 GHz. The TIAs consume 16.2 mW from a 1.1V supply.

C.4.1 Linear and nonlinear modes

Fig. C.6 shows the measured voltage conversion gain in the linear mode. The gain is reconfigurable from 17-53 dB and the IF bandwidth from 1-27 MHz. The 1dB compression point P1dB is -21dBm at 34 dB gain (TIA setting2). S11 is lower than 10 dB up to 2.7 GHz. The RF stage power consumption is 14 mW.

The nonlinear mode performance is shown in Fig. C.7, including the frequency-independent blocker suppression by the RF NIS stage and the corresponding

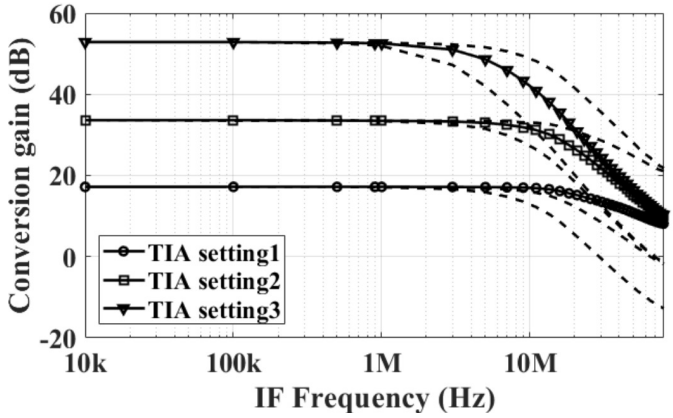

Figure C.6.: Conversion gain in linear mode with tunable gain from 17-53 dB and IF bandwidth from 1-27 MHz (selected settings 1,2,3 used in below).

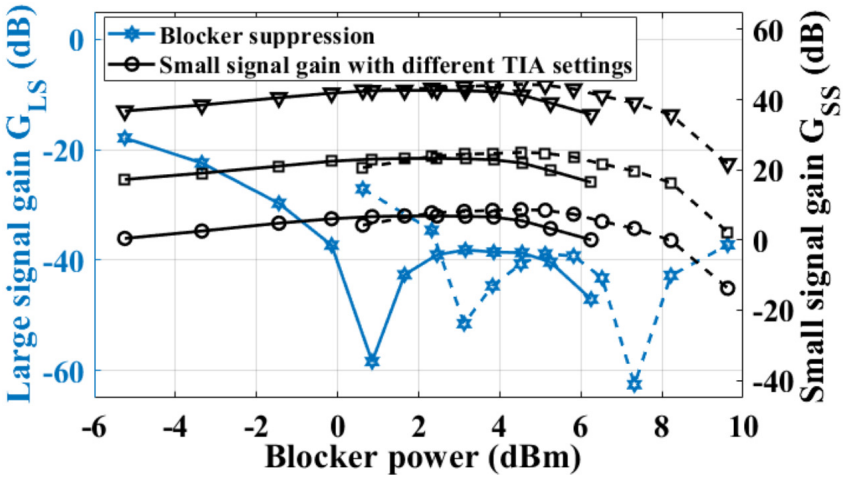

Figure C.7.: Frequency-independent blocker suppression by RF NIS stage and the small signal conversion gain measured with blocker located at f_{LO}+10MHz.

small signal conversion gain GSS. The IB blocker is located at f_{LO}+10MHz. The nonlinear mode has low-power and high-power mode with two current settings (I_d) and the suppression is achieved by changing VC for different blocker power in each current setting. The measured blocker suppression is more than 38 dB for a 0 – 9.6 dBm blocker, more than 20 dB for a -4.4 – 9.6dBm blocker and at 63 dB for a 7.3 dBm blocker. The power consumption of the RF stage is from 8.7 to 15.7 mW.

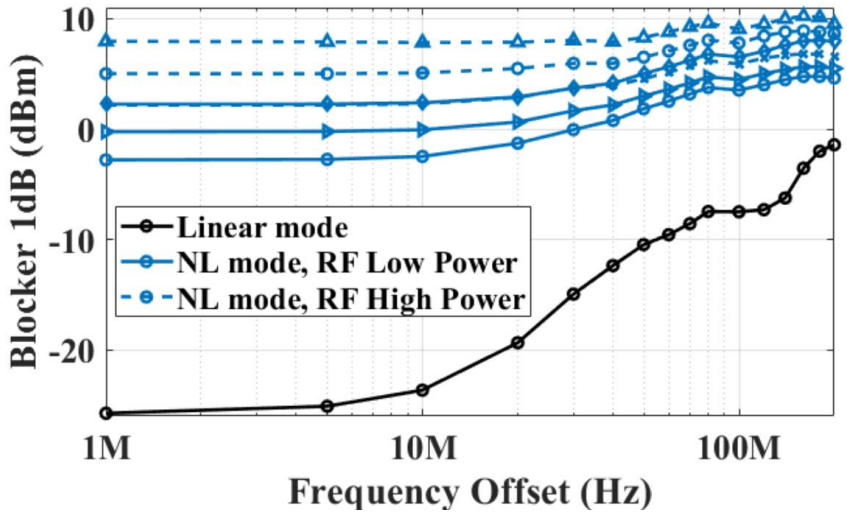

Figure C.8.: Measured blocker 1dB desensitization point (B1dB) with the blocker located at $f_{LO} + \Delta f$ with TIA setting2 shown in Fig. C.6.

C.4.2 Blocker 1dB compression point

The measured blocker 1dB (B_{1dB}) compression point in linear mode and nonlinear mode versus offset frequency is shown in Fig. C.8, using TIA setting2 as shown in Fig. C.6. The IB B_{1dB} at 1MHz offset is -25.7 dBm. The nonlinear mode B1dB is measured by sweeping blocker power at each V_C settings. The IB B_{1dB} at 1MHz offset ranges from -2.8 to 8 dBm for different VC values. Compared with linear mode, the nonlinear mode B_{1dB} is less dependent on offset frequency, but more dependent on the setting of blocker power (V_C & I_d), especially for IB frequency.

C.4.3 Blocker Noise Figure

The RX noise figure in the presence of a blocker is measured with the blocker located at f_{LO}+51MHz, as shown in Fig. C.9. The noise figure in linear mode degrades as blocker power increases due to gain compression and reciprocal mixing. In nonlinear mode, the noise figure is measured when the blocker experiences maximum suppression (V_C @ max. suppression). For blocker power larger than -4.3 dBm, the blocker noise figure in nonlinear mode is smaller than in linear mode, indicating that the influence of LO phase noise (-155 dBc/Hz @ 20 MHz) is much alleviated. It achieves 15.1 dB and 15.47 dB NF with a 0.65 dBm and 1.95 dBm blocker, respectively.

A receiver performance comparison is given in Table C.1. The power efficiency in the presence of a blocker is shown in Fig. C.10, indicating that

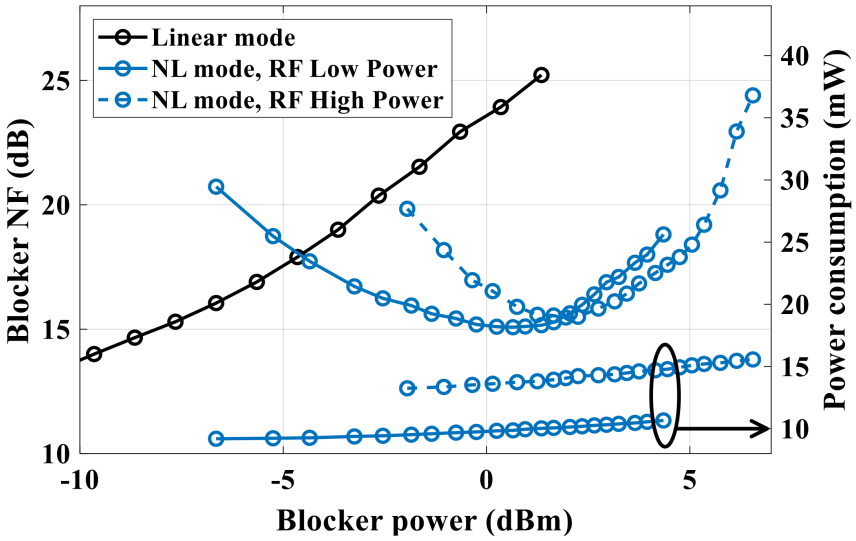

Figure C.9.: Measured receiver noise figure versus blocker power in linear mode and nonlinear mode, with blocker located at f_{LO}+51MHz.

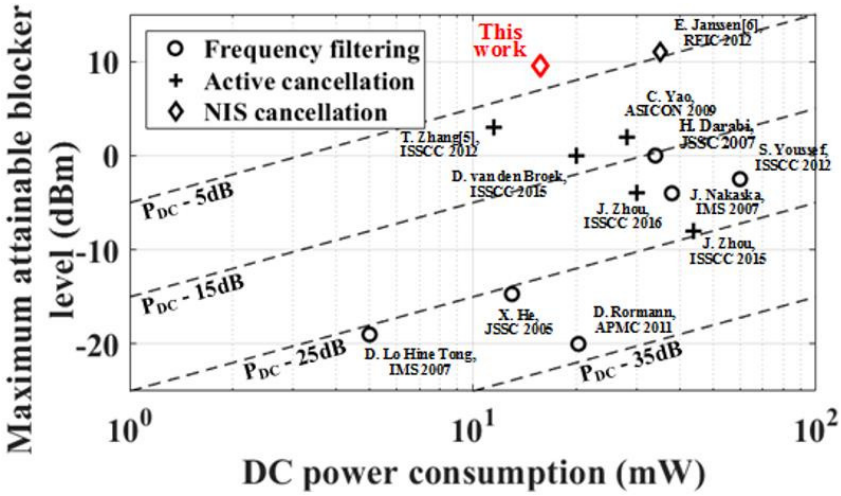

Figure C.10.: Maximum attainable blocker level versus power consumption. The 1dB compression point is used in case a maximum level is not specified.

only NIS cancellation technique exceeds the 'PDC-5dB' line. Compared with [6], the proposed NIS circuit maintains the maximal attainable blocker level at around 10 dBm while the power consumption is halved.

Table C.1.: Summary and Comparison Table

Reference	2017 RFIC [99]	2012 ISSCC [27]	2011 JSSC [24]	2017 ISSCC [100]	2015 ISSCC [29]	2012 RFIC [6]		This work	
Topology	Mixer First	Thermal NC	LNA + N-Path Filter	Adaptive filter, 2-path	Phase- and Thermal- NC	RF Amplifier		RF NIS + N-path	
						L	NL	Linear	Nonlinear
LO Generation	External	External	Integrated	Integrated	Integrated	N.A.		External	
Technology	45nm SOI	40nm	40nm	40nm	28nm	180nm		40nm	
Frequency (GHz)	0.2 - 8	0.08 - 2.7	0.4 - 6	1.7 - 2.2	0.2 - 3	1.85		0.5 - 2.7	
Blocker suppression (dB) Blocker power (dBm)	N.A	N.A	N.A	50 (BW=42MHz)	N.A.	30 / (0 ∼ 11dBm) 20 / (-3 ∼ 11dBm)		38 / (0 ∼ 9.6dBm) 20 / (-4.4 ∼ 9.6dBm)	
0dBm Blocker NF (dB) @ 80 MHz Offset (unless noted)	4.7 (0dBm) 9 (10dBm)	4.1 (0dBm) 13 (4dBm)	13 (0dBm) (Δ f=20MHz)	N.A.	5.5	12.8 (2dBm)		NL mode: @50MHz 15.1 (0.65dBm) 15.47 (1.95dBm) (-155dBc/Hz[##])	
0dBm Blocker NF (dB) (-141dBc/Hz @ offset)	32[**]			N.A.	13.5 (PNC on) 32 (PNC off)	N.A.			
HRR3/5 (dB)	N.A.	42/45	N.A.	N.A.	N.A.	N.A.		N.A.	
Gain (dB)/IF BW (MHz)	22/20	70/N.A.	70/0.5-30	20-35/N.A.	60/N.A.	17/N.A.	9.4/N.A.	17-53/1-27	
OB-B1dB (dBm) @ 100MHz	12.5	-0.5	N.A.	N.A.	-2.5	-1.9	N.A.	-1.42	4.6∼9.6
IB-B1dB (dBm) @ 1MHz	-10	-6 @ 30MHz	-20 @ 20MHz	3	N.A.			-25.7	-2.8∼8
Power (mW)	56∼290	32 (ex. LO)	30∼55 (ex. PLL)	11 (RF), 11.5 (canceller)	12(RF), 23(BB) 11(PNC)	3 (RF)	7∼35 (RF)	14 (RF)	8.7∼15.7 (RF)
								16 (BB)	

[**]Estimated and/or interpreted form plots, figures and/or reported numbers. Summarized in [29].
[##]Post-layout simulation results of on-chip divider-by-4 at 20MHz offset.

C.5 Conclusion

This paper presents an NIS-based receiver with frequency-independent filtering, operating from 0.5 to 2.7 GHz. The nonlinear RF stage uses a folded Gilbert structure for better blocker suppression and power efficiency. In nonlinear mode, it provides >38 dB suppression to a 0 – 9.6 dBm blocker while consuming 8.7 to 15.7 mW in the RF stage, with the maximum attainable blocker level exceeding PDC-5dB. The RX achieves - 2.8 to 8 dBm IB B_{1dB} at 1MHz offset. Since the blocker is suppressed at RF, reciprocal mixing (-155 dBc/Hz @ 20 MHz) is much alleviated, achieving 15.1/15.47 dB NF with a 0.65/1.95 dBm blocker. With the proposed novel NIS-based RX architecture, the trade-off between blocker suppression, blocker NF, IB linearity and power efficiency is significantly relaxed, making it suitable for usage in spectral-efficient wireless applications.

Acknowledgment

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D

A Wideband Receiver with 78.5dB SIR Improvement under a 5.3dBm Blocker at 10MHz Offset

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A new wideband receiver with nonlinear interference suppression technique is proposed that it delivers better linearity and NF performance over power consumption efficiency under strong blocker compared with conventional linear mode receivers. Simultaneous blocker suppression and small signal amplification is enabled by using nonlinear transfer function. The blocker suppression is done in the amplitude-domain, independent of the offset frequency between the blocker and the wanted signal. It greatly relaxes the design trade-off between linearity, NF and power consumption with strong blocker present. The prototype is implemented in 40nm CMOS and achieves more than 38dB blocker suppression over blocker power range from 0 to 9.6dBm. Compared with linear mode operation, the proposed receiver operates in nonlinear mode and offers 78.5dB SIR improvement under a 5.3dBm blocker with no extra power consumption.

Keywords - Receiver, blocker, nonlinear interference suppression (NIS), nonlinear transfer function, amplitude-domain filtering, software-defined radio (SDR), full duplex (FD), wideband, reconfigurable, CMOS, noise figure (NF), reciprocal mixing, linearity, signal-to-interference ratio (SIR), IIP3, blocker 1dB compression point (B1dB), power efficiency..

D.1 Introduction

With the ever increasing crowdedness of RF spectrum and hence the complexity of radio receiver design to support multiple standards, research efforts have been made to explore more efficient and flexible ways to use the spectrum. Examples are the software-defined radios (SDRs), full duplex (FD) systems and etc. A major challenge behind these architectures is the lack of filtering at the RF stage. To enable wideband operation, SDRs do not have off-chip SAW filters, hence it is prone to interference from a wide frequency range. For FD systems, the biggest problem is the strong transmitter self-interference to the receiver path which is operating at the same frequency. These interference power could be bigger than 0dBm. The problems associated with these strong interference are desensitization, reciprocal mixing and extra power consumption to tolerate the strong interference.

N-path filter topologies have been widely used in mixer-first receiver architecture to provide filtering for out-of-band interferers. Several works have reported to tolerate 0dBm out-of-band blocker [31, 36, 40, 51–53, 57, 65] and provide good out-of-band IIP3 and B1dB [44–46]. However the NF is high due to the lack of LNA [31, 36, 40, 44, 46]. The NF degradation due to reciprocal mixing is also a problem due to the limited filtering capability. To address the NF issue, a second auxiliary passive-mixer-based downconversion path was added in [27] to cancel the noise from the main path. Later in [29], a third phase-noise cancellation (PNC) path was added to cancel the reciprocal mixing products (similar idea in [59]) with the strong blocker. The NF is below 14dB under a 0dBm blocker at 80MHz offset while consuming extra 11mW power consumption in the PNC path [29]. However these techniques are based on frequency-domain filtering, thus do not apply to blockers at small offset to alleviate desensitization or reciprocal mixing.

Active and passive TX self-interference cancellation techniques are reported in [5, 66–69] by creating a TX replica and injecting it at the RX input. The main limitation comes from the phase and amplitude inaccuracy of the creation of the TX replica, which limits the amount and bandwidth of the cancellation. The work in [69] reported the TX leakage power at 1dB RX compression is 1.5dBm with 27dB cancellation.

An unique RF amplifier with nonlinear interference suppression (NIS) technique was proposed in [6]. The circuit uses a nonlinear transfer that essentially provides different gains for signals having different amplitude levels [102]. The method is based on amplitude-domain, and hence frequency independent. It requires the nonlinear transfer function according to the amplitude of the locally generated TX signal. It achieves more than 30dB suppression to a 0-11dBm blocker and consumes 7-35mW.

In this paper, a new wideband receiver with NIS technique is proposed. It has two modes of operation, linear mode for no blocker present and nonlin-

ear mode for strong blocker present. Compared with [6], the NIS technique is implemented at the RF stage with a folded Gilbert-cell structure and extended to operate in a wideband manner. It improves the amount of blocker suppression over a larger power range while consuming less power consumption. The system is also proposed to deal with both locally generated TX self-interference and external interference. Compared with other receiver works with frequency-domain filtering techniques, the proposed receiver provides excellent linearity, power efficiency and blocker NF performance when operating under strong blockers. The performances are not sacrificed when the blocker is at small offset frequency.

The paper is organized as follows. Section D.2 provides the introduction to the nonlinear interference suppression concept and the proposed receiver system. The NIS block design and analysis is presented in Section D.3. The implementation of the receiver is described in Section D.4. Measurement results are presented in Section D.5. Conclusions are drawn in Section D.6.

D.2 Introduction to Amplitude-Domain Filtering Mechanism

As discussed in section D.1, the recently published blocker-tolerant receivers were based on frequency-domain filtering. The ability of blocker filtering is directly dependent on the frequency offset between the wanted signal and the blocker signal. Moreover, the reciprocal mixing between blocker residue and LO phase noise adds noise degradation on top of the receiver noise figure. To avoid these unwanted effects, we propose a unique blocker filtering technique based on amplitude-domain filtering in [6, 103].The mechanism behind it is revisited here and explained how it is applied in the system.

D.2.1 Nonlinear transfer and frequency-domain behavior

With a typical nonlinear system as shown in Fig. D.1(a), a large interferer signal will cause desensitization and introduce large intermodulation products. In the frequency domain, the small signal with reduced gain is accompanied by the large interferer output, and the intermodulation products at $2\omega_{LS} - \omega_{SS}$ and $2\omega_{SS} - \omega_{LS}$. The power of the intermodulation products is proportional to the large signal amplitude A_{LS}.

However, the situation is different if the nonlinear transfer function is specially tailored to the amplitude of the strong interferer. The 3rd-order polynomial transfer in Fig. D.1(b) is an example here with $y(t) = c_1x(t) + c_3x(t)^3$. Assuming the large signal is $x(t) = A_{LS}sin(\omega_{LS}t)$, by choosing $c_3 = -4c_1/3A_{LS}^2$, the output becomes $y(t) = -c_1A_{LS}sin(3\omega_{LS}t)/3$. The large signal at the fundamental frequency is completely removed, while 3rd harmonic is created.

If a small wanted signal is also present with amplitude $A_{SS} << A_{LS}$, the large interferer suppression will not be affected and the small signal will be

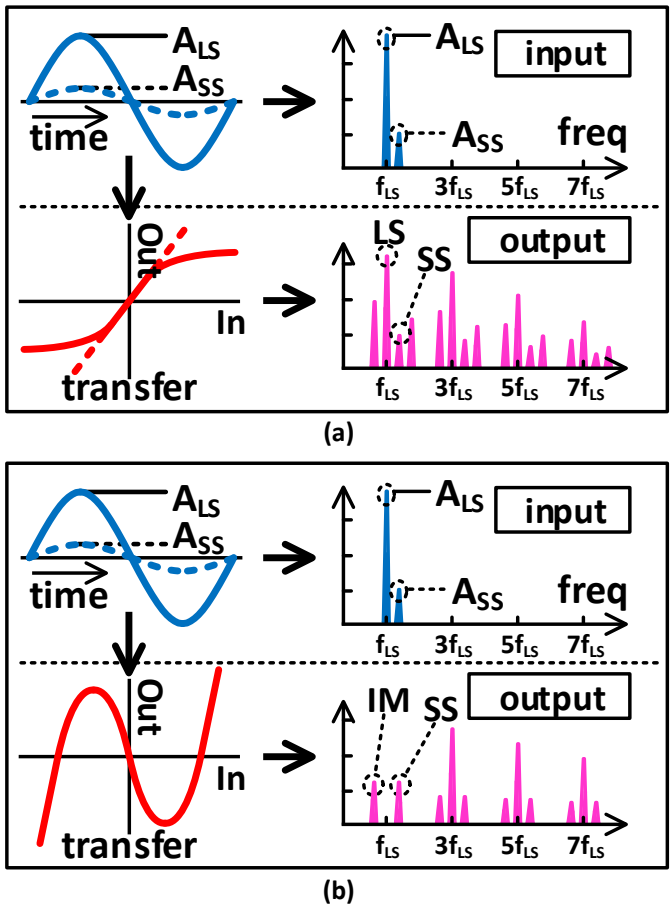

Figure D.1.: The transfer function of a (a)typical nonlinear transfer or (b)specially-tailored 3rd order polynomial nonlinear transfer and its effect on the input of a strong signal and a small wanted signal in frequency domain

amplified. The output frequency spectrum in Fig. D.1(b) is much cleaner at the fundamental frequency compared with Fig. D.1(a). An intermodulation product is created at an offset from the small signal that is twice the offset between the small signal and large interferer, and with the same power as the small signal. Harmonics are present at higher frequencies. As the 3rd order polynomial transfer function is only related to the amplitude of the large signal, the large signal suppression is independent of the frequency offset between the large interferer signal and the small wanted signal.

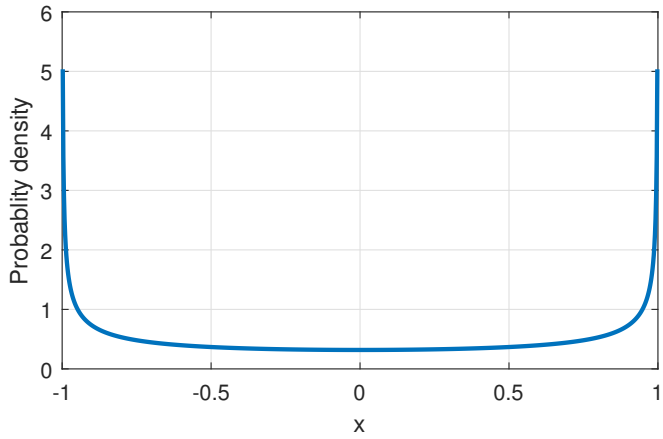

Figure D.2.: Probability density function (PDF) of a sinusoidal waveform with normalized amplitude.

D.2.2 Interpretation using Fourier Analysis

Fourier analysis is applied to the output to analyze the different consequences for the large interferer $Int(t)$ and the small wanted signal $s(t)$ [73]. The effective gain of the fundamental of the large signal, G_{LS}, and of the small signal, G_{SS}, can be expressed as

$$G_{LS} = \frac{1}{A_{LS} \cdot \pi} \int_{-\pi}^{\pi} f(A_{LS} sin\theta) \cdot sin\theta d\theta \tag{D.1}$$

$$G_{SS} = \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot PDF_{sine}(x) dx \tag{D.2}$$

where $f(x)$ is the nonlinear transfer function, A_{LS} is the amplitude of the large signal and $PDF_{sine}(x)$ is the probability density function (PDF) of the large signal.

For full suppression, i.e. $G_{LS} = 0$, transfer function f(x) must be odd function and have at least three crossings within the range of $[-A_{LS}, A_{LS}]$. For small signal gain G_{SS}, it is a function of the derivative of the transfer function, amplitude A_{LS} and PDF of the large signal. The PDF of a sinusoidal signal is shown in Fig. D.2. Therefore G_{SS} is strongly dependent on the derivative of the transfer function at the outer edges at $\pm A_{LS}$.

With Eqn. (D.1)(D.2), the output in Fig. D.1(b) around the fundamental

frequency can be described as

$$y(t) = G_{LS} \cdot Int(t) + \frac{1}{2}\left[A_{LS} \cdot \frac{\partial G_{LS}}{\partial A_{LS}} + G_{LS}\right] \cdot s(t) + \frac{1}{2}\left[A_{LS} \cdot \frac{\partial G_{LS}}{\partial A_{LS}} - G_{LS}\right] \cdot IM(t) \tag{D.3}$$

The first term is the residue of the large signal, the second term is the amplified small signal and the third term is the intermodulation product. If G_{LS}=0, the output becomes

$$y(t) = \frac{1}{2}\left[A_{LS} \cdot \frac{\partial G_{LS}}{\partial A_{LS}}\right] \cdot \left[s(t) + IM(t)\right] \tag{D.4}$$

The small signal output and the intermodulation product have the exact same amplitude. In other words, spectrum mirroring happens between signal located at ω_{SS} and image at $2\omega_{LS} - \omega_{SS}$. Consequently, a 3dB noise penalty is introduced, assuming the input noise power density and noise matching is equal at ω_{SS} and $2\omega_{LS} - \omega_{SS}$.

Similarly, we can describe the noise figure of the nonlinear transfer. If assuming the input signal is thermal noise, the noise factor can be expressed as

$$F = \frac{\mathrm{SNR}_{in}}{\mathrm{SNR}_{out}} = \frac{1}{\mathrm{SNR}_{out|v_{in}=v_n}} = \frac{\mathrm{P}_{noise}}{\mathrm{P}_{signal|v_{in}=v_n}} \tag{D.5}$$

The output signal power with input as white noise equals to

$$\begin{aligned} \mathrm{P}_{signal,v_n} &= v_n^2 \cdot G_{SS}^2 \\ &= v_n^2 \cdot \left| \int_{-A_{LS}}^{A_{LS}} \frac{\partial f(x)}{\partial x} \cdot \frac{\partial x}{\pi\sqrt{A_{LS}^2 - x^2}} \right|^2 \end{aligned} \tag{D.6}$$

For output noise power, however, no matter what the sign of $\frac{\partial f(x)}{\partial x}$ is, it always leads to additive behavior. The noise power is calculated as, assuming white thermal noise source only,

$$\begin{aligned} \mathrm{P}_{noise} &= \int_{-A_{LS}}^{A_{LS}} \left| \frac{\partial f(x)}{\partial x} \cdot v_n \right|^2 \cdot \frac{\partial x}{\pi\sqrt{A_{LS}^2 - x^2}} \\ &= v_n^2 \cdot \int_{-A_{LS}}^{A_{LS}} \left| \frac{\partial f(x)}{\partial x} \right|^2 \cdot \frac{\partial x}{\pi\sqrt{A_{LS}^2 - x^2}} \end{aligned} \tag{D.7}$$

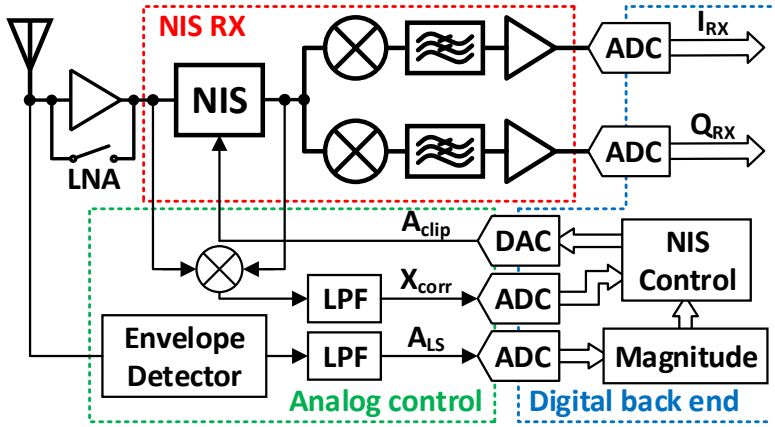

Figure D.3.: The nonlinear-transfer-based NIS receiver system architecture for interference suppression.

Considering the 3rd polynomial in Fig. D.1(b), the noise factor is equal to 3, or a noise figure of 4.7dB. This is resulting from the noise folding from the mirroring product and the 3rd harmonic, assuming the input noise density and noise matching is equal at the fundamental and the 3rd harmonic frequencies. However in reality, the noise at 3rd harmonic frequency can be suppressed rather easily.

D.2.3 Nonlinear Interference Suppression Receiver System

The system diagram of the nonlinear interference suppression (NIS) based receiver is shown in Fig. D.3. The key mechanism behind is to exploit the amplitude difference between two signals, and use a nonlinear transfer to create a notch filter at the amplitude of the large signal. Hence, the application of this mechanism requires, firstly the large interferer amplitude A_{LS} is much larger than the small signal amplitude A_{SS}, otherwise there is no need of large interferer suppression. Secondly, the dynamic adaptation of the nonlinear transfer to track A_{LS} for a modulated interferer.

The best location to implement the nonlinear transfer is before the mixer, but maybe after the LNA. The large blocker is suppressed at the RF stage so that the performance and power consumption of the following chain are relaxed. It also reduce NF degradation due to reciprocal mixing between interferer residue and LO phase noise. Besides, with the gain and the frequency selectivity from the preceding LNA, the receiver with nonlinear transfer will achieve a good NF.

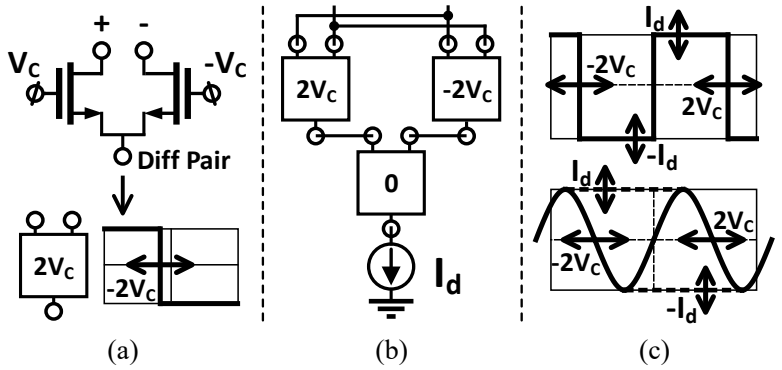

Figure D.4.: (a) Differential pair with a bias voltage offset of $2V_C$ and its V-I transfer function, (b) Gilbert-cell structure of combining three differential pair with bias voltage offset of 0, $2V_C$ and $-2V_C$, (c) the created nonlinear transfer in ideal (top) and implementation (bottom).

D.3 Design and Analysis of NIS Receiver

D.3.1 Schematic of NIS Transconductance Amplifier

For a differential pair with a bias voltage offset of $2V_C$ as shown in Fig. D.4(a), its V-I input-output transfer function is shifted towards negative by $2V_C$. By combining three differential pairs with bias offset of 0, $2V_C$ and $-2V_C$ respectively, the required nonlinear transfer can be created. The Gilbert-cell combining structure with a tail current source I_d is shown in Fig. D.4(b)and its transfer function is shown in Fig. D.4(c) both for the ideal case and for real implementation. The nonlinear transfer can be adjusted by both V_C and I_d.

The proposed NIS transconductance amplifier is shown in Fig. D.5, using a differential and complementary folded Gilbert-cell structure. The CG transistors M_{1p}, M_{1n} form the first differential pair with no bias offset. The ac current is fed into the second and third differential pair composed of M_{2p}, M_{3p} and M_{2n}, M_{3n}, with a bias offset of $-2V_C$ and $2V_C$, respectively. M_{4p}, M_{4n} are variable current sources. Transistors M_{5-8} make up the other differential part of the circuit. Capacitor C_M is used to compensate the pole introduced at the drain of the current sources to maximize suppression. In nonlinear mode, V_C and I_d are updated according to the blocker power. In linear mode, V_C is set negative so that the out-of-phase branches, M_{2p} and M_{6p}, are switched off.

In [6], the NIS circuit is realized by combining the outputs of a linear amplifier and a clipping amplifier. The current of the clipping amplifier is adjusted according to the instantaneous interferer amplitude. Compared with [6], the proposed circuit has three advantages. Firstly, the power consumption under different blocker power is well defined by the current source I_d. Secondly,

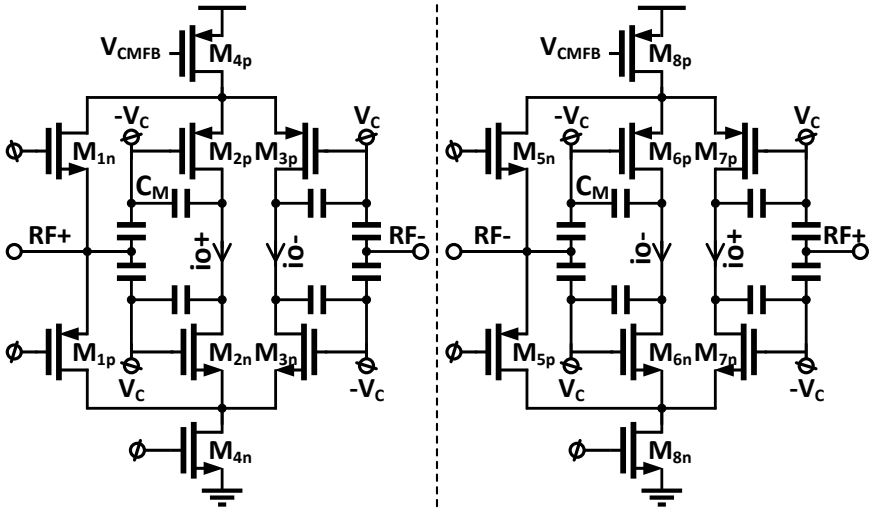

Figure D.5.: Schematic of the proposed NIS transconductance amplifier.

there are two degree of freedom, V_C and I_d, in the circuit. It helps to achieve an optimum performance between suppression and noise figure for different blocker power. Thirdly, there is no need to create two amplified copies of interferer that are then cancelled out. This makes the circuit power-inefficient and might contribute to a higher noise figure.

D.3.2 Nonlinear Transfer and Equivalent G_{LS},G_{SS}

An example of the nonlinear transfer and its derivative is shown in Fig. D.6 (a)(b) with setting I_d=4mA and V_C=170mV. The zero crossings are at 0 and around $\pm 2V_C$. The center region of the transfer is determined by the CG devices and the regions around $\pm 2V_C$ are determined by the differential pairs. The equivalent G_{LS}, and G_{SS} are calculated using Eqn. (D.1) and (D.2) and the results over A_{LS} are shown in Fig. D.6(c).

For very small A_{LS}, the circuit operates in the CG region. G_{LS} and G_{SS} are the same and are determined by the CG gm. When the interference amplitude start to increase, the circuit starts to operate nonlinearly and G_{LS}, G_{SS} start to behave differently. According to Eqn. (D.1), G_{LS}=0 happens when the integral over the CG region and the diff-pair regions equal to zero. This happens at $A_{LS} = 385mV$. For $A_{LS} > 385mV$, G_{LS} increases again as the integral result is now more dominant by the differential-pair region. On the other hand, according to Eqn. (D.2), G_{SS} is related to the convolution of the output transconductance Gm_{NIS} and the PDF of the large signal within $[-A_{LS}, A_{LS}]$. Therefore G_{SS} is largely dependent on the Gm_{NIS} around $\pm A_{LS}$. As shown in the figure, G_{SS} first decreases faster than G_{LS}, then follows the change of Gm_{NIS} in the

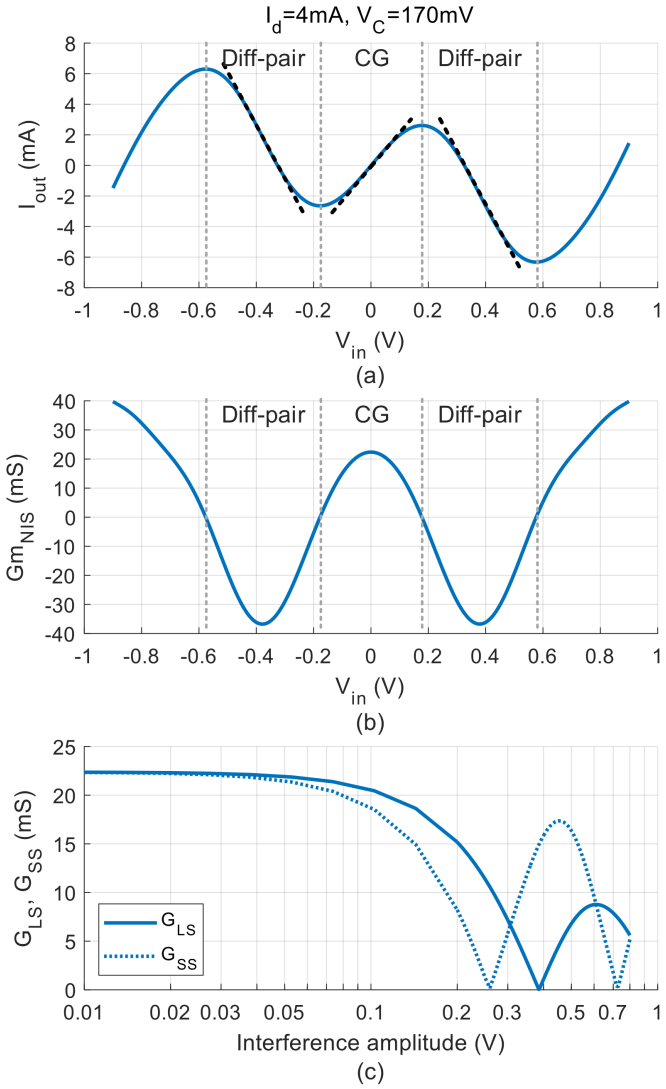

Figure D.6.: (a) The V-I transfer function with I_d=4mA and V_C=170mV, (b) the derivative, Gm_{NIS}, of the transfer function, (c) G_{LS} and G_{SS} as a function of the interference amplitude A_{LS}.

differential-pair region. Therefore, the behavior of the differential-pair decides the equivalent gain for the small signal G_{SS} and blocker 1dB compression point B_{1dB}. For this particular transfer function, maximum suppression happens at a blocker amplitude $A_{LS} = 385mV$ and the small signal transconductance gain G_{SS} is 15mS.

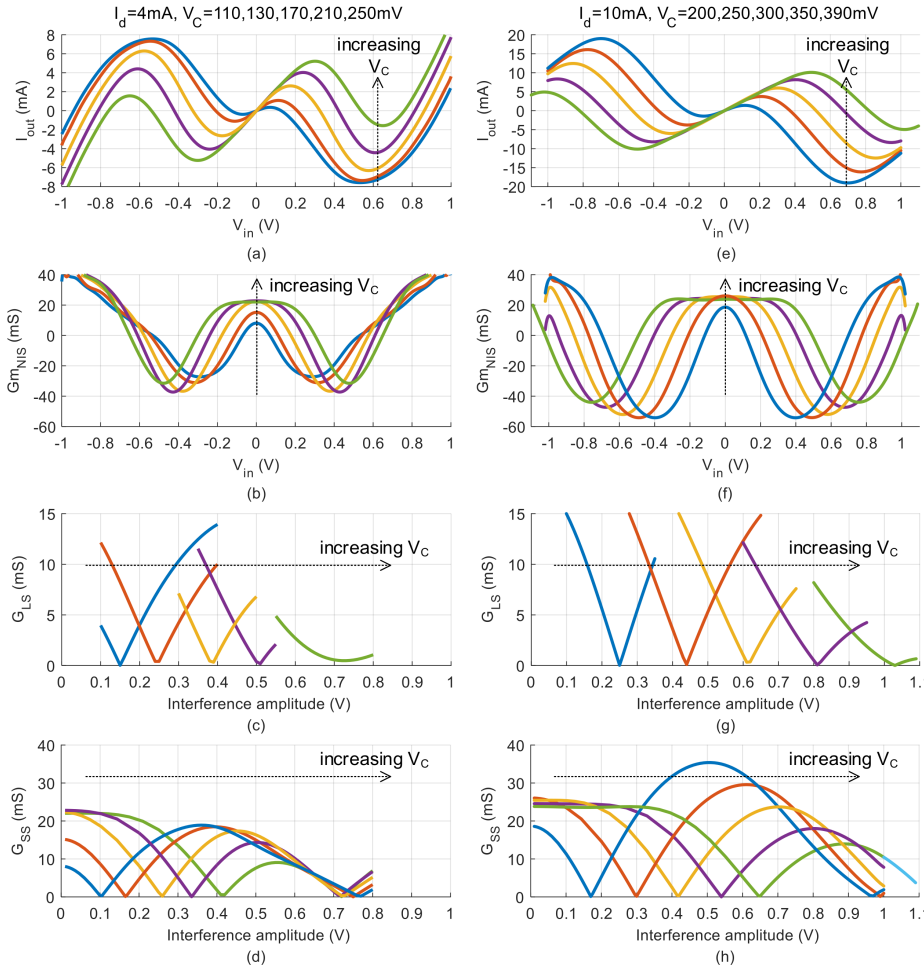

Figure D.7.: With Id=4mA and Vc=110 to 250mV, (a) The V-I transfer function, (b) the corresponding derivative, Gm_{NIS}, (c) G_{LS} at different Vc, (d) G_{SS} at different Vc. With Id=10mA and Vc=200 to 390mV, (e) The V-I transfer function, (f) the corresponding derivative, Gm_{NIS}, (g) G_{LS} at different Vc, (h) G_{SS} at different Vc.

D.3.3 Effect of V_C and I_d on G_{LS}, G_{SS} and Z_{in}

The transfer functions and their derivative Gm_{NIS} with $I_d = 4mA$ over different V_C values are shown in Fig. D.7 (a)(b). G_{LS} and G_{SS} are shown in Fig. D.7 (c)(d).

When is V_C as small as 110mV, there is no clear separation between CG region and differential-pair region in the nonlinear transfer. For V_C smaller than 110mV, the nonlinear transfer cannot be created as required.

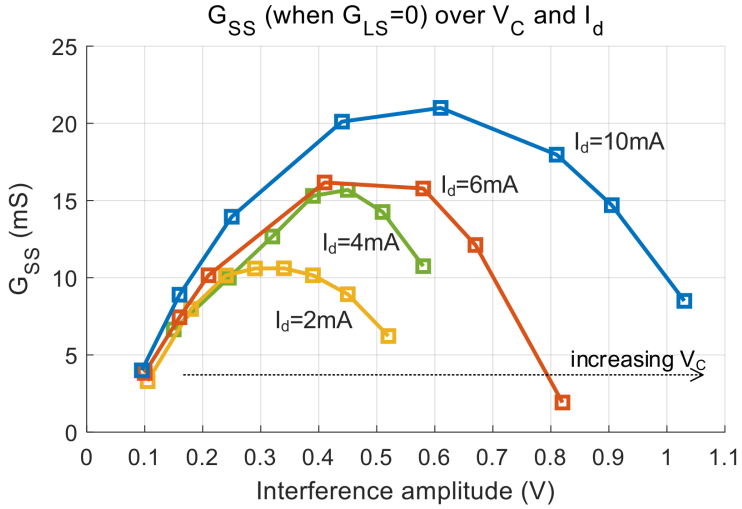

Figure D.8.: G_{SS} when G_{LS}=0 for different Vc and Id settings.

When V_C is increasing, the differential-pair region is shifted outwards. As a result, firstly, there is clearer separation between the CG region and the diff-pair region. secondly, the output transconductance Gm_{NIS} in the CG region is converging to the gm of the CG devices. Thirdly, the nonlinear transfer and Gm_{NIS} in the diff-pair region are similar and basically shifted on the x-axis for different V_C. Similarly the curves of G_{LS} and G_{SS} also shifted outwards.

When V_C gets as big as 250mV, the CG region is getting too big that the result of Eqn. (D.1) is always bigger than zero. This puts a limit on the largest interference amplitude A_{LS} that can be suppressed for a given I_d.

A bigger I_d can shift upwards the operation range of A_{LS}. The results with $I_d = 10mA$ over different V_C are shown in Fig. D.7 (e)-(h). The largest interference amplitude A_{LS} that can be suppressed is extended to above 1V. Larger current source will increase the range of A_{LS} at which the circuit has an acceptable Z_{in}. Besides, it also provides larger G_{SS}.

However if we combine Fig. D.7 (c) and (d), or (g) and (h), we shall see that G_{SS} at the A_{LS} where $G_{LS} = 0$ is dependent on V_C, or equivalently A_{LS}. This behavior over V_C and I_d is shown in Fig. D.8. This is a result of the cross-modulation between the large interferer and the weak signal. A digital compensation block can be used to correct cross-modulation by applying the inverse of the weak signal gain [104].

D.3.4 Noise Figure

In the presence of a large blocker, the transconductance of the CG and differential pair devices are changing periodically. Therefore, we must use Fourier

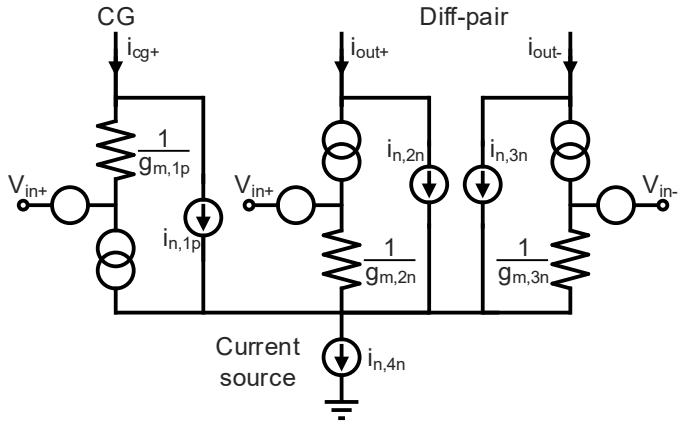

Figure D.9.: The 1/4 schematic with noise sources of CG, diff-pair and current sources.

analysis to analyze the noise contribution from each noise source within a period of the large blocker. Fig. D.9 shows the different noise sources from a quarter of the schematic, namely $i_{n_{1p}}$, $i_{n_{2n}}$, $i_{n_{3n}}$, $i_{n_{4n}}$. Besides, there is also noise from the source, $i_{n_{SRC}}$. The transfer, its derivative when using I_d=4mA, V_C=200mV and transconductance g_m of each transistor is shown in Fig. D.10(a)-(d).

Firstly, the noise transfer from the current source M_{4n} to the output is analyzed. When the circuit is working in the CG region, the noise current from the current source appears at the output directly. The output noise current spectral density is given in Eqn. (D.8). In diff-pair region, the noise current from the current source splits between the differential output according to $1/g_{m_{2n}}$ and $1/g_{m_{3n}}$. The output noise is given in Eqn. (D.9). The total current noise PSD from the current sources is shown in Fig. D.10(e).

$$\left|i_{n_{out,I_d}}\right|^2 = 4kT\gamma \cdot g_{m_{4n}} \tag{D.8}$$

$$\left|i_{n_{out,I_d}}\right|^2 = 4kT\gamma \cdot g_{m_{4n}} \cdot \frac{(g_{m_{2n}} - g_{m_{3n}})^2}{4(g_{m_{2n}} + g_{m_{3n}})^2} \tag{D.9}$$

Secondly, the noise transfer from CG device M_{1p} to the output is very similar as the noise from current source. The output nosie current spectral density of CG is given in Eqn. (D.10) and (D.11). The total current noise PSD from the CG devices is shown in Fig. D.10(f).

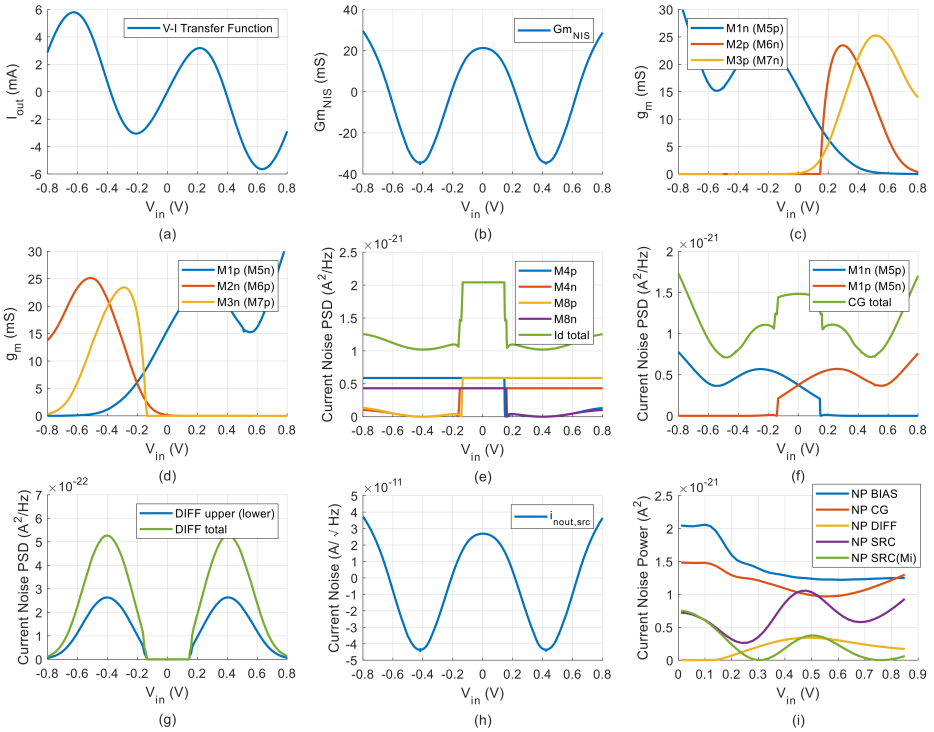

Figure D.10.: (a) The V-I transfer function with Id=4mA and Vc=200mV, (b) its derivative Gm_{NIS}, (c) gm of transistor M1n, M2p, M3p, or M5p, M6n, M7n, (d) gm of transistor M1p, M2n, M3n, or M5n, M6p, M7p, (e) the output current noise PSD of the current source, (f) the output current noise PSD of the CG, (g) the output current noise PSD of the diff-pair, (h) the output current noise due to the source, (i) the current noise power from each noise sources.

$$\left|i_{n_{out,CG}}\right|^2 = 4kT\gamma \cdot g_{m_{1p}} \tag{D.10}$$

$$\left|i_{n_{out,CG}}\right|^2 = 4kT\gamma \cdot g_{m_{1p}} \cdot \frac{(g_{m_{2n}} - g_{m_{3n}})^2}{4(g_{m_{2n}} + g_{m_{3n}})^2} \tag{D.11}$$

Thirdly, the output current noise due to the differential pair M_{2n} and M_{3n} is given in Eqn. (D.12) (D.13) and the corresponding output current noise

spectral density of differential pair is in Fig. D.10(g)

$$i_{n_{out,diff}} = \frac{i_{n,2n} \cdot g_{m_{3n}}}{g_{m_{2n}} + g_{m_{3n}}} - \frac{i_{n,3n} \cdot g_{m_{2n}}}{g_{m_{2n}} + g_{m_{3n}}} \tag{D.12}$$

$$\left| i_{n_{out,diff}} \right|^2 = 4kT\gamma \cdot \frac{g_{m_{2n}} \cdot g_{m_{3n}}}{g_{m_{2n}} + g_{m_{3n}}} \tag{D.13}$$

Fourthly, the output noise due to the source can be calculated similarly and the output current noise spectral density is given in Eqn. (D.14)(D.15).

$$i_{n_{out,src}} = \sqrt{4kTZ_{src}} \cdot G_{m_{NIS}} \tag{D.14}$$

$$\left| i_{n_{out,src}} \right|^2 = 4kTZ_{src} \cdot G_{m_{NIS}}^2 \tag{D.15}$$

The total noise from the circuit can be calculated with $|i_{n_{out,I_d}}|^2$, $|i_{n_{out,CG}}|^2$, $|i_{n_{out,diff}}|^2$ and $|i_{n_{out,src}}|^2$. Since noise in all regions in the nonlinear transfer is additive, we use Eqn. (D.7) to calculate the total noise due to the circuit and it becomes

$$\mathrm{NP}_{circuit} = \int_{-A_{LS}}^{A_{LS}} \left[|i_{n_{out,CG}}|^2 + |i_{n_{out,I_d}}|^2 + |i_{n_{out,diff}}|^2 + |i_{n_{out,src}}|^2 \right] \cdot \frac{\partial V_{in}}{\pi \sqrt{A_{LS}^2 - V_{in}^2}} \tag{D.16}$$

Finally, the calculation of noise current due to the source considering spectrum mirroring is different. As discussed previously following Eqn. (D.6) and (D.7), part of the noise figure of the circuit with nonlinear transfer is degraded by the noise folding from mirroring product and harmonics. Using Eqn. (D.6), the output noise power with input as noise voltage due to the source is given in Eqn. (D.17).

$$\mathrm{NP}_{src,mirror} = \left| \int_{-A_{LS}}^{A_{LS}} i_{n_{out,src}} \cdot \frac{\partial V_{in}}{\pi \sqrt{A_{LS}^2 - V_{in}^2}} \right|^2 \tag{D.17}$$

The current output noise power from different noise sources are shown in Fig. D.10(i). The two big contributors are the noise due to current sources and CG devices. This is because unlike the noise of differential pair, the noise due to current sources and CG devices directly appear at one of the output for a large part of the period. The gm of CG devices are also limited by the input matching requirement. The gm of current sources are relatively big due to the limited voltage headroom. The noise power of the source considering spectrum mirroring basically follows the change of $G_{m_{NIS}}$ and has two notches.

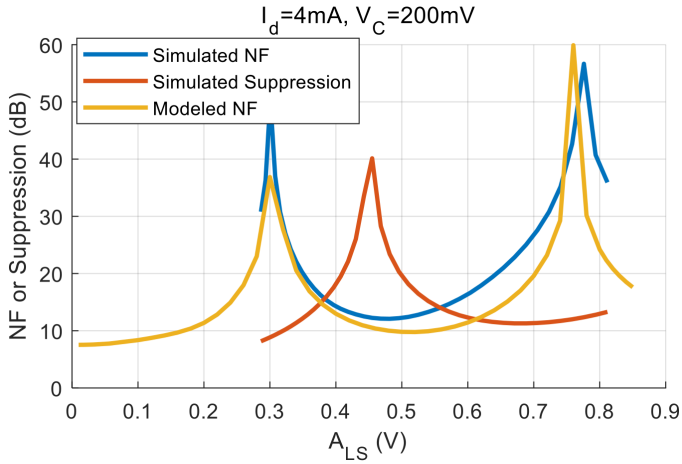

Figure D.11.: Comparison between modeled NF and simulated NF, and simulated blocker suppression.

Each notch happens at the position shortly after $G_{m_{NIS}}$ changes sign.

The noise factor is equal to total noise at the output divided by the noise at the output due to the source considering spectrum mirroring, as expressed in Eqn. (D.18).

$$\mathrm{F}_{NIS} = \frac{\mathrm{NP}_{circuit}}{\mathrm{NP}_{src,mirror}} \tag{D.18}$$

The modeled NF using Eqn. (D.18) is compared with the simulated NF and shown in Fig. D.11, along with the simulated blocker suppression. The modeled NF and simulated NF are matched quite well. They both have two peaks at the A_{LS} where the noise power due to the source, NP_{src}, is equal to zero. The minimum noise figure is achieved when NP_{src} is at its peak value, which is in the diff-pair region. Therefore for noise consideration, it is desirable to extend the diff-pair region so that the two NF peaks are further away. Thus a smaller NF can be achieved over a wider range of A_{LS}. This can be tuned by changing the bias voltage at the gate of the diff-pairs at the cost of smaller G_{SS}.

In Fig. D.11, there's still a gap between modeled NF and simulated NF. There are several possible reasons. Firstly, it can be the noise coefficient γ between modelling and simulation. $\gamma = 1.5$ is used in modeling. Secondly, the noise sources in the modeled NF only cover channel noise, while it does not cover other noise sources such as gate, source or drain resistance, or flicker noise. The diff pair is excited by a large blocker similarly to the operation of a mixer or an oscillator. The flicker noise of the current sources will be

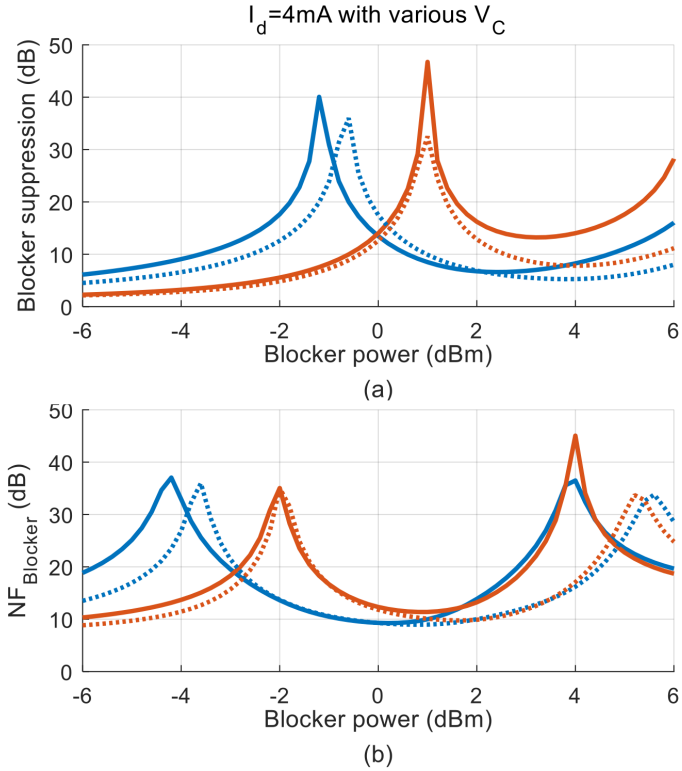

Figure D.12.: (a) The simulated blocker suppression, (b) simulated blocker NF. The bias voltage of the upper and lower diff-pair is changed from $\frac{1}{2}\text{VDD} \pm V_C$ to $\frac{1}{2}\text{VDD} + V_{offset} \pm V_C$ and $\frac{1}{2}\text{VDD} - V_{offset} \pm V_C$. $V_{offset} = 0$ for the solid lines and $V_{offset} = 0.2$ for the dashed lines.

upconverted to the blocker frequency ω_{LS}, which can be very close to ω_{SS}. Unlike oscillator design, a capacitor to ground is not appropriate here as a high impedance node is desired.

The simulated results on suppression and $\text{NF}_{Blocker}$ are shown in Fig. D.12. The bias voltage of the upper and lower diff-pair is changed from $\frac{1}{2}\text{VDD} \pm V_C$ to $\frac{1}{2}\text{VDD} + V_{offset} \pm V_C$ and $\frac{1}{2}\text{VDD} - V_{offset} \pm V_C$. $V_{offset} = 0$ for the solid lines and $V_{offset} = 0.2$ for the dashed lines. It is clearly seen that by changing the biasing voltage, the optimum region of NF is extended to cover a wider range of A_{LS}.

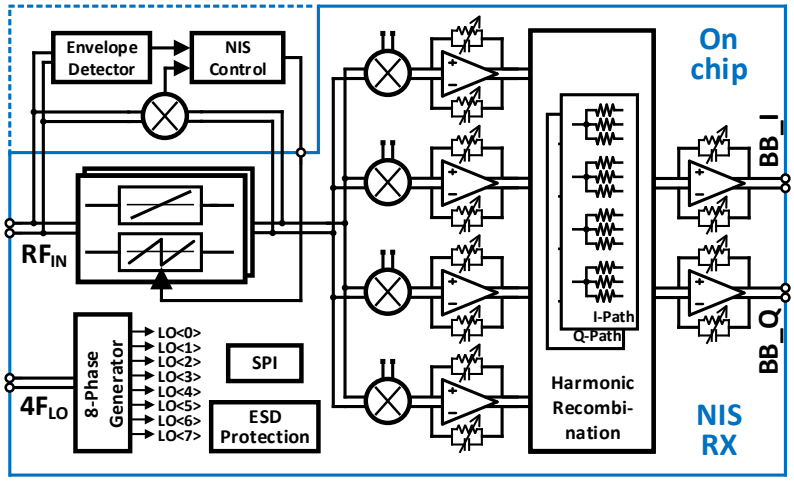

Figure D.13.: The system diagram of the proposed NIS-based receiver.

D.4 Complete Receiver

D.4.1 Receiver Topology

The block diagram of the proposed NIS-based receiver is shown in Fig. D.13. The on-chip part consists of the RF signal path and the LO path, while the NIS control path is placed off-chip. The signal path uses current-mode circuit to maximize large signal linearity. The RF stage is an NIS-based transconductance amplifier that has two operation modes. In linear mode, it is operated as an amplifier. The nonlinear mode is enabled when strong blocker is present and the circuit will perform simultaneous frequency independent blocker suppression and weak signal amplification. The circuit is designed for wideband operation. It suppresses large blockers fall in the bandwidth from 0.5GHz to 3GHz, independent of the offset frequency between the blocker and the wanted signal.

For current-mode operation, the impedance looking into the mixer is kept small. The impedance consists of the series on-resistance of the passive mixer switches and the up-converted input impedance of the TIAs. For 8-path passive mixer, the contribution is dominated by the switch on-resistance, which is around 50Ω. A differential passive mixer was used to avoid the noise figure degradation due to the LO-to-RF coupling of the LO phase noise [78].

D.4.2 Clock Generation and Harmonic Rejection

As shown in Fig. D.1(b), the nonlinear transfer output contains strong 3rd and 5th harmonics. An 8-phase passive mixer with 12.5% duty cycle clock is used

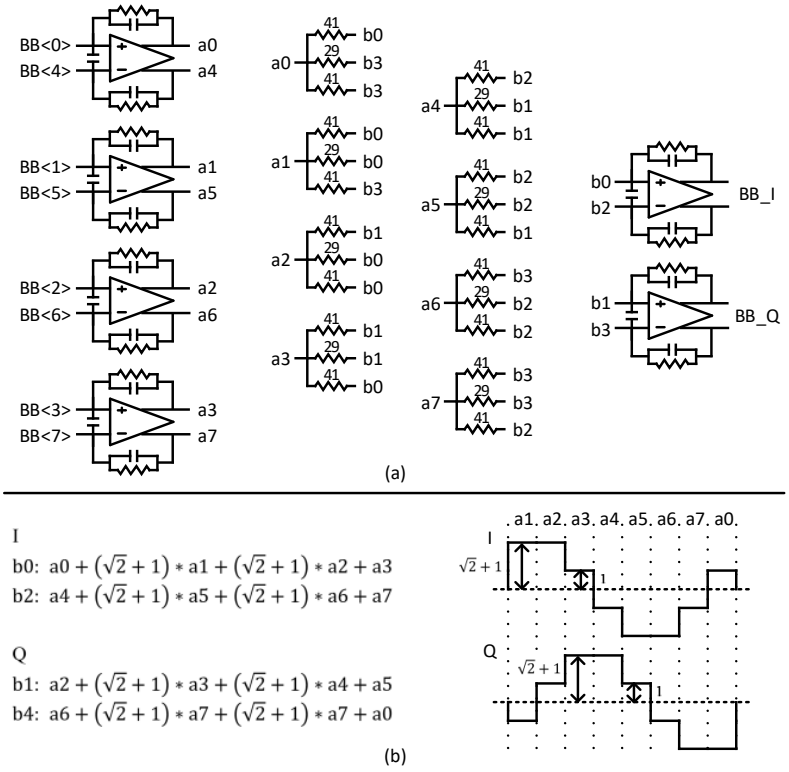

Figure D.14.: (a) Diagram of the baseband TIA and resistive harmonic recombination circuit, (b) the equivalent LO waveform to cancel 3rd and 5th harmonic.

here to avoid downconversion of the 3rd and 5th harmonic. The 12.5% duty cycle LO signals are created by performing AND function on three 50% duty cycle waveforms at $4f_{LO}$, $2f_{LO}$ and f_{LO} [77]. The dynamic power consumption at $f_{LO} = 1.5GHz$ is 12mW. The divide-by-4 circuit works up to 11GHz input frequency and achieves -155dBc/Hz at 20MHz offset. Note this phase noise will degrade the blocker NF for a receiver with little filtering capability.

The baseband harmonic recombination circuit is shown in Fig. D.14, by using resistive networks with a ratio of 41:29:41 to mimic the weighting ratio of $1 : \sqrt{2} : 1$. In order to alleviate the influence by resistor mismatch to the accuracy of weighting factors, the outputs of the first TIA are connected to multiple paths to average out the mismatch between different resistors. They are summed up at the input of the second TIA to achieve harmonic rejection.

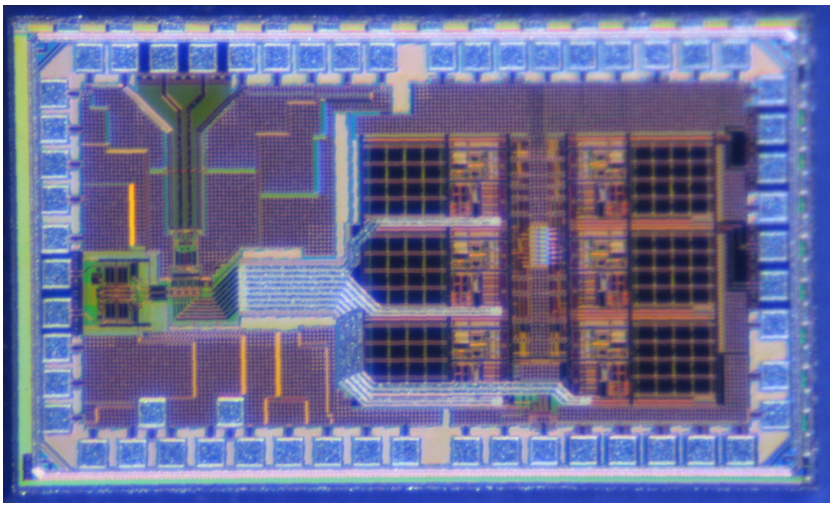

Figure D.15.: Die photo.

D.5 Measurement Results

The proposed NIS-based Receiver was implemented in a 40nm CMOS technology. The die photo is shown in Fig. D.15. The total area is $1.67mm^2$ including bonding pads. The dynamic power consumption of the divider is 12mW at 1.5GHz LO frequency. The baseband TIAs consumes 16.2mW from a 1.1V supply.

D.5.1 Linear Mode Conversion Gain

The conversion gain in linear mode is shown in Fig. D.16. The receiver has a reconfigurable gain and bandwidth from 17-53 dB and 1-27 MHz. Three TIA settings are highlighted and will appear in comparison later. The 1dB compression point P_{1dB} is -21dBm under TIA setting2 (34dB gain). S11 is lower than -10dB over the bandwidth. The RF stage power consumption is 14mW.

D.5.2 Nonlinear Mode G_{LS} and G_{SS}

Fig. D.17 shows the measured G_{LS} and G_{SS} for different nonlinear transfer with TIA setting2. The frequency for the LO, blocker and small signal are 2GHz, 2.01GHz and 2.0001GHz, respectively. The measured results are very similar to simulation in Fig. D.7. Fig. D.17(a) shows the notch filter behavior on the amplitude domain, at blocker power of 0.2dBm and 3.9dBm. Fig. D.17(b) shows the small signal gain as a function of blocker power. Fig. D.17(c) shows the 1dB compression point P1dB with blocker present is around -16dBm

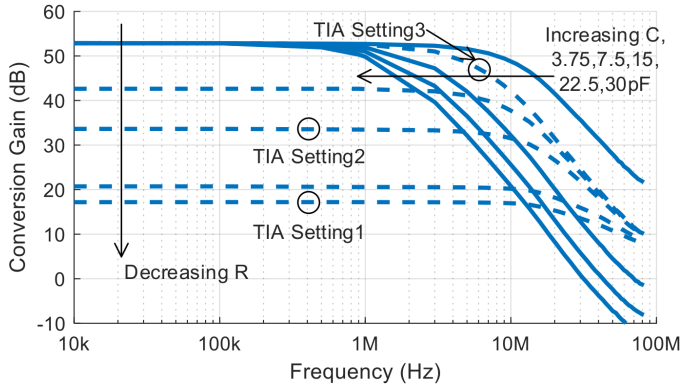

Figure D.16.: Measured conversion gain and IF bandwidth in linear mode.

or +8.7dBm OP1dB. The P1dB is mostly set by the nonlinear transfer and TIA output swing.

For a linear receiver, we use OP_{1dB}/P_{DC} as a figure-of-merit to characterize linearity over power efficiency. For the nonlinear mode, we can use a virtual OP_{1dB} that equals $P_{blocker} \cdot G_{SS}$, which is what a linear receiver needs when the blocker is present. This FOM would be smaller than 1 in a linear receiver but could be higher than 1 in this nonlinear receiver. In this work, this FOM is -2dB in linear mode and 11dB/14.6dB in nonlinear mode as in Fig. D.17.

Fig. D.18 summarizes G_{LS} and G_{SS} over different V_C and Id settings. The measured blocker suppression is more than 38dB for blocker power within [0, 9.6] dBm, or more than 20dB for blocker power within [-4.4, 9.6] dBm. Gss is dependent on NIS setting similar as in Fig. D.8. The NIS block power consumption is 8.7mW at low current setting (1*Id) or 15.7mW at high current setting (2*Id).

D.5.3 Linearity Improvement

Fig. D.19 shows the measured blocker 1dB compression point (B_{1dB}) in linear mode and nonlinear mode over the blocker offset frequency, using TIA setting 2. In linear mode, the IB-B1dB at 1MHz offset is -25.7dBm. The OB-B1dB at 80MHz offset improves to -7.5dBm as a result of baseband filtering. In nonlinear mode, the IB-B1dB at 1MHz offset ranges from -2.8 to 8 dBm for different settings. The OB-B1dB at 80MHz offset ranges from 4.6 to 9.6 dBm. Compared with linear mode operation, the IB-B1dB in nonlinear mode improves around 30dB as a result of the frequency-independent blocker suppression by the NIS block.

Fig. D.20 shows the IB-IIP3 measurement results over blocker offset in nonlinear mode at different V_C and I_d settings. The IIP3 test here is different

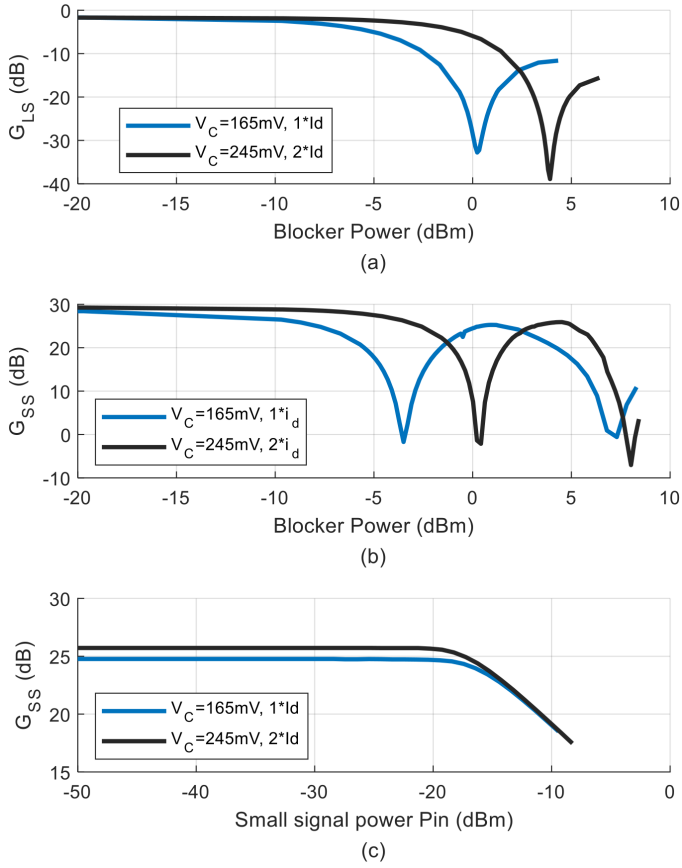

Figure D.17.: Measured (a) blocker suppression G_{LS} and (b) mall signal gain at different Vc and Id. (c) small signal gain G_{SS} over small signal input power, measured under the blocker power at min G_{LS} in (a).

that besides two small tones, the strong blocker is also present at the input. The blocker power is as noted in Fig. D.18 for different V_C and I_d settings. The measurement was made with LO=1.5GHz, 1st tone at 1.501GHz and 2nd tone at 1.5012GHz so that IM3 falls in-band at 800kHz. The blocker offset is swept from 2MHz to 80MHz. The measured IB-IIP3 is around -4dBm with a strong blocker at 2MHz and 2dBm with the strong blocker at 90MHz. These results suggest that with large amount of blocker suppression, the circuit operates linearly for the small signal. As the blocker suppression is frequency-independent, the IB-IIP3 variation over blocker offset is small.

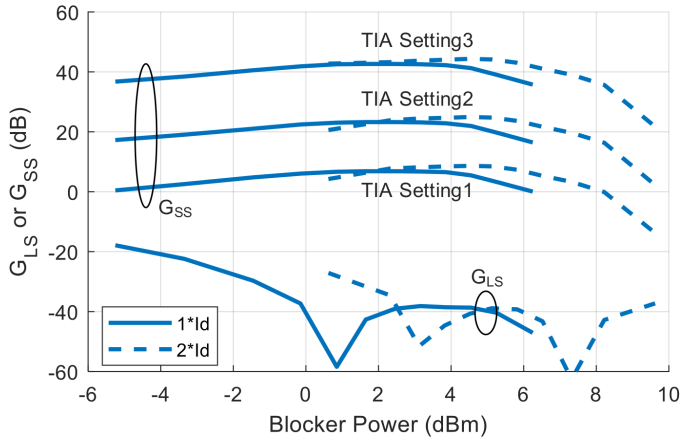

Figure D.18.: Measured blocker suppression G_{LS} by RF NIS block and the small signal conversion gain G_{SS} with the blocker at 10MHz offset.

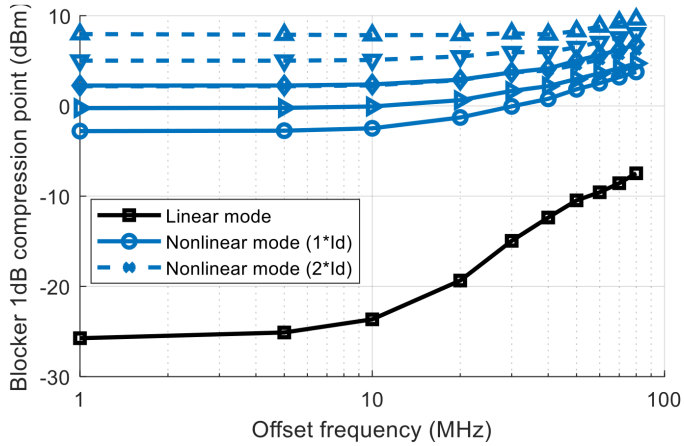

Figure D.19.: Measured Blocker 1dB compression point (B_{1dB}) with TIA setting2.

D.5.4 Noise Figure

Fig. D.21 shows the measured blocker noise figure with the blocker located at 51MHz offset. Note the simulated divider phase noise is -155dBc/Hz at 20MHz offset at 2GHz. In linear mode, the noise figure degrades quickly with increasing blocker power. In nonlinear mode, the noise figure is measured at different V_C and I_d settings to cover the blocker power range. For blocker power larger than -4.3dBm, the noise figure is smaller than the noise figure in linear mode. Because of the blocker suppression, the noise figure is determined by the NIS block and degradation due to reciprocal mixing is reduced.

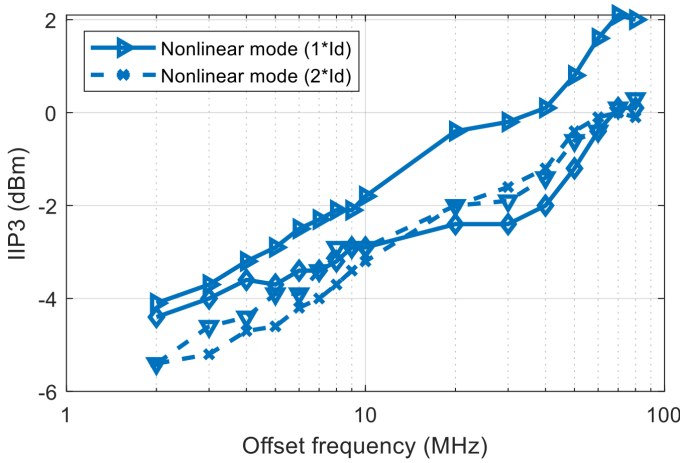

Figure D.20.: Measured IB-IIP3 in nonlinear mode over the blocker offset frequency.

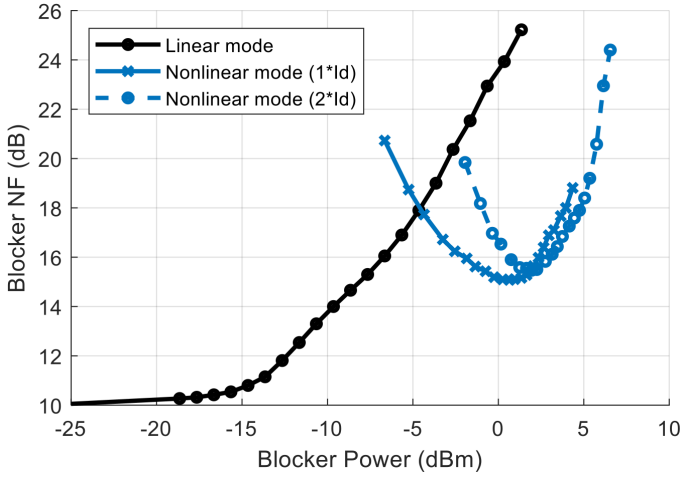

Figure D.21.: Measured blocker NF over blocker power in linear mode and nonlinear mode.

The blocker noise figure is 15.1dB or 15.5dB under a 0.65dBm or 1.95dBm, respectively.

This nonlinear receiver can be placed after an external LNA to reduce NF in applications that blocker power larger than 0dBm will not be encountered. Supposing with an LNA of 3dB noise figure and 10dB gain, the receiver will have a NF of 4.6dB in linear mode and 8.4dB in nonlinear mode with the presence of a -9.35dBm blocker power at 51MHz offset.

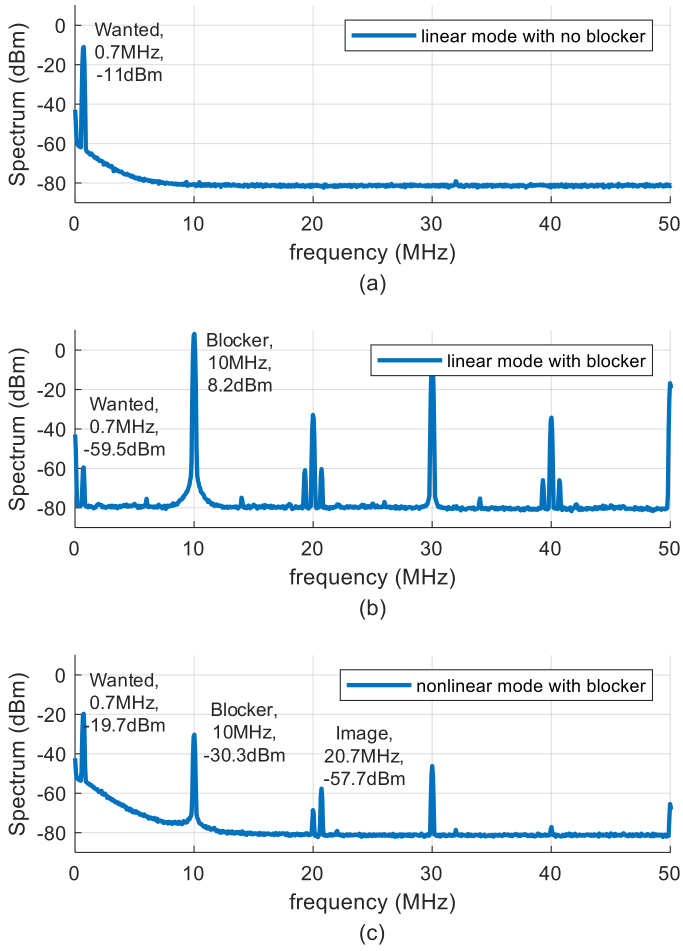

Figure D.22.: The measured down-converted output spectrum (a) with a -54dBm input small signal in linear mode, (b) with a 5.3dBm blocker at 10.7MHz offset in linear mode, (c) with the blocker in nonlinear mode.

D.5.5 SIR Improvement

Fig. D.22 shows the signal-to-interference ratio (SIR) comparison in linear mode and nonlinear mode. The measurement was made with LO at 1.5GHz, a 5.3dBm blocker at 1.49GHz and a -54dBm wanted signal at 1.5007GHz. The RF circuit consumes 14mW in linear mode and 8.7mW in nonlinear mode.

In Fig. D.22(a) without the blocker, the linear circuit provides 43dB gain and the small signal output is at -11dBm. In Fig. D.22(b) with the blocker, the receiver in linear mode is saturated by the large blocker. The blocker output is 8.2dBm. The small signal is attenuated by 5.5dB, at -59.5dBm. The SIR is

around -68dB. The baseband harmonics are clearly seen in the spectrum. In nonlinear mode as in Fig. D.22(c), compared with linear mode, the blocker is suppressed by 38.5 dB. At the same time, the small signal is amplified by 40dB. The SIR is now +10.5dB. Therefore 78.5dB SIR improvement is achieved with even less power consumption.

D.5.6 Comparison to State-of-the-Art

Table D.1 summarizes and compares the performance with other recently published wideband blocker-resilient receivers. Compared with [6], the frequency-independent blocker suppression is improved to more than 38dB for block power from 0dBm to 9.6dBm. For blocker NF, the result in this work is comparable with the result in [29] with PNC on, while consuming less power consumption. This work offers the best receiver performance when a strong blocker is present. In nonlinear mode, the receiver achieves more than 13dB OP_{1dB}/P_{DC} improvement, more than 30dB B_{1dB} improvement, and 78.5dB SIR improvement compared with in linear mode when the blocker is present.

D.6 Conclusions

A new wideband blocker-resilient receiver is introduced that utilizes nonlinear transfer function for simultaneous blocker suppression and weak signal amplification. This technique suppresses the strong blocker in the amplitude domain, independent of the offset frequency between the blocker and the wanted signal. Accordingly, it breaks the trade-off between blocker offset and receiver performance such as linearity, blocker NF, SIR and power consumption.

A prototype has been fabricated in a 40nm CMOS technology. More than 38dB blocker suppression is achieved for blocker power from 0 to 9.6dBm. 78.5dB SIR improvement with no extra power consumption under a 5.3dBm blocker is achieved in nonlinear mode operation compared with conventional linear mode operation.

Acknowledgment

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Table D.1.: Comparison with Other State-of-the-Art Blocker-Resilient Receivers

		JSSC'18 [45]	JSSC'12 [78]	JSSC'11 [51]	ESSCIRC'17 [68]	ISSCC'15 [29]	RFIC'12 [6]		This work	
Topology		Mixer-First	Noise Cancelling	LNA + N-Path Mixer	Adaptive Filter	Phase and Noise Cancelling	RF NIS		RF NIS + N-Path Mixer	
LO Generation		External	External	Integrated	Integrated	Integrated	N.A.		External	
CMOS Technology		45nm SOI	40nm	40nm	40nm	28nm	0.18um		40nm	
RF Frequency (GHz)		0.2 - 8	0.08 - 2.7	0.4 - 6	1.7 - 2.2	0.2 - 3	1.85		0.5 - 2.7	
Blocker suppression (dB) / Blocker power (dBm)		N.A.	N.A.	N.A.	N.A.	N.A.	30 / (0 $\sim$ 11dBm) 20 / ($-3 \sim$ 11dBm)		38 / (0 $\sim$ 9.6dBm) 20 / ($-4.4 \sim$ 9.6dBm)	
Blocker NF (dB), 0dBm blocker, $\Delta f = 80MHz$	Ideal LO, -174 dBc/Hz	4.7	4.1	13 (Δf=20MHz)	N.A.	5.5	12.8 $P_{blocker}$=2dBm		NL mode: 15.1 (0.65dBm) 15.47 (1.95dBm) (-155dBc/Hz @20MHz**)	
	Non-ideal LO, -141 dBc/Hz	32*			N.A.	32 (PNC off) 13.5 (PNC on)	N.A.			
Gain (dB)		22	70	70	20 - 36	60	17(L), 9.4(NL)		17 - 53	
IF BW (MHz		20	N.A.	0.5 - 30	N.A.	N.A.	N.A.		1 - 27	
Mode		N.A.					Linear	Nonlinear	Linear	Nonlinear
OB-B1dB (dBm) @100MHz		12.5	-0.5	N.A.	N.A.	-2.5	-1.9	N.A.	-7.5	4.6 $\sim$ 9.6
IB-B1dB (dBm) @1MHz		-10	-6 @30MHz	-20 @20MHz	3	N.A.			-25.7	$-2.8 \sim 8$
IB-IIP3 (dBm) @1MHz		5	-2.5	6	N.A.	N.A.	6.6	> 4	N.A.	$-4 \sim 2$***
OP_{1dB} / P_{DC} (dB)		N.A.	N.A.	N.A.	N.A.	N.A.	-6.7	4.6#	-2	14.6#
SIR improvement (dB) nonlinear vs. linear mode		N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	+78.5 $P_{blocker}$=5.3dBm
Power (mW)		56 - 290	32 (ex. LO)	30 - 55 (ex. PLL)	11 (RF) 11.5 (canceller)	12 (RF), 23 (BB) 11 (PNC)	3 (RF)	7 - 35 (RF)	14 (RF)	8.7 $\sim$ 15.7 (RF)
									16 (BB)	

*Estimated and/or interpreted form plots, figures and/or reported numbers. Summarized in [29].

**Post-layout simulation results of on-chip divider-by-4 at 20MHz offset.

***The setup of the IIP3 test here includes a strong blocker at the input besides two small tones.

#In nonlinear mode, virtual OP_{1dB} / P_{DC} = $P_{blocker} \cdot G_{SS}/P_{DC}$.

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Summary

Interference Suppression Techniques for RF Receivers

This thesis is dedicated to the investigation of interference suppression techniques that apply to 1) a multi-radio coexistence scenario; 2) a future spectral-efficient wireless system. We mainly focused on using a nonlinear-transfer (NIS) based technique to suppress strong interferers in a frequency-independent and power-efficient manner. In this thesis, we have analyzed the theory and modeling of the NIS receiver system, and also implemented a prototype in CMOS technology and verified the design through extensive measurements.

In Chapter 2, an overview of different communication standards in the sub-6GHz reveals the fact that strong interferers could accompany the small wanted signal at a small frequency offset. It causes degradation to signal integrity due to desensitization, intermodulation, reciprocal mixing, etc. Through reviewing the state-of-the-art, we found the current approaches are incapable of maintaining the receiver performance such as NF, linearity, power consumption and signal-to-interference ratio (SIR) while strong blocker is present. Furthermore, the performance further degrades with the increase of interferer power or the decrease of offset frequency. Hence we intend to investigate on interference suppression techniques that could improve the performance independence on the interferer power and offset frequency to a next level.

In Chapter 3, the nonlinear transfer based method was analyzed mathematically that the small signal gain and NF is dependent on the slope of the nonlinear transfer in different regions. System-level modeling of the NIS receiver verified the concept of interference suppression based on the amplitude difference between the strong interferer and the small wanted signal. The envelop extraction path requires high accuracy and small delay to maximize interference suppression and wanted signal quality.

To tackle the requirement on envelope extraction path, we have proposed an envelop detector topology in Chapter 4. It is based on quadrature signal

generation and 2nd harmonic cancellation to break the design trade-off between accuracy and delay, or in other words, ripple and detection bandwidth. The envelope detector was designed in 40nm CMOS and achieved 2% ripple, 0.64ns delay and 200MHz detection speed.

Chapter 5 presents the detail design and verification of the NIS receiver. In the presence of strong blocker, the RF transconductance amplifier operates in nonlinear mode and provides simultaneous blocker suppression and small signal amplification. This operation is frequency independent and happens at the first RF block, which is very beneficial for the performance and power consumption of the total receiver chain. To further suppress out-of-band interferers, frequency-translational filtering is used. We are using 8-path passive mixer with 12.5%-duty-cycle non-overlapping clock to suppression 3th and 5th harmonic down-conversion from the nonlinear RF block.

The chip implemented in 40nm CMOS is measured to provide more than 38dB suppression for blocker power from 0 to 9.6 dBm, in-band B1dB from -2.8 to 8 dBm and out-of-band B1dB from 4.6 to 9.6 dBm. This work also demonstrated superior receiver performance and power efficiency in nonlinear mode compared with linear mode under strong blocker. The virtual OP1dB is improved for 13dB. NF is improved by 10dB under a 1dBm blocker. SIR is improved by 78.5dB under a 5.3dBm blocker. These improvement holds for different offset frequencies and takes no extra power consumption.

Overall, this thesis has contributed to the development of nonlinear-transfer-based interference suppression techniques. Via both the theoretical study, and proposing and verifying the NIS receiver, the concept is proved to be unique to provide frequency-independent interference suppression and provide performance improvement from the current state-of-the-art approaches. It is promising for multi-radio coexistence and future spectral-efficient wireless systems.

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Chislehurst, May 2021

Biography

Kuangyuan Ying received the B.Eng degree in Microelectronics from Shanghai Jiao Tong University, Shanghai, China, in 2012 and the M.Sc. degree with Cum Laude in Electrical Engineering from Eindhoven University of Technology, Eindhoven, the Netherlands, in 2014. After Master studies, he was working towards the Ph.D. degree on the topic of interference-robust RF receiver techniques in the Integrated Circuit group, Eindhoven University of Technology. Since 2019, he is with MediaTek in Kent, UK, working on 5G cellular transceivers.

List of Publications

1. **K. Ying**, D. Milosevic, and P. Baltus, "A Reconfigurable Receiver with 78.5dB SIR Improvement under a 5.3dBm Blocker," in preparation of journal submission.

2. **K. Ying**, H. Gao, D. Milosevic, and P. Baltus, "An 8GHz Class-F_{23} VCO with 25% Tuning Range and Low Phase Noise and $1/f_3$ Corner Frequency," in preparation of journal submission.

3. C. A. M. Costa Júnior, C. Wang, **K. Ying**, Z. Chen, M. Dhaens, H. Gao, and P. Baltus, "Fully Integrated Tunable Wideband True Time Delay for Wireless Sensor Networks," *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019.

4. **K. Ying**, C. A. M. Costa Júnior, B. Wang, D. Milosevic, H. Gao and P. Baltus, "A Reconfigurable Receiver with 38 dB Frequency-Independent Blocker Suppression and Enhanced in-B and Linearity and Power Efficiency," *ESSCIRC 2018 - 44th IEEE European Solid State Circuits Conference (ESSCIRC)*, Dresden, 2018.

5. **K. Ying**, H. Gao, X. Min, D. Milosvic, and P.G.M. Baltus, "A Wideband Envelope Detector with Low Ripple and High Detection Speed," *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, 2018.

6. **K. Ying**, H. Gao, D. Milosvic, and P.G.M. Baltus, "A Nonlinear Transfer Function Based Receiver for Wideband Interference Suppression," *Journal of Sensors*, 2017.

7. H. Gao, **K. Ying**, M. Matters - Kammerer, P. Harpe, B. Wang, B. Liu, W. Serdijn, and P.G.M. Baltus, "60 GHz 5-bit digital controlled phase shifter in a digital 40 nm CMOS technology without ultra-thick metals," *Electronics Letters*, 2016.

8. H. Gao, **K. Ying**, M. Matters - Kammerer, P. Harpe, Q. Ma, A. van Roermund, and P.G.M. Baltus, "A 48–61 GHz LNA in 40-nm CMOS with 3.6 dB minimum NF employing a metal slotting method," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016.

9. B. Wang, H. Gao, **K. Ying**, M. Matters - Kammerer, and P.G.M. Baltus, "A 60 GHz phased array system evaluation based on a 5-bit phase shifter in CMOS technology," *2016 Symposium on Communications and Vehicular Technologies (SCVT)*, Mons, 2016.