# FORMAT: A Reconfigurable Tile-Based Antenna Array System for 5G and 6G Millimeter-Wave Testbeds

# FORMAT: A Reconfigurable Tile-Based Antenna Array System for 5G and 6G Millimeter-Wave Testbeds

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***Abstract*—This article introduces the FORMAT array, a reconfigurable millimeter-wave antenna array platform based on antenna tiles. FORMAT stands for Flexible Organization and Reconfiguration of Millimeter-wave Antenna Tiles, which is a unique hardware solution aiming to implement and demonstrate a variety of antenna array concepts, as well as different array architectures and configurations from the same basic module, providing even benchmark between different solutions and thus valuable insights into fifth-generation (5G) and beyond-5G antenna systems. The combination of a minimum-sized $2 \times 2$ tile with 3D-printed frame parts enables antenna arrays of a variety of sizes, allows multiple beamforming architectures, and a range of different antenna element positioning in the array. The hardware implementation is thoroughly described, with a few different array assemblies being manufactured and measured, validating their antenna performance with over-the-air measurements. Finally, using FORMAT hardware as both base station and user equipment, a 5-m wireless communication link was set up, achieving 4.8 Gbps downlink speed with QAM64 modulation.**

***Index Terms*—6G, antenna arrays, antenna tile, beamforming, fifth-generation (5G), massive MIMO.**

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## I. Introduction

THE ever-growing demand for higher data-rate and higher connectivity has led the fifth-generation (5G) of telecommunication systems to look at millimeter-waves (mm-waves), where bandwidth availability is higher [1]. Smart antenna solutions are at the forefront of 5G and future sixth-generation (6G) mm-wave research, in order to overcome the excess propagation losses and the high cost of components at those frequencies [2]. The enormous complexity of innovative antenna systems requires a joint effort between industry and academia, and within this context, the SILIKA consortium was put together between three leading European academic institutions, two key industrial players, and several other small and medium-sized enterprises. As the main goal, the consortium aims to research, integrate, and prototype innovative mm-wave multi-antenna massive multiple-input and multiple-output (MIMO) systems using silicon-based semiconductor technologies [3].

### A. Antenna Arrays in mm-Wave 5G

The use of high-gain antenna arrays with beamforming capabilities has been studied for base stations as a solution for the mm-wave propagation challenge in mm-wave 5G and beyond-5G systems. One possible approach is the focal plane array (FPA), which uses an antenna phased-array to feed a reflector, combining the beam-steering capabilities of antenna phased-arrays with the high gain and low cost of reflectors [4]. Irregular sparse arrays (ISAs) are also being investigated as a possible solution for base-stations. ISAs have a larger antenna aperture when compared to a dense array with the same number of elements, leading to narrower beams and thus promising spectral and energy efficiency improvement in massive MIMO scenarios [5], [6]. The high sidelobe issues with periodic sparse arrays can be improved by the use of space-tapered arrays, with densely

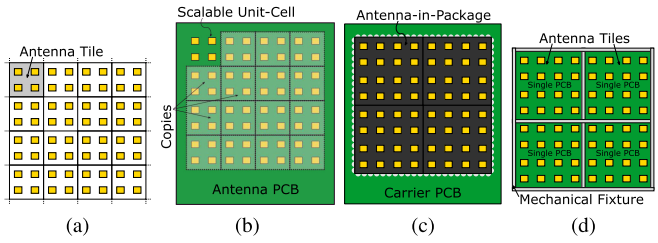



Fig. 1. Block diagram representation of antenna tile array implementation. (a) General antenna tile concept. (b) Scalable unit-cell approach. (c) Antenna-in-package approach. (d) Standalone tile approach.

spaced elements in the center and sparsity at the edges, providing antenna sparsity while simultaneously achieving low sidelobes [7], [8].

In addition to innovations on the radiating portion of the system, investigations on other array aspects are of great interest. One key area of research has been array architectures, with hybrid beamforming (HBF) offering an attractive trade-off between the low-cost and simplicity of analog beamforming (ABF) and the flexibility and performance of digital beamforming [9], [10]. However, HBF architectures come at the cost of limited angular sector width and the nonconvex nature of HBF problems [11], [12]. Besides architectures, the arrangement of antenna elements also appears to impact the overall performance. For example, the study in [13] reveals that signal linearity in the farfield strongly depends on array configuration.

With several variables to be considered when implementing antenna arrays for mm-wave 5G, it is extremely challenging to compare different antenna arrays on a leveled playing field. Many of the innovative antenna solutions available in the literature offer promising theoretical results but lack the experimental validation. Additionally, when hardware implementations are available, the comparison between multiple approaches can be unfair due to different components and measurements.

Therefore, one central idea has been the implementation of a reconfigurable antenna array hardware that could be used to implement and experimentally validate the different antenna concepts and architectures. This hardware should enable a quick and easy reconfiguration of the array, making it much more convenient to evaluate different antenna positioning and beamforming architectures. Furthermore, in addition to the various antenna concepts, the same hardware could be applied to implement a standard dense array with ABF to serve as a benchmark. Moreover, all topologies would be composed by the same basic module, leveling the different antenna concepts and providing a solid comparison reference.

### B. Prior Art

To address these requirements, a platform with Flexible Organization and Reconfiguration of Millimeter-wave Antenna Tiles (FORMAT) was conceived. The FORMAT is a novel antenna array system with a unique reconfigurability property based on an active antenna tile approach [14]. The tile approach of implementing phased-arrays is pictured in Fig. 1(a). A tile is a subset of the radiating elements, active elements, and signal distribution, all integrated in parallel layers. Each tile module is then positioned side-by-side, resulting in the large phased-array construction [15]. The challenge with the tile approach lies in the interconnection between modules. To overcome these challenges, three main approaches are seen in literature: scalable unit-cell, antenna-in-package, and standalone tiles.

*1) Scalable Unit-Cell:* The scalable unit-cell approach, pictured in Fig. 1(b), consists in grouping the tile elements during the design phase, designing a unit-cell structure which can be easily copied to scale the array to the desired size. All elements are then placed the same printed-circuit board (PCB). This approach is often an effective method to reduce overall costs and scaling of phased-arrays, as it can be implemented using low-cost PCB manufacturing, and allow easily build up of large arrays from the unit cell. However, any modification in the array configuration requires a board redesign, initiating a new development cycle, manufacturing, and debugging - not meeting the flexibility requirements for FORMAT. Nonetheless, this approach has been shown effective for the array implementation, especially when scaling is targeted. For example, the work from [16] implemented a $2 \times 2$ scalable unit-cell, which was then used to implement a larger $4 \times 8$ array in [17], scaling up the array. However, it required the manufacture and assembly of a new PCB, taking a large effort to change the array configuration. Similar approach is followed in [18], with a $4 \times 4$ unit cell used to build a $4 \times 16$ array.

*2) Antenna-in-Package:* The antenna-in-package (AiP) approach, pictured in Fig. 1(c), has been the preferred method by industry. It consists in integrating the radiating elements at the chip packaging level, leading to a component with a standard packaging (typically a ball-grid array) to be soldered onto a carrier PCB. The large array is then determined by the carrier PCB in which the AiP is assembled to.

The use of AiP simplifies the scalability of the array, providing high aggregated value for system houses. However, when it comes to flexibility, the AiP module can be reused but requires the redesign of the carrier PCB, falling on similar drawbacks as the scalable unit-cell approach. Moreover, AiP manufacturing requires high-cost substrates and low-tolerance manufacturing process, increasing substantially the overall costs and nonrecurring expenses (NRE). AiP, therefore, targets mass-production use-cases. The number of elements per tile is often large to justify the high NRE required, limiting the possible array configurations.

This approach was pioneered by IBM [19], effectively packaging 64 elements with four beamforming chips in a single AiP tile [20], [21]. The work from Qualcomm demonstrated a 16-element AiP tile in [22], which was used to build a $8 \times 16$ antenna array in [23].

*3) Standalone Tile:* The standalone tile approach, pictured in Fig. 1(d), consists in designing a self-contained tile that can operate on its own (aside from connectorized input). This approach is ideal for flexibility since each tile operates independently from the others. Therefore, building arrays with different sizes becomes a mechanical arrangement challenge rather than a

manufacturing challenge. Without a carrier PCB, a mechanical fixture is often required to keep each tile in place.

From a scalability point-of-view, the standalone tile is not as effective as the scalable unit-cell or the AiP method, where some of the functions to make a standalone tile operable can be synergized. With the standalone approach, each tile requires every component to make it operable—often a challenge with the limited real-estate of mm-wave antenna arrays. Nonetheless, as FORMAT is targeted to be a flexible platform to demonstrate several antenna array concepts, architectures, and configurations, the standalone tile approach is the most suitable.

Although the standalone tile approach has been used at mm-waves before [15], [24], they arise in a different context where mm-wave chip scale integration was not yet available. These works also had several constraints that led to the development of FORMAT, such as high-cost substrate and assembly, large minimum tile size, increased interelement spacing, and different targeted application. Therefore, with FORMAT, we targeted the development of a low-cost, flexible antenna array platform with a minimum $2 \times 2$ standalone tile, with 0.5 $\lambda$ spacing (where $\lambda$ denotes wavelength), to enable the experimental validation of the several concepts discussed in Section I-A.

### C. Contributions

The main contributions of this article are as follows.

1) We propose a novel mm-wave antenna array platform with an unique reconfigurability property. Here each tile operates as a standalone device, without requiring the use of a carrier for proper functioning. Instead, 3-D-printed components are used as holders to allow the antenna tiles to snap in position in a Lego-like manner. This enables a flexible and quick assembly of the array panel without requiring a complete redesign of the electronic components. In addition, as each tile operates standalone, the number of tiles used is not restricted, enabling the use of a single tile to emulate a user equipment (UE) as well as different sizes of arrays, with one axis limited to up to four elements. Furthermore, as each tile is fed individually, different beamforming architectures can be implemented. For that, the tile size is kept to a minimum of $2 \times 2$, allowing us to benchmark different beamforming architectures for arrays/sub-arrays, from a single-beam ABF to a multiple-beam HBF by using several RF chains.
2) The proposed system is designed, manufactured, and we present three distinct assembled configurations. These assemblies are validated, with over-the-air measurement results shown for both standalone tile and a $4 \times 8$ analog array assembly.
3) We demonstrate a wireless link by employing the proposed hardware as both base station and UE. A 4.8-Gbps downlink speed was achieved with QAM64 modulation over a 5-m distance, showing that, despite focusing on reconfiguration capabilities rather than pure array performance, the proposed platform achieves the requirements expected from 5G systems.

### D. Paper Outline

This article is organized as follows. Section II describes the problem to be solved by the proposed platform. An in-depth description of the reconfigurable hardware is laid out in Section III. Antenna measurements using the FORMAT platform are presented in Section IV, and link measurements are shown in Section V. A conclusion is given in Section VI.

## II. Problem Statement and System Design Decisions

The FORMAT array aims to be a platform to demonstrate multiple antenna array concepts, as described in the introduction. Therefore, several aspects should be taken into account.

- From the radiating element perspective, the demonstrator must enable both dense arrays and sparse arrays. Dense arrays can be used as a benchmark of a traditional implementation and also be employed as an antenna feed for the FPA concept, while sparsity between elements is also desired to be explored with the ISA/space-tapered antenna array concept. Therefore, the final system should allow a flexible positioning of the antenna tiles.
- Another desired aspect to take into account is the implementation of arrays with different sizes. While large arrays are interesting to emulate base-stations and small cells (SCs), smaller arrays are more suitable to emulate UE or customer premise equipment. This way, one single hardware implementation can be used on multiple nodes of the link in a testbed.
- In addition to different array sizes and antenna positioning, the FORMAT array also aims to allow different beamforming architectures, from full ABF all the way to having as many digital chains as possible.

Taking the aforementioned elements into perspective, we proposed a tile-based implementation. The tile approach offers the advantage to integrate many of the elements that make the array operational in a single block, such as the radiating elements, the beamforming chip, and connectors. Since reconfigurability is the target, the antenna tile was kept to a minimum size of $2 \times 2$, using a quad-channel analog beamformer chip. Having a minimum size tile offers more possibilities for antenna positioning as well as array sizes. Furthermore, the beamforming architectures are less limited, with a minimum subarray size of $2 \times 2$ for HBF configurations.

Naturally, to adjust for many opposing requirements, a few design choices were made to accommodate each requirement on a certain level. First, the form-factor of a $2 \times 2$ antenna array at 28 GHz is extremely small, and thus it is challenging to fit all required components within such a compact area. To avoid increasing intraelement spacing (IES) to accommodate all components, as done in [15], [24], a different approach was taken, in which extra space was gained by extending the tile on one edge while keeping the antenna array at the opposite edge. The downside of such an approach is the limitation to large-array configurations of a maximum of four elements in one direction of the array. Also, the implementation of sparse arrays is possible from a tile-to-tile level instead of an element-to-element level. Although not as optimal, since the tile has a

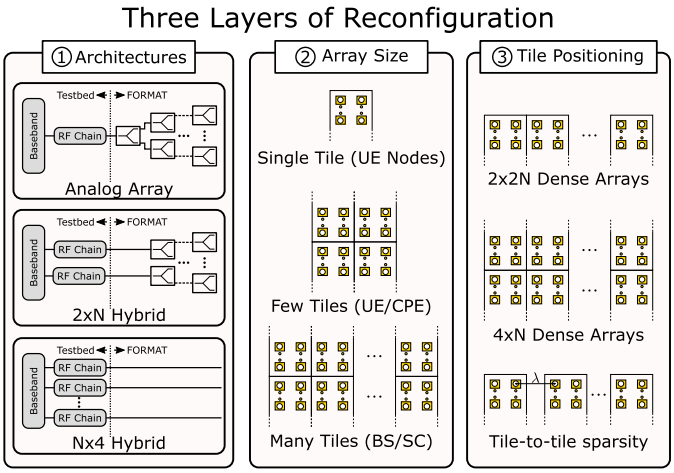



Fig. 2. Diagram with the three layers of reconfigurability of the FORMAT: multiple architectures, different array sizes, and several possibilities for tile positioning. UE, user equipment; CPE, customer premise equipment; SC, small cell; BS, base station.

minimum size of $2 \times 2$, the benefits of an ISA architecture can also be demonstrated using the same hardware. Despite these drawbacks, allowing up to four elements provides a good trade-off between hardware flexibility, beamsteering capabilities, and EIRP: While hardware flexibility is extremely challenging with a larger number of elements, the beam is narrower and effective isotropic radiated power (EIRP) is 6 dB higher when compared to two elements.

The reconfiguration possibilities can be summarized into three different layers, as visually described in Fig. 2. The first layer is related to the architecture, where multiple architectures can be used by changing the number of inputs and the number of tiles. With a single input and power splitters, a standard ABF architecture can be implemented. On the other hand, with several inputs, HBF with $2 \times 2$ analog subarrays can also be implemented. The second layer shows the different array sizes, with a single tile used to emulate a UE and multiple tiles to emulate a SC or base station. The third layer shows the different array configurations, with possibility for two or four elements in the vertical axis, as well as arbitrary spacing between each tile, emulating dense and sparse arrays.

Fig. 3 shows a block diagram of the primary usage of the FORMAT within a mm-wave testbed, such as MATE [25]. From the base station side, multiple tiles are combined in a single array, while individual tiles are used as UE nodes. As multiple streams feed each subarray, HBF can be used and thus several beams can serve each UE node, demonstrating massive MIMO scenarios. With multiple digital inputs, signal processing algorithms can be tested and benchmarked across several antenna array concepts, providing valuable insights on the real-life performance of each system.

## III. Array Assembly

To allow the desired reconfigurability, the array assembly is composed of several parts.

- An active antenna tile, composed of a $2 \times 2$ subarray with a quad-channel analog beamformer chip;
- a motherboard, which provides dc power and digital I/Os to the tile;
- a 3-D-printed array holder system, to build a large array and hold the tiles in place; and
- power splitter/combiner to enable analog arrays.

When compared to the conventional approach of integrating the whole array in a single PCB carrier, the proposed approach trades off its performance for flexibility. With many separate components to assemble one array versus a single PCB, the performance of key indices of the array (such as gain and efficiency) is degraded. However, it is important to highlight that the goal of the FORMAT platform is the demonstration of several antenna concepts with the same building blocks, leveling the playing field between implementations. From this perspective, this flexible implementation serves a better purpose, while also offering some other benefits, such as easy replacement of faulty elements without requiring a new assembly round. In this section, we describe the design and implementation of each of those parts, as well as a few final array assemblies to illustrate how those parts combine.

### A. Antenna Tile

The core of the reconfigurable array is the active antenna tile. It is composed of a $2 \times 2$ antenna array with an ABF chip and both RF and dc/digital I/O connectors.

*1) Board Stack and Antenna Elements:* The antenna design drives the substrate definition, and to minimize overall costs, a minimal stack was used to implement the tile consisting of two dielectric core layers of 406 $\mu$m ($\varepsilon_r = 3.38, \tan\delta = 0.0027 \,@\, 10\,\text{GHz}$) fixed by a same thickness PrePreg layer in between ($\varepsilon_r = 3.52, \tan\delta = 0.004 \,@\, 10\,\text{GHz}$). Both the circuit and radiating elements are then laid out in four metal layers (top, first-middle, second-middle, and bottom layers), and to further simplify the manufacturing process, only two types of vias were used, a through-hole via and a buried via between the top and first-middle layer, avoiding back-drilled vias [26]. Via size is also kept coarse at 250 $\mu$m to comply with aspect ratio limitations of low-cost PCB manufacturing [27]. The board-stack is pictured in Fig. 4.

The antenna elements used in the tile are depicted in Fig. 5, a proximity-fed patch antenna with a circular slot to enhance bandwidth. The bottom-two elements are mirrored in the vertical plane, which requires a $180^\circ$ phase-shift compensation from the beamforming IC. The antenna design targeted a low mutual coupling between elements, to reduce its impact on different array configurations. It was measured with probes, showing a mutual coupling level below $-12$ dB [26]. More details on the standalone antenna element design, dimensions, and performance are found in [26].

*2) Analog Beamforming Chip:* To obtain all the benefits from a HBF configuration, the module board was designed using the ABF integrated circuit from NXP. The analog beamformer has a 1:4 splitter/combiner and four individually controlled channels, where each channel utilizes a vector modulator to achieve a

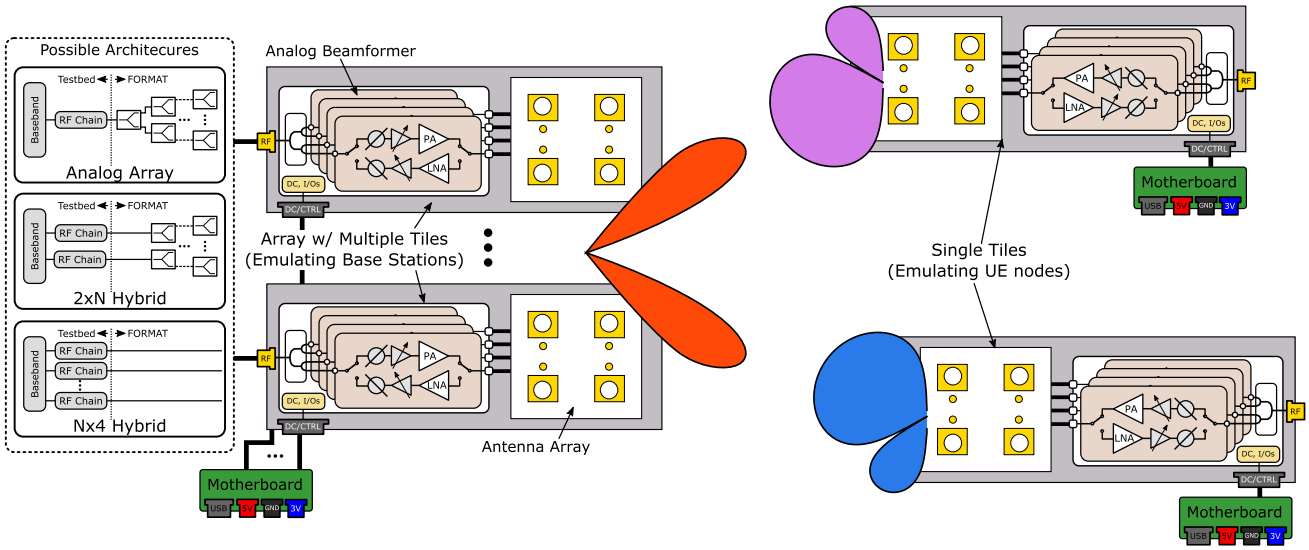



Fig. 3. Block diagram of the FORMAT usage in a multiple user scenario. Single tiles are employed as UE while many combined tiles are used as base station. Different base station implementations are possible, providing even benchmark between each antenna solution.

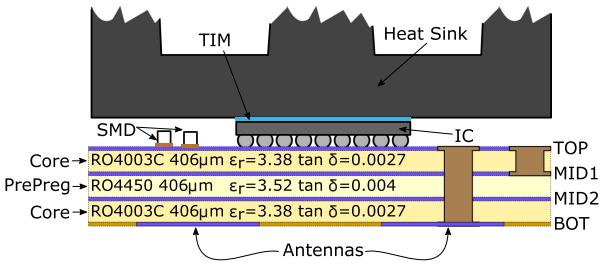



Fig. 4. Board stack and cross-sectional representation of the tile, with $\varepsilon_r$ and $\tan\delta$ given at 10 GHz.

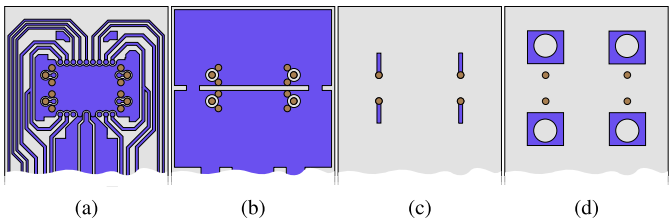



Fig. 5. Antenna design, indicating metal layers and vias at (a) top, (b) first-middle, (c) second-middle, and (d) bottom layers. Details on design and dimensions are given in [26].

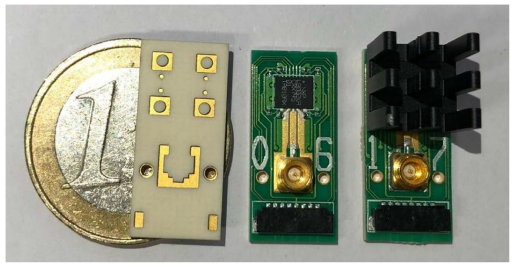


Fig. 6. Final assembly of the tile module, with dimensions 10 mm × 23 mm. The metal structures below the antennas were placed to increase the mechanical bond between connectors and PCB.

phase-shifting resolution of $5.625^\circ$ with an amplitude resolution of 0.4 dB while delivering up to 20 dB gain in Tx mode. It operates in both Tx and Rx modes, allowing the tile to be bidirectional. The control of the chip is performed through a serial bus. The chip's block diagram is shown in Fig. 3.

*3) Circuit Design and Final Tile:* The RF connection is delivered by a male subminiature push-on micro (SMPM) connector, with ≈0.2 dB loss and voltage standing wave ratio of 1:1.35 up to 40 GHz. It has a compact size of approximately $4 \times 4$ mm, and high performance at the aimed bandwidth. A co-planar waveguide was designed to bridge the signal between the RF connector and IC, as shown in the bottom of Fig. 5(a).

The dc and digital control connections were served to the module through a single connector, avoiding excessive cabling. To fit within a 10-mm width constraint, a 0.8-mm pitch connector from Hirose was selected (DF52-8S). Both dc and digital lines were routed in the top layer of the board, keeping board layers to a minimum. Isolation between radiating elements and dc/digital circuit traces is achieved through the first middle-layer ground plane [see Fig. 5(b)], which is also the patch antenna ground plane [26]. Based on the mentioned aspects, the tile board was designed and assembled. Its cross section is represented in Fig. 4. The finalized tile is $10 \times 23$ mm large, with two 1.2-mm holes added to allow the overall fixation to the antenna holder. In order to not influence the antenna behavior, poly(methyl methacrylate) plastic screws are used. The assembled board is pictured in Fig. 6. As one can see, the real estate in the tile is very limited, despite the extended side. To overcome the need of one extended side on a minimum size tile without increasing the IES, a general miniaturization of the connectors is needed.

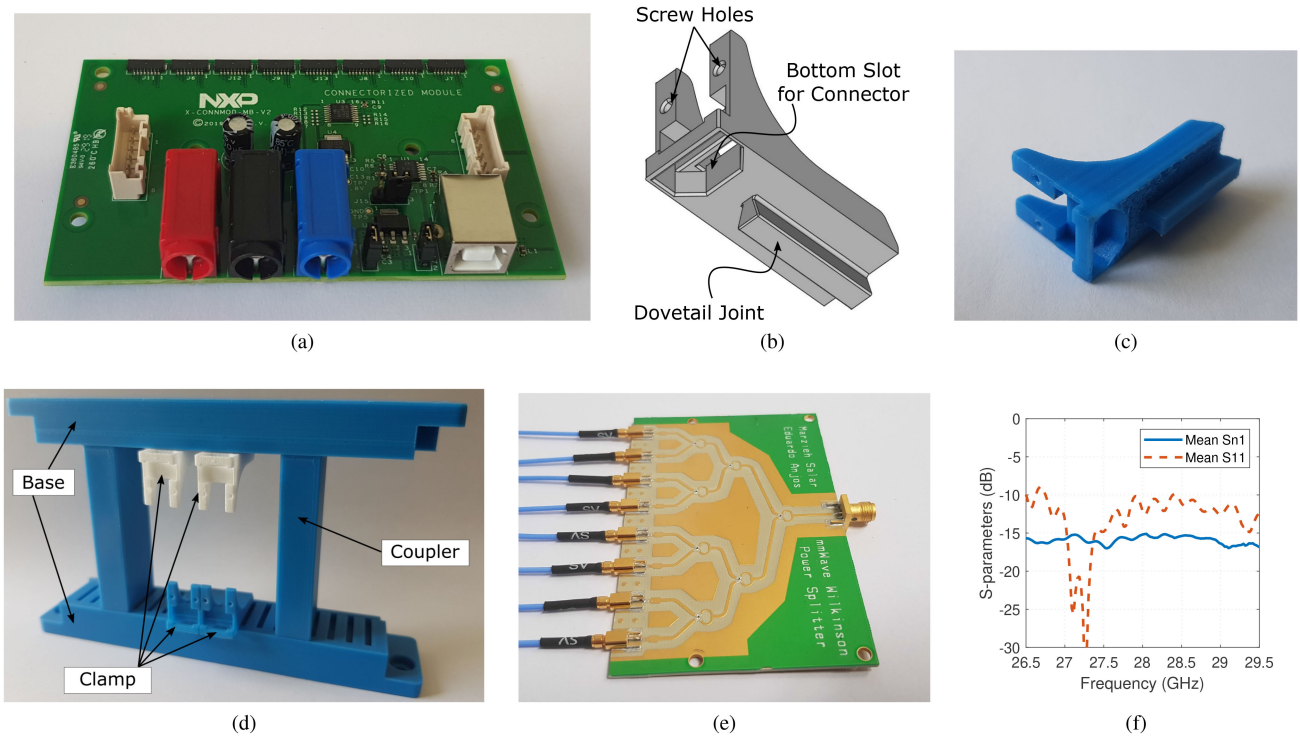



Fig. 7. Supporting building blocks. (a) Photo of the assembled motherboard. Row of dc/CTRL connectors on the top connect to the antenna tile. (b) Tile clamp 3-D design. (c) Photo of 3-D-printed tile clamp. (d) Photo of the 3-D-printed antenna holder parts interacting with each other. (e) Photo of the standalone power splitter. (f) Measured S-parameters of the standalone power splitter. Results show the average $S_{11}$ and $S_{n1}$, where port $n$ represents each output and port 1 the input.

### B. Supporting Building Blocks

To enable seamless assembly of the antenna array, several building blocks are needed, which are depicted in Fig. 7. The motherboard [Fig. 7(a)] provides the digital control and voltage biasing for the ABF chip through a single connector. An interface between controller and the elements is provided via USB. One motherboard can feed up to eight elements, and it can be cascaded with other boards to increase the number of controlled tiles.

Figs. 7(b)–(d) show the 3-D-printed system developed to assemble the tiles in place. It uses three components: i) a tile clamp to hold the antenna tile in place via plastic screws [Fig. 7(b) and (c)]; ii) a base to slide the clamp in place and attach the array in an enclosure; iii) a coupler to place two bases on top of each other thus enabling $4 \times N$ architectures, where $N$ is the number of antennas in the other direction. All components together are shown in Fig. 7(d). To change tile positioning, one can simply slide it in place via its dovetail joint. By changing the base design, the tile configuration can be changed as desired. For example, a special base could be 3-D-printed with dovetail slots concentrated in the center and sparse at the edges to implement a space-tapered array, with the minimum space limited to 0.5 $\lambda$.

To enable ABF architectures, a 1:8 Wilkinson power splitter was designed, pictured in Fig. 7(e). Its design used the same board stack as the tile (see Fig. 4). Fig. 7(f) shows the measured S-parameters of the standalone power splitter. An average transmission loss of 15 to 16 dB shows 6 to 7-dB insertion loss on top of a 9-dB splitting loss. The $S_{11}$ below $-10$ dB gives reasonable matching across the bandwidth.

### C. Final Assembly

Fig. 8 shows a few examples of possible assemblies, with a 5-V off-the-shelf cooling fan added to the assemblies to improve the tile temperature regulation. A standalone module is pictured in Fig. 8(a), which can be used as a receiver node in a MIMO testbed. In Fig. 8(c), a $4 \times 8$ analog array is pictured. The power splitter presented in Section III-B can be seen in Fig. 8(c) driving the tiles, enabling a fully analog architecture. Fig. 8(b) pictures a $2 \times 16$ HBF array with eight individual inputs to be used in a mm-wave massive MIMO testbed, such as [25]. These assemblies are some of the few possibilities of implementation using the system proposed here. The assemblies were designed targeting a 28-GHz carrier frequency, but can operate within the frequency range from 27 to 29 GHz.

## IV. Antenna Measurements

The assembled arrays were evaluated in different configurations using over-the-air measurements. Without loss of generality, we selected both the single tile [Fig. 8(a)] and the $4 \times 8$ analog array [Fig. 8(b)] to be characterized, since both have a single input. These measurements aim to demonstrate the capabilities of both the standalone tile and the large array.

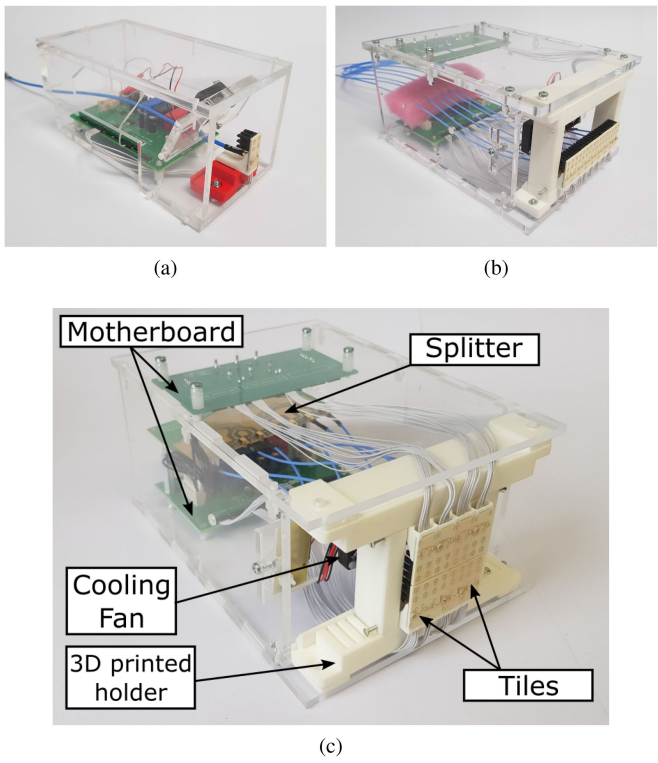



Fig. 8. Examples of assemblies of the FORMAT. (a) Standalone single tile ($2 \times 2$) to emulate receiver nodes. (b) $2 \times 16$ hybrid beamforming array. (c) $4 \times 8$ analog array with components annotated.

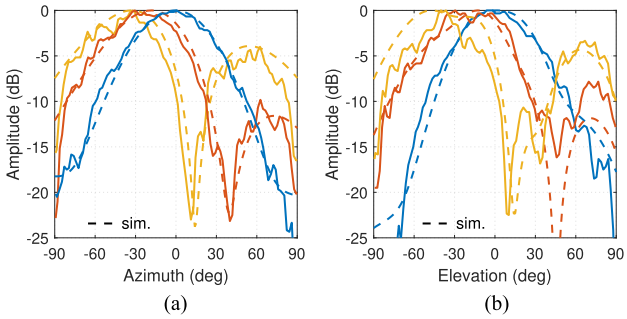



Fig. 9. Simulated and measured tile radiation patterns in Tx mode at $f = 27.5$ GHz and with the main beam steered to $0°$, $-15°$, and $-30°$ for both (a) H-plane and (b) E-plane.

## A. $2 \times 2$ Standalone Tile

The standalone tile configuration was measured over-the-air in an anechoic chamber, with the tile uncalibrated. The tolerance for these measurements is $\pm 0.5$ dB. To observe beam steering, the ABF chip was set to steer the beam broadside ($0°$), $+15°$, and $+30°$ in both horizontal (H-plane) and vertical (E-plane) plane without amplitude tapering. The simulated and measured radiation patterns were normalized, and then plotted in Fig. 9. Simulated results were obtained using CST. Since the number of elements in the standalone tile configuration is relatively small, it exhibits large sidelobes, as expected. The slight asymmetry observed in the E-plane is due to the elongated edge in the vertical axis. The standalone tile performance was also validated using a reverberation chamber, with the results shown in [28].

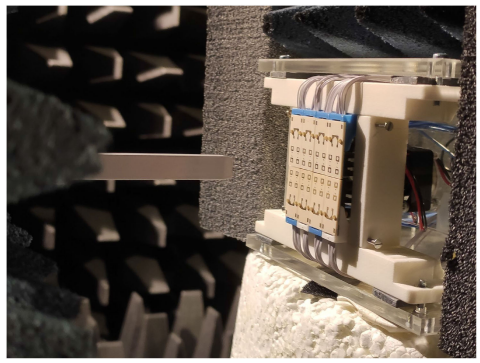


Fig. 10. Photograph of near-field scanner measurement setup.

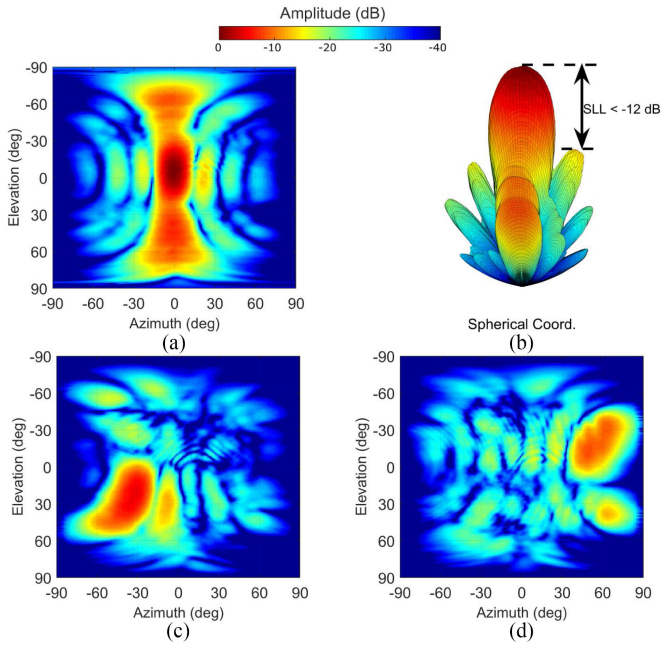



Fig. 11. 3-D normalized radiation patterns at 28 GHz without any array calibration. (a) Broadside colormap and (b) spherical coordinate plot for spatial visualization. (c) Beam steered to $-30°$ elevation, $-30°$ azimuth. (d) Beam steered to $+15°$ elevation, $+50°$ azimuth.

## B. $4 \times 8$ Analog Array

To evaluate the large array, we have selected the analog $4 \times 8$ configuration shown in Fig. 8(c). The analog array was then measured in an anechoic chamber using both far-field measurements and near-field scanner, with the latter used to obtain 3-D radiation patterns. Fig. 10 pictures the near-field scanner measurement setup.

Fig. 11 shows 3-D radiation patterns obtained using the near-field scanner, with all patterns obtained without any calibration of the array under test. The tolerance for these measurements is $\pm 0.5$ dB. Broadside radiation pattern is illustrated in Fig. 11(a) and (b), with a colormap and a spherical coordinate plot for 3-D visualization. The broadside pattern shows a sidelobe level below $-12$ dB in the azimuth, where eight antenna elements are

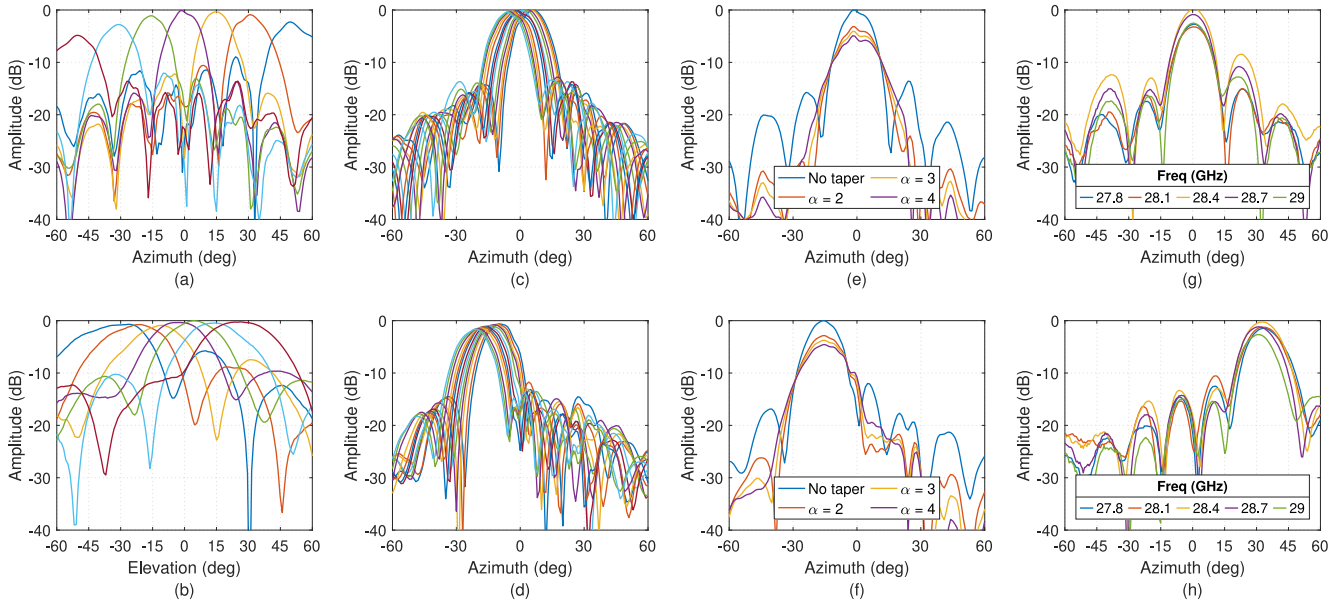



Fig. 12. 2-D normalized radiation patterns at 28 GHz without any array calibration. (a) Beamsteering in H-plane. (b) Beamsteering in E-plane. (c) Fine resolution steering around broadside beam, with $1^\circ$ steps. (d) Fine resolution steering around $-15^\circ$ azimuth beam, with $1^\circ$ steps. (e) Cosine alpha amplitude tapering of broadside beam for different alpha values. (f) Cosine alpha amplitude tapering of $-15^\circ$ azimuth beam for different alpha values. (g) Radiation pattern vs. frequency for broadside beam. (h) Radiation pattern vs. frequency for beam steered at $+30^\circ$ azimuth.

placed. 3-D beam steering is shown in Fig. 11(c) and (d), with the beam steered to different angles. Notice a wider spread over elevation than azimuth, due to a smaller number of elements. The smaller number of elements can also explain the higher sidelobes in Fig. 11(c) and (d), as the beam is steered toward endfire. Another possible cause for the sidelobes is the use of an uncalibrated array, where the difference between tiles is not mitigated.

For better visualization, Fig. 12 shows cuts in both H-plane (elevation $= 0^\circ$) and E-plane (azimuth $= 0^\circ$). All patterns are obtained without any array calibration. We performed beam steering in azimuth, resulting in Fig. 12(a), steering the beam from $\pm 50^\circ$ in several steps, with the beams steering to the correct location. Steering was also performed in elevation from $\pm 30^\circ$ in $15^\circ$ steps, shown in Fig. 12(b). The smaller number of elements in the vertical direction leads to a broader beamwidth. Fig. 12(c) and (d) shows fine-resolution beamsteering in azimuth. Each beam has $1^\circ$ step between them, around the broadside beam and around $-15^\circ$ azimuth beam. The fine resolution is achieved due to a phase-shifting resolution of $5.6^\circ$ of the analog beamformer chip.

To demonstrate amplitude control, Fig. 12(e) and (f) shows both broadside beam and $-15^\circ$ azimuth beam under a cosine tapering window ($\cos^\alpha(\cdot)$). Tapering is applied in azimuth, and the coefficients are shown in Table I. Without tapering, the first sidelobe is expected to be around $-12$ dB, as seen in Fig. 12(e) and (f). By applying tapering, a lower sidelobe-level is achieved, however with the expense of a lower peak amplitude and larger main beamwidth.

Variation over frequency for different beams is shown in Fig. 12(g) and (h). Since the beamforming chip uses phase-shifters instead of true-time delays, beam squint can be observed in [29]. Variation in magnitude and SLL is also seen, with SLL kept below $-8$ dB across different beams and different frequencies. The maximum magnitude variation is kept below 3 dB across 1.2 GHz.

TABLE I
APPLIED ATTENUATION SETTINGS PER COLUMN, IN DB, FOR DIFFERENT AMPLITUDE TAPER

| | Attenuation (dB) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Element column** | **#1** | **#2** | **#3** | **#4** | **#5** | **#6** | **#7** | **#8** |
| **No taper** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $\alpha = 2$ | 11.2 | 6.4 | 2.4 | 0.4 | 0.4 | 2.4 | 6.4 | 11.2 |
| $\alpha = 3$ | 14.8 | 8.8 | 3.6 | 0.4 | 0.4 | 3.6 | 8.8 | 14.8 |
| $\alpha = 4$ | 17.6 | 11.2 | 4.4 | 0.4 | 0.4 | 4.4 | 11.2 | 17.6 |

Fig. 13(a) and (b) shows the measured scan loss vs. angle for both H- and E-plane. A scan loss of 4 dB is observed with a scanning from $\pm 50^\circ$ in the H-plane and above 3 dB for a $\pm 30^\circ$ scan range in the E-plane. Differences between Tx and Rx mode are observed due to the different active components used in each mode. Antenna calibration could mitigate those variations. Scan loss variation over frequency is shown in Fig. 13(c), with losses better than 4.5 dB from 27 to 29 GHz. Cross-polarization level versus scan angle is shown in Fig. 13(d) for both H-plane and E-plane, with results showing a cross-polarization level below $-20$ dB over the desired scan range.

## V. LINK MEASUREMENTS

To evaluate system capacity and constellation quality of the FORMAT platform from a noise and distortion perspective, a 5-m link measurement setup was developed, as shown in Fig. 14. Using the arbitrary waveform generator M8190A combined with the signal generator PSG E8267A, we are capable of generating modulated signals with a bandwidth up to 2 GHz. To keep the signal generation equipment operating at its optimal point, a power amplifier is added prior to the array, working on its linear

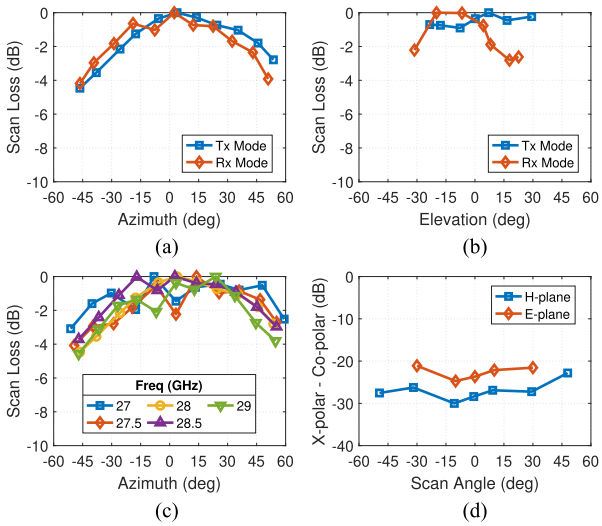
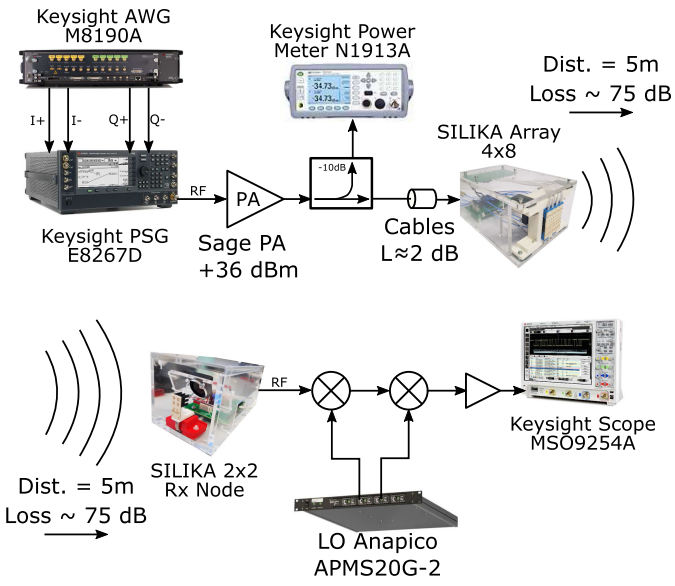



Fig. 13. Measured scan loss and cross polarization levels for different scanning angles. (a) Scan loss in the H-plane at 28 GHz for different operation modes. (b) Scan loss in the E-plane at 28 GHz for different operation modes. (c) Scan loss in the H-plane, Tx mode, for different frequencies. (d) Cross-polarization level vs. scan angle for both H- and E-planes.



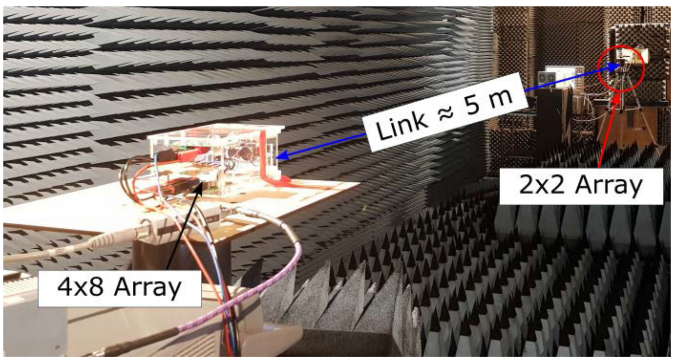



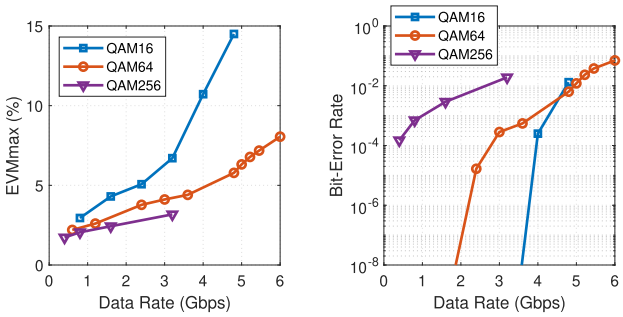

Fig. 14. Link measurement setup. (a) Block diagram. (b) Setup photo.

region to mitigate any influence of the PA into the input signal. A directional coupler with a power meter is used prior to the array to assess the average input power, thus estimating the array EIRP at a given signal level. The array selected as a transmitter node had a dense $4 \times 8$ configuration with a 1:8 power splitter, thus having a single input and using ABF.

On the receiving side, 5 m apart, a single tile ($2 \times 2$ configuration) is used to emulate a UE node. The received signal is downconverted in two steps as the equipment used for the local oscillator has maximum frequency limited to 20 GHz. The downconversion brings the signal to an intermediate frequency of $\approx 1$ GHz, which is then acquired by the scope. Since only a line-of-sight component is present, we have considered a free-space line-of-sight channel for the link measurements. Using MATLAB, we extract the constellations from the time-domain signal acquired by the scope, applying typical signal-processing corrections during postprocessing. This procedure corrected carrier-frequency and phase offset, I/Q imbalance, bandpass filtering, and amplitude equalization. Since the transmitted signal is known, we can compare the received constellation with it, obtaining the error vector magnitude (EVM) and the bit-error rate (BER) [30]. It is important to highlight the following: 1) Through this article, all EVM results will be reported normalized by the maximum constellation magnitude, i.e., using the $\text{EVM}_{\text{max}}$ definition from [31]; 2) measurements were performed without any array calibration.

With both arrays in broadside, we measured several constellations using QAM16, QAM64, and QAM256 modulation schemes under different symbol rates up to 1.2 Gbaud. The carrier frequency was fixed at 28.5 GHz and the constellations were drawn with 10 000 points. The results are summarized in Fig. 15. Fig. 15(a) shows the EVM in percentage with respect to data rate, and Fig. 15(b) shows the BER vs. data rate obtained after 10 000 symbols. EVM is kept below 5% up to 4 Gbps when QAM64 is used, and below 12% for QAM16. For QAM256, EVM is kept below 2.5% up to 1.6 Gbps, with the BER degrading above 1% for 3.2 Gbps (400 Mbaud). Although EVM for QAM64 is lower than QAM16 for higher data rates, a more complex constellation leads to higher bit-error rates. BER is kept below 0.1% up to 4 Gbps using QAM64 and up to 4.4 Gbps using QAM16. However, between 2.4 and 4 Gbps, no errors were obtained, in a 10 000 symbol run, using QAM16, indicating a better choice for lower errors, with the price of higher bandwidth. Fig. 15(c) shows selected constellations for each modulation scheme. With low data rates, constellation points are clear, and overlap between symbols is not observed. With higher data rates, the constellation points spread out around the center.

To evaluate EVM performance versus power, we have fixed the constellation modulation scheme and data rate, and observed the effect on EVM as power is increased. Results are shown in Fig. 16, where QAM16 with 600 Mbaud and QAM64 with 400 Mbaud were selected. In order to preserve sensitive data, all absolute power values in Fig. 16(a) were normalized with respect to the output power backoff, which is the difference between array EIRP and the EIRP at the 1-dB compression point. Due to a higher peak-to-average power ratio (PAPR) in more

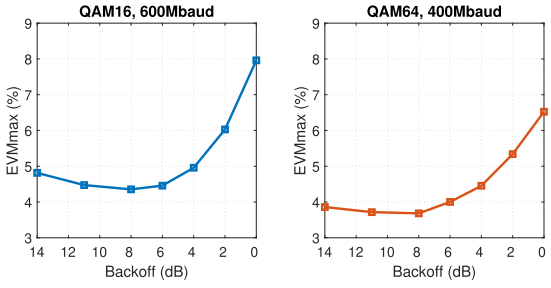



(a) (b)

| QAM16 | QAM64 | QAM256 |
|---|---|---|
| 800 Mbps | 600 Mbps | 400 Mbps |
| EVM = 2.95% | EVM = 2.201% | EVM = 1.726% |
| BER = 0 | BER = 0 | BER = 1.5e-4 |
| 4 Gbps | 4.8 Gbps | 1.6 Gbps |
| EVM = 10.72% | EVM = 5.782% | EVM = 2.432% |
| BER = 2.5e-4 | BER = 6.3e-3 | BER = 2.9e-3 |

(c)

Fig. 15. Link measurement results for different modulation schemes and data rates. (a) Measured EVMmax vs. data rate. (b) Measured bit error rate (BER) vs. data rate. (c) Selected measured constellations.




(a)

| QAM16 600 Mbaud | | QAM64 400 Mbaud | |
|---|---|---|---|
| 6 dB Backoff | 0 dB Backoff | 8 dB Backoff | 0 dB Backoff |
| EVM = 4.458% | EVM = 7.961% | EVM = 3.683% | EVM = 6.523% |
| BER = 0 | BER = 0 | BER = 5e-5 | BER = 1.6e-2 |

(b)

Fig. 16. Measured EVM for different power backoff levels. (a) EVMmax vs. backoff for QAM16, 600 MBaud (left) and for QAM64, 400 MBaud (right). (b) Selected constellations shown linear and compression operations.

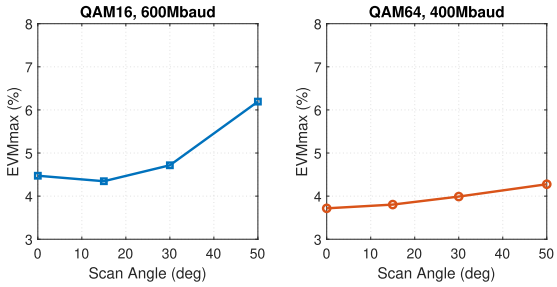



Fig. 17. Measured EVMmax vs. scan angle for QAM16, 600 MBaud (left) and for QAM64, 400 MBaud (right).

| QAM16 | | QAM64 | |
|---|---|---|---|
| 4 Gbps | 5 Gbps | 2.4 Gbps | 4.8 Gbps |
| EVM = 8.765% | EVM = 11.76% | EVM = 4.364% | EVM = 6.232% |
| BER = 5e-5 | BER =2.1e-3 | BER = 5e-5 | BER = 1.3e-2 |

Fig. 18. Measured constellations with both FORMAT 2×2 receiver node and FORMAT 4×8 analog array with 30° steering.

complex modulations, the EVM increase for QAM64 begins between 8 and 6 dB backoff, while for QAM16, it starts around 6 dB backoff. This result is consistent with the theoretical PAPR values of QAM16 (6.6 dB) and QAM64 (7.7 dB) after passing through a root-raised cosine filter (a rolloff factor of 0.35 was used) [31]. Fig. 16(b) shows the two selected constellations around their optimal backoff and without backoff. Notice that, without backoff, distortion starts to appear at the corners. This leads to symbol errors, as visible from QAM64-0 dB backoff plot.

We also characterized EVM performance versus scan angle. Assuming a symmetrical performance, we have only rotated the transmitter array one side while keeping the receiver node fixed. The transmitter was rotated from broadside to 15°, 30°, and 50°, while simultaneously steering the beam toward the receiver to compensate the rotation. The input power was kept at 11 dB backoff. Results are shown in Fig. 17, where the EVM for QAM64 400 Mbaud is less affected by the scan loss than QAM16 600 Mbaud. We suspect that this effect is mostly due to the limited dynamic range of the scope, as the larger bandwidth signal has its SNR more affected by the beamsteering scan loss. Such effect could be overcome by an increase in power, up to 6 dB backoff.

The final measurement consisted of rotating both the transmitter and receiver array by 30°, while pointing both beams to each other. Under this setup, we aim to demonstrate the system capability to fully emulate antenna arrays at UE side. Under such setup, several constellations were measured, as shown in Fig. 18. Certain configurations, such as QAM16 4 Gbps, performed even better at the rotated angle when compared to broadside, most likely due to lack of calibration. Nonetheless, these constellations demonstrate the capability of the proposed system to perform beamforming at both sides of the link, emulating real mm-wave communication systems.

TABLE II
STATE-OF-THE-ART 28 GHZ TILE-BASED PHASED-ARRAYS

| **Reference** | **This Work** | IBM/Ericsson 2017 [20], [21] | UCSD 2018 [16], [17] | Qualcomm 2018 [22], [23] | TokyoTech 2020 [18] |
|---|---|---|---|---|---|
| **Frequency (GHz)** | **28** | 28 | 28 | 28 | 28 |
| **IC Integration** | **RF Beamformer** | RF/IF beamformer, up/down conversion from/to 3-GHz IF | RF Beamformer | RF beamformer, up/down conversion from/to 6-GHz IF, PLL | RF Beamformer |
| **Antenna array configuration** | **4x8 (32)** | 8x8 (64) | 4x8 (32) | 8x16 (256) | 4x16 (64) |
| **Elements per tile** | **2x2 (4)** | 8x8 (64) | 2x2 (4) | 4x4 (16) | 4x4 (16) |
| **Type of tile** | **Standalone** | AiP | Scalable unit-cell | AiP | Scalable unit-cell |
| **Element Spacing** | **x:** $0.5\lambda$**; y:** $0.5\lambda$ | x: $0.59\lambda$; y: $0.59\lambda$ | x: $0.5\lambda$; y: $0.63\lambda$ | x:$0.5\lambda$; y: $0.5\lambda$ | x: $0.6\lambda$; y: $0.6\lambda$ |
| **Antenna Integration Approach** | **PCB (4-layer)** | Organic build-up package (14-layer) | PCB (4-layer) | Organic HDI package | PCB (7-layer) |
| **Calibration** | **No** | Yes | No | No | Yes |
| **Over-the-air data rate** | **5 Gbps 16-QAM @ 5m 4.8 Gbps 64-QAM @ 5m** | 6.7 Gbps 64-QAM @ 50m | 6 Gbps 16-QAM @ 5m 3 Gbps 64-QAM @ 5m | 100 MHz OFDM 64-QAM @ 2m | 15 Gbps 64-QAM @ 1m 6.4 Gbps 256-QAM @ 1m |
| **Supported Antenna Polarizations** | **Tx: single Rx: single** | Tx: dual Rx: dual | Tx: single Rx: single | Tx: dual Rx: dual | Tx: dual Rx: dual |
| **Reconfigurability** | **Architecture (HBF/ABF) Array Size Tile spacing** | No | No | No | No |

Table II summarizes the performance of the proposed work versus the state-of-the-art. When compared to the other tile-based phased-arrays, the FORMAT platform achieved a competitive performance, with the added benefit of its reconfigurability property.

## VI. CONCLUSION

In this article, we have introduced the FORMAT platform, a mm-wave tile-based antenna array with one-of-a-kind reconfigurability property. The reconfiguration possibilities are threefold: First, several beamforming architectures are enabled, from a single-input ABF to a multiple-input HBF; second, different array sizes are possible, from a single tile to emulate UE to a large array with many tiles to emulate base station, with one axis limited up to four elements; finally, the positioning of each tile can be arranged at will, enabling dense arrays, or sparse arrays, on a tile-to-tile basis. Different combinations of these layers enable a new array configuration, which can be benchmarked against other configurations on a leveled playing field. The hardware implementation was then thoroughly described, with a few different configurations implemented, assembled, and measured. The antenna characteristics were evaluated for both a single tile as well as a large ABF analog array, and a wireless link was built between the two parts, demonstrating a 4.8-Gbps data rate using QAM64 at 28.5 GHz.

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