3D-Integration on Wafer Level of Photonic and Electronic Circuits

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3D-Integration on Wafer Level of Photonic and Electronic Circuits

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by Marc Spiegelberg

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Cover designed by Marc Spiegelberg based on a microscope picture of the integrated indium phosphide wafer with partly removed substrate (Appendix B, step 54).
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Dedicated to my Ohana

"Hawaiian Vibes" painted by Merel van Eck

Summary

3D-Integration on Wafer Level of Photonic and Electronic Circuits

A novel integration technique is demonstrated for the first time. It combines state-of-the-art photonic wafers, based on generic indium phosphide (InP) technology, with matching electronic wafers, realized with bipolar CMOS (BiCMOS) technology. The new technique encompasses adhesive wafer bonding and through-polymer electrical interconnects.

Optical modules used for datacenters and telecommunication face bandwidth limitations based on the non-optimal electrical interfaces between photonic and electronic integrated circuits (ICs). One possibility to improve the performance of the electrical connections is to simply shortening them, and thereby reduce the parasitic characteristics. With adhesive bonding it is possible to bring the photonic and electronic circuits in close contact. The intermediate polymer layer functions as an optical, electrical and thermal isolator. Bonding is performed on a wafer scale level and thus enables maximum scalability. The photonic wafer is reduced to its functional epitaxial layer stack, by removing the “useless” substrate on which the circuits are initially realized, which makes it possible to etch through the remaining membrane and the bonding layer to create electrical connections between the photonic and electronic ICs. This 3-D integration technique offers new design possibilities regarding placement of I/O’s and functionalities.

In this work a design and process flow is created, taking into account the different wafer sizes by dicing a 200 mm BiCMOS wafer into several identical 3-inch wafers to match the InP wafer dimensions. The photonic layout is designed to match the electronic one. Bonding these wafers, which have topologies of several microns, with alignment accuracies of less than 4 μm is achieved. A process to create the electrical interconnects is developed and is successfully demonstrated.

To monitor the photonic devices during the processing, vertical mirrors and several test structures are implemented. These have been used to characterize the impact of the integration technology on the device performance. Passive components show only minimal changes in performance, due to the added adhesive polymer, which functions as a cladding, and to the thermal expansion of the photonic membrane, resulting from the different coefficients of linear thermal expansion. Active components have been included to enable data transmission experiments. The modulated optical signal is generated with an electro-absorption modulator (EAM) and detected with a PIN photodiode (PD). The small signal response measured after the integration process is 16.5 GHz (EAM) and 27.5 GHz (PIN PD), respectively. As light source a distributed feedback (DFB) laser is integrated. Its performance suffers strongly from the lack of a cooling element at the photonic membrane side. A series of DFB laser is used with Bragg wavelengths between 1545 and 1554 nm. An average optical power of 48 μW (coupled into a fibre) is measured for injection currents up to 45 mA.

In cooperation with the TU/e IC-group and Ghent University hybrid transmitter (TX) and receiver (RX) designs have been created to demonstrate the feasibility of this new integration technology. The RX module achieved a data transmission rate of 10 Gbits/s, which is limited by the used electronic circuit design. In case of the TX, a data transmission experiment of the hybrid module is not performed as the EAM bias point does not match the initial design value. However, characterizing the photonic circuit itself showed open eye diagrams for bit rates up

to 25Gbit/s and a bit error rate (BER) of 3E-9 for 12.5 GBit/s.
The results achieved, show the feasibility of this new 3-D integration technology. Further development, in particular regarding thermal management and optical interfacing, will make it suitable for industrial applications.

List of abbreviations

μTP	micro transfer printing
ALD	atomic layer deposition
AR	anti-reflection
ASE	amplified spontaneous emission
AWG	arrayed waveguide grating
BB	building block
BER	bit error rate
BERT	bit error rate tester
BiCMOS	bipolar CMOS
BPG	bit-pattern generator
BSA	backside alignment
CBB	composite building block
CMOS	complementary metal oxide semiconductor
CTE	coefficient of linear thermal expansion
CW	continuous wave
DC	direct current
DFB	distributed feedback
DUT	device under test
EAM	electro-absorption modulator
EBR	edge bead removal
EDFA	erbium-doped fiber amplifier
EIC	electronic integrated circuit
EUV	extreme ultra violet
FP	Fabry-Perot
FPR	free propagation region
FSR	free spectral range
GDSII	graphic design system II
GSG	ground-signal-ground
HHI	Fraunhofer Institut for Telecommunication, Heinrich Hertz Institut
IC	integrated circuit
ICP	inductively coupled plasma
ICP-CVD	inductively coupled plasma chemical vapour deposition
IL	insertion loss
IMOS	InP membrane on silicon
IP	intellectual property
IR	infrared
LCA	lightwave component analyser
LNA	low noise amplifier
MMI	multi mode interferometer
MPW	mutli project wafer
MZI	Mach Zehnder interferometer
NRZ	non return to zero
OSA	optical spectrum analyser
PCB	printed circuit board
PD	photodiode
PDK	process design kit
PIC	photonic integrated circuit
PRBS	pseudorandom binary sequence
RF	radio frequency
RIE	reactive ion etching
RX	receiver

SEM	scanning electron microscope
SMF	single mode fiber
SMP	Smart Photonics
SMSR	side mode suppression ratio
SOL	short open load
SOP	state of polarisation
SSC	spot size converter
TEC	thermoelectric cooler
TIA	transimpedance amplifier
TPV	through polymer vias
TU/e	Eindhoven University of Technology
TX	transmitter
UHNA	ultra high numerical apperature
UV	ultra violet
VNA	vector network analyser
VOA	variable optical attenuator
WDM	wavelength devision multiplexing
WGT	waveguide transition

List of chemicals

$\mathbf{Al_2O_3}$	aluminium oxide
$\mathbf{AlF_3}$	aluminium fluoride
BCB	benzocyclobutene
$\mathbf{CHF_3}$	fluoroform
$\mathbf{H_2O}$	water
$\mathbf{H_2O_2}$	hydrogen peroxide
$\mathbf{H_2SO_4}$	sulfuric acid
$\mathbf{H_3PO_4}$	phosphoric acid
HCl	hydrochloric acid
HMDS	hexamethyldisilazane
InGaAs	indium gallium arsenide
InP	indium phosphide
IPA	isopropanol
KCN	potassium cyanide
KOH	potassium hydroxide
$\mathbf{N_2}$	nitrogen
$\mathbf{O_2}$	oxygen
Si	silicon
$\mathbf{SiN}_x$	silicon nitride
$\mathbf{SiO_2}$	silicon dioxide

Contents

Chapter 1

Introduction

One of the most cited statements in electrical engineering is the prediction of Gordon E. Moore [1], which says that the density of electrical components in electronic integrated circuits (EICs) is doubling roughly every two years. A similar trend can be seen for photonic integrated circuits (PICs) [2, 3] (see figure 1.1). The increase of PICs density requires corresponding EICs, to provide the necessary electronic control interfaces. However, this introduces the question on how to integrate the electronic and photonic circuits. One example on how to combine both circuits is placing them side-by-side and connecting them electrically via wire bonds. This technique is limited by the physical boundaries (number, length and uniformity of the wire bonds) and the achievable bandwidth. Alternative solutions on how to integrate photonics and electronics are proposed in literature. An overview of the most relevant concepts will be given in the next section. At the end of this chapter a motivation is given and the content of the thesis is listed.

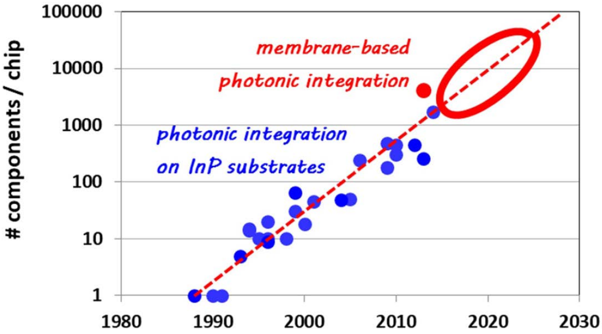

Figure 1.1: Moore's law for photonics: number of components per chip plotted for the year of publication, originally published in [2]

1.1 Existing integration concepts

Classical photonic and electronic circuits are fabricated within different technologies and material systems. Electronics is based on silicon (Si) and is fabricated using complementary metal oxide semiconductor (CMOS) technology, or a similar one. For photonic components the used material depends on the desired wavelength range. Within this work the focus is on near infrared light, which is used for optical communication. Compositions of III-V materials especially those based on indium phosphide (InP), are used for this purpose.
The integration of photonics with electronics can be achieved by including both functionalities within one of the existing technologies (monolithic integration) or by combining them (heterogeneous integration).

Monolithic: InP
For InP this means the realization of electronic circuits. This is possible and has been demonstrated [4]. The InP material system offers transit frequencies of beyond 400 GHz at breakdown voltages of 5.5 V [5], which makes it suitable for high speed EICs. However, due to the fact that InP wafers are expensive and not available in large sizes, the use of this material is still limited to specialized electronic application [6].

Monolithic: CMOS
CMOS technology is providing Si wafers with diameters up to 450 mm. The fabrication processes are highly optimized and can achieve 7 nm nodes by using extreme ultra violet (EUV) lithography. This facility is the motivation for the rapidly growing interest in silicon photonics. Any platform that uses a Si based waveguide structure belongs to the silicon photonics category [7]. It offers many of the functionalities of a photonic platform, except a very important one: an efficient light source. Si has an indirect bandgap, which prohibits the efficient emission of light. Several groups are working on a concept to overcome this limitation [8], with a recent breakthrough in achieving a direct bandgap structure by growing Si with a hexagonal lattice structure [9]. However, these structures are still far away from being usable, let alone that it can be integrated within the CMOS fabrication process flow.

Heterogeneous: CMOS and InP
The heterogeneous concept can combine the advantages of both platforms. The existing concepts can be sorted into four technology groups:

1. III-V integrated in silicon photonics platform
2. micro transfer printing (μTP)
3. hybrid integration
4. InP membrane on Si (IMOS)

For the first approach reference [7] classifies three different categories on how the integration of a III-V laser source into a silicon photonic platform can be achieved. These are: direct growth of III-V on Si, bonding of III-V material with subsequent device processing, or a combination of both by growing the III-V material on Si and subsequently bonding this with a patterned Si wafer. The growth of III-V material on Si suffers strongly from the lattice mismatch, resulting in dislocations. To reduce the induced defects in the grown material several techniques are explored, like the use of strain superlattices layers [10] or the introduction of quantum dot layers to filter dislocations [11]. Bonding of III-V material onto the silicon photonics wafer resulted in several successful realizations [12, 13]. Two different bonding techniques are explored: direct and adhesive bonding. In both cases the III-V elements provide the gain material required for a laser. Different integration concepts are used, with a wide application range for which the III-V material can be selected specifically. However, the scalability of this technology seems challenging.

The μTP approach relies on fully fabricated III-V components and uses a sacrificial layer to enable a transfer process from the original wafer substrate onto the Si wafer. This stamp process requires a high alignment accuracy of 1.5 μm and enables good scalability and throughput [14]. It also enables the use of several different materials to be transferred to the target wafer.

The term "hybrid integration" refers to the combination of two or more independently operating circuits realized within different technologies. Depending of the level of integration the concepts can be categorized in 2D, 2.5D or 3D approaches. In figure 1.2 (b),(c) and (d) an overview of these categories is presented. The 3D integration refers to stacking the two circuits on top of each other, using a flip-chip approach. The resulting electrical interconnects are short and enable high bandwidth operation [15]. In case of 2.5D integration an interposer carrier is used, through which both circuits are connected [16]. The interposer enables additional radio frequency (RF) lines, to optimise the signal transmission. The 2D integration is based on a side by side placement of the two circuits with wire bond connections in-between.

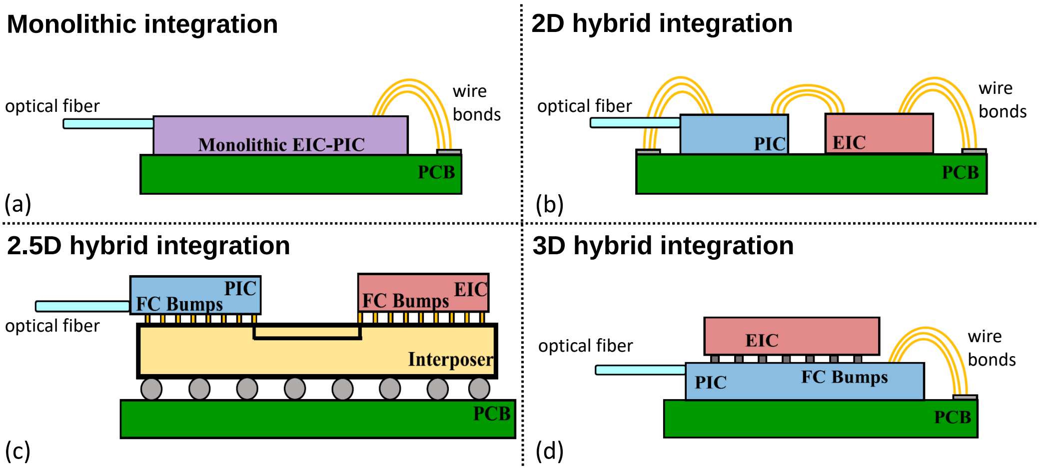

Figure 1.2: Schematic overview of the different integration concepts, [16]

Within the Eindhoven University of Technology (TU/e) another integration method is pursued, which can not be assigned into any of the introduced concepts. It is a wafer level integration, whereby an InP wafer is combined with a silicon wafer, using adhesive wafer bonding. This platform is called InP membrane on silicon (IMOS). The InP wafer assembles a full PIC environment relying on III-V waveguides [17, 18]. The technology uses the high refractive index contrast with the underlying adhesive polymer to form high density photonic circuits, enabling the full functionality of a InP platform. The silicon wafer is used only as a carrier so far, but has the perspective of being replaced with a CMOS wafer for a full photonic electronic integration.

1.2 Motivation

A new integration technology is proposed for integrating PICs with matching EICs. The main difference with IMOS is that the PIC and EIC are operating independently with classifies this approach to be hybrid. The used photonic platform relies on a generic process in contrast to the IMOS high refractive index platform. The fabrication is envisioned on wafer level to enable scalability. The technology is based on adhesive wafer bonding. Thereby a polymer is used in between the two wafers to mechanically combine them. The optical, thermal and electro-magnetic domains of the two wafers will be decoupled after the integration, because of the properties of the polymer used. The electrical connections between the two circuits are realised through the photonic membrane and through the polymer bonding layer. This concept enables high density of short interconnects. The research presented in this work is aiming to identify the opportunities and limitations of the proposed technology. Special attention will be paid towards the thermal, optical and electrical interfaces of the resulting devices.

The aim of this work is furthermore a successful demonstration of the proposed technology through realizing co-designed hybrid transmitter and receiver modules. Both the photonic and electronic circuit are created by using a mature foundry process. Adaptations will be needed to enable the integration of both platforms, which will be explained within this work.

The creation of a hybrid module requires matching photonic and electronic designs. However, there is no software available which is capable of directly creating this. Therefore a design flow will be presented to design matching wafer layouts.

To define the integration process it is important to understand the limitations of the materials and available technologies. A concept for wafer alignment is needed, which should be compatible with the intended bonding approach. Fabrication parameters like process temperature, chamber pressures and chemical selectivity have to be explored and adapted towards the integration technology.

The used PICs and EICs are highly valuable, which makes it important to monitor the functionality through the whole integration process. Therefore a new optical coupling interface will be used to monitor the passive structures on the photonic wafer. The performance of the bonded active photonic components will be compared to the foundry specifications.

At the end of the integration process modules have to be created from the wafer. Therefore a new singulation process will be introduced. The resulting modules can be used with standardized packaging solutions, which puts certain requirements on the optical and electrical interfaces.

The analysis of the resulting modules regarding the impact of the developed 3D integration technology is a central part of the research presented in this thesis.

1.3 Outline

Within this work a new integration technology, combining generic PICs with matching EICs is proposed, fabricated and characterized to evaluate its potential. The content of this thesis is structured as follows:

- **Chapter 1** lists an overview of existing integration concepts to combine photonic and electronic circuits. A short descriptions of the proposed 3D integration technology is given, highlighting the conceptual approach.
- **Chapter 2** elaborates on the proposed design and process. A roadmap is given, describing the integration path towards the realization of hybrid modules. The design flow is presented in detail, including analysis of the optical, electrical and thermal limitations of the hybrid assembly. A compact process flow description is given as guidance for the explicit report following in chapter 3.
- **Chapter 3** concentrates on the developed technology, starting with defining the necessary foundry requirements for a successful integration. Furthermore, this chapter contains a description of the first hybrid module realization, explaining the required adaptions with respect to the initially proposed process flow .
- **Chapter 4** reports the measurement results of the photonic components. The chapter is divided into sections on the passive and active components. The former will be characterized before and after the demonstration of the investigated integration technology, while the active components will mainly be characterized after the integration. Both will be compared with the foundry specification. The measurements results identify the impact of the technology. The corresponding test structures are introduced in this chapter. A wafer of the second generation is characterized before the integration process to compare and evaluate the wafer quality difference between the two fabrication runs.
- **Chapter 5** presents the performance achieved for the electrical interconnects and the hybrid photonic-electronic demonstrator. A transmitter and receiver module are created, and data transmission experiments are executed.
- **Chapter 6** summarizes the understanding gained of the investigated integration technology, and proposes future research questions and technology improvements.

Chapter 2

Integration Roadmap

The novel approach of integrating a state-of-the-art InP wafer with a matching electronic CMOS wafer, using adhesive wafer bonding, enters a technological domain which promises many new opportunities. However, it also creates uncertainty on how to best link these two worlds. In this chapter the challenges of the integration concept are introduced and the various technology decisions made are motivated.

Both technology platforms have been developed over many years, but the development of the electronic IC process (CMOS) started several decades before that of the photonic one. Therefore its foundry procedures are advanced and set to certain standards. This has the advantage that boundaries for simulation and design are well known, because of the availability of a robust and reproducible process. However, due to this the CMOS process is less flexible or adaptable towards the integration with PICs. Therefore it is the more flexible PIC process that needs to adapt towards the integration requirements. Thereby it is a key requirement that several photonic foundries are supported. Consequently adaptations should be generally applicable to these different PIC foundry platforms.

Here three platforms are considered: the Fraunhofer Institut for Tele-communication, Heinrich Hertz Institut (HHI) [19], Smart Photonics (SMP) [20] and IMOS [17, 18]. SMP and HHI are two generic foundries, enabling a fundamental set of photonic building blocks (BBs), such as gain or laser sections, modulators and detectors, to be integrated in their particular platforms. Next to those they provide several unique BBs, only supported by one specific foundry. Both platforms generate individual devices or PICs fabricated on an InP substrate. IMOS on the other hand is a membrane platform, based on a thin layer of InP which is applied with adhesive wafer bonding to a silicon wafer. The InP material there has a total thickness of a few 100 nanometres. The TU/e develops the IMOS process towards a mature platform, which is under constant improvement to enhance process stability and device performance. The experience with adhesive wafer bonding offers a promising approach towards integration with the electronic circuitry. This forms the basis for the wafer scale integration of photonics and electronics demonstrated in this work.

An IMOS structure consist of the silicon wafer as a carrier, the adhesive polymer and the InP membrane on top. To create the latter a sacrificial InP substrate is needed on which the layer stack is epitaxially grown. This layer stack is processed from the topside to prepare the BBs. Subsequently the InP wafer is bonded to a silicon wafer with the grown and pre-processed layer stack facing the silicon wafer. After removing wet-chemically the InP substrate, and an sacrificial etch stop layer, the InP membrane is obtained. Its backside is now exposed and can be further processed to finalize the actual photonic structures. The IMOS platform uses this possibility of double side processing, which offers a promising approach to connect the photonic layer with underlying structures, like electronic circuits, by using through polymer viass (TPVs).

The generic foundries, Smart Photonics and HHI, also process their PICs within a grown epitaxial layer stack on top of an InP substrate. The approach of bonding this layer on a new carrier wafer is possible. To enable this approach a few adaptations have to be made to enable the wet-chemical removal of the substrate and to guarantee the performance of all BBs. The membrane that will remain is up to 10 μm thick, which is 20 times the thickness of an IMOS-membrane.

In this chapter the integration concept is introduced by explaining the different design considerations. First the general design flow is explained followed by sections, concentrating on specific design aspects: electrical, thermal and optical. At the end of this chapter the integration concept is explained including a compact description of the intended realization. In the following the photonic wafer material refers to the HHI generic foundry, which provided all the InP wafer used in this work.

2.1 Design flow

Creating photonic and electronic integrated circuits (ICs), using mature foundry processes, starts with the design. The software used for designing these ICs is quite different as each material system focuses on technology specific simulations and design values. They are developed by different industries, which do not have a direct overlap in applications. Each foundry provides access to its designer through an intellectual property (IP) protected process design kit (PDK). At the moment, there is no combined PDK for the used photonics and electronic platforms. Thus, there is no software to simulate and design a complete hybrid device, which induces difficulties for efficient co-design. Fortunately the mask file format "graphic design system II (GDSII)" is used in both electronic and photonic industries. This offers the opportunity to align wafer layouts by matching them on the GDSII level.

The wafer dimensions used in the photonic and electronic fabrication do not match in size. Standard InP-wafers are available with a diameter of 50.8, 76.2 and 100 mm (2, 3 and 4 inch), while bipolar CMOS (BiCMOS)-wafers are normally 200 or 300 mm across. In this work a diameter of 76.2 mm for the photonic and 200 mm for electronic wafer are used, which are defined by the corresponding foundry. Within the NanoLab facilities at TU/e process tools are limited to 3 inch. Therefore 200 mm BiCMOS wafer has to be diced into several 3 inch wafers.

The electronic material comes from a mutli project wafer (MPW) run. Such a wafer has one fundamental cell, called a reticle, which is repeated over the wafer with a constant pitch. This reticle contains designs of various projects and from multiple designers, who share the available area. With this approach the manufacturer can fabricate on one wafer a number of submitted designs. To increase the amount of produced circuits for each design, several identical wafers can be fabricated. This is cheaper than the fabrication of a dedicated wafer run for each designer, as high costs are connected with the lithography mask sets. However, this means that the influence a designer has on the BiCMOS wafer layout is rather limited. Due to the number of participants, each designer obtains only a small design area within the BiCMOS reticle.

To demonstrate and test the wafer-scale integration technology a transmitter (TX) [21, 22] and receiver (RX) [23, 24] circuit are designed for the electronic MPW run , as well as an electronic interconnect test cell. These three different cells are designed by research partners[1]. The GDSII files of these circuits are created by the designer. The remaining content of the BiCMOS reticle is not known. To design a matching InP wafer it is important to know the position of the electronic cells on the 200 mm BiCMOS wafer. This floorplan is a GDSII file which is not shared. To define the design positions within the 200 mm wafer the reticle grid is defined first by using the fundamental cell size, the reticle placement pitch in 2 perpendicular directions and the absolute positioning on the 200 mm wafer. Adding the TX, RX, and test cell layout files, at the relative positions within the reticle, which are provided by the foundry, leads to the reconstructed 200 mm wafer GDSII layout. A picture of this is presented in figure 2.1. Based on this layout the dicing of the 3 inch BiCMOS wafer can be defined, and only after this is done the design of the InP wafer layout can start.

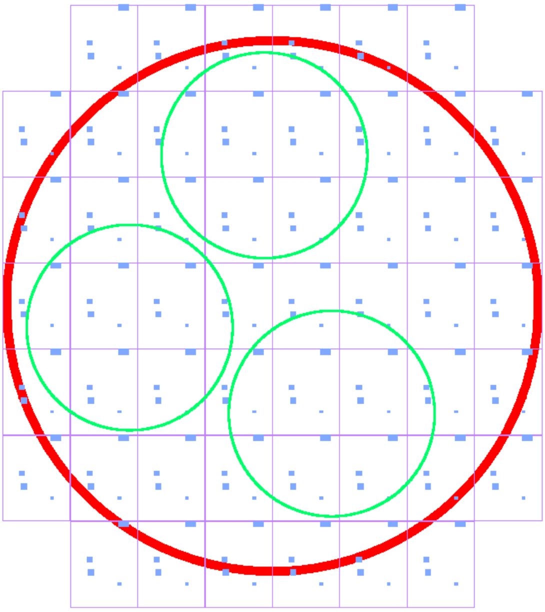

Figure 2.1: Reconstructed GDSII of the 200 mm BiCMOS wafer (red circle) including the 3 inch cut-out positions (green circle)

A disadvantage of this approach is that the final design of the photonic wafer has to wait for the availability of the electronic floorplan, which extends the total design time. To reduce this effect the design process is divided into several sub tasks. First the co-design of the photonic and electronic cells is addressed. The electronic cell designs are then submitted to the foundry. Thereby a few boundary conditions have to be taken into account. The orientation of the electronic designs should be fixed, since it is related to the orientation of the photonic design. This is because, for technological reasons, several photonic building blocks (BB) have to be orientated in the same direction over the InP wafer. Examples are the active BBs, like the distributed feedback (DFB) laser, the electro-absorption modulator (EAM) and the

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[1] Gertjan Coudyzer, University of Ghent; Xi Zhang, IC group TU/e, now with NXP Semiconductor

PIN-photodiode (PD). These all have to be orientated perpendicular to the major wafer flat. Furthermore, the minimal distance between the cells is defined by the size mismatch of the photonic and electronic cell design. This is because the photonic design is larger, due to the presence of spot size converters (SSCs). Therefore it is important that the designed electronic cells are placed with sufficient distance to compensate for this footprint mismatch. Both of these boundary conditions are taken into account by the electronic foundry.
With the reconstructed 200 mm floorplan the 3 inch cut outs are planned carefully, according to the following conditions:

1. all obtained 3 inch wafers should be identical
2. the number of our design cells included is maximized
3. an equal amount of the different designs is preferred
4. the designs are aligned towards further processing

The first condition is used to ensure that only one photonic wafer has to be designed, and therefore reduces the required design time. For each wafer a matching photonic wafer has to be created, which requires a set of optical masks. By using identical wafers only one mask set is needed, resulting in a reduction of costs. Based on this first condition the total number of 3 inch wafers is limited to three. The second and third point aim at a maximum yield for the three different designs. The last condition refers to process related limitations. The equipment that is used requires alignment markers within certain position windows. These markers are part of the designed cells itself and have to align towards the requirements of the processing tool. A more detailed explanation will be given in section 3.3. The cutting of the wafers is done with laser dicing. Subsequent grinding of the wafer edges is applied to remove the debris resulting from the laser cut[1].

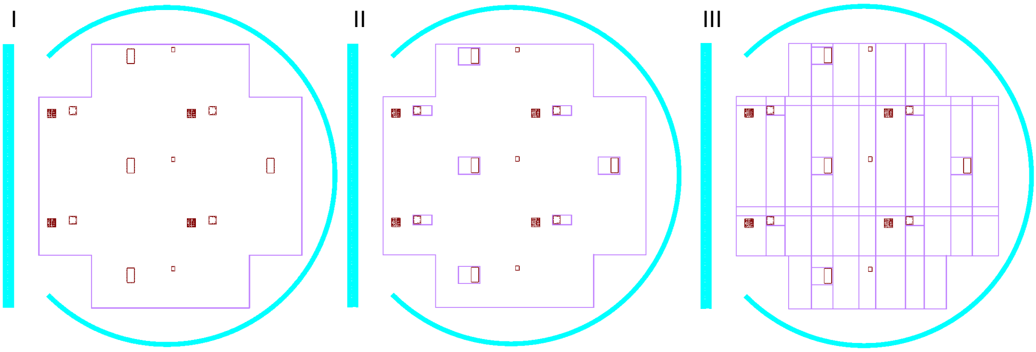

Figure 2.2: Cell definition process starting with (I) the 3 inch wafer surface including the actual design area (cross) and the electronic ICs, (II) defining the final hybrid module dimensions, (III) dividing the remaining area in groups of cells

Regarding the InP wafer the next task is to define the design area and the cell division. For this special dicing lanes are defined, their functionality will be explained in section 2.4. In figure 2.2 the different steps for placing these lanes are presented. In the left figure the outside of

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[1] This task was outsourced to Philips Innovation Lab

the 3 inch InP wafer is drawn in blue. It is aligned towards the 3 inch cut out from the 200 mm BiCMOS wafer, which defines the position of the included electronic cells (brown). The outline of the effectively usable InP design area, which has the shape of a cross, is also shown. This cross is predefined by the HHI foundry. It is 60 mm wide and equally high. The outline of the cross is part of the dicing lane definition. The centre figure shows the design, including the frames of the photonic cells of the transmitter and receiver designs. These boxes are predefined by the co-designed cell definitions. Based on these initial lines, the rest of the wafer is divided. The final result of this design process is shown in figure 2.2 (III).

The wafer is divided in cells of various sizes. The amount of different cells has been minimised as much as possible, thereby enabling repetition of each type. This concept has the advantage that each design is created several times at different positions on the wafer. Therefore the influence of local defects on the wafer is minimised. The approach of dividing the InP design area into groups of various cells sizes is chosen to gain the maximum design area. It also enables a minimum size of the final hybrid modules.

To make the best use of the remaining surface of the InP-wafer, the rest of the design space is filled with photonic test cells, alignment markers and additional functionalities. The test cells are used to characterize the different photonic BBs, which will be further explained in chapter 4. After finishing this design it is submitted to HHI for processing. Finally the post processing masks need to be designed, which are used for processing after receiving the foundry wafers. The post processing will be described in chapter 3.

2.2 Electronic design considerations

Usually photonic and electronic modules are designed independently and rely on a standardized impedance to transfer high frequency signals across interfaces. The standard value is based on a patent from 1929 from Lloyd Espenschied and Hermann Affel describing the coaxial cable [25]. The value is chosen to be 50 Ohm, which is a trade-off between the maximum power handling capability within the coaxial cable (at 30 Ohm) and the minimum attenuation (at 77.5 Ohm) [26]. This traditional value however doesn't ensure the best impedance for photonic-electronic co-design. Several publications present InP structures that rely on termination resistance [27, 28] to diminish RF reflections and optimize performance, but this leads effectively to an increase of the total energy consumption.

Co-design interface optimization is a key opportunity to create more power efficient devices. Within this work two InP building blocks rely on electrical high frequency input or output signals: the EAM within the TX design and the high speed PIN- PD, which is the heart of the RX design. To minimize the power consumption the interface impedance between the electronic ICs and these photonic BBs is optimized. The BBs are electrically represented by equivalent circuit models, which are provided by the InP foundry. Applying impedance matching to these models reduces reflections without using termination resistances on the InP membrane. This consequently translates into an improved power consumption of the hybrid modules. This concept assumes that the influence of the electrical interconnects itself is either negligible, or can be included in the model. Which of these two options is valid depends on the design choice made on how to integrate the two circuits.

In general two possible concepts are applicable. The first one relies on placing the matching photonic and electronic circuits directly on top of each other, enabling perpendicular TPVs. This results in very short interconnects. Their length is mostly defined by the polymer layer thickness itself. The second approach uses a metal routing layer between the two circuits, if they are placed with an lateral offset with respect to each other. The routing could for example be realized within an intermediate polymer layer. The flexibility that this gives for connecting designs which are not pre-aligned on the two wafers can speed up the design and fabrication process, as each wafer can be designed and processed independently. The disadvantage is however that the interconnects can become extremely long. This might be compensated with high frequency transmission lines within the routing layer, to avoid bandwidth degradation and prevent reflections. Nevertheless, the fabrication seems challenging. This approach seems to be too complex and should be avoided. The new 3D integration technology that is presented here is aiming at techniques that lead to a manageable fabrication process. Therefore the first approach (short interconnects between aligned designs) is chosen for further investigation.

Placing the corresponding high frequency metal pads on the two wafers relatively close to each other creates short interconnects. The realization developed in this work relies on a small lateral shift of the pads, in the order of the polymer layer thickness. The interconnect length is then approximately $\sqrt{2}$ times the polymer layer thickness. This offset is needed in the processing and will be further explained in chapter 3. However, the interconnect is still very short, despite the offset. Its performance is simulated and the results are presented in [21]. To verify the performance of the interconnect a test cell is included[1], the results of which are presented in section 5.1. The simulated properties of the interconnects and the equivalent circuits of the InP BBs are used to optimize the BiCMOS ICs.

To enable a compact hybrid module assembly within a standard electronic package requires electrical control interfaces via the BiCMOS side. The InP circuit is therefore completely controlled through the electronic IC. All external interfaces are placed on the edges of the BiCMOS chips. A main advantage of this approach is the possible usage of several independent metal layers, which enables efficient signal routing and line crossings. Additionally it offers RF transition lines, which can be fabricated with a high precision. Within this work two full design cycles have been completed, each including a transmitter and receiver circuit. The second generation constitutes a progression with respect to the first one. In figure 2.3 a schematic top view of the 2nd TX generation design is show. In (a) the InP membrane (blue) is covering most of the hybrid module area, thus representing the final appearance; (b) shows the actual design embedded in the photonic layer. The metal contact pads are represented in orange for the

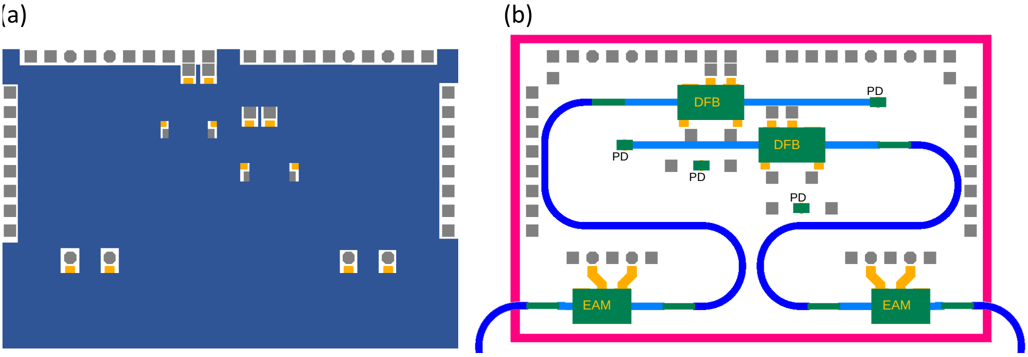

Figure 2.3: Top view of the TX design from the second generation; (a) with the InP membrane in blue, sealing most of the area, (b) with a transparent photonic membrane to identify the different BB

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[1] Design by Xi Zhang (BiCMOS) and Arezou Meighan (InP)

photonic layer and in silver for the electronic one. The pads along the three edges (left, top, right) of the chip are intended to be used as external probing interface. The pads within the design area are used for connecting the electronic and photonic wafer. The shown schematic represents a dual channel design, which is based on two nearly identical designs. Only three sides of the electronics are used for external electrical interfacing as the remaining side is reserved for optical fibre coupling. The electrical pads placed at the top are used for high frequency and direct current (DC) signals, while the other pads are used for DC only. These general design principles are the same for the TX and RX designs of both generations.

2.3 Thermal design considerations

In active photonic components heat is generated due to mechanisms like joule heating, non-radiative recombination, reabsorption of radiation and mirror absorption [29]. Depending on the amount of heat generated and its flow, the device temperature increases. This can lead to performance penalties, device degradation or even complete destruction. To avoid this, it is important to optimize the heat flow by adding passive or active cooling elements and/or by limiting the heat generation. For example in a gain section this could be achieved by reducing the pump current. The InP and BiCMOS wafer both include active components that dissipate heat. These wafers are separated by the intermediate bonding polymer, which has a relatively low thermal conductivity. Commercially available software is used to simulate the heat flow within a simplified 2D cross section.

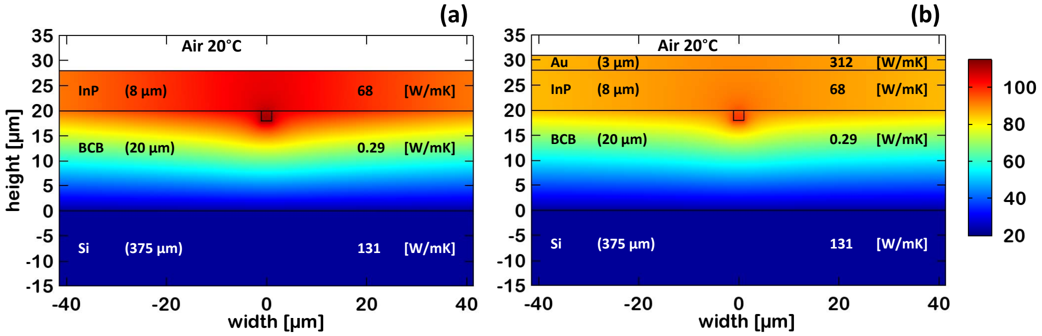

Figure 2.4: Colour coded temperature map resulting of the two dimensional thermal simulation of the envisioned structure without (a) and with (b) gold heat spreader, including the thermal conductivity values for the different materials and the thickness used

In figure 2.4 (a) a fraction of the simulation environment is presented. The interfaces of the different materials are displayed with black lines. The colour code represents the temperature at stationary condition. In this simulation the electronic wafer is at the bottom and thermally represented with a 375 μm thick silicon layer. On top of it is a 20 μm thick bonding polymer layer followed by an InP layer of 8 μm, representing the photonic membrane. The simulation area is 500 μm wide and is restricted to the sides with an isolating boundary condition. The bottom of the Si wafer is attached to an ideal heat sink with a fixed temperature of 20 °C. The topside of the InP wafer is surrounded by air with a temperature of 20 °C resulting in convective heat flux (5 W/m^2K).

In the centre of figure 2.4 (a) a 2-by-2 μm wide InP waveguide is placed, connected with the membrane on top and surrounded by the polymer layer. This waveguide is used to represent a laser structure, which is the only heat source for this simulation. The dissipated heat for the laser is calculated from the electrical input power of 175 mW (50 mA, 3.5 V) reduced by the emitted optical power of 5 mW, resulting in 170 mW. This value has to be divided by the total laser length of 420 μm to determine the heat dissipated per unit length, which is used in 2D. The thermal conductivity values which have been used are given in figure 2.4. For InP and Si the numbers are taken form the software data base. The polymer used is benzocyclobutene (BCB), for which thermal conductivity is given by the supplier [30]. It can be seen that the value for BCB is more than 200 times smaller than for InP. The dimensions used are representative for the envisioned structure. In figure 2.4 (a) it can be seen that the temperature in the laser structure rises to a maximum value of 112 °C. Because of the thick polymer layer the heat flux through the silicon wafer is reduced dramatically and the heat flux at the surface is limited. A possibility to improve the heat sinking is an increase of the lateral heat spreading, and therefore to enlarge the surface used for this convective heat flux.

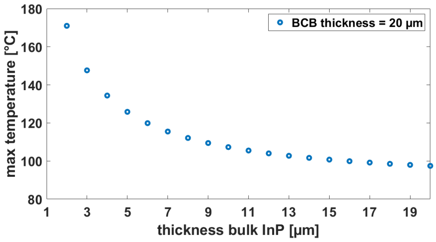

Figure 2.5: Simulated maximum temperature within the InP membrane for different InP layer thickness

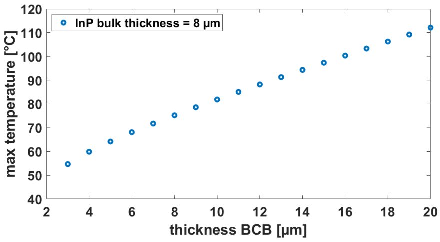

Figure 2.6: Simulated maximum temperature within the InP membrane for different BCB layer thickness

Because of the substrate removal the InP material is thinned down and lateral heat spreading within the membrane is limited. This can be seen by simulating the maximum temperature in the InP laser structure as a function of the InP membrane thickness. The resulting graph is presented in figure 2.5. The thicker the membrane is, the lower the temperature. However, for large layer thickness this effect is limited by the thermal conductivity of the material itself. As the membrane thickness is predefined by the foundry an alternative method is proposed to increase the lateral heat spreading. It relies on metal structures, which are created on the backside of the InP membrane. This can be fabricated as part of the electrical interconnection step (described in section 3.6). The resulting metal structures are 2– 4 μm thick. A comparison of a structure with and without metal heat spreader is presented in figure 2.4 (a) and (b) respectively. The maximum temperature is reduced by 13 °C with a 3 μm thick and 250 μm wide gold structure. Beside this property of spreading the heat the metal can also be used as an interface for a passive or active cooling element to reduce the temperature even further.

The intermediate polymer can thermally isolate the photonic from the electronic wafer, depending on its thickness. In figure 2.6 the maximum temperature within the simulated InP laser is plotted as a function of the BCB thickness. Because of the poor heat flux towards air the temperature is increasing nearly linearly with polymer thickness. For the envisioned process an intermediate BCB layer of 20 μm is anticipated, which is needed to enable the adhesive wafer bonding (see section 3.3).

The actual structure will have heat sources both in the PIC and the EIC. The intermediate bonding polymer reduces the thermal crosstalk between these two circuits. However, isolating the two sides means that each one has to have a sufficient heat sinking on its own, to reduce temperature increase. While the electronic ICs will work up to a temperature of 150 °C, the photonic circuits requires stable values to operate at the target wavelength.

The refractive index of InP is temperature depended [31], which influences all BBs, especially the arrayed waveguide gratings (AWGs). Another example is the temperature dependency of the DFB emission wavelength, which changes roughly with 1 nm per 10 °C [32].

Heat generation in the photonic membrane can also be used to control these BBs. A heating element is included into the DFB BB to manipulate the temperature, and therefore shift the wavelength. The aspect of using heat for controlling BBs has not been further investigated here.

To determine the actual temperature in the photonic membrane the dark current of a photodiode can be used. The temperature dependency [33] has to be characterized beforehand by heating the sample and measuring at steady state condition the resulting dark current. Also the wavelength shift of the DFB laser can be used to determine the temperature.

It is important to extract sufficient heat from the membrane to enable operating devices. For the hybrid module double side cooling is envisioned. That means both the electronic and photonic circuits will be cooled separately by adding passive or active cooling elements. The actual development of the thermal packaging was beyond the scope of this work. The alternative would be to cool both circuits simultaneously from the BiCMOS-side, which would require a heat flow through the bonding polymer. This could be achieved by designing the placement of thermal vias.

2.4 Optical design consideration

Emitting and receiving optical signals with the hybrid modules requires optical interfaces to couple light into (and from) a single mode fiber (SMF). The requirements for such an interface are: low coupling loss, polarization independence, robust and stable fixture, tolerant alignment, no reflection and minimal influence on the transmitted signal itself. Optical interfaces can be divided in two groups, based on the coupling scheme: edge and surface coupling. Both have their advantages and disadvantages and will be used within this work. For the monitoring of the process surface coupler are used to enable wafer level measurements. Edge coupling is the selected option for the hydride modules as it is intended to package them into standard housing solutions.

Edge coupling requires smooth facets, which are normally created when cleaving the InP wafer along its crystal planes into bars and subsequently into single chips. This approach is not applicable for the combined layer stack of InP and BiCMOS.

The here proposed solution consist of two steps: first the InP facets are created when etching the dicing lines into the InP-wafer, before bonding. These will be filled with the adhesive polymer. After bonding, followed by substrate and etch stop layer removal, the lines are accessible. The second step is sawing along these lines to separate the modules. Thereby most of the polymer is removed, while a few micrometre thick layer is left in front of the InP facets. The polymer facet resulting after sawing is not smooth and includes some debris. This will induce some scattering . Based on the relatively small refractive index difference between polymer and air this scattering effect will be reduced, as compared to a similar rough InP air interface. Nevertheless, it would be best to remove the polymer completely, leaving the undamaged smooth InP facet for optical coupling.

The coupling efficiency between the photonic chip and the glass fibre depends on the optical mode matching and their alignment. Using identical modes shapes and sizes the coupling will be defined solely by the alignment. The coupling efficiency is calculated with the mode overlap integral. If they are perfectly aligned and no reflections are present its value is 1. If the two modes vary in size or shape the value is smaller, which translates to coupling loss. For optical transmission SMFs are used which have an outer diameter of 125 μm. These have a round core with a diameter of 9 μm, surrounded by a cladding material with a slightly lower refractive index. The mode guided within this fibre is circularly shaped and has a mode field diameter of round 10 μm. On chip level the used modes are not circular, and have mode field diameters of 1 to 2 μm. Coupling a SMF directly to a standard InP waveguide mode therefore induces large coupling loss, mainly due to the mode size mismatch. There are special fibres using an ultra high numerical apperature (UHNA), which have a reduce mode field diameter, down to 4 μm, which is however still too large for efficient coupling. Therefore it is necessary to increase the mode diameter on chip. The BB that achieves this is called a sport size converter (SSC). These are foundry specific BBs which expand the mode diameter to match SMF or UHNA fibres as closely as possible. The increased mode size on the chip has the additional advantage that the polymer facet roughness has a reduced influence.

A disadvantage of edge coupling, however, is the fact that it is not possible to use it before separating the wafer into single chips. Therefore one can not monitor the behaviour of photonic devices during the process. It is important to guarantee the operation of the two foundry wafers before starting the bonding process, and to monitor changes during it. For the electronic circuits this can be realized with electrical probing and measuring the characteristic properties. The photonic wafer on the other hand needs additionally optical probing to verify its performance. Coupling light into the devices on wafer level can be achieved by using surface couplers. HHI developed a special BB, the vertical mirror, applicable for this purpose. It is a facet etched into the membrane under an angle close to 45 ° with the surface of the membrane. This facet acts like a mirror, due to total internal reflection, directing the light perpendicular out of the wafer surface (or conversely, allow light to couple in). This enables monitoring of the photonic circuits before and after bonding. More details about that BB are given in section 4.1.1.

2.5 Integration Concept

The research presented in this work is intended to create a new hybrid platform, which enables short electrical interconnects between the photonic and electronic domain to increase the bandwidth and reduce the power consumption of the resulting modules. Additionally the target here is to develop a technology based on robust wafer scale fabrication processes, using state-of-the-art materials and devices.

The technology is intended to be adapted towards different photonic and electronic foundries. It can be divided in six steps: design, wafer bonding, substrate removal, opening electrical interfaces, creating interconnects and a back-end process. The design flow is presented in section 2.1.

Wafer bonding:
The physical integration starts after obtaining the two co-designed wafers from the foundries. Bonding two wafers to each other is a well-known concept and several different techniques have already been developed. In [34] the existing bonding techniques are summarized as: direct bonding, anodic bonding, solder bonding, eutectic bonding, thermo-compression bonding, direct metal-to-metal bonding, ultrasonic bonding, low-temperature melting glass bonding and adhesive bonding. This list shows the variety of approaches. A few boundary conditions have to be considered when choosing a suitable concept for our case.
The two materials that are bonded, InP and BiCMOS, have to form a stable bond to enable post processing. After bonding several steps are needed to create a functioning module. The bond has to sustain these without severely limiting the process. Additionally, each of the two wafers should operate without influencing the other, therefore optical, electromagnetic and thermal decoupling of both materials is necessary. The bonding technique needs to support patterned surfaces, as both wafers incorporate several microns of topology. All these requirements are fulfilled best by adhesive bonding, when using an appropriate intermediate material.
The IMOS technology uses such an adhesive wafer bonding. It relies on the fact that both wafer surfaces have a negligible topology. Replacing the silicon wafer with a BiCMOS wafer already changes this. Using generic InP material instead of IMOS increases the topology even more dramatically. Mimicking the initial assumption of bonding flat surfaces, the adhesive polymer is used to planarize the wafers before bonding them. In figure 2.7 a schematic is presented showing the 3D integration approach. The starting point in the figure 2.7 (a) shows the InP wafer (bottom) and BiCMOS wafer (top), both facing upwards. The topology derives from the BBs fabricated within the epitaxial layers. The second figure (b) shows the electronic wafer flipped and aligned with respect to the electronic wafer, where both surfaces are planarized with polymer to cover the existing topology. After bonding the two wafers (figure 2.7 (c)) the polymer provides mechanical stability for the assembly throughout the subsequent processing. It also provides isolation between the two wafers.

Substrate removal:
To enable electrical interconnects between the photonic and electronic circuits it is needed to etch through one of the wafers. The InP wafer is chosen for this. This is because etching through the BiCMOS wafer is highly impracticable, due to the many metal layers present there. Preparing for further processing requires thinning of the InP material. By removing the substrate the photonic wafer is reduced to its epitaxial layer stack. While the substrate is not required for the functionality of the photonic circuits, it does provide mechanical stability. During the bonding process both wafers are heated, glued and cooled down again. As the coefficients of linear thermal expansion (CTEs) for InP and Si are different, the mechanical fixation at high temperatures, by cross-linking of the polymer, is followed by an unequal material shrinking, which creates strain. This can be determined by measuring the bow of the combined wafer stack after bonding. This warping however is reduced due to the substrate removal. As the InP material becomes thinner, it becomes more flexible and can adjust better to the BiCMOS-wafer, which is a positive effect of the substrate removal.

Opening electrical interfaces:
The bonded assembly is constructed further by opening the InP membrane locally to access the underlying electrical pads. In figure 2.7 (d) the schematic cross section is presented. It is flipped so that the photonic membrane is on top and facing down. The schematic shows the

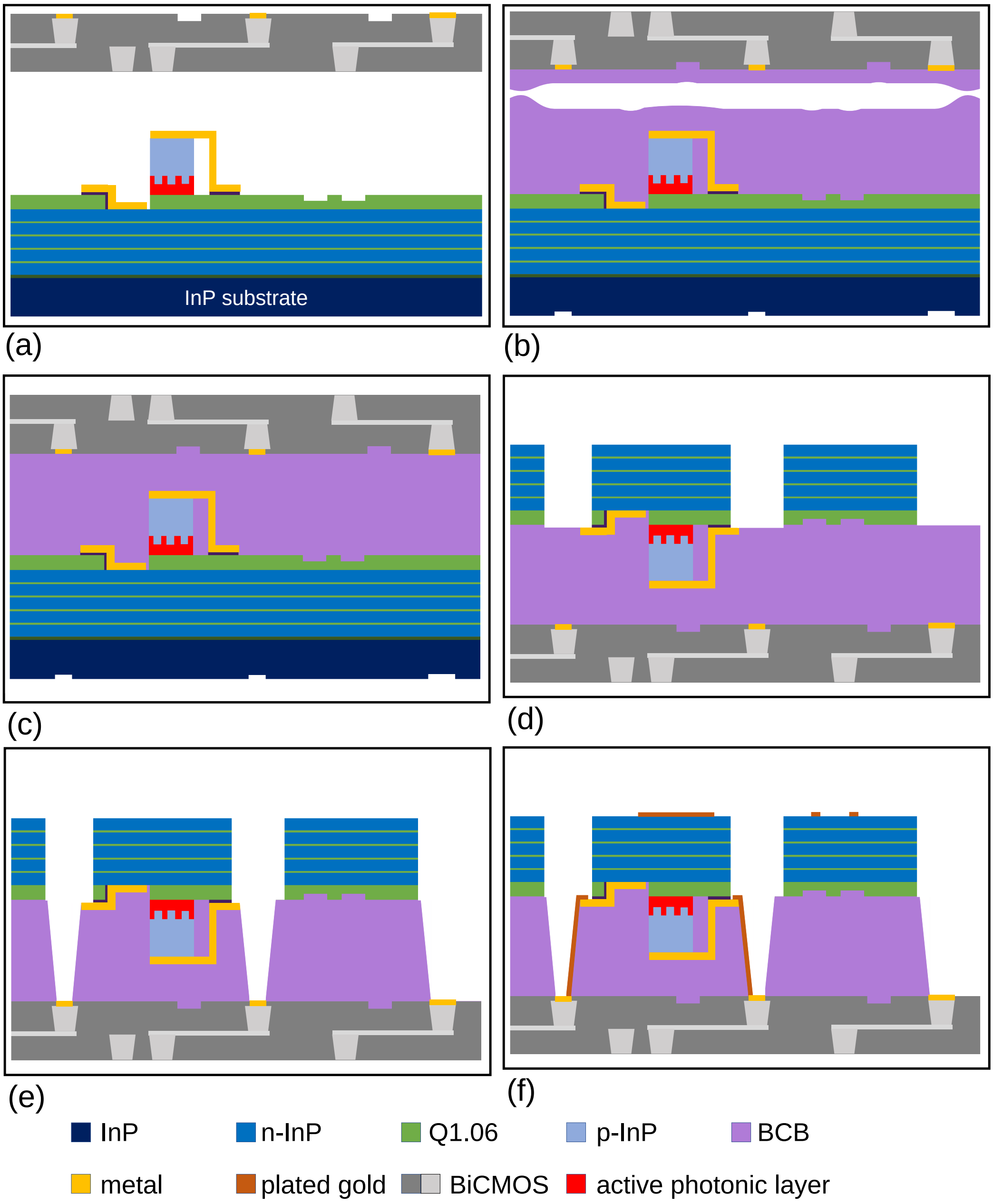

Figure 2.7: Schematic of the process flow; (a) starting point, InP wafer at the bottom, BiCMOS wafer at the top, both facing upwards; (b) pre-bonding, both wafers aligned and facing each other, topology is planarized with adhesive polymer; (c) bonded wafer stack; (d) flipped assembly, InP substrate removed, photonic membrane opened; (e) opening of the polymer layer; (f) realization of the electrical interconnects with electroplating

assembly after substrate removal and subsequent opening of the InP windows. The InP metal contact pads are accessible immediately after etching through the InP layer stack, while the BiCMOS metal pads are opened subsequently, by etching through the polymer resulting in the cross-section presented in figure 2.7 (e).

Creating interconnects:
In the last step the interconnects are created with electroplating. All electrical contacting of the final module will be realized through the BiCMOS. The benefit of this is that all contacting pads, including those for the active photonic devices, can be placed at the edge of the chips. The routing through BiCMOS is very efficient, as several metal layers are available for this purpose, which for example enables electrical line crossings. Additionally, the process is highly reproducible; each signal line and its interaction can be simulated with standard design software, resulting in accurate RF lines wherever they are needed. Finally, use can be made of well-developed contacting techniques to connect the modules electrically to the outside world. The electronic and photonic layers are connected with electro-plated gold interconnects. A schematic is presented in figure 2.7 (f). This also shows additional metal depositions on the backside of the InP membrane. These are intended as heat spreaders and heat transfer contact to be used for cooling the photonic membrane. At this point the wafer process is complete and a separation into modules has to be achieved.

Back-end process:
InP wafers are normally cleaved along crystal planes of the wafer. The BiCMOS wafer is normally sawed along dicing lanes, since cleaving of Si is not a reliable process. The process of sawing however constitutes a high risk of damaging the InP membrane. Especially the roughness due to sawing on the InP facets would be unacceptable for coupling light.
In section 2.4 the two-step approach has been introduced. First pre-dicing lanes in the InP wafer are defined by etching deep trenches into the membrane before bonding. These dicing lanes are 50 μm wide and separate the different InP cell designs. This etching process is performed by HHI and provides good quality facets to the InP waveguides. After bonding and removing the substrate these lanes become visible. They are sealed with polymer used during the wafer bonding process. The stacked wafer can then be separated by sawing the BiCMOS wafer along the predefined dicing lanes, through the BCB. The sawing blade has a width of 30 μm, so with careful positioning it leaves some of polymer on each InP facet. Ideally this layer would be removed afterwards, however that has not been realized within this work.

2.6 Conclusion

In this chapter the 3D-integration concept has been presented, giving an general overview of the different challenges engaged in this work. A method to co-design the PICs and EICs is reported using the GDSII files. The used design flow on how to create matching wafers is given, followed by an introduction for the electrical, thermal and optical design considerations. The process flow, including wafer bonding, substrate removal, opening electrical interfaces, creating interconnects and a back-end process, has been introduced. In the following chapter the creation of the hybrid modules is given thereby describing the created technology platform.

Chapter 3

Technology

The III-V cleanroom from Nanolab@TU/e is well equipped and offers all necessary tools to process photonic devices. Years of research have resulted in reliable processes and tool expertise for InP PIC fabrication. The possibility of integrating photonics and electronics is proposed for the IMOS platform. A short description is given in chapter 2. An integration of InP photonics with CMOS based electronics has however not yet been demonstrated. Up to now IMOS has used bare silicon wafers as carriers instead of CMOS, having comparable mechanical and thermal properties.

In this chapter a new integration technology is presented to integrate generic InP single project wafers provided by HHI with BiCMOS MPWs provide by NXP. Each wafer itself is highly valuable and the fact that both the electronic and photonic wafer are co-designed increases this value even more. Therefore it is decided to rely on known processes as much as possible, to reduce the risk. Fabrication approaches from the IMOS platform are the starting point for the development of the integration technology, but are adapted towards new requirements. It is important to create a reliable integration technology with an optimized risk management.

In the following the process flow is presented, highlighting technology based decisions.

3.1 Foundry Requirements

The materials used for the realization of integrated photonics and electronics are provided by HHI and NXP Semiconductor, respectively. As mentioned in section 2.5 our goal is to create a process that can make use of different foundry providers. To enable such an integration process a few changes have to be introduced to the foundry supplied wafers.

The electronics is based on a 200 mm silicon wafer and is created in a 0.25 μm SiGe:C BiCMOS process. The wafer is thinned down to a total thickness of 375 μm. This is more than the regular 200 μm in order to keep a safe minimum thickness for handling. The BiCMOS wafer doesn't need any further adaptations.

The photonic material is fabricated on a 3 inch InP wafer. Integrating both wafers is done by using adhesive wafer bonding. For the hybrid module only the processed epitaxial layer stack of the InP wafer is required. This membrane can be obtained after the bonding of the two wafers by removing subsequently the InP substrate and a sacrificial etch stop layer. This etch stop layer has to be added by the foundry below its standard layer stack. Additionally a few of the InP BBs might need to be adapted, because the resulting structures will have no InP substrate any more, which may change optical, electrical and/or thermal properties of the devices. One of the affected BBs is the SSC. It is used to couple light efficiently from the edges of the photonic membrane into a SMF, and vice versa. For this a diluted waveguide is used, which is placed below the rest of the InP layer stack. The SSC BB is designed to enable adiabatic coupling between the standard and the diluted waveguide. The latter has an effective refractive index close to that of the InP substrate. Therefore the optical mode can partly expand into this substrate. Without it, the diluted waveguide has an air cladding. In that case the refractive index contrast is increased substantially and the optical mode is more confined within the diluted waveguide, which results in an overall smaller mode size. This leads to higher optical coupling losses between chip and SMF. It has been verified that the BB will function also without the substrate[1]. Nevertheless, the mode diameter will be smaller than with the substrate. Alternatively, it is possible to replace this BB with one based on a different approach. A concept, that has been thought of, uses the bonding layer to create an optical waveguide structure, with a mode field diameter matching a standard SMF. For the remaining BBs no adaptations are implemented. The standard HHI PDK is used, complemented by EAMs based on aluminium containing quaternary material.

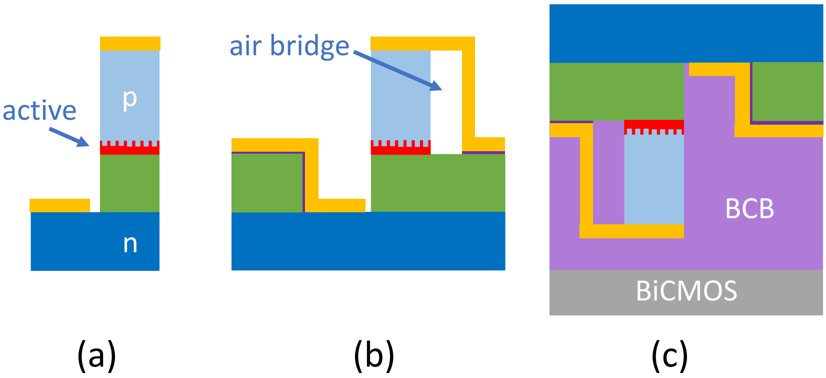

Figure 3.1: Schematic cross section of a DFB laser (a), with extended metal routing (b) and after flipping and bonding (c)

To integrate the photonic membrane with the electronic wafer, post processing is needed. This requires marker structures, which are used after bonding to align the post processing masks. It is decided to etch marker structures through the entire functional InP layer stack and into the etch stop layer. In that way the markers will become visible after removing the substrate and the etch stop layer. The same etching step is also used to create dicing lanes. These fulfil two basic functions. First, they provide separation of the InP cells, as needed in the final creation of hybrid modules from the bonded wafer. Second, the resulting facets form the optical coupling interfaces. It is important that this etch goes all the way through the InP membrane and stops inside the etch stop layer. If the etch is too shallow the marker structures and dicing lanes will not be opened. On the other hand, if the etch is through the etch stop layer the wet chemical etchant for substrate removal will damage the InP membrane. HHI creates these structures by

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[1] This analysis has been done by HHI, contact Francisco Soares

using a dry etch step. While the etch rate is well controlled, the total layer stack thickness varies with foundry specific tolerances up to several percent. To compensate for this, it is important that the etch stop layer is thick enough. Thus the foundry has more tolerance on the etch depth, while guaranteeing not to etch into the substrate.

Part of the post processing is the creation of the electrical interconnects. This will be explained in section 3.6. To support this the foundry creates a single accessible contact layer. In figure 3.1 (a) a schematic of a DFB laser is presented. The semiconductor contacts of the laser are connected with metal tracks for current feeding. These are further routed to one common horizontal layer (b). This enables accessing the contacts after bonding (c) with a single etching step. As the routing creates some distance towards the actual devices, this reduces the risk of damaging them during the contact opening step. In Figure 3.1 (b) it is also visible that HHI uses an air-bridge in the metal routing. HHI normally fills the space below the air-bridge with polymer in one of the last fabrication steps. This step is skipped for our purpose, as it might create enclosed air bubbles, which would be detrimental for the hybrid integration process.

As this overview shows only a few limited, but necessary, adaptations have been made to the foundry platform and process. The fundamental structure of the PDK is not changed and no foundry specific knowledge is needed to fulfil the requirements for co-integration with an electronic wafer. Therefore every photonic foundry could in principle provide suitable material, which is one of the requirements itself.

3.2 Wafer Preparation

The integration process starts, after receiving the wafers, by preparing them for the actual fabrication. The necessary steps to prepare the two wafers are presented in this section, starting with the electronic wafer.

The 200 mm large BiCMOS wafer has to be cut into 3 inch wafers. This is performed with laser dicing, a process that releases a lot of heat at the cutting edge. The heat creates warping, leaving debris on the wafer edge, thus adding extra topology. To remove this unwanted material a grinding step is added. This reduces the wafer size, therefore it is important that the wafer is cut somewhat larger than the target size. Additionally, the removal of material leaves particles on the surface, which could affect the further process. To avoid this the 200 mm wafer is initially protected with a resist layer of sufficient thickness, which seals the actual surface and will be removed after the grinding step. The laser dicing and grinding is done by an external company.

The first step after receiving the photonic wafer is characterizing a few fundamental BBs, to ensure their functionality. The measurement results are presented in chapter 4. During the characterization dusk particles can fall on the surface, which have to be removed before clean room processes. The clean room process of the InP wafer starts with preparation for the wafer-to-wafer alignment. In [34] an overview of the different concepts is presented. For the creation of the hybrid module the infrared (IR) shine through technique has been initially investigated as a possible candidate, but due to the fact that the BiCMOS wafer turned out to be non-transparent for the used wavelength range this method has been discarded. Further information about the shine through technique can be found in Appendix A. For an alternative technique the university invested in a new wafer alignment tool and a corresponding bonder. This enables the so-called backside alignment (BSA) technique. Thereby the two wafers are placed with respect to each other by aligning the topside of one wafer to corresponding markers structures on the backside of the other. In the following the fabrication of these

backside marker features will be described, before explaining the wafer-to-wafer alignment.
The fabrication of the backside markers is based on optical contact lithography. The mask used has to be designed together with the photonic and electronic circuits. The optical contact lithography is performed using the same BSA system which will be used for the wafer-to-wafer alignment.

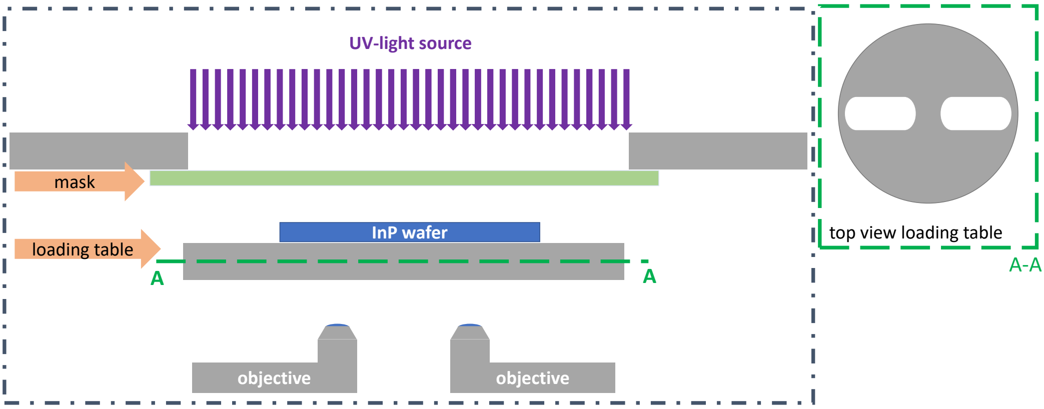

Figure 3.2: Schematic of the backside alignment lithography: marker mask (light green) to InP (blue)

Figure 3.2 shows the schematic tool setup. At the top is the light source used for the ultra violet (UV) exposure. The grey parts represent the tool frame elements. The two frame elements closest to the UV light source are used for fixing the mask (light green) with vacuum. The central piece is the loading table. It can move in and out of the tool, and up and down while loaded. At the bottom two objective arms are located, which are used for the actual optical alignment. To allow the marker structures to be defined on the backside, the InP wafer is placed top side down onto the loading table. To prevent damage to this surface, including all the sensitive photonic structures, it has to be protected during the whole backside marker process. For this purpose a thick layer of photoresist is spin coated on the InP topside. With the original topside protected the backside process starts with an oxygen plasma to clean the surface. Afterwards inductively coupled plasma chemical vapour deposition (ICP-CVD) is used to create a silicon dioxide (SiO_2) layer on the backside. Subsequently photoresist is spun onto the wafer. The next step is the pattern transfer to the photoresist.
In the lithography tool the mask is loaded first and fixed with vacuum. With the two objectives an image of the markers is taken, after which the objectives are locked at their positions. These objectives have a limited field of view, which is defined by two windows in the loading table. In the top right hand corner of figure 3.2 a cut through the A-A plane is shown to visualize these window areas. It is important that the alignment marker positions are designed to fit into these areas. The InP wafer is loaded next, as mentioned with its topside facing downwards. The alignment is done using the markers from the InP wafer top side, which are visible via the objectives, and positioning them towards the previously stored mask image. Then the wafer is brought into contact with the mask and the resist is exposed using the UV light source. The pattern transfer is finalized by developing the resist. The developer used is not affecting the protective photoresist layer on the topside of the InP wafer. Next the pattern is transferred into the SiO_2 layer with reactive ion etching (RIE), based on a gas mixture of fluoroform (CHF_3) and oxygen (O_2). The remaining resist on the backside is removed with an oxygen plasma. The SiO_2

pattern is used as a hard mask to etch the pattern into the underlying InP substrate. This has been tested on several structures and has created reliable results.

The photonic wafer provided by HHI had a strongly polluted backside. It is normally removed by a substrate polishing step, as it is offered by HHI. However, this has not been requested because the risk of breaking the wafer during this step seemed to be too high. An attempt to clean the backside of the wafer with an oxygen plasma was unsuccessful. Other methods of cleaning this backside had not been tested, due to the risk of damaging the topside. Because of this backside pollution the surface is very rough. This affected the result of the pattern transfer into the InP. After etching the pattern into the InP substrate, and subsequently removing the SiO_2 hard mask, the achieved contrast between the InP surface and the etched pattern would not be sufficient. Therefore, it has been decided to keep the SiO_2 layer in place for the wafer-to-wafer alignment.

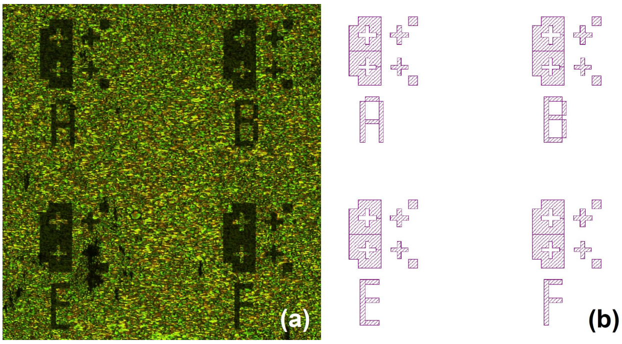

Figure 3.3: Picture of SiO_2 markers on the backside of the InP wafer from HHI (a) and the used pattern design (b)

In figure 3.3 the designed and realized SiO_2 markers can be seen. The disadvantage of this approach is that the dielectric layer introduces strain, which could be problematic for the bonding process.

The last step of the backside marker process is the removal of the photoresist protection layer from the topside. This is achieved with an oxygen plasma, followed by a 2 minutes bath in diluted phosphoric acid (H_3PO_4) (10 %) to remove possible oxidized and phosphorus depleted InP surface layers.

3.3 Wafer Bonding

The adhesive wafer bonding is an essential part of the photonic electronic integration process. The general technique is well known and described in literature [34]. The main challenge here is the combination of two materials with different properties. To enable this concept as a valid future technology, the bonding process has to achieve an alignment accuracy in the order of a few micrometres, while compensating for the wafer topologies.

The photonic wafer has a topology of 7 μm, while the electronic wafer has a topology of 3 μm. To achieve the best bonding result the wafer surfaces have to be planarized. To achieve this it is important to choose a suitable adhesive polymer. Based on experience within the IMOS platform, BCB is selected as the adhesive polymer. It is available in various dilutions (with solid content of 35, 43, 57 or 63 %) enabling different viscosities and therefore different ranges of layer thickness. It has a planarisation degree of more than 90 % [35]. This value refers to the topology reduction, which can be achieved by using a polymer layer with twice the thickness of the maximum step height in a given topology. This planarisation degree is sufficient for the intended process. For the photonic wafer this means that the initial topology of 7 μm can reduced to 700 nm by applying a 14 μm thick BCB layer. For the electronic wafer a layer of 6 μm would be needed to reduce the topology to 300 nm. This implies a total thickness of more than 20 μm of BCB. The IMOS platform on the other hand uses a thickness of less than 2 μm. There are several advantages of having such a thick dielectric layer between the two wafers. It decouples the electromagnetic, thermal and optical interaction of the two domains. For the bonding process itself a thick layer of BCB is beneficial as it can tolerate unwanted small particles to a certain degree, and therefore reduces the probability of bonding defects. However, the application of thick polymer layers is more difficult.

The results reported in this work are achieved using spin coating. The starting point is the experience within the IMOS platform. There the polymer is only spun coated on top of the InP wafer. In IMOS this is the only wafer incorporation topology. When using a fully processed BiCMOS wafer instead that approach seems unusable. Therefore spin coating BCB on both surfaces is introduced. Each BCB layer thickness is targeted to be twice the corresponding wafer topology, to achieve a planarisation of 90 %.

In the following the quality of a wafer-to-wafer bond is determined from inspection of the intermediate polymer layer. This has to be smooth, without inclusions of gas bubbles or particles. Additionally, the interface between the two different BCB layers must be invisible, which indicates good crosslinking. These criteria are difficult to evaluate as both InP and Si are non-transparent for visible light. Therefore initial bonding tests are performed using a silicon and a glass wafer. The bonding experiments are combined with alignment tests, which also rely on microscope inspection. Marker structures are fabricated on both wafers. The silicon wafer has alignment markers etched in a silicon nitride (SiN_x) layer, while the glass wafer uses metal structures created with a lift-off process.

Before applying BCB a preparation step is needed, to improve the adhesion between the semiconductor surface and the polymer. For this both wafer surfaces are covered with a SiO_2 layer, using a low temperature ICP-CVD process. SiO_2 provides a good foundation for the adhesion promoter AP 3000, which is recommended by the polymer supplier [30] to achieve strong chemical bonds with the used BCB type [36]. Before applying the adhesion promoter it is necessary to extract gaseous chemical residues which are formed at high temperature within the SiO_2 layer. Skipping this step would mean that the gas bubbles will form during the actual bonding process. These would disable further processing steps which use vacuum chambers. Outgassing of the SiO_2 layers is performed in a nitrogen (N_2) atmosphere for 1 hour at 240 °C.

After spin coating the adhesion promoter, BCB[1] can be applied by spin coating. The resulting layer thickness depends on the used spin coater type, the acceleration, the spin speed and the BCB type. For the InP wafer a polymer dilution with a solid content of 63 % is deposited. This results in a 16 μm thick polymer layer when using a closed spin coater with a spin speed of 2000 rpm. With the same settings and a solid content of 57 % in the BCB dilution, a 7.5 μm film can be achieved, which is used for the BiCMOS wafer. Both polymer layers are thicker than the required minimum values (6 and 14 μm). After spin coating the BCB on both wafers a soft bake is performed, to remove remaining solvents. The polymer state after this will be called "soft baked". It is done on a hotplate at 100 °C for 5 minutes. The soft baked BCB has a cross linking percentage as delivered of 35 %.

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[1] The Commercial cyclotene 3000 series from Dow [30] is used

In the next step the wafer alignment tool is used to position the two wafers with respect to each other and fix them in one bond assembly. The process is performed by adapting the tool, which was used before during the InP backside marker lithography (see section 3.2). In figure 3.4 the schematic of the new tool configuration is presented. The tool frame parts are coloured in grey.

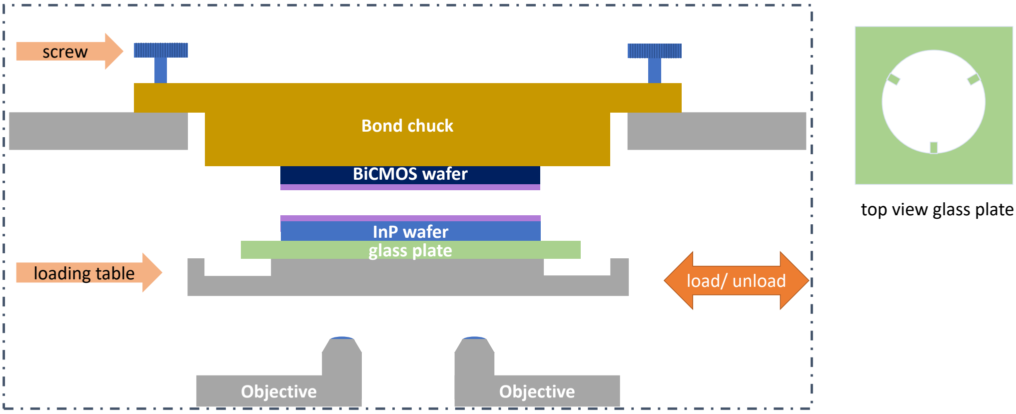

Figure 3.4: Schematic of the wafer assembly by using backside alignment after loading both wafers: bond glass (light green), InP wafer (bottom) and BiCMOS wafer (top)

At the top the bond chuck (yellow) is added. It is fixed to the frame with three screws (blue, in the schematic only two of them are shown). After the alignment these screws are removed, in order to transfer the bond chuck together with the clamped wafer stack, to the bonding tool.
The alignment process starts with placing the bond chuck into the tool and fixing it. Then the BiCMOS wafer, is loaded, with its bonding interface facing downward. First this wafer is placed on a specific bond glass on the loading table. In the top right hand side of figure 3.4 a schematic of the bond glass is shown. In the centre a circle is cut out with a diameter of 3 inch. It is discontinuous, as three small rectangle pins are positioned at the edge of the circle, facing towards its centre. These are placed at 120 degree angles. The wafer is carried by these pins, which are the only contact points. This minimizes the wafer interaction with the holder, thereby limiting pollution of the soft baked BCB. The bond glass itself is fixed with vacuum on the loading table. An image of the BiCMOS alignment features is stored, using the two objectives at the bottom. They are then locked at their locations. The alignment markers need to be placed within the two windows cut into the loading table (indicated in the top right hand side of figure 3.2). This is an important detail, as the used markers are part of the actual BiCMOS design cell. In section 2.1 "design flow" it was mentioned that the designs have to be aligned regarding the following processing. This is referring to the window positions of the alignment tool.
In the next step the loading table is lifted to bring the BiCMOS wafer into contact with the bond chuck. The wafer will be fixed to it by swapping the vacuum from the loading table to the bond chuck. After the table is lowered again the InP wafer can be loaded, with the BCB coating facing upward. This situation is captured in the schematic shown in figure 3.4. The backside markers of the InP are facing the two objectives and can now be aligned to the stored image from the BiCMOS wafer. For the first realization the top metal lines of the electronic wafer design are used as alignment features. After the alignment step both wafers are brought into contact. To fix the alignment two mechanical clamps are used to fix the wafers in-between the bond glass

and the bond chuck. In the last step before the actual bonding, this bond assembly is removed from the alignment tool. In figure 3.5 a picture of the bond assembly is shown. The two red arrows show the mechanical clamps holding the bond glass in position. The three white arrows point at the rectangular pins, which are the only contact points of the bond glass with the wafer stack underneath. In the cut out (the central open circle in the bond glass) a dark grey pressure disc, made from graphite, is placed. The picture in figure 3.5 shows how the assembly, formed by bond chuck, wafer stack, bond glass and pressure disc, is placed in the bonding tool. The pressure disc is slightly thicker than the bond glass, in order to transfer the bonding force uniformly to the wafer surface. This force is applied with a piston from the top, pressing downwards onto the pressure disc. The InP wafer is on top now, so the assembly has been flipped with respect to the alignment process. InP is a fragile material and during the initial bonding experiments it cracked several times. BCB leaks through these cracks and thereby pollutes the pressure disc. This introduces non uniformities for subsequent bonds and thus the pollution has to be removed. It is difficult to clear cured BCB as the etching solution for this attacks other materials as well. For this reason the initially used graphite pressure disc has been replaced by a glass one, which can be cleaned in a piranha solution: a mixture of sulfuric acid, water and hydrogen peroxide. A disadvantage of the glass pressure disc however is its lower thermal conductivity, which has to be considered while designing the actual bonding recipe.

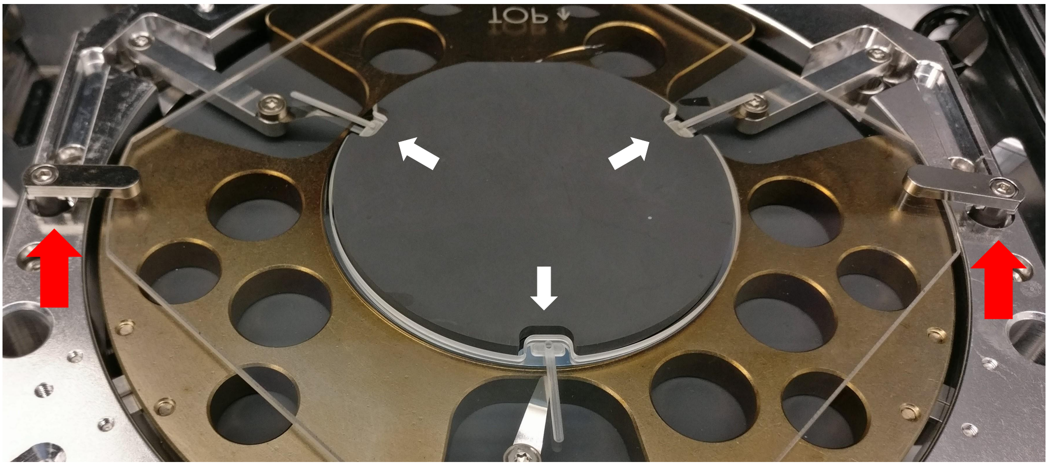

Figure 3.5: Picture of the bond assembly with a wafer stack (not visible) hold in position by bond glass and the pressure disc insert

The bonding is performed using the following sequence:

1. closing the chamber
2. heating up 100 °C
3. evacuating the chamber
4. applying a bonding force of 700 N
5. releasing the force
6. floating the chamber with N_2
7. heating up to 240 °C
8. curing the BCB for 10 hours
9. cooling down to room temperature

The final step is removing the bonded wafer stack from the bonding tool.

Several process parameters have been surveyed to accomplish this process flow. BCB and its properties have been of particular influence on the process, which will be explained in the following.

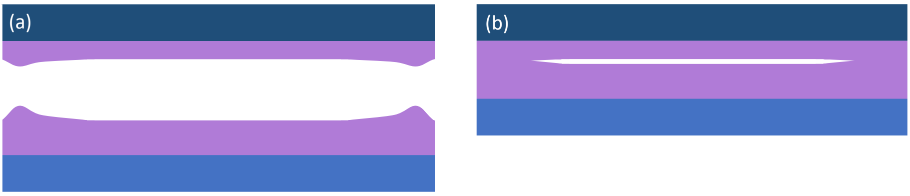

Figure 3.6: Schematic of two wafers with spin coated BCB - separated from each other (a) - in contact (b)

In figure 3.4 the BCB layer on top of the wafer surfaces is presented as a flat and levelled layer. A more accurate schematic of these layers is shown in figure 3.6 (a). Applying BCB with spin coating results in so-called edge beads; a local thickening of the polymer around the circumferences of the wafers. This effect depends mainly on the viscosity of the polymer. For the BCB used the viscosity is high and the related effect is thus non-negligible. This influences the bonding quality. In case that both wafers are brought into contact directly after soft baking an air inclusion is created, see figure 3.6 (b). The edge beads of both wafers merge and seal the air inside. This leaves no path for the air to be evacuated. Literature [37, 38] suggests that BCB with a slightly higher level of cross linking can also be used for bonding. By increasing the cross linking from the after soft baking 35 % to 43 % [37], the material hardens and the two edge beads will not merge completely. The air in the centre can therefore be evacuated before applying the actual bond force. This idea has been tested by curing the BCB on both wafers for 1 hour at 175 °C (in an N_2 atmosphere to avoid oxidation of the polymer [35]). The resulting bond was however incomplete. Only the edge beads are found to be bonded. The used bond force (700 N) is apparently not sufficient to bring both BCB surfaces into full contact. Increasing the bond force could overcome this problem, but this induces a high risk of breaking the InP wafer. Therefore, it has been decided to cure only one polymer layer, instead of both. In this way the edge bead on the other wafer will still be soft enough to allow both wafers to be pressed together.

The BCB layer on the BiCMOS wafer is chosen to be pre cured at 175 °C for 1 hour. It is thinner than the layer on the InP wafer (7.5 μm compared to 16 μm), which enables a better full contact after applying the bond force. The result is a defect free bond, as assessed with visual inspection. This is due to the non-uniformity of the edge beads. The soft baked polymer layer on the InP side is not able to fully compensate variations of the (pre-cured) edge bead on the BiCMOS side. Therefore the air in the centre is not sealed and can be evacuated when pumping down the bond chamber. The bond force of 700 N however is sufficient to bring the soft baked BCB into full contact with the pre-cured layer, which leads to a good bond result. This method is used for all presented wafer bonding results, if not mentioned otherwise.

In figure 3.1 (b) the air-bridge structures from HHI have been introduced. The gaps below the air-bridges are not filled by HHI. As mentioned before, the viscosity of the used BCB is relatively high. Therefore it is uncertain if these air-bridges can be refilled. The dimensions of these structures vary depending on the BB. They can be several tens of micrometres long and the gaps below are only a few micrometre high. To evaluate the capability of the BCB used to

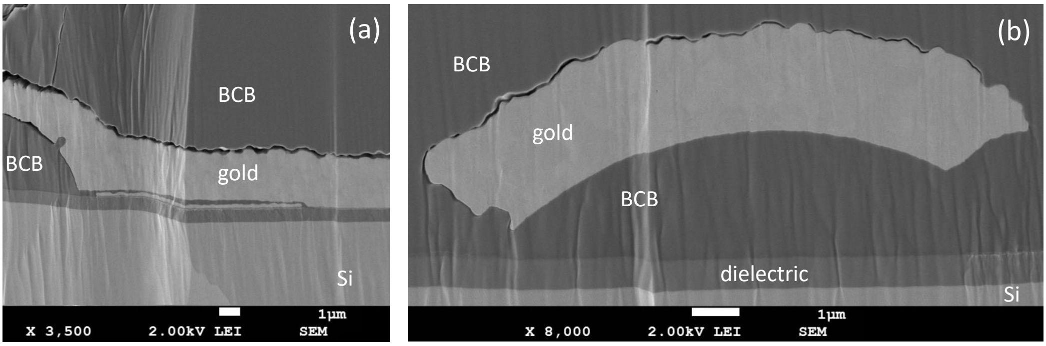

Figure 3.7: Scanning electron microscope (SEM) pictures of cross sections of two different metal air-bridges surrounded by BCB; in (a) the anchor is visibly attached to the dielectric layer (on the right side); in (b) a top part of the air bridge is shown (pictures taken by Tjibbe de Vries)

fill these trenches, without incorporating air, test structures are fabricated[1]. In figure 3.7 two scanning electron microscope (SEM) picture of a cleaved test wafer is shown, with the cross sections at the position of an air-bridge. In picture (b) the metal air bridge is completely surrounded by BCB. At the bottom of both pictures two different materials can be identified. This is a silicon wafer with a dielectric layer on top, on which the air-bridge is fabricated. In can be seen that the air-bridges are fully sealed with BCB. This indicates a good refilling of the structures. This initial result has been confirmed during the fabrication of the first hybrid modules using the HHI material.

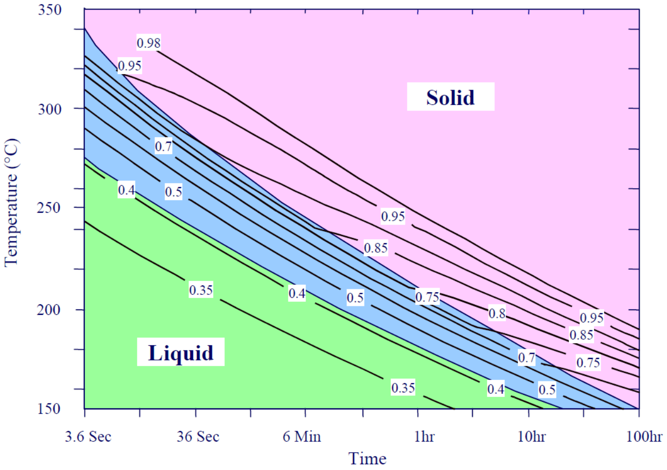

Figure 3.8: BCB cure depending on the used temperature and time [30, 39]

In [39] the temperature and time dependency for curing BCB are investigated. Figure 3.8 shows the visually enhanced plot resulting from this paper. It can be seen that BCB can be cured faster when using higher temperatures. A 98 % BCB cure can be achieved at 250 °C after 1 hour

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[1] The fabrication has been done in cooperation with Tjibbe de Vries and Barry Smalbrugge

or at 220 °C after 10 hours. To be certain that a full BCB cure is performed a tolerance margin can be added by increasing temperature, time or both. The chosen process parameters are defined by the limitations of the BiCMOS-devices. It is important to guarantee that each element still works as designed after the integration process. For that purpose several low noise amplifier (LNA) chips [40] are used to perform temperature treatment tests. In cooperation with the IC-group[1] the gain curves of these devices are measured before and after these tests. As the available number of samples is limited, a more in-depth analysis is not possible. It could be seen that the devices start to degrade after exposing them to a temperature of 280 °C for 1 hour. For 240 °C no degradation has been detected, even when extending the time to 15 hours. Based on these results the whole integration process has been aimed at a maximum temperature of 240 °C. A curing time of 10 hours is chosen to assure a full BCB cure.

3.4 InP substrate removal

After bonding the two wafers, the electrical interconnects have to be realized. For this the InP substrate has to be removed. In the following paragraph this process is explained. The impact of the different CTEs for the two wafer materials will be introduced. Its impact on the process will further be explained in section 3.5. At the end of this section process anomalies of the first hybrid module realization are discussed.

Before the InP-substrate can be removed, the backside of the wafer has to be cleaned. That begins with removing the SiO_2 layer, which has been used as the alignment mask. This layer is etched using a RIE process. The applied plasma is based on a gas mixture of CHF_3 and O_2 (ratio 10:1). In the next step another RIE etch is applied to remove residuals of BCB covering the outside edge of the wafer. This material is squeezed out during the bonding process and covers the sides. To enable a complete substrate removal these polymer residuals have to be removed. The plasma used for this is based on CHF_3 and O_2, in the ratio of 1:5, with a high chamber pressure of 50 mTorr. Afterwards, the substrate can be removed by selective wet chemical etching using a mixture of hydrochloric acid (HCl) and water (H_2O), in the ratio 4:1 at a temperature of 35 °C [41]. The used RIE process to etch the BCB however has an anisotropic character. That means that the substrate itself shields parts of the lower wafer edge. To overcome this the polymer and substrate are removed in two cycles. Each consists of a RIE step to remove the BCB, followed by the wet chemical InP etch. The complete substrate removal takes 50 minutes, which is divided equally into 25 minutes per cycle.

Subsequent to the InP substrate removal the etch stop layer is resolved wet chemically using a solution based on H_2O, sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2), in the ratio 10:1:1. After this the dicing lanes and post processing markers should be visible. In figure 3.9 a picture of such an assembly is presented. The InP-membrane is at the top. It is covered with a SiO_2 layer (navy blue), which will be used as a hard mask for the following etching steps, which will be explained in the next section.

The two bonded wafer have a differed CTE. The value for InP at room temperature (20 °C/ 293 K) is 4.75E-6 K^{-1} [42, 43] and for silicon it is 2.55E-6 K^{-1} [44, 45]. As both materials are bonded at high temperature (240 °C/ 513 K) and cooled down to room temperature an expansion mismatch of 4.84 ppm will be stored in the form of strain within the bonded wafer stack. Part of it is released in mechanical deformation. By inspecting the bonded stack after the bonding this can be detected in form of a warping effect. By reducing the photonic wafer

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[1] Xi Zhang ,Zhe Chen

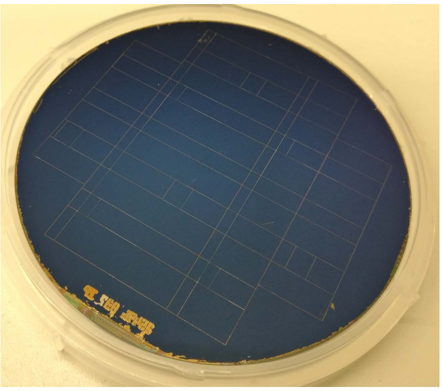

Figure 3.9: Picture of the bonded wafer stack after substrate removal, the obtained InP membrane is at the top with an unpatterned SiO_2 layer

thickness, during the InP substrate removal, the membrane becomes more flexible, therefore the mechanical warping effect is reduced.
During the first hybrid module realization process the dicing lanes have not been visible after removing the substrate and etch the stop layer. The reason has been an insufficient etch depth of these structures. As further processing without marker and dicing lanes is not possible, it is necessary to remove more material until these features become visible. This has been done uniformly by using several dry etch cycles until the structures became visible. Therefore roughly an extra 1.2 μm of InP has been removed. For most BBs this reduction of material has a negligible influence, except for the SSC, which is based on the diluted waveguide layer stack. This is initially closest to the substrate and therefore at the top after the etch stop layer removal. The change in dimension has an impact on the optical mode profile and the BB efficiency. It has been found that the SSC with the new estimated dimensions should still work[1], but that a higher insertion loss (IL) for SMF coupling has to be expected.

3.5 Impact of thermal expansion

In section 3.4 it has been explained that bonding two wafers with different CTE values will create strain. The fact that both wafers are bonded at a high temperature also means that the two wafers expand/contract differently, which will lead to a mismatch between the two designs. In this section the impact of the different CTE values on the design will be presented. An example of a resulting design mismatch, based on the different thermal expansion coefficients, can be seen in figure 3.10. It shows a picture of two markers, one on the glass and one on the silicon wafer. As mentioned in section 3.3 several alignment test had been performed using these wafers to verify the capability of the alignment and bonding tools. In figure 3.10 a horizontal shift of 15.4 μm can be detected and a vertical one of 2.3 μm. This marker is positioned at the coordinates [0, 32.5] mm with respect to the centre of the wafers (taken as the coordinate origin, because the thermal expansion does not shift the two wafers). Based on the marker position the horizontal shift is a superposition of the thermal expansion mismatch and the achieved alignment accuracy. To calculate both values several marker

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[1] Simulated by HHI, contact person Francisco Soares

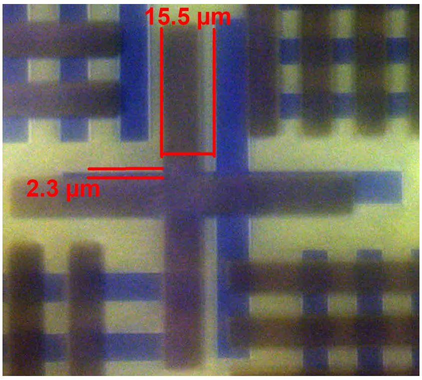

Figure 3.10: Picture of a wafer alignment marker set after bonding a fused quarts and a silicon wafer; red lines represent the marker offset measurement

positions and shifts have to be measured. The values are fitted towards the original design using variables for rotation, magnification, horizontal and vertical shift. The misalignment of the two wafers has been determined to be 2.6 μm (horizontally) and 2.3 μm (vertically). The measured thermal expansion is 554 ppm. At the shown marker position [0, 32.5] mm (figure 3.10) the thermal expansion based mismatch is 18 μm.

In section 3.4 the CTE values at room temperature for InP (4.75E-6 K^{-1}) and silicon (2.55 K^{-1}) have been given. Based on the experience with the IMOS platform, it is known that the photonic membrane is stretched less than expected. The predicted value is based on the curing temperature and the difference between the two CTE values, which is equal to 2.2e^{-6}. IMOS is curing the BCB at 280 °C that would translate to a membrane expansion of 572 ppm. However, the measured value is only 310 ppm [46].

The process presented in this work uses a different bonding temperature and a thicker BCB layer and photonic membrane. It has been decided to measure the expansion value instead of simulating it. Therefore two InP test wafers are prepared with through membrane marker structures and dicing lanes. Each has been bonded to a silicon wafer. Sequentially the substrate and etch stop layer have been removed, so that the etch trough marker structures become visible. These are used to perform a second lithography, transferring a pattern which includes matching marker structures. The used mask is aligned towards the initial positions without thermal expansion correction. By measuring the differences between the two marker sets the thermal expansion can be calculated using the same fitting variables as before. For the two test wafers 307±10 ppm and 301±9 ppm have been measured. These values are smaller than the expected 484 ppm (based on 240 °C), but similar to the reported IMOS value. One possible explanation it that the used BCB layer has an elastic capability that compensates part of the thermal expansion mismatch and therefore reduces the overall value.

The InP membrane is stretched after bonding by a factor of 1.000305, which influences the overlay of the photonic and electronic circuits. This has to be taken into account during the different wafer designs. As there is no influence on the BiCMOS design, the InP design has to be adapted for this effect. It has to be reduced by the scaling factor of 1.000305. The mask used for realizing the backside alignment markers includes structures matching the photonic design (before bonding) and the electronic design. These markers should therefore be positioned without being scaled. This enables the optimum alignment result. For the first realization of the hybrid modules the InP design has not been adapted. The resulting structures have a systematic mismatch, which can accumulate to upto 9 μm (30 mm away from the centre), based on the linear thermal expansion. For this reason, all post processing masks are expanded with the scaling factor.

3.6 Electrical Interconnects

In this section the realization of the electrical interconnects is explained. It is divided into two parts. The first explains the different process steps needed to fabricate the electrical interconnects and motivates the decisions that have been made. The second part presents the challenges that appeared during the first hybrid module realization and how these have been addressed.

3.6.1 Fabrication

After removing the InP substrate the electrical interconnect fabrication starts by opening the InP membrane, to access the photonic metal structures. Subsequently the polymer between the two wafers is etched to open up the BiCMOS metal pads. The electrical connection between both is achieved by covering the sloped intermediate polymer with metal. In this section these three steps are explained in detail.
Different types of contact pads are present, these can be grouped into pads that are either used for the interconnect fabrication, or for direct device probing. The BiCMOS contacts used for direct probing are designed to supply the necessary inputs. The hybrid devices are fed via these probing pads. Most of the photonic surface is used for independent test structures, it is important to enable the characterization of these as well by opening the InP metal pads for probing. All contact pads are opened with etching through the complete InP membrane. For this a hard mask is used, which is created first by depositing and patterning a SiO_2 layer. The ICP-CVD is used for this deposition to keep the samples at sufficient low temperature. Next photoresist is spin coated and afterwards patterned with optical contact lithography. It is transferred into the SiO_2 layer with a RIE process based on CHF_3 and O_2 (ratio 10:1). Next the remaining photoresist is removed. In figure 3.11 the result of this mask transfer can bee seen.

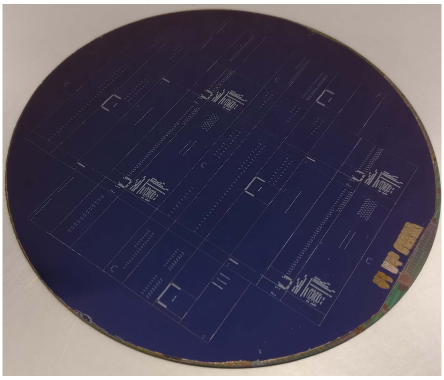

Figure 3.11: Picture of the bonded wafer stack, the InP membrane is at the top with a patterned SiO_2 layer

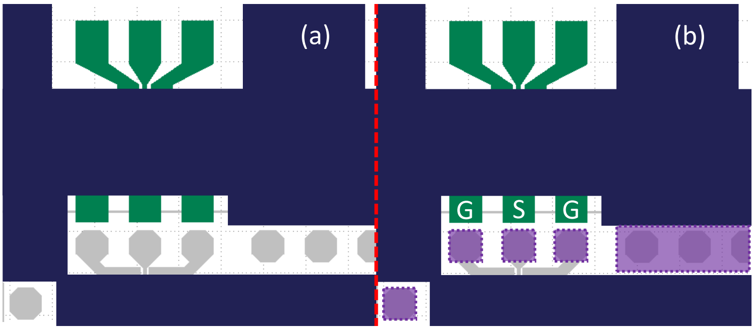

Figure 3.12: Designed windows etched into the photonic membrane (blue) to open the InP (green) and BiCMOS (silver) metal pads (a), extended by the designed BCB etch pattern (purple) (b)

The dielectric layer has a thickness of 120 nm (which corresponds to navy blue). The windows in the InP membrane are etched using an inductively coupled plasma (ICP) process, based on CH_4 and H_2. The etch is self limiting, as it stops either on the photonic metal pads or on the BCB. In figure 3.12 (a) a schematic top view of the etched windows is presented. The blue part represents the area where the InP membrane is still in place. The green structures are the photonic metal pads and the silver pattern represent the electronic metal pads. The latter are still buried under the (transparent) intermediate polymer. After the InP etch, the hard mask is removed using the dry etch process for pattern SiO_2.

The following step is etching through the BCB layer to open the BiCMOS metal pads. This is done with a dry etch process based on CHF_3 and O_2 plasma (ratio 1:5). The masking pattern for this is transferred into photoresist using contact lithography. The resist layer has a total thickness of 24 μm. Etching more than 20 μm of BCB (7.5 μm + 16 μm) with one single photoresist layer of 24 μm is not possible, as the resist is etched slightly faster than the BCB. Increasing the photoresist layer thickness even more is limited by the lithography process. It has not been possible to find a exposure dose suitable for thicker resist layers. The reason is the non-uniform reflectivity of the underlying BiCMOS wafer. The values vary between high, in case of metal contact pads, and low, in case of passivation layers. Everything is exposed with the same UV light source, but the effective dose is different due to the change in reflectivity. It is important to find an exposure dose which enables open patterns independent of the underlying structures. During the exposure N_2 is formed. If the dose is too high the gas can not diffuse out in time and bubbles are formed, which destroy the resist patterns. The total dose can be split in several cycles, consisting of a short exposure times followed by long pauses, to enable the N_2 to diffuse out. However, this dose optimization becomes more difficult for thicker photoresist layers. Additionally, the lithography result generally worse for thicker photoresist layers. Due to all of this the polymer layer is etched in two steps, each using the same mask transferred into a 24 μm thick resist layer. The etching time is divided into two equal blocks. After completing the first etching cycle the remaining photoresist is first removed before spin coating the new layer which is used for the second cycle. This approach has the disadvantage that the two mask lithography will be slightly shifted relative to each other. This will result in a small step in the BCB sidewalls, which has further no influence on the process.

Relying on thick photoresist as etch mask results in sloped sidewalls, as the material reflows and reshapes during the etching process. This effect is depending on the temperature within the RIE chamber. The impact of this reflow has been analysed to define the boundaries of the

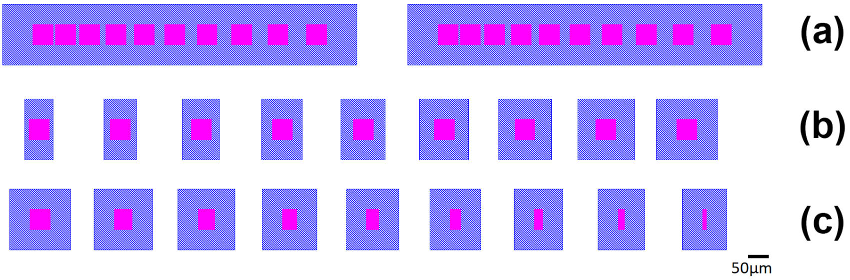

Figure 3.13: Design of the polymer etch test structure showing the InP etch pattern (blue+pink) and the BCB etch pattern (pink)

process. In figure 3.13 the design of an etching test series is presented. Each row is intended to analyse one of the following parameter:

- (a) the minimum distance between two independent etched polymer openings (d_{opening})
- (b) the minimum distance between etched BCB opening and etched InP opening
- (c) the smallest possible BCB opening (width, w_{design})

The etching results are analysed by measuring the height profile for each row. In figure 3.14 the step height measurement of one BCB opening is presented. The top level represents the backside of the InP wafer, which is used as reference level. The first step of 5.1 μm represents the etch through the photonic membrane. The second, deep step is the result of the polymer etch. The width, w_{design}, at the bottom of opening is designed to be 25 μm wide. This actual value is only 21 μm. This indicates that the used dose is too small, or the development time too short. In figure 3.15 the achieved pad opening widths are plotted for the intended design values. Each dimension is round 5 μm smaller than the design value. The total polymer etch depth is 21.8 μm, which is close to the target value of 20 μm. An important note can be made that even the smallest pattern, with a measured value of 5 μm, is opened completely, representing an aspect ratio of more that 1:4 (width:height).
The left and right polymer slopes are different in angle, which is based on the double lithography step and the introduced shift thereby. The left slope has a horizontal expansion of 16.6 μm and the right one 28.8 μm. For optical contact lithography an error of 1-2 μm would be acceptable. The measured difference is too large to be explained by standard lithography tolerances. This will be discussed in section 3.6.2. The slope is the determining factor for how close two BCB openings can be placed without influencing each other. If the distance between two openings, d_{opening}, is less than twice the lateral expansion of the slope, w_{slope}, the polymer trench between the two structures is reduced in height as the etched profiles start to overlap. This can be expressed by:

$$d_{\text{opening}} \geq 2 \cdot w_{\text{slope}}$$

An minimum value can be estimated by summing the lateral expansion of the left and right slope. This gives 45.4 μm and represents the estimated minimum distance between two BCB openings. However the measured value based on the design shown in 3.13 (a) is 40 μm.

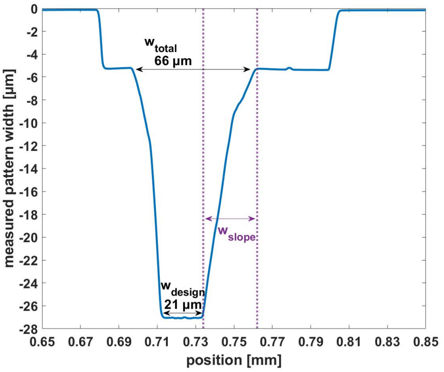

Figure 3.14: Measured height profile of the through polymer etch.

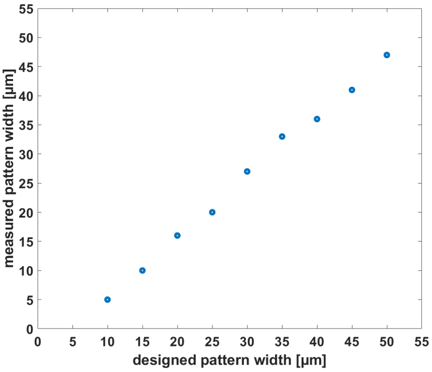

Figure 3.15: Plot of the measured pattern opening for the different designed values.

The electrical interconnects are realized using electroplating. For this a seed layer has to be deposited, which covers the entire surface, including the sidewalls. Several techniques can be used to achieve this, like sputtering, atomic layer deposition (ALD) or metal evaporation. The latter is the standard process available in the Nanolab@TU/e clean room. It has the disadvantage of being strongly directional. That means boundary conditions have to be respected to enable the coverage of all structures, including their sidewalls. In figure 3.16 a schematic of the metal evaporation tool is presented. The sample is clamped on a holder at the top of the metal evaporation chamber. The assembly is angled by 45 ° relative to the metal source, which is at the bottom of the tool. The sample rotates continuously during the deposition. The rotation axis is in the centre of the holder and normal to the bonded wafer stack. This setup enables metal sidewall coverage for all structures having a etch depth equal to or smaller than their total opening dimensions (w_{total}). For deeper structures the sidewalls will give shadowing effect, resulting in metal free surface areas.

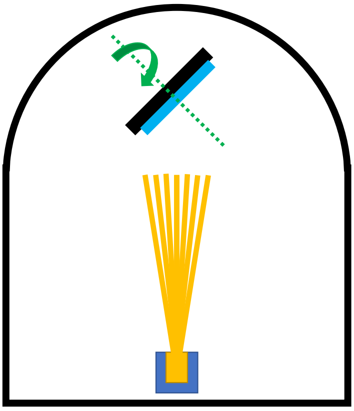

Figure 3.16: Schematic of the metal evaporation process: at the bottom of the chamber (black) is the metal source (yellow) while the sample (blue) is fixed on the rotating holder at the top

Beside covering the entire surface with a seed layer, it is required that the actual interconnect can be realized with electroplating. For this one slope of the BCB opening will be used to connect the two electrical contact layers. This is realized by designing the two metal pads with a lateral shift equal to the lateral expansion of the polymer slope (w_{slope}). In figure 3.12 (b) an example of the polymer etch pattern, coloured in purple, is presented. In this schematic the electrical interconnects will be created between the InP G-S-G pads and the three corresponding BiCMOS pads below. As mentioned the two pad arrays are lateral separated to enable the interconnect over the sloped polymer sidewall. On the right hand side of the schematic another group of BiCMOS pads will be opened. While the interconnect pad pairs are accessed through individual etched openings, the second group uses only one etch window. This is an example for pads designed for direct probing.

The BiCMOS metal pads are made of aluminium. The dry etch process used to open these is based on fluorine (CHF_3) and oxygen (O_2). The aluminium acts as a natural etch stop layer, as the top layer forms aluminium fluoride (AlF_3) or aluminium oxide (Al_2O_3) which both blocks further etching. The formed monolayer has no measurable influence on the electrical interconnect performance.

The deposited seed layer consist of 50 nm titanium, for adhesion, and 100 nm gold as a seed for the electroplating bath. Before entering this first a masking pattern has to be defined. That is done by optical contact lithography. Several photoresist types had to be investigated for this process step. The challenge is the topology of more than 25 μm. Initially it has been attempted to cover the wafer with a thick photoresist layer, with a thickness larger than the topology. This failed for the same reason as given before in the context to etching the round 20 μm with a single resist layer. Furthermore to cover the wafer topology a photoresist with low viscosity has been used, which is capable of covering the entire topology profile. This works best with smooth transitions in the topology profiles. At sharp interfaces, like the edges of the InP openings, the resist thickness is reduced due to the surface tension. This effect has been countered by using multi layer spin coating.

After exposing and developing the photoresist, a short descum O_2 plasma is used to obtain a hydrophilic surface before entering the electroplating bath. The gold growth rate is controlled by setting the electric current, measured between anode and cathode. The value depends on the total electroplating area and has to be calculated beforehand. This process step is simultaneously used to make heat spreader (see section 2.3) on the backside of the modules and to place markers for identifying the different buried photonic structures. The use of these will be shown in chapter 4. After electroplating the photoresist mask is removed.

The last step of the wafer fabrication is a wet chemical removal of the seed layer. The gold is etched with potassium cyanide (KCN) and subsequently Ti is removed by a solution of oxalic acid, 4 mol/L potassium hydroxide (KOH) and H_2O_2. Then the wafer is ready to be diced into individual modules.

In this section the development of the full interconnect process is described. However, when realizing the actual hybrid modules several issues appeared, which will be discussed in the next section.

3.6.2 First hybrid module realization

The wafer scale fabrication of the hybrid modules is the first complete demonstration of the developed process. A few deviations from the ideal fabrication have been made towards unpredicted circumstances, like the polluted InP backside (substrate) and the reduced etch depth of the dicing lanes and post processing markers. In the following section the impact of a tool based mistake will be explained, showing how the electrical interconnect process flow has been adapted to achieve the best possible result.

To test the different process steps, before using them on the actual HHI wafer, a dummy InP wafer has been created. This so called "front runner" has been processed at the TU/e. It consists of a 6 μm thick epitaxial InP layer and a 300 nm thick etch stop layer. It includes the through membrane dicing lanes and marker structures. The wafer also includes metal patterns, created by electroplating, imitating the HHI metal pads.

The first step of the electrical interconnect realization is the opening of the InP membrane. At that state an alignment error between the two wafers can be detected and measured.

Before using the bond tool it has been re-evaluated to guarantee the specified performance. During these test it is noticed that a systematic wafer shift in one direction appears for all bonded samples. This was not the case during the process development phase, where reproducible alignment errors of less than 4 μm for various BCB bonding layer thicknesses had been achieved (see [47]). To find the cause of this shift several components of the tool have been tested, but without conclusive results. By using a glass and silicon wafer it is proven that the alignment tool works according to its specifications. Therefore the shift is resulting from the bonding tool itself. However, the shift between the bonded test wafers, glass and silicon, has a reproducible value of 90-110 μm. This shift is unacceptable for further processing. Therefore it has been tested if it can be compensated by aligning the two wafers with a compensation offset of 100 μm. The resulting shift after bonding is reduced to 10 μm, which is acceptable.

The shift, and therefore the pre compensation, depends on the used wafer thickness, used BCB layer, bonding recipe and the wafer topology. The first three parameters are comparable for the glass-silicon bond and the actual InP-BiCMOS fabrication. However, the test structures do not include topology. Therefore it has been decided to use the before mentioned front runner, which will be bonded to a BiCMOS wafer, to determine the resulting wafer shift.

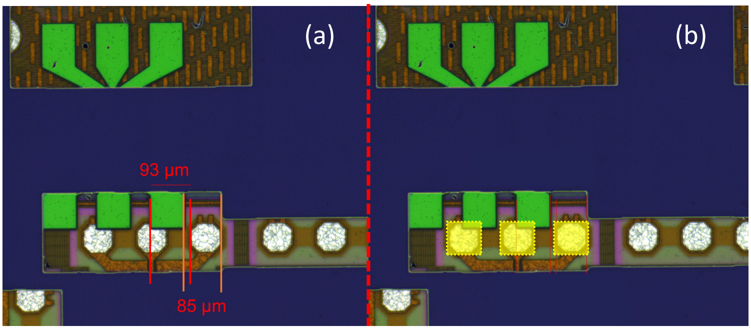

Figure 3.17: Picture of the bonded HHI wafer onto the BiCMOS wafer, after opening of photonic membrane (a) including the intended BCB etch pattern positions (yellow) (b); the wafer shift is 89 μm

After removing the InP substrate and etch stop layer, the metal structures of both wafers can be recognized as an imprint on the backside of the InP membrane. The overlay of both metal structures enables an estimation of the wafer shift. The offset between the two wafers is too large to continue with the intended process. The pattern of the InP etch mask would not open sufficiently large areas to access both metal pads of the interconnection. Therefore the used mask needed to be transferred twice into the dielectric hard mask, and thus into the photonic membrane. One mask is aligned to the marker structures, the other is placed with an offset to compensate the wafer shift. Both mask patterns are overlapping resulting in larger merged windows. After opening the InP membrane with this hard mask a 30 μm shift is measured. This value is used for the pre alignment compensation of the actual HHI wafer.
The estimated wafer shift for the bonded HHI wafer, visible after the substrate and etch stop layer removal, is around 100 μm. Therefore the same approach of multiple mask exposures is used to open sufficiently large areas. In figure 3.17 (a) a picture of the HHI wafer, after etching through the InP membrane, is presented. The measured wafer shift is 89 μm. Furthermore the wafer is shifted in the opposite direction, which means that the 30 μm pre-alignment increased the shift, instead of compensating for it. So far it has not been possible to identify the reason for this wafer shift. It is assumed that the clamp force, which is used to keep the two wafer aligned and in place while transferring the bond chuck from the wafer aligner to the bonder, is not uniform and therefore induces an imbalance during the bonding process. This is supported by the observation that these clamps are orientated in the direction of the resulting wafer shift. However, it is decided to continue processing this structure.
After opening the InP membrane, the BCB has to be etched to continue the interconnect process. The masked used is designed to be aligned towards the marker structures embedded in the photonic membrane. Because of the large wafer shift this becomes impractical. Therefore the mask pattern is aligned directly towards the actual electronic metal pads. In figure 3.17 (b) this approach is illustrated. The yellow squares represent the mask pattern. As explained before this mask is used twice, to achieve sufficient etch depth. Based on this alignment approach the shift between the two masks is larger than normally expected from optical contact lithography. The effect can be seen in figure 3.14. It has no further influence on the rest of the process.

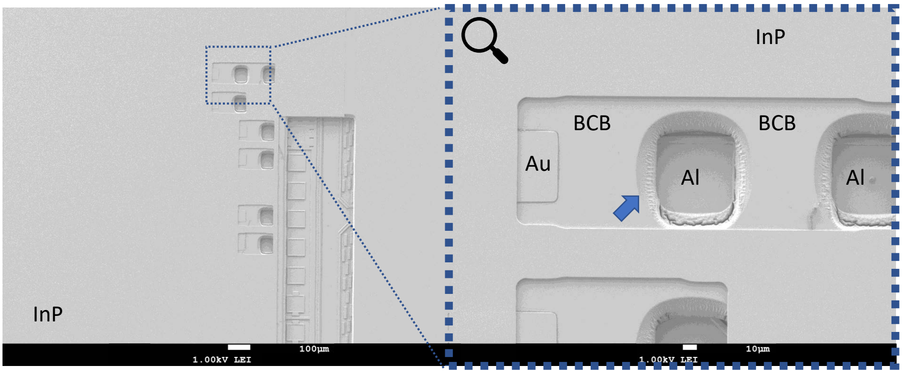

Figure 3.18: SEM picture of the seed layer covering the different structures taken with two magnifications (left and right), blue arrow indicates the BCB slope

The electrical interconnects are created with electroplating, after the seed layer is deposited with the metal evaporation process as described in section 3.6.1. In figure 3.18 a SEM picture from the front runner is presented. The blue arrow points to the BCB slope, which will be used to create the electrical interconnect. In the next step a photoresist pattern is created, enabling the following electroplating step. Optical contact lithography is used for this purpose. Based on the large offset between the two bonded wafers the initially designed patterns are too small. This is solved by transferring the mask multiple times to the positive photoresist, each time with a small shift in order to increase the resulting open area. By doing so it is important to verify that a larger metal area is not resulting in short circuiting.

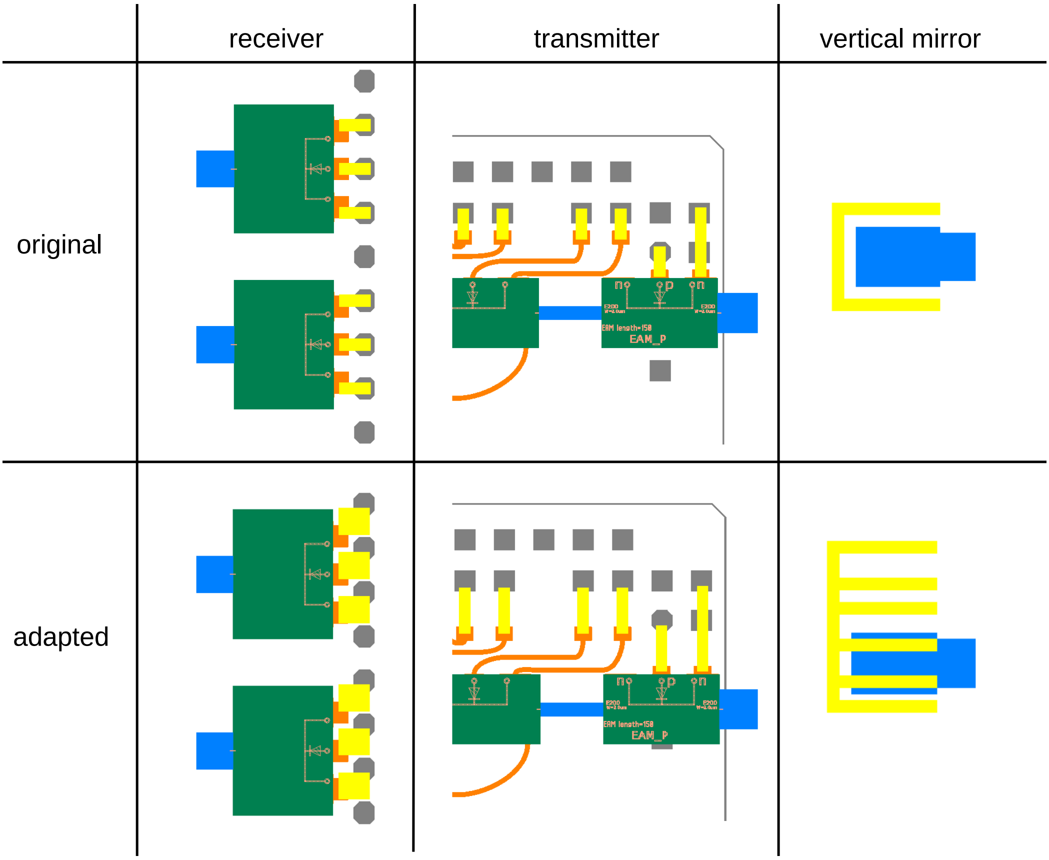

Figure 3.19: An comparison of the original with the adapted designs

In figure 3.19 three different designs are presented. The green rectangles are the photonic BB with orange contact pads. The grey shapes are the BiCMOS metal pads. Both will be connected by electroplating a gold layer (yellow structures). This layer is also used to create markers to identify the position of waveguide structures (blue) as it can be seen in the design of the vertical mirror BB (third column). The two wafers are shifted along the vertical axis. Therefore the interconnects for the transmitter and receiver design have to extended in that direction. All three designs in the bottom row have been created by transferring the original mask 3 times into the photoresist. Thereby the mask is shifted by 5, 25 and 55 μm respectively. On the basis of the designs presented in the bottom row is can be seen that extending the metal interconnects further would result in short circuiting between the contact pads of the PD. It was not possible to avoid that the resulting metal structures overlap with the vertical mirror BB. However, the actual mirror structure within is in the centre of this BB and is 2-by-2 μm large. The distance towards the electro plated gold should be sufficient to allow the mirrors to work well. The further process follows the description given in section 3.6.1.

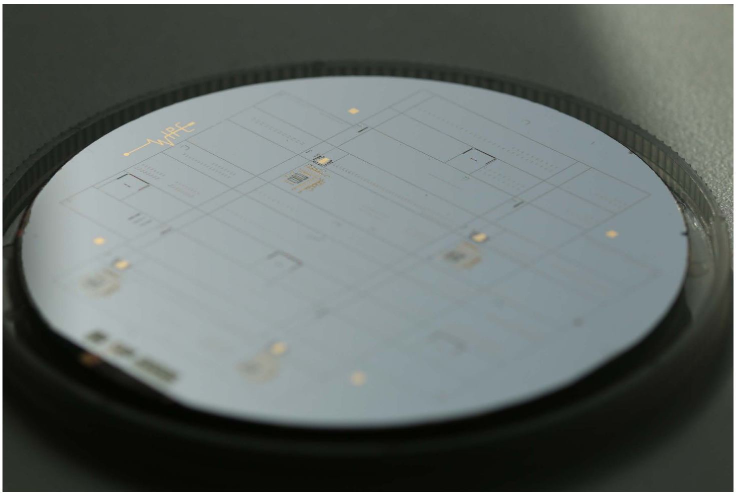

Figure 3.20: Picture of the fabricated hybrid wafer stack (Picture by Florian Lemaitre)

3.7 Conclusion

A successful demonstration of the developed 3-D integration technology has been presented. A description of the different process steps leading to this result is given. The necessary adaptations for the electronic and photonic foundries are given. These are limited to a minimum, to enable access to this technology for multiple foundries. Adhesive wafer bonding is introduced as the method of choice to enable the compensation of two wafer topologies and to simultaneously decouple the two wafers in the thermal, electro-magnetic and optical domains. The fabrication of the first hybrid module is explained. A malfunction of the wafer bonder resulted in a shift of 89 μm. However, it was possible to continue processing for most of the included devices, by adapting several lithography steps. In the following the photonic devices will be characterized to define the impact of the integration technology.

Chapter 4

Photonic Platform and its 3-D Integration

The aim of the 3D integration of photonic and electronic ICs with the technology presented in chapter 3 is the creation of a hybrid module, that relies on the strengths of each individual platform. Therefore it is important to know if the devices on the photonic and electronic wafer are operating within their specifications and compare their performance before and after the integration process. In this chapter the influence of the technology on the photonic BBs will be disused. The passive photonic BBs are characterized before and after the integration process, while the active photonic BBs are mainly characterized after the integration process. Both will be compared to the specifications of the foundry. The electronic components have been analysed in the work of Xi Zhang [21] and Gertjan Coudyzer [23].

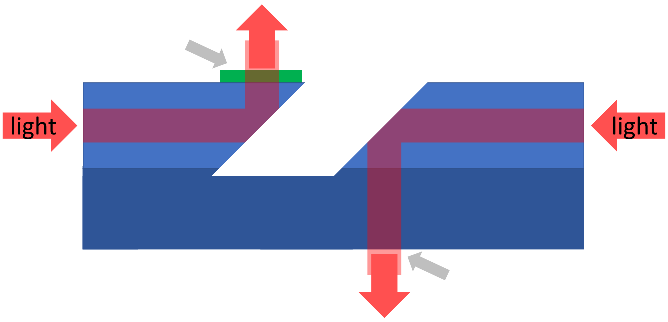

Figure 4.1: Schematic cross section of the vertical mirror building block, red arrows indicate the light path (which also holds in the reverse direction), grey arrows point at interfaces with unwanted reflection, green indicates an anti reflection coating based on dielectrics

The integration process is performed on wafer level. Thus it is necessary to characterise the photonic material on wafer level as well. As mentioned in section 2.4, special surface coupling is needed to enable this. Vertical mirrors are used for this purpose. They are based on a facet that is etched under an angle of approximately 45 ° into the waveguide. In figure 4.1 a schematic cross section of this BB is shown. The light, propagating through the waveguide, is totally reflected at the angled interface of InP and air. It is coupled out of the membrane perpendicular to the surface. The used etching process creates two mirror structures, each with a nominal angle of 45 °. One reflects the light upwards and the other one downwards, depending on the orientation of the connected waveguide. This structure enables the characterization of the InP BB. The setup used for this purpose is based on a modular approach. A schematic is presented in figure 4.2. The centre piece is the sample stage. It consist of several parts, the top one is the sample holder, which is available in different shapes and dimensions to enable the handling of single chips, bars or full wafers. The different devices are kept in place with vacuum. The sample holder includes a thermistor, which is used to detect the temperature close to the device under test (DUT). The signal is used for a thermoelectric cooler (TEC) controller to regulate a Peltier element, which is placed between the sample holder and the underlying thermal reservoir. The measurement temperature is set to 21 °C, if not mentioned otherwise. This assembly is placed on several linear stages to control the position. The sample stage is surrounded by two coupling stages, placed opposite to each other. These are assembled from linear stages for course movement and a piezo based stage for fine movement, all supporting x,y and z alignment. On top is an optical fibre holder. The fibre can either be placed parallel or perpendicular to the table, to enable edge or surface coupling respectively. The former can be used after the integration process and singulation of the wafer into single chips. Depending on the structure different fibre types can be used, if not mentioned otherwise a lensed SMF with an anti-reflection (AR) coating and a spot size of 2.5 μm is used. The optical input and output are interchangeable. Electrical signals are provided with probe needles or with specific probe assemblies.

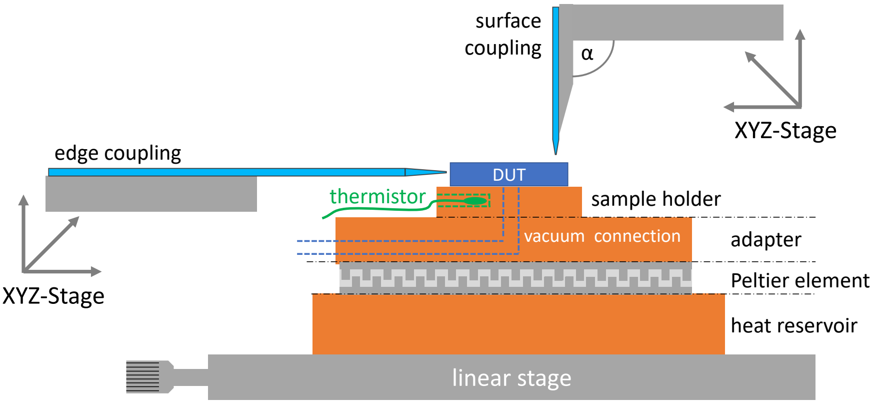

Figure 4.2: Schematic of the used characterization setup

This setup is used to characterize the different optical components before and after the integration process. The results will be presented in this chapter, which is divided in sections on passive and active optical components.

4.1 Passive Structures

In this section the results of the basic passive BB characterizations are presented, starting with the waveguide structure and the vertical mirror. The structures are measured before and after the integration process to analyse the impact of the developed technology. Different designs are explored and analysis techniques are explained.

4.1.1 Waveguide

The HHI foundry platform defines three different waveguide structures: E200, E600 and E1700. Schematic cross sections of the different types are shown in 4.3. The number after the "E" gives an indication for the etch depth used (in nanometres). The E200 waveguide is therefore a shallow etch structure with an etch depth of only 200 nm, while the E1700 is a deep etched waveguide with a mesa of 1700 nm high. These particular two types are the only ones used in this work. In the following text the E200 structure will be referred to as "shallow etched waveguide", and the E1700 one as "deep etched waveguide". Each structure has its specific application. The deep etched waveguide has a strong lateral mode confinement due to the high refractive index contrast between the waveguide material (Q1.06) and the surrounding air. This enables waveguide bends with radii as small as 150 μm. However, the overlap of the optical mode with the sidewalls for this structure is large. Imperfections during the waveguide definition process result in sidewall roughness, which leads to higher transmission loss. The shallow etch waveguide on the other hand has a small interaction of the mode with the sidewalls and the weak lateral confinement translates into an overall wider optical mode profile. The waveguide loss is low for this type. Bending of the shallow etched waveguide is not possible with reasonable bend radii (smaller than 2 mm), due to the limited confinement.

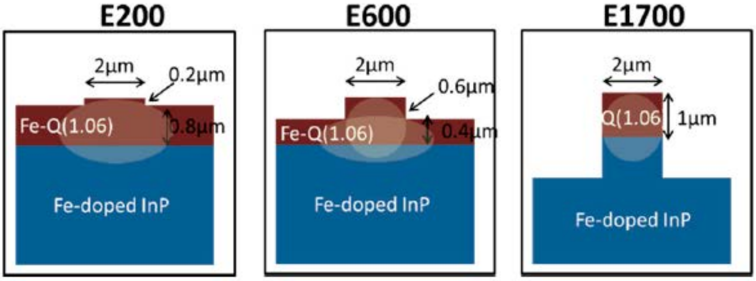

Figure 4.3: Schematic cross section of the three different HHI waveguide structures, picture from [19]

Waveguides are used in all following designs and form the basis for further analysis. It is important to determine the propagation loss α, as it gives an indication for the process quality. This can be done by measuring a series of waveguide structures with varying length. Hereby the vertical mirror BB is used to couple light from the chip into the fibre, and vice versa. This surface coupler enables coupling light downwards through the InP membrane, or upwards, depending on the orientation of this BB and the connected waveguide. In figure 4.1 the schematic of a vertical mirror is presented. A single etch creates two facets. The light through the left waveguide is reflected upwards and through the right one downwards. When the photonic design was submitted only one mirror orientation for each coupling direction has been offered. Thus in case of connecting a straight waveguide section with two couplers a bend of 180 ° is needed to orientate both vertical mirror BBs in the same direction. This bend can be either added at one end of the waveguide, or split in two 90 ° bends, each used at one end of the waveguide. The second approach has been chosen here to create structures for length dependent measurements with a small footprint.

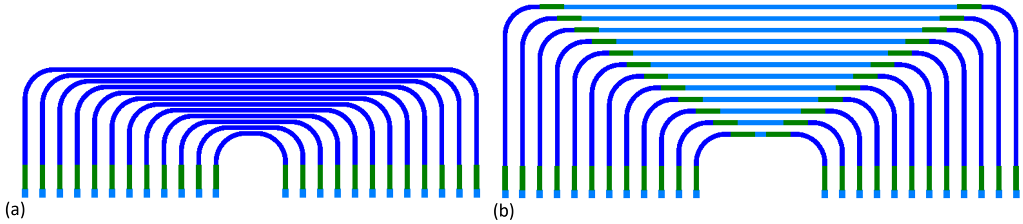

Figure 4.4: Design for length dependent loss measurement for deep (left) and shallow etched waveguides (right)

The designs are presented in figure 4.4. The left picture shows the structure used for characterising the deep etched waveguides and the right one is used for the shallow etched ones. For the characterization a tunable laser is used which sweeps the wavelength from 1510 nm to 1610 nm. The laser output power is set to 10 mW. Figure 4.5 shows an example of a transmitted signal. Due to reflections a Fabry-Perot (FP) cavity is formed. This occurs as the light is partly reflected at the transition interface of InP and air (see grey arrow in figure 4.1). In figure 4.6 a small range of the measured spectrum is enlarged and the FP fringes can be distinguished. Based on their spacing and the group index n_g it is possible to calculate the cavity length according to $L = \frac{\lambda^2}{2n_g\Delta\lambda}$ [48]. The calculated value of 1745 μm equals the distance between the two mirrors for this particular measurement. The envelope of the received optical power in figure 4.5 shows no significant wavelength dependence. Therefore it can be concluded that the used BBs (vertical mirror, waveguide transition (WGT) section and waveguide) are operational for a broad wavelength range.

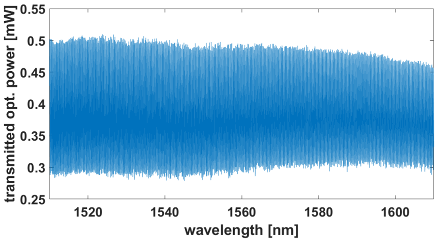

Figure 4.5: Measured transmission for a deep etched structure, before integration

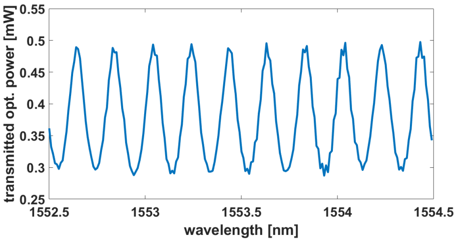

Figure 4.6: Small range of the measured optical power transmission shown in fig. 4.5

To determine the waveguide loss two methods have been used. Both are based on measuring multiple waveguides series (see figure 4.4). In the following the different analysis methods are described:

First method:
This analysis is based on the overall length dependent transmission. The structures presented in figure 4.4 show two loss contributions: a fixed part, identical for each structure, resulting form the insertion loss of the vertical mirrors and the WGT section, and a variable part, resulting from the different waveguide lengths. For the deep etched waveguide structure the variable loss contribution is purely based on one waveguide type. For the shallow etched test structure presented in figure 4.4 (b) this is not the case. Based on the properties of the vertical mirror BB two bends of 90 ° have to be used to connect the input and output side. Therefore deep etched waveguide sections are required. If these would have the same length for each structure they would be part of the fixed loss contribution. However, to keep all vertical mirrors on one horizontal line, which simplifies the measurement procedure, the deep etched waveguide section is increased systematically and adds to the variable propagation loss instead. To exclude this contribution the measured transmission is corrected by subtracting the variable deep etched waveguide loss for each measurement.
Plotting the transmission as a function of waveguide length results in the plots presented in figures 4.7 and 4.8, presenting the results before the integration process for the deep and shallow etched structures respectively. The different series refer to different locations on the wafer.

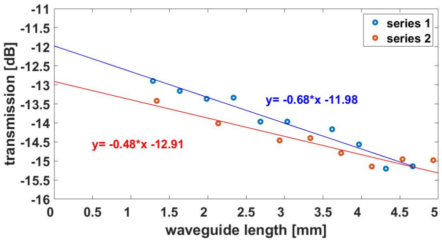

Figure 4.7: Measured transmission for deep etched waveguides, before integration

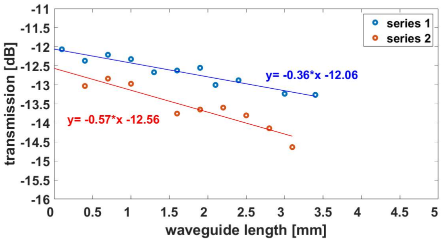

Figure 4.8: Measured transmission for shallow etched waveguides, before integration

By performing a linear regression the propagation loss α can be determined directly from the slope in dB/cm. The value at the crossing point with the y-axis comprises all constant loss contributions. For the deep etched waveguides the measured propagation loss is 4.8±0.5 dB/cm for the first series and 6.8±0.5 dB/cm for the second one. The waveguide loss is expected to be 1.5-2 dB/cm according to [19]. The fitted values exceed the specification by more than a factor of two. The error of this method depends on the coupling accuracy and stability. Depending on the angle of the vertical mirror, which can deviate from the target value of 45 °, the orientation of the fibre with respect to the surface has to be adapted for optimal coupling. Its orientation within one measurement series is constant, but may vary between measurements, as they are performed on different days and wafer locations. Based on the experimental experience is the coupling accuracy is estimated to be ±0.5 dB per coupler.
Figure 4.8 shows the result for the linear regression for the shallow etched waveguide structures. The values for the two measurement series are 3.6±0.4 dB/cm and 5.7±0.8 dB/cm. The uncertainty of the subtracted deep etched waveguide section, calculated with 5.8 dB/cm, has to be added, making the result of this design and measurement doubtful. Nevertheless, a tendency of smaller waveguide loss values can be seen. As mentioned earlier this can be expected.

The value at the crossing point with the y-axis for the different measurements shown in figure 4.7 and 4.8 is similar, which should be as the fixed part of the structures are nearly identical. The constant loss value for the deep etched test structures includes two times the vertical mirror insertion loss and two WGT sections, while the shallow etched structures have 4 WGT sections. In section 4.1.2 the loss per WGT will be determined to be 0.13 dB. Subtracting this accordingly results in 12.0±0.5 dB insertion loss per structure, which translates to 6.0±0.3 dB per vertical coupler.

Second method:
The first approach has the disadvantage of being sensitive to the fibre to chip coupling stability. The presented method here uses the FP fringes visible in figure 4.6 to decouple the waveguide propagation loss measurement from the fibre coupling. It is inspired by a method described in [49]. The FP fringes can be defined by [49, 50]:

$$\frac{I_t}{I_i} = \frac{(1-R)^2 G}{(1-GR)^2 + 4GR \cdot \sin^2(\Phi/2)} \tag{4.1}$$

where I_t is the transmitted optical power, I_i is the optical input power, R is the reflectivity of the mirrors, $G = e^{-\alpha L}$ is the total optical loss, depending on the cavity length L, and Φ is the phase delay. It is defined as:

$$\Phi = 2kL = \frac{4\pi n_{\text{eff}} L}{\lambda}$$

where k is the wavenumber and n_{eff} is the effective refractive index. Equation 4.1 holds when both mirrors have the same reflectivity. The ratio I_t/I_i is maximal for Φ equal 0 and minimal if for Φ equal π respectively. In the following the ratio of maxima and minima is named "y". It is defined as:

$$y = \left(\frac{1+GR}{1-GR}\right)^2$$

By transposing the relation:

$$G = e^{-\alpha L} = \left(\frac{1}{R}\frac{\sqrt{y}-1}{\sqrt{y}+1}\right)$$

Equation 4.2 can be obtained.

$$\ln(GR) = \ln\left(\frac{\sqrt{y}-1}{\sqrt{y}+1}\right) = -\alpha L + \ln(R) \tag{4.2}$$

By plotting the logarithmic term for different waveguide lengths, this linear relation can be used to determine α and R from the slope and the crossing with the y-axis respectively. The advantage is that the reflectivity can be determined with this method as well. An initial guess can be made due to the refractive index contrast between the waveguide material Q(1.06) and air. This results is a reflectivity of 28.1 %. However, an anti reflection coating based on SiN_x has been added by the foundry to reduce this value and makes it therefore difficult to predict the actual reflectivity. Furthermore, R is an effective reflection here, since its value includes the fixed losses in the structures as well.

For the analysis identical test structures and measurements have been used. In figure 4.9 the extracted value ln(GR) is plotted as a function of waveguide length.

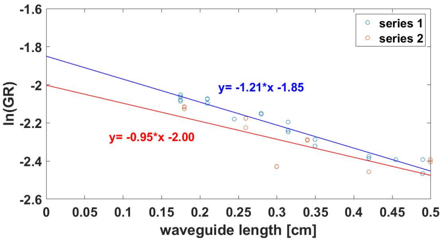

Figure 4.9: Measured ln(GR) as function of length for the deep etched waveguide structures

By performing a linear regression the waveguide propagation loss can be determined from the slope. It has been measured to be 1.2±0.1 cm^{-1} and 0.9±0.2 cm^{-1} which translates to 5.2±0.4 dB/cm and 3.9±0.8 dB/cm respectively. These values are in general smaller than the ones obtained with the first method, however they show the same tendency. Also the error margins are comparable, making both methods equally favourable to determine the waveguide propagation loss. However, the advantage of this analysis is the possibility to calculate the effective reflection. The measured values are 15.7±0.3 % and 13.5±0.3 %. The difference between them probably results from variations of the dielectrics layer, which is used as anti reflection coating, as both structures are measured at different wafer positions.

After the integration process:

To evaluate the integration technology, it is important to compare the device performances before and after the integration. As mentioned before the vertical mirror BB enables this functionality. The designs presented in figure 4.4 have also been realized with backside couplers, useable after bonding. As mentioned in chapter 3 the backside vertical mirror BB makes use of a metal marker structure to find the coupling position. However, process adaptations compromised the initial design so that the mirror BB is partly covered with the metal marker.

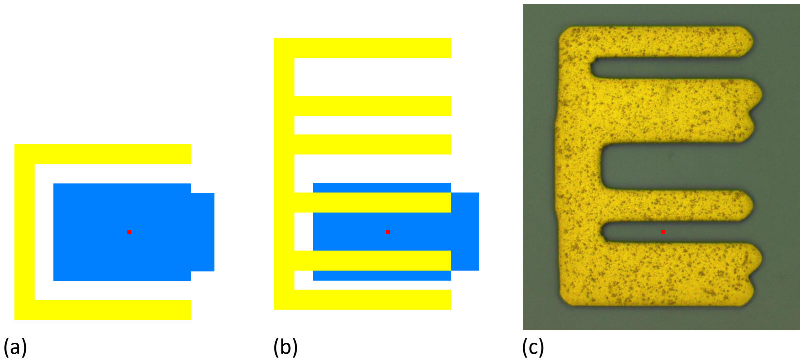

Figure 4.10: Vertical backside mirror and marker design as initially intended, the BB dimensions of the vertical mirror are blue and the metal marker is yellow (a), adapted towards process variations (b) and a picture of the realized structure (c)

In figure 4.10 (a) the original design is shown. The vertical mirror BB, blue, is enclosed by the metal marker (yellow). The actual mirror is 2-by-2 μm wide and indicated with a red dot in the centre of the BB. The latter is 42 μm high and 70 μm wide. In figure 4.10 (b) the design resulting from the necessary process adaptation is presented. While the metal structures overlap with the BB, this design should still provide a gap between the actual etched mirror and the metal, of 9 μm in each direction. Figure 4.10 (c) shows the fabricated structure. The metal tracks widened, which leads to a reduced distance towards the etched mirror structures in the centre. The vertical spacing is reduced to round 11 μm, that leaves a 4.5 μm gap from the etched mirror (2 μm wide) towards each side, assuming that it is in the centre. Metal has a strong interaction with light, therefore it is important that there is sufficient distance. A measurement result for one waveguide transmission is presented in figure 4.11. By comparing this results with the before bonding case it can be noticed that the difference between minimum and maximum of the FP fringes is reduced, while the envelope of the signal shows a wavelength dependency. This transmission is representative for all measured lengths. The maximum transmission value for each measurement is plotted. The result is shown in figure 4.12. By performing a linear regression the waveguide loss α is determined to be 4.4± 0.4 dB/cm and the mirror insertion loss is 8.1±0.1 dB per coupler.

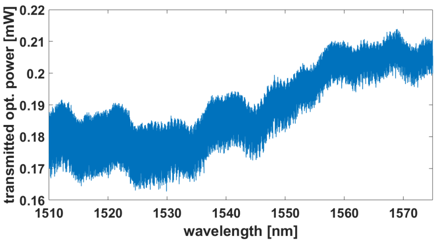

Figure 4.11: Measured transmission for a deep etched structure, after integration

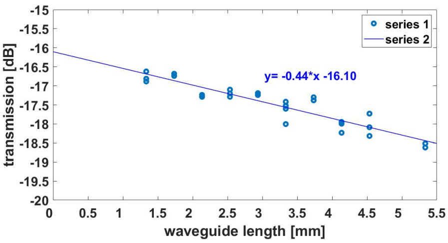

Figure 4.12: Measured propagation loss for deep etched structure, after integration

The waveguide loss is smaller than the initial results obtained before the integration process by the same method. This can be explained by the variations over the wafer surface, which have been indicated before. Another aspect is the difference in material contrast. At the beginning of the integration process the waveguide structures are surrounded by air, while at the end they are embedded in BCB. The refractive index contrast between the waveguide and the surrounding material is now smaller, which reduces scattering effects at the sidewall and can therefore reduce the overall waveguide propagation loss [51]. The insertion loss for the vertical coupler is larger, which can not be explained by fabrication tolerance. However, as mentioned before, the metal structures are in close proximity to the etched mirrors and therefore might influence the coupling efficiency and/or the insertion loss. Additionally, the angle of the mirror facet might not be 45 °: a deviation would influence both coupler types, but the light coupled into the wafer after the integration process passes through the full photonic membrane, experiencing several materials with different refractive indices. The backside has no anti reflection coating, which means that the reflectivity might increase to 28 % (based on refractive index contrast), adding roughly 0.6 dB per coupler. However, due to the metal marker a fair comparison between the two vertical mirror couplers is not possible. The fact that the waveguide propagation loss is stable, even slightly improved, provides a good basis for further investigation of the technological influence on BB performance.

In this section the properties of the waveguides and vertical mirrors have been measured before and after bonding. The results have been presented and show that the waveguide propagation loss value is worse compared to the foundry specification. The integration process has shown limited influence of the waveguide structures. However, the vertical mirror building block shows strong changes in behaviour, which can be explained by the unwanted gold coverage and the missing anti reflection coating on the backside of the wafer. In the following section the WGT will be analysed.

4.1.2 Waveguide transition section (WGT)

The vertical mirror BB is based on a shallow etched waveguide. However, to connect two of these mirrors with each other a bend of 180 ° is needed. Bends can only be realized using deep etched waveguide structures. To couple the two differently etched waveguides with each other transition sections are needed to transform the mode at one into that of the other and thereby reduce reflections and coupling loss. This fundamental BB is used in most designs. To quantify the loss of this device test structures are made, which include a series of them; with respectively 2, 4, 8 and 16 elements.

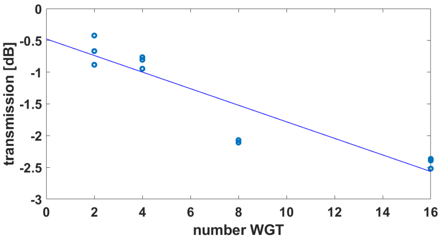

Figure 4.13: Measured transmission for an increasing number of waveguide transitions, before integration

Figure 4.13 presents the transmission measurements. The loss per WGT is determined to be 0.13±0.02 dB. An influence from the integration process on the WGT BB has not been seen. In the following section the multi mode interferometer (MMI) BB will be characterized. It can be used to measure the same components before and after the integration process, by combining upward and downward vertical mirrors with the same device.

4.1.3 Multi mode interferometer (MMI)

Splitting a guided wave into two or more separate ones is a necessary functionality required for most complex designs. MMI couplers are used for this, based on their good fabrication tolerance, bandwidth and polarization independence [52–54]. Several different types are offered by the foundry. To limit the amount of different BBs only a deep etched 1x2 MMI with a 50:50 splitting ratio is selected for use in the circuits designed in this work.

The MMI is used to enable measurements of a structure before and after the integration process. Therefore the 2 ports of the MMI are connected to two vertical mirrors, one for coupling upwards and one for the downwards direction. The single port is connected to the DUT. For experiments that require transmission trough the test structure this composite building block (CBB), the MMI and combined mirrors, can be used at both sides.

In figure 4.14 a design example is given. It consist of the vertical mirrors (light blue), the WGT (green) and the MMI (orange). The components are connected using deep etched waveguides to enable the 180 ° bends.

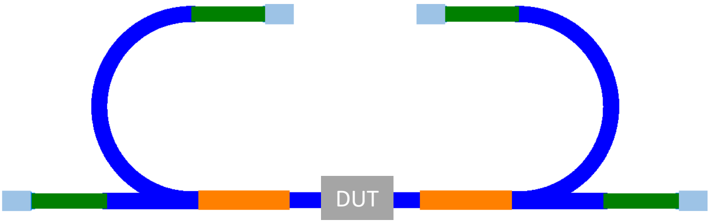

Figure 4.14: Design based on 1x2 MMIs to enable the measurement of a DUT before and after the integration process

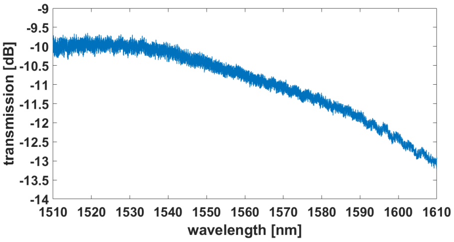

Figure 4.15: Measured transmission for the design presented in figure 4.14, before integration

The measured transmission through such a structure before the integration process, where the DUT is a short deep etched waveguide section, is presented in figure 4.15. It can be seen, that longer wavelengths lead to higher loss. This effect results from the MMI itself, as all other BBs in the circuit have been proven to operate in a broad wavelength range. For this plot the mirror losses are already subtracted, leaving only the loss of the two MMIs. Several structures have been measured to determine the MMI induced loss. At a wavelength of 1550 nm the loss is 5.0±0.2 dB. Thereby 3 dB is due to the designed 50:50 splitting ratio. So, although this structure enables the characterization of different BB before and after the integration process, it also introduces additional loss.

4.1.4 Arrayed waveguide gratting (AWG)

The passive BBs presented so far work over a large wavelength range. In data and telecommunication a basic technique to increase the bandwidth of a fibre is the use of multiple wavelength channels to transmit independent data streams. To enable this application a component is needed that combines the separate streams into one output, or vice versa, that can split the incoming light into the different channels. These components are called multiplexer and de-multiplexer, respectively. The application based on this approach is wavelength devision multiplexing (WDM).

One of the most important BB that is used as a multiplexer and de-multiplexer for InP is the AWG [55]. It has been reported first by M. Smit in 1988 [57,58].

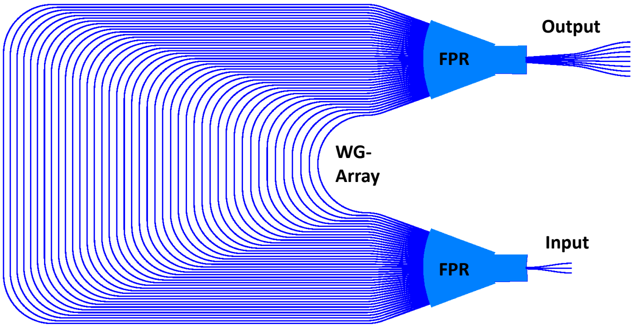

Figure 4.16: 3x8-AWG design based on the the HHI foundry platform

In figure 4.16 an example of such an AWG is shown. It consists of the following elements: one or more input waveguides, an input free propagation region (FPR), a waveguide array, an output FPR and output waveguides. The presented structures has 3 input and 8 output waveguides. The working principle is explained in [55]:

The light entering the first FPR diverges and couples into the separate waveguides of the adjoining array. These waveguides are designed with different optical path lengths, the difference being equal to an integer multiple of the central AWG wavelength λ_c. The light from the different waveguides converge again in the second FPR. For λ_c the conversion in the second FPR is exactly inverting the divergence of the first one. To spatial separate the wavelengths into different output ports the arrayed waveguide lengths increase linearly, which introduces a wavelength dependent phase shift in the waveguides, and thus a varying tilt at the output of the array, leading to a different focal point for each wavelength in the output plane of the FPR. With an AWG it is therefore possible to separate the light into different wavelength channels, or vice versa, to combine them, as the BB can be used bidirectional.

An AWG is a complex passive BB that requires a relatively large area. As mentioned in chapter 3 the InP membrane will be stretched after bonding and the waveguides will be sealed with BCB. Both these effects might have an influence on the AWG performance. To analyse if there is indeed such an effect an AWG design has been created using commercially available design software[1]. The resulting design is presented in figure 4.16. The channel spacing is designed to be 0.8 nm (100 GHz), with λ_c equal 1550 nm (193.1 THz). The free spectral range (FSR) of the structures is 8 times the channel spacing, resulting in 6.4 nm. The second order FSR follows the first one without gap, resulting in a so called cyclic AWG structure.

In figure 4.17 the design circuit to test the AWG is presented. Each input and output is connected with a WGT section and a vertical mirror. There are two designs, each including only one type of surface couplers (either up or down). The MMI based CBB has not been used as the additional loss made the characterization difficult.

Two AWGs are included on the wafer and have been measured before the integration process: one located in the centre of the wafer, the other close to the edge. The results are presented in figures 4.18 and 4.19, respectively. Both show the targeted channel spacing of 0.8 nm. The first and last channel of one FSR order are dark blue. Comparing the two AWGs the FSR is shifted

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[1] Bright Photonics; brightphotonics.eu

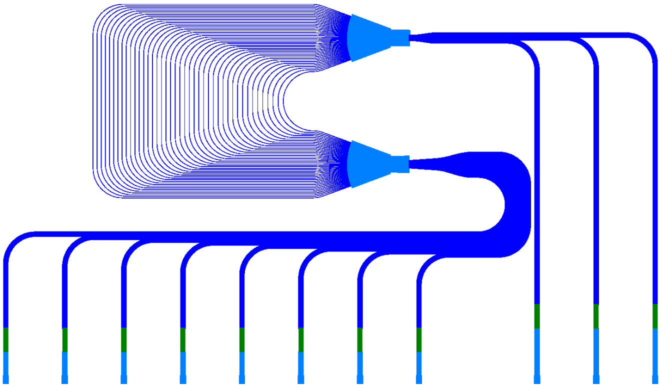


Figure 4.17: 3x8-AWG design connected with vertical mirror for characterisation

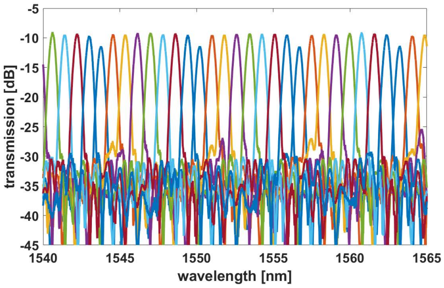


Figure 4.18: Measured transmission for an AWG located at the centre of the wafer

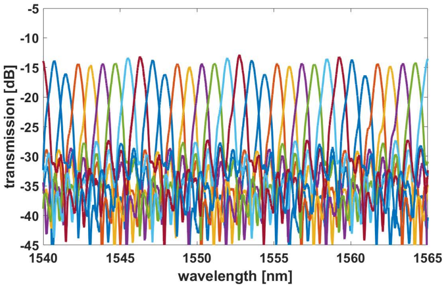


Figure 4.19: Measured transmission for an AWG located at the edge of the wafer

by 2.3 nm, visible by tracking the two dark blue channels. The transmission is corrected for the vertical mirror coupler loss, but not for the extra waveguide length. All measurements have been performed using the central waveguide input. The AWG induced loss varies, depending on the measured channel, between 9 to 11.5 dB and 13 to 16.4 dB respectively. The crosstalk, defined as the difference between the minimum transmission and the highest side channel signal is 14.1 dB (centre device) and 10.9 dB (edge device). The two structures differ due to their wafer position and therefore process related non-uniformities. The relatively high insertion loss is explained by the generally high waveguide loss, which has been measured before (see section 4.1.1) possibly resulting from sidewall roughness. This effect is stronger at the edges of the wafer. The crosstalk at the edge of the wafer is larger than in the centre this is cause by face noise resulting from critical dimension variation.

While measuring the AWGs a polarization manipulator has been used to optimize the state of polarisation (SOP). It consists of three coils in the optical input fibre. These three elements form a sequence. Each coil induces birefringence in the fibre, thereby mimicking a series of retardation plates. With this device the polarisation state of the incoming light has been varied to determine the impact on the transmission. In figure 4.20 the result of this experiment is shown. It shows multiple measurements of a single channel using different polarization states of the incoming light. Two peaks can be identified, representing the two orthogonal

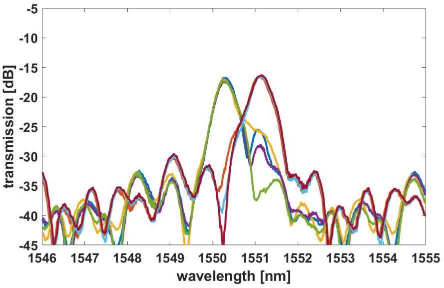


Figure 4.20: Measured transmission for an AWG located at the edge of the wafer using different input polarizations

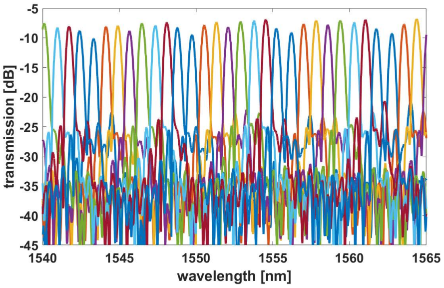


Figure 4.21: Measured transmission for an AWG after the integration process

polarizations. Additionally hybrid states are visible, containing fractions of both polarizations. It can be seen that there is a polarization dispersion of 1 nm. This qualitative analysis shows the importance of the polarization control to avoid high nearest neighbour crosstalk on the wavelength channels. For all AWG related measurements the polarization state of the incoming light has been tuned to result in maximum transmission for the SOP with the peak at the longest wavelength.

This component is used to analyse the impact of the integration technology. In figure 4.21 the resulting transmission for a fully integrated AWG is presented. The signal is corrected for the insertion loss of the back side vertical mirrors. Comparing the results with the initial topside measurements a clear agreement can be seen with the spectra presented in figure 4.18. The same colour scheme has been used and shows a nearly identical positioning and spacing. As these devices are characterized after the modules have been made it is not possible to identify where this structure has been originally located on the wafer, but this good match suggests that this structure is originally from the centre. The FSR width changed from 6.4 nm to 5.5 nm, showing a smaller channel spacing, however the distance between two grating orders is the same. The smaller channel spacing results from the thermal expansion of the InP membrane, changing the optical path length variations in the arrayed waveguide section, thus resulting in a shift in the focal plane of the FPR. This thermal expansion can be compensated in the design.

4.2 Active Structures

The technology developed in this work targets the integration of photonic and electronic ICs. As a demonstration transmitter and receiver circuits will be realised. The characterization of the active components used in these circuits will be reported within this section. In the transmitter a DFB laser and an EAM are used. The receiver circuit is based on a high speed PIN PD. Just as with the passive components, also the active devices should be analysed before and after the integration process, in order to determine possible performance changes. However, as active components require electrical probing, the measurements before the integration process are limited to a minimum, because the mechanical contact force implies a mayor risk to break the fragile InP wafer. Therefore only spring loaded probe needles are used to measure a limited amount of devices, to reduce this risk. This means that high speed characterization of the devices is not possible. Furthermore, emitting, detecting and modulating light is based on optoelectronic effects that generate heat. After the integration process the InP substrate is removed and thus the membrane lacks an important heat reservoir. It is expected that the temperature within the active devices increases in the membrane, which will have the strongest effect on the DFB laser structures. Also other possible effects of the integration technology will have their major influences on these delicate devices. Therefore the comparison of devices before and after the integration process will mostly concentrate on the DFB lasers.

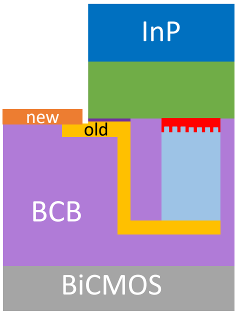


Figure 4.22: Schematic cross section of the new photonic contacts at the end of the integration process

To enable the characterization of the different active BBs after bonding, without endangering the actual structure, only a fraction of the contact pads, created by the foundry, is opened. These pads will be connected to a new larger metal contact pad. This pad is created on the BCB layer and will be used for the actual probing. A schematic of this structure is presented in figure 4.22.

In this section the properties and performance of the different active components will be described. For the photodiode and the EAM high frequency measurements are performed to indicate potential data transmission rates.

4.2.1 Photodiode

The Fraunhofer PDK offers two types of PDs, one optimized for high frequency response and the other for monitoring functions. It is not known what is inside the different BBs and how they differ in terms of layer stack and fabrication. However, the high speed PD is equipped with a ground-signal-ground (GSG) probe pad configuration, while the monitor PD has simple p- and n- contacts. This results in a footprint difference of the two structures. The monitor PDs are used to track optical power or temperature, by measuring the photo or dark current respectively. However, due to necessary process adaptations during the first hybrid module realization, the p- and n- contacts of each monitor PD are electrically connected and thus short circuit the actual BB. The reason is a process induced shift between the two wafers which is in detail explained in section 3.6.2. In figure 4.23 (a) the originally intended design is shown, figure 4.23 (b) presents the resulting design, after the process adaptation complemented. A microscope picture of the realized device is given in figure 4.23 (c). The contacts of the high speed PIN PDs are not short circuited, but the metal contact pad is widened (see figure 4.24 (a) for the original design and (b) for a microscope picture of the fabricated structure, including the adaptation of the metal layers).

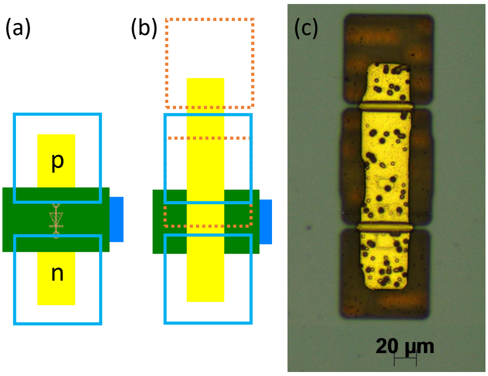


Figure 4.23: Original design of the monitor PD metallisation with InP membrane openings (blue frames) (a), adapted version of the first hybrid module realization including shifted InP membrane openings (orange frames) (b), microscope picture (c)

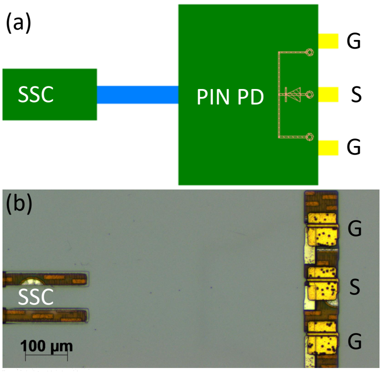


Figure 4.24: Adapted design of the high speed PIN PD metallisation (a), microscope picture of the first module realization (b)

This larger area has an influence on the contact capacitance, and therefore on the frequency response of the device. This will be explained in more detail when discussing the small signal response measurements. Furthermore the gap between the different pads is reduced, which could result in an enhanced electrical leakage path and a higher capacitance.

The first property of the PIN PDs that has been characterized is the responsivity. The foundry specifies this value to be better than 0.8 A/W. The structures are only measured after the integration process, which enables two coupling schemes, using either the backside mirror or the SSC. The latter was introduced in section 2.1 and is used to improve the edge coupling of the chip with an optical fibre. In section 3.4 it is explained that the height of the SSC deviates, due to additional material removal, which will result in reduced coupling efficiency. To characterize the insertion loss of this edge coupler the PD responsivity measurements have been used. This can be done by comparing the results determined using backside mirror with the ones measured using the SSC.

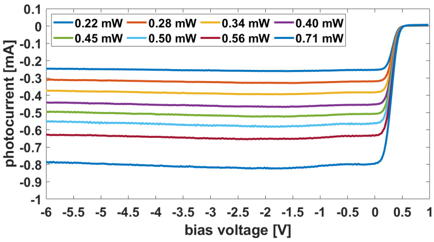


Figure 4.25: Measured high speed PIN PD photocurrent for different bias voltages and optical input power (vertical mirror)

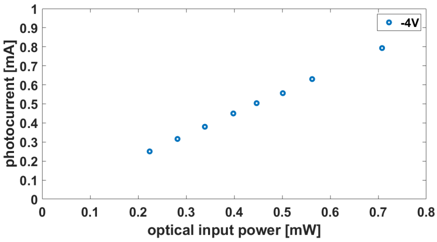


Figure 4.26: Measured high speed PIN PD photocurrent for different optical input powers at a bias voltage of -4 V

In figure 4.25 a series of photocurrent measurements, using the vertical mirror BB, for different reversed voltages is presented. The optical input power varies for the individual curves. The power is controlled directly with the external laser module. The given values are corrected for the insertion loss added by the used BBs (vertical mirror 8 dB, MMI 5 dB). Each of these components adds an measurement error, which has an influences on the determined value. The measured curves in figure 4.25 show all the same general behaviour.

The photocurrent increases for higher optical input power values. In figure 4.26 the measured currents for the different optical input powers are plotted for a fixed bias voltage of -4 V. From the linear increase of photocurrent vs optical input power it can be seen that the PD is not reaching saturation. The responsivity is the slope of this linear relation. It is measured to be 1.12±0.01 A/W. The small error is the result of an improved fibre coupling procedure. The measurement is performed using one optical fibre only, which reduces the overall misalignment error as compared to the measurements on the passive devices in section 4.1, which need both input and output coupling. The optimization of the coupling is additionally simplified as the photocurrent can be monitored directly and functions as coupling quality indication. Therefore it can be assumed that the overall coupling accuracy for these measurements is improved with respect to those in section 4.1. However, as mentioned before, the error on the incorporated insertion loss of the other involved BB has an impact on the measurement accuracy. For example: in case of a lower insertion loss than 8 dB for the vertical mirror the responsivity would be reduced. If the insertion loss would be 1 dB smaller, the responsivity would be 0.89 A/W, which would still fulfil the foundry specification. This clearly points towards the importance of the different loss terms.

Further measurements have been performed using the edge coupling scheme. Therefore the SSC BB had to be characterized first. The mode field diameter of the SSC is unknown. Both a standard SMF and a lensed SMF, with spot sizes of 10 μm and 2.5 μm respectively, have been used. The optical input power is set to 10 mW. The measured photocurrent varies only slightly, therefore the coupling loss must be similar for the two fibre types, indicating that the spot size of the SSC must be around 5 μm. In table 4.1 the results are summarized.

	photocurrent [mA]	insertion loss [dB]
SMF	2.7±0.1	6.2±0.2
lensed SMF	2.8±0.1	6.0±0.2

Table 4.1: Calculated insertion loss for the SSC depending on the used fibre type

The loss might be influenced by the actual facet design. As mentioned in the paragraph back-end process of section 2.5 the semiconductor facets are covered with BCB as a result of the wafer dicing approach. In figure 4.27 (a) a schematic cross section of the SSC is shown. The waveguide is lateral tapered, so that the mode expands into the diluted waveguide section. At the left side of this schematic the chip facet is illustrated. The interface (at the top of the schematic) is defined by the remaining BCB. The actual InP facet is laterally separated from the BCB/air interface. This distance is in the order of a few micrometer. In figure 4.27 (b) a top view microscope picture of a SSC is presented and in (c) the corresponding facet can be seen. The spot size converter is in the centre of the two trenches. These have been etched by HHI through the InP membrane. The remaining InP mesa in the centre has a with of 50 μm. The actual BB is only 10 μm. In all the pictures the position of the fibre mode is specified by a light blue arrow and in case of figure (c) by a circular shape. The latter indicates the optical mode of the diluted waveguide and its estimated size.

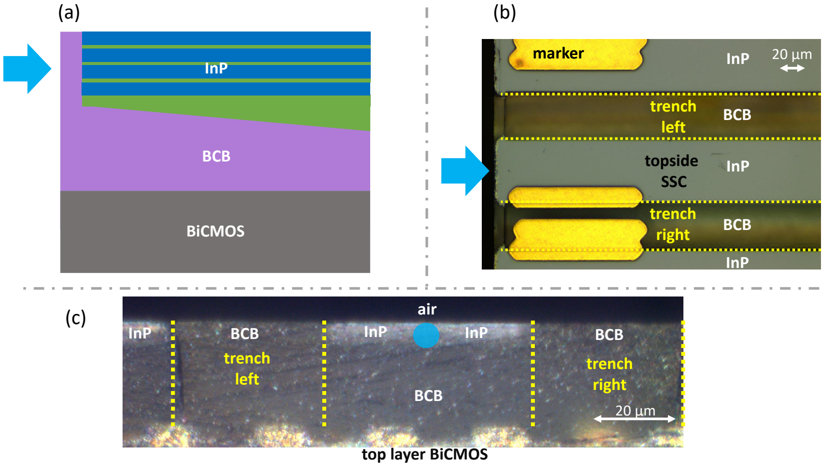


Figure 4.27: (a) schematic cross section of the bonded SSC, (b) top view microscope picture of the integrated SSC, (c) microscope picture of the SSC facet, the blue dot and arrow indicate the position of the fibre mode

The BCB layer during sawing captures debris, which is visible as speckles in figure 4.27 (c). It can also be seen that a certain degree on roughness (also due to sawing) exists. Both aspects reduce the coupling into the diluted InP waveguide, which implies additional coupling loss. However, taking into account that this is a first time realization, without optimization of the sawing process, the achieved coupling loss is promising enough to further investigate this approach. One possibility is complete BCB removal in front of the InP facet. This would eliminate the impact of the debris and roughness completely. However, this can not be achieved with a wet etch process as this would also remove the bonding layer and therefore destroy the complete hybrid module. As an alternative a dry etch process can be used with requires advanced masking techniques to protect the InP membrane and facet from the physical bombardment used for removing such a thick polymer layer. Also polishing the BCB could be further explored, by removing the debris and roughness a residual of the BCB could remain. As the coupling efficiency is slightly higher for the lensed SMF all subsequent measurements with SSCs will be performed with this type of fibre.

Dark current

In figure 4.28 the measured dark current for several PDs is presented. These are much higher than expected. For a bias voltage of -4 V the dark current is measured to be 2.3±0.5 μA, while a value smaller than 10 nA is specified by the foundry. An explanation might be the demanded fabrication changes. It has been requested to deliver the wafer without the usual polymer planarisation, to avoid the presence of in-captured gasses (see section 3.1). This polymer could act as a passivation layer, which is missing for the received structures and therefore result in reduced performance. Unfortunately, these structures have not been measured before the integration process started, otherwise a comparison would have been possible. However, the same structure has been measured on a similar wafer, originated from this the same process batch, for comparison. This wafer has been stored as delivered for one year before the measurement has been performed. For a bias voltage of -0.5 V a dark current of 3 mA has been

measured, being a factor 1000 larger then the processed sample, indicating poor device quality or a dramatic degradation over time due to the missing passivation layer.
An alternative explanation for the processed sample is given by the created enlarged contact pads. The distance between two signal pads is reduced to a few micrometers and this could therefore form a current leakage path if the intermediate material BCB is not a perfect isolator, explaining the increased values.

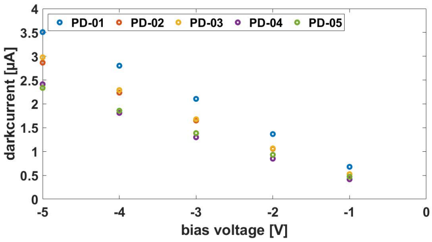


Figure 4.28: Measured voltage dependence of the dark current for different high speed PIN PDs

Next to the dark current, the responsivity and linearity of the PD, also the polarization dependency has been investigated. All structures are characterized with a the three coil based polarization controller. The difference between the minimum and maximum photocurrent is determined to be small: 0.6±0.4 dB.

Small signal response
Finally the high frequency properties of the photodiode are characterized by measuring the small signal response. A schematic of the used setup is presented in 4.29. A vector network analyser (VNA) is used with a bandwidth of 67 GHz, and an integrated lightwave component analyser (LCA). The optical output of the LCA is coupled via a lensed SMF into the chip. The electrical signal from the PD is measured with a GSG probe. A bias tee is used to apply a reverse bias voltage to the photodiode.

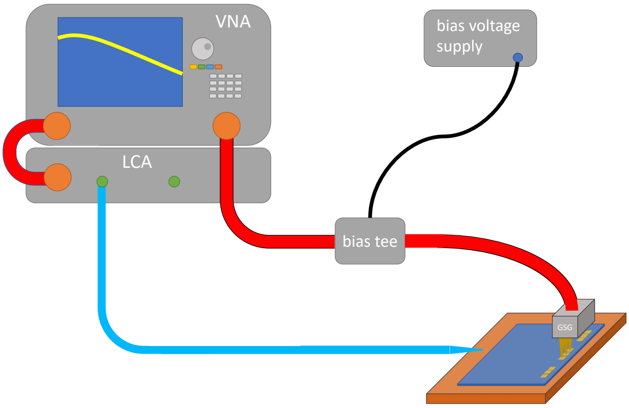


Figure 4.29: Schematic of the measurement setup used to characterise the high frequency response of the PIN PDs

The high frequency signal is analysed by the VNA. The electrical path has been de-embedded using a standard short open load (SOL) calibration substrate. The output power of the LCA is set to be 5 dBm. Due to the 6.0 dB coupling loss of the SSC the PD receives -1 dBm. The small signal modulation is set to -15 dBm. In figure 4.30 the measured S_{21} response of one photodiode is presented for different bias voltages. The horizontal line is the 3 dB level which is defined as the point where the electrical modulated signal is reduced to 50 % of the maximum value. For a bias voltage of -4 V a 3 dB frequency of 27.5 GHz is achieved. The small signal response is almost identical for bias voltages from -2 to -6 V. At round 30 GHz the spectra shows an artefact. This seems to result from reflections within the optical circuit. As mentioned before the PD is connected to a SSC. This BB has a total length of 2.5mm. It is possible that there are interfaces within this structure, which lead to reflections and therefore form a cavity. Its fundamental frequency can be calculated by $\nu = c/2nL$, where c is the speed of light, L is the length of the cavity and n is the refractive index (for InP $n = 3.17$). A frequency of 30 GHz is equal to a cavity length of round 1.6 mm. Such a cavity might be formed between the facet of the SSC and an interface within the SSC BB, for example a transition from the taper section to the standard waveguide.

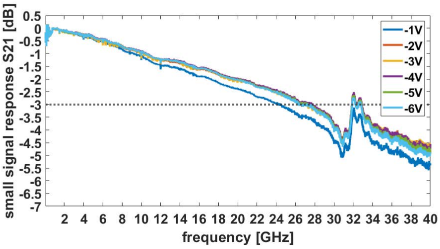


Figure 4.30: Measured small signal response of the high speed PIN PDs for different bias voltages

The 3 dB bandwidth of the PD is smaller than expected (45 GHz [19]). This result is difficult to evaluate as the device performance itself has not been characterized before the integration process. It is possible that the creation of the hybrid devices influences the performance. In particular the metallization of the PD contact pads could play a role. The original HHI BB contacts are enlarged and the distance between them is strongly reduced due to the process adaptations (see figure 4.24). Both contributions are effecting the capacitance of the device and might therefore limit the 3 dB bandwidth [59]:

$$f_{3\mathrm{dB}} = \frac{1}{2\pi RC} \tag{4.3}$$

The performance of the high speed PIN PD is characterised in this section. Some indication is found that the integration process influences the device performance, especially due to the increased contact pads, which might be reducing the 3 dB bandwidth and increasing the dark current. This effect can be avoided during a new fabrication run.

4.2.2 Distributed feedback laser (DFB)

For the success of the proposed 3D technology the laser BB is of particular importance, as it generates the largest amount of heat from all the photonic components. For the first hybrid module fabrication DFB lasers are integrated. These will be used to analyse the feasibility of the proposed technology. After receiving the foundry wafer the laser structures are first characterized.

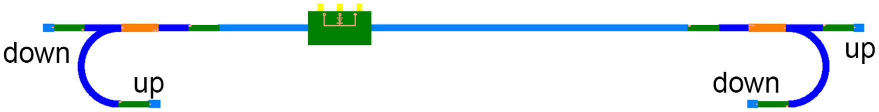


Figure 4.31: Design of the DFB laser test cell, based on vertical mirrors

Therefore the DUT configuration is used as has been introduced in section 4.1.3. The designed circuit consists of a set of two 1x2 MMIs, each connected to two vertical mirrors to enable characterization before and after the integration process. Between the two MMIs the DUT is placed. It includes the DFB laser, two shallow etched waveguides and two WGTs to connect the DFB laser with the MMIs. In figure 4.31 the corresponding circuit design is shown. A series of DFB lasers is used with different Bragg wavelengths. The shortest wavelength is 1545 nm, while the longest is 1554 nm. The spacing between the different designed Bragg wavelengths is 1 nm, resulting in 10 different structures. To reduce the risk of breaking the wafer only one series of DFBs has been characterized before bonding. In figure 4.32 the optical power (in fibre) for the different DFBs is plotted as a function of the DC drive current.

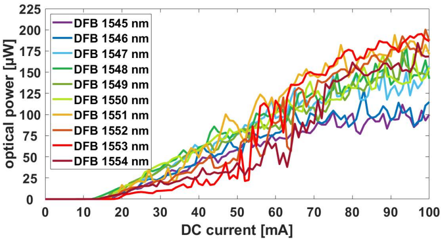


Figure 4.32: Measured optical power in fibre as a function of DC current for a set of DFBs with different designed Bragg wavelengths, before integration

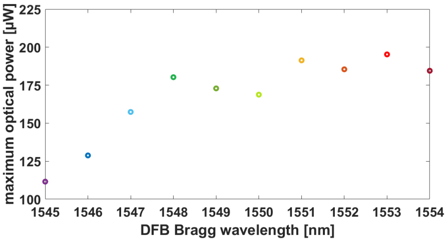


Figure 4.33: Measured maximum optical power for the DFBs laser, determined from the series presented in figure 4.32

This result is not corrected for an estimated excess loss of 14.5 dB, composed of 6 dB for the vertical mirror insertion loss, 5 dB for the MMI BB and 3.5 dB resulting form an external optical 3 dB splitter. Furthermore the laser is emitting at both facets identically, which means that the total emitted power is round 17.5 dB higher than the actually measured values. Therefore the maximum output powers is in the order of 10 mW. In figure 4.33 the measured maximum output power for the series of DFBs is presented, without loss correction. It can be seen that the power is generally increasing towards longer wavelength. By correction these values for the excess loss all devices achieve an maximum output power larger than 3 mW, which is the value specified by the foundry [19]. However, by comparing the different DFBs a variation of the optical output power of nearly 3 dB is found. Furthermore it can be observed that the LI-curves show instabilities, visible as spikes and kinks in the plot. These are not due to an unstable chip-fibre coupling, since when repeating the same measurement the spikes and kinks are reproduced.

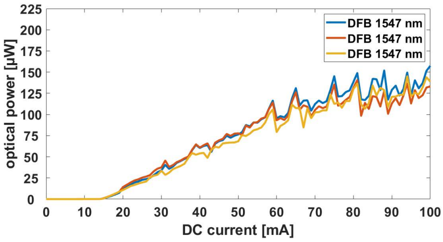
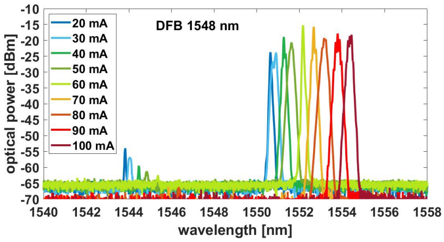


Figure 4.34: Measured optical power as a function of DC currents for a DFB with a designed Bragg wavelength of 1547 nm, before integration

In figure 4.34 an example is given where one DFB structure has been measured at 3 separate times. The similarities between the measurements show that there is an internal cause for the behaviour. To further analyse the kinks in the LI-curves an optical spectrum analyser (OSA) has been used to record optical spectra for each DFB at various DC currents. Figures 4.35 and 4.36 present the resulting plots for DFB lasers with designed Bragg wavelengths of 1548 nm and 1550 nm, respectively. The spectra are measured at current steps of 10 mA. The presented curves resemble complex coupled DFB lasers [19]. The grating stop band can clearly be seen in the spectra. DFB lasers can emit at 2 possible wavelength, either on the blue or the red side of the stop band. For structures with a designed Bragg wavelength below 1549 nm the dominant lasing mode is at the longer wavelength side of the stop band, independent of the used injection current.



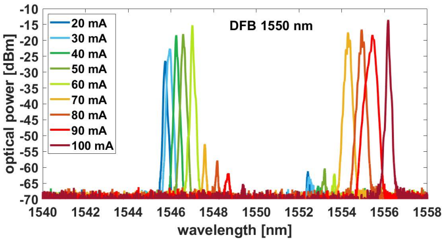


Figure 4.35: Measured optical spectra for the DFB laser with a designed Bragg wavelength of 1548 nm, before integration

Figure 4.36: Measured optical spectra for the DFB laser with a designed Bragg wavelength of 1550 nm, before integration

In figure 4.35 the spectra for the 1548 nm DFB are presented, demonstrating this behaviour. In case of a DFB laser with a designed Bragg wavelength of 1549 nm and longer the lasing mode changes, depending on the current. An example is given in figure 4.36. It can be seen that for small current values the laser operates at the short wavelength and for larger ones the longer wavelength mode is dominating. This can be explained by the temperature dependency of the gain peak. For currents below the threshold band filling is the dominant effect for the gain curve, which leads to a blue shift of its peak with current. At threshold the gain is clamped, so further band filling is stopped. By increasing the current beyond threshold Joule heating increases the internal laser temperature, resulting in a red shift of the gain curve. Evidence for this heating behaviour can be found in figure 4.35 and 4.36, where the emission peak shifts proportional to I^2. All laser structures use the same active gain material and it seems that the gain peak is within the DFB range (1545-1554 nm). Therefore DFB lasers with a Bragg grating, that have a designed wavelength smaller than the gain peak, will start lasing at the long wavelength side of the stop band, while larger bragg wavelength will lead to initial lasing at the shorter wavelength side. By increasing the current beyond the threshold the gain spectra and the Bragg grating wavelength both shift towards the red, resulting in a general shift of the emission wavelength. However, it seems that the temperature effect on the gain spectra is more dominant, leading to a red shift relatively to the Bragg wavelength. This results in a mode jump for the laser structures, which were initially lasing at the short wavelength of the stop band, as can be seen for all DFB lasers with a Bragg grating designed for 1549 nm and longer.

By analysing the spectra in figure 4.35 and 4.36 it can be seen that for some operation points the optical modes have multiple peaks, which could indicate the presence of an external cavity influencing the laser. In section 4.1.1 it has been seen that the vertical mirror BB, that is usable before the integration process, has 16 % of reflection. Therefore it is likely that a cavity between the DFB laser and the vertical mirrors is formed. Additional reflections from other components like the MMI and the second vertical mirror type (usable after the integration process) may contribute as well, making this DUT structure unfavourable for precise characterization of feedback sensitive devices like the DFB laser. It is therefore likely that the kinks in the LI characteristic of the different DFB laser result from external cavities, formed by the vertical mirrors.

After the integration process

After the integration process the DFB BB is analysed using edge coupling. The laser is connected to a SSC and a lensed SMF is used to collected the emitted light. First the DFB BB has been tested with a DC current supply, however no lasing has been detected. Therefore electrical pulse measurements are performed, to eliminate self heating effects of the laser. All pulsed measurements have been performed with a pulse frequency of 1 kHz and with a pulse width of 4 μs, if not mentioned otherwise.

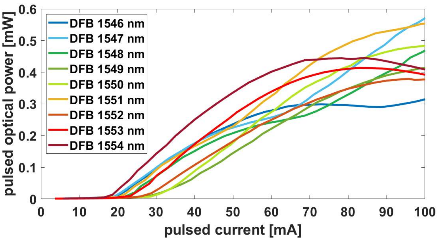


Figure 4.37: Measured optical power, pulsed, in the fibre as a function of pulsed current for a set of DFBs with different designed Bragg wavelengths, after integration

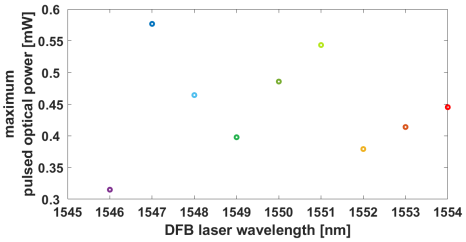


Figure 4.38: Measured maximum optical power, pulsed, for the DFBs laser determined from figure 4.37

In figure 4.37 the measurement of the pulsed optical power in the fibre for a series of DFB lasers is presented as a function of the pulsed current. The result is not corrected for the fibre coupling loss (6 dB) and only one side of the laser is coupled to the fibre. The actual laser power is therefore round 9 dB higher, resulting in 4.5 mW. This value is smaller in comparison with the values achieved before the bonding process. It indicates that the laser degraded in some way due to the integration process. Another indication for this is the increased threshold current. However, it has to be noted that the current calibration for pulsed currents smaller than 25 mA is doubtful for the used measurement equipment and may vary by ±8 mA. As mentioned before are these LI curves measured by using the SSC BB. By comparing these results with the curves presented in figure 4.32 an absence of peaks can be seen, which confirms the assumption, that the vertical mirrors formed a external cavity influencing the DFB performance. This is not the case for the circuits using SSC.

In figure 4.38 the maximum optical power for pulsed operation is plotted for the different DFB Bragg wavelengths. No tendency is detectable, but the variation is comparable to that of the laser structures measured before the integration process.

Some of the presented LI curves show a thermal roll over at higher currents. The pulses used for the characterization have a pulse width of 4 μs and a repetition frequency of 1 kHz, which translates to a duty cycle of 0.4 %. The thermal roll over is a result of poor heat sinking and an increase of the internal temperature.

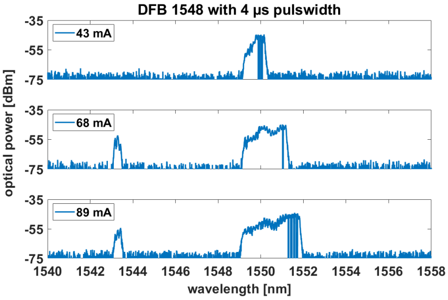


Figure 4.39: Measured optical spectra of DFB 1548 nm for different pulsed currents and a pulse width of 4 µs, after integration

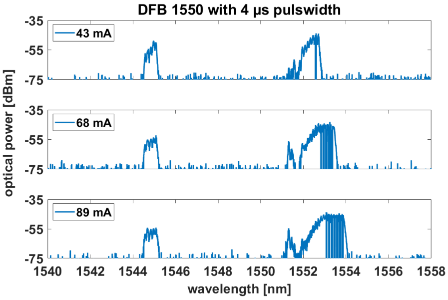


Figure 4.40: Measured optical spectra of DFB 1550 nm for different pulsed currents and a pulse width of 4 µs, after integration

As mentioned before the optical spectra can be used to analyse the thermal behaviour. Therefore a series has been measured for different pulsed currents and pulse widths. While sweeping one of these parameters the other is fixed. The optical spectra at different electrical injection currents use a pulse width of 4μs and a repetition frequency of 1 kHz. The results for the DFB lasers with the designed Bragg wavelengths of 1548 nm and 1550 nm are presented in figures 4.39 and 4.40 respectively. The stop band of both DFB laser can be clearly identified. Some of the spectra show artefacts where the optical signal drops to the noise level within the optical peak. This is based on insufficient triggering during the measurement. For the presented spectra the emission wavelength and stop band width are in agreement with the observations made before bonding. However, the modes at the sides of the stop band are wider and a broadening effect can be observed by increasing the used injection current. The measurement of the optical spectra is not time resolved, which means that the detected

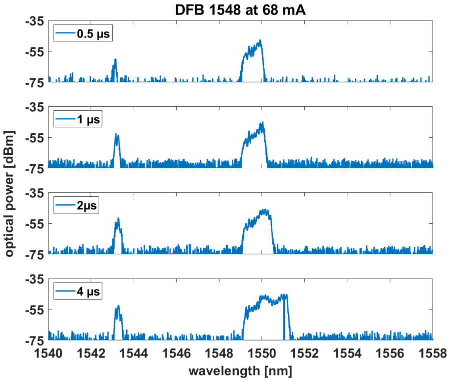


Figure 4.41: Measured optical spectra of DFB 1548 nm for different pulse widths and a current of 68 mA, after integration

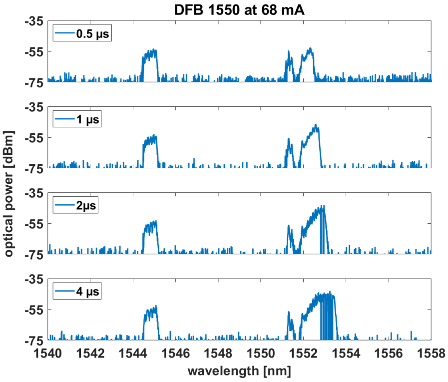


Figure 4.42: Measured optical spectra of DFB 1550 nm for different pulse widths and a current of 68 mA, after integration

broadening is a result of self heating during the pulse. Thereby the mode would redshift. A possibility to verify this is the use of different pulse widths with constant injection current. These measurement results are presented in figures 4.41 and 4.42, using the same devices as before. The current is fixed at 68 mA. By increasing the pulse width stepwise form initially 0.5 μs to maximally 4 μs the same broadening effect as before can be observed. To quantify the capability of the laser structure to dissipate the heat the thermal impedance Z_{thermal} is used [61]. It is defined by:

$$Z_{\text{thermal}} = \frac{\Delta\lambda/\Delta P}{\Delta\lambda/\Delta T} \tag{4.4}$$

Thereby is P the used electrical power and T the temperature. To determine $\Delta\lambda/\Delta T$ the ambient temperature is tuned and the laser is driven with the shortest possible pulse width (200 ns) to reduce the induced heating to a minimum. In figure 4.43 the measured optical spectra are presented.

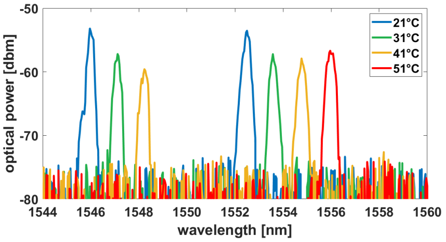


Figure 4.43: Measured optical spectra for different ambient temperature, DFB 1551, pw=200 ns, 70 mA

The ambient temperature was tuned between 21 °C and 51 °C. The wavelength shifted by 3.4±0.1 nm, resulting in 0.11±0.003 nm/K. The wavelength dependency on power is extracted from the pulse width variation measurements. The electrical power is calculated by multiplying the current, 68 mA, with the measured voltage of 4.2 V. By adding the duty cycle as a factor the average dissipated power is obtained. The wavelength dependency is measured as the shift of the long wavelength edge, resulting in 1.17 nm (this is the difference between 0.5 μs and 4 μs pulse length).

For Z_{thermal} a value of 10400 K/W has been determined in this way. For comparison, the thermal impedance for the DFB laser before the integration process can be calculated using the same $\Delta\lambda/\Delta T$ relation, as the InP material is the same in both cases. For the determination of $\Delta\lambda/\Delta P$ there the measurement results presented in figure 4.35 are used. Before the integration process a thermal impedance of 71 K/W is determined. By comparing this with the value after the integration process, which is more than 2 orders of magnitude higher, it can be explained that the DFB lasers are not operating in continuous wave (CW) operation mode: the heat can simply not be removed sufficiently, leading to overheating of the laser. However, during further investigations of the DFB laser structures, it has been discovered that a CW operation can be partly enabled by treating the structures with a high DC current. Thereby an injection current of 150 mA is applied to the laser structure for around 20 seconds.

After this treatment the LI characteristics of the device changed and cw lasing operation is appearing. In figure 4.44 and 4.45 the measured LI and VI curves for a DFB with an designed Bragg wavelength of 1547 nm are presented, before (figure 4.44) the high current treatment and after (figure 4.45). The resulting LI curve shows two current regions where lasing operation appears: 18 to 30 mA and 32 to 38 mA. The maximum optical power in the fibre increases by 23 dB to 50 μW.

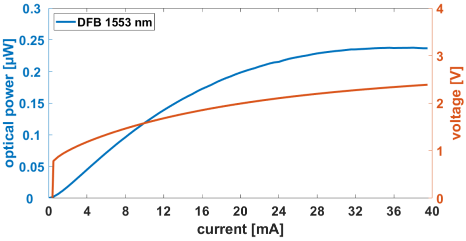


Figure 4.44: Measured LI-curve for DFB 1553 nm before "burn in" treatments

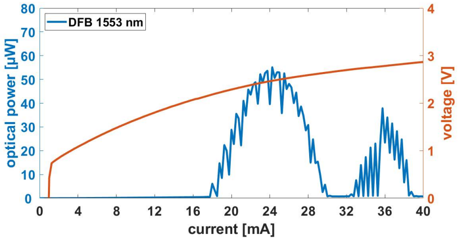


Figure 4.45: Measured LI-curve for DFB 1553 nm after "burn in" treatment

This effect can be observed for all tested laser structures, although the maximum power and current regions varies for each device. This refers mainly to the increase in optical output power. For one series of DFB lasers, with designed Bragg wavelengths between 1546-1554 nm, the maximum optical output power has an average value of 48 μW with a standard deviation of 30 μW. Furthermore, not each laser has two current based lasing regimes as in figure 4.45, but only one. All DFB structures stop working for injection currents beyond 45 mA. This seems to be based on self heating. As mentioned before, a higher injection current leads to an increase in temperature. This is the main mechanism stopping the laser from operating. The fact that some lasers stop working and start again at slightly higher injection currents can be explained by instabilities within the laser, which can induced by external feedback (for example from the out coupling facet), or a phase shift due to the temperature increase. This is supported by the fact that the LI-curve shows multiple sharp spikes, where the laser power drops dramatically. The current used to achieve this "burn in" effect is found empirically by testing different operation points. A statistical analysis has not been performed, due to a

limitation of samples and time. However, for currents higher than 200 mA the laser structure is destroyed irreversible, while for currents below 100 mA no effect has been observed. A time of 20 seconds is proven to be sufficient without degrading the structure, which has been observed experimentally for longer times.
The VI curves show an increased slope after "burn in" and therefore indicate a higher serial resistance. However, this is not always detectable and it requires more measurements to statistically prove this.

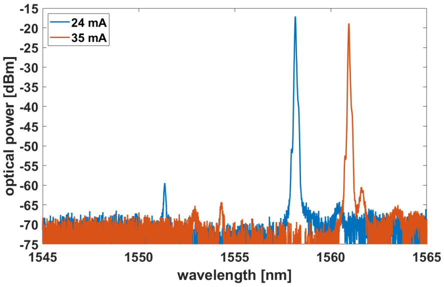


Figure 4.46: Measured optical spectra for DFB 1553 nm after "burn in" treatment for 24 mA and 35 mA

In figure 4.46 the measured optical spectra for the DFB laser with the designed Bragg wavelength of 1553 nm is presented. The current has been set to 24 mA and 35 mA, respectively. These values have been selected as they are in the centre of the two operation regimes visible in figure 4.45. Both spectra show clear single mode lasing operation with a side mode suppression ratio (SMSR) of more than 30 dB. Increasing the current from 24 mA to 35 mA shifts the lasing peak by 2.8 nm, which must result from the self heating based on the applied electrical power. Calculating the corresponding thermal impedance results in a value of 660 K/W. This value is nearly 10 times larger as compared to the structure before the integration process, but clearly smaller than measured before the "burn in" treatment. This indicates a change of the thermal properties. As the VI-curve shows only minor changes it is suspected that thermal resistance changed due to a creation of a better thermal conductivity. In detail it is assumed that the thermal connection between the initial foundry metal contact and the added probing pad is increased by melting the interface. This would explain the minimum current that is needed to achieve this effect. The probing pad increases the overall heat flow and reduces therefore the thermal impedance.
The DFB laser BB clearly suffered from the integration process, which is mainly due to the poor thermal conductivity towards the cooling element. However, the laser is still operational in pulsed and CW operation mode.

4.2.3 Electro absorption modulator (EAM)

For the demonstration of the integration technology transmitter and receiver circuits are realized. While the central BB in the receiver circuit, the photodiode, is capable of transforming the modulated optical signal directly into an electrical one, the transmitter is relying on two separate BBs to perform the inverse operation. One to generate light with a single wavelength, the DFB laser, and the other to transfer the electric modulated signal onto the emitted light, an EAM. In this section the characteristics of this latter BB after the integration process are presented. Ideally the performance would be compared with the initial device properties, but as mentioned earlier, high frequency measurements on the full InP wafer are not performed, to reduce the risk of breaking the wafer. The measurements after bonding are performed using the integrated DFB BB as a light source. As mentioned in the section 4.2.2, the performance of this BB is not uniform for the different emission wavelengths, which influences the EAM characterization.

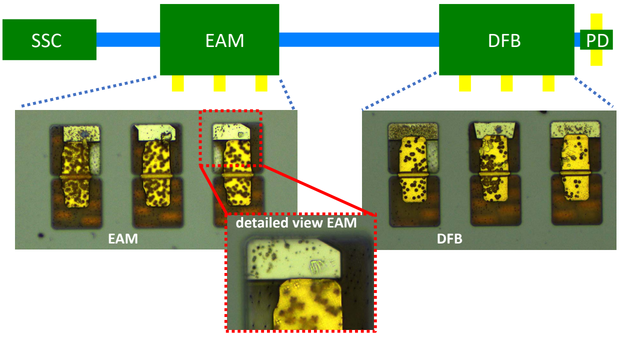


Figure 4.47: Design of the EAM test structures (top) including pictures of the realized metal contact pads showing the open connection for the EAM

In figure 4.47 the design used is presented. It consist of the SSC, EAM, DFB and a monitor PD. The latter is short circuited, due to alignment issues. In the bottom of the figure are two pictures of the realized metal contact pads. In the right picture it can be seen that the golden pads overlap with the original ones from HHI (silver colour). For the EAM BB, presented in the bottom left of the figure, this is not the case. A small gap between the two pads is visible in the enlarged picture. Fortunately the opened contact area of the initial foundry pad is large enough to probe these directly. All measurements are performed using a GSG probe with a pitch of 125 μm.

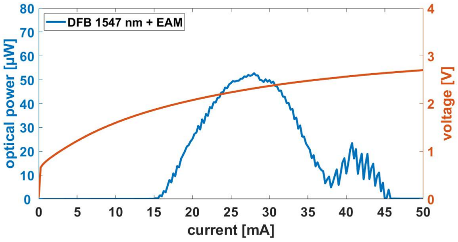


Figure 4.48: Measured LI-curve for DFB 1547 nm after "burn in" treatments

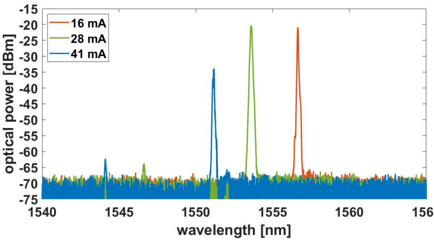


Figure 4.49: Measured optical spectra for DFB 1547 nm for 3 different injection currents

First the CW operation of each DFB laser is activated by applying 150 mA injection current for 20 sec as described in section 4.2.2 ("burn in"). The laser is then characterized, whereby the light travels trough the electrically unconnected EAM BB. This absorbs part of the light and so induces additional insertion loss. Due to the DFB performance variation is it not possible to determine these extra losses. In general the performance of the used DFB laser, in combination with the EAM, is comparable to the results determined for the single laser. In figure 4.48 an example of a measured LI curve for a DFB EAM combination and in figure 4.49 the corresponding spectra for 3 different injection currents are presented.

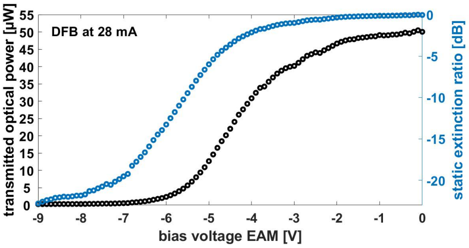


Figure 4.50: Measured transmitted optical power as function of the EAM bias voltage

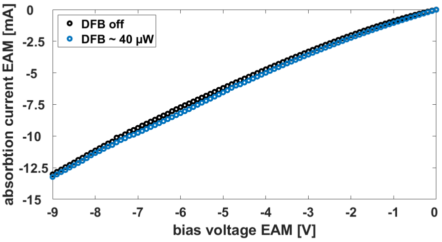


Figure 4.51: Measured EAM absorption current as function of the bias voltage

For the characterization of the EAM structures a bias voltage is applied. The absorption current and the transmitted optical power are measured as a function of different voltage values. A representative example for such measurements is shown in figures 4.50 and 4.51. The first shows the measurements of the transmission. On the left axis the received optical power is plotted in μW, representing the results on a linear scale, while the right axis uses the logarithmic unit dB, expressing the ratio between the transmission at 0 V and at the applied bias voltage. For small bias values nearly no light is absorbed and the transmission is high. Starting from -2 V the received optical power is reduced, reaching the maximum slope between -4.5 and -7 V (operation region) after which saturation begins, limiting further absorption increase. A maximum static extinction ratio of 23 dB has been achieved. However, the fact that the transmission is unaffected for the first 2 V is unexpected. The foundry EAM BB description defines -2 V as the actual operation point. Therefore the absorption curve is shifted. Two reasons have been found that could contribute to this behaviour. The first is based again on the internal temperature. The EAM structure itself does not dissipate much heat. However, the absorption band is designed to operate around -2 V at room temperature. As reported earlier the DFB laser suffers from self heating, resulting in a shift of the emission wavelength towards longer values. As the bandgap of the EAM shifts less, due to a smaller change in local temperature, the absorption is reduced. This can be compensated by either heating the EAM or by increasing the bias voltage. The latter can be seen for the measured EAMs absorption curves.

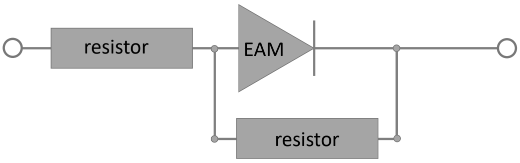


Figure 4.52: Schematic circuit explaining the additional voltage drop over the EAM structure

The second reason is related to the measured current of the device, which is shown in figure 4.51. This curve should follow the shape of the light absorption plot in figure 4.50, however due to a large dark current this behaviour can not be seen. The dark current is not specified by the foundry, but values within the mA range, as measured for this device, are clearly too large and indicate an under lying problem. In case of the PD BB the dark current is found to be two order of magnitude higher than expected. For the EAM this might be identical, leading to the same conclusion that an additional leakage current path is existing due to missing device passivation. Part of the bias voltage is used for this unwanted resistance, resulting in a reduced voltage drop over the actual EAM structure, visible as a shift of the operation point. A schematic of such a electrical circuit is presented in figure 4.52. For the next realization it is important to measure the absorption current before bonding, which could be achieved with spring loaded probes only and the use of the vertical mirror BB.

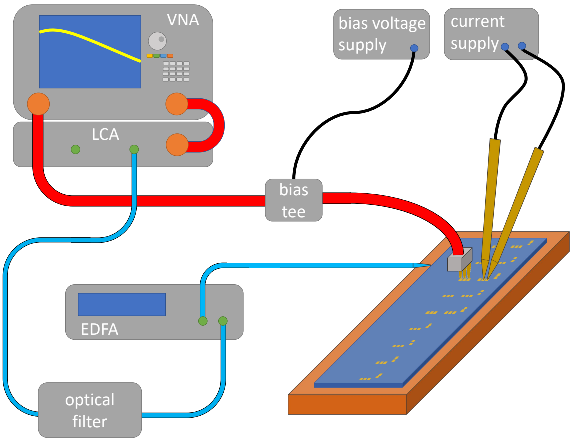


Figure 4.53: Schematic of the setup used for the small signal response measurement of the EAM

The high speed characteristics of the EAM BB are analysed by measuring the small signal response with a VNA, in combination with a LCA element. The used setup is schematically presented in figure 4.53. Due to the limited DFB output power an erbium-doped fiber amplifier (EDFA) has been used, cascaded with an optical filter, to increase the overall output power while suppressing the amplified spontaneous emission (ASE).

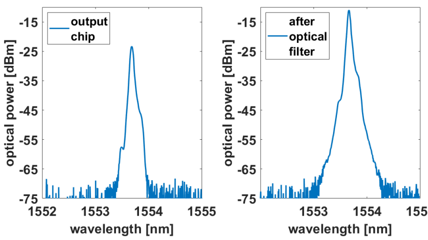


Figure 4.54: Measured spectra at the output of the chip (left) and after the optical filter (right)

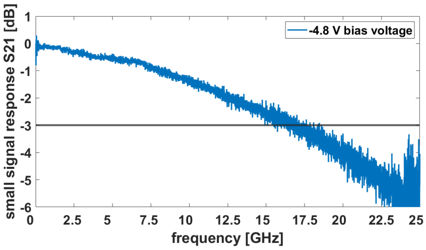


Figure 4.55: Measured EAM small signal response

The EDFA is operated in constant gain mode and operates at 20.5 dB gain to achieve an output power of 5 dBm. In figure 4.54 a comparison of the original optical spectra and the one after the filter is presented. The peak power is increased from -23 dBm to -11 dBm, which is coupled into the LCA. The electrical path from the VNA to the EAM is de-embedded using a standard SOL calibration substrate. The magnitude of the measured small signal response for S-parameter S_{21} is plotted in figure 4.55. The DFB laser is operated at 28 mA and a bias voltage of -4.8 V is applied over the EAM. The 3 dB bandwidth is determined to be 16.5 GHz. For the modulator this bandwidth describes the point where 50 % of the optical modulated power is lost. In [19] a 3 dB bandwidth of 45 GHz is specified for the EAMs. However, the devices used for the first hybrid module realization have been delivered with the indication of reaching 28 GHz. The achieved result doesn't reach either of these specifications. As was the case for the photodiode, the reason could be, that the received material provides only limited quality devices due to fabrication problems, or the integration process impacted the devices.

4.3 2nd wafer generation

For the demonstration of the integration technology two design cycles have been completed, resulting in two wafer batches from each foundry. However, only one wafer pair, from the first generation, has been used for demonstrating the 3-D wafer level integration technology. It has been decided that a second process run can be started after the results from the first one have been analysed to improve the integration technology itself and save the valuable material for that purpose. However, this strategy leads to a time constrain.

The wafer design for the second generation has been submitted before receiving the first generation wafer batch and could therefore benefit only partly from the first realization. Nevertheless, some new designs have been included in particular, to improve the measurement accuracy of the waveguide propagation loss, and a new polarization independent AWG has been introduced. In the following section these adapted designs and their characterization before the integration process are presented. The extracted parameters will be compared with those from the wafer material used for the first generation hybrid module realization.

4.3.1 Waveguide loss structures

In section 4.1.1 two methods have been described to determine the waveguide propagation loss. Both are using a series of a test structures with varying waveguide lengths. For the first method the maximum transmission is plotted as a function of that length, which results in a direct measurement of the insertion loss and propagation loss. The second method uses the ratio between the wavelength depended minima and maxima, resulting from the FP cavity between the vertical mirrors. Both concepts have been reused for the designs of the second wafer generation. The first design is an improved version of the first method presented in section 4.1.1 and will therefore be described as first method. Another design uses the concept of an interferometer and is therefore introduced as the third method.

First method

One limitation of the initial design is the limited total device length. If the measured waveguide loss is smaller than the measurement resolution it is impossible to determine the actual value.

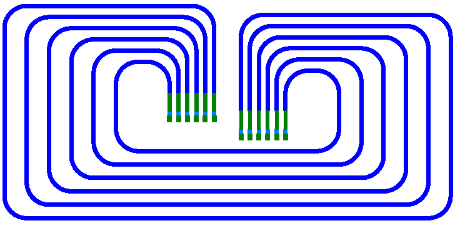


Figure 4.56: Improved design for length dependent loss measurement

To avoid this a new design, presented in figure 4.56, is introduced. It consists of two vertical mirrors connected via a long folded waveguide track. The design has a length increment of 2 mm per structure. The longest one is 15.8 mm, where the first generation design achieved a maximum length of 5.2 mm. The footprint increases by a factor of 2.5 (5 mm^2 versus 12.5 mm^2). The second design has all the vertical mirror BBs within a small area, which can either be an advantage or a disadvantage, based on the measurement setup. The setup used here has just one optical microscope, a small travelling range between input and output is therefore beneficial.

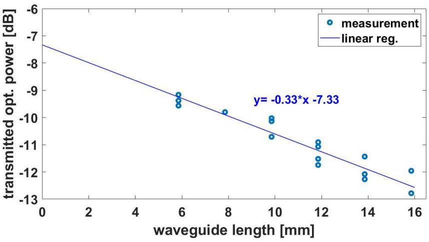


Figure 4.57: Measured propagation loss for deep etched waveguides, second generation

The measured transmission for the different waveguide lengths is plotted in figure 4.57. The propagation loss α is determined to 3.3±0.3 dB/cm and the loss per vertical mirror is 3.7±0.2 dB. Both values are improved compared to the wafer used for the first hybrid module realization, confirming the assumption that the first wafer suffered from process deviations during the fabrication. The absolute error of the waveguide propagation loss also improved, as is to be expected. However, the increase in length makes the second method, based on the FP cavity to determine the waveguide propagation loss, not useable any more. The distance of the FP fringes shrinks with increasing cavity length. How accurate these fringes can be sampled, depends on the resolution of the spectrometer used. For a cavity length longer than 5 mm the distance of two fringes is smaller than 70 pm which leaves less than 7 sampling points to determine the minimum and maximum value. This already affects the error margin. This new design achieved the intended error reduction using the first method, but at the price of a large footprint increase.

Third method
The third method is based on a Mach Zehnder interferometer (MZI) with a length difference ΔL between the two arms. It has the advantage of being independent of loss contributions and fluctuations, which are outside of the MZI structure itself. The original idea by Jos van der Tol was first realised within the work of Josselin Pello [62]. Based on the optical length difference between the two arms interference occurs. The ratio C of the maximum ($P_{\max}$) and minimum ($P_{\min}$) transmission can be used to determine the waveguide propagation loss. In [62] the mathematical description of this technique is presented. The relation between the propagation loss α and the maximum and minimum transmission value can be expressed by the following equation:

$$\frac{C+1}{C-1} = \cosh(0.5\alpha\Delta L) \tag{4.5}$$

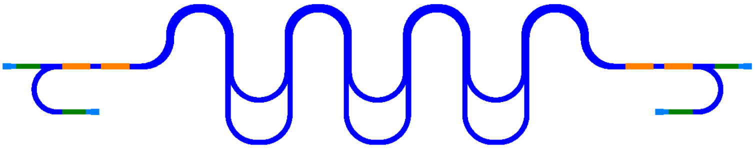


Figure 4.58: MZI design with a length difference between the two arms of 2.1 mm to determine the waveguide propagation loss

The measurement has been performed using the design presented in figure 4.58. It shows the two waveguides connected with a 1x2 MMI at each side to form the MZI. Both arms of the MZI use the same amount of bends to avoid an additional loss unbalance between them. Two designs have been created with length differences of 2.1 mm and 2.4 mm, respectively. The interferometer itself is embedded within the DUT test structure which has been introduced in section 4.1.3. This approach uses in total four 1x2 MMI BBs where two 2x2 MMIs would have simplified the design. However, in that case a possible unbalance in the MMI BB would lead to a systematic error. Since the 1x2 MMIs are symmetric devices, they do not have an unbalance.

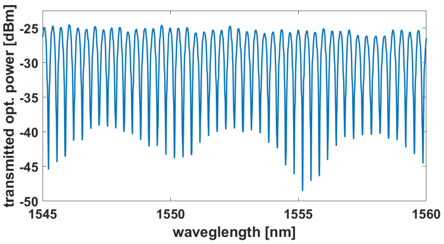


Figure 4.59: Results of the transmission measurement for the MZI based structure presented in figure 4.58

The transmission measurement result for a MZI with a length difference between the two arms of 2.1 mm is presented in figure 4.59. It shows ratios between the maximum and minimum transmission of more then 20 dB. The waveguide propagation loss is calculated using equation 4.5 resulting in 0.992±0.26 cm^{-1} which is equal to 4.3±1.1dB/cm. The error is based on the standard deviation of the measurement results including both of structure ($\Delta L = 2.1$ mm and 2.4 mm). The waveguide propagation loss value is 1 dB larger as compared to the result of the first method. This is within the error range of the third method, which is nearly 3 times larger. Two possible reasons can be given for explaining this larger error. The first one is the high requirement on the dynamic range of the PD: for measuring an α of 3 dB/cm a dynamic range of more than 29 dB is required. Second, the measured maximum and minimum values strongly depend on the sampling. For these long cavities the distance between maxima and minima becomes so small that the value can only be determined with limited accuracy. Beside these two measurement limitations additional parasitic modulations, due to reflections in the circuits, decrease the measurement accuracy as well.

Conclusion
The new designs introduced in the second photonic wafer have been used to determine the propagation loss and the insertion loss of the vertical mirror. The presented results show a clear improvement for both parameters. The introduced methods itself show diverging potential. The first method delivers the best measurement accuracy for all compared techniques, however it requires a large design area. The second method is independent of external power fluctuations, however the achieved measurement accuracy is limited by the method itself. Improvements could be achieved by using equipment with higher accuracy.

4.3.2 Polarization independent AWG

In section 4.1.4 the results of a 3x8 AWG have been presented, which has been used for measuring the effects of the photonic electronic integration technology. The fabricated structure shows a polarization dispersion of 1 nm, which makes it unusable for de-multiplexing, as the incoming signal (of unknown polarization) could shift by a more than a channel spacing. However, for multiplexing this first design could still be used, as the light emitted by the diode laser has a fixed polarisation.

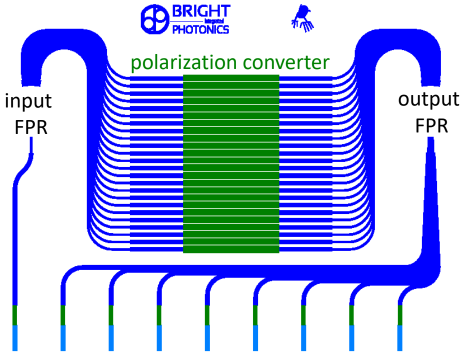


Figure 4.60: Polarization independent AWG design connected with vertical mirror structures for characterization

To de-multiplex an incoming signal a polarization independent AWG is needed. A design to achieve this is presented in figure 4.60. It has been developed together with Bright Photonics. Every AWG design uses a series of bend waveguides to achieve the length variation needed to split the light into different wavelengths. These bends can have an influence on the SOP. The concept proposed here is based on a symmetric design and a full polarization rotation in the centre of the AWG. Therefore the different polarization states would experience the same effects when propagating through the structure. For this approach the polarization rotating BB from HHI has been placed in the centre of the design.

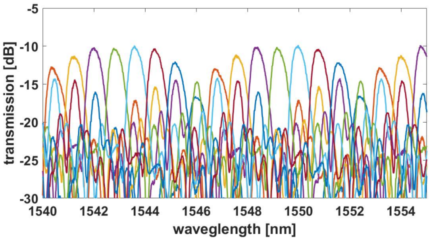


Figure 4.61: Measured transmission for the polarization independent AWG design

The measurement results are presented in figure 4.61. The different channels can be identified, the channel spacing and FSR correspond to the design values, but the high crosstalk between the channels makes this AWG unusable. Each channel shows an additional transmission peak at half of the FSR value. To analyse this further a reference structure has been used for comparison, which is an identical AWG design with straight waveguides instead of the polarization converter BB. The reference structure shows no FSR/2 peak. A possible explanation is a reflection from the polarization converter BB. As shown in section 4.1.1 the vertical mirrors used on the first wafer generation have a back reflectivity of around 14 %. This means some light will be reflected at the vertical mirrors, which are used at the ends of the AWG testing circuits. If the polarization converter reflects part of the light, the following path is possible: Part of the light enters the AWG and is reflected at the polarization converter, therefore propagating back towards the input mirror, where it is reflected back into the AWG. In this way part of the light propagated effectively twice through the input side of the AWG resulting in a double phase shift at the output FPR, which leads to a spurious peak at half the FSR from the main channel. More analysis of this effect requires detailed knowledge about the actual AWG and polarization converter design, which has not been available.

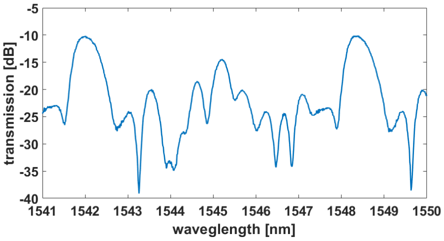


Figure 4.62: Measured transmission for one channel of the polarization independent AWG

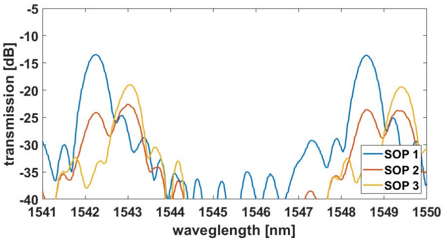


Figure 4.63: Measured transmission for different SOP of for one channel of the reference AWG

The main intention of this AWG design is the creation of a polarization independent de-multiplexer. Therefore a single channel has been measured for different polarization input states using an external polarization controller (3-coil design). No measurable polarization dependence has be seen. An example measurement is presented in figure 4.62. For comparison the reference structures has been measured as well and shows a polarisation dispersion of 1 nm (see figure 4.63). This concludes that the concept for this AWG is working. However, it important to identify the cause of the FPR/2 peak. Therefore measurements with a different coupler type like the SSC could be performed for comparison. Suitable designs are included for in this wafer design, but these can only be measured after the integration process is completed and the chips are singularised.

4.4 Conclusion

Wafer material from the Fraunhofer HHI foundry has been used to analyse the effect of the 3-D integration process. Therefore the performance of the photonic BBs has been analysed before and after the integration process to identify its impact. This has been possible due to the use of the vertical mirror BB, which has been introduced for this purpose. The waveguide propagation loss has been measured before and after the integration process showing a improvement for the integrated structures. An overview of the measured values is presented in table 4.2. The insertion loss is determined for the different passive BBs. This value increases for vertical mirror structure after the integration process from initially 6.0 dB to 8.1 dB per coupler, due to added metal marker structures and the absent of an anti reflection coating at the backside. The performance of the passive components before and after the integration process is comparable. An impressive example is the realised AWG structure, which is only minimal influenced by the expansion of the InP membrane in the bonding process.

waveguide propagation loss	before integration process		after integration process
	method 1	method 2 / 3	method 1
deep etched WG series 1	4.8±0.5 dB/cm	3.9±0.8 dB/cm	4.4±0.4 dB/cm
deep etched WG series 2	6.8±0.5 dB/cm	5.2±0.4 dB/cm	-
shallow etched WG series 1	3.6±0.4 dB/cm	-	-
shallow etched WG series 2	5.7±0.8 dB/cm	-	-
deep etched WG 2nd generation	3.3±0.3 dB/cm	4.3±1.1 dB/cm	-

Table 4.2: Summery of the extracted waveguide propagation loss values, note that the series do not imply the same structure before and after the integration

For the characterization of the active components PIN PDs, DFB lasers and a EAMs have been characterised. The comparison of the devices before and after bonding is limited to the DFB laser, as to reduce the risk of destroying the wafer during the measurement before bonding to a minimum. After the integration process all structures are analysed using the integrated SSC BB. The PIN PD and the EAM BBs show both a large dark current which could indicate an impact of the integration technology. This might result from by a missing passivation layer. However, both devices operated at reasonable performance values and enable the targeted operation speeds of 25 Gbaud/s. The DFB laser suffers from poor heat sinking, which initially limited the structure to pulsed current operation only. It has been found that the heat sinking performance of the device can be improved by applying a "burn-in" current of 150 mA for 20 seconds to the structures, resulting in an improvement of the thermal impedance from 10400 K/W down to 660 K/W. After this "burn in" treatment the laser can be operated at small CW injection currents.

These initial results of the 3-D integration process show a promising starting point for the operation with the co-designed electronic circuits, which will be further explored in chapter 5.

Chapter 5

Co-designed assemblies

It has been demonstrated that the photonic components are still operating after the integration process. Therefore the co-designed circuits are investigated to further verify the 3D integration approach. The obtained results will be presented in this chapter. To verify that the electrical connection between the photonic and electronic circuits is not limiting the overall device performance, a characterization of the electrical interconnect is performed first. Afterwards two demonstrators are presented to illustrate the opportunities of this technology: a dual channel transmitter and receiver circuit. For this purpose data transmission experiments are performed.

5.1 High bandwidth electrical connections

The 3D integration technology relies on high speed broadband electrical interconnects. In cooperation with Xi Zhang and Arezou Meighan a test cell has been designed. Its functionality is described in Xi Zhang's PhD thesis [21] chapter 2.

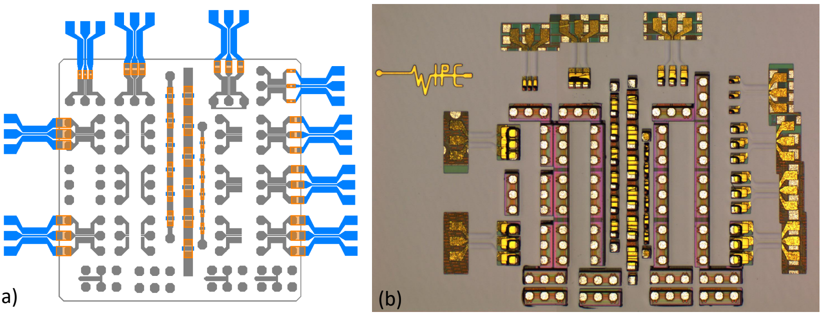


Figure 5.1: (a) design of the electrical interconnect cell - InP metal tracks are blue, BiCMOS metal tracks are grey, electrical interconnect are yellow; (b) a picture of a realized structure

Figure 5.1 (a) shows the combined design file for electronics and photonics. The metal tracks on the InP are presented in blue, the BiCMOS ones are shown in grey. Each layer consists of

GSG transmission lines, of which one end will be connected to the co- designed counter part. The positions of the electrical interconnects are highlighted in orange. A microscope picture of the first realization is presented in figure 5.1 (b). Different pad sizes and pitch dimensions have been designed to evaluate the capability of the process. The measurements are performed on a front runner wafer as it suffered less from the wafer shift induced by the bonding tool. Due to this wafer shift only the large pad sizes are successfully connected. Each design includes de-embedding structures (the InP ones are not included in figure 5.1) to subtract the influence of the contact pads and taper structures. However, the measurement results reported in [21] have been achieved without applying de-embedding.

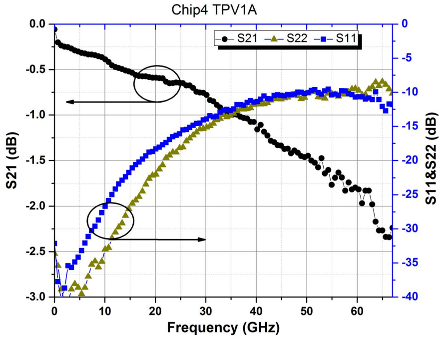


Figure 5.2: Measurement results of an electrical interconnect originally published in [21]

The characterization has been performed using a VNA with a bandwidth of 67 GHz. An example of the achieved S-parameter characterization results is presented in figure 5.2. These are cited within this work to present a complete analysis of the 3-D integration technology. The electrical 3 dB bandwidth of S_{12} exceeds the bandwidth limitation of 67 GHz of the used equipment. The reflection values (S_{11} and S_{22}) are below -10 dB up to frequency of 50 GHz. These results have been achieved for the largest GSG pads (65 by 65 μm) and a pitch of 125 μm. This performance falls behind the expectation based on simulations. Nevertheless, these results are impressive, considering the process difficulty involved and the omitted de-embedding. The electrical interconnect supports the technology intended within this work and shows potential for further improvement based op process optimization.

5.2 Receiver

The hybrid receiver module is developed in cooperation with Ghent University, Belgium, in particular with Gertjan Coudyzer. He provided the design for the BiCMOS transimpedance amplifier (TIA) [24]. The photonic design is adapted towards the electronic design. In section 2.2 the placement of the electrical contact pads has been introduced, resulting in assembling all electrical control interfaces of the hybrid module at 3 edges of the chip. In figure 5.3 half of the resulting dual channel RX design is presented. The full structure can be reconstructed by mirroring this picture along the dotted line at the top. The right part of figure 5.3 shows the electrical I/O's of the BiCMOS wafer (grey). They surround the actual TIA design (not visible). The metal pads at the right hand side, bottom and top (the latter is not visible in this picture) are the ones opened to electrically access the hybrid module. The PIN PD is connected to three pads at the left hand side of the TIA design.

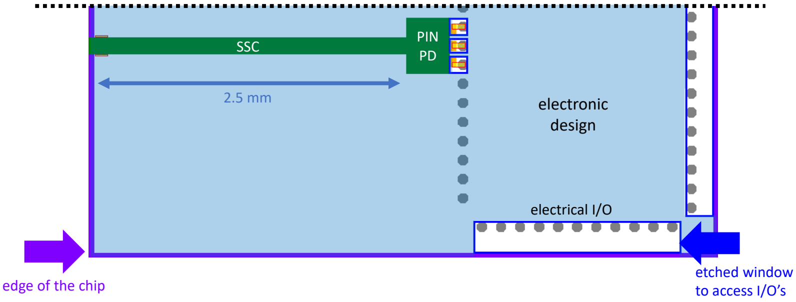


Figure 5.3: One channel from the co-designed RX layout, right side: electronic design, left side: photonic design, light blue layer: InP membrane, grey circle: BiCMOS contacts

The photonic structure consist of the PIN PD connected to a SSC. The resulting hybrid chip size is defined by the purple outer line. These dicing lanes (introduced in section 2.1) match the design area and form a facet at the end of the SSC. The photonic and electronic structures are placed side by side, which results in a non-optimized footprint. The PD is placed with a lateral offset to avoid heat transfer from the electronics to the photonics layer. It is necessary to orientate the SSC in the direction dedicated for fibre coupling, resulting in the ensemble presented in figure 5.3.

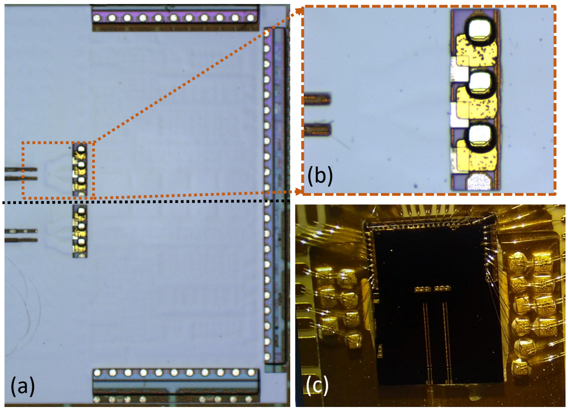


Figure 5.4: Realized RX chip in (a) with a detailed view in (b); (c) presents the assembled module (picture by Gertjan Coudyzer)

In figure 5.4 (a) a top view of the fabricated chip is presented and in 5.4 (b) a detailed view on the interconnects for the top PD is shown. After the singulation of the wafer into the hybrid chips, the RX has been assembled onto a printed circuit board (PCB) board (designed by Gertjan Coudyzer). The connection between the chip and the board has been achieved with wire bonding. A picture of the resulting module is presented in figure 5.4 (c). A transmission experiment has been performed at Ghent University and gives a proof of concept. An open eye has been measured for a 10 GBit/s non return to zero (NRZ) signal. Higher bit rates are not possible due to a design mistake. The electrical path to supply the bias voltage to the cathode of the PD is not decoupled, and therefore introduces an extra inductance, limiting the overall bandwidth of the hybrid module assembly. This path is the connection from the edge of the chip to the interconnects in the centre.

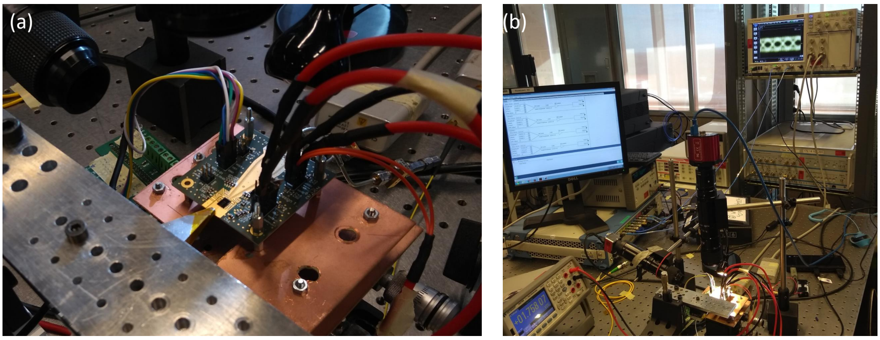


Figure 5.5: (a) detailed view on the measurement setup used for the RX hybrid module realization, (b) wider view with the 10 Gbit/s eye diagram visible in the background (both pictures by Gertjan Coudyzer)

This limitation can be resolved by adding a decoupling capacity on chip, close to the actual interconnect. As shown earlier neither the PIN PD nor the electrical interconnects are limiting the performance of this assembly. For the second generation the electronic design has been adapted and future experiments are needed to evaluate the performance. Nevertheless, a working hybrid receiver module has been presented and no process related limitation are detected.

5.3 Transmitter

The hybrid transmitter module is achieved in cooperation with the IC group at the TU/e, especially with Xi Zhang, who provided the EAM driver design [21].

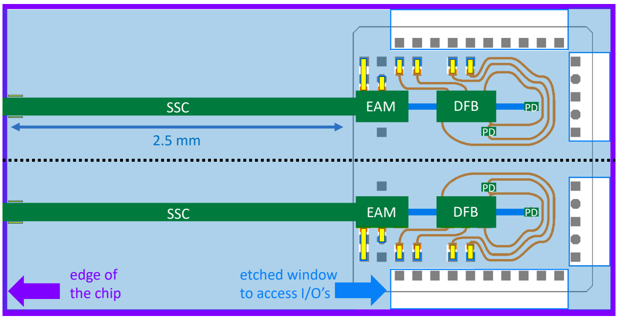


Figure 5.6: Co-designed TX layout, light blue layer: InP membrane, grey circle: BiCMOS contacts, orange: metal routing on the InP layer

The layout for the transmitter is presented in figure 5.6. It includes two channel, which are mirrored along the doted horizontal line in the centre. They are based on the combination of the DFB and EAM BB. Two monitor PDs are included as well. One is optically connected to the DFB to absorb the part of the light emitted towards the backside. The other is placed with a small lateral offset and is intended for measuring the temperature by monitoring the dark current of the PD.

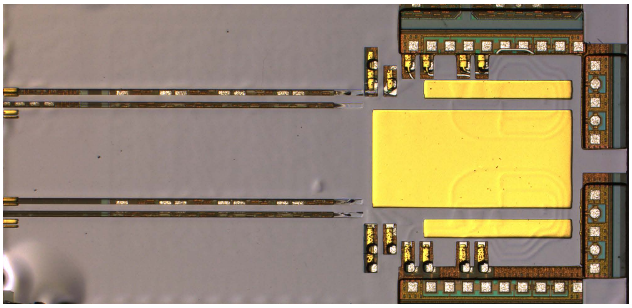


Figure 5.7: Realized transmitter chip with metal heat spreader on the backside

In figure 5.7 the fabricated device is presented. A relatively large gold plate can be seen on the backside of the InP membrane. This is intended to function as a heat spreader and as thermal interface in case that cooling elements are connected. During the measurements it has not been possible to thermally connect to these metal structures to an external cooling element. Their heat spreading efficiency will be estimated in the following.

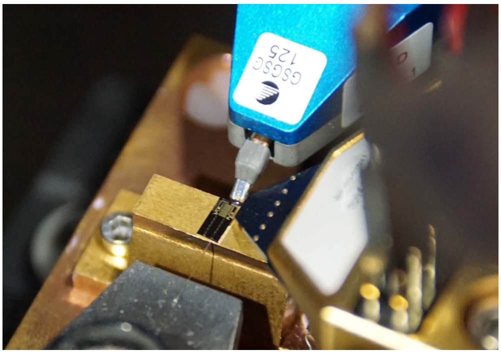


Figure 5.8: Picture of probed transmitter chip

The first hybrid wafer realization resulted in 4 transmitter chips. This amount is the maximum possible, which is limited by the NXP MPW cell size. Due to the wafer shift only one channel per chip is functional. The characterization of these devices is performed using directly the BiCMOS control contact pads at the edges of the chip. Each channel uses two arrays of pads with a 90 ° angle between them (see figure 5.6). The array parallel to the optical path (top and bottom of the chip in figure 5.7) provides the interfaces for all DC signals, while and the shorter row (at the right of the chip) forms of a GSGSG pad configuration used for the differential high speed input of EAM driver. Each array is probed with a multi pin probe. A picture of the assembly is presented in figure 5.8.

First the DFB laser of each transmitter has been characterised. All structures show the electrical characteristic of a diode and 2 out of 4 structures are lasing. The best one achieves a CW output power of 7μW in fibre. The fact that all structures can be probed via the electronic wafer proves the functionality of the electrical interconnects. The LIV curve for the best transmitter module is presented in figure 5.9.

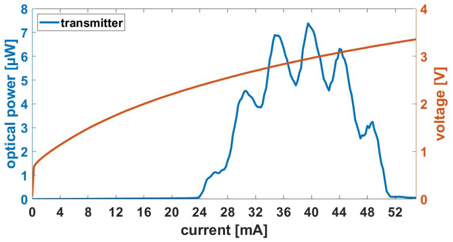


Figure 5.9: LIV curve of the best performing DFB laser integrated in a transmitter circuit, measured through BiCMOS

The maximum current at which lasing occurs is 6 mA higher than measured for the test DFB structures, resulting in 51 mA. The difference between these structures is an additional metal plate on the backside of the InP membrane and the direct electrical connection to the BiCMOS wafer (electrical interconnect). These structures are only used for the transmitter circuits. The difference in maximum lasing current indicates that heat dissipation is improved and therefore reduces the thermal resistance. This leads logically to a delayed thermal role over. An estimation of this improvement relies on the dependency of the temperature and the electrical power. The improvement in temperature ΔT is proportional ΔI^2 which is equal $2 * (6\ mA/51\ mA)$ resulting in 24 %. Identical behaviour has been seen for the second lasing transmitter module, supporting this theory. This means that if it is possible to connect a cooling element to this metal plate the laser performance would be significantly improved.

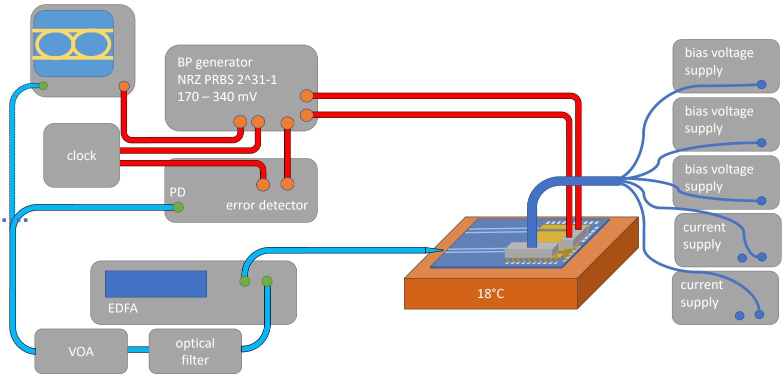


Figure 5.10: Schematic setup used for the hybrid module data transmission experiment

The hybrid transmitter with the best performing laser has been selected to further investigate the performance of the module. The EAM is fully integrated so it is not possible to test it independent from the electronic circuit. A characterisation of the S-parameter matrix could not be achieved, as the EAM driver uses a differential input signal, which can not be provided by the available equipment. The performance of the hybrid module has been analysed by performing a data transmission experiment. The setup used for this measurement is presented in figure 5.10. The transmitter chip is placed on a temperature controlled chip holder with the InP membrane facing upwards. A bit-pattern generator (BPG) is used to generate a pseudorandom binary sequence (PRBS) with a length of $2^{31}-1$. The data and inverse data output of the BPG have been connected to the input of the BiCMOS driver by using a GSGSG-probe. An additional bias voltage has been added to the signal by using a bias tee (not included in the schematic) which is needed for the driver to operate [21]. The optical output of the transmitter is amplified using an EDFA, cascaded with a band pass filter to suppress ASE. After the filter a variable optical attenuator (VOA) is used to define the input power of the receiver. The gain of the EDFA is set to reach a maximum receiver input power (measured after the VOA for 0 dB attenuation) of 1 mW. The output of the VOA is connected to either the photodiode integrated in the bit error rate tester (BERT) or the the eye diagram analyser. It has not been possible to measure an eye diagram for the tested hybrid module. Nearly no extinction ratio has been seen. This was independent of the selected operation parameters, which are the voltage swing that can be set at the BPG to values between 170 mV and 360 mV (peak-to-peak), and the EAM bias point. The latter is controlled via the driver circuit and is limited to a maximum value of -2 V. As shown in section 4.2.3 the EAM operation point has shifted to higher reverse bias points, which makes this hybrid assembly non operational. However, the driver circuit indicated its functionality, which has been evaluated based on parameters like voltage drops and the currents, which match exactly the designed values. A direct measurement of the electronic circuit after the integration process is not possible as all available structures have been connected to the photonic membrane. Based on the fact that the electrical TIA circuit for the receiver (see section 5.2) has operated as intended, the functionality of the EAM driver has not been in doubt. Apparently the operation of the hybrid module is purely limited by the mismatch in EAM bias voltage.

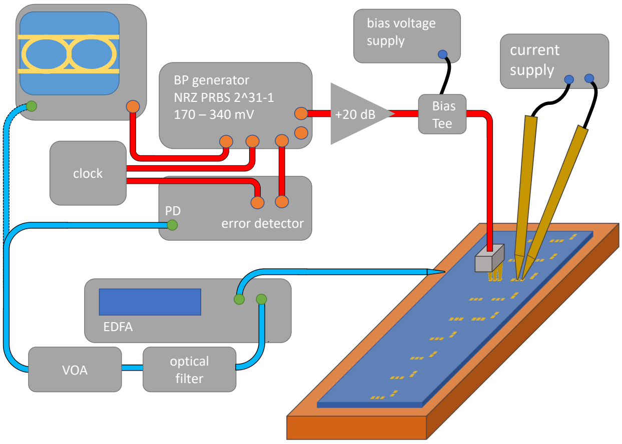


Figure 5.11: Schematic setup used for integrated photonic chip data transmission experiment

For demonstration purpose of only the photonic circuit a transmission experiment has been performed using the DFB EAM combination presented in section 4.2.3. The used setup is shown in figure 5.11. The BPG delivers a voltage swing of 250 mV_{pp}, which is amplified by 20 dB resulting in an voltage swing of 2.5 V_{pp}. The operation point of the EAM was set to -4.8 V using a bias tee. The laser injection current was set to 28 mA, which corresponds with the maximum output power. The optical output of the chip is amplified with an EDFA, cascaded with a band pass filter and a VOA to control the receiver input power. As with the hybrid module characterization is the EDFA set so that the maximum optical power is 1 mW (measured in PD) in case of no attenuation. The emission wavelength is 1553.9 nm. The measured eye diagrams for a receiver input power of 1 mW are presented in figure 5.12. The measurement has been performed for 12.5, 20, 25 and 30 Gbit/s, with achieved extinction ratios of 5.6, 5.1, 4.7 and 4.3 dB respectively. It can be seen that the top rail contains an instability, resulting in a wide band. This behaviour results from the DFB laser and the thermally introduced noise due to the self heating effect. Nevertheless open eyes have been measured up to a data rate of 25 Gbit/s.

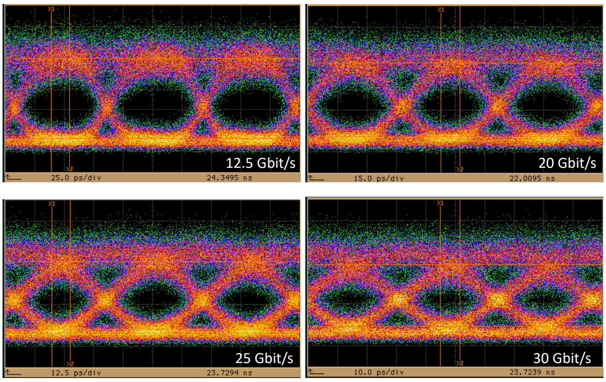


Figure 5.12: Measured eye diagrams for the integrated optical transmitter at different bit rates

For a bit rate of 12.5 Gbit/s the bit error rate (BER) has been measured as a function of the receiver input power. The result is presented in figure 5.13. For 0 dBm receiver input power a BER value of 3E-9 has been achieved. The BER increases rapidly by reducing the receiver input power which made BER measurement of higher bit rates unreasonable.

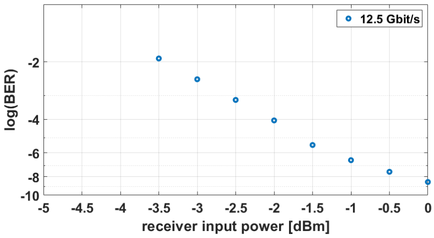


Figure 5.13: Measured BER for the integrated photonic chips for a bit rate of 12.5 Gbit/s

For the hybrid transmitter it can be concluded that the addition of the metal head spreader enlarges the usable current range, which is an indication of improvement of the device performance. Because of the changed bias voltage operation point of the EAM the driver is unsuitable for the photonic assembly. However, it has been demonstrated, that the photonic circuit could work with the proposed driver if the bias voltage would be adapted.

5.4 Conclusion

The capability of the 3D integration technology, under investigation, is demonstrated by characterizing an electrical interconnect test cell, a receiver and a transmitter circuit. This work has been achieved in cooperation with the Gent University and colleagues from the TU/e. The electrical interconnects show a 3 dB bandwidth of more than 67 GHz, which was limited by the used measurement equipment, and was not yet corrected for the effects of on chip transmission lines. The receiver module operated at a bit rate of 10 Gbit/s, which was limited by the interconnect parasitics of the PD cathode trace, which was not sufficiently anticipated (decoupled) in the EIC design. For the transmitter no data transmission experiments could be performed, due to a shift of the EAM bias voltage point to values outside the range of the EIC EAM driver, which is limited to -2 V. To nevertheless show the capability of the photonic transmitter circuit, a comparable device has been used to measure open eyes up to a 25 Gbit/s and a BER of 3E-9 at 12.5 Gbit/s for 0 dBm receiver input power. The demonstration of these first realized hybrid modules provides a clear indication of the feasibility of this integration technology.

Chapter 6

Conclusions and Outlook

6.1 Conclusion

A novel 3D integration technology to combine PICs with EICs on wafer level is demonstrated. This has been achieved in cooperation with Fraunhofer HHI and NXP, who provided the InP photonic and BiCMOS electronic wafers. The first step is the creation of the EICs and PICs layouts. The electronic designs have been provided by research partners[1], while the photonic part is reported in this work. A co-design phase has been included to optimize the resulting hybrid modules. It includes the definition of the interconnects and the electrical connections, which are used to control the hybrid module. The electrical probing is performed exclusively via the electronic circuit. A definition of the layout is made, assigning three edges of the chip to be used for the electrical control interfaces, while the remaining on is used for the optical interface. The interconnect positions are designed to provide the shortest possible connection between the photonic high speed elements (PIN PD, EAM) and the corresponding electronic control structures (TIA, EAM driver). The remaining connections can be placed freely over the surface. Each interconnect assembles however a thermal connection between the layers which has to be considered during the layout. Since there is no software, which can be used to design both circuits simultaneously, the co-designof the electronic and photonic circuits is defined in the GDSII files. Several design iterations are performed to align the photonic and the electronic circuit designs.

Two boundary conditions for the submission of the designs to the MPW run of the electronic foundry are defined: 1) a minimum distance between the different cells has to be included to provide the required space for the corresponding photonic layout 2) the relative rotation between the designs has to be fixed, as all active components on the photonic wafer support only one absolute orientation.

The integration on wafer level is achieved by matching the corresponding layouts. The design flexibility on the MPW based BiCMOS wafer is limited, therefore it is decided to design the photonic layer to be matching the electronic layer. The integration process is based on matching wafer sizes. The provided electronic circuits are fabricated however on a 200 mm Si wafer, while the photonic circuits are made on a 76.2 mm (3 inch) InP wafer. To unify the

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[1] Gertjan Coudyzer, University of Ghent; Xi Zhang, IC group TU/e, now with NXP Semiconductor

dimensions three identical 3 inch wafers are cut out of the 200 mm electronic wafer. This can be achieved by reconstruction of the basic BiCMOS floorplan based on the following specifications: the dimensions of fundamental reticle, the reticle pitches in two orthogonal directions, the global wafer offset and the position of the submitted designs within the fundamental reticle. The three cut outs are designed to be identical, to reduce the amount of InP wafer layouts and therefore reduce the overall costs. Additional criteria are the inclusion of a maximum amount of designed circuits and a uniform number of the different types. The designs are used as markers for the wafer to wafer alignment as well, which requires a certain positioning of these cells within the cut out wafers.

The electronic 3 inch wafer is used as a basis for the InP wafer design. Several steps are undertaken to create the photonic layout, which includes the co designed circuits and a repetition of several test cells. Between the different structures dicing lanes are placed, which will be used during the singulation process. The wafers are combined with an adhesive wafer bonding approach. It provides a stable mechanical bond, can compensate for wafer topologies and decouples the two wafers in optical, thermal and electro-magmatic domains. Each wafer topology is planarized with spin coating the bonding polymer (BCB). For the combined topology of 10 μm (3+7) a BCB layer thickness of more than 20 μm is used. The alignment of the two wafers is achieved with the backside alignment technique, which was first introduced to the clean room of NanoLab@TU/e within this work. Alignment accuracies of better than 4 μm have been achieved for BCB thicknesses up to 18 μm. The bonding process is performed at 240 °C, instead of the standard 280 °C, to protect the electronic devices from degradation. Preparatory experiments show that applying 240 °C for 15 hours has no measurable effect on test samples, while 280 °C at 1 hour resulted in reduced performance. Therefore the whole process is performed at low temperatures. The reduction to 240 °C results in a curing time of 10 hour. The impact of the different coefficients of linear thermal expansion (CTEs) of Si and InP results in a thermal expansion of the InP membrane of 304 ppm, which should be compensated for future designs. It has been used here to adapt post processing masks. To create the electrical interconnects after the wafer bonding process, first the InP substrate is removed, followed by etching windows through the remaining InP membrane to access the photonic contact pads. The connection between both wafers is realised by creating sloped sidewalls in openings in the BCB layer and cover these afterwards with plated gold. The angle of these sidewalls is around 45 °, resulting in a required lateral distance between the top and bottom contact pad of $\sqrt{2}$ times the BCB thickness. Additional metal heat spreading structures and markers are included on the backside of the InP membrane, before it is singularised by sawing simultaneously through the BCB filled dicing lanes and the underlying BiCMOS wafer.

During the first hybrid module realization a malfunction of the bonder resulted in a lateral shift between the two layouts of 90 μm. Several repair steps have been applied including an adaptation of all post processing lithographies. Due to this most of the devices and circuits have been saved for characterization.

The technology is analysed by characterized multiple photonic BBs before and after the integration process. This is enabled by the vertical mirror BB, which can be used to couple light into or from a fibre, placed perpendicular to the chip surface. Based on the orientation of the connected waveguide the mirror can be used before or after the integration process. To enable measurements of the same device a design is proposed including two 1x2 MMIs to connect both mirror types to the input and output of the structure. This design is however not practical for feedback sensitive structures like the DFB laser, as it introduces reflection at the vertical mirror facet of round 15 % (as measured for the topside mirrors).

The waveguide propagation loss α is measured using different methods. The wafer used for the first hybrid module realization has a average propagation loss for deep etched waveguides of 5.8±0.5 dB/cm before and 4.4±0.4 dB/cm after the integration process. This improvement is explained by the added BCB layer covering the sidewalls, which reduces the impact of roughness due to a lower refractive index contrast. The InP wafer from the second generation shows an improved waveguide propagation loss of 3.3±0.3 dB/cm indicating that the first generation suffered during the foundry process. The characterization of an AWG shows that the general performance is comparable, but that the channel spacing is reduced after the integration process. This is due to the change of optical path length from the thermal expansion during the bonding process. This can be compensated in the design phase.

Characterized active components are the DFB, EAM and PIN PD, which are mainly measured after the integration process to reduce the risk of demanding the photonic wafer before processing. For the optical coupling the SSC BB is used. This component suffered in particular from the integration process. Part of its epitaxial layer stack has been removed, resulting in a smaller mode field diameter. Additionally the InP facet is sealed with a rough and polluted BCB layer, which is a leftover of the singulation process. Both effects result in a high optical coupling insertion loss of 6 dB.

Before the integration process the DFB lasers operated within the foundry specifications, but are compromised by the vertical mirror coupling scheme. After the integration process the DFB lasers are only operating in pulsed current mode. Further analysis shows a clear temperature limitation, which is quantified with thermal impedance value of 10400 K/W. However, a "burn in" mechanism has been discovered enabling CW operation after applying an 150 mA current for 20 sec. This resulted in a reduction of the thermal impedance to 660 K/W, which is still nearly 10 times larger than the pre-processing value of 71 K/W. However, for the different laser structures an average CW output power of 48 μW (in fibre) with a standard deviation of 30 μW is measured using injection currents up to 45 mA. For larger currents the thermal roll-over limits lasing operation. The laser structures with additional thermal heat sinking showed larger operation current regions, indicating a thermal impedance of 500 K/W. This confirms that better temperature control results in improved performance.

The EAM and PIN PD are only characterized after the integration process. Both are operating. The EAM has a maximum static extinction ratio of 23 dB and the PIN PD has a responsivity of 1.12±0.01 A/W. The measured dark currents for these two BB is much larger than expected, which could result from a poor initial device quality, a missing passivation layer or the integration process. Subsequent measurements on a none boded PD, which has been stored for more than a year, shows a dark current of around 3 mA at -0.5 V, indicating either a poor device quality or a degradation due to the missing passivation. A complete explanation has not been found yet and needs further research. The high speed characteristics are determined with small signal response measurements. The PIN PD achieved a 3 dB bandwidth for of 27.5 GHz and the EAM reaches a value of 16.5 GHz. Both are below the expected values , which can be explained by the RC limitation. In case of the PD the capacity increased due to a significant enlargement of the contact pads and a related distance reduction. For the EAM the resistance increased dramatically, which is not explained yet.

For the demonstration of the hybrid integration technology a receiver and transmitter module are realized. The fabricated electrical interconnects demonstrate a 3 dB bandwidth of more than 67 GHz, which is limited by the measurement equipment and includes the on chip transmission lines[1]. The hybrid receiver module has been packaged on a PCB[2]. A data experiment has been performed demonstrating an open eye diagram at 10 Gbit/s[3]. Higher bit rates could not be demonstrated, due to a bandwidth limitation resulting form a design mistake within the EIC, which can be solved by adding a decoupling capacitor to the design. Nevertheless, the receiver module showed no process related performance limitation. A data transmission experiment for the transmitter is not possible, because the operation point of the EAM BB shifted to higher voltages that can not be supplied by the integrated EAM driver. The reason for this shift is not completely explained. It can result from an additional resistance splitting the applied voltage, or it could be based on a reduce bandgap overlap between the emission wavelength of the DFB laser and the absorption of the EAM. This can occur due to an increased laser temperature, which leads to a shift of its emission wavelength towards higher values. To demonstrate the photonic design of the transmitter an integrated test circuit is used to perform a data transmission experiment, resulting in open eye diagrams up to 25 Gbit/s and a BER of 3E-9 for 12.5 Gbit/s NRZ with a receiver input power of 0 dBm.

All-in-all, this work successfully demonstrates a 3-D wafer level integration technology for PICs and EICs. Some limitations have been indicated, which will require additional research. However, the demonstrated process offers a scalable approach that gives the designer the freedom of placing the electrical interconnects at any position, enabling high speed connections between EIC and PIC. The circuits can also be adapted towards the required impedances, thereby opening the opportunity of energy efficient modules. The technology is platform independent, which means that in principle any EIC and PIC foundry process can be used, with only minor adaptations.

6.2 Outlook

The work presented in this thesis demonstrates a feasible integration technology. It became clear that several aspects need to be further investigated to improve the overall performance and to create a better understanding of the technology limitations. In this section the open questions are explained and design and technology improvements are proposed.

The CW operation of the DFB laser after bonding has been achieved by performing a "burn in" step, which leads to an improvement of the thermal impedance. It is concluded that the interface between the new metal layer and the InP contact pads melted and therefore provide a better thermal conductivity. However this appears to have an effect on the VI characteristic of the device as well. The initial characterizations do not show a conclusive result. Therefore an expansion to more measurements is needed, which could provide statistical evidence. The dark current of the PD and the leakage current of the EAM are much higher than expected and it is not completely clear if these parameters are affected negatively by the integration process. However, since it has been demonstrated that DC measurements can be performed on wafer level before the integration process, it is important to characterize the electrical performance of these BBs at this state. This can also give more insight into the shift of the EAM operation voltage point.

To improve future characterization a simple addition of cell identifiers should be added to the backside of the InP membrane before the singulation step. By this it would be possible to

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[1] These measurements have been performed by Xi Zhang and are reported in [21]

[2] Designed by Gertjan Coudyzer

[3] Performed by Gertjan Coudyzer

identify the origin of the characterised cell, and thus compare the measured devices before and after the integration process.

To improve the performance of the hybrid transmitter modules it is important to reduce the laser temperature by applying the intended top side cooling element. So far this has not been realized. An alternative would be to package the chip to include the designed double side cooling, or to use a probing tool which cools the tip of its probe and can therefore be used to extract the heat from the photonic part of the transmitter module. The EAM driver design should have a wider bias point range to allow for fabrication variations and still guarantee a working device. This flexibility will however reduce the power efficiency of the EIC and should therefore be optimised continuously in future designs, where fabrication control of the EAM will improve.

To optimally use the now integration technology the malfunction of the wafer bonder has to resolved. Based on the fact that a wafer shift only appears along one axis, and that it was not seen at the beginning of the process development, indicates that it results from an imbalance in the used clamping mechanism. After adapting the clamp force the bonding uniformity has to be verified, using a bond stack with one transparent wafer, to document the wafer alignment for each step of the bonding process. Another improvement of the integration technology is the adaptation to the InP membrane expansion within the design files. Thereby it is important to include marker structures for the wafer to wafer alignment and for the post processing. In this work it has been doubted if the device are sufficiently passivated. This has to be further analysed in order to design an appropriate process flow for achieving optimal passivation.

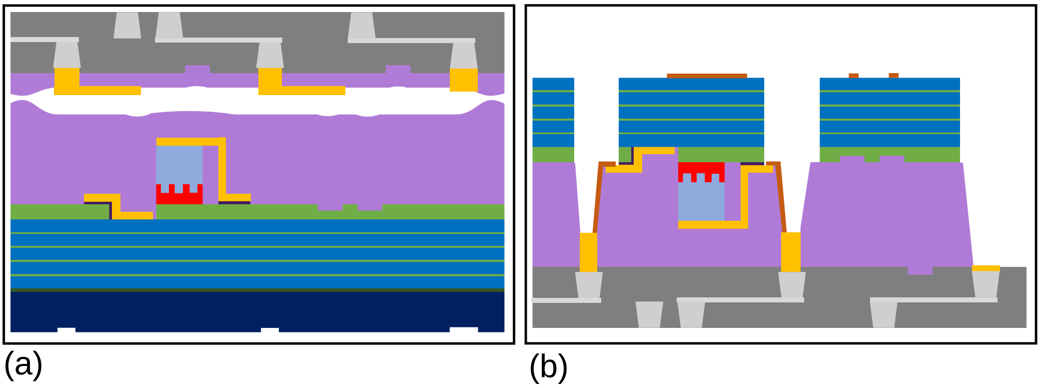

Figure 6.1: Schematic cross section of the proposed technology adaptation, (a) showing the metal routing on top of the BCB layer, (b) presenting the final hybrid device with reduced BCB etch depth

Developing this technology towards a higher density of electrical interconnects would be beneficial. It is mainly limited by the dimensions of the BCB sidewalls, which depend only on the angle and the polymer thickness. The angle depends on the seed layer deposition technique and could be reduced by stepping over to an ALD process. The BCB thickness derives purely from the topology. A schematic of a concept to reduce the relative BCB thickness is presented in figure 6.1. In figure 6.1 (a) the BiCMOS and InP wafer are planarized with BCB. The polymer on the electronic wafer has been pre-cured, which enables pattern definition within the polymer. The created pattern is afterwards filled with plated gold, resulting in a planarized surface with the electronic metal pads extended to the top of this layer. After bonding the wafer stack the distance from the photonic membrane to the metal interfaces is reduced, which improves the possible electrical interconnect density. A schematic of the resulting structures is presented in figure 6.1 (b). An additional advantage of this approach is the possibility to create routing layers on top of the soft cured BCB layer, which improves the design freedom. The metal pillar in the soft cured polymer can also be used to create a thermal connection which can be used to extract heat from the InP membrane towards the Si wafer.

The InP facets of the SSC are covered with BCB after the first hybrid module fabrication. This polymer layer incorporates debris and shows roughness, due to the sawing process. It would be beneficial to remove this layer afterwards. A wet chemical solution must be excluded, as it would dissolve all BCB and therefore disconnect the photonic and electronic chips. An alternative is a dry etch process which is either strongly isotropic, so that the vertical etch reduces the physical effect of the plasma on the SSC layer stack, or by using a mask to protect the wafer during the dry etch process. This mask layer has to be processed just before the singulation.

To increase the yield of the integration technology it is necessary to step over to single project wafers from the electronic foundry. In that case the fundamental reticle size can be optimized to increase the amount of devices per wafer. An alternative is the reconstruction of a Si wafer. For this the designed circuits must be delivered as single chips. By placing these chips on a Si carrier a reconstructed Si wafer can be obtained. This process would offer a cost effective way of combining photonic and electronic devices.

Appendix A

IR-wafer shine through technique

The key for the wafer scale integration is the wafer-to-wafer alignment. Connecting the photonic and electronic ICs electrically can only be achieved if both structures are placed with sufficient lateral precision on top of each other. How accurate that alignment has to be depends on the dimensions of the interconnect pads. This can be adapted within the limitations of the foundry to fulfil the requirements. Thereby smaller dimensions will demand stricter tolerances. In section 3.2 the used backside alignment process is presented, which was enabled by the investment into a wafer bonder and aligner. In [34] an overview of different wafer-to-wafer alignment techniques is presented. Initially the IR shine through technique has been studied to align the two wafer too each other. The gained knowledge is presented within this appendix.

The shine through technique makes use of an IR light source. The emitted light should travel trough the two wafers and be detected on the other side. Therefore marker structures on both wafers become visible and can be used for the alignment. This technique has the advantage that it can be performed in-situ in the bonding chamber. However, the light can only travel through non-absorbing materials. The epitaxial layers used for active components will absorb light with a wavelength below 1550 nm. Also indium gallium arsenide (InGaAs), which is often used as etch stop layer for the substrate removal blocks short wavelengths (<1650 nm). The active area only constitutes a small fraction of the full 3 inch wafer. Therefore alignment features could be placed outside these areas. The InGaAs etch stop layer can be replaced by a quaternary material ($In_{1-x}Ga_xAs_yP_{1-y}$) to allow transmission of shorter wavelengths. Thereby it is important that the composition of the edge stop layer is not too close to InP, otherwise the chemical selectivity is too small and this layer will be resolved during the wet chemical etching of the substrate. Different quaternary material compositions are tested and it is found that a Q1.25 layer will provide sufficient selectivity to act as an etch stop layer. The term Q1.25 refers to a band gap of 0.992 eV[1] corresponding to a photon wavelength of 1.25 µm. Each quaternary composition $In_{1-x}Ga_xAs_yP_{1-y}$ with a smaller band gap then 0.992 eV will be suitable as an etch stop layer, but will also absorb a larger part of the IR spectrum used for alignment. Another limitation of the shine through technique is the susceptibility to scattering effects. Rough surfaces of the InP or Si wafer will compromise the achievable resolution and therefore reduce

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[1] $E = \frac{h\nu}{\lambda} \equiv E(\text{eV}) = \frac{1.24}{\lambda(\mu m)}$

the alignment accuracy. Polished substrates would be needed. The expected alignment accuracy is in the order of 10 μm [34]. An initial test is performed to judge the capability of our equipment and the intended materials. In figure A.1 the result of this initial test is presented. It shows two sets of markers with figure (a) and (b) showing images from two detectors, which are laterally separated by 65 mm. An InP wafer and a silicon wafer are used. Both are double side polished. A layer of SiN_x is deposited on each wafer in which the pattern, a cross, is etched. In figure A.2 the marker dimension and position on the wafer are indicated. These markers can be identified in figure A.1, but the contrast is limited. Furthermore the right detector (A.1 (b)) shows a large alignment mismatch of the structures. This is due to the fact, that the alignment process has not been optimised during this experiment. For an InP and silicon wafer the achieved visibility result is acceptable. An uncertainty that remains is the IR transparency on the BiCMOS material. It was predicted that the dicing lanes of the electronic wafer consist of pure silicon and dielectrics, which should provide a transparent window for the alignment. Testing an actual BiCMOS wafer however disproved this assumption. No IR light could be detected, through these lanes, as apparently the metal layers in the BiCMOS extend into them. Therefore the IR shine through technique is concluded not to be suitable for the intended purpose.

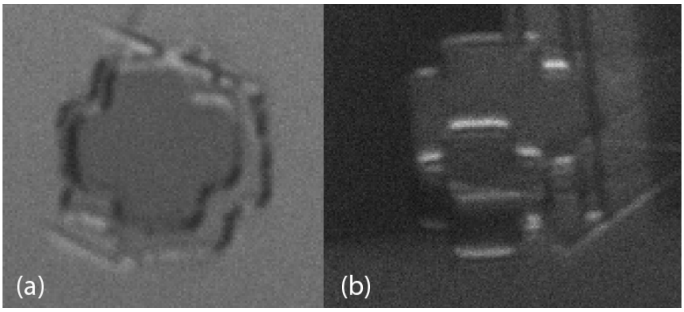
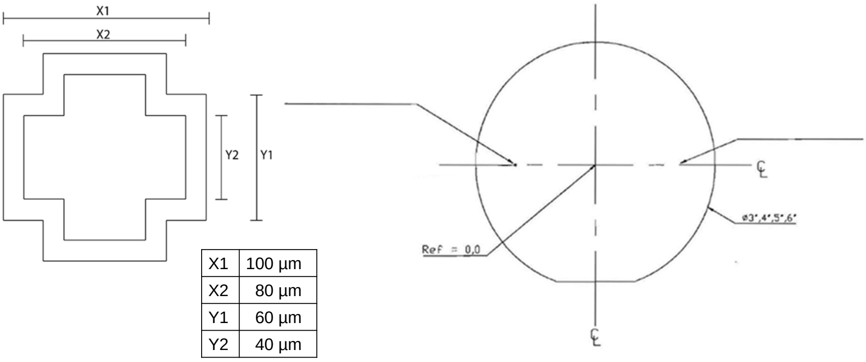


Figure A.1: In-situ detector image of the IR shine through for an InP and Si wafer



X1	100 µm
X2	80 µm
Y1	60 µm
Y2	40 µm

Figure A.2: Alignment marker recommendation from the supplier [63]

Appendix B

Process Flow

step	wafer	task/tool/description	remarks
1	InP top	cleaning surface with N_2 piston	repeat step 1 to 3 until surface is cleaned from dusk particles
2	InP top	cleaning wafer in isopropanol (IPA)	
3	InP top	cleaning surface with N_2 piston	
4	InP top	microscope inspection	
5	InP top	250 Watt O_2 plasma 2x 10 min 50 °C	to clean the surface
6	InP top	rinsing in water	
7	InP top	primer oven HMDS	
8	InP top	spinning thick AZ resist AZ 9260 @ 1500 rpm; 60 sec; 4+ ml	
9	InP top	place on hotplate @ 90 °C for 5 min change temp of hotplate to 120 °C	
10	InP top	hard bake 120 °C for 120 min	
11	InP top	change temp of hotplate to 20 °C wait until temp =< 30 °C	≈ 60 min
12	InP back	250 Watt O_2 plasma 2x 10 min 50 °C	cleaning backside
13	InP back	ICP-CVD 120 nm SiO_2	
14	InP back	rinsing in water	
15	InP back	primer oven HMDS	
16	InP back	spinning AZ 701 1.5 ml 3000 rpm	
17	InP back	soft bake 90 °C 3 min	
18	InP back	EVG aligner for lithography	
19	InP back	development MIF-D 726 pure 90 sec	
20	InP back	microscope inspection	use yellow light only
21	InP back	hard bake 110 °C 3 min	
22	InP back	RIE 7 min; CHF_3:O_2 50:5 sccm	etch rate is ≈ 30 nm/min
23	InP back	250 Watt O_2 plasma 2x 10 min 50 °C	
step	wafer	task/tool/description	remarks

step	wafer	task/tool/description	remarks
24	InP back	step height measurement SiO_2 =	these steps are optional, SiO_2 can be kept as alignment mask
25	InP back	ICP etch standard 5 cycle	
26	InP back	250 Watt O_2 plasma 2x 10 min 50 °C	
27	InP back	step height measurement $O_2 + InP =$	
28	InP back	RIE 7 min; CHF3:O2 50:5 sccm	
29	InP back	250 Watt O_2 plasma 2x 10 min 50 °C	
30	InP back	microscope inspection	
31	InP top	1000 Watt O_2 plasma 2x 10 min 50°C	remove resist from topside
32	InP top	diluted H_3PO_4 (10%) 2min	
33	InP top	ICP-CVD 50 or 120 nm SiO_2	
34	BiCMOS top	receive 3 inch BiCMOS wafer with photoresist as protection layer	
35	BiCMOS top	Acetone + IPA both for 5 min	
36	BiCMOS top	ICP-CVD 50 or 120 nm SiO_2	
37	BiCMOS top	outgassing; 1 h; 240 °C; N_2 atmosphere	
38	BiCMOS top	spinning AP 3000 (0.5 ml): 1 sec; 500 rpm; acc 2.5k 60 sec; 2000 rpm; acc 5k	
39	BiCMOS top	hotplate 135 °C for 5 min	
40	BiCMOS top	spinning BCB 3022-57 (2-3 ml): 1 sec; 500 rpm; acc 2.5k 60 sec; 2000 rpm; acc 5k	BCB thickness > 2x topology 3022-57 @ 2000 rpm ≈ 7.5 μm
41	BiCMOS top	hotplate 100 °C 5 min	"soft bake"
42	BiCMOS top	EVG bonder BCB cure 175 °C 1 h	"pre cure"
43	InP top	outgassing; 1 h; 240 °C; N_2 atmosphere	
44	InP top	spinning AP 3000 (0.5 ml): 1 sec; 500 rpm; acc 2.5k 60 sec; 2000 rpm; acc 5k	
45	InP top	hotplate 135 °C for 5 min	
46	InP top	spinning BCB 3022-63 (4 ml): 1 sec; 500 rpm; acc 2.5k 60 sec; 2000 rpm; acc 5k	BCB thickness > 2x topology 3022-63 @ 2000 rpm ≈ 16 μm
47	InP top	hotplate 100 °C 5 min	"soft bake"
48	BiCMOS top	take out BiCMOS wafer	
49	wafer stack	wafer aligner: BSA wafer alignment use overlay methode	load BiCMOS first
step	wafer	task/tool/description	remarks

step	wafer	task/tool/description	remarks
50	wafer stack	bonding 240 °C; 10 h; 700 N	use glass pressure disc
51	Bond	remove bonded wafer stack from bonder	
52	Bond	RIE O_2:CHF_3; 20:4 sccm; 50 mTorr 240 min	
53	Bond	HCl:H_2O (4:1) @ 35 °C, 750 ml total volume; 25 min	bond parallel to table;
54	Bond	RIE O_2:CHF_3; 20:4 sccm; 50 mTorr 240 min	
55	Bond	HCl:H_2O (4:1) @ 35 °C, 750 ml total volume; 25 min	until solved completely
56	Bond	$H_2O/H_2SO_4/H_2O_2$ (10:1:1) total volume H_2O = 300 ml	Q1.3 etch stop layer etch time ≈ 3 min; colour change add 30 sec
57	Bond	ICP-CVD 120 nm SiO_2	
58	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
59	Bond	rinsing in water	
60	Bond	primer oven HMDS	
61	Bond	spinning AZ 701 1.5 ml 3000 rpm	
62	Bond	soft bake 90 °C 3 min	
63	Bond	EVG aligner for lithography	
64	Bond	development MIF-D 726 pure 90 sec	
65	Bond	microscope inspection	use yellow light only
66	Bond	hard bake 110 °C 3 min	
67	Bond	RIE 7 min; CHF_3:O_2 50:5 sccm	etch rate is ≈ 30 nm/min
68	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
69	Bond	diluted H_3PO_4 (10%) 2min	
70	Bond	step height measurement $SiO_2 =$	
71	Bond	ICP etch standard X cycle	calculate amount of cycle
72	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
73	Bond	diluted H_3PO_4 (10%) 2min	
74	Bond	step height measurement $InP + SiO_2 =$	
75	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
76	Bond	diluted H_3PO_4 (10%) 2min	
77	Bond	RIE 7 min; CHF_3:O_2 50:5 sccm	
78	Bond	microscope inspection	
79	Bond	step height measurement $InP =$	
80	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
step	wafer	task/tool/description	remarks

step	wafer	task/tool/description	remarks
81	Bond	rinsing in water	
82	Bond	primer oven HMDS	
83	Bond	Spinning AZ 9260 4 ml; 1500 rpm; acc 2500; 60 sec	
84	Bond	hotplate 110 °C; 80 sec	soft bake
85	Bond	Spinning AZ 9260 4 ml; 1500 rpm; acc 2500; 60 sec	
86	Bond	hotplate 110 °C; 160 sec	
87	Bond	10 min waiting time	rehydration of photoresist
88	Bond	EVG aligner for lithography	
89	Bond	10 min waiting time	
90	Bond	Development AZ400k:H_2O 1:4 (150ml: 600ml); 4 min	4 inch beaker; wafer parallel to the table; constant movement
91	Bond	RIE 150 min; CHF_3:O_2 50:5 sccm	use yellow light only
92	Bond	no hard bake !	
93	Bond	step height measurement *photoresist* =	≈ 24 μm
94	Bond	RIE O_2:CHF_3; 20:4 sccm; 50 mTorr 150 min	
95	Bond	Aceton + IPA 4 min each	
96	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
97	Bond	rinsing in water	
98	Bond	primer oven HMDS	
99	Bond	Spinning AZ 9260 4 ml; 1500 rpm; acc 2500; 60 sec	
100	Bond	hotplate 110 °C; 80 sec	soft bake
101	Bond	Spinning AZ 9260 4 ml; 1500 rpm; acc 2500; 60 sec	
102	Bond	hotplate 110 °C; 160 sec	
103	Bond	10 min waiting time	rehydration of photoresist
104	Bond	EVG aligner for lithography	
105	Bond	10 min waiting time	
106	Bond	Development AZ400k:H_2O 1:4 (150ml: 600ml); 4 min	4 inch beaker; wafer parallel to the table; constant movement
107	Bond	RIE 150 min; CHF_3:O_2 50:5 sccm	
108	Bond	no hard bake !	
109	Bond	step height measurement *photoresist* =	≈ 24 μm
110	Bond	RIE O_2:CHF_3; 20:4 sccm; 50 mTorr 150 min	
111	Bond	Aceton + IPA 4 min each	
step	wafer	task/tool/description	remarks

step	wafer	task/tool/description	remarks
112	Bond	250 Watt O_2 plasma 2x 10 min 50 °C	
113	Bond	diluted H_3PO_4 (10%) 2min	
114	Bond	rinsing in water	
115	Bond	metal evaporation angle 3 inch wafer holder by 45 ° metals: 50 nm Ti + 100 nm Au	
116	Bond	spinning AZ 701 14 cp 3.5 ml @ 1000 rpm	for AZ 701 14 cp: repeat 3 times for AZ 701 29 cp: repeat 2 times
117	Bond	hotplate 100 °C 3 min	
118	Bond	edge bead removal (EBR)	to remove plating ring
119	Bond	EVG aligner for lithography	
120	Bond	development MIF-D 726; pure; 120 sec	
121	Bond	microscope inspection	use yellow light only
122	Bond	hotplate 120 °C; 20 min	
123	Bond	RIE O_2 20 sccm; 15 mTorr; 10 sec	
124	Bond	step height measurement *photoresist* =	
125	Bond	rinsing water (part of plating)	
126	Bond	electro plating for 15 min set current to 1.5mA/openArea[cm^2]	calculate open area before
127	Bond	step height measurement *photoresist* =	calculate plating rate
128	Bond	rinsing water (part of plating)	
129	Bond	electro plating set current to 1.5mA/openArea[cm^2]	calculate time with measured electro plating rate
130	Bond	step height measurement *photoresist* =	verify Au thickness
131	Bond	Aceton + IPA	as long as needed as short as possible
132	Bond	RIE O_2 20 sccm; 15 mTorr; 2 min	
133	Bond	microscope inspection	
134	Bond	KCN etch ≈ 20 sec	colour change
135	Bond	Spinning MAN 440 2 ml; 2000 rpm	
136	Bond	hotplate 120 °C 20 min	
137	Bond	edge bead removal (EBR)	minimal 3x; open Au plating ring
138	Bond	KCN etch	
step	wafer	task/tool/description	remarks

step	wafer	task/tool/description	remarks
139	Bond	RIE O_2 20 sccm; 15 mTorr; 1 min	
140	Bond	Aceton + IPA	as long as needed as short as possible
141	Bond	RIE O_2 20 sccm; 15 mTorr; 1 min	
142	Bond	oxalic acid, Ti etch	
143	Bond	step height measurement *Au* =	
step	wafer	task/tool/description	remarks

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Acknowledgments

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Curriculum Vitae

Marc Spiegelberg was born on the 21st of February 1989, in Frankfurt (Oder), Germany. After finishing school he helped as a civil servant for nine months at the national park "Märkische Schweiz". He proceeded with university studies and received the Bachelor of Science degree in Physics from the Berlin University of Technology in 2012. His bachelor thesis was carried out in cooperation with the Fraunhofer Institute for Telecommunications, Heinrich Hertz Institute (HHI), where he worked during his studies as a research assistant. The topic of his bachelor thesis is the design of a characterization setup for InP-based high power BA-laser. During his studies Marc volunteered as a firefighter, fulfilling the rank of a squad leader, educating new recruits.

In 2015 he completed his studies at the Berlin University of Technology with a Master of Science degree in applied Physics. The research of his master thesis was performed in the group of Prof. Bimberg and co-supervised by Prof. Hoffmann on the topic of high-frequency pulse emission of mode-locked GaAs-based quantum dot lasers.

In January 2016, he started his PhD research in the Photonic Integration group (PhI) at Eindhoven University of Technology (TU/e), the Netherlands. His work focuses on the subject of wafer scale integration of photonics and electronics. The results of this research are presented in this thesis. Currently he is working as a Postdoctoral researcher in the Electro-Optical Communication group (ECO) at the TU/e on the topic of programmable photonics.

List of Publications

W. Yao; X. Liu; M. Matters-Kammerer; A. Meighan; **M. Spiegelberg**; M. Trajkovic; J.J.G.M. van der Tol; M.J. Wale; X. Zhang K.A. Williams *Towards the integration of InP photonics with silicon electronics: design and technology challenges.* In: Journal of Lightwave Technology (accepted)

Y. Jiao; N. Nishiyama; J. van der Tol; J. van Engelen; V. Pogoretskiy; S. Reniers; A.A. Kashi; Y. Wang V.D. Calzadilla; **M. Spiegelberg**; Z. Cao; K. Williams; T. Amemiya; S. Arai; *InP membrane integrated photonics research.* In: Semiconductor Science and Technology, vol. 36, no. 1, art. no. 013001, 2020

K.A. Williams; X. Liu; M. Matters-Kammerer; A. Meighan; **M. Spiegelberg**; J.J.G.M. van der Tol; M. Trajkovic; M.J. Wale; W. Yao; X. Zhang; *Indium Phosphide Photonic Circuits on Silicon Electronics.* In: Optical Fiber Communication Conference (OFC), OSA Technical Digest (Optical Society of America), paper M3A.1, 2020

M. Spiegelberg; J.P. van Engelen; K.A. Williams; J.J.G.M van der Tol; *Wafer scale technology to integrate photonics on BiCMOS electronics.* In Proceedings Symposium IEEE Photonics Society Benelux, Amsterdam, 2020

X. Zhang; X. Liu; **M. Spiegelberg**; A. R. van Dommele; M. K. Matters-Kammerer; *A DC-51.5 GHz Electro-Absorption Modulator Driver with Tunable Differential DC Coupling for 3D Wafer Scale Packaging.* In: IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), Nashville, TN, USA, pp. 1-4., 2019

X. Zhang; X. Liu; **M. Spiegelberg**; A. Meighan; J.J.G.M. van der Tol; M.K. Matters-Kammerer; *A 50 Gb/s PAM-4 Optical Modulator Driver for 3D Photonic Electronic Wafer Scale Packaging.* In: 18th Mediterranean Microwave Symposium (MMS) Istanbul, pp. 112-115, 2018

M. Spiegelberg; J. van Engelen; T. de Vries; K.A. Williams; J.J.G.M. van der Tol; *BCB bonding of high topology 3 inch InP and BiCMOS wafers for integrated optical transceivers.* In: Proceedings Symposium IEEE Photonics Society Benelux, Brussels pp. 160-163, 2018

M.B.J. van Rijn; M.K. Smit; **M. Spiegelberg**; S. Paredes; *Heat sinking of highly integrated photonic and electronic circuits.* In: Proceedings Symposium IEEE Photonics Society Benelux, Delft, 2017

M. Spiegelberg; M.P.A. Verhaegh; M.B.J. van Rijn; J. Bolk; L.M. Augustin J.J.G.M van der Tol; *Integrated polarization filter for 1550 nm based on a narrow waveguide section.* In: Proceedings Symposium IEEE Photonics Society Benelux, Delft, pp. 144-147, 2017

M. Spiegelberg; A.D. La Porta; B.J. Offrein; V.M. Dolores Calzadilla; J.J.G.M van der Tol; K.A. Williams; *Optical coupler concept for wafer scale fabrication of adhesively bonded photonic end electronic circuits.* In Proceedings of the 21st Annual Symposium of the IEEE Photonics Society Benelux Chapter, Gent, Belgium, pp. 215-218, 2016