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Abstract

The paper proposes a robust and ultra-fast short circuit detection method based on the voltage dip in the half-bridge due to the presence of stray inductance. Results show that the short circuit is detected in less than 100ns, which is a promising solution against the Fault Under Load due to Single-Event Burnout failure type.

1   Introduction

In recent years, there has been a growing concern about vehicle road comfort and safety. On the suspension level, these requirements translate to the usage of electromagnetic (EM) suspension, as it can respond to the road condition quickly. However, the inverter used in the EM suspension poses a problem, namely the possible failure of the power switches [1]. One of the most probable failure types that can happen in the system is a short circuit in one of the converter's Half-Bridges (HB) which is illustrated in **Figure 1**. It is necessary to have a robust and fast short circuit detection to prevent further damage and fault propagation in the system,. In literature, some short circuit detection schemes such as desaturation circuit, current sensing, *di/dt*, and gate voltage sensing have been proposed [2]. Among these schemes, the desaturation circuit is the most widely used solution as it is easy to implement and uses a voltage measurement, which does not insert any resistive or inductive component in the power loop. However, this circuit needs a certain blanking time to avoid a false alarm, which slows down the detection time [3]. Also, this circuit is not very robust as the performance depends on the saturation voltage characteristic of the switch, which varies according to the junction temperature [4].
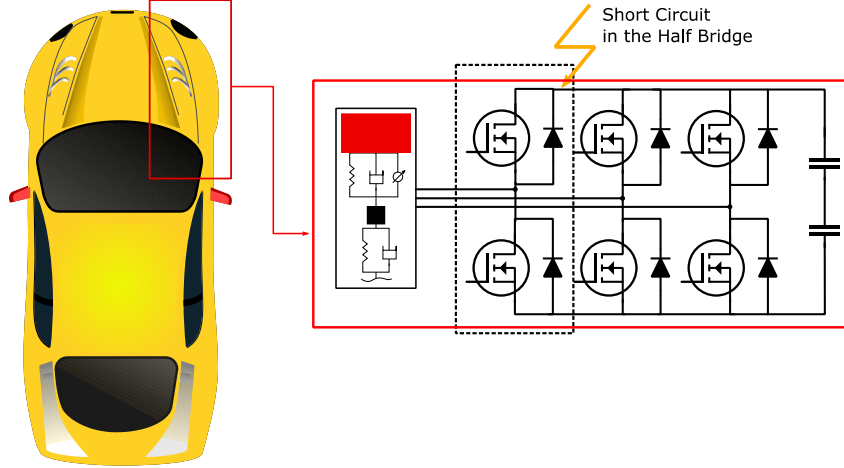
Figure 1 The top view representation of a car. On each corner, the EM suspension is installed with the configuration as shown in the circuit on the right.

This paper proposes a method for robust and ultra-fast short circuit detection at Fault Under Load (FUL). FUL appears when a MOSFET switch is shorted by an unintended turn-on of the complementary switch in an HB [5]. The method described here is intended to detect the most challenging situation, that is, a FUL due to Single-Event Burnout (SEB). SEB happens because of secondary cosmic particles that hit a power switch when it is blocking [6]. It causes deposition of tens to several hundreds of MeV energy over a few micrometers distance and happens in less than one nanosecond [7]. This paper proposes an indirect short circuit detection by measuring the HB voltage-dip during a short circuit due to the stray inductance (L_σ) between the DC-Link capacitor and the HB. This method is dubbed as Stray Voltage Capture (SVC). As it is impractical to measure the voltage across L_σ, the HB voltage is measured instead. A High Pass Filter (HPF) is used for passing through the voltage dip and filter out the DC component. Additionally, a Low Pass Filter (LPF) is implemented to avoid a false-triggering alarm during the HB switching transition.

In order to show the merits of SVC, some key performance indicators (KPI's) are compared with those from the other short circuit protection methods from reference [11]. This comparison is shown in **Table 1**.

Table 1 Comparison of KPI's between existing and proposed short circuit detection method

Methods	Parameter	Detection Time	Detecion Level	Comments
Current Mirror	I_{ds}	~100ns	Device Protection	Expensive, not all devices have a port for current mirror
Source Current Detection by resistor	I_{ds}	~100ns	Device Protection	Increases resistive loss and parasitic inductance in Power Loop
Source Current Detection by Rogowski Coil	I_{ds}	~100ns	Device Protection	Expensive
Desaturation Circuit	V_{ds}	~1µs	Device Protection	Depend on the device saturation voltage characteristics
Desaturation Circuit with adaptive blanking time	V_{ds}	~250 ns	Device Protection	Many additional components (reducing robustness), Adaptive with the changing of the transistor
Gate Driver Voltage Sensing	V_{ds}	~100ns	Device Protection	Needs Two Op-Amps and a Logic Circuit for Ignoring Switching transient
Stray Voltage Capture (Proposed Solution)	V_{dsds}	<100ns	Subsystem Protection	Use LPF and HPF for capturing voltage dip.

From table 1, it can be seen that the SVC method is superior in the term of detection speed. Therefore, SVC is suitable for detecting a Single-Event Burnout as will be discussed further in section III. Furthermore, SVC detects the short circuit from a subsystem point of view, that is, for a Half-Bridge. Hence, the SVC implementation reduces the circuit cost as it only needs three protection circuits for a 3-phase system.
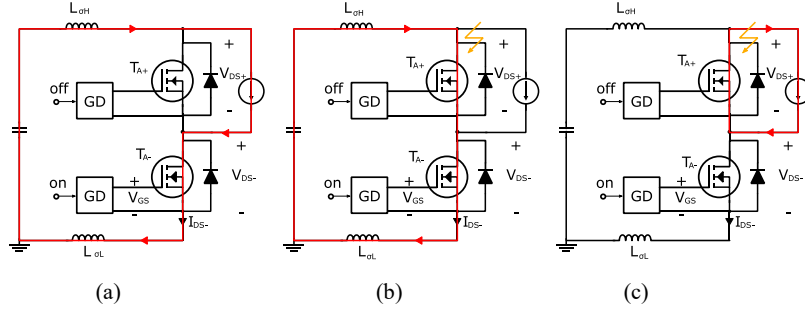
2 Fault Under Load and Single Event Burnout

Figure 2 A sequence of FUL in a Half-Bridge (a) TA- is already on and is conducting the load current (b) The unintended turn on of TA+ causing the short circuit to happen (c) TA- is turned off by the protection circuit after the short circuit has.

A MOSFET in an HB can be subjected to FUL/SEB, as illustrated in **Figure 2** A sequence of FUL in a Half-Bridge (a) TA- is already on and is conducting the load current (b) The unintended turn on of TA+ causing the short circuit to happen (c) TA- is turned off by the protection circuit after the short circuit has..Typical waveforms for this event are shown in **Figure 3a**. At t_1-t_2, the T_{A-} is already on and carrying a load current (I_{Load}). At t_1, a FUL happens when T_{A+} is unintentionally shorted by one of the short circuit failure mechanisms, as presented in [1]. In this stage, the drain-source current of T_{A-} increases very rapidly with L_σ being the only limiting factor until the MOSFET reaches its saturation at t_2. A rise in the V_{ds} of MOSFET T_{A-} leads to the rise of its V_{gs} through the Miller capacitance C_{gd}. As a consequence, the I_{ds} keeps increasing, and at some point, it will decline as the V_{gs} is going back to the normal on-state value. From t_2-t_4, the MOSFET reaches its saturation region. At t_4, the short circuit protection is triggered by the conventional detection, i.e., desaturation circuit, which discharges switches V_{gs} of T_{A-} to zero. This hard-switching turn-off gives an overvoltage spike in V_{ds} due to L_σ.

As depicted in **Figure 3b**, the I_{ds} of Si and SiC MOSFETs continues to increase with the rise of V_{ds} for a long time due to the large ohmic region. As a result, the short circuit withstands time of a MOSFET is in general lower than that of an IGBT. A SiC MOSFET can only sustain around 7μs during a short circuit event [8].
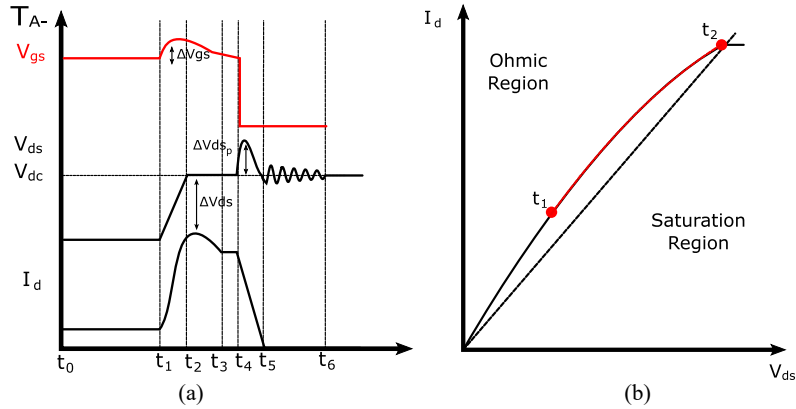
Figure 3 (a) MOSFET behavior at FUL by using conventional short circuit protection scheme, (b) MOSFET region during FUL/SEB event.

It is aforementioned that there is a voltage dip due to L_σ during the FUL/SEB event. The HB simulation during FUL/SEB is conducted in SPICE and illustrated in **Figure 4a**. Here, an ideal switch is used to mimic the SEB occurrence. **Figure 4b** shows the SPICE simulation of V_{dsds} with the variation of L_σ.

(a)   (b)
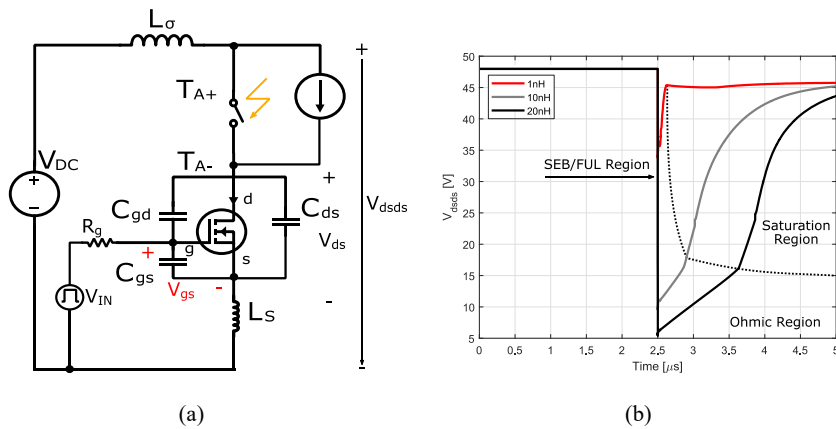
Figure 4 (a) The illustration of simplified HB during FUL/SEB event (b) SPICE simulation by varying Lσ and its detection region

From **Figure 4b**, the region of detection is divided into a SEB/FUL, an ohmic, and a saturation region. A higher value of L_σ gives a higher voltage dip magnitude in the SEB/FUL Region. Therefore, a minimum value of L_σ is necessary to achieve an optimum trade-off between the switching and detection performance. SVC is able

to detect a short circuit in the SEB/FUL region, with some uncertainty (ex: component-time delay). Thus, the SVC method guarantees the detection while the MOSFET is operating in the ohmic region.

3 Stray Voltage Capture Principle
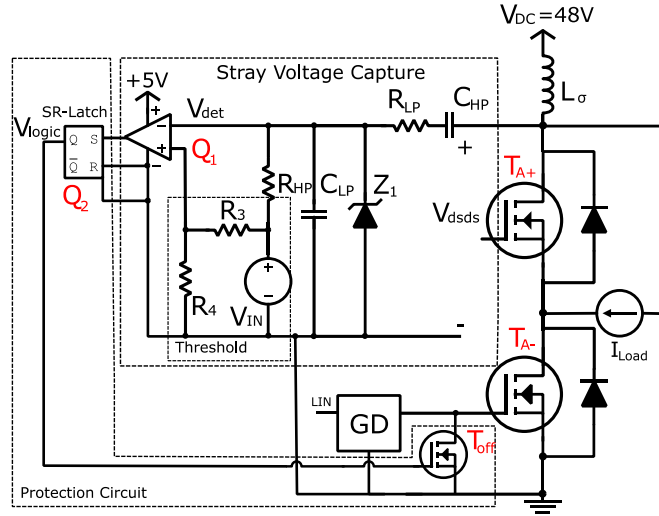
Figure 5 Stray Voltage Capture implementation for short circuit detection in a Half-Bridge

Figure 5 shows a possible circuit implementation of the SVC method as a combination of an HPF and a LPF, which together are realized by a two-port RC network. It consists of $C_{HP}, R_{HP}, C_{LP}, R_{LP}$. The output of the network is given an offset by V_{IN} to match the comparator input. The transfer function from the HB voltage measurement V_{dsds} to the network output V_{det} can be written as

$$V_{det} = \frac{s}{C_{LP}R_{LP}s^2 + \left(1 + \dfrac{C_{LP}}{C_{HP}} + \dfrac{R_{LP}}{R_{HP}}\right)s + \dfrac{1}{C_{HP}R_{HP}}}V_{dsds} + V_{IN} \qquad (1)$$

A Zener diode (Z_1) is placed in cascade with the RC network to protect the comparator from a huge undershoot of V_{det}. The SVC performance at SEB and FUL is examined in the SPICE environment, with the result as depicted in **Figure 6**.

Figure 6 The Waveform of Vds-, Vds+, Ids, and the logic output of SVC (a) during FUL (b) during SEB
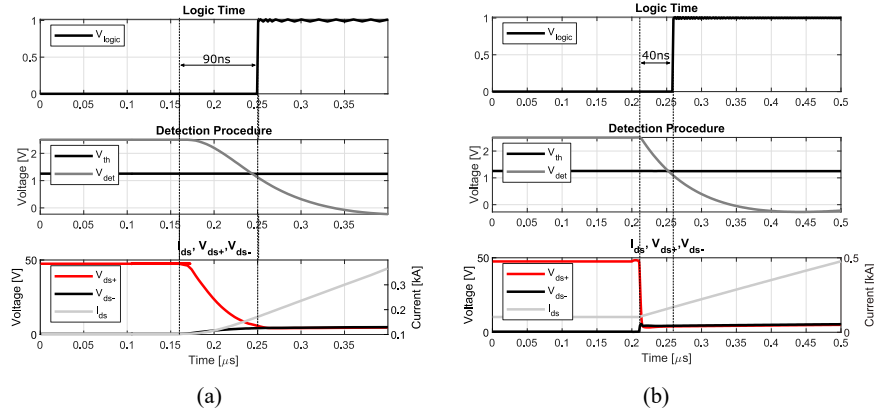
In the SPICE model, a-Si MOSFET 48V/180A IPB024N10N5 is used as an example. The SEB is realized by turning on an ideal switch located in parallel with T_{A+}. Meanwhile, a "normal" FUL is realized by turning on the gate driver logic input of T_{A+}, which is acting like a normal MOSFET. If a SEB or normal FUL occurs, the input signal of comparator V_{det} will become lower than V_{th}. The SPICE circuit parameters are listed in **Table 2**.

<div align="center">

Table 2 SPICE SVC Parameter Values

L_σ	30nH	R_{HP}	100Ω	Q_1	LT1721
V_{IN}	2.5V	C_{HP}	1nF	T_{off}	RJK005N03
R_{LP}	1kΩ	C_{LP}	1nF	Q_2	SN74LS

</div>

The signals in figure 6 show that the SEB and normal FUL are detected after 40 and 90 ns, respectively. It should be noted that the detection speed also depends on the comparator and SR-latch time delay. In this simulation, this time-delay is 6ns as an ultra-fast comparator (Q1) is used. The simulation of the full protection scheme during Single-Event Burnout is presented in **Figure 7**.
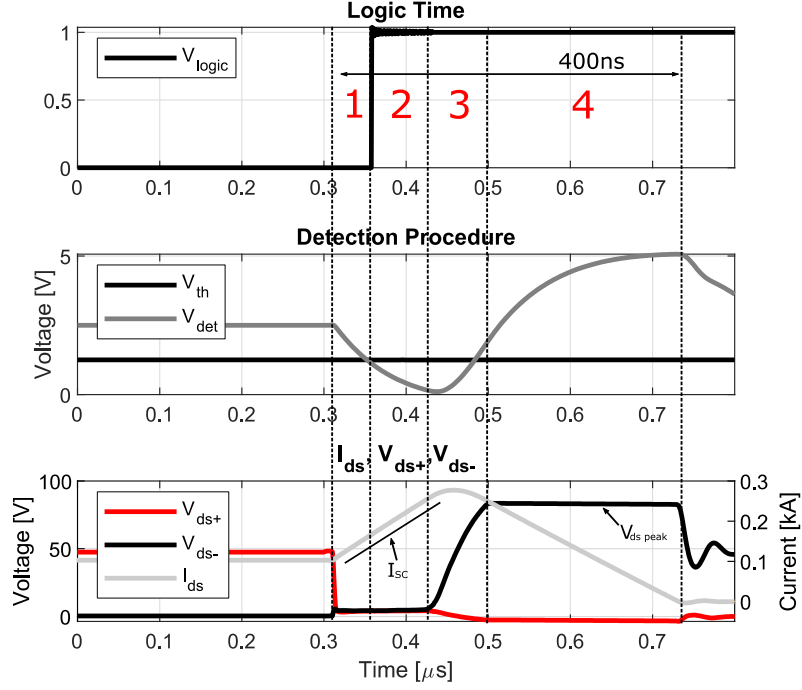
Figure 7 The protection of Single-Event Burnout which is divided into four working areas.

The signals in **Figure 7** show that the short-circuit protection scheme which works in the ohmic region of the switch is realized. The working area can be divided into four regions. The first region starts when a short circuit occurs which results in the rapid rise of current with L_σ is the limiting factor. Mathematically, the short circuit current is expressed as

$$V_{DC} = (L_\sigma + L_s)\frac{dI_{SC}}{dt} + 2R_{dson}I_{SC} = \frac{V_{DC}t}{L_\sigma + L_s}e^{-\frac{2R_{dson}t}{L_\sigma + L_s}} + I_{Load} \qquad (2)$$

where I_{sc} is the short circuit current of the HB, R_{dson} is the on-resistance of T_{A+} and T_{A-}, L_s is the stray inductance of the MOSFET source and I_{load} is the load current. The second region starts when the SVC detects the short circuit, there is an additional delay due to the protection circuit. Therefore, the current is still increasing, as formulated in (2). The total short circuit time (t_{total}) is therefore:

$$t_{delay} = t_{comp} + t_{latch} + t_{prot}, \quad t_{total} = t_{SC} + t_{delay}, \qquad (3)$$

where $t_{comp,}$, t_{latch} , t_{prot} are time delays due to comparator, SR-latch, and protection respectively. The third starts at T_{A-} where, as $V_{gs} < V_{TH}$, V_{ds} is still rising while I_{ds} already starts falling. The final region starts, where I_{ds} keeps falling until MOSFET is completely turned off and V_{ds-} starts its oscillating period. In this area, there is an overvoltage of V_{ds-} due to the energy stored in L_σ. Note that this overvoltage should be limited to prevent secondary breakdown of the MOSFET. During the I_{ds} current falling period, the behavior of the circuit **Figure 4a** is analytically modeled by using a similar technique as in [9] and [10], leading to:

$$V_{gs} = \left(\frac{I_{SC}(t_{total})}{g_{fs}} + V_{TH} \right) e^{\frac{-t}{T}} \left(\cos \omega t + \frac{\sin \omega t}{\omega t} \right), \text{ underdamped response} \qquad (4)$$

$$V_{gs} = \left(\frac{I_{SC}(t_{total})}{g_{fs}} + V_{TH} \right) \frac{1}{T_2 - T_3} \left(T_2 e^{\frac{-t}{T_2}} - T_3 e^{\frac{-t}{T_3}} \right), \text{ overdamped response} \qquad (5)$$

where

$$T = \frac{2A}{B}, \quad \omega = \sqrt{\frac{4A - B^2}{4A^2}}, \quad T_2 = \frac{2A}{B + \sqrt{B^2 - 4A}}, \quad T_3 = \frac{2A}{B - \sqrt{B^2 - 4A}},$$

$$A = R_g g_{fs} C_{gd}(L_\sigma + L_s), \quad B = R_g(C_{gs} + C_{gd}) + L_s g_{fs},$$

Here, R_g, C_{gs}, C_{gd}, g_{fs} are extracted from the MOSFET datasheet. The underdamped response occurs when $4A\text{-}B^2 \leq 0$ while overdamping occurs when $4A\text{-}B^2 > 0$. The V_{ds} overvoltage peak can be written as

$$I_{ds}(t) = g_{fs}(V_{gs}(t) - V_{TH}), \quad V_{ds\,peak} = \max\left(V_{DC} - (L_\sigma + L_s)\frac{dI_{ds}(t)}{dt} \right). \qquad (6)$$

4   Limitation of Stray Voltage Capture

As an example, consider a change of the LPF parameters from **Table 2**, with C_{LP} and R_{LP} are 330pF and 10 Ω respectively. Results of circuit simulation are shown in figure 8 for a normal HB switching transient.
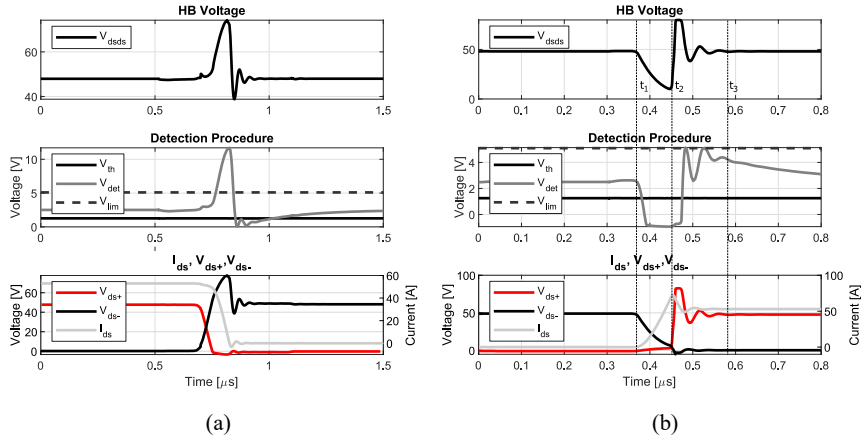

Figure 8 The limitation due to the switching transient (a) comparator input overvoltage, (b) false-triggering alarm.

Here, V_{lim} is the comparator input limit from the datasheet. From **Figure 8**, it is shown that too low LPF component values give catastrophic events in the SVC, namely, comparator input overvoltage and false-triggering alarm. The former occurs due to the overvoltage turn-off of T_{A-}. The latter could be analyzed from figure 8b. At t_1-t_2, the fault-alarm is triggered because of the V_{dsds} voltage dip during the hard commutation of the MOSFET T_{A+}. This makes the V_{det} fall and quickly surpass the V_{th}, which is clamped by the Zener diode (Z_1). At t_2, I_{ds} has a peak overshoot due to the T_{A+} body diode's reverse recovery. After t_2, there is an overvoltage turn-off of T_{A+}, which can harm the comparator. It is important to consider that the event depends on the I_{Load} direction. If the I_{Load} direction is reversed, the transient behavior of V_{dsds} in **Figure 8a** will follow the same pattern as in V_{ds-} transient behavior in **Figure 8b**. Similarly, it also happens for the transient behavior of V_{ds-} in **Figure 8a**.

To test the dependency of SVC with L_σ, consider a change of L_σ value into 2nH. In **Figure 9a**, Δ_{mp} is introduced and expressed as $\Delta_{mp} = \min(V_{det})$-$V_{th}$.
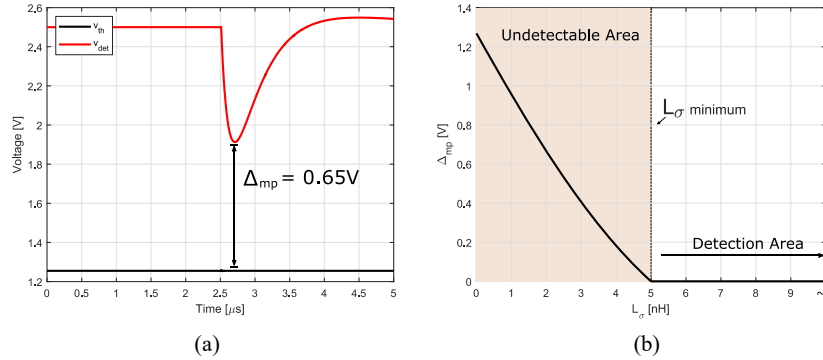
(a)　　　　　　　　　　　　　(b)

Figure 9 The limitation due to (a) the introduction of Δmp with Lσ is changed to 2nH, (b) value with the variation of Lσ.

In **Figure 9a**, an SEB is introduced at t=2.5µs. If Δ_{mp},>0 a FUL/SEB is not detected by the SVC. Note that the magnitude of V_{det} is reduced as the value of the LPF component, i.e., C_{LP} and R_{LP} increases. Therefore, it is necessary to have a compromise between the L_σ and false-triggering limitations in choosing the LPF parameters. **Figure 9b** shows the operating area of SVC. As shown, Δ_{mp} is reduced linearly with the increase of L_σ. We conclude that in this application, the minimum value of L_σ is 5nH to ensure the correct operation of SVC.

5   Conclusion

SVC is proposed as an ultra-fast and robust FUL/SEB detection. By using SVC, the FUL/SEB detection in the ohmic region of the MOSFET is realized. The results show that the SVC can detect the FUL/SEB very quickly, with response times in the order of less than 100ns.

The limiting factors of the SVC are the false-triggering due to the switching transient, the comparator input overvoltage, and the minimum value of L_σ. In the example application shown, the minimum value of L_σ is 5nH.

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2 Keywords

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