Exploring the Boundaries and Effects of the Discontinuous Conduction Mode in H-Bridge Inverter with Dead-time

Exploring the Boundaries and Effects of the Discontinuous Conduction Mode in H-Bridge Inverter with Dead-time

Qihao Yu, Erik Lemmen, Korneel Wijnands, Bas Vermulst
Department of Electrical Engineering, Eindhoven University of Technology
P.O. Box 513, 5600MB
Eindhoven, The Netherlands
Email: q.yu@tue.nl
URL: http://www.tue.nl/epe

Keywords

≪Time-Domain Analysis≫, ≪Pulse Width Modulation (PWM)≫, ≪Dead-time≫.

Abstract

Dead-time of an H-bridge inverter can cause nonlinear error on the inverter output. In different switching cycles during a fundamental period, the effect of dead-time might be different. The H-bridge inverter in different switching cycles can operate in three kinds of modes, including soft-switching continuous conduction mode, discontinuous conduction mode and hard-switching continuous conduction mode. In addition, the discontinuous conduction mode can be further classified into four different types, which have not been fully studied in previous research. In this paper, four different kinds of switching cycle in the discontinuous conduction mode are investigated. The effect of the dead-time on the voltage error is elaborated and the boundaries of each kind of switching cycle are determined by a series of constraint functions. Based on the analysis, a complete mathematical expression of the voltage error in a fundamental period is given and it yields a better accuracy compared to previous publications.

Introduction

The sine-pulse-width-modulated (SPWM) H-bridge inverter is widely used in industry, such as lithography and magnetic resonance imaging (MRI). Those applications demand high precision and low distortion on the inverter output [1, 2]. In practice, a certain dead-time should be applied to the H-bridge inverter to prevent short circuit. This dead-time introduces nonideal effect to the inverter output [3, 4, 5], which is typically the most dominant source of the distortion [6, 7]. In order to further reduce the distortion for high-precision applications, the effects of the dead-time should be investigated accurately.

During the dead-time, switches of both the upper and lower legs in the H-bridge inverter are turned-off. The switch-node voltage is then determined by the direction of the filter inductor current and the conductivity of the anti-parallel diodes, such as the body diodes of the MOSFETs [8]. Most of the previous researches have only considered the case of a distinctly positive or negative inductor current by neglecting the current ripple during the dead-time [9, 10, 11]. Neglecting the current ripple results in a fixed voltage error to the switch-node voltage. However, as illustrated in [12], soft-switching is achieved near the zero-crossing region of the inductor current, where there is no voltage error. Furthermore, discontinuous conduction mode (DCM) of the inductor current might be present in some switching cycles, which causes a variable voltage error to the switch-node voltage [13]. In [14], a mathematical expression was given to describe the values of the switch-node voltage under different conditions of the inductor current in a fundamental period. The expression was derived based on the assumption that the moving average value of the inductor current is equal to the reference output current. However, due to the voltage error in

some switching cycles, current error is introduced to the output. Therefore, there is a deviation between the filter inductor current and the ideal output current. This deviation leads to an inaccurate estimation of the voltage error and the boundaries of DCM, especially in case of a high inductor current ripple.

The aim of this paper is to investigate the dead-time effect on the H-bridge inverter output in DCM. The effect of different DCM are analysed in detail. The clamping time during which inductor current is clamped to zero during the time is calculated. Moreover, an accuracy-improved model of the voltage error in DCM compared to [14] is proposed by taking the deviation of inductor current from the ideal current into consideration. The boundaries of the DCM are determined with a numerical method. Simulations are conducted to verify the model, underlining the proposed model have significantly increased the accuracy.

Switching cycle analysis

The topology of an H-bridge inverter is shown in Fig. 1. In this research, digital natural sampling PWM and bipolar modulation are used for illustration, as shown in Fig. 2. The output capacitances of the switches are neglected thus the rise and fall time of the switching transient are assumed to be zero.

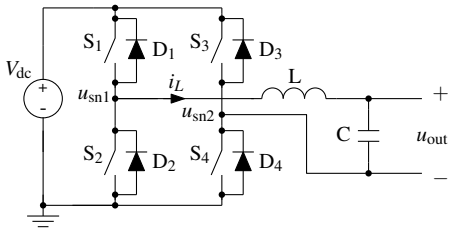

Fig. 1: The topology of an H-bridge inverter with output filter.

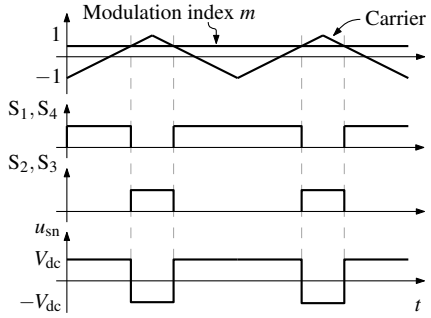

Fig. 2: The ideal PWM waveforms without dead-time. m is the modulation index. S_1,S_4 and S_2,S_3 represent the on-and-off state of each switch. $u_{sn} = u_{sn1} - u_{sn2}$.

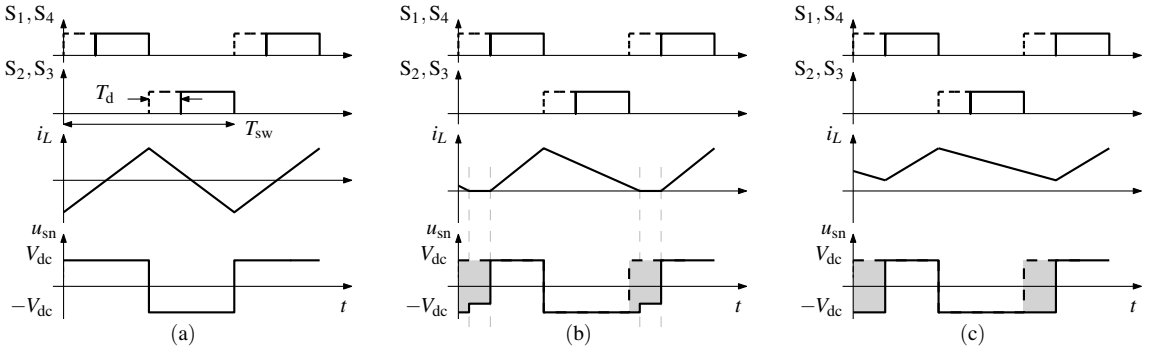

Fig. 3: Waveforms during a switching cycle. (a): soft-switching continuous conduction mode; (b): discontinuous conduction mode; (c): hard-switching continuous conduction mode. The dashed and solid line represent the ideal case without dead-time and practical case with dead-time respectively.

During a switching cycle $[nT_{sw}, (n+1)T_{sw}]$ with T_{sw} representing for the switching period and n a non-negative integer, the modulation index for a digital PWM is defined by

$$m(n) = M \sin\left(\frac{2\pi n}{N_{sw}}\right), \tag{1}$$

where M is the modulation depth and N_{sw} is the ratio of the switching frequency f_{sw} to the output frequency f_o. The moving average value of the switch-node voltage and the output voltage are defined by $\langle u_{sn}(n)\rangle$ and $\langle u_{out}(n)\rangle$ respectively and the operator $\langle\cdot\rangle$ is the average value in a switching cycle. Ideally $\langle u_{sn}(n)\rangle = \langle u_{out}(n)\rangle = V_{dc}m(n)$. However, a certain dead-time T_d is required to prevent short

circuit in practice, which results in a voltage error and is given by

$$\langle u_{\mathrm{e}}(n)\rangle = \langle u_{\mathrm{out}}(n)\rangle^{*} - \langle u_{\mathrm{out}}(n)\rangle, \tag{2}$$

where $\langle u_{\mathrm{out}}(n)\rangle^{*}$ is the moving average value of the reference voltage. As shown in Fig. 3, the switching cycle can be divided into three modes depending on the inductor current waveform: soft-switching continuous conduction mode (SSCCM), discontinuous conduction mode (DCM) and hard-switching continuous conduction mode (HSCCM). SSCCM and HSCCM have been investigated into in [14] and they are not the focus in this paper. While for DCM, it can be further classified into four different switching modes, as shown in Fig. 4.

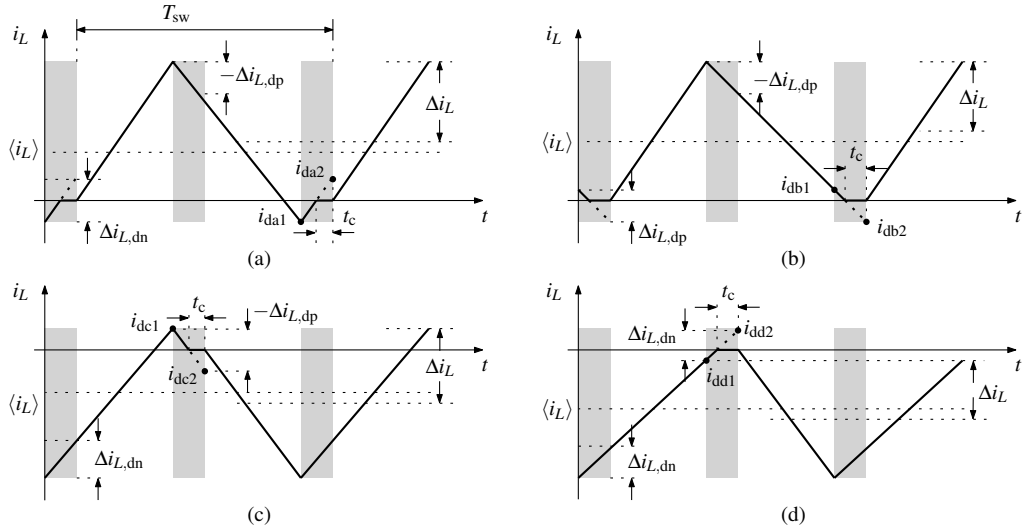

Fig. 4: The inductor current waveforms for DCM. The inductor current (a) rises from negative to zero and is clamped during dead-time with a positive average value in a switching cycle; (b) falls from positive to zero and is clamped during dead-time with a positive average value in a switching cycle; (c) falls from positive to zero and is clamped during dead-time with a negative average value in a switching cycle; (d) rises from negative to zero and is clamped during dead-time with a negative average value in a switching cycle.

In order to describe each DCM switching cycle, several parameters should be defined as follows. The ideal moving average value of filter inductor current without dead-time during a switching cycle is

$$\langle i_L(n)\rangle^{*} = \frac{MV_{\mathrm{dc}}}{Z}\sin\left(\frac{2\pi n}{N_{\mathrm{sw}}} - \varphi_o\right), \tag{3}$$

where Z and φ_o are the impedance and phase angle of the load. If dead-time is neglected, the peak-to-average inductor current ripple $\Delta i_L(n)$ during a switching cycle is given by

$$\Delta i_L(n) = \frac{T_{\mathrm{sw}}V_{\mathrm{dc}}}{4L}\left[1 - m(n)^2\right]. \tag{4}$$

The inductor current change during dead-time when the inductor current is distinctly positive and negative, which is achieved in SSCCM and HSCCM, is defined by

$$\Delta i_{L,\mathrm{dp}}(n) = -\frac{V_{\mathrm{dc}}T_{\mathrm{d}}}{L}\left[1 + m(n)\right] \tag{5}$$

and

$$\Delta i_{L,\mathrm{dn}}(n) = \frac{V_{\mathrm{dc}}T_{\mathrm{d}}}{L}\left[1 - m(n)\right] \tag{6}$$

respectively. Taking the switching cycle analysis of DCM shown in Fig. 4 (a) for an example, the actual

Table I: Clamping time $t_c(n)$ and moving average voltage error $\langle u_e(n)\rangle$ of each discontinuous conduction mode

Mode	$t_c(n)$	$\langle u_e(n)\rangle$
(a)	$\frac{\langle i_L(n)\rangle^* - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n)}{\frac{\Delta i_{L,\mathrm{dn}}(n)}{T_d} - \frac{\Delta i_L(n)}{T_{sw}} + \frac{[1-m(n)]}{ZT_{sw}}}$	$\frac{V_{dc}[1-m(n)]t_c(n)}{T_{sw}}$
(b)	$\frac{\langle i_L(n)\rangle^* - 2\frac{V_{dc}T_d}{ZT_{sw}} - \Delta i_L(n) + \frac{1}{2}\Delta i_{L,\mathrm{dp}}(n)}{\frac{\Delta i_{L,\mathrm{dp}}(n)}{2T_d} - \frac{\Delta i_L(n)}{T_{sw}} - \frac{[1+m(n)]}{ZT_{sw}}}$	$\frac{2V_{dc}T_d - (1+m(n))V_{dc}t_c(n)}{T_{sw}}$
(c)	$\frac{\langle i_L(n)\rangle^* + \Delta i_L(n) + \Delta i_{L,\mathrm{dp}}(n)}{\frac{\Delta i_{L,\mathrm{dp}}(n)}{T_d} + \frac{\Delta i_L(n)}{T_{sw}} - \frac{[1+m(n)]}{ZT_{sw}}}$	$-\frac{V_{dc}[1+m(n)]t_c(n)}{T_{sw}}$
(d)	$\frac{\langle i_L(n)\rangle^* + 2\frac{V_{dc}T_d}{ZT_{sw}} + \Delta i_L(n) + \frac{1}{2}\Delta i_{L,\mathrm{dn}}(n)}{\frac{\Delta i_{L,\mathrm{dn}}(n)}{2T_d} + \frac{\Delta i_L(n)}{T_{sw}} + \frac{[1-m(n)]}{ZT_{sw}}}$	$\frac{-2V_{dc}T_d + (1-m(n))V_{dc}t_c(n)}{T_{sw}}$

moving average inductor current can be written as

$$\langle i_L(n)\rangle = \frac{T_{sw}-t_c(n)}{2T_{sw}}\cdot 2\Delta i_L(n) - \frac{2[T_d - t_c(n)]}{[1+m(n)]T_{sw}}\cdot 2\Delta i_L(n), \tag{7}$$

where $t_c(n)$ is the clamping time during which the inductor current is clamped to zero. In previous research [14], $\langle i_L(n)\rangle$ is assumed to be $\langle i_L(n)\rangle^*$. However, a current error introduced by the voltage error during the dead-time is introduced. For a inductive load with dominant resistance, the actual moving average inductor current can be simplified by

$$\langle i_L(n)\rangle = \langle i_L(n)\rangle^* - \frac{\langle u_e(n)\rangle}{Z}. \tag{8}$$

The moving average voltage error $\langle u_e(n)\rangle$ in Fig. 3 (a) is governed by

$$\langle u_e(n)\rangle = \frac{[1-m(n)]V_{dc}t_c(n)}{T_{sw}}. \tag{9}$$

Solving (7),(8) and (9) for $t_c(n)$ leads to

$$t_c(n) = \frac{\langle i_L(n)\rangle^* - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n)}{\frac{\Delta i_{L,\mathrm{dn}}(n)}{T_d} - \frac{\Delta i_L(n)}{T_{sw}} + \frac{[1-m(n)]}{ZT_{sw}}}. \tag{10}$$

Therefore, the moving average voltage error $\langle u_e(n)\rangle$ in Fig. 3 (a) can be solved by substituting (10) into (9). Similarly, the clamping time and the moving average voltage error $\langle u_e(n)\rangle$ of DCM described in Fig. 3 (b), (c) and (d) can be analytically solved, which are listed in Table I.

In order to obtain a complete expression of the moving average voltage error $\langle u_e(n)\rangle$ in a fundamental period, the boundaries of each DCM should be found. As shown in Fig. 4, the boundaries of the switching cycle depicted in Fig. 4 (a) can be described by

$$\begin{cases} \langle i_L(n)\rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n) \geq 0, \\ \langle i_L(n)\rangle - \frac{V_{dc}T_d(1-m(n))}{ZT_{sw}} - \Delta i_L(n) + \frac{T_d}{T_{sw}}\Delta i_L(n) < 0. \end{cases} \tag{11}$$

Based on the above analysis, two constraint functions $y_{sn}(n)$ and $y_{dn}(n)$ can be defined to simplify the expressions as

$$\begin{cases} y_{sn}(n) = \langle i_L(n)\rangle - \Delta i_L(n) + \Delta i_{L,\mathrm{dn}}(n), \\ y_{dn}(n) = \langle i_L(n)\rangle - \frac{V_{dc}T_d(1-m(n))}{ZT_{sw}} - \Delta i_L(n) + \frac{T_d}{T_{sw}}. \end{cases} \tag{12}$$

Table II: The boundaries and time intervals of each switching modes

Mode	Boundary	Time interval
(a)	$\begin{cases} y_{\rm sn}(n) = \langle i_L(n)\rangle - \Delta i_L(n) + \Delta i_{L,\rm dn}(n) \geq 0, \\ y_{\rm dn}(n) = \langle i_L(n)\rangle - \frac{V_{\rm dc}T_{\rm d}(1-m(n))}{ZT_{\rm sw}} - \Delta i_L(n) + \frac{T_{\rm d}}{T_{\rm sw}}\Delta i_L(n) < 0. \end{cases}$	$[N_{\rm sn1}, N_{\rm dn1}) \cap (N_{\rm dn2}, N_{\rm sn2}]$
(b)	$\begin{cases} y_{\rm dn}(n) = \langle i_L(n)\rangle - \frac{V_{\rm dc}T_{\rm d}(1-m(n))}{ZT_{\rm sw}} - \Delta i_L(n) + \frac{T_{\rm d}}{T_{\rm sw}}\Delta i_L(n) \geq 0, \\ y_{\rm hn}(n) = \langle i_L(n)\rangle - \frac{2V_{\rm dc}T_{\rm d}}{ZT_{\rm sw}} - \Delta i_L(n) + \frac{1}{2}\Delta i_{L,\rm dp}(n) < 0. \end{cases}$	$[N_{\rm dn1}, N_{\rm hn1}) \cap (N_{\rm hn2}, N_{\rm dn2}]$
(c)	$\begin{cases} y_{\rm sp}(n) = \langle i_L(n)\rangle + \Delta i_L(n) + \Delta i_{L,\rm dp}(n) \leq 0, \\ y_{\rm dp}(n) = \langle i_L(n)\rangle + \frac{V_{\rm dc}T_{\rm d}(1+m(n))}{ZT_{\rm sw}} + \Delta i_L(n) - \frac{T_{\rm d}}{T_{\rm sw}}\Delta i_L(n) > 0. \end{cases}$	$[N_{\rm sp1}, N_{\rm dp1}) \cap (N_{\rm dp2}, N_{\rm sp2}]$
(d)	$\begin{cases} y_{\rm dp}(n) = \langle i_L(n)\rangle + \frac{V_{\rm dc}T_{\rm d}(1+m(n))}{ZT_{\rm sw}} + \Delta i_L(n) - \frac{T_{\rm d}}{T_{\rm sw}}\Delta i_L(n) \leq 0, \\ y_{\rm hp}(n) = \langle i_L(n)\rangle + \frac{2V_{\rm dc}T_{\rm d}}{ZT_{\rm sw}} + \Delta i_L(n) + \frac{1}{2}\Delta i_{L,\rm dn}(n) > 0. \end{cases}$	$[N_{\rm dp1}, N_{\rm hp1}) \cap (N_{\rm hp2}, N_{\rm dp2}]$

Solving $y_{\rm sn}(n)$ and $y_{\rm dn}(n)$ in the period of $[0, N_{\rm sw}]$ gives zero-crossing $N_{\rm sn1}$, $N_{\rm sn2}$ ($N_{\rm sn2} > N_{\rm sn1}$) and $N_{\rm dp1}$, $N_{\rm dp2}$ ($N_{\rm dp2} > N_{\rm dp1}$) respectively. Therefore, when $n \in [N_{\rm sn1}, N_{\rm dn1}) \cap (N_{\rm dn2}, N_{\rm sn2}]$ and $n \in \left[N_{\rm dp2}, N_{\rm sn2}\right]$, the voltage error is given by (9). The similar analysis also applies to other DCM switching cycles illustrated in Fig. 4 (b), (c) and (d) in order to obtain the voltage error. A complete expression of the boundaries of DCM is given in Table II. A typical plot of the constraint functions is depicted in Fig. 5.

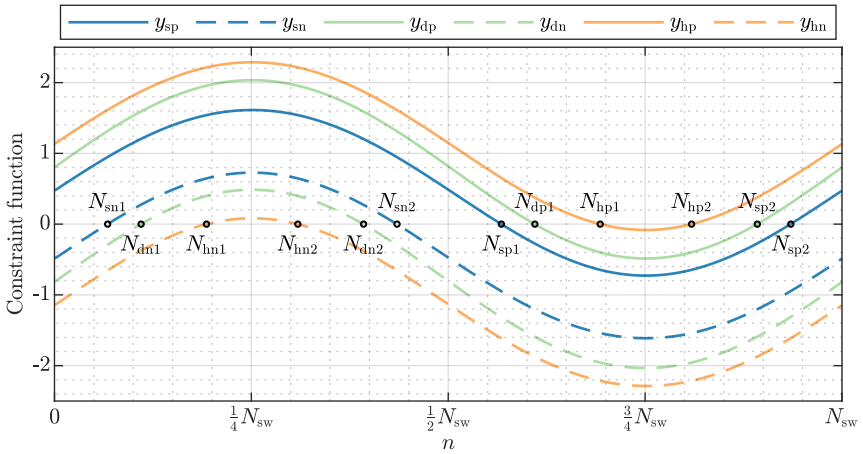

Fig. 5: A typical plot of constraint functions.

With the boundaries of DCM clear, it is easy to derive that SSCCM is achieved in $[0, N_{\rm sn1}] \cup \left[N_{\rm sn2}, N_{\rm sp1}\right] \cup \left[N_{\rm sp2}, N_{\rm sw} - 1\right]$ and the moving average voltage error $\langle u_{\rm e}(n)\rangle$ is zero. HSCCM happens in $[N_{\rm hn1}, N_{\rm hn2}]$ and $\left[N_{\rm hp1}, N_{\rm hp2}\right]$. The moving average voltage error $\langle u_{\rm e}(n)\rangle$ is $\frac{2}{T_{\rm sw}}V_{\rm dc}T_{\rm d}$ in $[N_{\rm hn1}, N_{\rm hn2}]$ and $-\frac{2}{T_{\rm sw}}V_{\rm dc}T_{\rm d}$ in $\left[N_{\rm hp1}, N_{\rm hp2}\right]$. As a result, a complete expression of the voltage error in a fundamental period can be easily derived.

It should be noted that the constraint functions have not necessarily two zero-crossings. For example, if $y_{\rm sp}(n)$ and $y_{\rm sn}(n)$ have no zero-crossing point in a fundamental period, then there is no DCM or HSCCM switching cycle and thus soft-switching is achieved all the time. In this case, the dead-time causes no voltage error. Similarly, if $y_{\rm hp}(n)$ and $y_{\rm hn}(n)$ have no zero-crossing point in a fundamental period, then there are only SSCCM and DCM but no HSCCM switching cycle. The HSCCM cycle exists if and only if all the constraint functions have two zero-crossing points. Fig. 6 depicts three typical combinations of the constraint functions and the calculated voltage error for an H-bridge inverter working under different modulation depths. As shown in the figure, when solely changing the modulation depth, the time intervals of the switching modes in a fundamental period change accordingly. When the modulation depth is low, the output current is low making the inductor current ripple relatively high and SSCCM can be achieved all the time. When increasing the modulation index, DCM and HSCCM appear one after another.

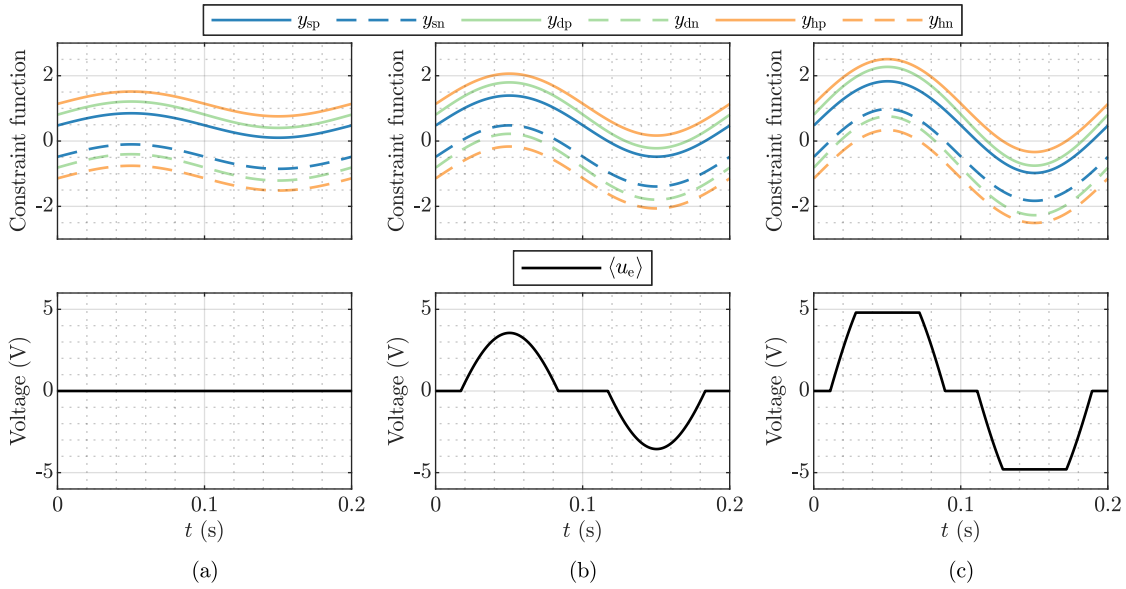

Fig. 6: Waveforms of the calculated constraint functions y_{sp}, y_{sn}, y_{dp}, y_{dn}, y_{hp} and y_{hn} and the calculated moving average voltage error $\langle u_e \rangle$ of an H-bridge inverter working at $V_{dc} = 48$ V, $T_d = 5$ μs, $f_{sw} = 10$ kHz, $f_o = 5$ Hz, $L = 2$ mH, $C = 30$ μF, $R = 10$ Ω and (a) $M = 0.08$, (b) $M = 0.2$, (c) $M = 0.3$.

Experimental validation

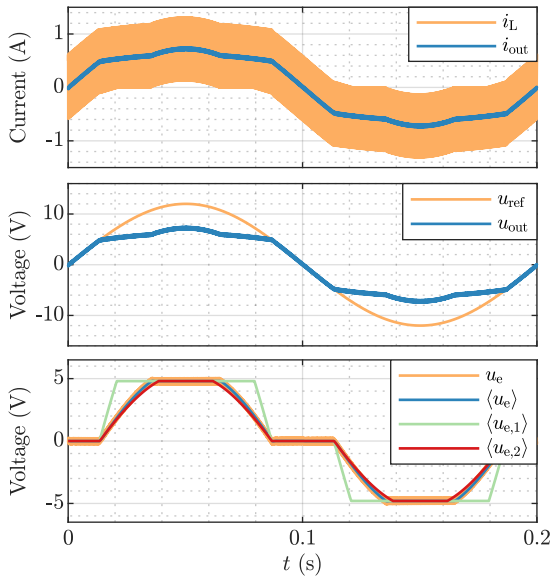

Fig. 7: The simulated waveforms of the H-bridge inverter.

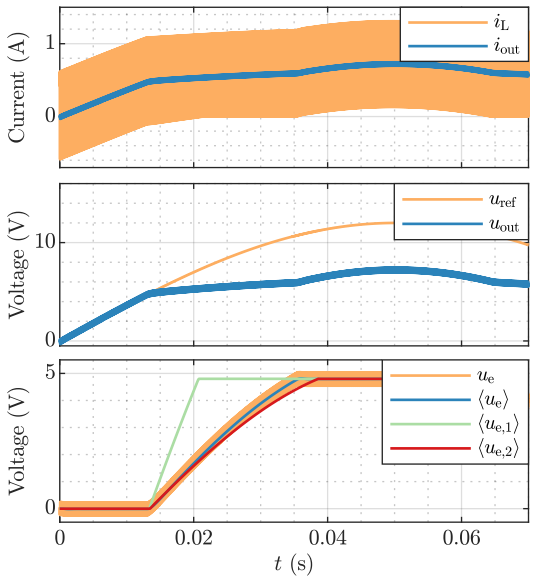

Fig. 8: A zoom-in of the simulated waveforms in DCM.

Simulations were done using MATLAB/Simulink by adopting ideal MOSFETs with no parasitic capacitance to verify the presented model. The simulation is conducted under the condition that $V_{dc} = 48$ V, $M = 0.25$, $f_o = 5$ Hz, $f_{sw} = 10$ kHz, $T_d = 5$ μs, $L_l = 0$, $R = 10$ Ω, $L = 2$ mH and $C = 30$ μF. The simulated waveforms in a fundamental period are depicted in Fig. 7 and a zoom-in of the waveforms in DCM is shown in Fig. 8, where u_e, $\langle u_e \rangle$, $\langle u_{e,1} \rangle$ and $\langle u_{e,2} \rangle$ are the simulated voltage error, the moving average value of the simulated voltage error, calculated moving average value of voltage error based on the method in [14] and in this paper respectively. As can be seen, both the voltage error magnitude and the boundaries of DCM estimated by this paper shows an improved accuracy compared to the previous one.

Euclidean distance is a mathematical indicator of the similarities of two different sequence [15]. By using the simulation results as a benchmark, the accuracy of the calculated results by the different methods can

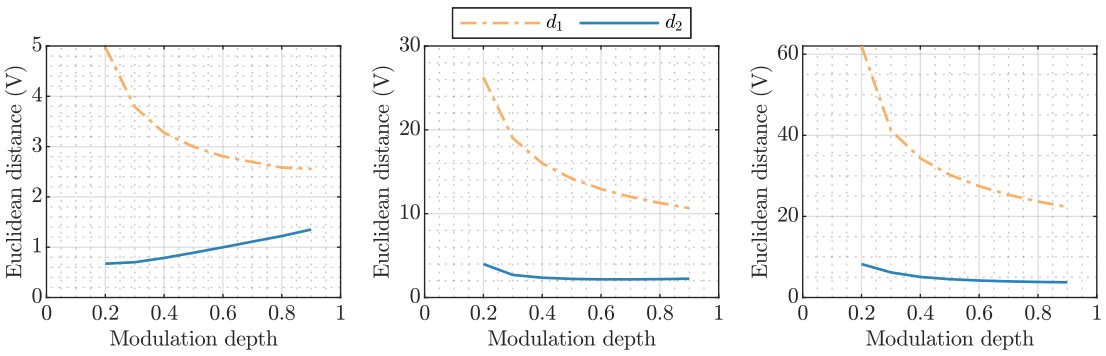

Fig. 9: The Euclidean distances for the different methods under (a) $T_\mathrm{d} = 1\ \mu$s; (b) $T_\mathrm{d} = 3\ \mu$s; (c) $T_\mathrm{d} = 5\ \mu$s.

be compared. The Euclidean distance is defined by

$$d_x = \sqrt{\sum_{n=0}^{N_\mathrm{sw}-1} \left(\langle u_{\mathrm{e},x}(n)\rangle - \langle u_\mathrm{e}(n)\rangle\right)^2},\ x = 1,2. \tag{13}$$

As an example of the waveforms shown in Fig. 7 and Fig. 8, the differences of the calculated results by the method from [14] and the method presented in this paper yield to $d_1 = 47.4$ V and $d_2 = 7.59$ V. In general, a smaller Euclidean distance indicates a better similarity of two waveforms.

In order to see the accuracy comparison under different conditions, simulations are done by varying the modulation depth and the dead-time value while other properties remaining unchanged and the results are shown in Fig. 9. As can be seen, the presented model in this paper has a better accuracy than the previous one under different dead-time and modulation depth. Normally, a greater dead-time results in a larger Euclidean distance for both methods since a larger dead-time causes a larger portion of DCM and the calculation error in DCM accumulates as regards Euclidean distance. Not only the value of Euclidean distance increases with an increasing dead-time, but also the difference of the value is exaggerated, underlining the accuracy and the effectiveness of the presented model.

In general, the Euclidean distance is smaller with a higher modulation depth due to the fact that the portion of HSCCM is larger while that of DCM is smaller thus the calculation error in DCM becomes less significant. However, as shown in Fig. 9 (a), Euclidean distance calculated by this method increases with an increasing modulation depth. The reason is that with such small dead-time, the portion of DCM is small thus the calculation error in DCM is not dominant in the final result of Euclidean distance. On the other hand, the voltage error introduced by the SPWM becomes dominant and with an increasing modulation depth this error becomes governing on Euclidean distance.

Conclusion

Previous researches have not fully explored the dead-time effect in DCM of an H-bridge inverter. In this paper, four different DCMs are elaborated and the effect of dead-time to the output voltage error in different DCM is analysed and described by mathematical models. A series of constraint functions are defined such that the boundaries and the time intervals of each DCM can be determined. The combination of the voltage error models and constraint functions enables a complete expression of the voltage error in a fundamental period. Compared to previous researches, by taking the current error of the inductor current compared to the ideal current into consideration, the calculation done in this paper yields a better accuracy which is validated by simulations. The method and the results of the calculation introduced in this paper can be used for output harmonics or distortions modelling and feed-forward dead-time compensation, especially for high-precision applications.

References

[1] S. J. Settels, J. Duarte, J. van Duivenbode, and E. Lomonova, "A 2kV Charge-based ZVS Three-level Inverter," *IEEE Trans. Power Electron.*, vol. 8993, no. c, pp. 1–1, 2019.

[2] Q. Yu, R. Baeten, E. Lemmen, B. Vermulst, and K. Wijnands, "A 1 MHz Wide Bandgap Power Amplifier for High-Precision Applications," in *2019 21st Eur. Conf. Power Electron. Appl. (EPE '19 ECCE Eur.* IEEE, sep 2019, pp. P.1–P.7.

[3] F. Chierchie and E. Paolini, "Analytical and numerical analysis of dead-time distortion in power inverters," *Argentine Sch. Micro-Nanoelectronics Technol. Appl. (EAMTA), 2010*, pp. 6–11, 2010.

[4] N. Urasaki, T. Senjyu, T. Kinjo, T. Funabashi, and H. Sekine, "Dead-time compensation strategy for permanent magnet synchronous motor drive taking zero-current clamp and parasitic capacitance effects into account," *IEE Proc. - Electr. Power Appl.*, vol. 152, no. 4, p. 845, 2005.

[5] Z. Zhang and L. Xu, "Dead-time compensation of inverters considering snubber and parasitic capacitance," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 3179–3187, 2014.

[6] R. J. Kerkman, D. Leggate, D. W. Schlegel, and C. Winterhalter, "Effects of parasitics on the control of voltage source inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 1 I, pp. 140–150, 2003.

[7] S. Y. Kim, W. Lee, M. S. Rho, and S. Y. Park, "Effective dead-time compensation using a simple vectorial disturbance estimator in PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 5, pp. 1609–1614, 2010.

[8] A. Munoz and T. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 683–689, jul 1999.

[9] C. Wu, W. H. Lau, and H. S. H. Chung, "Analytical technique for calculating the output harmonics of an H-bridge inverter with dead time," *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 46, no. 5, pp. 617–627, 1999.

[10] C. Attaianese, V. Nardi, and G. Tomasso, "A novel SVM strategy for VSI dead-time-effect reduction," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1667–1674, 2005.

[11] Yong-Kai Lin and Yen-Shin Lai, "Dead-Time Elimination of PWM-Controlled Inverter/Converter Without Separate Power Sources for Current Polarity Detection Circuit," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2121–2127, 2009.

[12] J. M. Schellekens, R. A. M. Bierbooms, and J. L. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," *19th Int. Conf. Electr. Mach. ICEM 2010*, pp. 1–6, 2010.

[13] M. A. Herrán, J. R. Fischer, S. A. González, M. G. Judewicz, and D. O. Carrica, "Adaptive dead-time compensation for grid-connected PWM inverters of single-stage PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2816–2825, 2013.

[14] Q. Yu, E. Lemmen, and B. Vermulst, "A Numerical Method for Calculating the Output Spectrum of an H-Bridge Inverter with Dead-time Based on Switching Mode Analysis," in *2019 IEEE Energy Convers. Congr. Expo.* IEEE, sep 2019, pp. 2245–2251.

[15] C. Faloutsos, M. Ranganathan, and Y. Manolopoulos, "Fast Subsequence Matching in Time-Series Databases," *ACM SIGMOD Rec.*, vol. 23, no. 2, pp. 419–429, 1994.