TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

ArF scanner lithography for InP photonic integrated circuit fabrication

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Jeroen Bolk

ArF Scanner Lithography for InP Photonic Integrated Circuit Fabrication

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus Prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op dinsdag 12 mei 2020 om 13:30 uur

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Dank voor alle steun van mijn gezin en ouders,
opgedragen aan mijn broertje Chris Bolk †. . .

Summary

ArF Scanner Lithography for InP Photonic Integrated Circuit Fabrication

Over the past few decades, lithography has defined the capability of advanced electronic integrated circuit fabrication. It determines the minimum feature size that can be printed uniformly on a wafer, the shape of the chip patterns at a nanometer scale, the relative positioning of device layers on top of each other, and the throughput and wafer size which impact the manufacturing cost of these devices.

A considerable effort has been made to create photonic integrated circuit (PIC) platforms using existing manufacturing infrastructure of the traditional electronics industry. This approach is widely known as Silicon photonics. While important progress has been made, this platform still requires InP to provide gain and lasers to create efficient optoelectronic devices. It is therefore important to create precision photonic components directly on InP substrates which enables the advantages of full monolithic integration.

So far, generic InP platforms have been restricted to the use of electron-beam, stepper and contact lithography. For volume production of photonic integrated circuits, stepper lithography is needed, but minimum feature sizes have been limited to 250 nm. This limitation comes from the fact that the shortest wavelength illumination and highest performance imaging have only been available for the latest large Silicon wafer diameters. While 4-inch InP wafers are used for high volume photonic devices and 6-inch are starting to become available, the InP industry has mostly been operating on substrates of 3-inch for high functionality PICs. Therefore, many of the techniques for precision manufacturing for the Silicon industry have not been explored for InP PICs.

In this thesis, the challenges and advantages of ArF deep ultra-violet lithography for InP PIC fabrication are explored and implementation of such processes is demonstrated for the first time. This work was performed with an ASML PAS5500/1100B scanner, modified to be the only system in the world at this technology node, to perform cassette to cassette exposures on 3-inch substrates at the time of writing, with a possibility to scale up to larger wafer sizes. The research activities have led to multi-layer ArF coating and development recipes, identifying and meeting high uniformity and quality standards for 100 nm patterning on semi-automated equipment. InP wafer quality, in terms of flat accuracy and overall wafer flatness were measured

and improved in collaboration with a substrate supplier.

It can be extremely challenging to use the thin ArF resist mask to pattern InP based high topography geometries. Three different patterning modules were developed to transfer the ArF lithography patterns into the InP substrate, for several steps in the existing generic process. A wet etch patterning module for active-passive butt-joint integration. A dry etch module for performing transfer of 200 nm pitch grating structures into to the semiconductor material. Lastly, a patterning module to define high topography waveguides with the ArF resist. This waveguide definition module was demonstrated to enable the fabrication of ultra-low excess loss arrayed waveguide gratings. Due to the advantages in critical dimension uniformity and reproducibility, the developed technology was directly implemented, resulting in a world-first commercial ArF enabled InP foundry process.

Since the required resolution for imaging gratings comes quite close to the limits of the installed ArF scanner, resolution enhancement techniques were explored. This work was supported through a collaboration with a software supplier to perform simulations of the lithography process. Double patterning and off-axis dipole illumination were both studied for the first time for grating imaging at 200 nm pitch. Off-axis dipole illumination was evaluated in collaboration with the equipment supplier, resulting in a significant image quality improvement for these gratings in terms of line edge roughness. Rule-based optical proximity correction (OPC) was investigated and applied for the first time on InP, using a sidewall grating design as a demonstrator. It was found that rule-based OPC can significantly improve resist pattern fidelity by over 70%.

In the later stages of the generic PIC fabrication process, it becomes impractical to use ArF lithography due to the increasing wafer level device topography. These layers however, can be imaged using i-line stepper lithography, which has advantages in terms of overlay and defectivity compared to contact lithography. A procedure was developed to perform overlay matching between a scanner and stepper of these generations for the first time, providing a route to full non-contact lithography and the associated performance benefits. Two components were identified that can exploit the improvements in overlay. A process was proposed and tested to fabricate optical spot-size converter devices. Another process was proposed to fabricate polarization converters (PCs) with scanner and stepper defined layers. Single section fabricated PC devices were characterized, exhibiting up to 98.9% conversion. An improved fabrication route and design are proposed to further increase the manufacturability of these devices.

The application of ArF lithography for InP PIC fabrication, is a highly promising scalable solution for the next generation photonic devices. The implementation of ArF lithography in the generic foundry platform makes this technology accessible to create a wide range of high precision InP photonic devices. In fact, it completes a circle where certain projects are currently working on PICs for sensing applications to improve capability for the lithography tools of the future.

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Acronyms

AIM American Institute for Manufacturing.

AR anti-reflection.

AWG arrayed waveguide grating.

BARC bottom anti-reflection coating.

BHF buffered hydro-fluoric acid.

BrMeOH bromine methanol.

BSR back side rinse.

CD critical dimension.

CDL critical dimension loss.

CDSEM critical dimension scanning electron microscope.

CDU critical dimension uniformity.

CP center point.

CTLM circular transmission line measurements.

DBR distributed Bragg reflector.

DFM design for manufacturing.

DLW direct laser write.

DOE design of experiments.

DOF depth of focus.

DSP double side polished.

DUV deep ultra-violet.

EBL electron beam lithography.

EBR edge bead removal.

ECO Electro-Optical Communications.

EDS energy dispersive spectroscopy.

EUV extreme ultra-violet.

FEM focus energy matrix.

FIB focused ion beam.

FPR free propagation region.

FSR front side rinse.

GDS graphic database system.

HHI Fraunhofer Heinrich Hertz Institute.

HMDS hexamethyldisilazane.

IBL ion beam lithography.

ICP inductively coupled plasma.

IMOS Indium Phoshide membranes on Silicon.

IO input/output.

IPI Institute for Photonic Integration.

LELE litho-etch, litho-etch.

LER line edge roughness.

LFLE litho-freeze, litho-etch.

LS line-space.

MEMS micro-electromechanical systems.

MFD mode field diameter.

MMO matched machine overlay.

MOVPE metal organic vapor phase epitaxy.

MPW multi-project wafer.

NA numerical aperture.

NIL nanoimprint lithography.

NILS normalized image log-slope.

OED opto-electronic devices.

OPC optical proximity correction.

PC polarization converter.

PDK process design kit.

PDM polarization division multiplexing.

PEB post exposure bake.

PECVD plasma enhanced chemical vapor deposition.

PER polarization extinction ratio.

PhI Photonic Integration.

PIC photonic integrated circuit.

PM polarization-maintaining.

POTDR polarization optical time domain reflectometry.

PR photoresist.

RET resolution enhancement technique.

RIE reactive ion etch.

SADP self-aligned double patterning.

SEM scanning electron microscope.

SMO single machine overlay.

SPL scanning probe lithography.

SSC spot-size converter.

SSP single side polished.

TARC top anti-reflection coating.

TE transverse electric.

TEM transmission electron microscopy.

TLS tunable laser source.

TM transverse magnetic.

TMAH tetra methyl ammonium hydroxide.

ttv total thickness variation.

TU/e Eindhoven University of Technology.

UPW ultra-pure water.

VLSI very large scale integration.

WPH wafers per hour.

XOR exclusive-or.

Chapter 1

Introduction

Electronics evolved from circuits built with discrete components soldered together on a printed circuit board, into integrated circuits consisting of millions of interconnected transistors on a single chip. Photonics is now at the start of an era where components are interconnected on a chip to create diverse and complex optical device functionality. In some cases, these photonic chips offer alternatives to existing bulky and expensive discrete optical devices. In other cases, integrated photonics enable novel applications that were impossible to realize through traditional methods. InP foundries are currently emerging to fabricate these chips through a generic technology platform requiring fabrication methods that move away from the lab-scale level in terms of volume and yield. Critical choices need to be made for the lithography capability, that meet the precision requirements of photonics, on substrate sizes suitable for the current as well as mid-term market volumes.

This chapter introduces the concept of a photonic integrated circuit (PIC) and continues to compare the main fabrication platforms. It zooms in on the principle of a generic InP platform. It gives an overview of different maskless and mask-based types of lithography that can be used for device fabrication, and in particular highlights optical lithography as the predominant technology for very large scale integration (VLSI) manufacturing. These types are then compared in the context of fabrication of high precision InP PICs. Next, the challenges of introducing high-resolution optical lithography for InP PIC fabrication are explained followed by a descriptive outline of the remaining chapters of this thesis.

1.1 Photonic integrated circuits

Photonics is the entire science and technology field that encompasses the generation, propagation, modification and detection of light. It is almost impossible to imagine the current world or future without photonics. Some of the most obvious consumer applications are in LED lighting, device displays, solar panels, and compact disc, DVD or Blu-ray media devices. Internet communication is mostly transmitted as light over glass fibers which can cross the oceans and today even reach as far as people's homes.

Data is stored in the cloud, which consists of huge interconnected datacenters that need optical means to move this data around. Less visible applications are in sensing, for instance in cameras, spectrometers, thermometers, and structural integrity monitoring on bridges, oil pipes or airplane wings.

Apart from the existing applications that were previously mentioned, there are many technologies leveraged by photonics and many new applications are being developed that will provide technical solutions for today's challenges in energy consumption, agriculture, healthcare and transport. The entire photonics business market was estimated to be approximately 615 B€ by the year 2020 [1]. Although this is only 20% of the electronics business, the European commission has underlined the importance of photonics with an annual growth rate of 7%, labeling it as one of six pillars of key enabling technologies from 2013 forward [2]. In the United States the importance of photonics was also recognized in 2015, leading to an investment of 600 M$ in the American Institute for Manufacturing (AIM) integrated photonics [3].

A PIC is a chip that consists of interconnected components that enable the handling of light at a micron or even nanometer scale. A single PIC containing many photonic capabilities can therefore fit on the tip of a finger and can be mass manufactured similarly to traditional microelectronic integrated circuits on wafers as illustrated in Fig. 1.1.

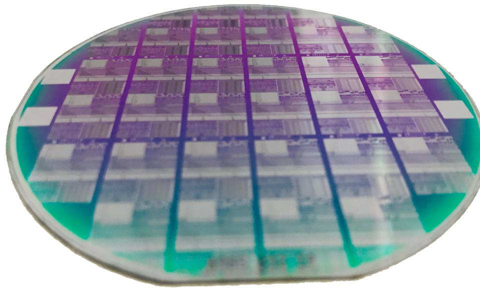


Figure 1.1: Example of a 3-inch indium phosphide PIC wafer.

1.2 Photonic integrated circuit platforms

There are three major technology platforms that enable the fabrication of PICs which can be separated into the following categories: indium phosphide (InP), silicon (Si), and silicon nitride (SiN) photonics. Each of these platforms, named after the material that forms the basic waveguides, has its strengths and weaknesses. Table 1.1 which was published in the Jeppix Roadmap 2018 [4], shows the availability and performance of specific PIC building blocks for each of the respective platforms.

This table shows that some PIC building blocks on Si photonics can only be offered through hybrid integration and some functionality is not available at all using a SiN platform. The only technology platform type that can offer all functionality through monolithic integration is InP. The Institute for Photonic Integration (IPI) in Eindhoven, focuses on the integration of InP technology in two sub-platforms. The most

Building Block	Performance InP	Si	SiN
Passive Components	**	**	***
Polarization Components	**	**	
Lasers	***	H	H
Phase Modulators	***	**	*
Electro Absorption Modulators	***	**	
Switches	**	**	*
Optical Amplifiers	***	H	H
Detectors	***	**	H

*** - Very Good, ** - Good, * - Moderate, H - Hybrid

Table 1.1: PIC technology platform capability comparison [4].

mature platform is the “Generic” integration platform [5,6], which uses a moderately confined waveguide structure. The other platform, which is still under development, is called Indium Phoshide membranes on Silicon (IMOS) [7,8]. The IMOS platform uses highly confined waveguide structures, which enables significantly smaller footprints for a chip as well as hybrid integration onto other substrates.

1.3 Generic InP photonic integrated circuit fabrication

The concept of generic PIC fabrication is to have a universal process flow that can simultaneously realize the available photonic components of the platform on a single wafer. This allows a PIC designer to determine the placement of individual components in the horizontal plane of a chip and to interconnect them as desired. The main advantage of this approach is that the fabrication process is fully decoupled from the application. This avoids the need to redevelop new process technology for every new application. Instead, each iteration of the process technology focuses on introducing new or improved versions of existing building blocks, making the process development significantly more efficient. This concept was proven to be very successful and has driven the microelectronics industry for years by enabling the exponential growth described in Moore’s law [9, 10]. In 2012 Smit et al. predicted that a similar trend could apply to the complexity growth of photonics as well [11]. Generic photonic integration is therefore required to enable this growth.

The InP generic technology platform of the Eindhoven University of Technology (TU/e) was originally developed within the former COBRA research institute and is currently being used by IPI for academic research and Smart Photonics for their foundry services. Within this platform, a wide selection of building blocks is available to create different photonic components from the process design kit (PDK). The PDK allows to device designer to string building blocks together at an abstraction level where he only needs to be concerned with building block specifications and interactions at the device level. The designer does therefore not have to worry about

how, and in which order different parts of the underlying individual components are physically made.

The restrictions of the fabrication process with respect to the design, are documented in the design rules of the technology platform and will be checked during the design phase of the PIC. These rules can for instance specify minimum or maximum size for certain building blocks or distances between in and output ports, metallization tracks or possibly even total component density. The complete design of the PIC is put together at the component level and the layout is then split over the different process layers to form a complementary mask set. Depending on the lithography technology used by the platform at each process stage, a layer can be written directly, or physical mask plates will be ordered prior to starting the fabrication of the PICs. The different stages of this workflow are illustrated in Fig. 1.2.

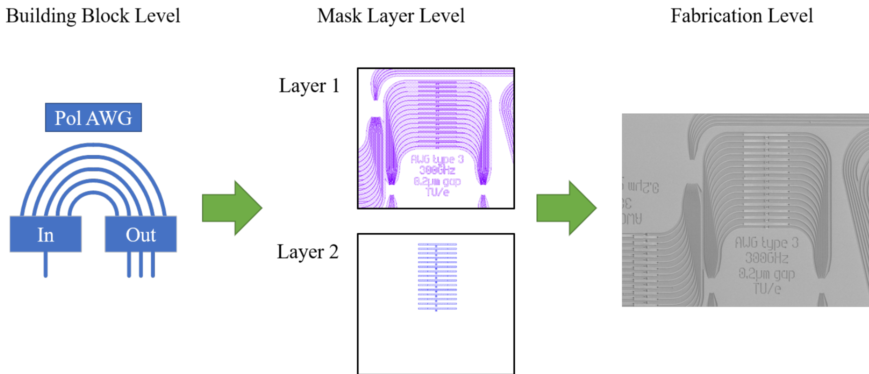


Figure 1.2: Workflow: Building block level design, separation into mask layers, and fabrication.

1.4 Lithography

At the heart of any integrated circuit fabrication process lies its lithography capability. This is the ability to transfer a design pattern onto the platform substrate. In most cases, the initial transfer of the pattern is done into a temporary material which is then used as a mask to transfer further into the definitive material. However, in some specific cases, lithography is performed directly into the desired pattern material. There are several techniques used for lithography in IC manufacturing which can be separated into two main categories: maskless and mask-based lithography.

1.4.1 Maskless lithography

Maskless lithography includes technologies that are widely applied such as electron beam lithography or direct laser write lithography. Some less familiar technologies such as ion beam lithography and scanning probe lithography also belong to this category. Since there is no predefined mask, this group of technologies is in principle

very flexible in terms of design iterations and corrections. However, maskless lithography is very time-consuming because every designed polygon needs to be written individually. maskless lithography is therefore often found in research, prototyping and low volume applications.

1.4.1.1 Electron beam lithography

There are many applications that rely on the use of electron beam lithography (EBL). Most masks that are used for high-resolution nanoimprint stamps or projection lithography reticles, are manufactured by EBL [12,13]. Simultaneously many nanofabrication applications in research as well as production have EBL as the preferred technology [14]. This lithography technique needs a temporary layer sensitive to electrons to transfer the design pattern onto a substrate. Under high vacuum, an electron beam is generated with a narrow diameter at an acceleration voltage between 10 and 100 kV. The position of this beam is controlled by the system as well as the position of the substrate. This allows an EBL system to write a pattern with minimum feature sizes as small as a few nanometers with excellent overlay specifications [15, 16]. The EBL process is illustrated by Fig. 1.3 showing both negative and positive resist processing. The electron beam can also be used to activate a precursor to etch or deposit material directly, which is referred to as focused electron beam etching and electron beam induced deposition respectively [17].

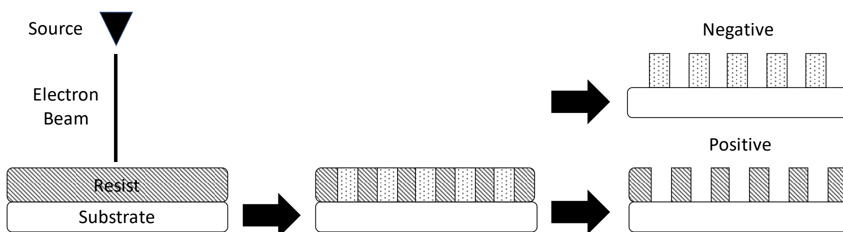


Figure 1.3: Schematic representation of the electron beam lithography process.

Write times for EBL are notoriously long and depend on the size of the written area as well as the sensitivity of the resist and beam current. As an example, assuming a 1% write area, on a 300 mm wafer using a chemical amplified resist that requires a dose of 200 μC/cm^2 [18] at a beam current of 2 nA, an exposure would take 8 days. To compensate for the long writing times, without sacrificing the advantages of EBL, multi-beam systems have been in development up to 2018 by Mapper. These tools were capable of writing with up to 65000 beams simultaneously. The performance of this equipment was demonstrated on 300 mm wafers at one wafer per hour with very good resolution, critical dimension uniformity, line edge roughness and overlay [19]. The commercial product however, did not make it to market and the intellectual property was acquired by ASML in 2019.

1.4.1.2 Direct laser write

The principle of direct laser write (DLW) is similar to that of EBL except that the beam consists of photons instead of electrons as is represented in Fig. 1.4. DLW is relatively limited in terms of minimum feature size because the wavelength of the laser source is much larger than that of the electrons in an EBL system. DLW also has a significantly larger writing spot, which causes the write times of DLW to be significantly shorter than that of EBL and makes it an interesting option for lower resolution binary or greyscale mask fabrication [20, 21], micro-electromechanical systems (MEMS) [22] and applications such as 3D lithography [23].

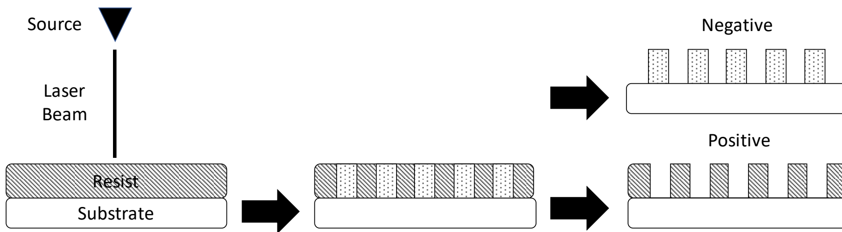


Figure 1.4: Schematic representation of the direct laser write process.

1.4.1.3 Ion beam lithography

For ion beam lithography (IBL), a bundle of positively charged ions is generated under vacuum conditions [24, 25]. Unlike electrons in EBL, ions have significant mass and with the acceleration voltage, a relatively large momentum. Light ions in the form of protons can be used to expose a layer of resist like EBL with the advantage of very low beam broadening at the impact location of the beam. Heavy ions enable the possibility to remove material from the location targeted by the beam as illustrated in Fig. 1.5. It is therefore not needed to use an intermediate layer for pattern transfer. Although this may be an advantage to the technology, it is even more time-consuming than EBL and the removed material can redeposit elsewhere causing defects at undesired locations. The technique is mostly used in the semiconductor industry for failure analysis on integrated circuits and to prepare transmission electron microscopy (TEM) lamellas.

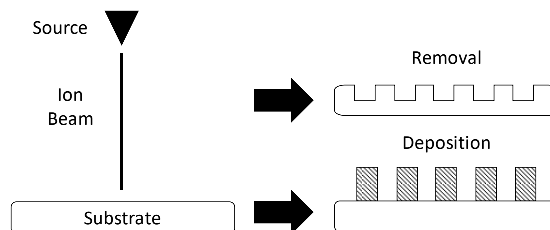


Figure 1.5: Schematic representation of the ion beam lithography process.

The impulse of the ion beam can also be used to stimulate chemical reactions at the impact location of the beam. This allows for very localized deposition under the right circumstances and can therefore also be used to create specific material patterns [26]. Lastly, the ion beam can also modify resists in a similar fashion as EBL, in which case it is found that it can improve writing times, while still achieving resolution in the order of a few nm [27].

1.4.1.4 Scanning probe lithography

Scanning probe lithography (SPL) uses a nano-scale probe to move accurately over the surface of the substrate. Because the tip of the probe can be very small this technique allows manipulation with minimum feature sizes reaching as low as a few nm. IBL can be used to mechanically remove material to create a pattern as is shown in Fig. 1.6. Alternatively, the probe can be augmented to cause thermal, diffusive or electrical effects in the material layer. This can be achieved by respectively heating, dipping or charging the probe. Depending on the properties of the material and probe, positive or negative pattern transfer is possible. Although some approaches are being investigated to use arrays of probes in parallel to increase throughput, IBL is still very slow and currently not suitable for cost efficient mass manufacturing yet. However, its versatile capabilities make it a very interesting candidate for various novel research applications [28–31].

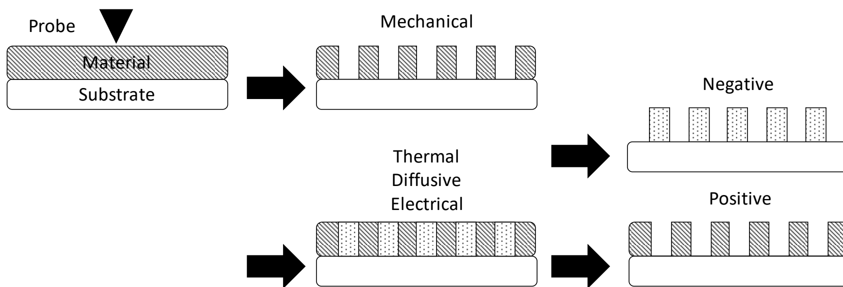


Figure 1.6: Schematic representation of the scanning probe lithography process.

1.4.2 Mask-based lithography

For high throughput applications where repeatability is very important, Mask-based lithography is often the technology of choice. This includes nanoimprint lithography, contact- and projection photolithography. Although the required masks for these techniques are still fabricated through maskless methods, in principle the mask should only be fabricated once. The mask can then be reused for a significant amount of predefined pattern transfers, typically exposing repeating patterns on different positions of a wafer, a substrate roll, or even an entire wafer at once.

1.4.2.1 Nanoimprint lithography

Nanoimprint lithography (NIL) is a technique where the mask is called a mold or stamp which can be crafted from different materials. The mold is pressed into a polymer and leaves an inverted imprint of the pattern that was on the mold [32]. This process is described schematically in Fig. 1.7. During the contact phase different variants of NIL can use either thermal, UV or electrochemical stimulation to transfer the pattern onto the substrate. NIL can be performed on a single sample in a run to run configuration or even in a field by field configuration for very high overlay and resolution applications [33–36]. Roll to plate and roll to roll techniques have also been implemented for mass manufacturing [37].

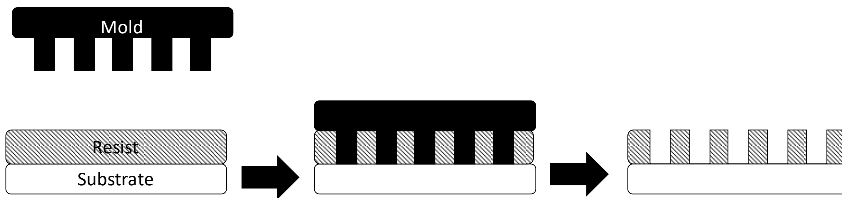


Figure 1.7: Schematic representation of the nanoimprint lithography process.

1.4.2.2 Photolithography

The most popular and widely applied type of lithography for high volume electronic IC production is undoubtedly photolithography. This technique uses a light source and a transparent mask plate with an absorbing metal pattern on it, to expose a photo-sensitive layer called photoresist. This exposure will cause a localized chemical reaction activated by the light which is often stimulated by a post-exposure bake. Depending on the chemistry of the resist, a wet developer will remove either the areas that were exposed to the light or alternatively the unexposed parts. This is called positive or negative pattern transfer respectively and is illustrated in Fig. 1.8.

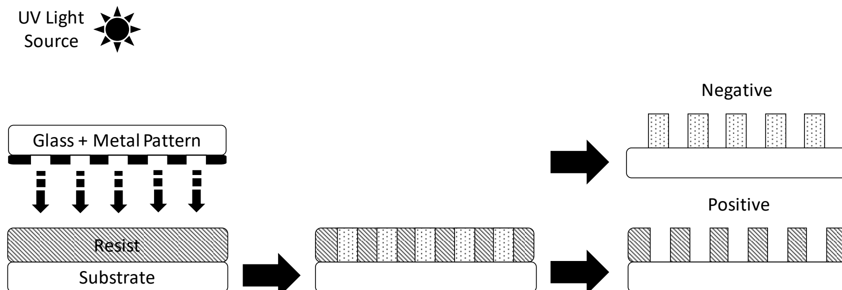


Figure 1.8: Schematic representation of the photolithography process.

With contact lithography the mask is brought in physical contact with the resist which results into a 1:1 pattern transfer of the mask. The resolution of this technology is very much limited by the diffraction and thus wavelength of the light coming from the source. Mercury lamps are commonly used as a light source and filters can be used to take advantage of the specific emission wavelengths at 435 nm (G-line), 405 nm (H-line) and 365 nm (I-line) respectively. A big disadvantage of contact lithography is the fact that the technique is very sensitive to defects on the substrate causing poor contact with the mask. Poor contact will result in poor definition of the pattern on the wafer. On top of this, random defects can also stick to or even damage the mask, resulting in problems for subsequent exposures. However, since the technology is very cost effective and has very high throughput, this type of equipment is still being manufactured and used for various research and production applications [38, 39].

Projection lithography was developed to circumvent the main disadvantages of contact lithography. The mask was moved away from the substrate to solve the physical contact and defectivity issues. A projection lens was positioned between the mask and substrate to bend the diffracted light pattern back onto the substrate with a typical de-magnification factor of 4. This resulted in increased tolerances on the mask manufacturing side. The minimum feature size of a line-space (LS) pattern that can be reliably imaged with a specific projection lithography system, can be derived from the Rayleigh criterion [40].

As shown in (1.1) the minimum critical dimension (CD) that can be resolved, is linearly dependent on the wavelength of the light source (λ) and inversely proportional with the numerical aperture (NA) of the projection lens. Lastly the constant (k1) represents the applicable lithography process conditions. This constant includes resist and developer sensitivity, mask engineering, illumination conditions, and advanced process integration-based enhancements such as double patterning.

$$\mathrm{CD} = k_1 \frac{\lambda}{NA} \tag{1.1}$$

From this equation can be derived that to shrink the minimum CD, it is advantageous to use a shorter wavelength source. This trend has been seen in the industrial lithography systems [41, 42] where traditional filtered 365 nm Mercury light sources were replaced by 248 nm excimer lasers and later 193 nm lasers [43–45]. Currently extreme ultra-violet (EUV) sources with 13.5 nm wavelength are being deployed for large scale ultra-small CD production systems [45].

Next to the source, an improved projection lens can shrink the minimum CD as well [41]. Better and more complex lens systems were developed over the years, increasing the NA from approximately 0.4 to around 0.9. Scanners were developed that differ in operation from steppers in a way that they only use the best part of a lens for each exposure. To maintain maximum image field size, these systems added a degree of complexity. On a scanner, each image is exposed while both the reticle and wafer are moving through a narrow slit of light that then passes through the projection lens. This dynamic method of exposure requires accurate control of the position of both the reticle and wafer relative to each other.

At that point the physical limit of what a lens with practical size and excellent quality could achieve was almost reached. To improve the NA even further the air be-

tween the projection lens and the substrate was replaced by water allowing systems to reach a NA of 1.35 with so-called immersion systems [41]. For EUV systems however, traditional optical lenses did not work anymore and ultra-flat mirror systems were introduced instead. This has caused an effective decrease in NA to approximately 0.33. While improvements to the NA are being developed it is still clear from Eq. 1.1 that with the improved wavelength EUV still yields a net minimum CD shrink.

Since in practice the lens and wavelength of a specific system are hardware defined, people have also worked on improved process technology to lower the k1 factor. Some examples of this are high contrast resists, off-axis illumination, phase-shift masking, optical proximity correction and double patterning. This postponed the need to replace existing expensive lithography infrastructure with next generation hardware at a particular node.

1.4.3 Lithography solutions for InP photonic integration

Based on the previous paragraphs, Table 1.2 was constructed to summarize the strengths and weaknesses of each lithography technology. The table lists the maskless technologies at the top and the mask-based types below. Most of the rated properties in this table are equally important for generic photonic integration. In essence, photonic integration requires exceptionally high dimensional control and low roughness which is proportional to the resolution. Some photonic components also require a challenging degree of overlay control. Lastly, generic InP integration aims to exploit the scalability of the technology platform to leverage the PIC prices. It is therefore logical that high throughput, indicated as 300 mm equivalent wafers per hour (WPH), and very good defectivity performance, are also required to deliver large volumes of high-yielding wafers. It is therefore not surprising, that projection lithography comes out as an excellent candidate for InP photonic integration.

Lithography (type)	Resolution	Overlay (Single Machine)	Throughput (300 mm)	Defectivity
		Maskless		
EBL	6 nm	5 nm	0.005 WPH	***
DLW	500 nm	30 nm	30 WPH	**
IBL	6 nm	30 nm	0.1 WPH	*
SPL	5 nm	5 nm	0.01 WPH	**
		Mask-based		
NIL	20 nm	2.5 nm	90 WPH	**
Contact	500 nm	250 nm	160 WPH	*
Projection	13 nm	1.4 nm	125 WPH	***

*** Very Good, ** Good, * Moderate

Table 1.2: Lithography capability comparison, showing resolution, overlay, throughput and defectivity, assuming 1% write area for maskless technologies for determining throughput in 300 mm wafer equivalents.

In recent years, Silicon photonics platforms have been able to exploit the existing high-resolution manufacturing infrastructure of the traditional electronics industry. This advantage has allowed the manufacturing of devices with ArF 193 nm immersion lithography used for technology nodes as low as 28 nm [46, 47]. It is, however, important to create precision photonic components on InP substrates that enable monolithic integration with lasers and high efficiency optoelectronic devices. So far, generic InP platforms have been restricted to the use of e-beam, stepper and contact lithography. For the volume production of PICs, stepper lithography is needed, but minimum feature sizes have been limited to 250 nm [5]. This limitation comes from the fact that the shortest wavelength illumination and highest performance imaging have only been available for the latest large silicon wafer diameters. While 4-inch InP wafers are used for high volume photonic devices and 6-inch are starting to become available, the InP industry has mostly been operating on substrates of 3-inch for high functionality PICs.

In 2011 an ASML PAS5500/1100B was installed at the NanoLab@TU/e cleanroom in Eindhoven and modified to be, to our knowledge, the only scanner in the world to allow for 100 nm resolution exposures with 15 nm overlay, at high speeds on InP substrates as small as 3-inch. In 2013, a PAS2500/40 stepper was also installed with up to 800 nm resolution and 250 nm overlay. This machine could replace most traditional contact lithography steps and enabled an upgrade in terms of overlay, dimension control and defectivity. A photograph of both these tools is shown in Fig. 1.9.

Figure 1.9: ASML equipment: PAS5500/1100B (left) and PAS2500/40 (right).

1.5 Lithography challenges for InP photonics

Due to physical limits that determine how to interact with light, minimum feature sizes of photonic components [48] do not scale down as far as state-of-the-art electronics [49–52]. However, uniformity tolerances on CD are exceptionally strict for photonic components despite their size, because the CD directly influences the effective index [46, 53]. Opposed to the requirements on dimensional control, stands the cost of exploitation of the fabrication technology. The choice for a particular manufacturing infrastructure is therefore always based on a compromise where the cost needs to be met with appropriate volume. The ArF scanner model installed in

NanoLab@TU/e, enables reproducible imaging down to 100 nm CD with very good overlay specifications. Less critical steps can be exposed with the installed i-line Stepper that can exploit existing resist process modules to deal with the patterned wafer topography. The transition of moving from i-line contact lithography to ArF scanner lithography has taken the silicon electronics industry close to 20 years to complete [42]. The application of such lithography in InP photonics inherently poses unique and different challenges that require extensive research to overcome as well.

To create waveguide geometries in InP, etch depths of over 1 μm are often required, while ArF resists suitable for 100 nm CD patterning only have a thickness of around 200 nm. One challenge is in fully covering the wafer topography with a uniform, high-quality resist layer and anti-reflection coatings. The aggressive CD shrink that happened in electronics, also led to scaling in layer thickness of the integrated circuit materials. Improvements in terms of wafer topography and flatness were required to deal with reduced depth of focus (DOF) implied by high-resolution lithography systems. Similarly, flatness of InP substrates needs significant improvement to enable high-resolution lithography. Many PICs require edge coupling of light to and from the chip, while maintaining phase, polarization, wavelength and intensity. Because PIC dicing is often performed by cleaving along the crystallographic plane, this requires accurate matching of the chip coordinate system to the orientation of the substrate.

Another challenge is to transfer a thin ArF lithography pattern into the semiconductor material. This requires highly selective and low critical dimension loss (CDL), hard mask patterning techniques, through the development and optimization of several uniform etch steps. In this work several process modules were developed to achieve this for a specific set of materials and applications.

Some InP photonic components will push the limits of what the TU/e scanner can resolve. In that respect, it is required to investigate methods of imaging improvement to stretch tolerances and limits of this system. Double patterning is a method that is exploited in electronics to achieve this and will be investigated. Secondly, lithographic simulation and application of off-axis illumination by using diffractive optical elements will be investigated. Lithographic simulations are also used to apply optical proximity correction (OPC) to designs, to enable structures that were otherwise impossible to image with traditional binary masking.

Other PIC components have challenging dimensions and require high performance in terms of overlay. This requires development of matching techniques between two generations of tools, which previously has never been attempted. This enables a route to high-precision photonic components in a scalable manufacturing platform.

1.6 Thesis Outline

This thesis will describe the research that was performed to introduce ArF scanner lithography for InP generic integration. It gives answers to how the exploitation of such fabrication technology can be achieved and how it enables novel developments in InP photonics through improved resolution, overlay, uniformity and reproducibility. More specifically the following research questions are addressed in the next chapters.

- Chapter 2 - What is needed to realize 100 nm resolution ArF resist patterns on InP substrates down to 3-inch? In this chapter, the ArF coating and development processes on 3-inch InP substrates are presented, as well as the challenges and requirements to perform ArF lithography on InP substrates in terms of wafer crystal orientation and flatness.
- Chapter 3 - Which generic process layers can take advantage of ArF lithography and how can the resist patterns be transferred into those layers? The integration of scanner lithography with the pre-existing generic InP process is described for the most critical mask layers. Independent process modules were defined for active-passive patterning as well as grating and waveguide definition. Improved arrayed waveguide gratings fabricated and enabled through ArF scanner lithography are presented.
- Chapter 4 - What can be done to improve imaging quality near the resolution limit of the scanner? A method is shown to simulate, measure and improve imaging quality for specifically InP distributed Bragg reflector grating device fabrication.
- Chapter 5 - How can the gap between design intent and fabricated photonic structures be closed? The application of optical proximity correction was investigated, to improve pattern fidelity for InP sidewall grating devices.
- Chapter 6 - How can overlay accuracy be exploited and what new components are enabled by this? In this chapter, the results of optimizing overlay between scanner and stepper are highlighted to enable fabrication of spot-size converters and polarization converters in the generic InP platform.
- Chapter 7 - In this chapter, conclusions are drawn from the research that was performed and an outlook for future work to be done on this subject is provided.

Chapter 2

ArF lithography on InP substrates

2.1 Introduction

Lithography solutions for InP photonics platforms have in a sense been bound by the available diameters of high-quality material substrates. In fact, the ASML PAS5500/1100B scanner that was installed at the NanoLab@TU/e cleanroom in 2011 was originally developed to support 200 and 300 mm substrates only. The initial intention of the TU/e research proposal for this equipment was to harness the 100 nm technology node capability of this tool generation, by exposing small InP wafers on top of a 200 mm carrier wafer.

This way of working however, automatically imposes some undesirable inaccuracy in terms of leveling and overlay. Additionally, this method would require some degree of manual handling to mount the wafer, which would impact particle related defectivity performance and throughput. It was therefore proposed by ASML to modify this machine's hard- and software, based on their experience with small wafer diameter steppers of the same platform generation. This effort resulted in the world's first ArF deep ultra-violet (DUV) scanner, able to handle 3-inch InP substrates for native cassette to cassette 100 nm resolution exposures, with a possibility to scale up to larger wafer sizes.

The methods to apply ArF lithography to achieve 100 nm resolution on InP substrates however, were not known prior to this work. This chapter describes the infrastructure requirements and challenges to perform ArF scanner lithography for the first time on small InP substrates. The development of the resist processing recipes is presented along with experimental results on process delay sensitivity. The next section discusses the substrate requirements in terms of flat-cut accuracy and the impact of wafer flatness improvement on critical dimension uniformity (CDU). Finally, conclusions are drawn from the chapter.

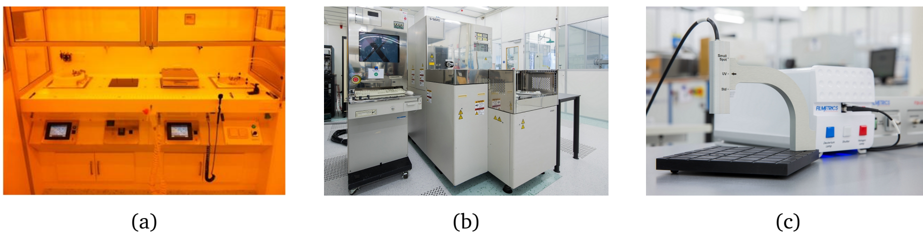
2.2 Composition of an ArF infrastructure

Prior to this work, the TU/e generic process was using broadband (g-line, h-line and i-line) contact lithography with manual microscope alignment. This was limited to a minimum CD of approximately 800 nm with overlay errors in the region of 1 μm. From these numbers it is clear, that the capabilities of a scanner with a minimum CD of 100 nm and overlay errors less than 15 nm are a significant improvement. The requirements for performing ArF DUV lithography near the scanner's resolution limit however, are significantly more stringent than for contact lithography.

A multi-layer coating is required to reduce reflections during the exposure that could lead to dimensional variation. Layer thickness and uniformity need excellent control and reproducibility for each of the three layer coatings: bottom anti-reflection coating (BARC), photoresist (PR) and top anti-reflection coating (TARC). The DUV chemically amplified resists are known to be very susceptible to specific volatile compounds [54], requiring chemical filtering of the wafer environment. Lastly, due to the thickness of these coatings, particle contamination as well as local wafer topography due to circuit geometry, can be challenging.

In industry such coatings are commonly applied with advanced automated and integrated "track" systems which control the local environment, baking temperatures, spin speeds and timing with very high precision and throughput [39, 55–57]. With only a limited amount of cleanroom space available in the dedicated compartment of the ArF scanner, it was decided that semi-automatic equipment would be installed inside a pre-existing wet bench for the chemical processing. Based on specifications deduced from ASML's experience with ArF processes, Brewer Science' "Cee(X)" process equipment was carefully selected, modified and installed for processing of the lithographic layers.

In total, four tools were installed to do the processing as is illustrated by the photograph in Fig. 2.1a. A spin coater and developer unit with recipe controlled dispense sequencing, acceleration and spin speed control, frontside rinse, backside rinse, chemical dispense lines and a wafer-centering mechanism. A hotplate with recipe controlled timing, lift pin position sequencing, accurate temperature control, and uniformity. A chill plate with active cooling and manual lift pin control. With these tools, apart from manually transferring wafers from one step to the other, all process related aspects can be done automatically.



(a) (b) (c)

Figure 2.1: ArF infrastructure: Brewer science resist processing equipment (a), Hitachi CDSEM (b), Filmetrics reflectometer (c).

To complement the ArF lithographic capability of the cleanroom, it was also required to install suitable metrology equipment to quantify the processing results. A critical dimension scanning electron microscope (CDSEM) is a programmable microscope specialized to perform automated top-down measurements. This is particularly necessary for ArF processing, because this type of resist is known to be very susceptible to deformation under the influence of an electron beam [58,59]. Fully automated measurements enable repeatable fast results, with minimal deformation of the resist patterns, contrary to manual scanning electron microscope (SEM) inspection. A Hitachi S9200 CDSEM was installed in 2013 and customized to handle small substrates using a carrier construction (Fig. 2.1b). In this construction, a 3-inch InP substrate is mounted on top of a 200 mm silicon carrier wafer with a clamping mechanism. Utilizing this carrier construction, the equipment was able to satisfy the need for reliable automated CD measurements. A Filmetrics reflectometer as illustrated in Fig. 2.1c was installed in 2015, to measure coating thickness and uniformity. Prior to this installation however, for the initial recipe developments described in the following sections, a KLA ASET F5 ellipsometer at ASML was used for this purpose.

2.3 ArF Resist Processing

ArF coatings are mostly used by high volume production sites in semiconductor industry. Resists are typically chosen for imaging performance and process requirements like plasma resistivity, viscosity for achieving certain thickness and sometimes chemical compatibility. Unfortunately, because of the mainly industrial demand, these coatings are mostly available in large quantities. With the short expiry dates on these chemicals, the university was fortunate to sample smaller quantities via ASML's process lab within the existing collaboration. For the work described in this thesis, a selection of chemicals was used, that was provided to us by ASML and suitable for 100 nm node ArF patterning. These chemicals are listed in Table 2.1.

Chemical Name	Type	Thickness	3σ
JSR NFC TCX041	TARC	90 nm	$<$ 1.5 nm
TOK TARF-P6111 ME	PR	225 nm	$<$ 2.5 nm
AZ ArF-1C5D Coating 30	BARC	38 nm	$<$ 1.5 nm
FUJIFILM RER 500	Organic Solvent	-	-
FUJIFILM OPD5262	Developer	-	-

*- = Not applicable

Table 2.1: List of selected ArF Chemicals with thickness and uniformity targets.

The recipes for applying each of the coatings, were optimized with a technique called design of experiments (DOE). The basis of this method is described in Appendix A, whereas the results and interpretation of the performed experiments are discussed in the following sections. Target layer thickness and uniformity specifications for each coating were provided by ASML, based on their lithography simulations

of a selection of representative photonic structures: waveguides, arrayed waveguide gratings (AWGs) and distributed Bragg reflector (DBR) gratings. These values are listed in Table 2.1, where the uniformity specification limit is defined as the 3σ layer thickness distribution over the wafer in nm.

2.3.1 Coating recipe development

In collaboration with Brewer Science, starting-point recipes were set up to coat the BARC, PR and TARC layers. For each of these chemicals, a spin curve (spin speed versus thickness plot) was first determined to approximate the target layer thickness. Then, the recipes were tuned further to meet the requirements from Table 2.1 for each particular coating. The initial recipe setup was performed on 200 mm silicon wafers, because at the starting point of the project, the scanner qualification would be done using this wafer diameter. It was found that the coating recipes showed identical performance on smaller InP substrates and did not require re-optimization. Layer thickness measurements were performed by ASML with a KLA ellipsometer with a 49-point radial pattern at 8 mm edge exclusion. Fig 2.2 shows a top down representation of this measurement pattern. The average thickness as well as the 3σ coating uniformity were derived from these measurements.

During optimization of the coatings, it was found that a few modifications to the spin coater hardware were required. First, a splash ring was installed ensuring that material that was spun off the wafer, would be deflected downwards without risk of landing back onto the wafer. Secondly, it was found that a glass cover plate with holes in the lid of the spin bowl, improved the airflow through the system, preventing solvent aerosols to land back on the wafer and cause coating defects.

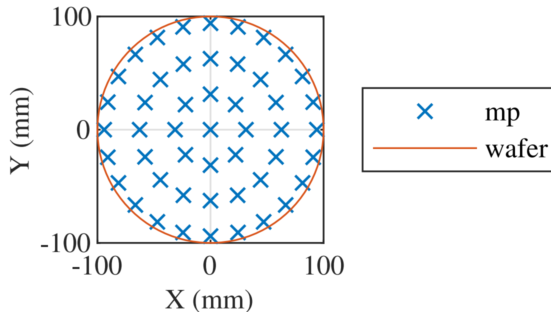


Figure 2.2: KLA ellipsometer radial layer thickness measurement point pattern on 200 mm wafer with 8 mm edge exclusion.

2.3.1.1 Bottom anti-reflection coating results

The spin curve for the BARC is shown in Fig. 2.3 and shows the obtained layer thickness as a function of the spin speed. Based on this result, a speed of 1750 RPM was chosen as a center point (CP) for the subsequent DOEs. A representation of the coating recipe for the BARC is shown in Table 2.2 including the hardbake step. For this

layer, a “dynamic” dispense method was applied to achieve good coating integrity and uniformity. This means, that the dispense happens while the wafer is actively spinning in step 2, to spread the chemical over the entire wafer surface. After the dispense step, the spinspeed is further increased in step 3, to reach the appropriate thickness for the layer. In step 4-6, the edge bead removal (EBR) and back side rinse (BSR) are performed. These steps make sure that the backside and edge of the wafer are free from coating residues that could contaminate the exposure tool.

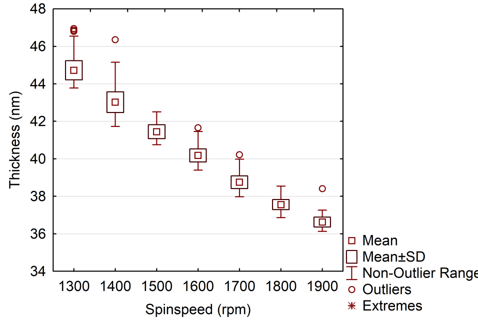


Figure 2.3: Spin curve for 1C5D BARC coating, thickness as a function of spin speed.

Step	Speed	Acceleration	Time	Dispense	Exhaust
1	1000 RPM	5000 RPM/s	3 sec		50%
2	1000 RPM	5000 RPM/s	2 sec	1C5D	50%
3	1750 RPM	5000 RPM/s	45 sec		50%
4	250 RPM	5000 RPM/s	3 sec		100%
5	250 RPM	5000 RPM/s	3 sec	EBR/BSR	100%
6	1500 RPM	25 RPM/s	30 sec		100%
Hardbake: 90 sec at 200°C					

Table 2.2: BARC coating recipe.

Two separate full factorial 2^3 DOEs were performed with duplicate randomized experimental runs and several CPs, to find optimal layer thickness and uniformity conditions for the BARC layer, as well as to determine sensitivity to the tested process parameters:

- DOE 1 - Step 3 spin speed, Step 2 dispense volume and exhaust setting
- DOE 2 - Step 2 spin speed, hardbake temperature, hardbake time

The setup and measurement results of both DOEs are detailed in Appendix B.1. Based on the analysis of this data, the step 3 spin speed has a significant influence on the thickness of the layer. An interaction between the hardbake temperature and time also has a significant influence on the thickness within the tested process regime of the

second DOE. The thickness of the BARC layer was tuned by adjusting the spin speed to meet the specifications in Table 2.1. The hardbake temperature and time were kept at the recommended setting from the chemical supplier. The uniformity was unaffected by the tested parameters and below the specification limit for all experiments. A nominal thickness of 38 nm was achieved with a 3σ distribution below 1.5 nm over the wafer. The thickness was found to have a "sombrero" shaped distribution over the wafer with greater thickness in the center and near the edge of the wafer.

2.3.1.2 Photoresist coating results

The spin curve for the PR is shown in Fig. 2.4 and shows the obtained layer thickness as a function of the spin speed. Based on this result, a speed of 800 RPM was chosen as the CP for the subsequent DOE. A representation of the coating recipe for the PR is shown in Table 2.3 including the softbake step. For this layer, a “static” dispense method was applied to achieve good coating integrity and uniformity. In this case, the dispense happens while the wafer is stationary, forming an initial resist puddle in step 2. The PR then spreads over the wafer in step 4 where the spin speed is chosen to achieve the correct thickness. The EBR and BSR are performed in steps 5-7 for this recipe.

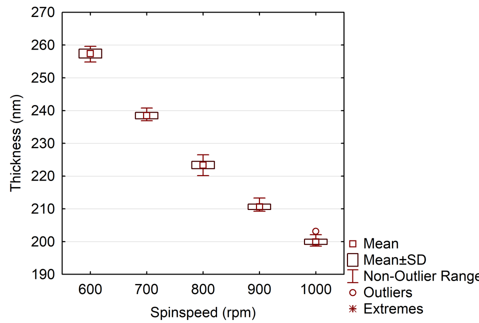


Figure 2.4: Spin curve for P6111 PR coating, thickness as a function of spin speed.

Step	Speed	Acceleration	Time	Dispense	Exhaust
1	0 RPM	5000 RPM/s	1 sec		50%
2	0 RPM	5000 RPM/s	4 sec	P6111	50%
3	0 RPM	5000 RPM/s	1 sec		50%
4	800 RPM	5000 RPM/s	45 sec		50%
5	250 RPM	5000 RPM/s	3 sec		100%
6	250 RPM	5000 RPM/s	3 sec	EBR/BSR	100%
7	1500 RPM	25 RPM/s	30 sec		100%
Softbake: 90 sec at 125°C					

Table 2.3: PR coating recipe.

It was found that this is the most difficult layer for processing without defects. Any particle in the coating material or on the wafer surface, will become highlighted by resist thickness variation, resulting in distinct color transitions. A frontside solvent rework recipe was developed based on RER 500 from Table 2.1, to fully remove the coating in case of defects. This resulted in a fast method to reattempt the coating process with minimum delay time. For the PR thickness and uniformity, a full factorial 2^3 DOE was performed with duplicate randomized experimental runs and several CPs, varying spin speed, dispense volume and the softbake temperature.

The outcome and setup of this DOE are detailed in Appendix B.2. The DOE analysis shows that only the spin speed proved to be significant for the thickness of the PR coating. This speed was tuned to meet the specifications of Table 2.1. However, for the uniformity of the coating, both the spin speed and an interaction between the spin speed and dispense volume proved to be significant. With the chosen settings a 3σ range below 2.5 nm was achieved with a nominal resist thickness of 225 nm. The distribution was observed to have a similar pattern to the BARC layer.

2.3.1.3 Top anti-reflection coating results

The spin curve for the TARC layer is shown in Fig. 2.5 and shows the obtained layer thickness as a function of the spin speed. Based on this result, a speed of 1550 RPM was chosen as the CP for the subsequent DOE. A representation of the coating recipe for the TARC is shown in Table 2.4 including the softbake step. For the TARC, a "dynamic" dispense method in step 2, gave the best results in terms of coating quality. In this recipe, the layer thickness is determined in the subsequent step 3, whereas EBR and BSR are performed in steps 4-6.

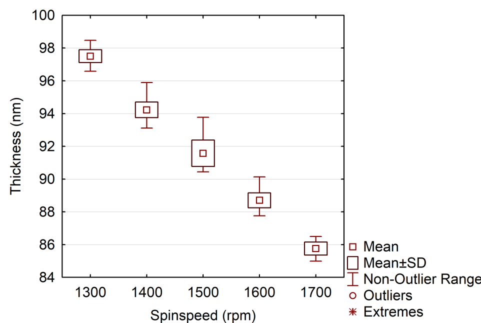


Figure 2.5: Spin curve for TCX041 TARC coating, thickness as a function of spin speed.

Apart from canceling out reflections, it was found that the TARC also plays an important role while developing wafers, which will be elaborated upon in the developer section: 2.3.2. Lastly the TARC functions as a protective coating to prevent harmful volatile components to diffuse into the sensitive PR layer during the lithography process. The following parameters were varied in a full factorial 2^3 DOE with duplicate randomized experimental runs and several CPs: spin speed, dispense volume and softbake temperature. The outcome and setup of this DOE are detailed in

Step	Speed	Acceleration	Time	Dispense	Exhaust
1	1000 RPM	5000 RPM/s	3 sec		50%
2	1000 RPM	5000 RPM/s	4 sec	TCX041	50%
3	1550 RPM	5000 RPM/s	45 sec		50%
4	250 RPM	5000 RPM/s	3 sec		100%
5	250 RPM	5000 RPM/s	3 sec	EBR/BSR	100%
6	1500 RPM	25 RPM/s	30 sec		100%
Softbake: 60 sec at 90°C					

Table 2.4: TARC coating recipe.

Appendix B.3. The spin speed proved to be a significant influence on the thickness as well as the softbake temperature. The coating uniformity was unaffected by the varied parameters with a "sombrero" shaped distribution below 1.5 nm 3σ range in all experimental runs. The recipe was tuned to reach a nominal thickness of 90 nm.

2.3.2 Developer process results

Like the coating recipes, the initial developer recipe was started on 200 mm Si substrates. It was found that the process is insensitive to the method of developer dispense to create a developer puddle on the wafer surface. CDSEM measurements were performed at ASML to compare the process window using a focus energy matrix (FEM) as described in Appendix C. These FEM wafers were treated with a post exposure bake (PEB) of 90 seconds at 126°C prior to development. The measurements revealed that with identical development times at room temperature, the recipe on the TU/e Brewer system performed identically to a fully automated process on a TEL ACT-series track at ASML. This was found, even though these tools were equipped with completely different dispense systems and puddle capabilities. The results are illustrated in the SEM pictures in figure 2.6, of dense 120 nm lines and spaces that were developed with the different systems.

The key challenge for a good development process, is in getting a uniform distribution of the OPD5262 (2.4 %) tetra methyl ammonium hydroxide (TMAH) developer

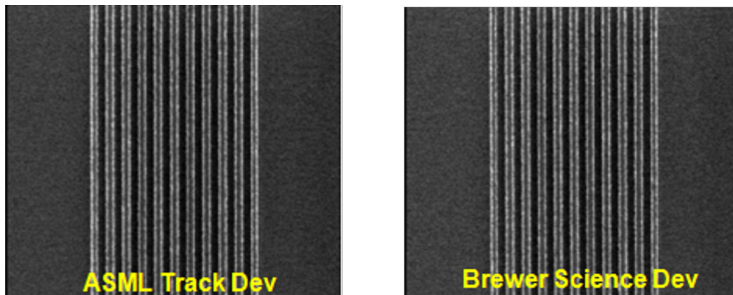


Figure 2.6: 120 nm lines and spaces on TEL ACT-series track (left) and Brewer spinner (right).

on the wafer within a short amount of time with a uniform developer concentration over the wafer. This ensures the development process starts and performs uniformly over the wafer. The details of the TMAH-based development recipe are shown in Table 2.5 including the final hardbake step. The distribution of the developer is performed with a two-step dynamic dispense in steps 1-3. In step 4, a static puddle development takes place. For terminating the development process step, it is necessary to uniformly remove the developer puddle from the wafer in step 5. The developer is then replaced by ultra-pure water (UPW) from the front side rinse (FSR) line, while simultaneously rinsing the backside of the wafer with the BSR line in step 6 and 7. In the last step, the wafer is dried by removing the remaining UPW at high speed.

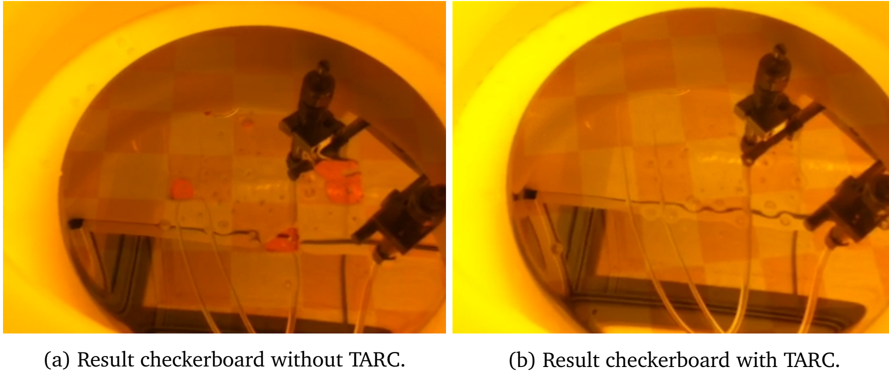
PEB: 90 sec at 126°C				
Step	Speed	Acceleration	Time	Dispense
1	15 RPM	5000 RPM/s	1 sec	
2	15 RPM	5000 RPM/s	1 sec	OPD5262
3	500 RPM	5000 RPM/s	2 sec	OPD5262
4	0 RPM	5000 RPM/s	20 sec	
5	1000 RPM	1000 RPM/s	2 sec	
6	1000 RPM	5000 RPM/s	20 sec	FSR/BSR
7	1000 RPM	100 RPM/s	10 sec	BSR
8	2000 RPM	100 RPM/s	30 sec	
Hardbake: 90 sec at 160°C				

Table 2.5: PEB and TMAH-based developer recipe.

As stated in the previous paragraph, the presence of the TARC proved to be a critical parameter for achieving a good developer distribution. An experiment was performed to confirm the influence of the TARC layer on the developer distribution. Fig. 2.7 shows photographs of two 200 mm wafers during the static puddle phase. These wafers were exposed with a high-transmission design image in a checkerboard pattern where half the fields remained unexposed. The wafer shown in Fig. 2.7a was not coated with a TARC layer, while the wafer shown in Fig. 2.7b was.

In in Fig. 2.7a can be seen that the fields that were unexposed with DUV light are very hydrophobic. The developer being an aqueous TMAH solution, is repelled by the unexposed resist which causes a non-uniform distribution of developer over the wafer. This in turn causes the development process step, not to start uniformly over the wafer and gives very poor results in a situation where an even larger part of the wafer area would remain unexposed. In Fig. 2.7b, the TARC was applied on the wafer. This causes the developer to distribute evenly over the entire wafer independent of the resist being exposed or not.

It is clear from these results that the coating of the TARC layer is needed for multiple reasons. For small feature sizes, the TARC will cancel out reflections which can be detrimental to imaging quality and dimensional control. Secondly, even if structure dimensions are too large to profit from the removal of these reflections, the developer distribution can be improved in low transmission designs making the developer pro-



(a) Result checkerboard without TARC. (b) Result checkerboard with TARC.

Figure 2.7: Photographs of developer wetting during puddle phase on 200 mm wafers.

cess step independent of the design density. Lastly the TARC will function as a barrier that can protect the PR from being contaminated by volatile chemical compounds in the environment. This subject is further discussed in section 2.3.3 on critical process delays in ArF lithography.

2.3.3 Process delays in ArF lithography

During the development of the lithography process, it was found that there are several stages at which the delay between consecutive steps is very critical. This is mainly because once coated, the chemically amplified resist is susceptible to interaction with volatile compounds that can dissolve into the layers and influence the intended chemical reaction of the lithography process [54]. As an example of this effect, Fig. 2.8 shows a trend of increasing resist contamination on a 120 nm LS pattern. The 200 mm wafer with this pattern, was contaminated during the transport from the TU/e to ASML, with several hours delay between the PEB and the development process steps. The SEM photographs were taken from the center of the wafer towards the edge. The left-most pattern (center) is still unaffected while on the next patterns, degradation can be observed. Eventually, there is complete loss of pattern definition on the right-most pattern (edge) turning the LS pattern into a single resist block.

The sensitivity of the ArF resist processing scheme to this failure mechanism, was tested for two delay situations that could occur in practice when fabricating wafers. Due to the required baking temperatures of the DUV coatings, cooldown and warmup

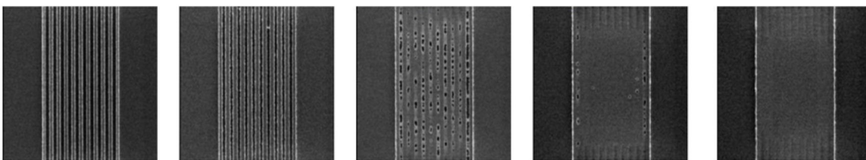


Figure 2.8: Effect of increasing pattern degradation from center to edge of a 200 mm wafer, due to resist contamination on a 120 nm LS pattern.

times of the hotplate, limit the total wafer throughput. It would therefore be efficient to coat wafers well in advance of doing the exposures. In this scenario the wafers would be waiting for the exposure step and could be affected by contamination. A second delay scenario that was predicted to be even more critical, is directly after the exposure when the PR is activated by the DUV light. This could in practice happen when wafers get stuck inside the system or when the hotplate is still busy adjusting to the PEB temperature.

An experiment was performed to test the delay sensitivity between the final coating step and the exposure of the wafers. A batch of 6 wafers was coated simultaneously with the full ArF coating process described in the previous sections. Half of the wafers were directly exposed, treated with PEB, developed, and hardbaked. The remaining wafers were stored under standard conditions, in a closed process box inside the cleanroom, for 48 hours prior to the remaining process steps. To quantify the result, extensive CDSEM measurements were performed on 600 locations per wafer on 200 nm isolated trenches, to determine the average CD and the distribution.

Fig. 2.9 shows boxplots of the CDSEM results of reference wafers without delay in blue, as well as wafers with a 48 hours exposure delay time in orange. The points inside the interquartile range boxes represent the median CD while the whiskers represent the non-outlier ranges of the measured wafers. From this data can be concluded that the mean CD of the trenches, deceased by more than 25% due to the prolonged storage of the wafers. This shift is larger than what was experienced from the wafer to wafer and batch to batch reproducibility of the exposure process. The exposure delay caused poor imaging performance which not only became evident in the CD, but also in the definition quality of the trenches by increased line edge roughness (LER). From experience with this material combination, it was found that prolonged storage deactivates the photo-active component in the resist, when stored longer than 24 hours.

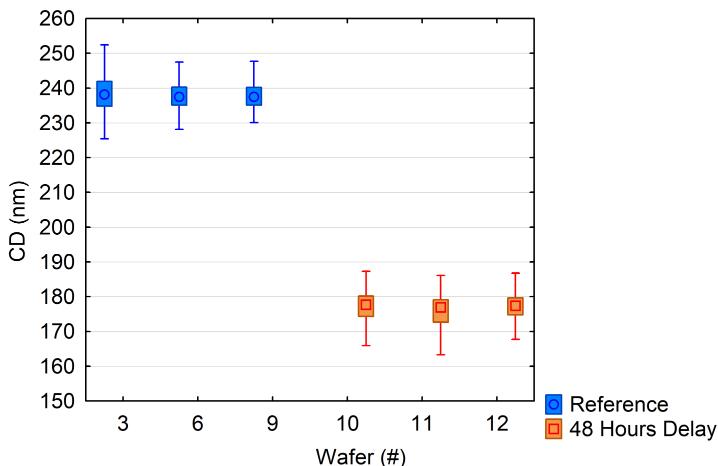


Figure 2.9: CDSEM results of the effect of a 48 hour exposure delay.

In a second experiment, the delay time between the exposure and the PEB was tested. For this experiment, several wafers were coated and exposed on the scanner. The PEB delay time was then varied between 0 minutes and 3 hours. After the variable delay times, the wafers were given a standard PEB, followed by standard development and hardbake. CDSEM measurements were then performed on 600 locations per wafer on 200 nm isolated trenches.

Fig. 2.10 shows the median CD of these wafers as the points inside the interquartile ranges of the boxes, while the whiskers represent the non-outlier ranges of the measured wafers for each PEB delay time. From this data can be seen that the size as well as the distribution of the trench CD is strongly influenced by the delay time. A clear trend is visible where the median CD and uniformity starts drifting away beyond 1 hour delay and imaging becomes worse to completely impossible after 3 hours delay. On these wafers it was observed that the outside dies were first affected by the contamination mechanism, spreading towards the center over time. The edge dies are more sensitive because the focus is less accurate when the level sensor is partially outside of the wafer. Based on this experiment, a maximum delay time of 1 hour between exposure and PEB was enforced in the working procedure.

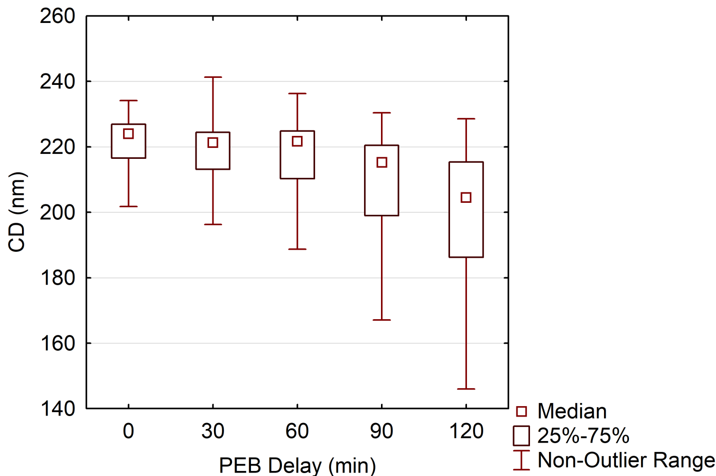


Figure 2.10: CDSEM results for wafers with different PEB delay times.

2.4 Substrate quality requirements

There are two aspects with relation to substrate quality that cause concern when introducing 100 nm wafer scale scanner lithography. In the next section, the matching of the crystallographic orientation with the PIC pattern orientation is first investigated. Secondly, the overall InP substrate flatness is a point of concern. It is very well known that for projection lithography, high resolution comes at the cost of reduced depth of focus [40]. This has direct implications for the wafer flatness requirements

of InP substrates, which were unprecedented prior to this work. The experimental results that link wafer flatness to CDU for realistic photonic structures are presented. Simultaneously, the substrate improvements, from the project collaboration with In-PACT as a substrate supplier, are highlighted.

2.4.1 High precision flat

In addition to electronic input/output (IO) channels, PICs also require optical coupling to the outside world. Although different schemes are implemented to realize this, one of the predominant methods is edge-coupling. This means that a chip is typically cleaved through the IO waveguides, along to the crystallographic plane of the wafer. This creates a mirror-like facet that can have a large influence on the coupling efficiency of the chip. To guarantee the accuracy of the position of the cleave as well as the quality of the facet, it is important to make sure that the chip patterns are accurately aligned to the crystallographic plane. There are two factors that play a role in the pattern to crystal alignment as illustrated in Fig. 2.11.

First, there is the accuracy of the creation of the wafer flat. When a substrate ingot is grown from a mono-crystal the exact orientation is in principle known. It is therefore up to the substrate supplier to make sure that the flat cut is done in this exact orientation. At the start of this work, the accuracy of the flat could only be guaranteed below a rotation offset of 3.5 mrad. During our collaboration, the accuracy of the flat cut, the measurement methods, and selection criteria at the substrate supplier were improved. This resulted in the capability to have a high precision flat, which improved the accuracy by an order of magnitude to a maximum rotation offset of 350 μrad.

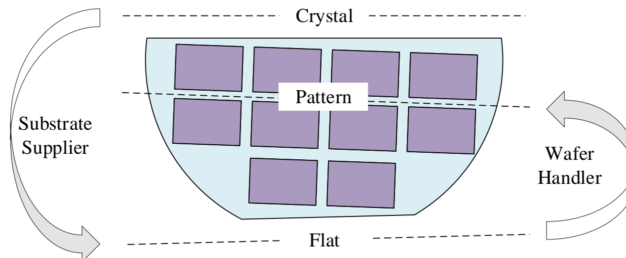


Figure 2.11: Illustration of wafer pattern orientation relative to flat and crystal orientation.

The second factor that plays a role, is the edge sensor of the wafer handling system of the scanner. This sensor scans the edge of the wafer to determine the flat position after it is placed on the pre-aligner. It then corrects the orientation of the wafer in such a way, that the internal robot (dipod) can place it on the wafer stage in the ideal position. The specification for the reproducibility of the edge sensor, is to have a standard deviation below 30 μrad. Apart from the reproducibility however, the average absolute positioning of the wafer plays a role. It is therefore important to calibrate the offset between the physical flat and a pattern that is printed based on the registration of the flat position. It was found that a systematic offset was required

to make sure that resist pattern matched with the physical flat orientation. With this additional value, it is possible to keep the wafer handling system calibrated at zero rotational offset, using a standard calibration wafer, meeting the edge sensor specification.

2.4.2 Wafer flatness

For scanner lithography, as with other forms of projection lithography, the minimum critical dimension CD of a LS pattern that can successfully be printed with below 10% CDU, can be derived from the Rayleigh criterion [40]. As described by (2.1) there is a direct dependency on the exposure wavelength (λ), 193 nm specifically for ArF type excimer laser light sources used in this study. The minimum CD also depends on the numerical aperture (NA) of the lens system installed on the exposure tool and a constant (k1) representing the applicable lithography processing conditions. The maximum NA of the examined system is 0.75 while the k1 for the studied process is 0.4. As shown in (2.2), a usable DOF can similarly be derived from the Rayleigh criterion to show a strong dependence on the same hardware defined parameters of wavelength (λ), (NA), and the processing constant (k2) with a value of 0.9.

$$\mathrm{CD} = k_1 \frac{\lambda}{NA} \tag{2.1}$$

$$\mathrm{DOF} = k_2 \frac{\lambda}{NA^2} \tag{2.2}$$

The DOF represents the tolerable distance along the optical axis of the lens in which the aerial image of the lithography process remains sharp. From the combination of these two equations, a reduction in minimum CD leads to a quadratic decrease in the DOF. This decrease has direct implications for the requirements with regard to the local flatness of the used wafers. Although lithography systems are typically equipped with sophisticated leveling systems to correct wafer topography in a global sense, local topography cannot be corrected. From a wafer manufacturing point of view, the local flatness is strongly related to the global flatness of a wafer. Therefore, the detected level sensor range can be used as a figure of merit to measure and compare wafers. This value equals the total z-range, of all the focal plane fits that are performed by the level sensor system, during the exposure of the wafer.

Due to the ever-increasing demand for smaller feature sizes in the electronics industry, wafer flatness of large silicon substrates was gradually improved to meet sub-micrometer total thickness variation on mass production substrate sizes [60]. In the InP industry however, this demand has only recently crystallized and lithography methods with relatively large DOF have previously been sufficient. In the following paragraphs, we highlight the results of the cooperation with InPACT as a substrate supplier, to improve the flatness of InP wafers.

Wafers with several flatness ranges were exposed on the DUV scanner with a 200 nm isolated trench design. All wafers were coated with TOK P6111 photoresist, AZ 1C5D bottom anti-reflective coating, and JSR TCX041 top anti-reflective coating. The layer thickness uniformity of these coatings, determined at 3 times the standard

deviation across the wafer, was measured to be below 1.5, 2.5, and 1.5 nm respectively on ultra-flat double side polished (DSP) silicon wafers, having a negligible effect on the DOF. Conventional illumination conditions as described in Section 4.4, were used with a numerical aperture of 0.75 and a σ setting of 0.366. After post exposure baking, the wafers were developed with Fujifilm OPD5262 and hardbaked. The trench widths on at least 600 measurement dies of each wafer were measured using a Hitachi S9200 CDSEM.

Fig. 2.12 shows CDU, defined as the size distribution of 200 nm trenches at three times the standard deviation for each measured wafer. The CDU data were plotted as a function of the measured global wafer flatness by the level sensor of the exposure tool. In this figure, the CDU values of standard single side polished (SSP) InP wafers are compared to both DSP InP and ultra-flat DSP InP wafers which have undergone an even further improved polishing process. The InP wafers are also compared to ultra-flat DSP Si wafers which represent the flatness benchmark for 3-inch wafers.

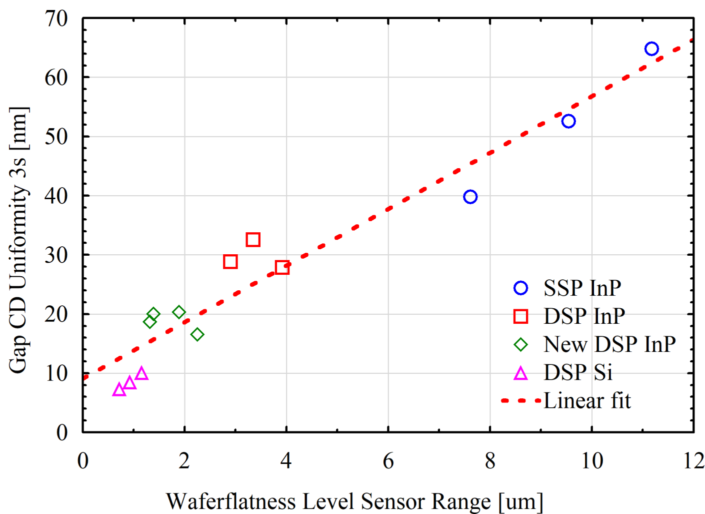


Figure 2.12: CD uniformity results of 200 nm trenches as a function of level sensor range [61].

Polishing both sides of the InP wafer results in a significant improvement of the overall wafer flatness. This process pushes the measured level sensor range from around 8-12 μm down to a 3-4 μm range. However, this is not enough to print 200 nm trenches with 10% wafer uniformity, resulting in a CDU of around 30 nm. By improving the polishing process, the level sensor range can be reduced further to around 2 μm with a result of 20 nm CDU on the 200 nm trenches. This comes quite close to ultra-flat Si reference wafers which have below 1 μm range and typical CDU values below 10 nm. With flatness of recent DSP InP substrates reaching below 1 μm range, imaging of 100 nm features is also possible on InP.

2.5 Conclusions

To achieve 100 nm node patterning results on a 3-inch wafer scale, it is necessary to install and modify an entire ArF infrastructure. This consists of the exposure tool, the resist processing equipment as well as metrology tools to determine layer thickness and realized pattern CD. Layer thickness and uniformity results were optimized for each coating, meeting specifications that enable a lithography resolution of 100 nm.

When PICs require edge coupling, it is necessary to optimize the flat orientation and the scanner wafer handling to match with the crystal orientation of the substrate. In collaboration with the supplier, the accuracy of the flat orientation was improved by an order of magnitude to 350 μrad. The scanner handling was recalibrated to match with the flat orientation to establish the correct coordinate system for the PIC patterns.

Because of the limited DOF of ArF lithography, substrate flatness was improved in collaboration with InPACT. Overall wafer flatness of reference material was improved from 10 μm range on SSP substrates, to below 2 μm range on improved DSP substrates. This improvement resulted in below 20 nm 3σ CD variation for 200 nm isolated resist trenches. Further reduction of the overall wafer flatness to 1 μm should improve these CDU results even further as was demonstrated on DSP silicon wafers. The continuous improvement of InP substrate flatness, paves the way for high-resolution wafer scale lithography.

Chapter 3

Generic ArF patterning process modules

3.1 Introduction

Prior to the work described in the previous chapter, ArF lithography on InP substrates had not been demonstrated. As a consequence, novel process integration solutions needed to be developed to perform the patterning. The resulting process step combinations are referred to as process modules. Transferring a high-resolution pattern from a temporary ArF resist layer into the permanent layers that constitute a generic PIC can be very demanding. In the TU/e process, many photonic component layers require significantly more etch depth than 100 nm technology node electronics, or need to be defined on layers that are untreated with planarization methods. This leads to process integration schemes that require extremely high selectivity, directionality as well as uniformity at wafer level, and compatibility with the material system of the platform. It is therefore very challenging to replace all existing i-line lithography steps by DUV, and this work is focused on the process modules of the PIC manufacturing flow that can benefit most from ArF lithography.

In this chapter, the introduction of ArF patterning for three independent process modules is investigated. In the first section, wet ArF patterning is applied for active-passive butt-joint integration in the TU/e generic process technology with the main purpose of defining a reference coordinate system while simultaneously exposing the first device layer. The resulting process module is presented and challenges with respect to marker strategy and wafer quality as a result of epitaxial regrowth are discussed. In the second section, 240 nm pitch grating patterns made with ArF lithography, are used for the first time as a scalable alternative to EBL, for fabricating integrated laser building blocks. Lastly, a process module is presented that uses a novel double hard mask process, to transfer an ArF pattern into InP material for waveguide definition. The obtained CDU improvements are supported by experimental results of a fabrication run and ultra-low excess loss, ArF enabled AWGs are demonstrated.

3.2 Active area patterning

At the start of the TU/e generic PIC manufacturing flow, the active layers of approximately 500 nm thickness, are grown on top of ultra-flat DSP InP wafers with atomic layer precision in terms of flatness, by metal organic vapor phase epitaxy (MOVPE) [62, 63]. Subsequently, during the active lithography stage, the structures are defined that will remain on the wafer, to be integrated with the passive parts of the PIC, through butt-joint regrowth processing [5, 6]. This process is schematically represented in Fig. 3.1a-c together with a SEM photograph of an actual butt-joint transition Fig. 3.1d. After lithography and pattern transfer, the active areas are protected with a silicon oxide hard mask, and the material is removed on the unprotected areas in Fig. 3.1a. Then, the passive layers are grown in these open areas in Fig. 3.1b. The hard mask is subsequently removed, and lastly the top cladding layers are grown on the entire wafer in Fig. 3.1c.

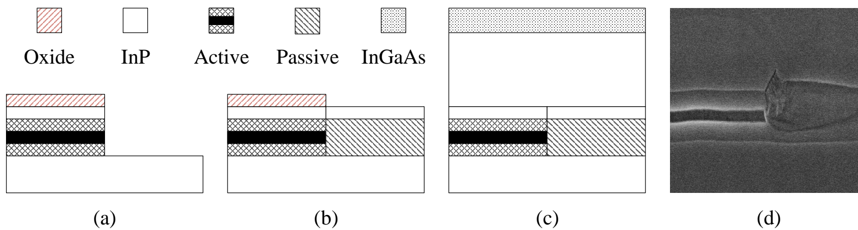


Figure 3.1: Active-passive integration process: active layer masking and removal (a), epitaxy of passive layer (b), top cladding growth (c), and SEM photo of butt-joint (d).

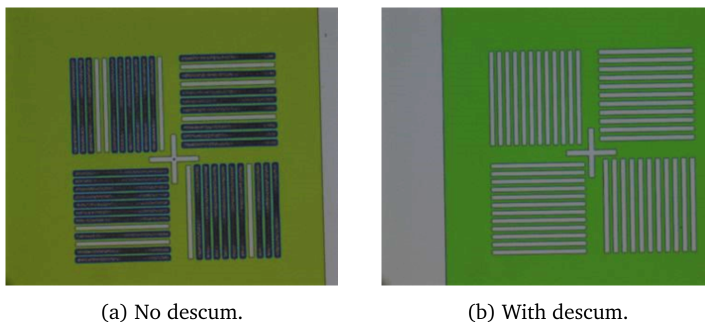
At the active lithography stage, there is no existing topography from previous mask layers, and it is necessary to establish the reference coordinate system aligned with the crystal orientation of the wafer, as explained in Section 2.4.1. A process module is described in this section that is suitable for defining both the alignment markers and the silicon oxide active mask simultaneously with the TU/e scanner. Solutions are discussed to preserve the marker quality throughout the process, to ensure all subsequent device layers can be accurately aligned.

3.2.1 Patterning process considerations and results

Since the active patterns and markers have a CD in the 10 μm range, it is not required to have anti-reflection coatings for this layer. Secondly, the BARC layer is an organic layer that requires a plasma etch to open which would require additional processing steps. It was therefore decided to remove the BARC layer from the ArF coating stack. The second purpose of the BARC layer however, is to promote adhesion of the PR layer. It was observed, that by coating just the resist stack on top of the dielectric hard mask, the subsequent buffered hydro-fluoric acid (BHF) wet etch, would delaminate the resist and destroy the entire mask layer definition. A primer procedure with hexamethyldisilazane (HMDS) [40] was therefore introduced to this process module to prevent this.

Like the BARC layer, the TARC is not needed from an anti-reflection point of view. However, the TARC is required for developer distribution reasons as was described in Section 2.3.2. This layer was therefore included in the active patterning process module. Because no plasma etching is performed in this module with the ArF resist as a mask, no post-development hardbake is required in the resist processing. The hardbake step was therefore removed from the process module.

It was also observed that during the silicon oxide mask wet etch with BHF, surface wetting was an issue on narrow structures such as the trenches in the marker quadrants. Fig. 3.2a shows an example of a marker pattern where the BHF did not fully penetrate these open areas to remove the dielectric layer. This resulted in dark areas with residual oxide, which causes the marker to be unusable for alignment of subsequent layers. A descum process is a plasma treatment that can be applied to remove organic residues, reduce resist footing, or modify material surfaces. Fig. 3.2b shows the result of the same marker structure with a low power oxygen descum process (5 min. 50 W) performed on the resist pattern, to improve surface wetting of the BHF etch. From this experiment can be concluded that the active pattern generation can be performed with ArF lithography, without a BARC layer and with a descum process, followed by the BHF etch and a clean. Table 3.1 shows an overview of the entire process module for ArF enabled active definition.



(a) No descum. (b) With descum.

Figure 3.2: Photograph of marker pattern after active layer BHF wet etching.

Step	Description
1	Hard mask deposition
2	HMDS primer
3	ArF PR and TARC coating
4	ArF exposure
5	PEB and development
6	Descum
7	BHF wet etch
8	Cleaning

Table 3.1: ArF enabled active area patterning process module steps.

The active process module was applied to a test design containing active areas with different sizes. Fig. 3.3 shows an example of an active area after wet etching the dielectric layer. This figure shows a successful definition of an active area with a visible under-etch of the oxide mask on the inside of the ArF resist mask.

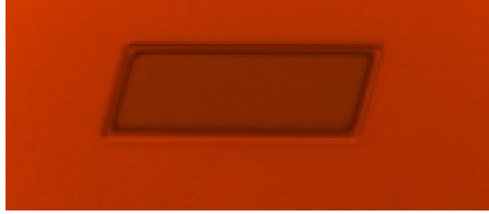


Figure 3.3: Example of ArF resist under-etch after BHF hard mask etching prior to cleaning.

3.2.2 Solutions for preserving marker quality

Two main options with regards to marker strategy were investigated to preserve marker quality throughout the manufacturing process. First, the markers can be defined simultaneously during the active definition as described in the previous section. It was found however, that the marker gratings in this case are strongly affected by local growth enhancement during the epitaxy. During the MOVPE regrowth process, the cracked metal organics diffuse off the dielectric mask, and increase the growth rate at the edge of the mask areas [63]. Fig. 3.4 shows a step height measurement obtained with a KLA Tencor Alpha-Step IQ surface profiler, across a regrown marker as highlighted with the red arrow on the blue marker.

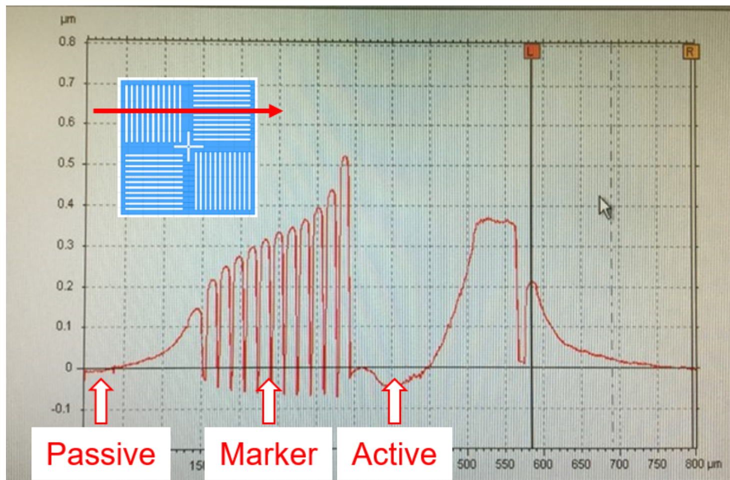
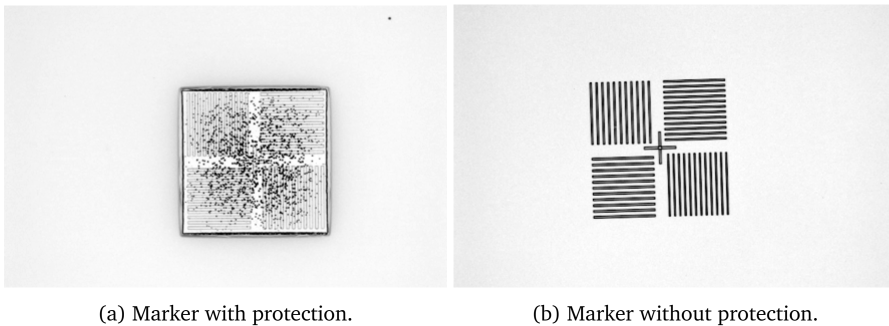


Figure 3.4: Example of step height measurement on active defined marker showing increasing step height on the grating towards the middle on the marker.

This figure shows evidence that the growth enhancement is higher towards the center of the marker. This causes asymmetry on the markers which in turn distorts the readout of the marker signal and definition of the coordinate system of the subsequent layers. In the low volume research runs that were performed with such markers, most wafers could still be aligned. However, they were found to be too unreliable for foundry scale production volumes, suffering from overlay errors in the nm to μm scale and sometimes even wafer rejects, resulting in yield and lead time loss.

Secondly, there is an option to define markers in a preparatory process stage (zero-layer) to the device layers. In this case, the challenge is to preserve the marker signal quality throughout the entire process, in particular when following up with less forgiving alignment systems of a stepper. This can be achieved by protecting the marker, or by fully overgrowing it during the MOVPE steps. In the case where the marker remains protected during the active definition, parasitic nucleation of semiconductor material can occur on top of the mask [63], as shown in Fig. 3.5a. These defects on top of the marker will distort the alignment signal. When the marker is unprotected however, the marker will stay clean as shown in Fig. 3.5b, but the duty cycle of the markers will shift due to the growth on top of the etched marker. This causes inaccuracy in the readout of the marker as well, and since the active layer removal is crystal orientation dependent, it can cause different behavior for the vertical and horizontal segments of the marker.



(a) Marker with protection. (b) Marker without protection.

Figure 3.5: Photographs of zero-layer defined markers scenarios.

In the marker protection scenario with a zero-layer, it is possible to make use of smaller scribe lane markers. These markers have separate images for the X and Y alignment zones. Due to the 700x70 μm rectangular dimensions of these marker images, they can be conveniently placed in a scribe lane rather than reserving a relatively large 400x400 μm square area for a traditional ASML primary marker. More importantly, these scribe lane markers are smaller than the diffusion length of the species inside the reactor which prevents the parasitic nucleation during the MOVPE regrowth. The readout of such markers however, is not possible with the less advanced alignment system of the TU/e PAS2500 stepper. A secondary set of standard primary markers would still need to be defined after the active-passive stage to work around this.

3.2.3 Effects of butt-joint integration on wafer backside quality

As discussed in the previous chapter, according to the Rayleigh criterion, there is a trade-off between resolution and depth of focus. Overall wafer flatness was greatly improved on InP substrates to meet this challenge, however the fabrication process itself can also contribute to wafer flatness. It was found that during the butt-joint integration process, the quality of the wafer backside visually degrades. Fig. 3.6 shows an example of a haze that is observed at the edge of a DSP InP substrate after the full regrowth process. The zoomed SEM photographs of these structures reveal local wafer roughness resulting in a topography of approximately 400 nm.

Such defects were previously observed by Masmut et al. [64] and can be explained by the epitaxy that takes place to grow the contact layer. During the growth of the InGaAs contact layer, there is no phosphorus in the MOVPE reactor. This causes the substitution of phosphorus in the InP crystal by arsenic forming InAs. Since the lattice constant of this material is greater than that of the InP wafer crystal, it forms local topography as illustrated in Fig. 3.6.

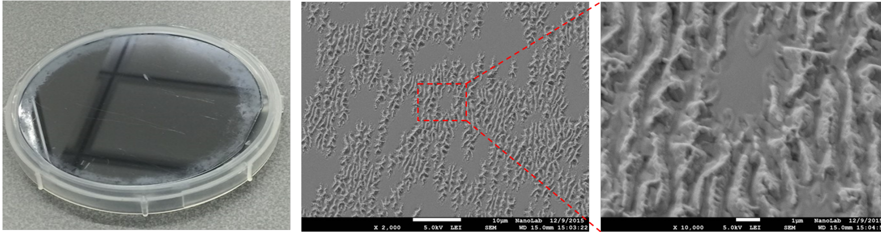


Figure 3.6: Photograph of haze on wafer backside after regrowth on the left and zoomed in SEM pictures of morphology in these areas at 2k and 10k times magnification.

When these defects are more closely inspected with energy dispersive spectroscopy (EDS) [65] on a SEM, specific elements can be traced as shown in Fig. 3.7. From this figure can be concluded that a local increase of As content (shown in blue) is observed while simultaneously the P content (shown in yellow) decreases. The In content slightly decreases as well due the increased lattice constant, while the green Ga concentration (shown in green) remains at background levels and with uniform distribution across the structure.

Level sensor data from the scanner has revealed that this does influence the total thickness variation of the wafer slightly. However, this effect does not cause much extra non-correctable focus with respect to leveling, as long as the defects are globally distributed over edges on the backside of the wafer. It is a point of concern that the InAs material can detach from the wafer due to mechanical friction in the machine. This can cause local particles on the exposure chuck, which cannot be compensated by the level sensor, and affects all subsequent exposures.

An experiment was performed to suppress the backside phosphorus substitution mechanism by changing the MOVPE growth process of the contact layer. In this experiment two solutions were tested and compared to the reference process. In the first solution, phosphorus was added to the contact layer growth process, resulting in a Q1.58 composition of the layer. In the second solution, the contact growth was

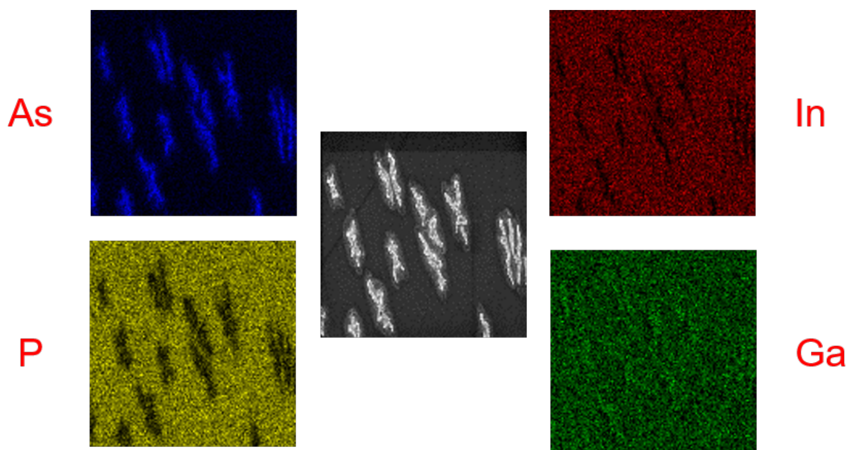


Figure 3.7: SEM photograph of backside morphology in the middle and EDS element scans of this structure in different colors for As, P, In and Ga respectively.

performed at lower temperature to reduce the substitution mechanism. It was found that both solutions improved the backside quality significantly at visual inspection. Since both solutions impact the composition of the contact layer, the contact resistance was determined with circular transmission line measurements (CTLM) [66]. Fig. 3.8 shows the means and 95% confidence intervals of the contact resistance for the tested solutions compared to the reference MOVPE process. This figure shows that with the incorporation of phosphorus in the contact layer, contact resistance is significantly higher than the reference process. With the low temperature growth however, contact resistance decreased slightly to approximately 2 $\mu\Omega cm^2$.

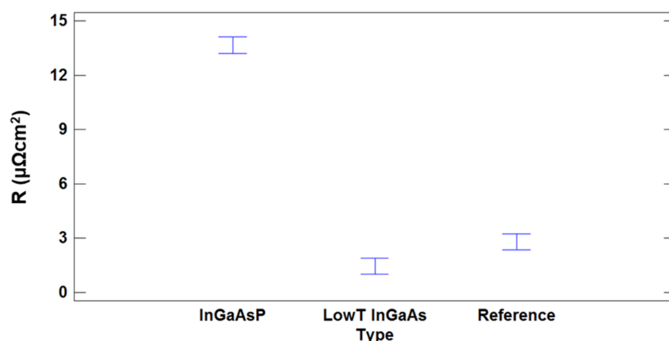


Figure 3.8: Contact resistances for layers grown with phosphorus addition, low temperature growth, and with the reference process.

3.2.4 Active patterning conclusions

In this section, a process module was developed to successfully perform active-passive butt-joint integration with ArF lithography. To establish a coordinate system, several marker strategies were tested. Scribe lane markers defined in an additional zero-layer show most promise for foundry scale production volumes, but are only compatible with PAS2500/40 stepper lithography when new markers are defined after the regrowth processing with the scanner.

The regrowth process affects the quality of the wafer backside, forming InAs topography on the surface that looks like a haze in the semiconductor material. This consumes part of the wafer flatness budget but more importantly can lead to particles on the exposure chuck of the scanner that would then require cleaning. It is possible to suppress this mechanism by the addition of phosphorus to the contact layer or lowering the MOVPE growth temperature. Both these solutions however, impact contact resistance and therefore the reliability of the PICs, and would need to be further investigated prior to implementation. It is proposed to investigate a backside protection scheme during the growth of the contact layer to prevent the substitution mechanism without impacting the composition of the contact layer.

3.3 Distributed Bragg reflector grating patterning

A photonic building block that requires high resolution and dimensional control but does not necessarily require high topography etching is a DBR grating. These gratings can be used to create periodic refractive index modulations in a waveguide. These index modulations individually cause very small reflections, but with proper design and fabrication of the grating, these reflections will be in phase and add up to a substantial reflection. With such gratings multi-wavelength and tunable lasers can be created [67, 68].

The TU/e generic platform operates at a wavelength of 1550 nm which requires the gratings to have a pitch of around 240 nm or even smaller when shorter wavelengths are desired. For integrated devices, typically EBL is the technology of choice to image such structures on InP substrates. The TU/e PAS5500/1100B scanner, is specified to have enough resolution to image such structures and could be suitable for larger PIC volumes. However, no process module was defined so far to perform the patterning of such ArF structures. In this section the transfer or such an ArF grating pattern from the resist into the InP semi-conductor material is investigated and results of fabricated DBR devices are presented. The ArF building block was applied in SMART Photonics foundry process [6] and compared to the same process with EBL.

3.3.1 Patterning process considerations and results

Since the structures of a DBR grating require extreme accuracy and come close to the resolution limit of the scanner, the full ArF coating process is required as described in Chapter 2. In the existing technology to fabricate DBR gratings with EBL, the silicon nitride hard mask that needs to be etched is relatively thin because only a small step

in the InP semiconductor material needs to be etched. The process to realize this with an ArF pattern is schematically represented in Fig. 3.9.

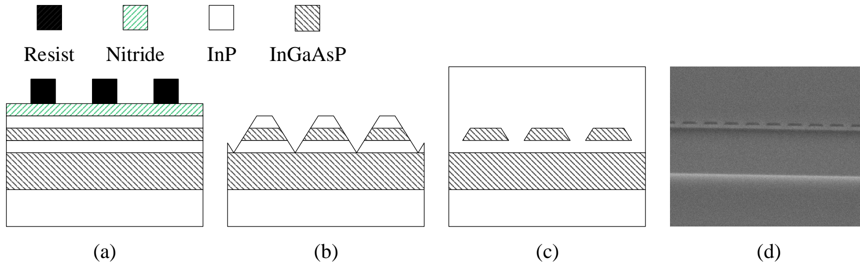


Figure 3.9: Integration scheme for DBR process module.

It is possible to use the ArF resist pattern as shown in 3.9a, directly to define a 50 nm nitride layer with the cyclic nitride etch process that is described in the waveguide patterning section 3.4 of this chapter. In this work, the resulting nitride pattern was used to transfer into the InP layer stack by a diluted bromine methanol (BrMeOH) wet etch. After hard mask removal with BHF, the structures look like Fig. 3.9b. The samples are then overgrown with the top cladding resulting in a buried grating pattern as shown in Fig. 3.9c,d. Table 3.2 shows an overview of the entire process module for ArF enabled DBR definition.

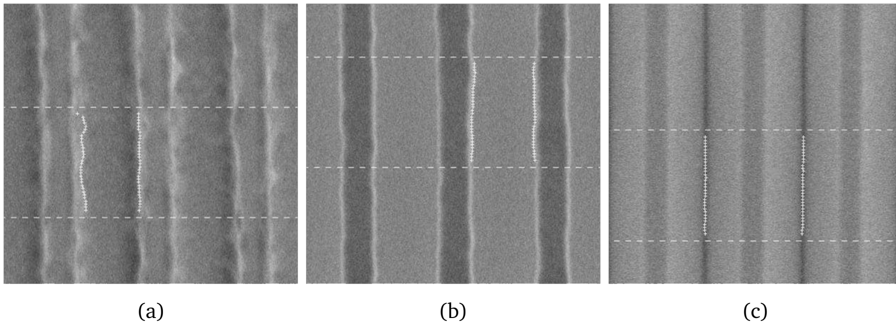
Step	Description
1	Hard mask deposition
2	BARC, PR and TARC coating
3	ArF exposure
4	PEB and development
5	Hardbake
6	Cyclic Nitride Etch
7	Cleaning
8	BrMeOH wet etch
9	BHF mask removal
10	Epitaxy top cladding

Table 3.2: ArF enabled DBR patterning process module steps.

DBR devices were fabricated with the discussed ArF enabled DBR process module. The structures with a pitch of 240 nm, were exposed with annular illumination conditions as described in Section 4.4, with a σ_{outer} of 0.85, a σ_{inner} of 0.55, at a numerical aperture of 0.75. CDSEM inspections were performed after step 5, 7 and 9 from Table 3.2 respectively as can been seen in Fig. 3.10. From these results can be concluded that the imaging quality of the gratings at the lithography stage in Fig. 3.10a is sub-optimal. The contrast seems to be limited causing poorly defined lines with considerable LER and some resist residues in the open regions. This imaging-related

problem however, will be addressed in the next chapter.

After etching as shown in Fig. 3.10b, the LER is slightly less pronounced and the resist residues have not led to nitride residues. Since the BrMeOH etch is crystal orientation dependent, it creates triangular shaped v-grooves along the [1 1 1] crystal plane as shown in Fig. 3.10c. This causes the pre-existing LER to fully disappear and results in sharply defined gratings at the designed pitch, with this wet patterning process. The pitch was measured on 63 locations of the wafer and found to be 240 nm with a 3σ CDU of 4 nm, which is mainly caused by the CDSEM measurement reproducibility that is specified at 3 nm.



(a) (b) (c)

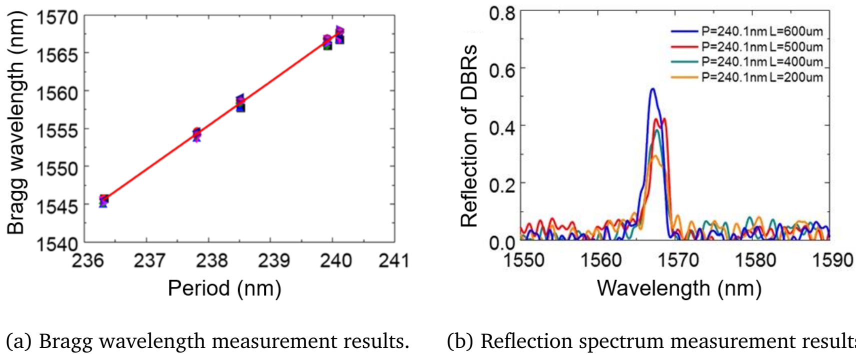
Figure 3.10: CDSEM inspection of DBR pattern in resist (a), nitride (b) and semiconductor (c).

3.3.2 Device manufacturing results

The devices from this experimental run were designed and characterized by Dan Zhao and presented at the IEEE Photonics Society Benelux symposium [69]. Fig. 3.11a shows the measured Bragg wavelength as a function of grating period for eight devices per period, coming from different locations of a single wafer. The red line represents a linear least squares fit of the measurement data. The Bragg wavelength increases linearly as the period increases and the standard deviation per period design is below 0.7 nm. This indicates a reproducible lithography process over a large wavelength span. Fig. 3.11b shows measured reflection spectra of 240 nm pitch devices, coming from different locations of the wafer with different grating length. The results show that the same period results in the same Bragg wavelength independent of wafer position indicating a reproducible lithography process. Secondly, the longer length of gratings results in higher peak reflectivity as expected.

The ArF enabled process module was implemented in the SMART Photonics foundry process and measurements of DBR laser devices were compared to similar devices fabricated with EBL. Fig. 3.12, shows the SMART Photonics measurement data with 3σ error bars of the measured Bragg wavelength as a function of grating period, for more than 200 devices fabricated with the TU/e scanner and EBL in blue and orange respectively. For the scanner results, 7 wafers from 4 batches were measured, while for the EBL a single wafer was included. In this data, it can be seen that both process modules show similar performance in terms of response to grating period design and intra-batch reproducibility. The outliers (4 devices) in the data

set, were concluded to be design or measurement related, rather than a variability of the lithography method. ArF lithography in this sense, holds the promise of being an alternative to EBL as a high-performance lithography solution for foundry scale production of DBR devices.



(a) Bragg wavelength measurement results. (b) Reflection spectrum measurement results.

Figure 3.11: ArF enabled DBR device characterization results [69].

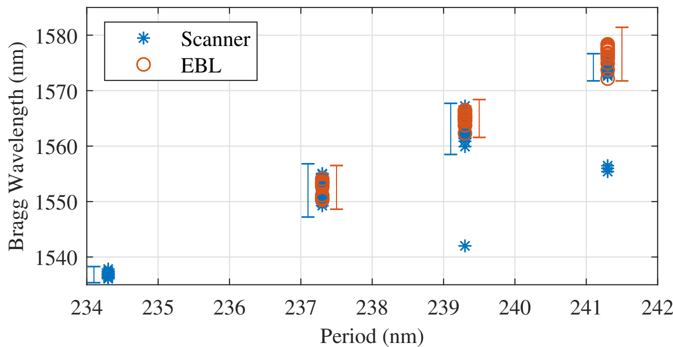


Figure 3.12: SMART Photonics measurement data with 3σ error bars of Bragg wavelength as a function of grating period for devices fabricated with EBL and ArF lithography.

3.3.3 Distributed Bragg reflector grating patterning conclusions

In this section, a novel DBR patterning module was successfully developed and implemented in the SMART Photonics foundry process. With this module, DBR grating devices were realized in InP-based materials with 193 nm DUV technology for the first time. The reflection properties of DBRs with different periods and lengths have been characterized. The Bragg wavelength of the DBRs can be precisely controlled, which is needed for laser applications. The ArF enabled process module was also compared with EBL and shows similar performance and response to intended design variations.

3.4 Waveguide patterning

The quality of the waveguide definition influences the performance of PICs in many ways. LER can impact the propagation losses of a waveguide whereas dimensional control impacts the effective index of a waveguide and therefore performance of wavelength selective and phase-sensitive devices. The application of ArF lithography to improve the definition of a waveguide is therefore interesting to investigate. Prior to this work, waveguides in TU/e process, were defined through broadband (g-, h-, and i-line) contact lithography with a resolution limit of approximately 800 nm. The resist used for this technology had a thickness of approximately 750 nm and was used to etch a thick nitride hard mask of 600 nm. As shown in Fig. 3.13, this hard mask was subsequently used in the traditional generic processing to etch the III-V device layer stack to form the waveguides.

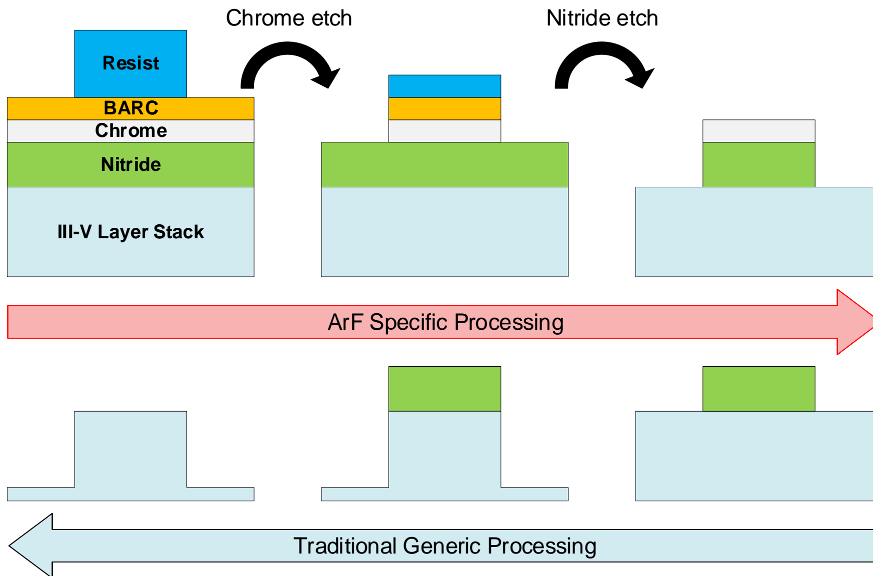


Figure 3.13: Integration concept of traditional generic processing in the TU/e process with novel ArF specific processing.

Since the ArF resist thickness is not enough to etch a nitride hard mask of 600 nm, a different approach is required to transfer an ArF pattern into the III-V layer stack. In the first part of this section the process steps are discussed that were introduced to overcome this challenge. In the second part of this section a comparison is made between the traditional contact lithography and ArF enabled waveguide definition. This is followed by characterization of fabricated AWG devices with reduced inter-waveguide gap size as low as 100 nm, which is enabled by the resolution of the TU/e scanner.

3.4.1 Patterning process considerations and results

Three ArF specific process stages were introduced as illustrated in Fig. 3.13 along the red arrow. A chrome etch was optimized, using the ArF resist stack as a mask. A novel cyclic nitride etch process was developed to transfer the 50 nm chrome waveguide pattern into the thick 600 nm silicon nitride layer with very high selectivity. From this stage, the chrome mask is removed, and the nitride pattern is cleaned. Then, traditional processing can be resumed resulting in a minimum number of changes to the standard TU/e generic process. In practice, each of the etch steps that form the waveguide will contribute to the critical dimension loss (CDL) of the entire process. Since each step will have its own wafer level signature, the final waveguide CDU is the sum of all these signatures. It is therefore important to optimize each individual step in terms of CDL and CDU.

The chrome etch is performed on an Oxford Plasmalab 100 inductively coupled plasma (ICP) 180 etcher. To etch the chrome layer, a Cl_2/O_2-based chemistry is used, which is often applied in semiconductor mask fabrication as well [70]. As a main reaction product, this chemical etch process forms volatile CrO_2Cl_2 [71]. The oxygen content in this plasma however, attacks the carbon-based resist mask as well, which results in a poor selectivity of this process. This recipe was originally implemented at the TU/e for chrome etching with EBL resist by B. Docter [72].

Due to the poor selectivity to organic materials, this etch can be used to etch through the BARC as well as the chrome layer in a single step. Fig. 3.14 shows a cross section of a chrome layer after etching with the residual mask still on top. From the slope of the chrome in this picture can be concluded that the process is isotropic in nature. This is undesirable in the sense that the slope, contributes to a substantial CDL on the subsequent process step, depending on the over-etch margin and selectivity to this chrome pattern.

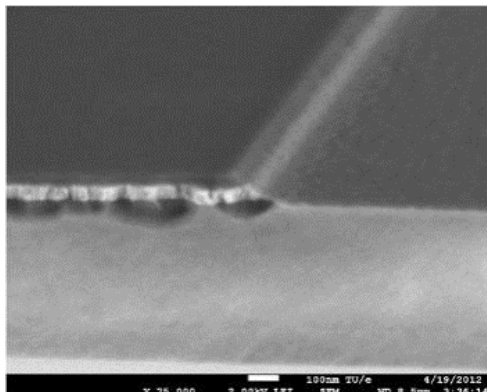


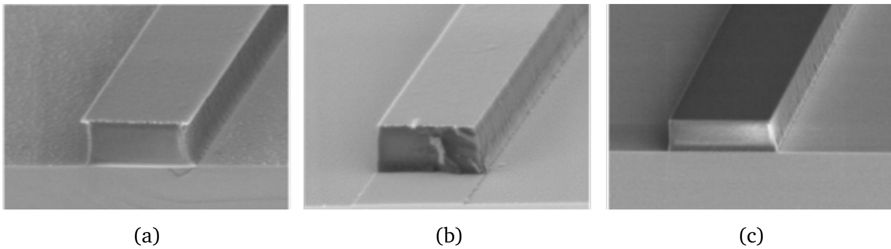
Figure 3.14: SEM cross-section of chrome etch.

The nitride etch, is performed on an Oxford Plasmalab 100 reactive ion etch (RIE) system. There were two recipes available that were developed for etching oxide and nitride layers, on smaller InP wafer diameters, with contact lithography or EBL resist masking. The "Standard" recipe employs a chemistry with a mixture of CHF_3 and

oxygen. The "Pure" recipe only uses CHF_3 to achieve higher selectivity and lower etch rates. It was found that neither of these pre-existing recipes was suitable for the ArF process module.

Fig. 3.15a shows a SEM cross-section of an ArF patterned wafer after the Standard etch process. With the chrome mask still visible in the cross-section, severe under etching is observed with this chemistry. It is assumed that the presence of oxygen in this recipe together with the absence of carbon contribution from the resist mask, reduces the sidewall passivation mechanism of the nitride etch [73]. This mechanism protects the sidewall of the pattern with a polymer that prevents chemical etching in the lateral direction. It was found that even with very low oxygen content at other recipe modifications, this mechanism remained suppressed.

The result of the Pure recipe is shown in Fig. 3.15b. In contrast to the Standard recipe, the sidewall passivation mechanism is overly present due to the absence of oxygen. With this chemistry, the polymer deposition causes roughness in the definition of the waveguide mask which can transfer into the semiconductor on the next steps. It was also found that the uniformity of this etch recipe on 3-inch wafer scale was not suitable for achieving a waveguide pattern with good CDU.



(a) (b) (c)

Figure 3.15: SEM cross-sections of ArF module nitride hard mask after etching with Standard recipe (a), Pure recipe (b) and Cyclic recipe (c).

The solution could not be found in a single step recipe, with a chemistry somewhere between the Standard and Pure recipe. Instead, it was found that using a cyclic recipe with settings that are listed below, was successful. The concept of this recipe is quite similar to the TU/e CH_4/H_2-based InP etch process, which is discussed in the next paragraph. In the etch part of the cycle, the nitride layer is partially etched building up polymers on the sidewall and rest of the wafer surface. During the descum part of the cycle, the oxygen plasma removes the deposited polymers. With a balanced duration of these steps, up to 600 nm of nitride was successfully etched with 50 nm of chrome mask. The cross-section in Fig. 3.15c, reveals that no under-etch is present with this recipe while a smooth sidewall is still preserved. Lastly it was also found that the etch rate uniformity was significantly improved with this approach.

- Etch: 15 mT, 50 W RF, 100 sccm CHF3 (60 s)
- Descum: 25 mT, 50 W RF, 20 sccm O2 (10 s)

For the InP etch the standard recipe for waveguide definition on the Oxford Plasmalab 100 ICP 180 was used based on a recipe described by Karouta et al. [74]. This

recipe employs cycles of CH_4/H_2 that etch InP but build up polymer on the wafer surface. This is alternated with an oxygen-based plasma that removes the built-up polymer. Fig. 3.16 shows a cross-section of an etched waveguide after the entire ArF enabled process module. This cross-section reveals that a slope of approximately 87° is present on an etched waveguide, resulting in a relatively large positive CDL, which will be quantified in the next section. An overview of the entire process module to define these waveguides with an ArF resist pattern is listed in Table 3.3.

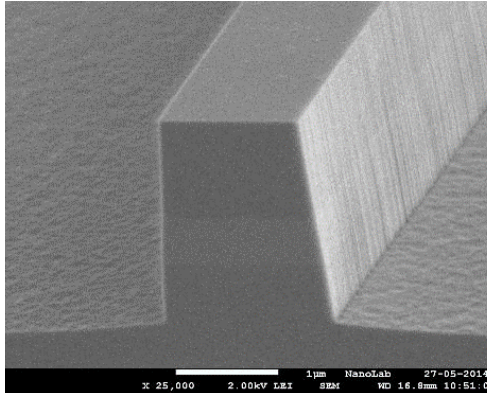


Figure 3.16: SEM cross-section of InP waveguide defined with ArF lithography.

Step	Description
1	Hard mask (Nitride + Chrome) deposition
2	BARC, PR and TARC coating
3	ArF exposure
4	PEB and development
5	Hardbake
6	BARC + Chrome etch
7	Nitride etch
8	Chrome removal and clean
9	InP Etching
10	Mask removal and clean

Table 3.3: ArF enabled waveguide patterning process module steps.

3.4.2 Waveguide critical dimension uniformity benchmark results

To quantify the advantages of the ArF enabled waveguide definition over traditional contact lithography-based process modules, a benchmark experiment was performed. In this experiment, three wafers with waveguide structures were processed with different patterning modules, and extensively measured with CDSEM. These measurements were performed after lithography, hard mask definition and waveguide etching

respectively. One wafer was processed with the ArF waveguide patterning module. A second wafer was processed with the traditional resist-based contact lithography patterning module. The last wafer was processed with a chrome-based contact lithography patterning module. Table 3.4 shows the CD, CDU and CDL results of the measurement stages for each wafer. The waveguide propagation losses of these wafers were determined by SMART Photonics on comparable deep-etched waveguides with a resulting CD of 1.5μm. These results are shown in Fig. 3.17.

Step	ArF (Chrome)	Contact (Chrome)	Contact (Resist)
Lithography:			
CD ± 3σ CDU	1529±8 nm	1346±133 nm	1330±97 nm
Step CDL	+29 nm	-154 nm	-170 nm
Hard mask:			
CD ± 3σ CDU	1417±10 nm	1220±133 nm	1142±63 nm
Step CDL	-112 nm	-126 nm	-188 nm
Waveguide:			
CD ± 3σ CDU	1711±16 nm	1442±158 nm	1400±129 nm
Step CDL	+294 nm	+222 nm	+258 nm
Total CDL	+211 nm	-58 nm	-100 nm

Table 3.4: Benchmark experiment: CD, CDU and CDL results for wafers fabricated with three different lithography processes.

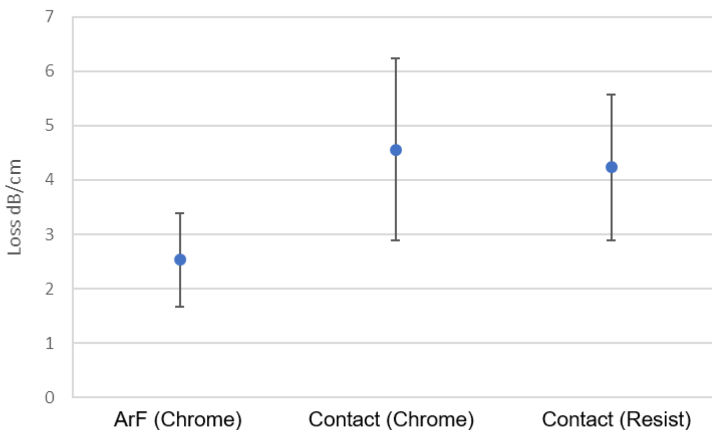


Figure 3.17: Benchmark experiment: propagation losses of 1.5 μm deep-etched waveguides for wafers fabricated with three different lithography processes.

Some very important results are visible in Table 3.4 and Fig. 3.17. Most importantly, the CDU of waveguides defined with the ArF lithography process module improves by almost an order of magnitude. This is an enormous step forward in terms of predictability and yield of photonic devices. The 200 nm CDL of the ArF process module, needs to be compensated at a design level. This will move the absolute CD of waveguides fabricated with the ArF process module towards the target dimension. In terms of waveguide propagation loss, there were only a limited number of waveguides with a comparable CD. The results of ArF fabricated waveguides are at least as good as or better than deeply-etched 1.5 μm waveguides fabricated with contact lithography. Due to these results, the process module as described in this section was adopted in the SMART Photonics foundry process immediately, as a follow-up to this work.

3.4.3 Arrayed waveguide grating results

AWGs, also known as phased arrays, enable critical (de)-multiplexer and spectrometer functionalities which are increasingly used in PIC designs in optical communication [75] and sensing applications [76, 77]. Given the increasing demand for higher data rates and energy efficiency [78], the performance of these PIC components needs to improve as well. In an AWG as shown in Fig. 3.18a, part of the signal is fundamentally lost due to the gap between the waveguides in the array. This loss occurs at the gaps where the waveguides, as shown in Fig. 3.18b, are attached to the free propagation region (FPR), depicted as “W” in Fig. 3.18c. Reducing the size of this gap can reduce the excess loss of the AWG component [79]. The minimum gap size is defined by the resolution limit of the lithography system and the patterning capability of the subsequent process flow.

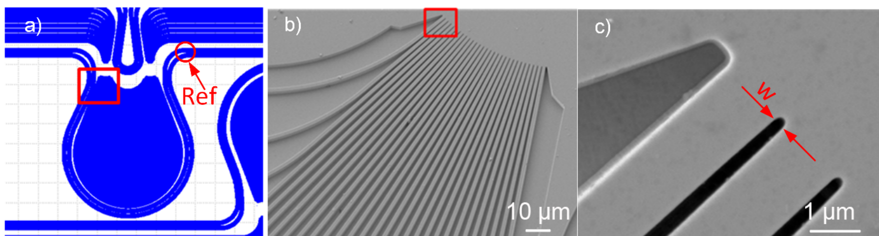


Figure 3.18: Waveguide mask layer for high-resolution arrayed waveguide grating and reference waveguides "Ref" (a), zoomed area SEM of the fabricated device (b), detail area SEM of the inter-waveguide spacing "w" at the free propagation region (c)

In this section, technical details of the application of ArF DUV lithography for the fabrication of AWGs are discussed which were previously published [61]. The simulated effect of the inter-waveguide gap scaling on excess losses of the AWGs is compared to experimental results from fabricated devices. These excess loss measurements are found by comparing transmission losses to co-fabricated reference waveguides depicted as "Ref" in Fig. 3.18a. Finally, the realization of a 3D-taper inside the gaps resulting from the lag effect is discussed.

3.4.3.1 Inter-waveguide gap scaling simulations

Simulations were performed by X. Leijtens, to quantify the anticipated effect of the inter-waveguide gap scaling. The model used for these simulations is published elsewhere [80]. A cyclic AWG with 8×8 channel design, a channel spacing of 200 GHz and free spectral range of 1600 GHz, was simulated. All waveguides were configured to have a width of 1500 nm. Fig. 3.19 shows the combined transverse electric (TE) polarized transmission spectrum of output ports 1 through 8, using port 4 as input for a deeply etched AWG with 100 nm gap size. As can be seen from this figure, the power transmitted per channel deviates in a symmetrical distribution around center channels, with a minimum excess loss of 2.6 dB for the channel at 1550 nm, and an increase of the losses to 3.9 dB at the outermost channels due to diffractive losses in the FPR [79].

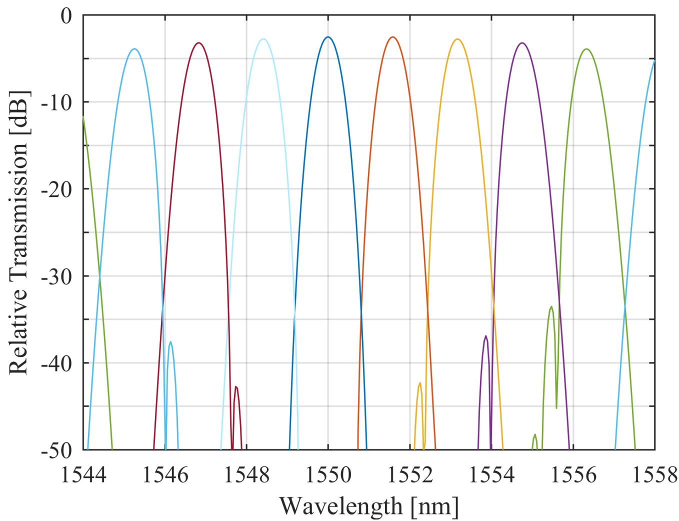


Figure 3.19: Simulated AWG transmission spectrum relative to input power from input channel 4 to all output channels with 100 nm gap size.

The loss in the star coupler dominates the loss in the AWG. In the above simulation, the array waveguides are assumed to be uncoupled. At small gap sizes however, this simulation overestimates the excess losses because the coupling between the waveguides in the array should be considered. A better representation can be obtained by calculating the overlap between the fundamental system mode of a large number of waveguides with a specific inter-waveguide gap, and the fundamental mode of a single wide waveguide matching the combined width. The result of this simulation is shown as the red line in Fig. 3.21, which depicts the simulated coupling loss of two star couplers in the AWG as a function of the inter-waveguide gap size. The excess loss decreases with smaller gap size. The excess loss improves by 1.8 dB by scaling the inter-waveguide gap size from 400 nm down to 100 nm, resulting in an excess loss of around 1.1 dB.

3.4.3.2 Arrayed waveguide grating device measurements

Passive PIC devices were fabricated using a representative generic layer stack with a top cladding of Zn-doped InP material, an intrinsic InP layer, and a waveguide core of InGaAsP material on top of a S-doped InP substrate [5]. These layers were patterned using the ArF enabled waveguide definition process module that was described in Section 3.4 with a modified nitride thickness of 400 nm. The originally 600 μm thick 3-inch wafers were then ground down to 200 μm thickness, before cleaving the devices and coating the chip facets with an anti-reflective coating to facilitate the transmission measurements.

The fabricated AWG devices were assessed using an Agilent 81940A tunable laser source via a polarization maintaining lensed fiber. The fiber was coupled into one of the central input waveguides, and the TE polarized transmission spectrum was measured at each of the eight output waveguides through a lensed fiber connecting to an Agilent 81636B power meter. The spectra coming from the AWG output waveguides were compared to those of reference waveguides with similar length and curvature, running along both the inside and outside of the AWG. The combined TE polarized transmission spectrum from an AWG with 100 nm gap size is shown in Fig. 3.20. The reference signal is plotted in the same figure in blue dots. At this gap size, the power of some channels is almost at the same level as the reference signal. The side-lobes at approximately -20 dB level can be explained by polarization rotation of the circuit [81]. The fraction of the resulting alternate orthogonal polarization propagates differently through the AWG bends, and recombines at a shifted wavelength at the output side. Since there was no polarization splitting at the output side, the combined spectrum is measured.

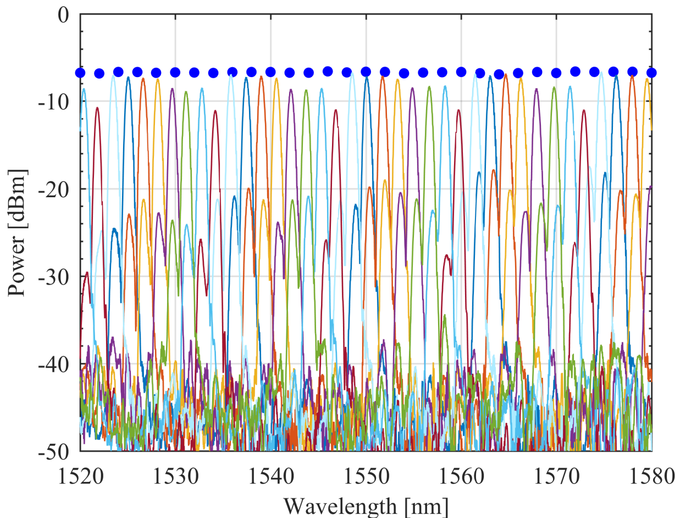


Figure 3.20: Measurement results for AWG transmission with 100 nm gap size between 1520 and 1580 nm wavelength, reference signal above in blue dots.

The losses were normalized to the maximum reference waveguide signal to represent worst case channel excess losses as opposed to average. The best channels over each free spectral range were then plotted as a function of designed inter-waveguide gap size in Fig. 3.21 This figure shows that in accordance with the simulations, the minimum excess losses decrease with smaller gap size. The 300 nm device performs 0.5 dB worse than expected from the trend of the other measured devices. These increased excess losses may be caused by additional losses on the input waveguide or the coupling of this specific device. The fabricated device with 100 nm inter-waveguide gap size exhibits an ultra-low minimum excess loss of 0.15 dB.

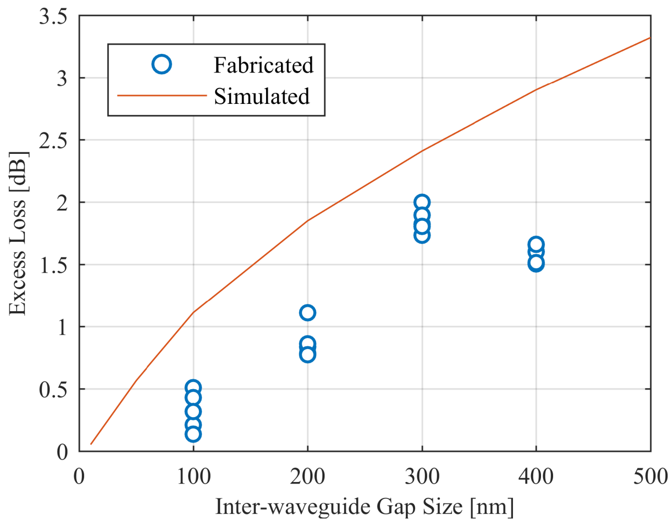


Figure 3.21: Simulated and fabricated best channel excess loss for AWGs with different inter-waveguide gap sizes, over the measured free spectral ranges.

3.4.3.3 Role of etch lag

One effect that the simulations have not considered, is that the width of the inter-waveguide gap has an influence on the effective etch depth. Due to the very high aspect ratios, defined as the depth divided by the width of a feature, etch lag occurs [82, 83]. This lag effect is the result of the difficulty to transport reactive species and ions into the trench and reaction products out of the trench. This slows down the physical-chemical process and results in an effective etch rate decrease in the trench when compared to open structures.

The lag effect was determined on multiple fabricated devices using a scanning electron microscope to measure the etch depth on cross-sections for various designed trench widths. Fig. 3.22 shows the lag effect inside a trench relative to the nominal etch rate on the open structure. As can be concluded from this figure, at 1250 nm trench width, the lag effect is only 12%. At a width of 250 nm however, the effective etch depth is at least 30% less than nominal.

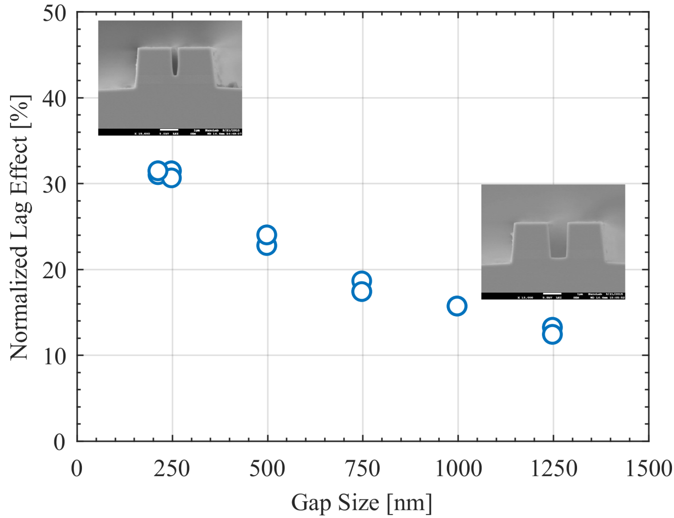


Figure 3.22: Lag effect for various inter-waveguide gap sizes.

From this trend, it can clearly be expected that when the gap size scales down even further, the lag effect will increase even more as well. On a 100 nm feature, it is therefore expected to have at least 35% lag effect, meaning that the start of the trench will have less than 65% of the etch depth while gradually transitioning to nominal as the waveguides in the array fan out. This creates a 3D taper with an effect similar to designed deep-shallow transitions in an AWG [84], that decrease the losses of the component. We assume that the simulated excess losses are worse than some of the fabricated devices because they do not include the effect of the 3D taper.

3.4.4 Waveguide patterning conclusions

In this section a process module was developed to transfer a high-resolution ArF resist pattern into the InP semiconductor to form high topography waveguides. This was realized by the application of a double hard masking strategy utilizing a novel cyclic nitride etch recipe. As a result, the waveguide CDU was demonstrated to improve by an order of magnitude when compared to traditional i-line-based waveguide patterning in the TU/e generic process. Waveguide propagation losses of devices fabricated with this module, were measured to be at least the same or better than the reference i-line process modules.

Excess loss of AWGs in InP generic PIC technology can be improved by reducing the inter-waveguide gap size. ArF lithography was successfully applied to define AWGs with gap sizes down to 100 nm. AWGs with sub dB excess losses as low as 0.15 dB, have been fabricated on InP wafers using DUV lithography. These losses seem to be lower than 2D simulation results, due to the etch lag effect inside the gaps. Using high-resolution lithography for InP PIC fabrication is a highly promising scalable solution for the next generation devices.

3.5 ArF Patterning Conclusions

ArF lithography was applied for the first time on 3-inch InP substrates to replace lithography steps in the existing TU/e generic PIC manufacturing process. Three complete patterning modules were developed to transfer ArF patterns into the relevant layers while minimizing the amount of required changes to the pre-existing process flow.

ArF lithography was applied for active-passive butt-joint integration and challenges were identified with respect to marker strategy and wafer backside quality. The most promising solution is a protected scribe lane marker that is defined before the device layers and is not affected by defect formation during the regrowth process. For PAS2500/40 stepper processing, it will still be necessary to have ASML primary marks, which could be introduced after regrowth processing.

An ArF process module was investigated for DBR grating fabrication. Devices were fabricated with this process module for the first time and characterized. Wafer level pitch CDU was determined to be below 4 nm and reproducibility of devices looks very promising. The process module was implemented in SMART Photonics foundry process and compared to EBL lithography. The trends for ArF and EBL enabled devices look very similar showing that ArF lithography is a promising candidate for foundry scale volume production of DBR devices. The resist image quality on gratings could be further improved and will be investigated in the next chapter.

Another process module was developed to use ArF lithography for patterning of the PIC waveguides. This process required the introduction of a chrome etch step as well as a novel cyclic nitride etch process. The ArF enabled waveguide process module was benchmarked against the existing process modules using both chrome and resist masking. This experiment showed an improvement in CDU by almost an order of magnitude with at least similar or better waveguide propagation losses. Based on these results, this process module was directly implemented in the generic foundry process to improve predictability and yield of PICs.

Low-excess-loss AWGs are enabled by unique application of ArF DUV lithography in InP integrated photonics through reduced feature sizes and more specifically, well resolved inter-waveguide gap dimensions. Arrayed waveguide grating devices were fabricated, and the effect of inter-waveguide gap scaling on the excess losses was measured and compared to simulations. Excess losses down to 0.15 dB were demonstrated to be lower than predicted with 2D simulations. The tapering of the etch depth inside the gaps due to the lag effect of the etch process may explain the improvements.

Chapter 4

Imaging improvement for InP grating devices

4.1 Introduction

In chapter 3 the results of ArF enabled grating patterning for fabrication of DBR laser devices were presented. In the TU/e InP PIC platform, 240 nm pitch grating patterns are required to fabricate lasers with an operating wavelength of 1550 nm, suitable for C-band communication applications [85]. At this grating pitch, it was observed that the image quality of the ArF photoresist is sub-optimal. Some resist residues and severe line edge roughness (LER) were observed in the grating image, indicating a poor contrast. For lower pitch gratings of 200 nm, suitable for fabrication of O-band laser devices at 1310 nm, the imaging is even more difficult, and the quality becomes worse as is illustrated in Fig. 4.1. Since these dimensions come very close to the resolution limit of the DUV scanner, it is interesting to investigate resolution enhancement techniques (RETs).

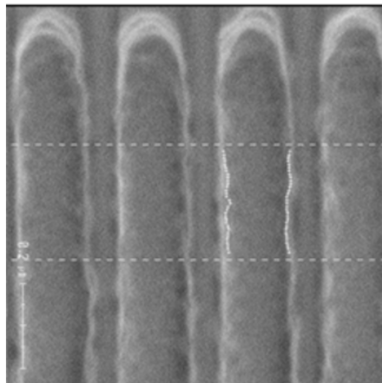


Figure 4.1: CDSEM photograph of 200 nm pitch grating image in ArF photoresist.

In this chapter, possibilities to extend the imaging capability limits of the ASML scanner, for gratings that can be used for InP PIC applications, are investigated for the first time. In the following section, a method is developed to quantify LER as a figure of merit for image quality, through post-processing of images from the CDSEM. In the next sections, two techniques are investigated to improve grating pattern quality. First, the research that was performed to introduce double patterning to improve image quality is presented. Then, the application of off-axis illumination with a dipole diffractive optical element is investigated. Finally, the conclusions for the application of RETs for the fabrication of InP gratings devices are drawn.

4.2 Image quality quantification

An accepted way to quantify the quality of a resist image for straight lines, is by measuring LER [86–89]. This is achieved, by determining the exact position of the edge of the pattern, along the direction of the line. The distance to the averaged position can then be determined, and the distribution of these measurements is figure of merit for the LER. This is illustrated by Fig. 4.2 where the LER can be defined as the 3σ distribution in the histogram of the measurements of Δx.

The accuracy at which the LER can be determined, is influenced by the image resolution of the line edge, the sampling distance and the number of samples. The Hitachi S9220 CDSEM can perform automated measurements of the LER, but due to the software, is limited to a maximum of 32 sample points per measurement. These points are always equally distributed along the length of the measurement box and the CDSEM image has a maximum resolution of 512x512 pixels. This means that the sensitivity of the LER measurement is bound to the magnification that is chosen. There's is a trade-off between the magnification that is used to measure the Δx accurately, and the length of the line that can be analyzed in a single measurement.

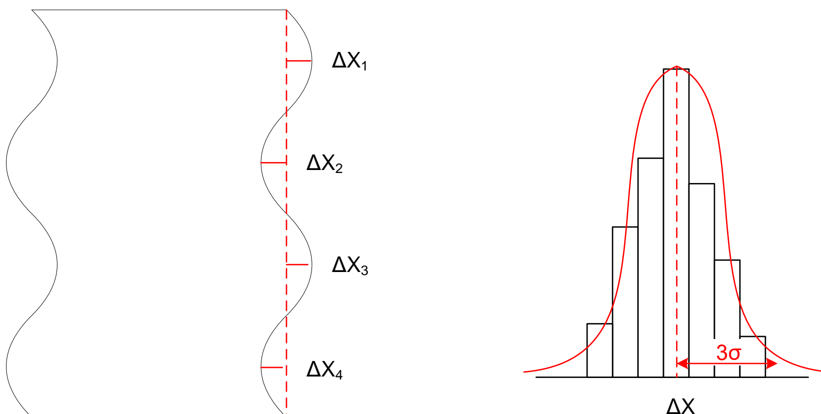


Figure 4.2: Measurement principle of LER as 3σ distribution of the measurements of Δx.

To circumvent some of the equipment limitations, a method was developed to perform post-processing on automatically collected CDSEM images. With this method, it is possible to perform edge detection on every horizontal pixel line of the image. Fig. 4.3 shows an example of edge detection on the normalized pixel intensity line of an image. Since left and right edges of a line are considered equal in terms of LER, the measurement points can be doubled by detecting both edges. Furthermore, if multiple resist lines are visible in the same field of view, the amount of measurement points are multiplied again. This method increases the total number of measurement points in this grating example by almost 2 orders of magnitude per CDSEM image, from 32 points to 512 pixels x2 edges x3 lines = 3072 points.

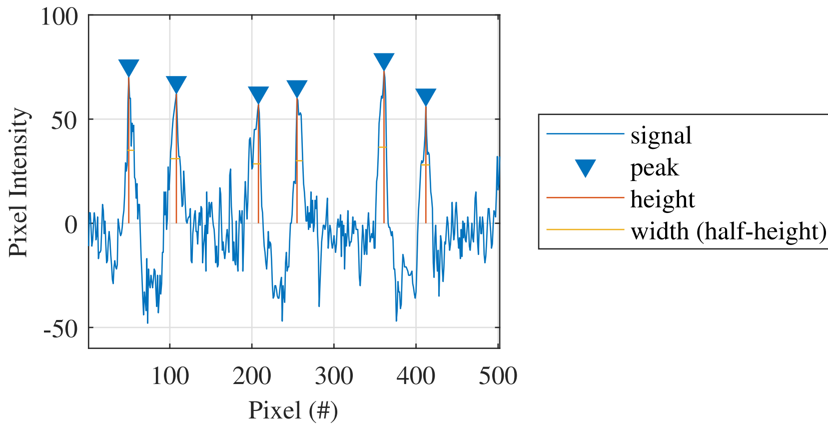
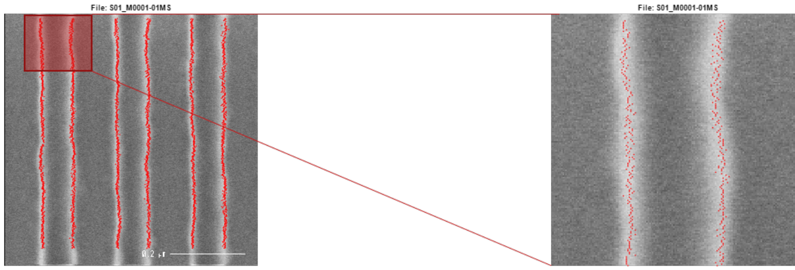


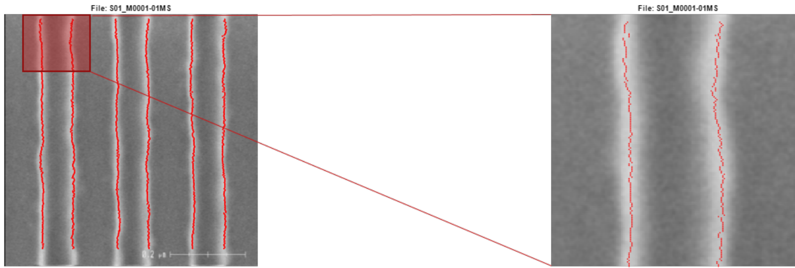
Figure 4.3: Example of edge detection on a normalized horizontal pixel intensity line.

Detection per individual pixel line on a CDSEM image is difficult because there is significant signal noise at a pixel level. Fig. 4.4a shows an example of the post-processing LER measurement, using edge detection on the raw image lines without further image processing. From the zoomed picture on the right, it can be seen that the LER is artificially increased by the pixel noise. The measured LER in this example was measured to be 8.8 nm. Gaussian filters are often applied to remove high frequency noise at the cost of contrast, while still enabling edge detection [90]. Fig. 4.4b shows the measurement of the same image, with a Gaussian filter with a σ setting of 1 pixel applied. From the zoomed image on the right, it can be seen that the measurement points follow the actual roughness profile of the line much closer. The resulting LER in this case was reduced to 6.8 nm which is a better representation of the actual shape of the resist line.

The CDSEM can acquire large numbers of images from different locations or wafers in an automatic way. This allows to perform the LER measurements, and gather statistics on the values which are in the 5-10 nm range and relatively close to the 3 nm measurement accuracy of the CDSEM. This results in a good method for quantification of image quality of gratings and is applied in the following sections for investigation of double patterning and off-axis dipole imaging respectively.



(a) Raw CDSEM image.



(b) Image with Gaussian filter applied.

Figure 4.4: Overview (left) and zoomed images (right) of post-processing LER measurements on 200 nm pitch gratings.

4.3 Double patterning

The first RET that was investigated to improve imaging quality for gratings is double patterning. This technique is currently widely applied in the semiconductor electronics industry to extend imaging capability of existing lithography infrastructure to reach lower CD technology nodes [91–94]. The principle of double patterning revolves around transferring semi-isolated structures at double pitch, to obtain the desired structure density at the intended pitch. The motivation for doing this, is that the imaging contrast of these semi-isolated features will be higher than for those at intended pitch. Contrast is defined as the relative intensity difference between exposed and unexposed areas, as a fraction of the total intensity of both areas.

$$\text{Contrast} = \frac{I_{max} - I_{min}}{I_{max} + I_{min}} \tag{4.1}$$

Fig. 4.5 shows an example of a theoretical contrast curve, where the relative intensity is zero underneath the mask and 1 on the transparent sections. In this specific example, contrast would be 100% but in practice this is never achieved on structures that are close to the resolution limit of a lithography system.

There are several process schemes that have been developed for double patterning. The litho-etch, litho-etch (LELE), litho-freeze, litho-etch (LFLE), and self-aligned

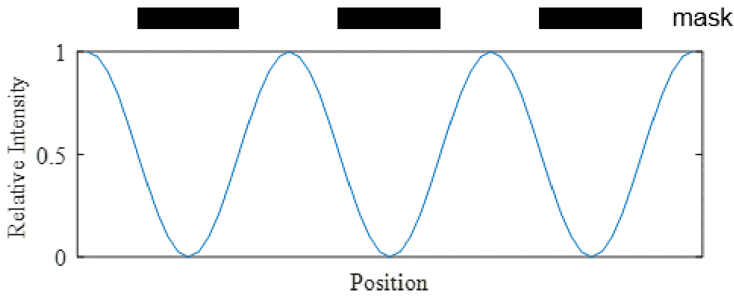


Figure 4.5: Example of intensity curve for mask exposure.

double patterning (SADP) methods have been described by Zimmerman [95]. In this work, the implementation of the LELE process for InP grating fabrication was studied. In the scheme that is schematically shown in Fig. 4.6, the pitch reduction is achieved by combining two lithography layers by etching the first pattern into a hard mask layer, so that it does not affect the exposure and etch of the second layer. This method did not require new process step development, since it is a repetition of the steps that were developed for grating patterning as described in Section 3.3. This process was therefore preferred to the other schemes, that would require specific chemicals and development of new processing steps.

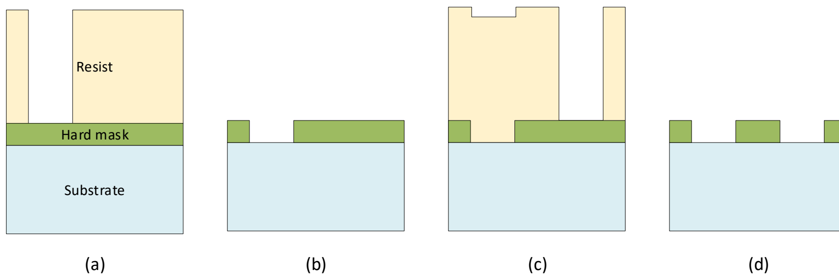


Figure 4.6: Schematic LELE double patterning process scheme: (a) Litho 1, (b) Etch 1, (c) Litho 2, (d) Etch 2.

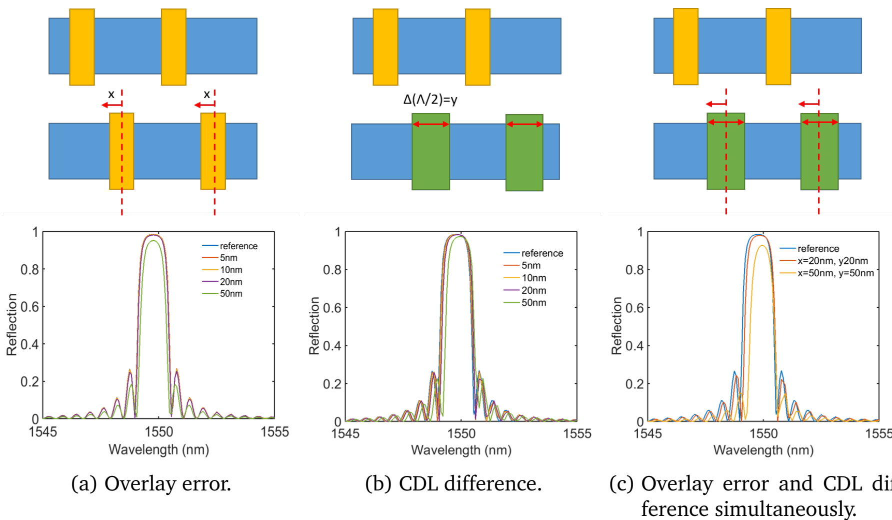
4.3.1 Device simulation results

From a DBR application point of view, there are two aspects that raise concern with the LELE double patterning scheme. Since the grating pattern will be built up from two separate exposures, there could be an offset between the two layers, causing a double-pitch distribution. Secondly, the CDL of these layers could be different which would cause a simultaneous double pitch and duty cycle distribution. The worst-case layer offset can be estimated from the single machine overlay error which is specified to be less than 15 nm for the TU/e scanner. The CDL difference can also be estimated

by taking the specified CD uniformity of this tool at 100 nm CD, specified to be less than 10 nm.

To estimate the impact of such fabrication errors on the DBR grating performance, simulations were performed by D. Zhao. The method of these simulations is described in Chapter 2 of her thesis [96]. For these simulations a 600 μm long grating with 238 nm pitch, fabricated in the SMART Photonics foundry platform was used as object of study. Apart from the errors under test, the rest of the fabrication was assumed to be perfect in terms of etch depth, waveguide dimensions, layer thickness and composition.

Fig. 4.7a shows the reflection spectrum of a reference grating with single step patterning, compared to double patterned gratings with an overlay error between 5 and 50 nm applied. Fig. 4.7b shows the effect when the same reference grating, is compared to a double patterned grating where there is a difference in CDL of 5 to 50 nm between the layers. Finally, Fig. 4.7c shows the reference grating compared to a double patterned grating, with a simultaneous overlay error and CDL difference of 20 and 50 nm for both respectively.



(a) Overlay error. (b) CDL difference. (c) Overlay error and CDL difference simultaneously.

Figure 4.7: Simulated effect of separate and simultaneous fabrication errors on DBR reflection spectrum increasing from 0 to beyond scanner capability.

From these figures, it can be seen that the DBR reflection spectra with these double patterning fabrication errors, only change significantly when the errors increase beyond 20 nm. It seems therefore feasible to fabricate DBR grating devices with the scanner, with double patterning, even though a double distribution in the pitch and duty cycle can occur as a result.

4.3.2 Lithography simulation of image contrast

The lithography process can be accurately predicted by simulations. In this work the GenISys LAB software was used [97]. This simulation tool performs a Fourier trans-

formation of the design intent which yields the diffraction spectrum. This result is then multiplied with the pupil function of the system which depends on the properties and settings of the exposure system, after which the resulting aerial image can be reconstructed by inverse Fourier transformation. From the aerial image, the dose and the optical properties of the layer stack, an image intensity profile in the resist layer is obtained. From this result, another simulation can be performed to estimate the resist response to the image intensity profile during the development process. This simulation was based on the 4 parameter Mack model [98, 99], that is calibrated through CDSEM analysis of a FEM exposure which is explained in Appendix C.

The simulated image intensity profile of a single step patterning grating with 100 nm lines and spaces (dense pattern), was compared to a double patterning grating with 300 nm lines and 100 nm spaces (semi-isolated) respectively. The starting point of the exposure settings that were used for these simulations, are listed in Table 4.1. The σ settings, represent the inner and outer diameter of the annular illumination source shape that is described in Section 4.4. Since the same resist process was used for both double patterning exposures, a dose offset was required to compensate for the overall lower obtained intensity with the semi-isolated feature. The focus offset is specified relative to the top of the resist in the approximate center.

For the layer stack, an InP substrate was included in the simulation, with a 50 nm plasma enhanced chemical vapor deposition (PECVD) SiN hard mask, and the full DUV resist coating stack as described in Chapter 2. The simulations were performed with a discretization of 5 nm in X and Y direction (design plane) and 10 nm in Z direction (layer stack) respectively.

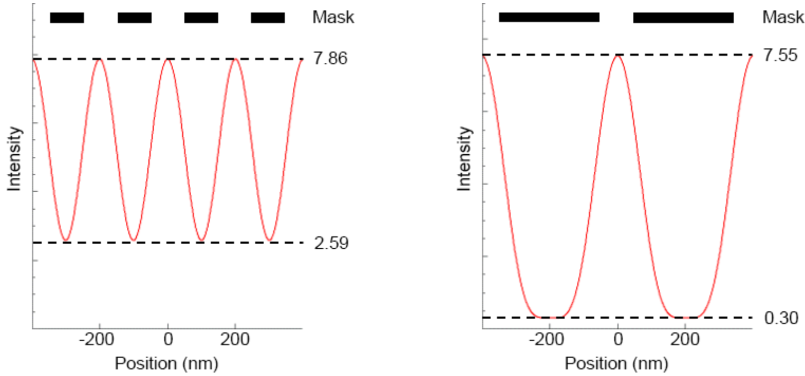
Parameter	Setting
Wavelength	193 nm
Illumination Type	Annular
Numerical Aperture	0.75
σ_{inner}	0.55
σ_{outer}	0.85
Dose	26 / 34 mJ/cm^2
Focus Offset	-0.1 μm

Table 4.1: Single step and double patterning comparison simulation settings.

Fig. 4.8 shows a representation of the dense and semi-isolated intensity curves with their minimum and maximum values. From these numbers the contrast for direct and double patterning can be determined at 50% and 92% respectively. These numbers support the expectation that the contrast can be significantly improved for the two independent exposures in a double patterning scenario.

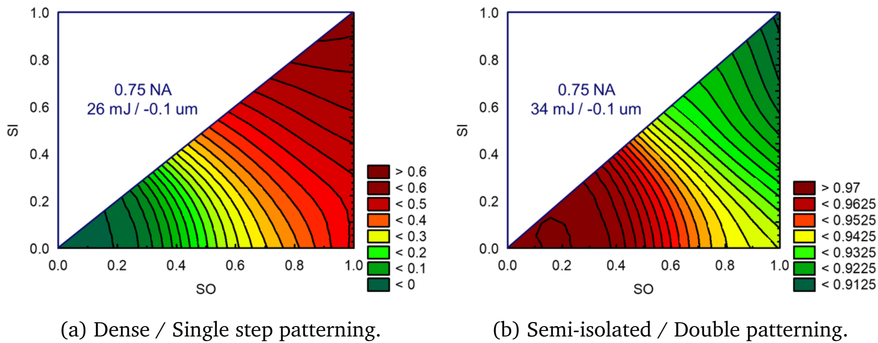
Since it was unknown how the applied σ_{inner} (SI) and σ_{outer} (SO) settings impacted the contrast for these features, a parameter sweep was performed at simulation level. Fig. 4.9 shows a contour plot of the simulated contrast as a function of the σ settings. The data on these figures, lies below the 45° line, since σ_{inner} cannot exceed σ_{outer}. The difference in contrast for dense and semi-isolated features can be recognized from the ranges of these plots, between 0-60% and 91-97% for Fig. 4.9a

and Fig. 4.9b respectively. It can also be seen that dense features are more sensitive to the σ settings and require higher σ values, whereas semi-isolated features require lower σ settings but gain little in terms of contrast.



(a) Dense: 100 nm lines and 100 nm spaces. (b) Semi-isolated: 300 nm lines and 100 nm spaces.

Figure 4.8: Image intensity curves for dense and semi-isolated grating features.



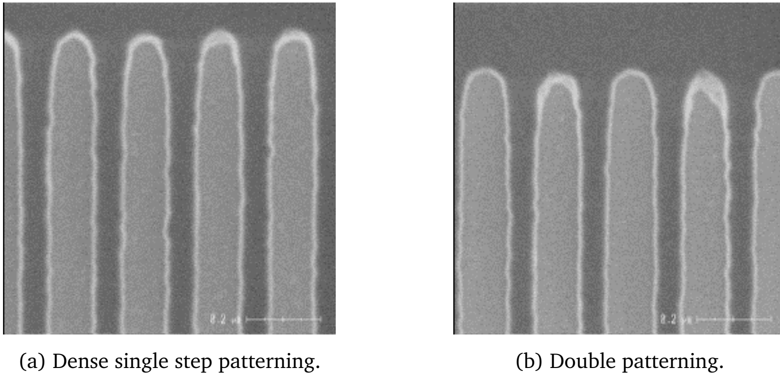
(a) Dense / Single step patterning. (b) Semi-isolated / Double patterning.

Figure 4.9: Simulated aerial image contrast as a function of σ_{inner} and σ_{outer} settings for different feature types.

4.3.3 Double patterning line edge roughness results

To verify if double patterning can improve LER of fabricated gratings, an experiment was performed. In this experiment, a wafer was processed with single and double patterned grating features at 200 nm pitch. For single step patterning, the directly patterned dense grating was inspected. For double patterning the composed structure of the two semi-isolated gratings was inspected. Since the composed result of the double patterned grating can only be observed in the hard mask, all SEM inspections and LER measurements were performed after SiN etching and cleaning as described in Section 3.3.

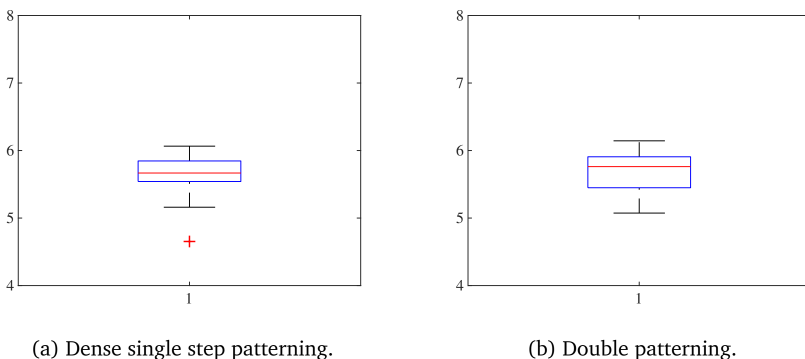
Fig. 4.10 shows a side by side SEM comparison of 200 nm pitch gratings fabricated with single and double patterning. In this figure, it can be seen that the DBR grating obtained with double patterning (4.10b), looks comparable to the reference single step patterning result (4.10a) in terms of imaging quality. Without performing accurate measurements, the resulting double pitch distribution can hardly be distinguished on the double patterned grating.



(a) Dense single step patterning. (b) Double patterning.

Figure 4.10: SEM comparison of fabricated 200 nm pitch gratings.

LER measurements were performed as described in Section 4.2, on 25 CDSEM images distributed over different locations on the wafer for both the single step and double patterning structures. The boxplots in Fig. 4.11, show the median of these LER measurements with the inter-quartile ranges (box) and non-outlier ranges (whiskers). The median LER values can be determined from these plots at 5.7 nm and 5.8 nm for the single step (4.11a) and double patterning (4.11b) techniques respectively. Based on the distributions of the measurements, the median LER is concluded to be the same for single and double patterning. The distribution of the measurements for double patterning however, is larger than for single step patterning.



(a) Dense single step patterning. (b) Double patterning.

Figure 4.11: Median LER, inter-quartile ranges (box) and non-outlier ranges (whiskers) of fabricated 200 nm pitch gratings.

Based on the obtained fabrication results, the lithography simulations from the previous section were revisited. Apart from looking at the raw contrast improvement, it is also required to take the slope of the intensity curve at the desired CD into account [100, 101]. This quantifies how fast the CD changes due to a small change of the intensity. This slope can be defined as normalized image log-slope (NILS) which is normalized to the intensity and CD.

$$\mathrm{NILS} = \mathrm{CD}\frac{d\ln(\mathrm{I})}{d\mathrm{x}} \quad (4.2)$$

From the simulated intensity curves of Fig. 4.8, the NILS for the single and double patterning solutions was determined to be 16 and 13 respectively at 100 nm trench width. This means that the NILS for these structures is decreasing by approximately 20%, contrary to the raw contrast which increases by almost 80% in a double patterning scenario. In principle this means that the slope of the intensity curve is less steep at dose to size, which causes local CD variation. This can explain why at an experimental level, no image quality improvement was observed in terms of LER.

4.3.4 Double patterning conclusions

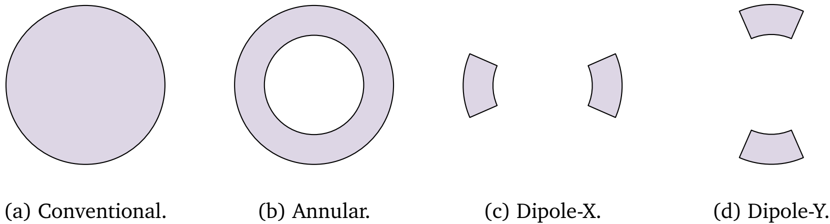
In this section, double patterning was investigated as a method to improve imaging quality of 200 nm pitch gratings. From the performed device simulations, it seems that double patterning can be used to fabricate DBR devices with the accuracy that is enabled by the scanner. From the fabrication results it can be concluded that the advantages of double patterning in terms of contrast do not translate to an improvement in terms of LER. Besides the raw contrast, it is important to take the NILS of the intensity curve into account at the desired dimension of the structure. For 200 nm pitch gratings, the NILS decreases by approximately 20% with double patterning, which explains the lack of measurable improvement in the fabrication results. Double patterning can however still be an interesting technique for pushing towards even smaller dimensions for Bragg gratings or different sub-wavelength features [48].

4.4 Off-axis dipole illumination

Since the diffraction behavior is different for every shape on a reticle, it is necessary to optimize the illumination conditions for each specific photonic component. There are several degrees of freedom to optimize the image quality aside from optimal energy and focus. The PAS5500/1100B has the capability to change the shape of the illumination source by adjusting specific lens elements in the lightpath. This enables conventional and annular illumination shapes that are illustrated in Fig. 4.12a and Fig. 4.12b. The conventional shape has an outer radius (σ_{outer}) that can be adjusted whereas for the annular shape also the inner radius (σ_{inner}) can be chosen.

Through the use of diffractive optical elements [102], more radical changes can be made to the illumination shape as is illustrated in the dipole-X and dipole-Y in Fig. 4.12c and Fig. 4.12d respectively. Like the annular setting, these shapes have an inner and outer radius specification, but also an angle to indicate which part of the

partial ring is illuminated. The dipole shapes are particularly useful when diffraction patterns of a mask layer are exclusively expected in a specific direction. A diffractive optical element is an exchangeable piece of hardware in the lightpath that reshapes the source pattern, and is optimized and applied for a specific device design. For high NA immersion systems, ASML has also developed a more versatile option called Flexray [103] where the shape is fully programmable through mirror optics and can be adjusted for each specific design.

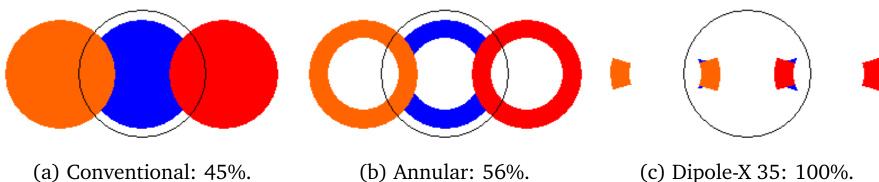


(a) Conventional. (b) Annular. (c) Dipole-X. (d) Dipole-Y.

Figure 4.12: Examples of typical illumination shapes.

The advantage of using alternative illumination shapes in projection lithography systems can be explained as follows. For reticle structures of which the dimensions approach the wavelength of the light source, diffraction takes place at the lightpath towards the projection lens. The numerical aperture of the lens determines how much of the diffraction orders can be captured to reconstruct the image. At the edge of the resolution capability of a lithography system, only part of the first order diffraction can still be captured, which contains the required spatial information of the reticle structures that are being illuminated. When the captured portion of the first order diffraction is increased, the image quality at the wafer level improves.

As an example, Fig. 4.13 shows the simulated diffraction patterns of conventional, annular and dipole illumination conditions for an exposure of a periodic 200 nm pitch line-space pattern. In this simulation with the ASML pupil filling tool, a 193 nm light source is used with a NA of 0.75 and σ settings at 0.85 and 0.55 respectively. The zero diffraction order is drawn in blue, whereas the -1 and +1 orders are drawn in orange and red. The lens aperture is drawn as the black circle to show which part of the first order is still captured. From these examples can be seen that the captured fraction of the 1st order becomes increasingly larger by using the more advanced illumination shapes, from 45% to 56% and 100% respectively. For the structure in this example, it is therefore expected that the image quality is best using a Dipole-X.



(a) Conventional: 45%. (b) Annular: 56%. (c) Dipole-X 35: 100%.

Figure 4.13: Simulated diffraction patterns for different illumination conditions

In this section, the application of dipole illumination as a RET for fabrication of DBR gratings is investigated. Specifically, a dipole-X 35 diffractive optical element was made available for study by ASML. In the first section, simulations are presented to estimate the advantage of dipole illumination in terms of contrast and NILS. These results are then supported with fabrication results of DBR gratings at 200 nm pitch. The process window of annular and dipole off-axis illumination conditions are compared, and the limits of dipole illumination for even lower pitch gratings are tested.

4.4.1 Lithography simulation of image contrast

Lithography simulations were performed with the GenISys LAB software [97] to compare annular and dipole illumination conditions for 200 nm pitch gratings. For both illumination conditions optimal dose and focus were chosen to achieve exactly 100 nm lines and spaces in resist. The simulation settings are listed in table 4.2. For the layer stack, an InP substrate was included in the simulation, with a 50 nm PECVD SiN hard mask, and the full DUV resist coating stack as described in Chapter 2. The simulations were performed with a discretization of 5 nm in X and Y direction and 10 nm in Z direction respectively.

Parameter	Setting
Wavelength	193 nm
Illumination Type	Annular / Dipole-X 35
Numerical Aperture	0.75
σ_{inner}	0.55
σ_{outer}	0.85
Dose	25 / 20 mJ/cm^2
Focus Offset	-0.1 μm

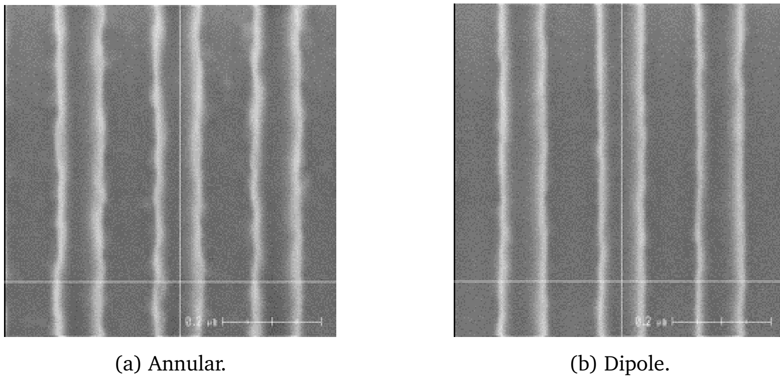
Table 4.2: Illumination condition comparison simulation settings.

With these conditions, it was found that the contrast for annular and dipole illumination was 52% and 84% respectively. This is a relative improvement of more than 60% in terms of contrast. From the simulated aerial images, it was found that annular and dipole illumination conditions had a NILS value of 19 and 32 respectively. This is also a relative increase of more than 60%. It is expected from these combined results that dipole illumination should result in better imaging quality for 200 nm pitch gratings. In the next section, the experimental work is described to verify the advantage of dipole illumination.

4.4.2 Dipole illumination line edge roughness results

A wafer was fabricated to verify and quantify the expected improvement of imaging quality for 200 nm pitch gratings by looking at the resulting LER. In this experiment an InP wafer with 50 nm PECVD nitride was coated with the full DUV resist coating stack as described in Chapter 2. On this wafer, many gratings were exposed with either annular or dipole illumination conditions. After development and hardbake, the

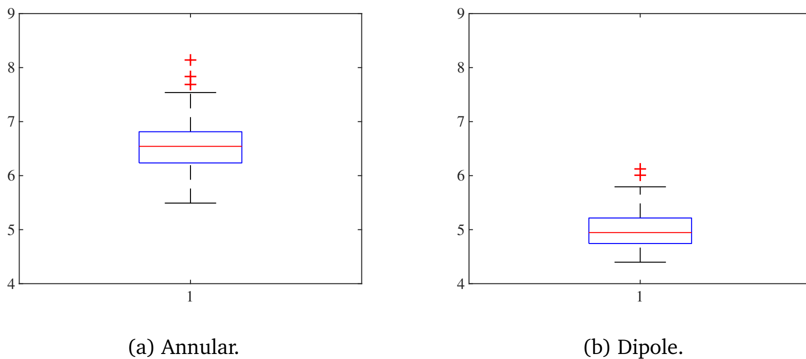
resulting resist images of these gratings were inspected with CDSEM. Fig. 4.14 shows the side by side comparison of gratings fabricated with both illumination conditions. In these SEM images, it can be seen that the annular exposure qualitatively shows slightly more LER and some resist residues in the open areas.



(a) Annular. (b) Dipole.

Figure 4.14: SEM comparison of fabricated 200 nm pitch gratings.

For each illumination condition, 81 images were taken with the CDSEM of exposed gratings, distributed over the entire wafer. The post-processing LER measurement as described in Section 4.2, was automatically performed on all of these images, on both edges of the 3 resist lines in the field of view at 200k times magnification. Fig. 4.15 shows the boxplots with the median of these measurements with the inter-quartile ranges (box) and non-outlier ranges (whiskers). The median LER values can be determined from these plots at 6.5 nm and 4.9 nm for these techniques respectively.



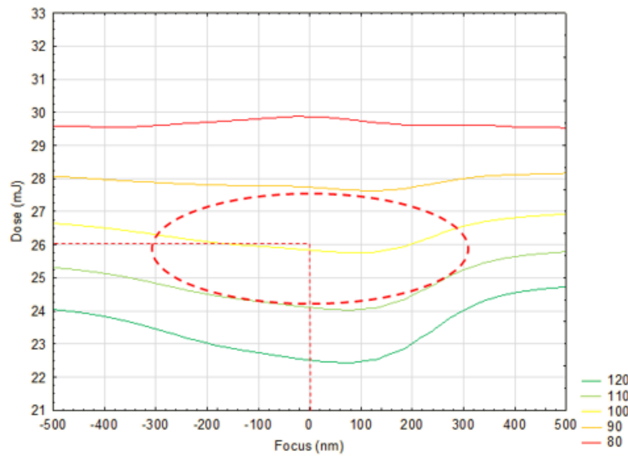
(a) Annular. (b) Dipole.

Figure 4.15: Median LER, inter-quartile ranges (box) and non-outlier ranges (whiskers) of fabricated 200 nm pitch gratings.

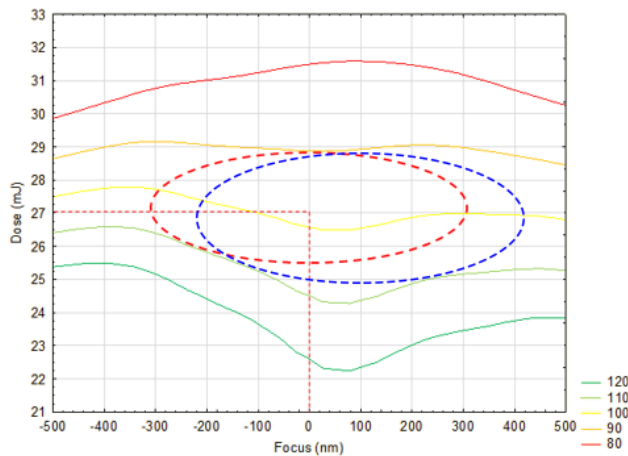
An unpaired t-test which analyzes the statistical difference between the data sets [104], was performed on these measurement results. The difference between the illumination conditions is statistically significant and the chance that both means of these results are part of the same distribution is practically zero (p-value of 6×10^{-49}).

From these plots can therefore be seen, that the LER of 200 nm pitch gratings exposed with a dipole-X 35 diffractive optical element, improves by 25%.

To verify the feasibility of this RET in a manufacturing situation, the process window was compared between annular and dipole illumination conditions. To achieve this, a wafer was exposed with images of both illumination conditions in a FEM layout. This technique is further explained in Appendix C. For this experiment the dimensions of CD of the resist line in the gratings was measured with a CDSEM as a function of dose and focus variations. Fig. 4.16 shows contour plots of both illumination conditions showing the target dimension of the resist line at 100 nm, as well deviations from this dimension at ± 10% and 20% respectively. The red dotted line in these figures, represents the process window at zero focus offset, as an elliptical area, where the dimension of the grating is within ± 10% of the target CD.



(a) Annular.

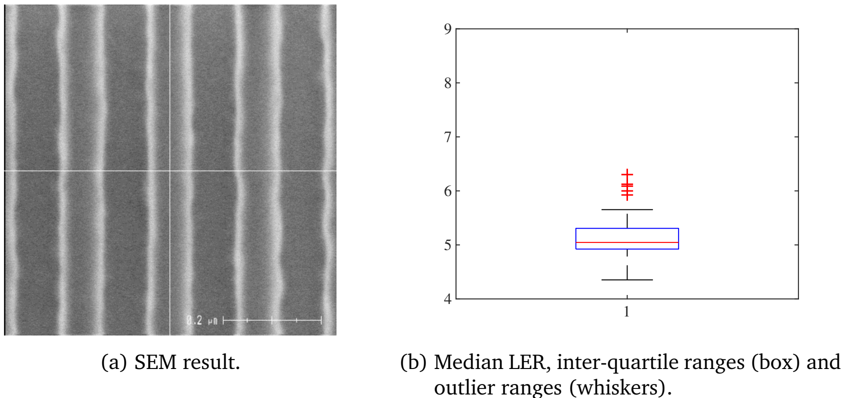


(b) Dipole.

Figure 4.16: Annular vs Dipole process window.

It can be seen from this data, that the process windows with both illumination conditions are very similar in size at zero focus offset. The dipole illumination condition requires a slightly higher dose of 27 mJ/cm^2. Additionally, with a focus offset of 100 nm, it is possible to slightly increase the process window size for the dipole condition, as illustrated by the blue-dotted line.

Simultaneously to the above described experiments, a wafer was exposed with smaller pitch gratings. Fig. 4.17 shows a SEM image of a 180 nm pitch grating as well as the resulting LER measurements of these structures, measured at 81 locations of the wafer. From Fig. 4.17b a median LER of 5.0 nm can be determined with similar distribution as the 200 nm pitch gratings. From this data, it can be seen that with the dipole illumination condition, gratings with 180 nm pitch can still be resolved with good imaging quality. At 160 nm pitch, it was found that image quality becomes significantly worse. Although the dipole-X illumination condition is unable to resolve equivalent features with perpendicular orientation, it was observed to start resolving features above 300 nm pitch.



(a) SEM result.

(b) Median LER, inter-quartile ranges (box) and outlier ranges (whiskers).

Figure 4.17: Grating imaging results with dipole illumination at 180 nm pitch.

4.4.3 Dipole illumination conclusions

In this section imaging quality improvement of gratings was investigated by the application of off-axis dipole illumination. Contrast and NILS improvements of more than 60% were simulated by the replacement of an annular illumination condition by dipole for 200 nm pitch gratings. A dipole-X 35 diffractive optical element was used to fabricate these gratings and a LER improvement of 25% was observed. No concession in terms of process window was measured for dipole relative to the reference annular illumination condition. Good imaging quality was observed on structures with down to 180 nm pitch. Dipole-X illumination conditions still allow larger structures with perpendicular orientation to be imaged in the same layer. Off-axis illumination was found to be advantageous for fabricating InP DBR gratings with a pitch below 240 nm.

4.5 Conclusions

In this chapter, two methods were investigated for the first time to improve ArF imaging quality of gratings for the fabrication of narrow pitch InP DBR laser devices. A post-processing algorithm was developed to quantify LER as a figure of merit for image quality of grating lines. Double patterning was simulated to be a viable technique to fabricate DBR grating devices with the manufacturing accuracy of the TU/e scanner. However, the investigated LELE double patterning scheme, does not improve the imaging quality of 200 nm pitch gratings because the NILS at dose to size does not improve. It could be interesting to investigate if this technique can extend the reach of the scanner, for pushing towards even smaller dimensions for Bragg gratings or different sub-wavelength features.

The application of off-axis dipole illumination was demonstrated to improve imaging quality of 200 nm pitch gratings in terms of LER by 25%. The process window in terms of sensitivity to focus and dose variations, was found to be similar to or greater than annular illumination conditions. The dipole RET also shows capability to image gratings with 180 nm pitch with good LER. The dipole-X 35 diffractive optical element is only suitable to resolve larger features above 300 nm pitch with perpendicular orientation. In a practical situation however, dipole-based building blocks can be designed in such a way to circumvent this disadvantage, or a Dipole-Y could be used for structures with perpendicular geometry.

For future work, it is interesting to fabricate laser devices with this imaging enhancement technique, in particular when dry patterning of the gratings or smaller pitch is required that would propagate the LER. It is proposed to investigate if alternative techniques can be used to improve imaging quality of DBR gratings. A technique that was not explored in this work to enhance the imaging quality for periodic structures, is phase-shift masking [105]. This technique relies on changing the phase of neighboring structures causing destructive interference in the diffraction patterns which could improve image quality. Discussions have been initiated with the mask supplier to investigate if this technique can be applied for future experiments.

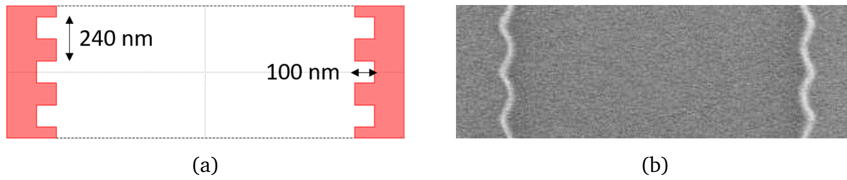
Chapter 5

Optical proximity correction for InP photonics

5.1 Introduction

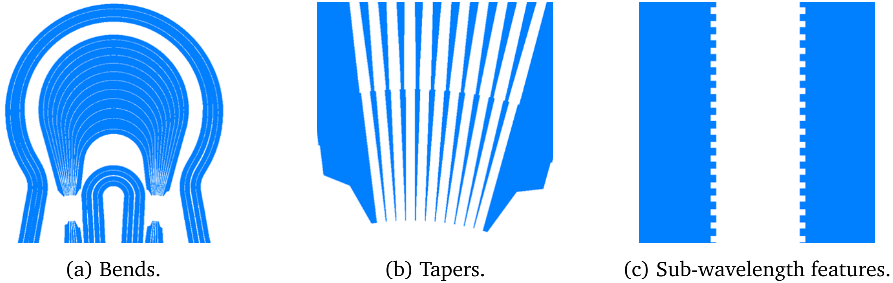
High-resolution lithography using 193 nm light sources has been applied for years in traditional electronics semiconductor manufacturing. For InP photonics however, the application of such manufacturing capability has only recently been demonstrated for foundry scale processing [6]. ArF lithography offers considerable advantages for PIC manufacturing. Process modules were developed in Chapter 3, that in some cases image structures with minimum feature sizes down to 100 nm on 3-inch InP. The need for the feature sizes enabled by this fabrication technology is not immediately evident from the dimensions of basic components such as a photonic waveguide. However, the dimensional control in PICs, has a large impact on the accuracy of wavelength selective devices [53], crosstalk and excess loss of AWGs, [61, 106] and propagation losses [87, 107]. PICs therefore require more advanced lithography equipment than equally dimensioned structures in electronics.

For some photonic structures, feature sizes are reaching the capability limits of the lithography equipment. This can cause a mismatch between the design intent and the shape of the resist pattern as is illustrated by Fig. 5.1. Replacing the existing equipment to solve this problem, requires substantial investments. This makes it desirable to investigate RETs [108] to extend the reach of existing manufacturing infrastructure, to decrease the mismatch and improve pattern fidelity. A common way in semiconductor manufacturing to achieve this, is to apply optical proximity correction (OPC). In contrast to electronics where most chips have a Manhattan type layout (orthogonal patterns), PICs have less conventional shapes like curves, tapers and sub-wavelength shape modulations as shown in Fig. 5.2. Due to this fact, the existing methods for electronics are not directly suitable for PICs and alternative methods need to be applied.



(a) (b)

Figure 5.1: Example of mismatch between design intent (a) and fabricated resist pattern (b).



(a) Bends. (b) Tapers. (c) Sub-wavelength features.

Figure 5.2: Examples of non-orthogonal and sub-wavelength geometries in PICs.

In this chapter, the need for and the benefits of OPC for InP photonics are investigated. A collaboration was established with GenISys [97], to simulate the lithography process for photonic structures and to apply and verify the effects of OPC. In the first section, the principle of OPC is explained. Then, an InP demonstrator design is introduced that illustrates the need for OPC and the lithography simulation results of this component are compared to an exposed resist pattern. A method to quantify pattern fidelity using a logical operation on the design intent and simulation pattern is explained. The next section discusses the chosen rule-based OPC types that were investigated in this work as well as the regression model that can be constructed with the simulation output of a DOE. The results of the pattern fidelity simulations are presented and the effects of the OPC parameters are characterized. A reticle with the best predicted OPC combinations was composed and patterning experiments are demonstrated to verify the simulation results at fabrication level. Finally, conclusions are drawn from the entire chapter.

5.2 Principle of optical proximity correction

The principle of OPC starts with simulating the pattern deformation in the design for manufacturing (DFM) phase. In this work the GenISys LAB software was used for this purpose, that is described in the previous chapter in Section 4.3.2. The simulation output can be used to predict the effect of sub-wavelength corrections to the patterns on the mask. Although these corrections are individually too small to resolve, they will affect the diffraction pattern resulting in a better intensity distribution to resemble the design intent. Existing OPC methods were specifically adapted for silicon

photonics to deal with the deviating shapes and orientations [109, 110]. For photonics it is not enough to look at quantifiers like width and length. It is required to look at the whole component geometry and quantify pattern fidelity as a figure of merit for the agreement with the design intent.

There are two main methods to perform OPC. The first method is rule-based OPC, where the design is scanned for violations of a predefined set of rules. Each violation is linked to a compensation method that is applied to all occurrences in the design. The compensation methods are typically derived from simulations of these type of geometries and previous fabrication experience. As an example, an OPC algorithm can check for structure corners in a binary design as shown in the Fig. 5.3a. In this example, the algorithm then proceeds to apply a positive or negative OPC-type called "Serif", depending on the type of corner, to prevent corner-rounding during fabrication. The resulting rule-based corrected design is shown in Fig. 5.3b.

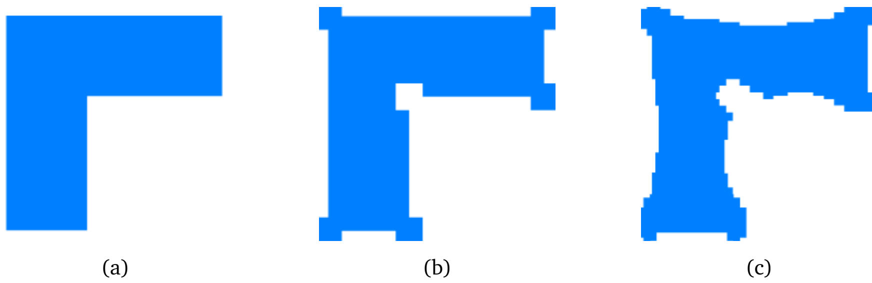


Figure 5.3: Example structure with the binary design intent (a), Rule-based Serif OPC design (b) and Model-based OPC design (c).

The second method is model-based OPC and revolves around calculating geometric differences between the design intent and the simulated pattern. At the locations that reveal differences above a threshold, geometry compensations are applied in an iterative procedure. This means that the compensated geometry is simulated and corrected repeatedly until the result meets the threshold. An example of such correction is shown in Fig. 5.3c. This method will lead to significant computation times but yields a much more accurate result. Modern-day OPC algorithms, are using rules to select the exact locations of the design that require model-based corrections, and can increase simulation resolution on the locations where it is most required.

5.3 Optimization methods

5.3.1 InP demonstrator design and simulation

An InP deep ridge waveguide with a nominal width of 1.5 μm, a sidewall grating with a period of 240 nm and width modulation of 100 nm per side, was used as a demonstrator design and is illustrated in Fig. 5.4(A). When this structure is imaged using the NanoLab@TU/e lithography process [61], the intended shape of the design is severely degraded due to diffraction of exposure light and a combination of the resist and developer properties as shown in the SEM image in Fig. 5.4(B).

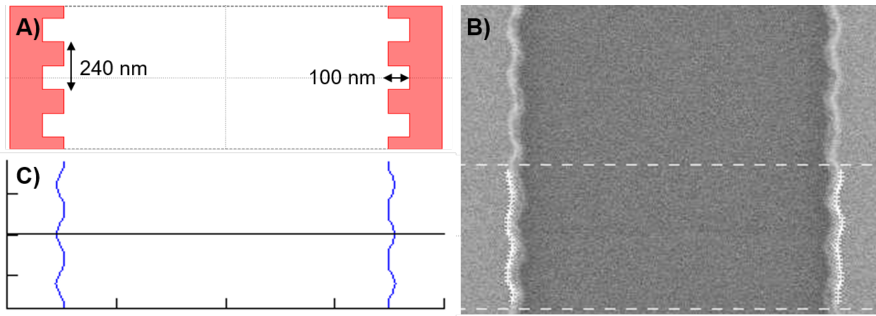


Figure 5.4: 1.5 μm waveguide design with sidewall grating at 240 nm pitch and width modulation of 100 nm per side: design intent (a), SEM image of fabricated resist pattern (b) and simulated resist pattern (c).

The exposure of the demonstrator design was simulated, using the exact illumination conditions of the exposure tool, the layer stack, and calibrated resist and developer models. The exposure settings that were used for these simulations are listed in Table 5.1. For the layer stack, an InP substrate was defined with a 400 nm PECVD SiN hard mask, and the full DUV resist coating stack as described in Chapter 2. The simulations were performed with a discretization of 5 nm in X and Y direction (design plane) and 10 nm in Z direction (layer stack) respectively. Fig. 5.4(C), shows the outline of the obtained resist profile using the design intent as input for the simulation. This result is very similar to the fabricated structure in Fig. 5.4(B) and is a validation that the loss of pattern fidelity can be accurately predicted with this lithography simulation method.

Parameter	Setting
Wavelength	193 nm
Illumination Type	Annular
Numerical Aperture	0.75
σ inner	0.55
σ outer	0.85
Dose	32 mJ/cm^2
Focus Offset	0 μm

Table 5.1: Sidewall grating projection Lithography Simulation Settings.

5.3.2 Pattern fidelity quantification

The purpose of performing OPC, is to improve the resist pattern to have better match with the design-intent by pre-correcting for systematic fabrication limitations and artefacts. This is realized by introducing small dimensional changes or sub-resolution features which individually are too small to be resolved but will impact the diffrac-

tion pattern of the full exposure. When the exposed pattern can be accurately predicted through simulation, it becomes possible to run an entire DOE as described in Appendix A, with OPC variations minimizing a quantifier that describes the pattern mismatch. Fig. 5.5 illustrates how the pattern mismatch can be quantified by performing a logical exclusive-or (XOR) operation on the intended design and simulated resist pattern from Fig. 5.4(A) and 5.4(C) respectively. The surface area of the resulting polygon can be calculated and extracted as a function of the applied OPC design parameters [110]. A smaller surface area of the XOR polygon in this case, represents a smaller mismatch and thus a better pattern fidelity.

Figure 5.5: Resulting mismatch polygon by performing XOR logical operation on design intent and simulated resist pattern.

5.3.3 Rule-based optical proximity correction workflow

In this work we have applied two types of OPC rules. Fig. 5.6(A) shows the application of a scatter bar to the original sidewall grating design of Fig. 5.4(A), which is parametrized by a size and distance. Fig. 5.6(B) shows the application of a hammerhead to the same design which is parameterized by a size, extent and overlap. The influence of these independent parameters was characterized with a DOE as described in Appendix A.

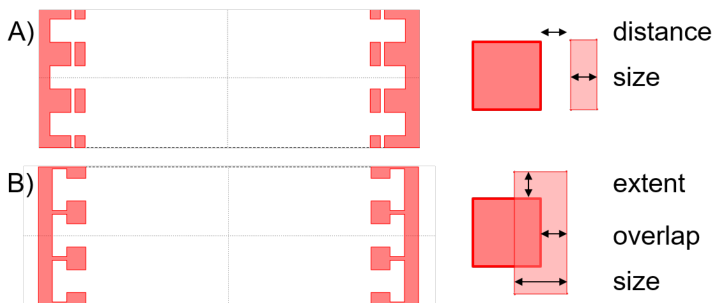


Figure 5.6: Scatter bar (a) and Hammerhead (b) OPC rule types applied to demonstrator sidewall grating design.

The workflow for the OPC DOE is illustrated by Fig. 5.7. The data that is generated at every operation in this workflow, is in a graphic database system (GDS) format. As input, the OPC rules were combined and applied to the sidewall grating device design, for each of the different rule combinations. The resulting corrected designs were individually run through the projection lithography simulation, followed

by the developer simulation. The resulting simulated resist pattern polygon was then compared with the original device design using a logical XOR operation. The resulting polygon surface was extracted, and the surface area was calculated as dependent result for each of the OPC parameter input combinations. The OPC parameters were each varied at 3 levels as listed in Table 5.2, using a 3^5 full factorial DOE with 243 runs, without randomization in the experimental order. This allowed screening for significant 1st and 2nd order effects of the input parameters as well as the first and second order parameter interactions.

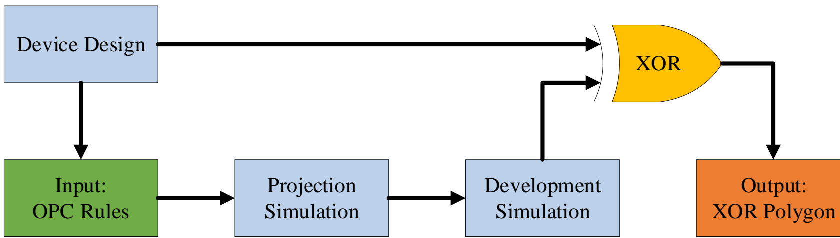


Figure 5.7: Design of experiments optimization scheme.

#	Scatter bar	Low	Medium	High
$P1$	Distance	10 nm	20 nm	30 nm
$P2$	Size	40 nm	50 nm	60 nm

#	Hammerhead	Low	Medium	High
$P3$	Extent	40 nm	50 nm	60 nm
$P4$	Overlap	60 nm	75 nm	90 nm
$P5$	Size	60 nm	75 nm	90 nm

Table 5.2: Design of experiments parameter variation settings for scatter bar and hammerhead OPC rules.

A regression model was constructed characterizing the XOR surface area as a function of each of the 5 OPC parameters and their linear and quadratic interactions. This 2nd order polynomial model was constructed as shown in (5.1) to (5.5). In this model, letters (a, b, c,..) represent the regression coefficients, whereas the independent parameters of the DOE are represented by ($P1$, $P2$, $P3$, ..).

Regression Model:

$$\text{XOR} = a + \text{Linear} + \text{Quadratic} + \text{Linear- and Quadratic-Interactions} \quad (5.1)$$

$$\text{Linear} = b * P1 + c * P2 + d * P3 \ ... \quad (5.2)$$

$$\text{Quadractic} = e * P1^2 + f * P2^2 + g * P3^2 \ ... \quad (5.3)$$

$$\text{Linear-Interactions} = h * P1 * P2 + i * P1 * P3 + j * P2 * P3 \ ... \quad (5.4)$$

$$\text{Quadratic-Interactions} = k * P1^2 * P2 + l * P1 * P2^2 + m * P1^2 * P2^2 \ ... \quad (5.5)$$

5.4 Optimization simulation and modeling results

Each of the regression parameters was tested for statistical significance and insignificant interaction effects were removed from the model. Fig. 5.8 shows an overview of the remaining standardized effects of all regression parameters that were included in the model. The red line in this graph represents the 5% significance threshold for a statistical zero-hypothesis test. The independent parameters are labeled as 1 to 5 as was illustrated in the first column of Table 5.2. Linear effects are labeled with "L" and quadratic effects are labeled with "Q". As an example, "3Lby5Q" refers to the interaction between the linear effect of the "hammerhead extent" and quadratic effect of the "hammerhead size" respectively. At the bottom of the graph, there are 3 effects that were concluded to be insignificant but were still included in the model because they were linear or quadratic main parameter effects. The detailed list the standardized effects, p-values and exact regression coefficients are shown in a table in Appendix D.

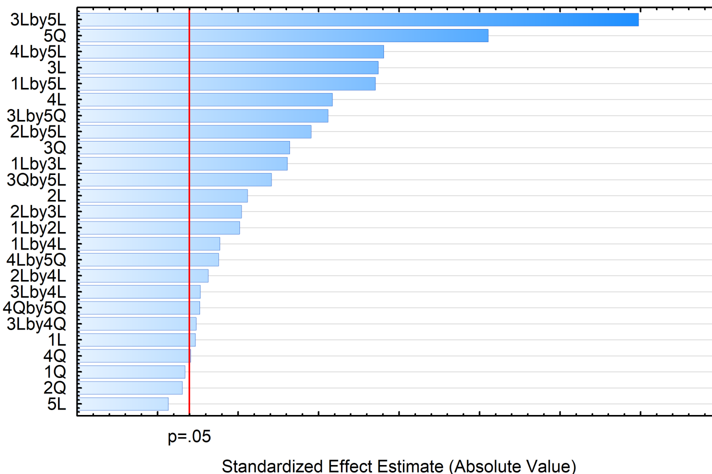


Figure 5.8: Summary of standardized effects included in the XOR regression model.

Fig. 5.9 shows the "predictions" of the constructed XOR surface area regression model as a function of the "observed" simulated XOR area for each parameter variation. This figure also shows the XOR surface area of the reference design without

OPC applied, signified by the red line at 0.064 μm^2. From these results it may be concluded that the constructed regression model for the XOR surface area can predict the pattern fidelity reasonably well, in particular for lower XOR values. Secondly, the application of OPC increases pattern fidelity for the majority of points that fall below the reference XOR threshold.

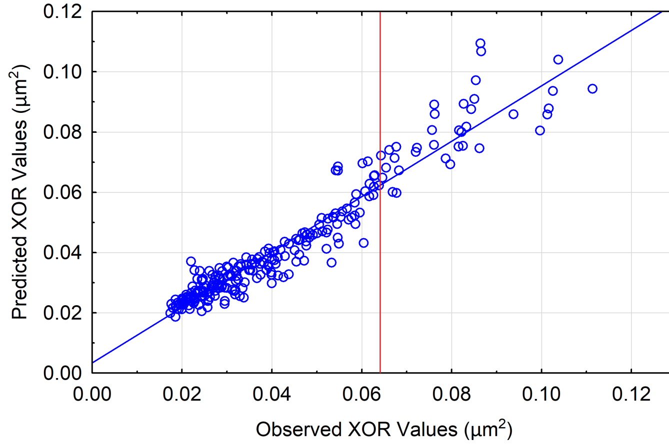


Figure 5.9: Correlation plot of predicted model XOR surface area versus observed simulated XOR surface area and reference XOR area without OPC marked with red line.

The response of the XOR area as a function of the independent parameters is shown in Fig. 5.10. This figure illustrates the trends of the model at the center of the simulated design space. From this figure can be concluded that all independent parameters have an influence on the resulting XOR area to some extent. It can also be seen that some of the parameters exhibit a clear none-linear behavior.

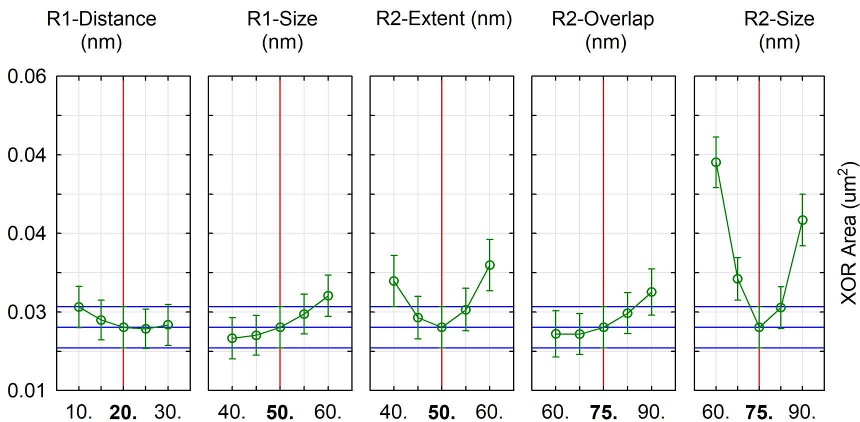


Figure 5.10: XOR area response to scatter bar (R1) and hammerhead (R2) parameters

The six OPC parameter combinations with the lowest XOR surface, were extracted from the total obtained data set and are listed in Table 5.3. This table also includes the simulated XOR surface area of a reference structure without OPC of 0.064 μm^2. In the most optimal parameter combination (OPC-5), up to 70% improvement in pattern fidelity is simulated, resulting in a lower XOR surface area of 0.017 μm^2.

	Scatter bar (nm)		Hammerhead (nm)			
Feature	distance	size	extent	overlap	size	XOR (μm^2)
OPC-1	20	40	50	75	75	0.018
OPC-2	20	50	50	75	75	0.020
OPC-3	10	40	40	75	90	0.019
OPC-4	20	40	60	60	60	0.018
OPC-5	10	40	50	60	75	0.017
OPC-6	30	50	60	60	60	0.019
Reference	-	-	-	-	-	0.064

Table 5.3: Best simulated OPC parameter combinations of scatter bar and hammerhead.

5.5 Patterning experimental results

A reticle was fabricated with test structures having the different OPC rule combinations from Table 5.3 applied. The devices were exposed on an InP substrate with a silicon nitride hard mask in a focus-energy matrix. Best exposure results for each of the OPC rule combinations were collected from a FEM using a Hitachi S9200 CD-SEM. The SEM images of the resist patterns of the three best OPC enabled sidewall gratings are shown in Fig. 5.11, in decreasing order of simulated pattern fidelity, at optimum dose and focus. In each corner of these images, the corresponding OPC enabled design is shown as well as the simulated resist profile in the center.

These resist profiles should be compared to the exposure result of such device without OPC as was shown in Fig. 5.4(B). All OPC designs show a significantly im-

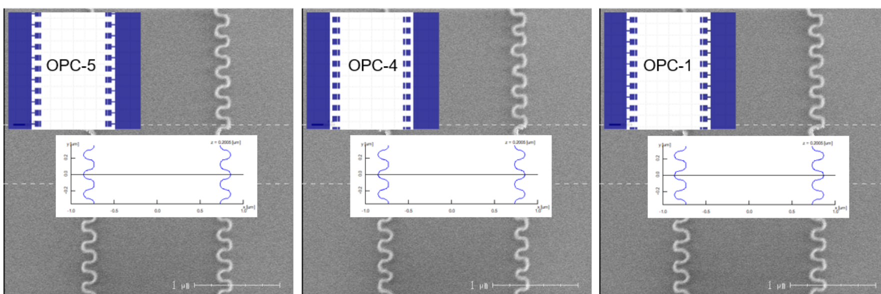


Figure 5.11: SEM images of sidewall gratings with best OPC rule designs in the top left corners and simulated resist pattern in the center.

proved pattern fidelity. The simulated results show excellent correlation with the fabricated resist patterns. This supports the claim that the effect of OPC corrections can be simulated, making the application and optimization of OPC parameters at the software level an ideal method for generating InP structures with optimal pattern fidelity on a high-throughput exposure tool.

The patterns from Fig. 5.11 were transferred into the silicon nitride hard mask after which the resist was removed. The hard mask structures were then transferred into the InP semiconductor subsequently followed by a removal of the hard mask with a buffered HF solution. Fig. 5.12 shows a comparison between an OPC enabled structure and a reference structure without OPC. Relative to the obtained resist patterns from Fig. 5.11, some additional loss of pattern fidelity is visible. This should be attributed to properties of both the nitride and InP etch like mask erosion, directionality, loading effects and aspect ratio dependence. These properties could still be improved by further tuning the etch chemistries. Despite the increased loss of pattern fidelity during the etch steps, the positive effect of OPC is still very visible. With OPC, there is still a clear waveguide modulation visible in the semiconductor, while without OPC, the modulation has almost fully disappeared.

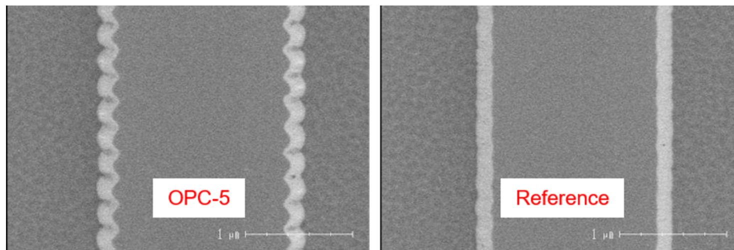


Figure 5.12: Patterning result with and without optical proximity correction applied.

5.6 Conclusions

Rule-based OPC was demonstrated for InP PICs using a sidewall grating device as a test vehicle. Pattern fidelity was optimized by performing an XOR operation on simulated resist profiles and the design intent and by minimizing the resulting surface area. Best OPC enabled structures show 70% improved resist pattern fidelity compared to a reference design without OPC applied. Although further improvement to the pattern transfer is required, the positive effects of OPC are well visible even into the InP semiconductor. Well-defined OPC rules derived from simulations are the way forward to match fabricated device geometries with the design intentions.

It is proposed to include the effects of the etch steps into the modeling phase of future work. This would require the identification of relevant parameters that influence the loss of pattern fidelity during the etch steps. Some parameters that may affect the etch behavior, could be the local pattern density but also the aspect ratio of the nano-features. With the proper set of parameters, optimization could be done at the circuit design level to compensate for these effects at the reticle design level.

Chapter 6

Overlay for photonic integrated circuits

6.1 Introduction

The term overlay is used in semiconductor manufacturing to describe the accuracy with which one fabrication layer can be put on top of a previous layer [40]. Since the lithography steps determine the pattern position, it is required to investigate the specific set of tools involved in exposing these layers. When trying to minimize the overlay errors, it is necessary to distinguish between the different contributions to these errors.

This chapter will define the overlay contributions and presents the matching method that was developed to optimize overlay between the Scanner and Stepper equipment in the NanoLab@TU/e cleanroom for fabrication of PICs on InP. The exploitation of the matching results is demonstrated by fabrication of a spot-size converter (SSC) through a combination of scanner and stepper layers. The overlay performance on this demonstrator run is determined and the first device measurements are presented.

Next, the need for a manufacturable polarization converter (PC) in the TU/e generic platform is motivated and the previous work on this topic is introduced. The choice for a specific device geometry is motivated together with simulation results on the performance and sensitivity of this geometry. Then, a conceptual process flow is proposed and the results of the feasibility study on this flow are shown. The fabrication results of a multi-project wafer (MPW) short-loop run with multiple PC device designs are described, followed by the characterization results of the single section polarization converter component. Based on these results, some follow-up experiments to improve the fabrication process are presented and some suggestions are proposed for further research on this topic. Finally, conclusions are drawn from the work that is presented in this chapter.

6.2 Overlay quantification and specification

Overlay performance is typically quantified as the distribution and size, of relative position errors of specific locations within two lithographic layers on a wafer. For the overlay performance, random stage positioning errors can be the cause of relative shifts between the layers. Apart from calibrating stages and maintaining their performance, these are mostly hardware limited and cannot be corrected for. Secondly, since both scanners and steppers repeatedly move the wafer to a specific location to perform a single exposure, systematic errors can occur. These can be divided in two categories as illustrated in Fig. 6.1. There are overlay errors between different exposure fields (inter-field), which can be caused by wafer deformation, rotation, translation errors, marker processing or readout. There are also overlay errors within exposure fields (intra-field), which are typically caused by magnification errors, skew or trapezoid deformation of the image, lens distortions and reticle rotation.

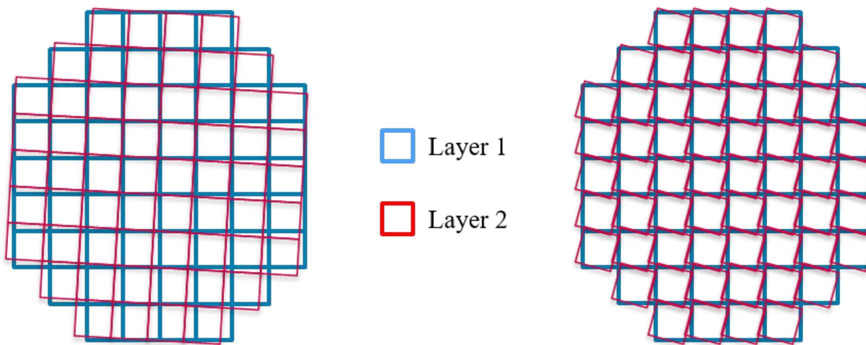


Figure 6.1: Systematic overlay errors between blue layer 1 and red layer 2: inter-field (left) and intra-field (right).

Because both inter- and intra-field overlay errors are systematic, they are typically smaller when both layers are exposed on a single machine than when two different machines are used. Specifications for single machine overlay (SMO) are therefore significantly tighter than matched machine overlay (MMO) specifications. Table 6.1 lists the ASML acceptance test protocol specifications for both NanoLab@TU/e tools, as well a PAS5500/60 stepper which is used for generic PIC fabrication by SMART Photonics. When combining different machines, MMO overlay specification is important, and the maximum performance is in principle always limited by the worst performing tool.

The performance numbers listed in Table 6.1 however, cannot be achieved and maintained without effort. For SMO, a machine can in principle drift over time, and the actual overlay numbers depend on marker quality and layer structure as well. For MMO, in addition to the above the systematic machine signatures are totally different to begin with. For these reasons, a system needs to be calibrated to achieve minimal overlay errors by a process called matching. By performing a matching procedure, a machine can be kept stable and various correction parameters can be calibrated to

System	Stage Rep.	SMO	MMO
PAS5500/1100B	< 8 nm	< 15 nm	< 25 nm
PAS5500/60	< 19 nm	< 90 nm	< 150 nm
PAS2500/40	< 100 nm	< 150 nm	< 250 nm

Table 6.1: Overlay related system specifications for lithography equipment used for generic PIC integration fabrication.

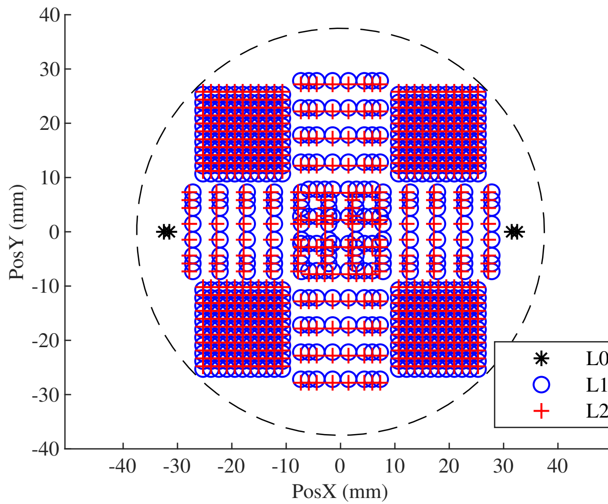
pre-compensate for the systematic overlay errors caused by the signature differences between the two tools. The best machine is typically used as the reference tool, while all other tools will be matched to this by pre-correcting their signatures.

6.3 Overlay matching procedure

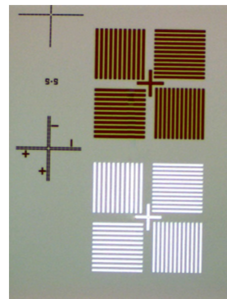
One of the big challenges to accomplish matching between the NanoLab@TU/e tools, was the fact that the scanner and stepper are almost 15 years apart in generation, stemming from the late 1980s and early years of this century respectively. There were no existing procedures for the unique combination of these tools, therefore a custom matching procedure needed to be developed. This was done in close cooperation with ASML application support by adapting and combining both old and new matching procedures, wafer- as well as reticle layouts.

The principle of matching revolves around exposing a wafer with a zero-layer (L0) on the best performing tool. This so-called reference tool, the ASML scanner in this case, is used without any overlay correction parameters enabled. Aligned to L0, layer one (L1) is exposed with the reference tool, containing various arrays of alignment markers distributed over the imaging field. The L0 and L1 markers are then transferred into the wafer substrate. Next, layer two (L2) is exposed with the stepper, aligned to L0 as well. This results in a total wafer layout as shown in Fig. 6.2a. The layout of L2 is in fact a copy of L1 with a deliberate position offset. After development of the L2 markers, the relative position of each L1-L2 marker pair as illustrated by Fig. 6.2b is measured using the stepper alignment system.

The deviation from the pre-determined offset of each pair is the resulting overlay error of the combination of the L1 and L2 exposure tools on a particular location of the exposure field. The overlay error data can then be modeled to calculate inter- and intra-field correction parameters as well as some residual shifts, based on exposure position of the field on the wafer. The correction parameters include red-blue offsets, translation scaling, rotation scaling, non-orthogonality, and mirror curvature. These are stored in the system as pre-compensation for all subsequent exposures. Typically, the L2 exposure can be redone for verification or reiteration of the matching result, after reworking the wafer, with the correction parameters applied. System drift can be compensated by repeating the matching procedure periodically.



(a)



(b)

Figure 6.2: Matching wafer layout (a) and photograph of L1 and L2 marker pair (b).

6.4 Overlay matching results

For interpretation of the matching result, the overlay error of each marker pair can be displayed as a vector. The relative size and direction of these vectors can graphically indicate the error at each position of the exposure field and wafer. Fig. 6.3 shows the overlay vectors for each of the four full-field exposures in the corners of the wafer. In the center, a calculated representation of averaged vectors of the fields is drawn in blue. The statistics on this field are displayed in the legend, showing mean overlay errors in both directions, standard deviation of these errors, the maximum error values for both directions, and lastly the size of the largest measured averaged vector of a marker pair. Fig. 6.3 represents the starting situation, prior to having any matching parameters enabled on the stepper. Apart from signature differences between the upper and lower fields, there is a large average field offset in the X direction of -188 nm and worst case overlay errors of the average field, are as high as -425 nm.

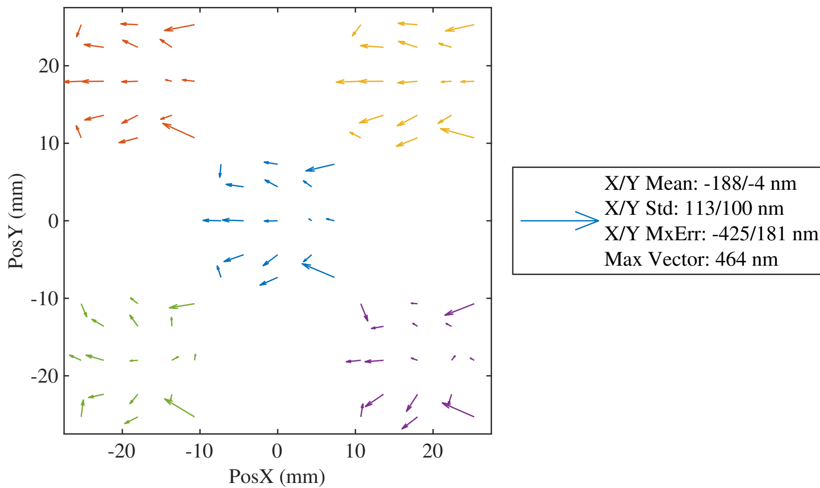


Figure 6.3: Field overlay error vectors in unmatched situation (17 markers).

After calculating the matching correction parameters to remove the systematic errors, and remeasuring new wafers where layer 2 was exposed with these corrections applied, the result shown in Fig. 6.4 was achieved. It is clear from this plot that the overlay has significantly improved. The exposure fields now have a negligible mean offset of less than 20 nm. Additionally, the individual fields have a much more comparable signature, indicating that inter-field overlay was significantly improved. Maximum overlay error of the average field only reaches as high as -246 nm, although intra-field standard deviations are still quite high in the low hundreds. What is most disturbing about these results, is that the vectors at the outer corners, point inward whereas most other vectors are pointing outwards. This indicates a 3rd order lens distortion, which cannot be corrected through lens corrections on this generation of tool. With this 17-point measurement layout, the corners of the exposure field have almost 25% influence on determining the overall matching correction parameters.

In principle, it is also possible to measure all the exposed marker pairs per field. By doing this, the weight of the outer corners as is illustrated by Fig. 6.5, is roughly reduced to 10%, with 12 out of 121 pairs. This is a significant improvement over the 17-point measurement layout. The increased number of measured markers also increases the accuracy of the modeling of both the inter- and intra-field overlay errors. By performing the matching procedure with the full marker set, a further improved result is achieved, as is shown by the listed overlay statistics. The average field vector is still close to zero while the maximum overlay error of the average field is below -238 nm. The overlay vector standard deviations for the average field are now below 80 nm, which shows that the MMO specifications from Table 6.1 can be reached.

It is also clear that if better overlay performance is required for certain applications, a concession can be made by reducing the image field size so that the intra-field overlay errors decrease. Additionally, the matching procedure can be performed only on a selection of markers within the required design space of the device reticle. Lastly,

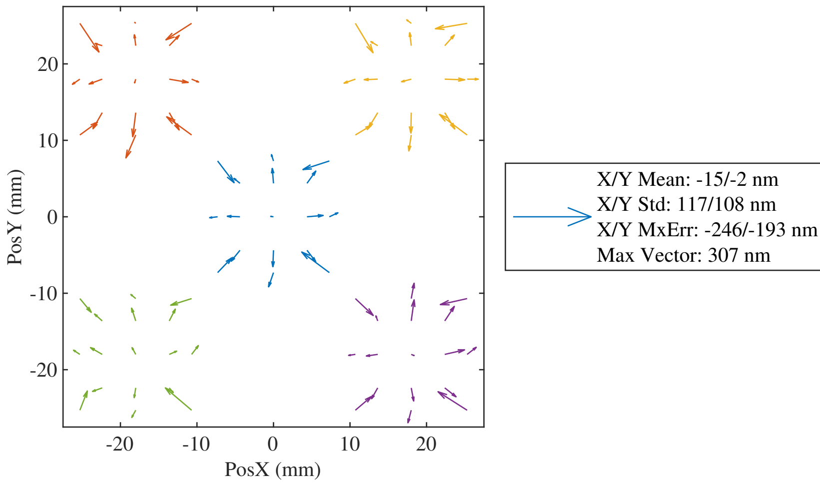


Figure 6.4: Field overlay error vectors in matched situation (17 markers).

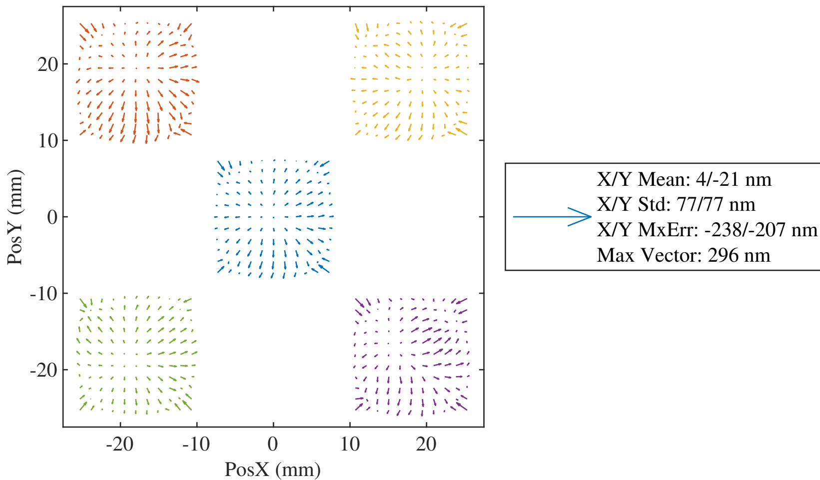


Figure 6.5: Field overlay error vectors in matched situation (121 markers).

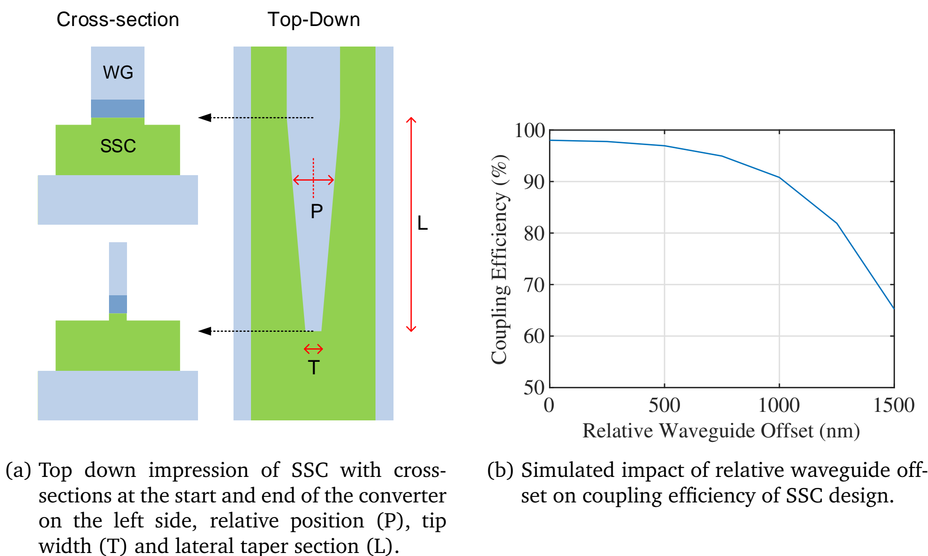
the 3rd order lens distortion of the stepper could be compensated at the reticle level in the design phase, if full field exposures are required. Despite the possibilities for further improvements, the overlay performance between scanner and stepper is a 4 times improvement over what could previously be achieved through overlay with contact alignment lithography alone. Realistically, overlay accuracy in the region of 1 μm was feasible here, through manual alignment with an optical microscope.

6.5 Generic integrated spot-size converters

A spot-size converter (SSC) is an example of a component that can take advantage of improved overlay and dimensional control. During this work, such building block was unavailable in the TU/e generic InP platform. The default output waveguides that are available in this platform have a mode field diameter (MFD) of approximately 2 μm, while a cleaved single mode optical fiber or an ultra-high numerical aperture fiber (NA 0.3-0.4) have a MFD of approximately 10 μm and 4 μm respectively. It is therefore desirable to increase the size of the waveguide MFD to increase the mode overlap and improve fiber-chip coupling efficiency as well as the alignment tolerances.

A proposed way to do this, is to create a wider waveguide with different material composition underneath the original waveguide level. This requires a substantial amount of epitaxy prior to the regular growth process. Therefore, it was decided to design for a 4 μm MFD which is suitable for coupling with ultra-high numerical aperture fibers. This SSC design is schematically represented in Fig. 6.6a. In this SSC, the light from a typical deep etched waveguide (1.5 μm), is adiabatically coupled into the lower waveguide (4 μm), by gradually tapering the width of the top waveguide along the propagation direction of the light in section (L).

Fig. 6.6b shows a simulation result of this SSC geometry performed by M. Spiegelberg, which shows that the positioning of the top waveguide relative to the lower waveguide (P) has a significant influence on the internal SSC waveguide coupling efficiency. Therefore, overlay matching as described in the previous sections is very important for the SSC performance. Additionally, the dimension control of the taper section and CD of the tip (T) are very important, which requires the use scanner lithography for the top waveguide.



(a) Top down impression of SSC with cross-sections at the start and end of the converter on the left side, relative position (P), tip width (T) and lateral taper section (L).

(b) Simulated impact of relative waveguide offset on coupling efficiency of SSC design.

Figure 6.6: Schematic of SSC component and simulated coupling efficiency.

A feasibility study of a fabrication process was performed to create SSCs with a combination of scanner and stepper lithography steps, as is schematically represented in Fig. 6.7. The top waveguide in this scenario is realized through regular scanner waveguide processing as described in Chapter 3. To realize the lower waveguide, a new thick nitride hard mask was deposited over the existing waveguide pattern in step 1. During overlay-critical step 2, stepper AZ4533 lithography was performed on top of the existing waveguide, aligned to the scanner layer. The resist pattern was then used to etch the nitride hard mask and the resist was removed during step 3. On the subsequent step 4, deep waveguide etching was performed using the Oxford ICP with standard CH_4/H_2 chemistry to pattern the lower SSC waveguide. Step 5 removed the nitride mask revealing the stacked waveguides on top of each other.

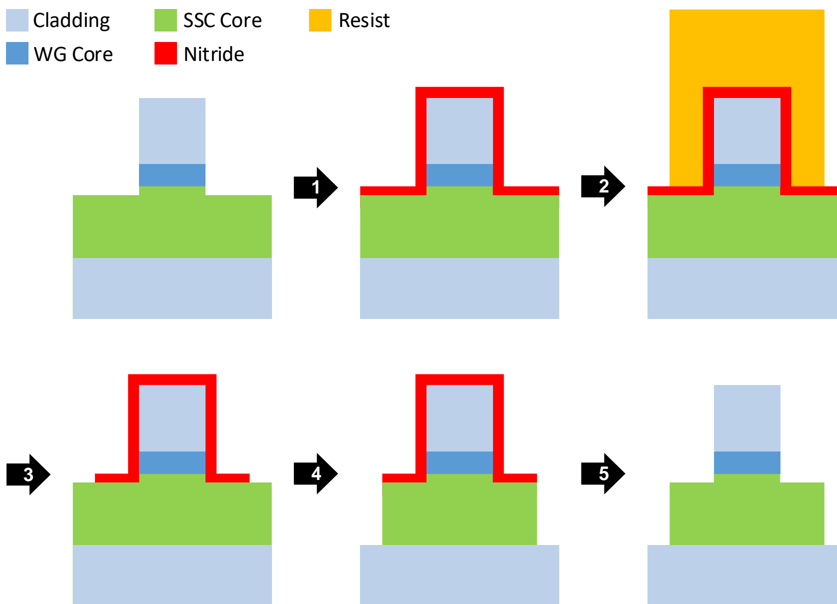


Figure 6.7: Spot-size converter fabrication concept.

Two wafers were processed with the proposed flow from the previous paragraph. As can be seen from the SEM photographs in Fig. 6.8, the narrow tip of the scanner defined waveguide was well preserved and aligned on top of the lower SSC waveguide. To confirm the overlay accuracy, CDSEM measurements were performed on 43 sites per wafer after full waveguide processing. The distance between the bottom of the upper and lower waveguides was determined on the left and right side of each SSC tip. The difference between both sides, was then divided by two to calculate the overlay error for each individual structure.

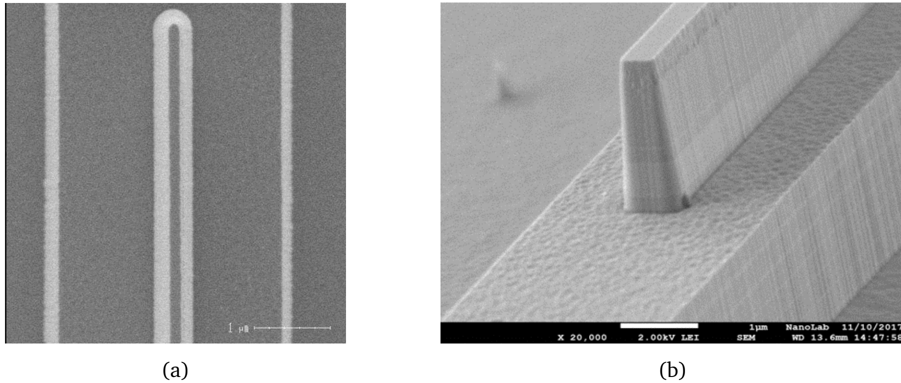


Figure 6.8: SEM photographs of SSC, top-down view (a) and tilted view (b).

Because the output waveguides were all oriented in the horizontal direction, only the vertical inter-field overlay error was determined. The measurement results presented in Table 6.2, show that the on-chip overlay errors for the measured wafers were less than ±250 nm, although a mean layer shift of -94 nm was observed on Wafer 2. This could be explained by a difference in marker quality between both wafers as the second wafer was initially rejected during the alignment stage of the exposure.

Overlay Errors (nm)	Wafer 1	Wafer 2
Mean	-14	-94
Minimum	-130	-220
Maximum	120	2
3σ	225	184

Table 6.2: Overlay error CDSEM results of fabricated wafers measured on 43 locations.

One of the chip designs for this run, contained a design of experiments on the different geometry aspects of the SSC. These parameters are illustrated in Fig. 6.9 as the different waveguides widths and taper lengths represented by W1-W5 and L1-L3 respectively. The design of experiments consisted of a fractional $2^{(8\text{-}4)}$ factorial setup for a total of 16 SSC variations. For each design variation, the SSC on the input and output side of the chip were identical and connected with a deep etched waveguide. Transmission measurements of these variations were performed by K. Prifti of the Electro-Optical Communications (ECO) group.

For the measurement setup, a tunable laser source (TLS) was used to pass light through a polarization controller to maximize coupling efficiency. Lensed fibers with a specified focus spot size diameter of 3.5μm, were used with three-axis stages to couple in and out of the chip. The power of the injected and transmitted light at 1550 nm was measured simultaneously. The SSC insertion losses were calculated from these values, correcting for the deep etched waveguide propagation losses which were estimated

to be 3.5 dB/cm. The six best-performing SSCs from the DOE are shown in Table 6.3. As can be seen in the table, a best-case insertion loss of less than 1.5 dB per SSC was measured on one of the designs. These SSCs were enabled by the improved scanner resolution and CDU in combination with stepper overlay matching.

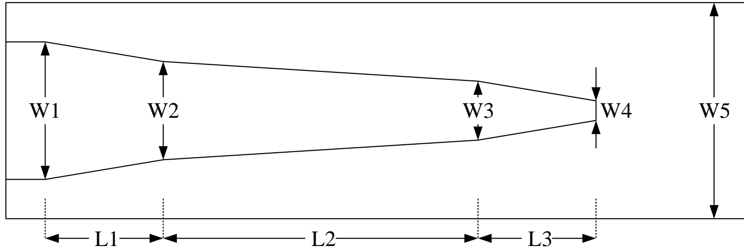


Figure 6.9: Top-down impression of SSC design of experiments parameters: waveguide widths W1-W5 and taper lengths L1-L3.

SSC Length μm	Tip Width nm	Insertion Loss dB/SSC
874	300	1.1
2239	600	2.8
1817	300	2.1
2239	300	2.6
2068	300	3.2
918	600	4.0

Table 6.3: Insertion losses of six best-performing fabricated SSCs.

6.6 Generic integrated polarization converters

Another component that can exploit the improved overlay and dimensional control of scanner and stepper lithography combinations is a polarization converter (PC). On-chip polarization handling can be very interesting to create polarization-sensitive functionality or to optimize chip component performance for specific polarization states. Typical applications taking advantage of polarization handling are in communication for polarization division multiplexing (PDM) [111] and sensing for polarization optical time domain reflectometry (POTDR) [112]. The idea of having a PC component available in a generic InP platform has therefore been topic of several academic research projects in the past.

In 2008, two projects were run to realize polarization handling for PICs. U. Khalique [113] fabricated PCs using different types of lithography with specifically optimized process flows. Contact, projection as well as electron beam

lithography were used to achieve maximum conversion of 90%, 96% and 99% respectively. However, the applied techniques only work with a specifically thin top cladding that is incompatible with the current TU/e platform. Almost simultaneously L. Augustin [114] realized PCs with up to 97% conversion using a compatible generic layer stack. However, the required overlay and dimensional tolerances could only be achieved through fabrication with EBL and i-line stepper at that time.

In 2014 M. Felicetti [115] worked on post-processing of PICs fabricated by Oclaro to realize a PC, but like with most realizations, EBL was required to enable this. Single section and double section devices were fabricated showing up to 97.5 and 99.5% conversion respectively. That same year, D. Dzibrou [116] completed a research project to realize a PC component in the Fraunhofer Heinrich Hertz Institute (HHI) platform. This component was realized through a combination of optical lithography and EBL steps and showed 95% conversion in the realization. The HHI polarization technology was further developed and most recently enabled the work of M. Baier [117]. In this work PC devices were measured with up to 99.6% conversion efficiency, while the PC component is now available in the HHI generic MPW process [118].

Apart from the above-mentioned PC concepts where asymmetry is created through a sloped sidewall some other concepts have been demonstrated as well. There have been several demonstrations on different material platforms, of waveguides with one or more narrow trenches etched into the waveguide on one side [119–122]. This concept requires very accurate control of the etch depth of the trench however, which is subject to an aspect ratio dependent lag effect, and would likely be hard to control. There are a few demonstrations of angled waveguides etched with chemically assisted ion beam etching [123, 124]. This dry etch technique however, is not very suitable for large-scale generic manufacturing at full wafer scale, since it relies on accurate 3D positioning of the sample relative to the ion beam in the reactor. An asymmetric waveguide with one shallow and one deep etched side was also demonstrated [125]. This concept could in principle be very well integrated, but the control of the shallow side would be quite challenging.

6.6.1 Creating a manufacturable converter

The operating principle of the polarization converters described in the previous section, is as follows. At the input side of the waveguide section with asymmetric geometry, two tilted modes are excited that propagate at a different speed. Due to the phase difference induced by the propagation in this section, these modes recombine into a different polarization state at the output side. As such, polarization rotation can be achieved and tuned by the geometry and length of the section. The manufacturability and performance of the component depends on how well the geometry of the asymmetric polarization section can be controlled.

With the HHI concept and several of the other demonstrations mentioned in the previous paragraph, the problem to apply this in the TU/e platform, is in the difference between the layer stack designs. The top of a waveguide in the TU/e process is significantly further away from the waveguide layer than in the case of HHI. For this reason, it is challenging to start the PC slope from the top of the waveguide mask.

The slanted sidewall of the waveguide would be too far from the waveguide core, resulting in a very inefficient PC.

The concept of L. Augustin seems most suitable for integration in the TU/e platform, since the biggest limitations are in the requirements for the lithography. With the projection lithography equipment, it should be possible to have enough dimensional control through the capability of the scanner, and enough overlay accuracy through the use of the stepper for the later fabrication stages. In contrast to the application of EBL, the projection lithography tools are very well suited for high volume production and pose no problems in terms of scalability of the technology platform.

In terms of manufacturing tolerances, it is known that the use of a "double section" device design can greatly decrease sensitivity to dimensional variations [126]. The schematic Fig. 6.10 shows a PC building block, where a passive deep waveguide is connected through a lateral taper, to a double polarization section and then via another lateral taper back to a passive deep waveguide. This creates a fully decoupled building block that can be integrated with the existing generic platform. To make sure that the slope is close to the waveguide core, it is necessary to control the width of the waveguide at the starting point of the slope, and to start the slope at a controlled etch depth close to the core.

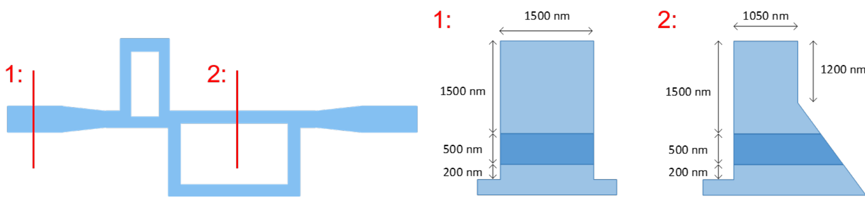


Figure 6.10: Top-down view of generic PC (left), and cross-sections at the marked intersections of waveguide (1) and polarization section (2).

6.6.1.1 Simulating polarization converter performance

The conversion performance of the proposed device geometry as shown in Fig. 6.10 was simulated and optimized through a full vectorial mode solver called FimmWave [127] by J. v.d. Tol of the Photonic Integration (PhI) group. The performance of single and double section devices was compared in terms of sensitivity to width variation in Fig. 6.11a. In these simulations, the target starting point for the slope was 300 nm above the waveguide layer. The total section length for the single and double section devices was chosen at 198 μm and 397 μm respectively. The simulations were performed at a target wavelength of 1550 nm. From this figure, it is clear that the optimal width is different for both device types and the sensitivity to width variations is much higher for single section devices.

Since the starting point of the slope has a high influence on the conversion behavior of this component, it is important to look at the accuracy of the etch depth that defines this starting point. Fig. 6.11b shows the sensitivity to depth variations of single and double section devices at a target width of 1000 nm and 1050 nm respectively. Negative numbers in this figure, indicate that the starting point of the slope

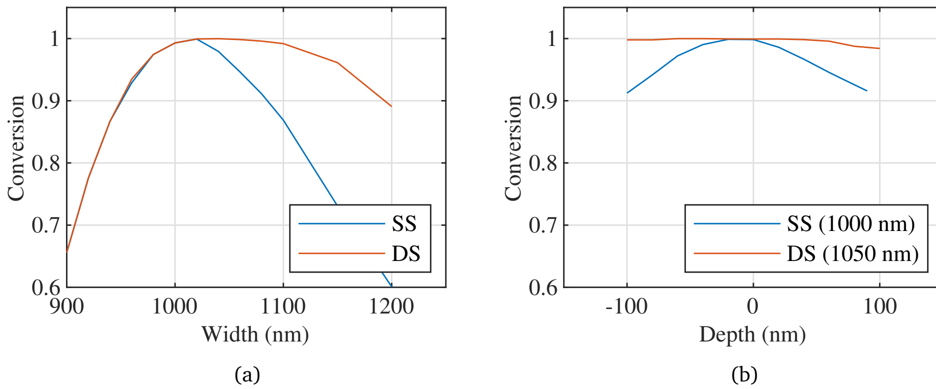


Figure 6.11: Simulated Conversion of Single Section (SS) and Double Section (DS) devices as a function of conversion section width (a) and etch depth (b).

moves closer to the waveguide layer and the other way around. Similar to the other figure, a tolerance improvement to manufacturing errors of double section devices is clearly shown. High conversion rates are predicted to be feasible with the proposed device geometry and manufacturing tolerances will in practice strongly depend on the conversion requirements of the application.

In terms of wavelength sensitivity, Fig. 6.12 shows above 96% and 99% conversion performance across the entire C band for single and double section devices respectively. The double section device shows significantly less sensitivity to the wavelength in terms of polarization conversion. As with the simulation on depth sensitivity, the widths for this comparison were chosen to be 1000 nm and 1050 nm for single and double section devices respectively.

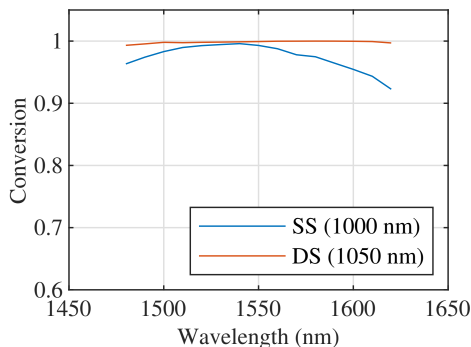


Figure 6.12: Wavelength dependence of single (SS) and double section (DS) devices.

6.6.1.2 Process flow feasibility study

To realize the polarization converter geometry from Fig. 6.10, the process flow shown in Fig. 6.13 was proposed. At the start of this process, a waveguide is defined with scanner waveguide patterning as described in Chapter 3, with a depth equal to the starting point of the slope. During step 1, the first overlay-critical stepper lithography is performed to protect the polarization section with AZ4533 resist. This overlay critical step needs to be done with the stepper since the topography at this stage of the process is too high to be done with the relatively thin ArF scanner resists. During step 2, the combined resist-hard mask is used to realize the correct waveguide etch depth outside the polarization sections after which the resist mask is removed.

Step 3 will deposit a conformal 100 nm SiN layer on the entire sample using PECVD. During Step 4 the next overlay-critical lithography step is performed which opens the polarization sections. After the dielectric dry etch of step 5, the polarization sections are open, while leaving a self-aligned spacer on the sidewall of the PC section. During step 6, the sloped sidewall is etched using diluted BrMeOH at a volumetric dilution of 1:1500. This etch is known to follow a crystal orientation leaving a slope of 54.7 degrees [128]. During the last step all dielectric material is removed from the sample through BHF, which exposes the desired geometry.

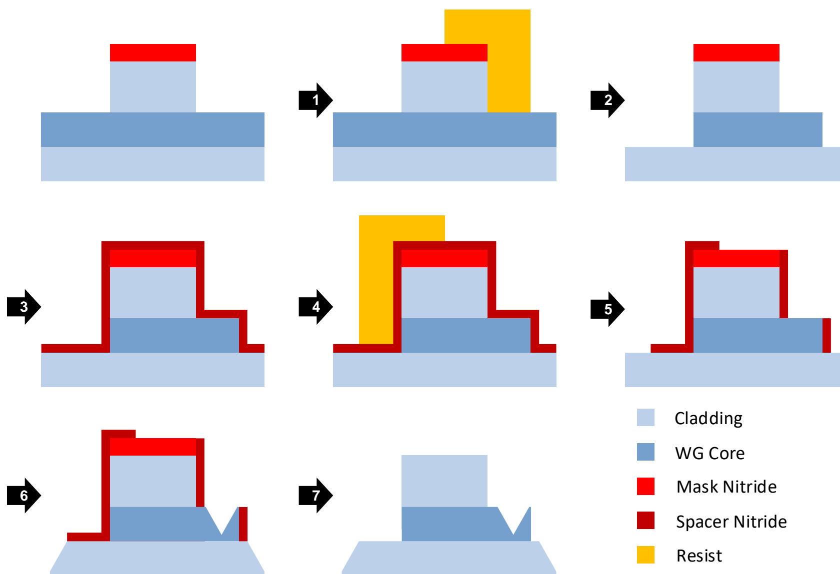


Figure 6.13: Process flow proposal for a generic polarization converter in the TU/e technology platform.

The feasibility of the proposed flow was tested on an InP wafer using a complementary set of scanner and stepper reticles containing an identical waveguide design for both tools. This test was performed, by masking the scanner waveguide with itself, slightly offset from the original position during the subsequent stepper lithogra-

phy steps. This was done to simulate the opening and protection of the polarization sections. A SEM photograph of the result of this experiment is shown in Fig. 6.14. This figure shows very good resemblance to the intended device geometry shown in Fig. 6.10. On the left side of the waveguide, the deep waveguide etch depth is generated, while the starting point of the BrMeOH etch is defined at a different depth by the initial scanner patterning. The slope looks very well-defined at the expected angle with a smooth etch surface. Further away the slope stops which is where the etch becomes diffusion-limited, does not follow the crystallographic orientation, and is significantly slower.

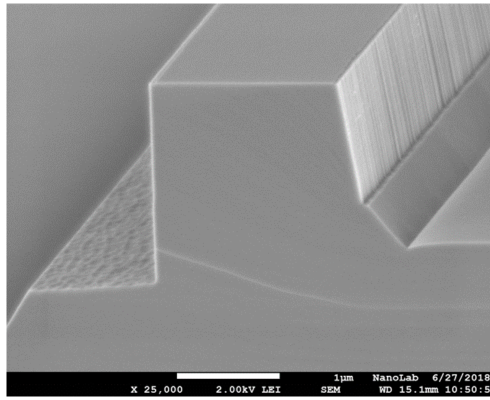


Figure 6.14: SEM cross-section of feasibility experiment on generic PC flow.

6.6.2 Fabrication of polarization converter devices

An MPW wafer layout was tested with the proposed process flow using a generic passive layer stack provided by SMART Photonics. Both deep and shallow passive building blocks were offered for this short-loop as well as a PC building block. This block was offered with some design freedom to choose between single and double section type, as well as PC section length and PC waveguide width. Since this was a short-loop, no passivation or metallization stages were performed to reduce the number of unnecessary process steps for the test. All samples were provided with anti-reflection (AR) coating on both sides, since the devices would be characterized with a transmission measurement setup, to reduce the impact of back-reflections. The super-cell layout as shown on the right side of Fig. 6.15, contained 6 designs from several users. The supercell was repeated at wafer level with a suitable layout to facilitate chip separation as shown on the left side of Fig. 6.15.

The resulting PC geometry of this run however, was unexpected as is illustrated by Fig. 6.16. This figure shows that the original design intent as illustrated on the left, was undercut during the BrMeOH wet etch step, resulting in a different device geometry as shown on the right side. This means that depending on the speed of this under etch, the slope moved closer to the waveguide core. This shift was estimated to be between 0 nm for the original starting point of the wet etch, and 180 nm

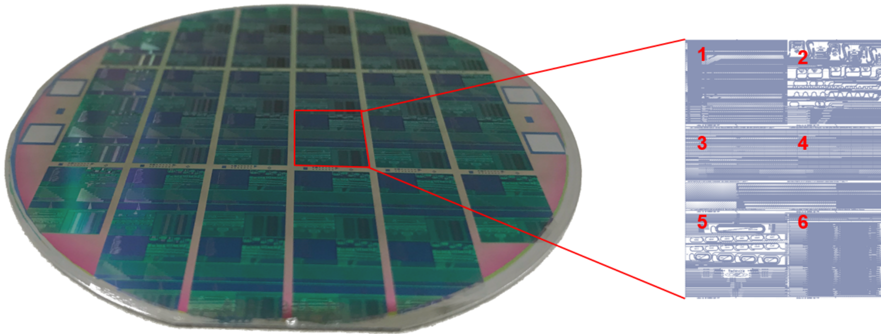


Figure 6.15: Photograph of MPW wafer layout (left) and super-cell design (right).

when fully undercut up to the top corner of the waveguide. L. Augustin showed in simulations that partial removal of the top cladding, does not necessarily create a poor PC component [114]. However, due to the unintentional offset in the obtained width, the component needs a shorter length to achieve maximum conversion. It was therefore expected that the MPW single and double section devices with the chosen lengths would rotate the polarization too far, resulting in a lower conversion.

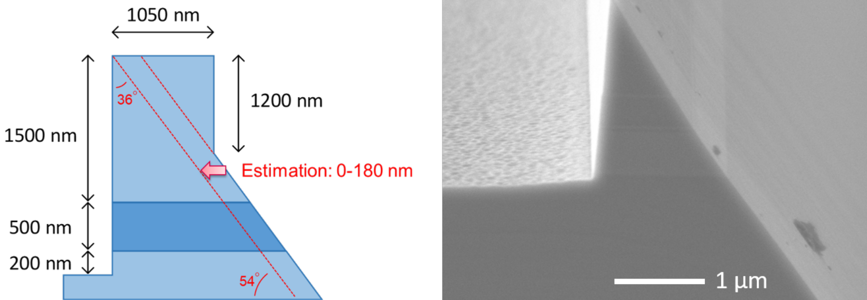


Figure 6.16: MPW short-loop PC section design (left) and resulting triangular geometry (right).

6.6.3 Device characterization

Due to the great number of PC devices with different widths, lengths and from several different chips and wafers, it was necessary to use a semi-automated measurement setup. Such a setup was built over the past few years to do automated transmission measurements with very high repeatability [129]. This capability reduces the required effort to perform these device measurements enormously. Although routines and hardware were present to run automated alignment of standard waveguides with this setup, polarization sensitive measurement capability was only recently added on the system.

To determine the polarization conversion efficiency of the fabricated devices, it is necessary to measure the transmitted signal in both transverse electric (TE) and transverse magnetic (TM) orthogonal polarization states. This is measured by sequentially using both orthogonal states as input. The conversion efficiency can be calculated from these measurements using (6.1) and (6.2), where $P_{(s1\text{-}s2)}$ represents the output power in polarization state (s2) and the input light has polarization state (s1) [114].

$$\text{Conversion} = \frac{\sqrt{x}}{1+\sqrt{x}} \tag{6.1}$$

$$x = \frac{P_{(TE-TM)}\,P_{(TM-TE)}}{P_{(TE-TE)}\,P_{(TM-TM)}} \tag{6.2}$$

To achieve this, a measurement setup was built as is schematically shown in Fig. 6.17. To maintain polarization states in the setup, polarization-maintaining (PM) fibers were used throughout the entire light path and connected by using tight fit connectors. A TLS was used as a source at 1550 nm wavelength at 10 dBm output power. To increase the polarization extinction ratio (PER), the TLS was connected to a polarization filter. Depending on the required input state of the measurement, a 90° polarization rotator was inserted. Both coupling lensed PM fibers were individually calibrated for maximum polarization extinction and permanently attached on a holder. In the fiber to fiber coupling situation, this resulted in a PER of 19.2 dB and 15.4 dB for TE and TM measurement respectively. Average transmitted power of the entire setup excluding the chip in this situation was 2.5 dBm.

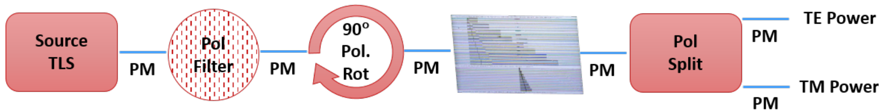


Figure 6.17: Transmission measurement setup for determining polarization conversion.

The chip was placed on a temperature-controlled vacuum stage that can be moved in a plane that is perpendicular to the light path. The lensed coupling fibers were both mounted on 3 axis stages, that allowed fully programmable movement in three dimensions. On the output side, a polarization splitter separated the power into both orthogonal states and allowed simultaneous measurement with calibrated power meters. The on-chip PER at 1550 nm for straight reference waveguides was determined to be 22.2 dB and 26.0 dB for TE and TM measurements respectively.

Data was collected from devices with different design widths and lengths from multiple chips. Due to an error in the device length variations of the double-section design, only single-section PC devices could be characterized. The length variations for the double section devices were accidentally spread over multiple conversion periods, making it impossible to get a reliable fit. The obtained power values were used to calculate conversion for every component where the total transmitted power of both polarization states was higher than −15 dBm (on average -3.5 dBm).

Fig. 6.18 shows the polarization conversion as a function of the length of the component for design widths ranging from 750 nm to 1250 nm. The measurement

data is represented in blue dots, whereas the red curve shows a numerical sinusoidal least-squares fit of the conversion data, described by (6.3). This fit-type was chosen, based on the periodic behavior that's expected from the beating of the guided modes in the polarization section of the component. In this equation, f_1 - f_4 represent the fit parameters, while the length is specified in μm.

$$\text{Conversion} = f_1 + f_2 \sin\left(f_3 \cdot \text{Length} + f_4\right) \tag{6.3}$$

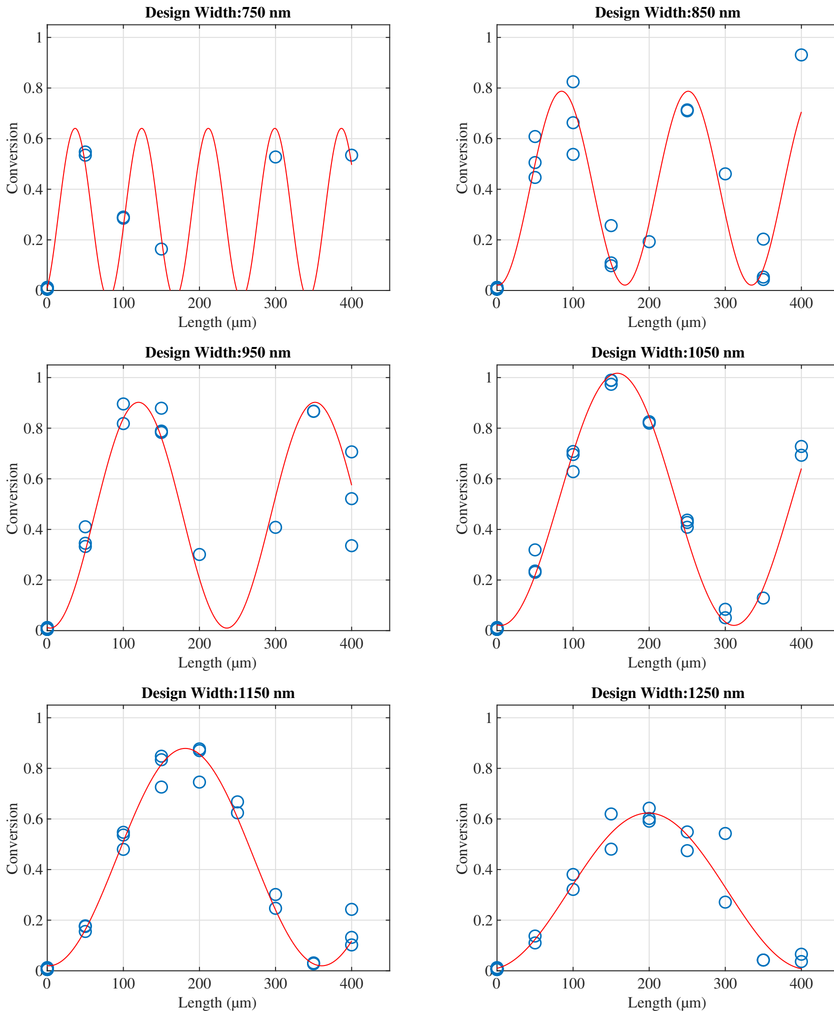
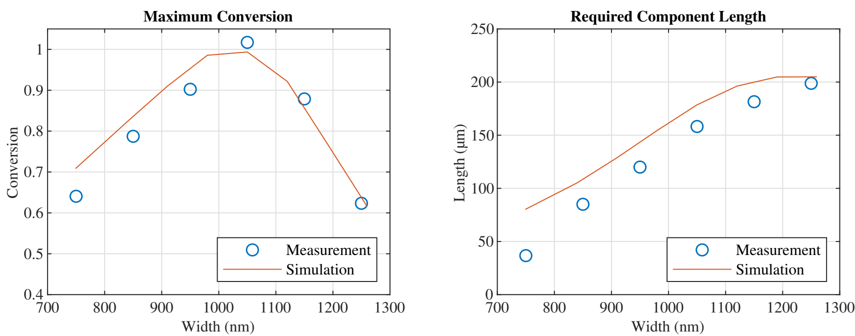


Figure 6.18: Conversion as a function of device length at different design widths, measurement points in blue and sinusoidal fit in red.

Several devices were measured at 1050 nm width and 150 μm length showing up to 98.9% conversion. As can also be seen in the measurement data of Fig. 6.18, there were no devices designed at any width with the exact length that would achieve maximum conversion. Therefore, the fit parameters were used to estimate maximum conversion as well as ideal component length for each design width, equivalent to the first maximum of each curve. The resulting data was plotted in blue dots in Fig. 6.19a and Fig. 6.19b respectively. This data was compared to additional simulation results obtained by J. v.d. Tol, for devices with the obtained triangular geometry of the MPW run. In terms of maximum attainable conversion as shown in Fig. 6.19a, there is an optimum width at around 1050 nm. For this width, there is agreement between the trends of the experimental data and simulation results.



(a) Maximum conversion for specific design widths at ideal length.

(b) Required component length for specific design widths.

Figure 6.19: Relation between design width and maximum conversion and required length, measurement data in blue and simulation of geometry as red line.

Fig. 6.19b shows that there is relation between the design width and the required component length to achieve maximum conversion. When the devices get wider, a longer polarization section is required to achieve maximum conversion for that width, corresponding to the period of the sinusoidal fits in Fig. 6.18. This happens because the beat length of the propagating modes increases, when the effective asymmetry of the waveguide decreases, and their propagation speeds approach each other. There is a width offset between the experimental data and simulation results. It is likely, that this can be explained by a difference between the designed width and the fabricated width of the devices. Based on the combined results, single section PCs with a design width of 1050 nm and a length of 159 μm will result in maximum conversion.

As previously discussed, double section devices could not be characterized because of an error in the length variations of the design. However, simulations were performed by J. v.d. Tol to determine and compare the width sensitivity of single and double section devices with the obtained triangular device geometry at fixed component lengths of 178.6 um and 355 μm. Fig. 6.20 shows that very high conversion can be reached over a significantly wider width range using the double section device configuration. The ideal width for a double section device is approximately 50 nm wider than a single section device, resulting in 1100 nm at a length of 355 μm. This ensures

fabrication tolerance on both the narrow and wider side of the dimensional variation. The double section PCs show significantly more tolerance to width variations while maintaining high conversion.

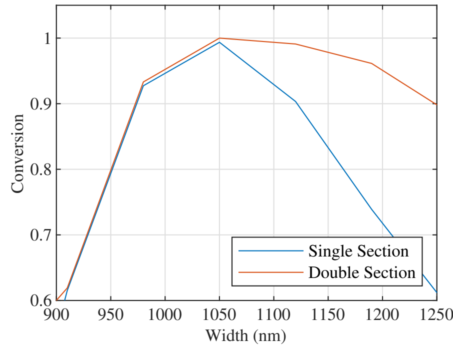


Figure 6.20: Conversion as a function of design width for single section devices with triangular geometry in blue and double section devices in red.

6.6.4 Process improvements and recommendations

The previous section discussed that the obtained PC geometry of the MPW run, can in fact reach very good performance in terms of polarization conversion when designed with the appropriate width and length. Furthermore, manufacturing tolerances are still expected to increase significantly when using a double section type design instead of the single section type devices that were characterized. To investigate if this geometry is manufacturable, it is necessary to look at the stability and behavior of the BrMeOH wet etch.

An experiment was performed to determine the BrMeOH under etch rate, and to observe if the etch was self-limiting in the upper corner of the device along the [1 1 1] crystallographic etch plane. In this experiment, the process flow as proposed in Fig. 6.13 was altered by replacing the dry etch in step 5, by a 60 second BHF wet etch step. The isotropic nature of the BHF step would supposedly expose the sidewall of the PC waveguide on one side and allow the BrMeOH etch to penetrate underneath the waveguide mask immediately from the start.

The experiment was analyzed using focused ion beam (FIB), to make local SEM inspections on device widths between 750 nm and 1250 nm on samples etched with different BrMeOH etch times. The under etch dimensions were measured and plotted in Fig. 6.21 as a function of etch time. As presented, the BrMeOH under etch behaves quite linearly at 1 nm/s independent of design width, up until the point that the etch plane reaches the outer top corner of the PC section. At this point, it seems that the etch accelerates slightly and the under etch dimensions could only be estimated by extrapolating the position of the etch plane to the top level of the waveguide.

This occurred on the narrowest width of 750 nm after 90 and 120 seconds of BrMeOH etch respectively, resulting in the outliers of Fig. 6.21. A cross-section of

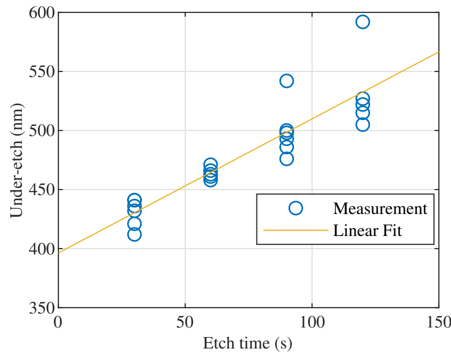


Figure 6.21: BrMeOH under-etch as a function of etch time for various design width variations.

what the device geometry is like after reaching the PC outer corner is shown in Fig. 6.22. This figure shows evidence that the etch does not seem to be self-limiting at the crystallographic plane, and needs to be controlled more strictly than expected in terms of etch time. The etch plane still propagates along the vertical direction of the PC geometry and leaves the original hard mask hanging from the sidewall protection spacer. This could also explain the increased etch rate at this point because the corner is expected to be subject to mechanical stress.

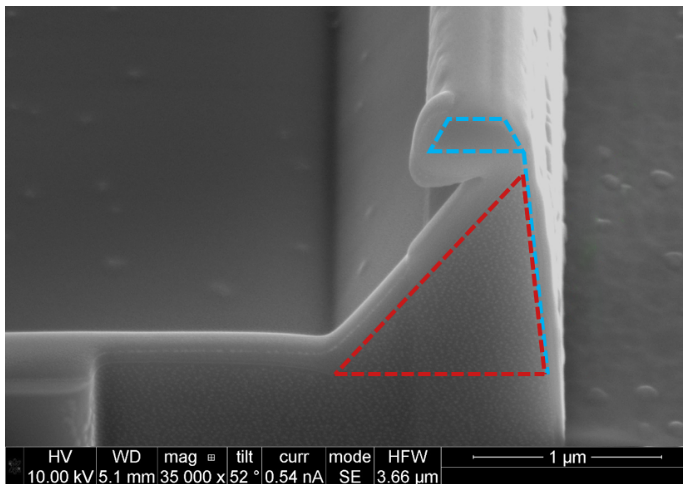


Figure 6.22: SEM photo of 750 nm PC section after 120 s BrMeOH etch, PC geometry outlined in red and the hard mask and sidewall protection in blue.

A second phenomenon that is visible in Fig. 6.21 is that the linear fit extrapolates to a value of around 400 nm under-etch at the start of the process. The reason for this is that the initial [1 1 1] etch plane still needs to be formed at the start of the etch. At that moment, there is already an existing etch depth, which makes this happen significantly faster than the process afterward, when the full crystallographic orientation is

exposed to the BrMeOH etchant. To get optimal control of this specific wet etch step, a change in the working procedure is proposed. In the standard way of working, a wafer is soaked in pure methanol, transferred into the next beaker of pure methanol and then submerged in the 1:1500 diluted BrMeOH etchant. Due to this transfer with a large volume of pure methanol on top of the wafer, the moment the BrMeOH etchant reaches the wafer surface at the intended concentration is uncontrolled. It is therefore recommended to dry the wafer with a N_2 gun briefly, so that the wafer will always be brought immediately into contact with the intended etchant concentration.

It is proposed to investigate if controlling the width of the PC etch area can help to enforce self-limitation of the BrMeOH etch. Fig. 6.23 shows an example where the width of the PC area is chosen in such a way that both sides of the structure come together in a V-shape in the middle, while stopping exactly in the outer corners of the waveguide structure. If the BrMeOH can be self-limiting this way, it becomes very easy to control the behavior of the wet etch, which would improve the reproducibility of the PC geometry and therefore control of the PC conversion performance.

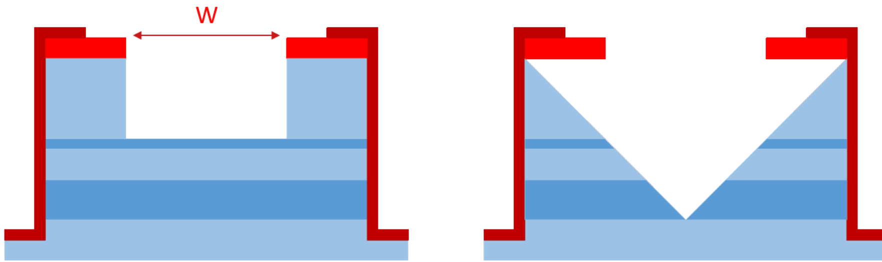


Figure 6.23: Proposed design change to control the size (W) of the PC area (left) to make the BrMeOH etch self-limiting resulting in the V-shape geometry (right).

6.7 Conclusions

A matching procedure was developed for the PAS5500/1100B and PAS2500/40 and was demonstrated for the first time, resulting in overlay errors of less than 250 nm between mask layers. Spot-size converters were fabricated with a combination of these matched lithography tools and measured to achieve coupling efficiency below 1.5 dB/facet. The design parameter combinations for the best manufacturable SSC, still require further investigation.

Polarization converters were fabricated and characterized in an MPW run exhibiting up to 98.9% conversion on single section devices. A process flow improvement was tested to reliably fabricate PC devices with the obtained triangular geometry. It was found that the wet etch to create the slope was not self-limiting. Some further improvements to the working procedure as well as the design were proposed to get a reliable device geometry. It is predicted that with optimized width and length for this geometry, in combination with a double section device concept, above 99% conversion can be achieved with increased tolerance for fabrication errors. It is proposed to

run follow-up experiments on this subject with adjusted designs for the polarization sections.

In this chapter it was demonstrated that it is possible to exploit the overlay capability of a matched scanner and stepper to fabricate devices that were otherwise only possible through the use of EBL. The increased dimensional accuracy and reproducibility of the combination of these tools enables a manufacturing route towards foundry scale volumes of InP PICs with such new building blocks. It is very likely that other design or manufacturing applications can be found to take advantage of the overlay improvement.

Chapter 7

Conclusions and outlook

7.1 Conclusions

The scope of this thesis is to investigate how ArF lithography can be implemented, as a scalable solution for the precision manufacturing of InP-based PICs. Mask layers were identified that can take advantage of such lithography capability, and process steps were developed to transfer the resist patterns into these layers. The imaging capability limits of the scanner around and beyond 100 nm resolution were explored, and solutions were proposed to overcome the encountered challenges. Methods were studied to close the gap between design intent and fabrication result on sub-wavelength InP photonic structures. It was also investigated how the overlay accuracy of scanner and stepper can be exploited to enable next generation PIC building blocks.

The core of this work was enabled by the installation of an ASML PAS5500/1100B scanner and PAS2500/40 stepper in 2011 and 2013 respectively. The research was performed with continuous support from ASML, and in close cooperation with SMART Photonics for implementation of the developed technology into the generic foundry process. The majority of this research was performed in the NWO Applied and Engineering Sciences Projects 12861 and 15367, which were supported by the Dutch Ministry of Economic Affairs.

- Chapter 2 - To perform ArF lithography on 3 inch InP substrates it is necessary to have the required infrastructure and processes. Apart from the exposure tool, resist processing equipment as well as metrology tools are of critical importance. Taking advantage of such infrastructure, can only be achieved by improving the substrate quality of InP wafers. The accuracy of the flat to crystal orientation was improved by an order of magnitude to 350 μrad, in collaboration with InPACT, to enable edge coupling and device separation on InP PICs. Secondly, the overall InP wafer flatness was improved from 10 μm range to below 2 μm range to realize imaging of 200 nm features with below 20 nm CDU. Through further reduction of the total thickness variation (ttv) of InP substrates, even better results can be achieved as was demonstrated on 3-inch ultra-flat silicon wafers.

- Chapter 3 - Three ArF-based patterning modules were independently introduced in the TU/e generic PIC manufacturing process, with minimal changes to the pre-existing process flow. ArF lithography was successfully applied, to establish a coordinate system by exposing markers and the active device layer simultaneously, for planar butt-joint integration. An ArF patterning module for DBR grating definition, was developed and compared, as a scalable alternative to EBL-based patterning of such gratings. Lastly a process module was introduced to perform waveguide definition with high-resolution ArF patterns. An improvement by an order of magnitude in terms of CDU was achieved in comparison to contact lithography, without negative impact on the waveguide propagation losses. Ultra-low excess loss down to 0.15 dB, was demonstrated on fabricated AWGs, enabled by reducing the inter-waveguide gap size to 100 nm.

- Chapter 4 - ArF imaging quality was investigated for the first time for the fabrication of InP DBR grating devices. A method to determine LER on CDSEM images of gratings was developed as a figure of merit for image quality. It was simulated that a concept of double patterning can be used for 240 nm pitch grating fabrication. The lithography process of the LELE double patterning process scheme, was simulated to improve contrast significantly. However, the investigated scheme, does not improve LER of fabricated 200 nm pitch gratings because the NILS at dose to size decreases. Off-axis dipole illumination was investigated as a second method to improve imaging quality. It was simulated that both contrast and NILS increase by up to 60% by the application of this technique. It was found on fabricated 200 nm pitch grating structures that this improved LER by 25%. It was also found that even smaller pitch structures as low as 180 nm, can be manufactured with good imaging quality.

- Chapter 5 - Rule-based OPC was investigated for InP PICs, using a sidewall grating device as a demonstrator, in collaboration with GenISys. Up to 70% improvement in resist pattern fidelity was achieved using simulations to determine optimal OPC parameter combinations. These results were confirmed on fabricated gratings at the resist level. Additional research is required to maintain the pattern fidelity in the subsequent etch steps. Well-defined OPC rules derived from simulations are the way forward to match fabricated device geometries with the design intentions.

- Chapter 6 - The topography challenge of InP PICs was addressed by using high-resolution ArF lithography on the early mask layers and accurately aligned i-line lithography steps at the high-topography processing stages. A method was developed to perform overlay matching between the PAS5500/1100B scanner and PAS2500/40 stepper for InP device layers. Through this result, two building blocks were studied for introduction into the TU/e generic process flow. First, a process flow for fabricating SSCs was demonstrated in a feasibility study, with insertion losses below 1.5 dB on initial device measurements. Secondly, a process was developed to fabricate PCs in the generic process. Devices that were fabricated with this process, were characterized and demonstrated with up to 98.9% polarization conversion efficiency.

7.2 Overall conclusions

The challenges of realizing 100 nm resolution ArF resist patterns on InP substrates were identified and successfully demonstrated to have been overcome. ArF lithography was introduced in three manufacturing layers and independent process modules were developed to transfer the ArF resist patterns into these layers. Arguably more important than the smaller CD that can be printed with this technology, this lithography node enables a hugely improved dimensional control that is required for the current and future InP photonic devices. In contrast to electronics where CD has been the main driver, PICs will benefit more of CDU improvement. The CDU translates into the effective index of waveguides, which in turn translates into accuracy and predictability of manufactured PICs in terms of wavelength, phase and polarization behavior. The advantage of projection lithography in terms of defectivity yield in comparison to contact lithography, should also be considered.

Imaging quality at the resolution limit of the scanner was investigated, and methods to quantify and improve this were proposed and demonstrated. Techniques like OPC combined with calibrated lithography simulations, can help to improve pattern fidelity and pre-compensate for systematic pattern deformation. The overlay of InP device layers is significantly improved by the combination of scanner and stepper lithography. This was demonstrated to enable novel components in the generic platform such as SSCs and PCs.

The application of ArF lithography for InP PIC fabrication, is a highly promising scalable solution for the next generation photonic devices. The implementation of ArF lithography in the generic foundry platform makes this technology accessible to create a wide range of high precision InP photonic devices. In fact, it completes a circle where certain projects are currently working on PICs for sensing applications to improve capability for the lithography tools of the future.

7.3 Outlook

Contrary to what was the case at the start of this project, substrate suppliers are aware that in principle, InP wafer flatness is important for future PIC devices. In recent measurements, it was observed that best effort wafers from various suppliers are getting closer to 1 μm ttv flatness. This is ultimately required to reach very good CDU for photonic structures with CDs down to 100 nm. While it is required to have a continuous improvement effort at this level, it is also necessary to look at the contribution of processing steps such as MOVPE, that can also consume part of the wafer flatness budget.

It is proposed to investigate what kind of accuracy for the geometry of InP PICs is ultimately required. From an application point of view, limits can be placed on effective index tolerances. This translates into manufacturing budgets for layer thickness uniformity and material composition on epitaxy, and CDU budgets in lithography and pattern transfer. Feed-forward algorithms could be used to compensate for material deviations in the lithography dimensions by using dose offsets. Lithography simulations can be used to pre-compensate for the influence of patterns shapes and density

through OPC. As a next step to OPC, it may be interesting to include etch modeling to compensate for local and global pattern density, and aspect ratio dependence of the various process steps.

Imaging of narrow pitch DBR gratings can possibly be further improved. NILS could improve with imaging of lines instead of trenches which would require a more complex LELE integration scheme. Other methods, like OPC features and phase-shift masking could improve the imaging in a direct or double patterning scheme. Lastly, alternative resists could directly improve imaging quality, or could be used for alternative patterning schemes like LFLE and SADP.

It is interesting to further investigate novel components and building blocks that are enabled by the overlay of this manufacturing technology. A feasibility study of two such examples were highlighted in Chapter 6. A project is ongoing, that further investigates the manufacturing and design tolerances for SSCs. A new project was also started to implement photonic integration for fiber sensing which requires polarization handling at a chip level. This will lead to further development of the PC technology and the implementation of improvements that were proposed at the manufacturing level.

The improved overlay could also be exploited to rigorously revise the planarization and metallization stages of the generic manufacturing process. Like in electronics, photonic components could be connected through vias and interconnection metal lines. Primarily, this will need accurate landing of contacts on top of a waveguide which is mostly dependent on alignment and etch selectivity tolerances. When multi-level metallization is desirable, the planarization of the process would need improvement, and it may be required to introduce more accurate etch-back schemes or chemical mechanical polishing processes.

Future research also includes the introduction of ArF lithography as a scalable solution for the nano-photonic platform that is being developed at the TU/e, known as IMOS. This next generation photonic platform has a higher index contrast and smaller dimensions. The manufacturing requirements in terms of CDU and overlay will therefore be significantly higher for this platform. Furthermore, double-sided processing on a bonded membrane is needed in this process. In that sense it will be interesting to look at front to back pattern alignment as well as membrane deformation from the bonding process itself.

Appendix A - DOE principle

Design of experiments (DOE) is a technique that involves the application of statistics to analyze a set of well-defined experiments [130,131]. By choosing the experimental settings in a balanced way, it is possible to pool the output results in specific groups and distinguish the effects of the individual experimental parameters and their interactions. The input and output parameters of such DOE are often referred to as independent and dependent parameters respectively.

Fig. A.1 shows an example where two distributions of a dependent result parameter are compared for a low and high setting of an independent input parameter. The mean effect of this parameter is shown by the dotted line and statistical significance can be determined based on the distributions of both groups of the dependent result. This analysis technique is particularly useful for multi-parameter experiments, but assumes either a linear or 2nd order relation between independent and dependent parameters within the design space. This technique is often used in industry and research to explore and optimize design space and process techniques where many different parameters can be of influence.

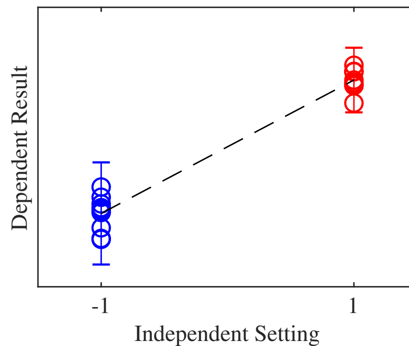


Figure A.1: Distributions for dependent result as a function of independent input parameter.

To obtain all interactions in addition to the main effects, it is necessary to run a full factorial design. This requires 2^n or 3^n experiments, to determine the effects for n parameters for respectively linear or quadratic interactions. A reduced factorial design can significantly reduce the number of required experiments, but in principle always causes aliasing between the dependent parameters, due to which it is impossible to distinguish between certain effects. For experiments where reproducibility is an issue, it can be necessary to run repeat experiments to get a sense of the natural variation of the experiment, and to determine the threshold of statistical relevance more accurately. It is recommended to apply randomization of the experimental order to prevent interaction between the runs and to distinguish drift effects of the experimental environment. When the output of an experiment is a simulation result however, run to run interactions and drift of the experimental environment are not likely and randomization can be omitted.

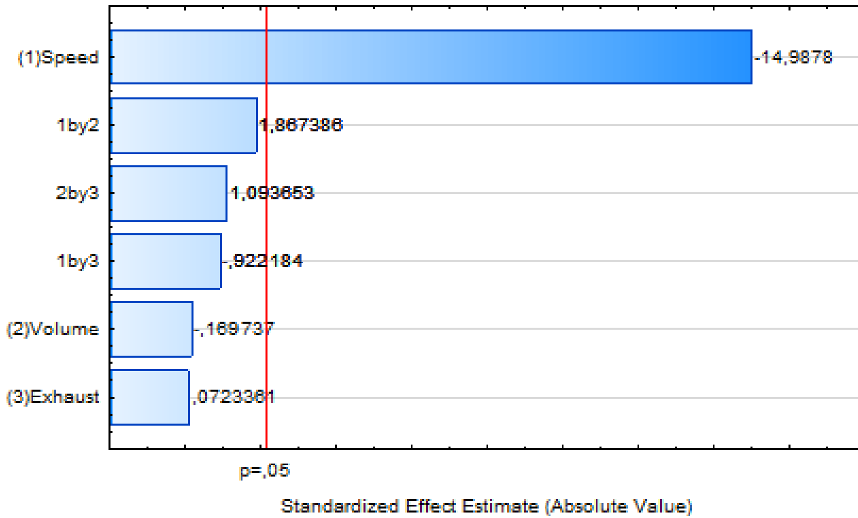
Appendix B - ArF coating DOEs

B.1 BARC recipe characterization

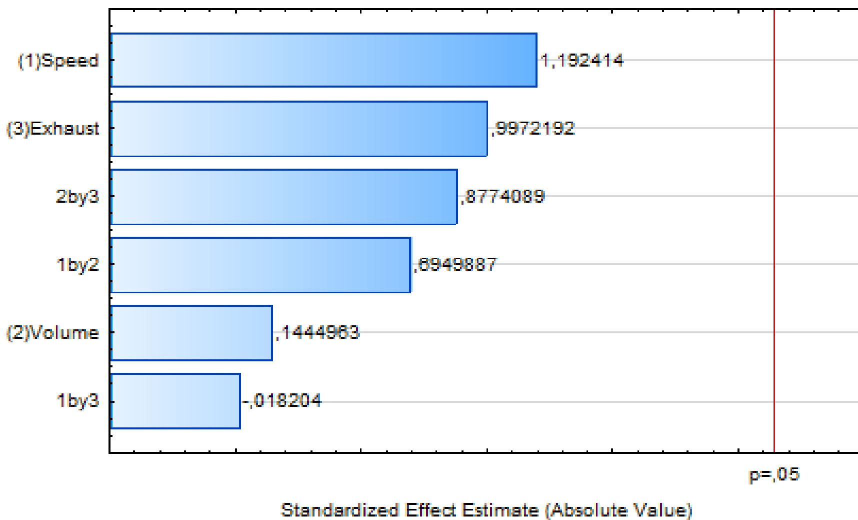
Table B.1 and Table B.2 list the experimental setup and results of the 1st and 2nd BARC DOE. The experimental order was randomized with several CPs to check for non-linearity, repeatability and drift of the experiments. Layer thickness and 3σ uniformity values were collected as output of each experimental run in nm for both DOEs. In the first DOE, spin speed of the coating distribution step was varied, as well as the dispense volume, and the setting of the exhaust valve of the spin bowl. The pareto charts of standardized main and interaction effects are shown in Fig. B.1 with the 5% significance threshold as red line. In the second DOE, the spin speed of the coating dispense step was varied, as well as the hardbake temperature, and the hardbake time. The pareto charts of standardized main and interaction effects are shown in Fig. B.2 with the 5% significance threshold as red line.

Run	Spin speed (RPM)	Volume (ml)	Exhaust (%)	Thickness (nm)	Uniformity (nm)
1(CP)	1750	2	50	39.67	1.14
2	1800	1	75	39.05	1.11
3(CP)	1750	2	50	39.34	1.02
4	1800	3	25	38.54	0.81
5	1700	1	25	39.67	0.69
6	1800	1	25	38.52	1.14
7(CP)	1750	2	50	38.79	0.93
8	1800	3	75	38.63	1.23
9	1700	3	25	39.45	0.6
10	1800	1	75	38.49	0.96
11	1700	1	75	39.65	0.99
12	1700	1	75	39.74	1.02
13	1800	3	75	38.59	1.2
14(CP)	1750	2	50	39	0.75
15	1700	1	25	39.81	1.14
16	1700	3	75	39.7	0.78
17	1800	1	25	38.64	0.99
25	1800	1	25	38.48	0.93
18	1700	3	25	39.5	1.11
19	1800	3	25	38.72	1.11
20(CP)	1750	2	50	38.9	0.78
21	1700	3	75	39.63	1.14
22(CP)	1750	2	50	38.93	0.96

Table B.1: BARC DOE 1 experimental setup and measurement results.



(a) Pareto for 1C5D layer thickness

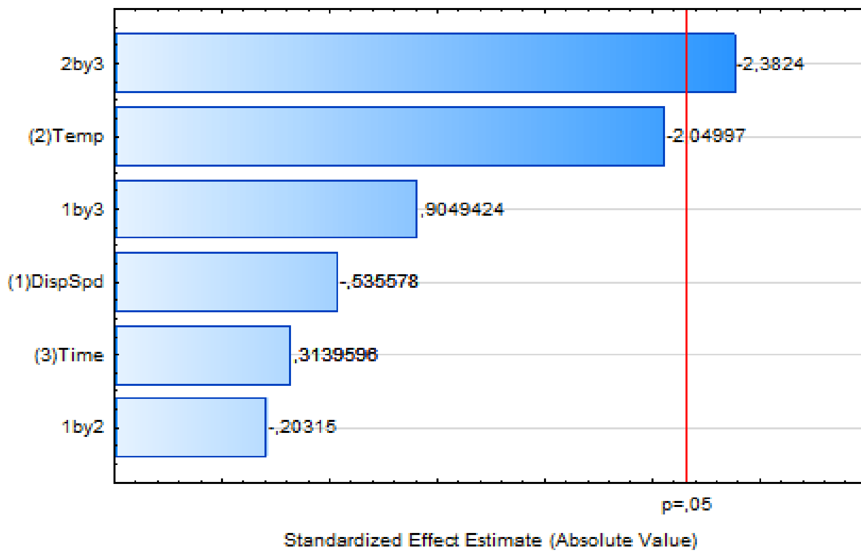


(b) Pareto for 1C5D 3σ uniformity

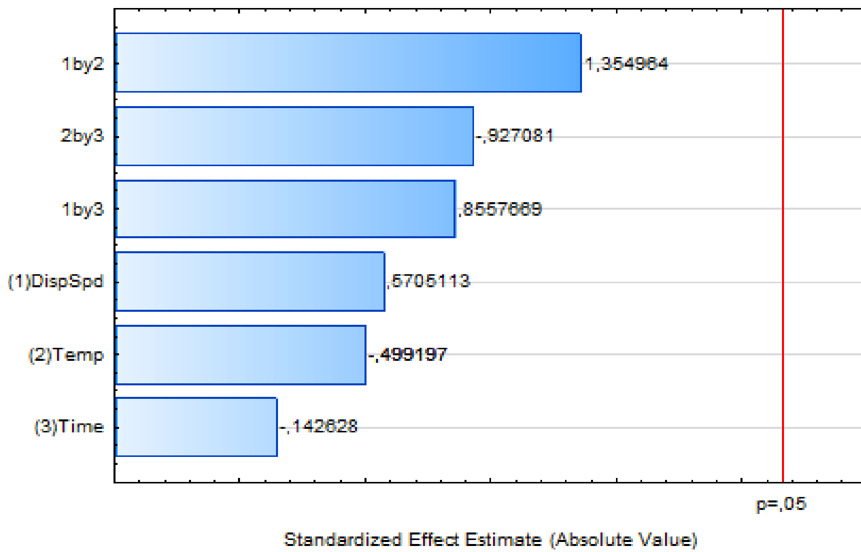
Figure B.1: 1C5D DOE 1 pareto charts of standardized main and interaction effects of spin-speed (1), dispense volume (2), and exhaust (3) and 5% significance threshold as red line.

Run	Spin speed (RPM)	Temperature (°C)	Time (sec)	Thickness (nm)	Uniformity (nm)
1(CP)	1000	200	90	38.35	0.9
2	500	195	120	38.24	0.96
3(CP)	1000	200	90	38.12	0.9
4	1500	205	120	37.91	0.96
5	1500	205	60	38.05	0.99
6	500	205	60	38.01	0.84
7	500	205	120	37.93	0.66
8	500	195	60	38.18	1.2
9	500	195	60	38.26	1.11
10(CP)	1000	200	90	38.27	1.5
11	1500	195	60	38.01	0.72
12	1500	205	60	38.24	1.35
13	500	205	60	38.37	0.93
14	1500	195	120	38.51	1.23
15	1500	195	120	38.25	1.08
16	1500	195	60	38.13	0.9
17(CP)	1000	200	90	38.16	0.9
18	1500	205	120	38.09	0.99
19	500	205	120	38.18	1.05
20	500	195	120	38.31	0.99

Table B.2: BARC DOE 2 experimental setup and measurement results.



(a) Pareto for 1C5D layer thickness



(b) Pareto for 1C5D 3σ uniformity

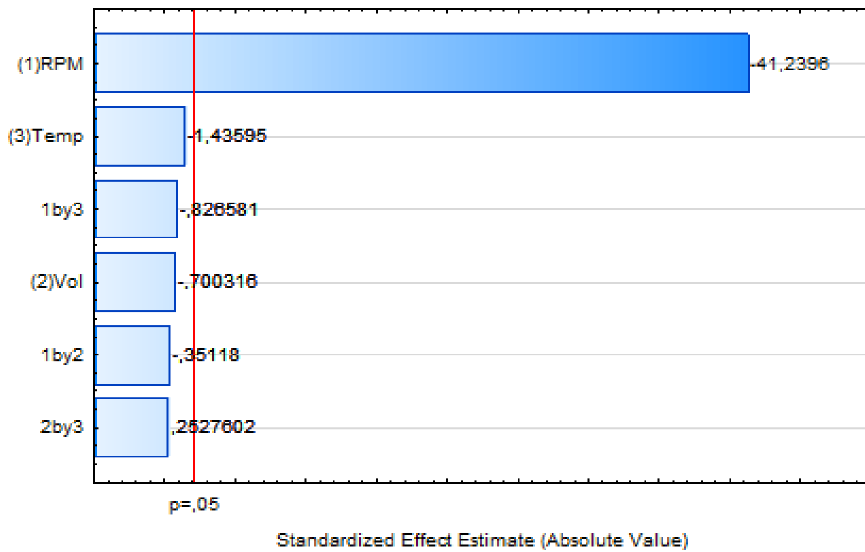
Figure B.2: 1C5D DOE 2 pareto charts of standardized main and interaction effects of dispense speed (1), hardbake temperature (2), and hardbake time (3) and 5% significance threshold as red line.

B.2 Resist recipe characterization

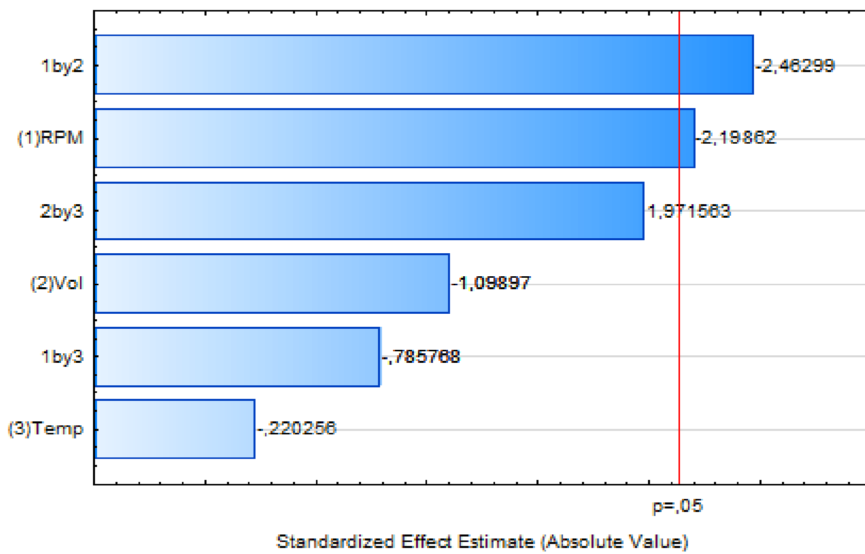
The following table lists the experimental setup and results of the PR DOE. The experimental order was randomized with several CPs to check for non-linearity, repeatability and drift of the experiments. Layer thickness and 3σ uniformity values were collected as output of each experimental run in nm for both DOEs. In this DOE, spin-speed of the coating distribution step was varied, as well as the dispense volume, and the softbake temperature. The pareto charts of standardized main and interaction effects are shown in Fig. B.3b with the 5% significance threshold as red line.

Run	Spin speed (RPM)	Volume (ml)	Temperature °C	Thickness (nm)	Uniformity (nm)
1(CP)	800	4	125	221.66	2.19
2	700	3	130	237.37	1.94
3(CP)	800	4	125	222.65	2.19
4	900	3	120	210.49	2.39
5	900	3	120	211.04	2.95
6	900	5	120	209.91	1.96
7(CP)	800	4	125	222.49	2.29
8	700	5	130	238.74	3.78
9	900	5	130	208.67	1.8
10	900	5	130	208.41	1.59
11	900	3	130	208.64	1.99
12(CP)	800	4	125	222.3	2.34
13	700	5	120	238.35	2.59
14	700	5	120	236.21	2.04
15	900	5	120	209.74	1.53
16	700	3	120	237.55	2.56
17	700	3	120	237.68	2.85
18(CP)	800	4	125	220.45	2.56
19(CP)	800	4	125	220.46	1.42
20	700	3	130	236.84	2.35
21	900	3	130	209.38	2.59
22	700	5	130	235.21	2.45

Table B.3: PR DOE experimental setup and measurement results.



(a) Pareto for P6111 layer thickness



(b) Pareto for P6111 3σ uniformity

Figure B.3: P6111 DOE pareto charts of standardized main and interaction effects of spin-speed (1), dispense volume (2), and softbake temperature (3) and 5% significance threshold as red line.

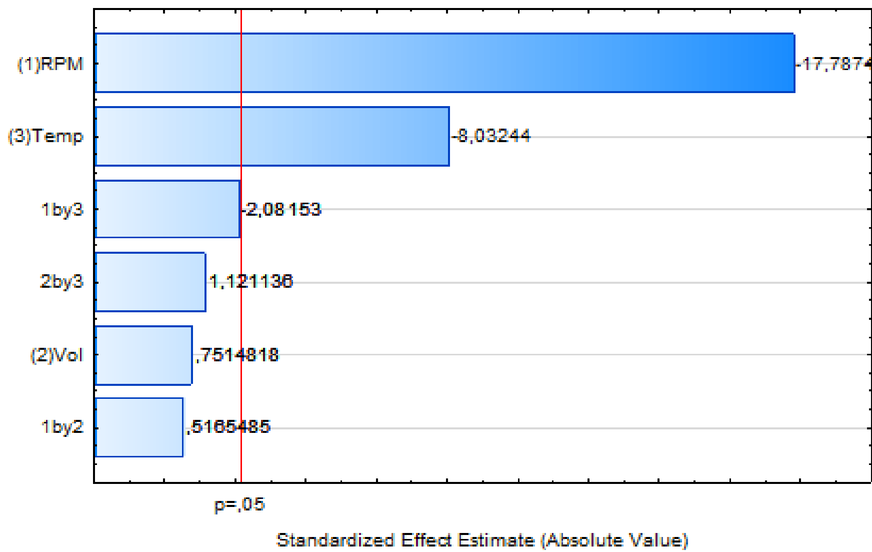
B.3 TARC recipe characterization

The following table lists the experimental setup and results of the TARC DOE. The experimental order was randomized with several CPs to check for non-linearity, repeatability and drift of the experiments. Layer thickness and 3σ uniformity values were collected as output of each experimental run in nm for both DOEs. In this DOE, spin speed of the coating distribution step was varied, as well as the dispense volume, and the softbake temperature. The pareto charts of standardized main and interaction effects are shown in Fig. B.4b with the 5% significance threshold as red line.

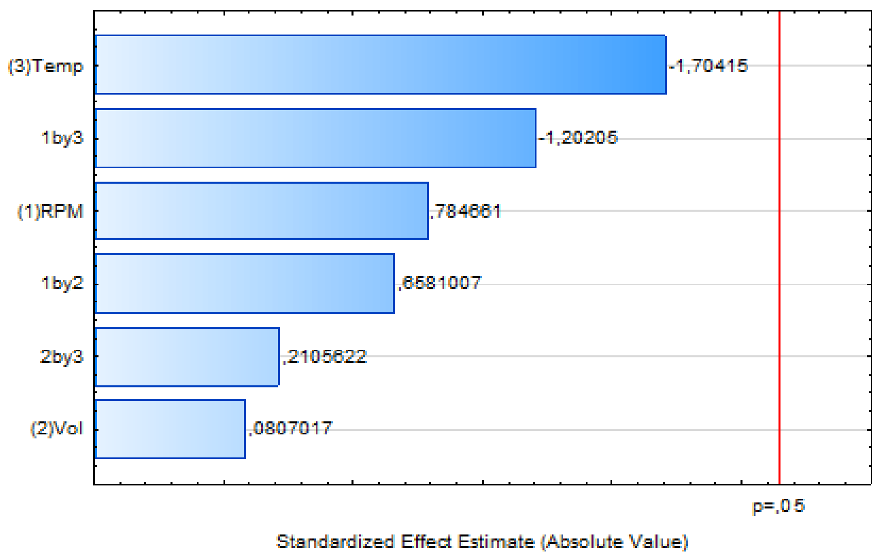
Run	Spin speed (RPM)	Volume (ml)	Temperature °C	Thickness (nm)	Uniformity (nm)
1(CP)	1550	4	90	89.91	1.09
2	1500	3	95	90.82	1.07
3	1600	3	85	89.48	1.14
4	1600	5	85	88.98	1
5	1600	5	85	89.11	1.24
6	1500	5	85	91.54	0.94
7(CP)	1550	4	90	89.77	0.98
8	1500	5	95	90.75	0.96
9	1600	5	95	87.87	1.02
10	1500	5	95	90.47	0.99
11	1600	3	95	87.75	1.02
12(CP)	1550	4	90	89.8	1.12
13(CP)	1550	4	90	89.7	0.93
14	1600	5	95	87.79	0.89
15	1500	3	95	90.26	0.85
16	1600	3	95	86.92	0.86
17(CP)	1550	4	90	89.26	1.02
18	1600	3	85	88.84	1
19	1500	5	85	* -	* -
20	1500	3	85	91.64	0.93
21	1500	3	85	91.3	1.13
22(CP)	1550	4	90	89.75	1.01

* - Result not included due to wafer problem

Table B.4: TARC DOE experimental setup and measurement results.



(a) Pareto for TCX041 layer thickness



(b) Pareto for TCX041 3σ uniformity

Figure B.4: TCX041 DOE pareto charts of standardized main and interaction effects of spin-speed (1), dispense volume (2), and softbake temperature (3) and 5% significance threshold as red line.

Appendix C - FEM principle

A focus energy matrix (FEM) is a typical stepper and scanner lithography wafer level analysis method that is used to find optimal exposure settings of a certain feature, or to characterize the process window of the exposure. In a FEM, the image of this feature is exposed on a wafer in a 2-dimensional array where the focus and energy of each exposure is deliberately varied in the orthogonal directions. This is illustrated by Fig C.1 where 9 focus and energy variations were exposed of a photonic crystal hole pattern. In this example can be seen that the crystal holes become larger with increasing dose from left to right while positive and negative focus offset seems to cause smaller holes until they stop resolving.

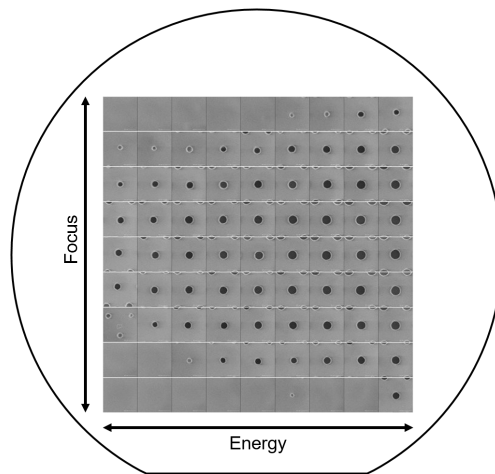


Figure C.1: Example of 9x9 FEM of photonic crystal holes with CDSEM results.

Appendix D - OPC regression model effects

The following table is the detailed list of standardized effect values, p-values and exact regression coefficients of the linear (L) and quadratic (Q) (interaction) effects from the OPC DOE. The parameters that were included in this experiment, are described in Table 5.2. This table lists the effects that were included in the regression model for OPC, because of statistical relevance or because they are main effects of which the interactions were concluded to be statistically relevant.

Linear/Quadratic (Interaction) Name	Standardized Effect	zero-hypothesis p-value	Regression Coefficient
Mean	106.57	0	0.0422
3L by 5L	29.88	0	0.0177
5Q	-20.53	0	-0.0086
4L by 5L	-14.05	0	-0.0083
3L	13.71	0	0.0066
1L by 5L	13.53	0	0.008
4L	10.87	0	0.0053
3L by 5Q	-10.59	0	-0.0054
2L by 5L	-9.53	0	-0.0057
3Q	-8.22	0	-0.0034
1L by 3L	8.06	0	0.0048
3Q by 5L	-7.07	0	-0.0036
2L	5.58	0	0.0027
2L by 3L	-5.22	0	-0.0031
1L by 2L	-5.1	0	-0.003
1L by 4L	-3.88	0	-0.0023
4L by 5Q	-3.8	0	-0.002
2L by 4L	3.14	0.002	0.0019
3L by 4L	-2.66	0.008	-0.0016
4Q by 5Q	-2.62	0.009	-0.0012
3L by 4Q	2.39	0.018	0.0012
1L	-2.35	0.019	-0.0011
4Q	-2.06	0.04	-0.0009
1Q	-1.7	0.09	-0.0007
2Q	-1.54	0.124	-0.0006
5L	0.66	0.507	0.0003

Table D.1: List of included effects in regression model separated at 5% significance level.

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Acknowledgments

The following text can be seen as the most popular part of any thesis, since it can be read and understood by anyone, even without any technical background. It was written in strange times where the entire world is fighting the ominous threat of an invisible opponent. Despite of this, I've decided to keep focus on bringing this journey to an end. The following paragraphs should be taken lightheartedly: no offense was intended in the writing of any of the text and no claims can be made with regards to the order of the naming. So here goes...

First and foremost, none of this would have been possible without the love and support from my family. In particular the past few years have not been the easiest in terms of physical presence at home and sometimes in state of mind. Mieke and Mitch deserve this credit, but also both our parents that have stepped up in times of need. Actually, I need to thank my parents for enabling me to go to college in the first place, despite the fact that I chose a technical profession instead of "dobbelen".

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I will now start an apology for the people I may have forgotten in this section, that may have (un)intentionally contributed to this work, even if it was only through the work atmosphere. There are too many things right now that make my head overflow so please excuse me, "I'm sorry and thank you as well".

Jeroen Bolk
Eindhoven, April, 2020

Curriculum Vitae

Jeroen Bolk was born on July 17th 1976 in Boxtel the Netherlands. He received the Engineers degree at higher vocational education level in chemical laboratory techniques with Fontys Hogescholen Eindhoven, in 1999.

He then started his technical career with Philips Research at the "NatLab" in Eindhoven, followed by Philips Semiconductors that later became NXP semiconductors in Nijmegen. During this period, he gathered almost a decade of semiconductor processing experience on various wafer diameters, in a research, development, and production environment, eventually reaching a level of senior process engineer.

In 2009, he joined the faculty of electrical engineering at the Eindhoven university of technology, as a technical staff member of the opto-electronic devices (OED) research group headed by prof. M. Smit. In this role, Jeroen focused on the process technology development for InP based photonic integrated circuits, contributing to many research projects. As a member of both PhI and NanoLab@TU/e departments, he facilitated the installation and adaptation of the world's first ArF scanner to expose 3-inch InP substrates.

In the following years, Jeroen contributed significantly to the development of the ArF related processing as a technical staff member. He was offered a PhD position in a NWO project by prof. K. Williams of the PhI group in 2017. The work that was performed in both these roles, is for a large part described in this thesis: ArF Scanner Lithography for InP Photonic Integrated Circuit Fabrication

List of Publications

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