Circuit design for low-cost smart sensing applications based on printed flexible electronics

Citation for published version (APA):
Fattori, M. (2019). *Circuit design for low-cost smart sensing applications based on printed flexible electronics*. [Phd Thesis 1 (Research TU/e / Graduation TU/e), Electrical Engineering]. Technische Universiteit Eindhoven.

Document status and date:
Published: 29/11/2019

Document Version:
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy
If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Download date: 08. Feb. 2024

Circuit Design for Low-Cost Smart Sensing Applications Based on Printed Flexible Electronics

Marco Fattori

This work was funded in the frame of the European project ATLASS (Horizon 2020, Nanotechnologies, Advanced Material and Production theme, grant agreement n°636130).

Cover designed by Marco Fattori.

Marco Fattori

Circuit Design for Low-Cost Smart Sensing Applications Based on Printed Flexible Electronics

Eindhoven University of Technology

A catalogue record is available from the Eindhoven University of Technology Library

ISBN: 978-90-386-4927-6

Circuit Design for Low-Cost Smart Sensing Applications Based on Printed Flexible Electronics

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische
Universiteit Eindhoven, op gezag van de rector magnificus
prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door
het College voor Promoties, in het openbaar te verdedigen op
vrijdag 29 november 2019 om 11:00 uur

door

Marco Fattori

geboren te Rieti, Italië

Dit proefschrift is goedgekeurd door de promotoren en de samenstelling van de promotiecommissie is als volgt:

voorzitter: prof.dr. E. Lomonova
1e promotor: prof.dr. E. Cantatore
2e promotor: dr.ir. P. J. A. Harpe
leden: prof.dr. J. Genoe (KU Leuven)
prof.dr. G. H. Gelinck
dr.ir. M. Pertijs (Technische Universiteit Delft)
adviseur(s): dr. M. Charbonneau (CEA-Liten)

Het onderzoek of ontwerp dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

To my parents

“Chi più in alto sale, più lontano vede.
Chi più lontano vede, più a lungo sogna”

Walter Bonatti

Table of Contents

List of figures

List of tables

List of abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AMO	Amorphous Metal-Oxide
AMS	Analog-Mixed-Signal
ASDM	Asynchronous Sigma-Delta Modulator
ASK	Amplitude-Shift Keying
ATLASS	Advanced high-resolution printing of organic Transistors for Large Area Smart Surfaces
a-Si	Amorphous-Silicon
BBPLL	Bang Bang Phase Locked Loop
BTI	Bootstrap Inverter
CAD	Computer Aided Design
CCD	Charge-Coupled Device
CLM	Channel Length Modulation
CMOS	Complementary Metal-Oxide Semiconductor
CSA	Charge Sensitive Amplifier
DC	Direct current
DCI	Diode-Connected Inverter
DCILS	Diode-Connected Inverter with level Shifter
DIBL	Drain-Induced Barrier Lowering
DOS	Density Of States
DR	Dynamic Range
DRC	Design Rule Checking
DRM	Design Rule Manual
DyC	Dynamic Cell
EDA	Electronic Design Automation
EDP	Energy-Delay Product
FCO	Feedback Controlled Oscillator
FE	Flexible Electronics
FoM	Figure-of-Merit
HF	High-Frequency
HOMO	Highest Unoccupied Molecular Orbital energy
IC	Integrated Circuit
IoT	Internet of Things
INL	Integral-Non-Linearity
LCD	Liquid-Crystal Display
LF	Low-Frequency
LFN	Low-Frequency Noise
LPE	Layout Parasitic Extraction
LSB	Least Significant Bit

LVS	Layout Versus Schematic
MM	More Moore
MIM	Metal-Insulator-Metal
MSIM	Metal-Semiconductor-Insulator-Metal
MISM	Metal-Insulator- Semiconductor-Metal
MtM	More than Moore
NTC	Negative Temperature Coefficient
ODL	Organic Dielectric
OLED	Organic Light Emitting Diode
OSR	OverSampling Ratio
OSC	Organic Semiconductor
OTFT	Organic Thin-Film Transistor
PCB	Printed Circuit Board
PCI	Pseudo-CMOS Inverter
PDK	Process Design Kit
PDMS	Polydimethylsiloxane
PCell	Parametrized Cell
PE	Printed Electronics
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate)
PEN	Polyethylene Naphthalene
PET	Polyethylene Terephthalate
PGC	Pass-Gate Cell
PSS	Polystyrene Sulfonate
PTC	Positive Temperature Coefficient
PVT	Process-Voltage-Temperature
PWM	Pulse Width Modulation
poly-Si	Poly-Silicon
RF	Radio-Frequency
RFID	Radio-Frequency Identification
RTD	Resistance Temperature Detector
R2R	Roll-to-Roll
SCC	Scan Circuit Cell
SCO	Sensor Controlled Oscillator
SNDR	Signal-to-Noise-Distortion-Ratio
SNR	Signal-to-Noise-Ratio
SQNR	Signal-to-Quantization Noise-Ratio
SoC	System-on-Chip
SiP	System-in-Package
S2S	Sheet-to-Sheet
S/D	Source/Drain
TC	Temperature Coefficient
TDM	Time-Division Multiplexing
TEM	Transistor Evaluation Module
TFT	Thin-Film Transistor
TIA	Trans-Impedance Amplifier
TLM	Transmission Line Model

VCO	Voltage-Controlled Oscillator
VRH	Variable Range Hopping
WORM	Write-Once-Read-Many
ZVI	Zero-V_{GS} Inverter

1. Introduction

1.1 Evolution of electronics: the role of flexible electronics

In the early 1960s, the concept of an integrated circuit (IC) was hardly considered an alternative to the use of discrete components. Indeed, integrated transistors were still unreliable, featuring low yield, while the cost of integrated circuits was significantly higher than stand-alone components. In 1961, Fairchild Semiconductor produced the first silicon integrated circuit containing only 4 transistors. By 1965, the same company was about to release a new chip integrating 64 components. In this context, Gordon Moore, director of research and development at Fairchild, formulated his most-known law [1]. He pointed out that maximizing the number of components which can be physically integrated in a chip is not always economically convenient. However, adding more and more components in a chip will generally lead to a lower cost per component. This trend remains valid until in the attempt of further increasing the integration density, at some point the probability of killer defects will raise. This will lower the technology yield and thus increase the costs. The optimal point is instead reached when the number of components integrated in a chip leads to the minimum cost per device. Under this assumption, Moore predicted that the number of components (resistors, capacitors, diodes and transistors) integrated in a single chip would double every year [1].

This prediction turned out to be quite accurate for several years. Indeed, 10 years later in 1975 the charge-coupled device (CCD) memory chips under development at Intel (company cofounded by Moore) could count some 32000 components, thus only a factor 2 off from the prediction [2]. In the same year, Moore revised downward his prediction correcting it to a biannual doubling of component count per chip [2]. He further identified three factors responsible for the new electronic integration trend: the decrease of the components size, the increase of the chip area and the so called device cleverness.

For years the downscaling of the component size has allowed to increase chip density, producing faster and less power hungry transistors. Indeed, according to Dennard's scaling rules [3], by reducing the device dimensions a factor $\lambda(>1)$, the voltage, current, capacitance and delay time of the transistor would reduce by $1/\lambda$, if the doping concentration increases by λ. As direct consequence, the number of devices which can be placed in the same area increase by λ^2 maintaining a constant power consumption per unit area between different generations of transistor technologies.

In other words, each new integrated transistor technology is better than the previous one, providing higher performance at lower cost per transistor. According to Mack [4], this approach has for decades sustained Moore's law. Initially, the progress in semiconductor technology led towards circuit up-scaling, producing larger and more complex chips (Moore's law 1.0) [4].

Instead, in the later decades, the technological push was mainly focused on downscaling, to achieve reduction of transistor size and cost even though the circuit complexity had stopped to scale up as fast as manufacturing technology would permit (Moore’s law 2.0) [4]. As a result, current manufacturing processes permit to economically integrate more than 10 billion transistors on a chip, even though this is not exploited in most of the applications in the market.

Since the early 2000s, the transistor sizes shrunk below 100 nm and Dennard’s scaling rules started to approach the limit. Manufacturing smaller transistors does not always make them faster and more efficient. Indeed, the reduction of the transistor voltage has become more difficult due to the rise of the device leakage currents. Thus, for the last decade Moore’s law for the Silicon manufacturing industry has been more about the costs than performance. However, difficulties in further downscaling the transistor feature sizes have led the cost per unit area of finished silicon to rise with about 10% per year [4]. On the other hand, the cost per transistor reduced by about 25% over the same time frame [4]. If the manufacturing costs will rise faster than the transistor area will decrease, the next generation of transistors will be more expensive than the last one.

This is to say that Moore’s law is effectively slowing down. In this scenario the prospective of microelectronics is uncertain. On one side, the research is projected towards ever-higher integration density, sustaining the historical scaling of CMOS technology. This trend has been denominated as “More Moore” (MM) [5]. On the other hand, the so called “More than Moore (MtM)” research development [5], aims to integrate in a system functional diversification based on the simultaneous use of heterogeneous technologies, that do not scale in accordance with Moore’s law (Figure 1). Thus, the progress of electronics will be defined by new forms of integration, which will allow to lower the cost of the whole system.

Future applications will require logic and non-logic functionalities such as RF communication, power control, passive components, sensors and actuators which could be added to the system in an economically efficient way by means of heterogeneous technologies. Mack [4], uses the name Moore’s Law 3.0 for a category of the MtM concept where the trend is to integrate capabilities such as sensors and actuators on chip, in order to take advantage of the low-cost, mass-production approaches common to silicon manufacturing. However, this is not the only possible form of functional diversification.

Future system architectures will make use of both Systems-on-Chip (SoCs) and Systems-in-Package (SiPs). The first will be mostly dedicated to data processing, while the interactions with the user and the environment will be mostly tackled with SiP methods. This approach is expected to enable the development of higher value systems, capable of providing both computing and interacting functionalities. However, the challenges here lie in the heterogeneous integration of logic and non-logic functions within the same system. Besides, the interconnection of the different components needs to guarantee the electrical connectivity and mechanical integrity of the system, and to ensure a reliable interface with the physical environment.

In this scenario, flexible electronics (FE) provides an attractive cluster of emerging (organic and inorganic) technologies to develop low-cost SiPs. Indeed, FE enables the

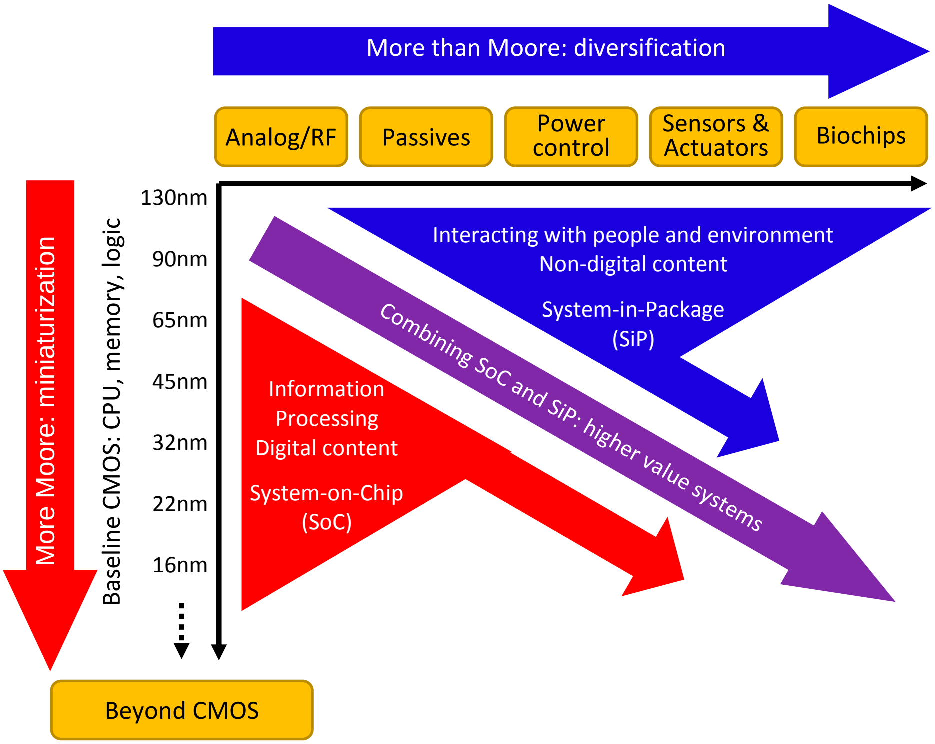


Figure 1. Future prospects of microelectronics. From "More Moore" to "More than Moore". Roadmap extracted from the International Technology Roadmap for Semiconductors 2011 [5].

production of Thin-Film Transistors (TFTs) on mechanically flexible substrates due to the low temperature budget (<200°C) required throughout the manufacturing process. Foil-based systems offer a suitable platform to combine non-logic functions, providing the capability of manufacturing ultra-thin components, at low-cost even on a large-area. The intrinsic flexible nature of FE could be further engineered to meet the mechanical requirements of bendability, foldability, stretchability and even conformability to suit a variety of market applications.

In the future, flexible electronics based on organic materials will enable for example the fabrication of flexible large-area photovoltaic cells that will replace the conventional expensive silicon-based solar panels. The mechanical flexibility will enable the solar cells to be embedded in curtains or laminated on window panes, improving energy harvesting capabilities in domestic environments and smart buildings. In the last decades, the potential of organic materials has been largely investigated. A remarkable example is the Organic Light-Emitting Polymer (OLED) discovered in the early 1990s and today heavily used in smartphone displays and TVs. OLED displays in contrast with the traditional Liquid Crystal Displays (LCDs) do not require a back light, reducing thickness and improving packaging and visual experience. OLEDs can be produced on flexible substrates and this will enable the production of electronic devices with unprecedented mechanical properties, from foldable phone displays (demonstrated for the first time in commercial products in early 2019) to roll-up TVs at longer term. Looking beyond our personal entertainment devices, the potential of flexible electronics could play an important role in human-machine interaction. Electronic skins could be developed exploiting the intrinsic flexibility and strechtability of the flexible electronics, while the use of new materials could further extend the skin sensing capabilities to e.g. temperature and infrared radiation (IR) sensing.

These are just a few examples of future possible applications of flexible electronics. It should be underlined that the aim of flexible electronics is not to provide a valid alternative to mainstream silicon technologies, but rather to address problems not solvable by silicon CMOS and a pure Moore's law approach. Flexible electronics will focus on applications where large active area is of great importance, or where mechanical flexibility and light weight are essential.

1.1.1 Flexible electronic technologies: state-of-the-art

Flexible electronics technologies, which will enable the applications mentioned in the previous section, can be divided in two categories: inorganic and organic, according to the nature of the semiconductor material exploited. Among the inorganic materials relevant to flexible electronics should be mentioned: amorphous silicon (a-Si), polycrystalline silicon (poly-Si) and amorphous metal-oxide (AMO) semiconductors (such as Indium-Gallium-Zinc Oxide, Zinc Oxide etc..) [6].

Amorphous Silicon TFTs have been successfully employed in applications such as displays and photovoltaics. Indeed, the relatively low processing temperature (< 350 °C) allows the use of several types of substrates, including plastic foils. However, a-Si transistors suffers from low carrier mobility ($\mu < 1$ cm^2/Vs) and bias-stress instability, making it unsuitable for applications demanding continuous operation at large currents [7]. In addition, a-Si technologies are generally unipolar, since the hole mobility is significantly lower, ranging in the order of 10^{-3} cm^2/Vs. Conversely, poly-Si transistors exhibit much higher carrier mobility ($\mu \sim$ 50-100 cm^2/Vs), achieved at the expenses of a much higher processing temperature (< 500 °C) which, for flexible electronics, requires the use of stainless steel substrates [8]. Low temperature poly-Si technologies which enable the use of plastic substrates have been also demonstrated [9].

Amorphous metal-oxide TFTs exhibit overall superior performance compared to other FE technologies. These devices are characterised by high electron carrier mobility (μ >60 cm^2/Vs) [10] and operational stability, achieved with a low thermal budget (typically < 250°C). In terms of speed performance, transistors achieving unity gain frequencies beyond tens of MHz have been already demonstrated [11]. However, AMO technologies are typically unipolar, since these excellent properties manifest in n-type transistors only.

Organic Thin-Film Transistors (OTFT) generally exhibit inferior performance with respect to their inorganic counterpart. However, recent advances in materials have allowed to surpass a-Si technologies. Indeed, carrier mobility values of the most recently synthesised organic semiconductors are in the range of 1 - 10 cm^2/Vs, with relevant improvements in terms of stability [12]. Despite mature organic technologies typically comprise p-type transistors only, complementary organic technologies have been also reported in literature [13][14][15][16][17]. However, the inferior performance of the n-type transistor, together with the more complex fabrication process and the lower device yield of complementary organic TFT technologies have limited their use until now. One of the major capabilities of organic technologies is the possibility of manufacturing electronics with processing temperatures lower than 100°C, enabling the use of very cheap plastic substrates such as polyethylene terephthalate (PET). Furthermore, as the OTFTs are made from organic compounds, they are extremely resilient to bending, and are also sensitive to biological and chemical agents, features that can be exploited e.g. to produce biochemical sensors [18][19].

Finally, organic and AMO TFTs show significantly higher flexibility compared to a-Si and poly-Si technologies [20]. Indeed, under strain, their relative change in carrier mobility is well below that of Si-based TFTs, and the maximum bearable strain is nearly an order of magnitude higher than the benchmarked technologies.

Given the above-mentioned features we can conclude that organic and AMO technologies represent the best two material platforms for the development of large-area and low-cost systems on foil.

1.1.2 Role of printed organic technologies

Another important aspect for large-area technologies is the possibility (or not) to enable solution-based manufacturing. Solution-based fabrication methods involve the dissolution of the electronic functional materials in suitable solvents, to create inks which can be selectively deposited on a substrate by means of printing techniques to create TFTs and other active device structures. Printing can be a high-throughput technique and thus can tremendously contribute to lowering the cost of flexible electronics. Printing can be carried out at atmospheric pressure and at room temperature. Additional annealing or curing steps at moderate temperature are usually required after deposition, to drive off the residual solvents or to activate the reactions, leading to the desired electronic materials. Organic, Si and AMO technologies based on printing processes have been already demonstrated [21][22][23][24][25]. However, amorphous metal oxide and Si transistors are typically inkjet-printed [21], whereas OTFTs can be produced even exploiting mass-production processes directly derived from the graphic art printing industry, such as screen-printing, offset-printing or gravure printing [22][23][24].

In general, printing processes can also be classified according to the substrate they exploit in Sheet-to-Sheet (S2S) and Roll-to-Roll (R2R) categories. The former are based on substrate sheets that are processed in batches, while the latter employs rolls that are continuously processed. S2S processes usually guarantee a better control over the fabrication parameters, at the expenses of higher overall production time and thus a lower throughput. On the other hand, R2R platforms enable continuous production, which lead to a further cost reduction based on economy of scale.

The availability of organic materials compatible with high-throughput printing processes, makes printed organic electronics a suitable candidate to potentially reduce the costs of large-area electronics, enabling single-use applications. These process platforms are expected to enable mass production of inexpensive smart Radio-Frequency Identification (RFID) tags, large-area sensing surfaces, and wearables, to give just a few examples.

1.1.3 Organic circuits: state-of-the-art

In the last decades, electronic circuits manufactured with organic materials, have been largely reported in literature. Basic analog and digital circuit blocks such as amplifiers [26][27][28][29][30], comparators [31][32][33][35], logic gates and flip flops [34][35][36] have been proposed at first, and further exploited for the development of more complex systems. Signal conditioning interfaces for sensor matrix applications [37][38], RFID tags

[39][40][41][42][43], display drivers [44][45][46][47] and a microprocessor [48] capable of executing up to 40 instructions/s, are just a few examples.

For what concerns mixed-signal systems, several data converters based on OTFTs have been also demonstrated. A Delta-Sigma architecture has been exploited in [28] to develop an Analog to Digital Converter (ADC) achieving a Signal-to-Noise-and-Distortion-Ratio (SDNR) of 24.5 dB in a bandwidth of 15.6 Hz. An ADC based on a Voltage Controlled Oscillator (VCO), achieving 6-bit resolution and 1 LSB Integral-Non-Linearity (INL), has been demonstrated in [49]. A Successive-Approximation-Register (SAR) ADC has been designed in [50] using a low-voltage complementary organic technology. The converter achieves 6 bit resolution and a maximum INL of 0.6 LSB, with a sampling frequency of 10 Hz.

The state-of-the-art presented above is related only to organic technologies fabricated with photolithography processes. These platforms allow the production of flexible circuits achieving complexities as high as ∼13000 TFTs [46]. Organic transistors processed from solutions exhibit lower yield and even larger parameter variations than their photolithographic counterparts. As a consequence, the complexity of printed circuits currently reported in literature does not exceed ∼200 OTFTs. Therefore, it is not surprising that state-of-the-art printed circuits are mainly limited to analog and digital blocks featuring basic functionalities [51][52][53][54]. Remarkable results have been reached in [55], with a counting ADC based on a resistive Digital-to-Analog-Converter (DAC), featuring 4 bit resolution and 0.42 LSB INL with a total transistor count of 158 devices. To the best of our knowledge, only few complete systems realized with fully printed organic transistors are reported in literature. An RFID tag developed using a combination of inkjet and gravure printing techniques has been proposed in [56]. A temperature threshold sensor tag has been demonstrated in [57]. This circuit is capable to detect when the environmental temperature exceeds a given set point, and stores this in a non-volatile memory. In this architecture, the logic blocks are developed with complementary TFTs, produced with inkjet, spin coating and laser ablation techniques. A printed passive reader-talks-first RFID tag based on silent tag communication protocol has been developed in [58] with a complementary printed organic technology. The tag is wirelessly powered by energy harvesting the 13.56 MHz carrier signal generated by the reader, and further provided with an envelope detector and a code recognition unit. The latter is used to verify the matching of the received demodulated data with the identity of the tag and send, via RF link, a response signal to the reader by means of load modulation technique.

1.1.4 Printed organic circuits: design challenges

While extremely attractive from an economical manufacturing point of view, printed electronics is not free of challenges. The low-temperature process, enabler of the mechanical flexibility, is also responsible for a low level of control of the printed material properties. This, together with the intrinsic structural disorder or organic semiconductors, which is typically exacerbated by solution-based processing, leads to the fabrication of printed OTFTs with typically lower performance compared to processes based on vacuum deposition.

Indeed, at the state of the art, printed organic transistors present mobility values typically in the order of $\mu \sim 1\ \mathrm{cm}^2/\mathrm{Vs}$ [15][59][60][61][62], shallower subthreshold slopes, and larger threshold voltages, which makes the realization of portable and battery-powered devices very difficult. In addition, the use of low cost manufacturing equipment poses severe limitations on the control of the printing process (layer resolution, layer registration, printing overflow etc.), and thus on the minimum achievable feature sizes. As direct consequence, the parasitic overlap capacitances of the devices increase, strongly impacting the unity-gain frequency f_T of the transistors and limiting the operational frequency of the printed organic circuits typically below the kHz range. Analog and digital circuits which make use of capacitive networks require explicit capacitors much larger than the parasitic ones, in order to maintain accuracy. However, excessively large capacitors are more prone to defects and thus failures. Therefore, circuits employing capacitive feedback networks must be designed taking into account the trade-off between accuracy and yield. Printed organic transistors exhibit modest performance not only from the perspective of the main electrical parameters, but also in terms of noise level. Indeed, the fluctuation of semiconductor conductivity and the low-quality interface between dielectric and semiconductor, are together responsible for large low-frequency noise (1/f) in organic transistors [63][64]. The 1/f component is usually the dominant noise contribution at the operation frequency of the organic circuits. For this reason, the design of frontend electronics for sensor interfaces achieving high resolution is very challenging. Improvements in the Signal-to-Noise Ratio (SNR) can be achieved exploiting auto-zeroing and correlated double sampling techniques [65]. However, the applicability of these techniques is limited by the requirement of large explicit capacitors. Alternatively, low-frequency noise can be mitigated employing chopping [65], which however leads to larger bandwidth requirements.

It is important to remark here that despite the modest electrical performance of printed OTFTs, this is not the major constraint which hampers the development of systems on foil. The limited electrical performance can be a showstopper for certain classes of applications, but many others could still be at reach. The factors that really matter to enable a successful development and commercialization of applications based on printed electronics are: sufficient yield, limited variability, and sufficient device lifetime.

Current state-of-the-art unipolar and complementary organic printed technologies achieve a hard yield performance at device level of < 98 % [66][55]. Shorts, opens, pinholes, particles and imperfections are typically responsible for the primary yield loss. From a more general circuit design point of view, the hard yield defines the maximum circuit complexity which can be manufactured economically. However, the technology yield is only one of the multiple aspects of reliability. Organic transistors suffer from large parameter variability (e.g. threshold voltage shift) due to the low-temperature and low-cost manufacturing process. This issue is exacerbated in solution-processed technologies due to low degree of spatial correlation between printed devices. The variability of the transistor electrical performance from the nominal behavior can potentially lead to soft failures at circuit level. However, this issue can be tackled at the circuit design stage. Thus, it is fundamental to employ architectures that desensitize the overall circuit performance from the device performance variability, in order to maximize the soft yield at circuit level. Additional challenges in the design of printed circuits on foil are introduced by stability issues of the organic materials related to the environment conditions [67], light exposure [68], limited shelf-time and bias stress [69]. It is worth noticing that most of these limitations cannot be easily mitigated at circuit level but should rather be tackled at the technology level.

As stated in the previous section, the highest yield performance in printed electronics has been achieved with unipolar technologies, and thus these are preferred to develop large area circuits. Complementary technologies require a more complex fabrication process to integrate both n-type and p-type transistors, which is intrinsically more prone to defects. Although inherently more reliable, unipolar technologies pose many restrictions on the circuit design. At first, well-known circuit architectures developed for CMOS processes cannot be applied to unipolar technologies. In addition, the lack of the complementary device requires the replacement of active loads with p-type transistors. Simple configurations such as zero-V_{GS} or diode-connected transistors can be employed at the expense of speed and reliability or gain [6], respectively. To give an example, the design of amplifiers with relatively high gain remains extremely challenging. The use of more complex architectures exploiting e.g. positive feedback techniques [54][70] can be effective, but has a negative impact on power efficiency and speed. Indeed, a much larger number of transistors is required, with consequently higher power consumption. Rail-to-rail output swing in analog circuits is also difficult to obtain with unipolar transistors, without the use of external biasing or bootstrap techniques. Even the design of digital logic is not free from restrictions. The basic inverter is usually implemented exploiting diode-connected loads, which leads to a skewed input-output DC characteristics and thus a reduced noise margin. Furthermore, the absence of n-type devices, makes the implementation of clocked gates in dynamic logic more cumbersome. Unipolar digital circuits perform poorly also in terms of power efficiency. The static power consumption associated to the direct current flow between driver and load transistors typically dominates over the dynamic contribution, given the modest switching speed achievable by OTFTs.

Finally, another important factor that negatively affects the evolution of printed electronics (PE) is the fact that Electronic Design Automation (EDA) tools for the design of complex systems based on PE technologies are still in their infancy. Only few Process Design Kits (PDKs) are reported in literature to-date [71][72][73]. Indeed, the constant evolution of the manufacturing steps during the technology advancement requires regular adjustments of the PDK, reducing its effectiveness. In addition, the development of accurate transistor models remains still challenging due the large variability and instability issues that affect the devices.

1.2 Problem statement

Despite the recent advancements of printed organic technologies, their use in commercial products remains up to date very limited. The challenges discussed in Section 1.1.4 still prevent printed systems on foil from commercial exploitation. However, several of these limitations can be tackled and mitigated at the circuit design level. In this perspective, the main challenge relies in the investigation of new design methodologies and topologies specifically suited for printed organic technologies, which are able to improve the robustness of the circuits and thus enable the use of PE for innovative market applications.

1.3 Aim of the thesis

This thesis aims to advance the state-of-the-art of printed organic electronics. The main focus is in the development of technology-aware design methodologies which allow to tackle variability and yield issues, typical of printed organic transistors, and fabricate robust systems-on-foil for the target applications. To achieve this, it is necessary to investigate at first the potential of the printed organic technology, starting from the capabilities of the printing process and following step by step the fabrication of the OTFTs. The study of the electrical characteristics of the devices further leads to the formalization of accurate models, capable to describe the OTFT behavior in different electrical regimes. This knowledge enables the development of a Process Design Kit, specifically tailored to the OTFT and printing process. At this point, systems-on-foil can be developed following a top-down approach. The complete system needs to be investigated at different levels of abstraction, starting from the system-level, moving to the circuit implementation and reaching down to the device level. In this perspective, the PDK connects the system to the technology platform, and permits to evaluate the effectiveness of different design techniques, improving the overall system reliability.

From a practical point of view, this work focuses on the following major aspects:

- Digital circuit design based on printed unipolar OTFT technology, to improve circuit robustness to transistor parameter variability and power efficiency while maintaining minimal circuit complexity in terms of transistor count.
- Design mixed-signal systems on foil providing sensing, data digitalization and energy scavenging functionalities, and even integrating complex circuit functions on a Si IC, as required by the specific applications.
- Design robust active sensor matrices , provided with analog frontend electronics for localized signal amplification, achieving high Signal-to-Noise-Ratio and spatial resolution, to enagle large-area sensing applications.

1.4 Scope of the thesis

In the first part of this work we especially focus on the development of the Process Design Kit (PDK) for a specific gravure-printed organic OTFT technology. This includes the OTFT model (static, dynamic, noise and parameter variability) and several Electronic Design Automation (EDA) tools which enable a robust assisted design flow.

In the second part, we specifically tackle the design and the characterization of four systems on foil, manufactured with a unipolar printed organic technology developed at CEA-Liten, Grenoble, France, for four different applications:

- Multiple-stage organic line drivers for matrix-addressing applications.
- A smart RFID tag for the temperature monitoring in food-packaging applications.
- A large-area proximity sensing surface for human-machine interaction applications.
- A large-area pressure sensing surface for car crash tests applications.

These applications have been selected according to their commercial impact, and are the lead applications of the European project “Advanced high-resolution printing of organic Transistors for Large Area Smart Surfaces” (ATLASS).

1.5 Original contributions

This work contributes to the advancement of the state-of-the-art of printed organic electronics in multiple aspects at system, circuit and technology level. The main author’s contributions are listed as follows, and further organized according to the manuscript chapters.

- In Chapter 3, a novel Process Design Kit is proposed, specifically developed for a gravure-printed OTFT technology. The PDK comprises an accurate model, capable to reproduce static, dynamic and noise behavior of the transistors. A methodology based on a reduced set of parameters is exploited for the formalization of the technology design rules, which are further needed to develop several EDA tools. Parametrized Cells (PCells) have been developed for the automatic generation of transistors, capacitors and resistors according to the design parameters. The proposed PDK is fully integrated in the commercial framework Cadence Virtuoso®, and further provided with design rule checking, layout versus schematic comparison and layout parasitic extraction functionalities, developed using the DIVA® EDA tools.

- In Chapter 4, several multi-stage line driver circuits are presented, which are fabricated with printed unipolar organic technology. The three proposed 8-stage architectures exploit different design approaches, which lead to different trade-offs between circuit complexity, power consumption and area occupation. Measurement results reveal that one of the novel dynamic cells proposed for the single delay stage outperforms other implementations in terms of complexity, energy efficiency, integration density and circuit yield. The 8-stage line driver circuit based on the dynamic cell comprises 139 OTFTs and 9 capacitors, requiring an area of 6.6 cm^2. From the yield point of view, 15/15 fully functional structures have been measured over 5 successive foils, demonstrating the possibility to further upscale the number of driving lines, while preserving a good circuit yield.

- In Chapter 5, a world-first smart temperature sensor on RFID in flexible printed electronics is demonstrated. The system-on-foil is capable of sensing the environment temperature, converting it to a binary representation exploiting a Pulse Width Modulation (PWM) and sending it to a reader through backscattering, via the radio frequency communication link. The system is further equipped with an energy scavenging circuit in order to be wirelessly powered by the reader. The sensing functionality is achieved by using printed resistive temperature sensors, while the analog to PWM conversion is performed with OTFTs, by means of a time-based interface which exploits a first-order Bang Bang Phase-Locked Loop. The temperature-to-duty cycle converter makes use of a stabilized reference oscillator in order to maintain the correct functionality of the system for a wide range of supply voltages. The smart sensor requires an average power consumption of 2 mW and a conversion time of 2 s to achieve a temperature resolution of 291 mK_{RMS}. In addition, the statistical characterization of 15 samples reveals a maximum temperature error smaller than ± 1.6° C (±3 sigma), achieved over the food-monitoring temperature range from 3° C to 27° C after systematic non-linearity correction and 2-point calibration.

- In Chapter 6, a first-ever fully-printed large-area proximity sensing surface with integrated Analog Fronted Electronics is presented. The proposed 5x10 active matrix is obtained by lamination of printed organic pyroelectric sensors on foil (frontplane) with printed organic frontend electronics (backplane). The role of the frontend electronics is to provide signal amplification and unambiguous pixel addressing in order to maximize the SNR and reduce the pixel crosstalk. In this perspective, each proximity sensor is read-out in current mode by means of a dedicate Charge Sensitive Amplifier (CSA) implemented with an inverter-based single-ended amplifier and a capacitive feedback network. The CSA requires in total 12 OTFTs and 4 capacitors. All the pixels belonging to the same matrix column are further readout in a Time-Division-Multiplexing (TDM) fashion by means of an active-addressing circuit, included in the frontend pixel electronics. From the application perspective, the complete matrix achieves a readout frame rate of 100 Hz, and enables the proximity detection of humans approaching from a distance > 40 cm. The robustness of the proposed system architecture is further proven by the high yield of the backplane electronics. Indeed, with a maximum of 96% fully functional pixels (in a single matrix), corresponding to 768 working devices, this circuit attains the record of complexity (in terms of device number) for a printed organic technology to date.

- In Chapter 7, for the first time a system architecture based on hybrid PE and Si-IC electronics is presented. The main innovation of this work relies on the successful co-integration in the very same system of a Si-IC (based on Si-65 nm CMOS technology) with a SiP (manufactured with printed organic materials). The use of printed organic technologies allows the development of a low-cost smart system-on-foil, exhibiting pressure sensing capabilities over large-area and unprecedented form factors. The core of the SiP is a 5x3 active matrix obtained by lamination of printed organic pressure-sensitive sensors on foil (frontplane) with printed organic frontend electronics (backplane). The pixel frontend electronics makes use of a transconductor to perform two functionalities at once: it guarantees a high-speed unambiguous pixel addressing and provides a voltage-to-current conversion which further enables the direct interconnection to the Si electronics. A customized Si-IC is designed to perform the matrix readout with additional analog-to-digital conversion of the output streams. From the system point of view, the use of active-matrix addressing functionality on SiP allows to drastically reduce the number of interconnections required for the IC, and thus the overall system cost.

1.6 Outline of the thesis

The manuscript is further organized as follows. In chapter 2, the printed OTFT technology is introduced in a bottom-up fashion, starting from the printing capabilities and reaching the device fabrication process. The OTFT electrical characterizations and the technology yield analysis are also reported in this chapter.

Chapter 3 discusses the development of the PDK for the printed organic technology. First, the OTFT models (static, dynamic and noise) are derived. Next, the methodology developed to define the technology Design Rule Manual (DRM) is introduced. The integration of the PDK in a commercial Computer Aided Design (CAD) framework is further discussed.

Chapter 4 focuses on the design and characterization of three multistage line driver architectures for matrix addressing applications. The experimental results are used to fairly compare the performance of the different implementations, and define the architecture which is most suitable for the target applications.

Chapter 5 shows the design and evaluation of a printed smart sensor on RFID, for temperature monitoring in food-packaging applications. The system requirements for the target application are derived at first. Next, the overall system architecture is defined, and the circuit implementation of each submodule is discussed. At last, the measurement results obtained from the system-on-foil characterization are presented.

Chapter 6 deals with the design of a proximity sensing surface on foil. The design flow is discussed with a top-down approach, starting from the system level, moving to the submodule architectures and reaching down the circuit implementations at transistor level. The experimental characterization of the overall system as well as each individual submodule is also provided.

In Chapter 7 presents the design and evaluation of a smart pressure sensor with hybrid electronics. The chapter mainly focus on the development of the SiP, Si-IC and their integration challenges. A thorough characterization of the system in all its parts is also provided.

Finally, conclusions are drawn in Chapter 8.

2. Unipolar OTFT technology

This chapter presents the process flow developed at CEA-Liten for the fabrication of the printed unipolar organic transistors, together with the results of the OTFT electrical characterization and the statistical analysis of technology yield and device variability. This information will be further exploited in chapter 3 to develop the technology process design kit (PDK).

The contents of this chapter have been published in the ESSDERC conference proceeding [74] and IEEE Electron Device Letters [75].

2.1 Introduction

Printed OTFTs are manufactured with fully-additive or combination of additive and subtractive processes [76], starting from a carrier substrate which can be flexible (plastic foils, paper, etc...) or rigid such as glass. Generally, the OTFT stack comprises an organic semiconductor (OSC) layer, an organic dielectric (ODL), two electrodes placed on the same plane (source, drain) and a third electrode placed on a separate plane (gate). Several transistor structures have been investigated in literature [77]. These can divided at first, in Top-Gate (TG) and Bottom-Gate (BG) structures, according to the position of the gate electrode with the respect to the layer stack. Each structure can be further defined as coplanar or staggered, depending on the relative position of the transistor channel and the source/drain (S/D) electrodes. The four main OTFT configurations are depicted in Figure 2.

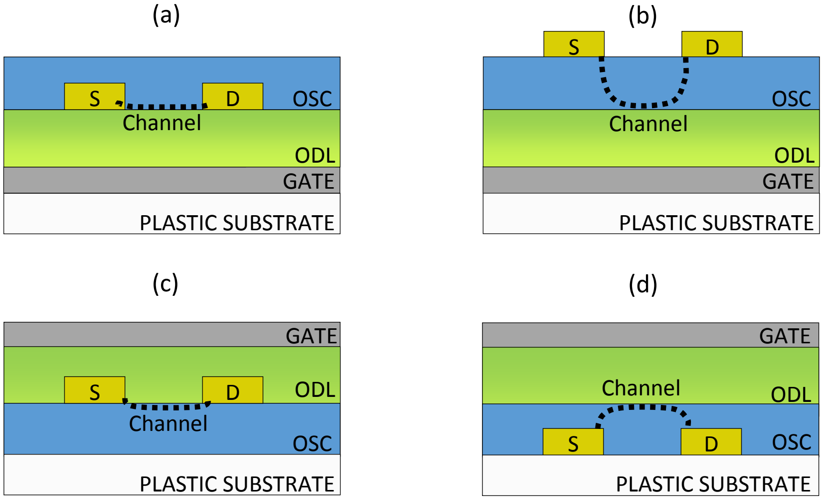


Figure 2. Organic Thin-Film Transistor configurations: (a) Coplanar Bottom-Gate, (b) Staggered Bottom-Gate, (c) Coplanar Top-Gate, (d) Staggered Top-Gate.

The choice of the transistor structure is typically dictated by constraints of the fabrication process, as well as the target device performance. BG structures are generally preferred to TG ones, since they allow the printing of the semiconductor as last layer of the transistor stack, minimizing the possibility of performance degradation introduced by the overprinting of subsequent layers. In addition, staggered OTFT configurations outperform in general the planar counterparts in terms of carrier injection capability, due to their larger injection surface provided by the OSC-S/D electrode interfaces [77]. However, the use of TG configurations can be attractive from the fabrication point of view. Indeed, high-resolution patterning techniques can be exploited to finely pattern S/D electrodes [15] reducing the transistor length, and thus improving transistor performance and integration density. However, short-channel effects such as drain-induced barrier lowering (DIBL) and channel length modulation (CLM), as well as charge injection issues, may become prominent with the reduction of the transistor length, limiting the effectiveness of downscaling.

The approach of using a finer pattern for source and drain has been exploited in this work to manufacture mostly-printed unipolar p-type organic transistors on a S2S (Sheet-to-Sheet) platform. The OTFTs are manufactured according to the staggered TG stack depicted in Figure 2(d). More specifically, the S/D electrodes are developed using photolithography techniques which guarantee relatively high-resolution patterning, while the organic semiconductor, the organic dielectric and the gate electrode are fabricated with high-throughput graphic printing techniques.

Recent research has focused on the use of printing techniques such as gravure and reverse offset to manufacture organic electronics and create fully printed organic electronics, compatible with low-cost mass-production [61][62][78]. Indeed, the use of these techniques allows to achieve high-resolution and superior overlay control performance compared to flexography and screen-printing [77]. These superior patterning characteristics can be beneficial for the improvement of the transistor speed performance, as well as for the reduction of the device footprints. In this perspective, gravure has been selected in this work for the printing of the OSC and ODL layers.

This chapter is further organized as follows: first, the S2S fabrication process is presented in the Section 2.2. Next, the electrical characterization of the OTFTs is provided in Section 2.3. Section 2.4 presents preliminary results about the technology yield analysis, and describes an adaptation of the fabrication steps to further reduce the device defectivity. In Section 2.5 the analysis of the OTFT electrical parameter variability is reported. Finally, conclusions are drawn in Section 2.6.

2.2 S2S fabrication process

The printed unipolar organic technology has been developed at CEA-Liten, on the PICTIC Pilot Line using the GEN1 sheet-based process in a cleanroom environment (500m² Class 10000). Since interface quality and overlay control are critical in OTFTs, a sheet-to sheet strategy on a glass carrier is exploited in this work, in order to enable high versatility, easier control of surface treatments and improved registration performance. The available design area (Figure 3(a)) is typically divided in four different modules featuring an area of 126x126 mm² each (Figure 3(b)).

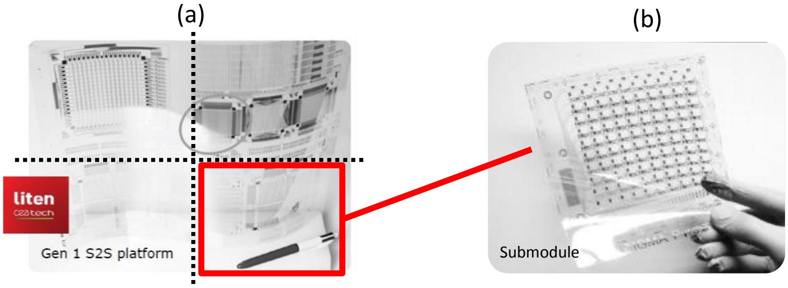


Figure 3. (a) Printed electronics on GEN1 PEN substrate. (b) 126 x 126 mm^2 submodule.

In Figure 4, the fabrication process flow of the S2S technology [74] is presented. The technology stack realizes a staggered top-gate OTFT configuration. The S/D contacts are directly developed with a photolithography process on a metallized GEN1-size Polyethylene Naphthalate (PEN) substrate laminated on glass carrier. In order to favor good charge injection and reproducible performance, source and drain electrodes are made of 30 nm thick gold. This step is followed by a short oxygen plasma treatment prior to semiconductor deposition, in order to ensure a clean surface and low contact resistance. The Organic Semiconductor (OSC) (SP500 Lisicon® polymer from Merck) is directly gravure-printed as a rectangular pad with a thickness in the range of 45 nm with the Ohio ACCUPRESS GEN1 Gravure Printing Unit. Next, a ~500 nm low-k dielectric (Lisicon® D320) is gravure-printed, giving an approximate capacitance per unit area of ~3.7 nF/cm^2. The interconnections between the S/D and GATE conductive layers are obtained with the use of VIAs. These are formed by the overlap of the two conductors in an area free from dielectric (Figure 4). Finally a 6µm conductive ink is screen-printed on top of the stack, to define the gate electrode. All processing steps were carried out in air and with baking temperatures below 120 °C.

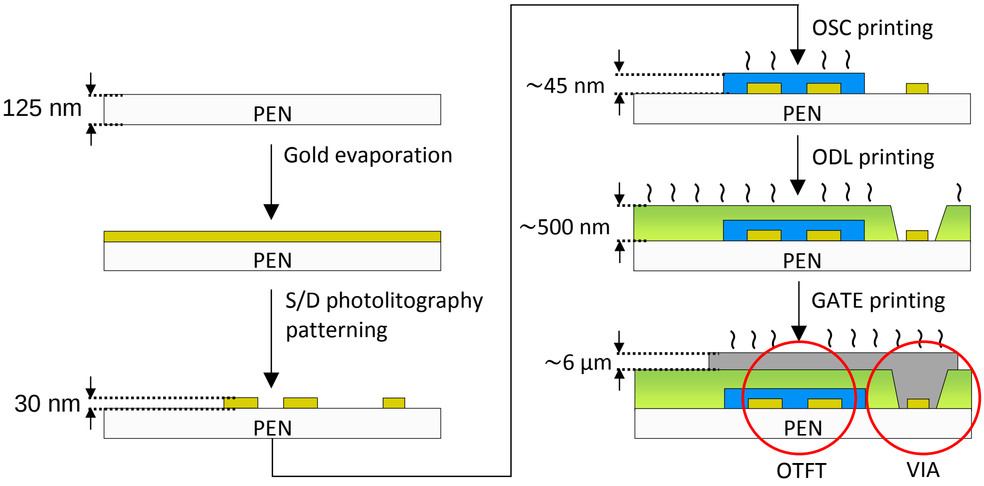


Figure 4. Fabrication process flow of the S2S printed unipolar organic technology. The cross-section shows step-by-step, the development of an OTFT and a VIA interconnection between S/D and GATE metal layers.

2.2.1 Source/Drain layer patterning

The first layer of the technology stack comprises the OTFT S/D electrodes and interconnections. Its fabrication involves the metallization of the plastic foils by means of gold evaporation, patterning through optical UV lithography and further development with wet etching. A typical GEN1 (300 x 400 mm^2) plastic substrate laminated on glass carrier and patterned with S/D layer is shown in Figure 5(a). The minimum feature size which can be developed with sufficiently high yield is limited to 6 µm, using the current photolithography process. Thanks to its relatively high-resolution and position in the stack, the S/D layer is also used as reference for the alignment of all the printed layers. Indeed, the registration capability is a critical parameter in OTFT devices to achieve printing downscaling at good overlay. Consequently, it is crucial to maintain the dimensional stability of the reference layer with respect to the intended design. In this perspective, the S/D patterning process has been optimized to reduce the maximum distortion of the structures on the S/D layer, caused by the deformation of the plastic substrate, to less than 10 µm in both X and Y directions (Figure 5 (b)).

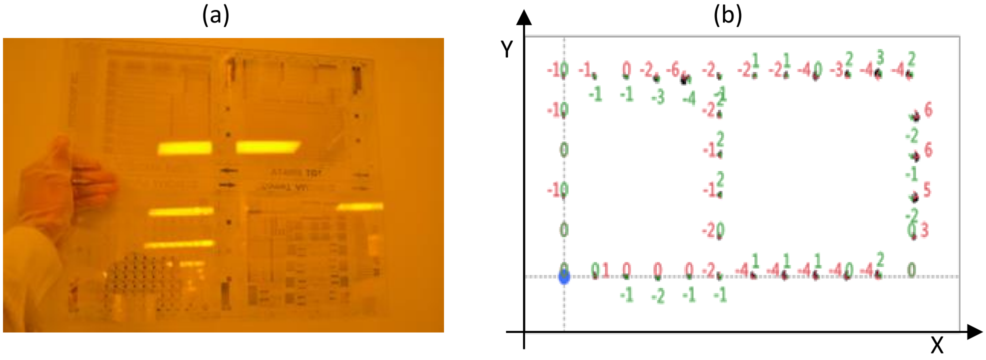


Figure 5. (a) GEN1 foil laminated on glass, with patterned S/D layer. (b) Evaluation of the position deviation between designed and fabricated structures on the S/D layer, caused by the substrate deformation. The position displacement is indicated in both X (red) and Y (green) directions for each analyzed point.

2.2.2 Organic Semiconductor printing

Rotogravure is a printing technique that transfers ink from small cells engraved in a cylinder to the plastic substrate by a rolling contact [77] (Figure 6). Stylus engraving technology has been selected here for the roll, because the resulting cell, which has a pyramidal footprint (Figure 7(a)), provides improved ink transfer. In this approach, however, the resolution of the cell, its volume and the capability of transfer are linked together. Consequently the parameters of the cells (stylus and density) have been co-optimized in order to enable a smooth and well-defined printing of the semiconductor. As shown in Figure 7(b), the process developed in this work is capable of printing distinguishable patterns down to an area of 75 x 75 µm^2. Indeed, the minimum feature size (75 µm) corresponds approximately to two times the writing resolution of the engraved cells (Figure 7(a)). The profile reported in the inset of Figure 7(b) highlights the successful optimization of both printing process and ink, which makes it possible to reach the 45 nm target semiconductor thickness with good uniformity and low roughness in the active area (< ±5 nm, a figure comparable with subtractive processes). The printing stability of the organic semiconductor has been optimized to allow 1 hour processing in air with thickness variations below 10%.

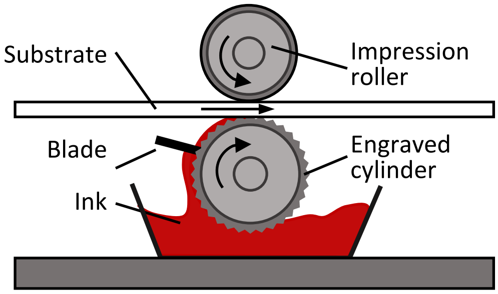


Figure 6. Operating principle of gravure-printing technique.

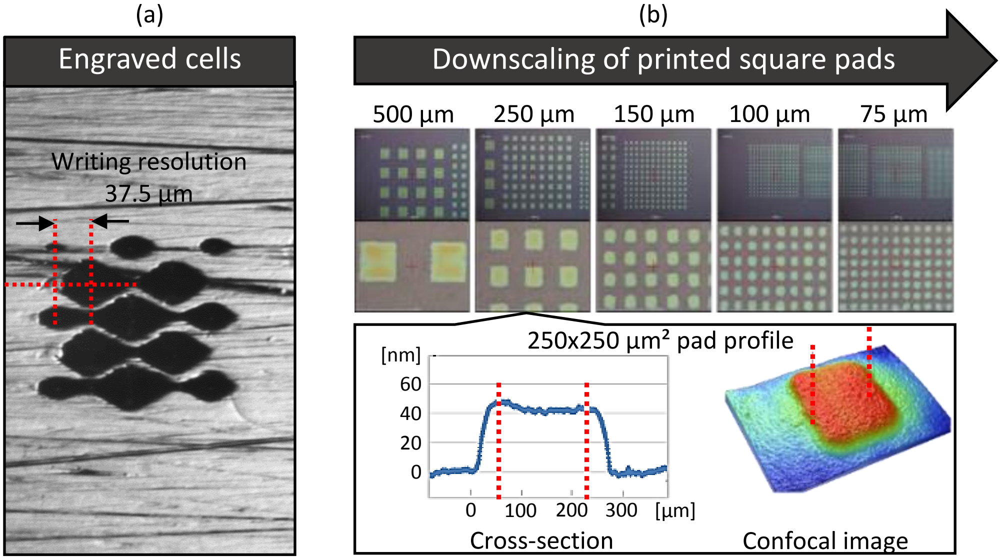


Figure 7. (a) engraved cells on printing roll. (b) Printing capability for a series of square semiconductor pads, featuring side length ranging from 500 µm to 75 µm. (Inset) Printing profile and confocal microscopy for a 250 x 250 µm² semiconductor pad.

The most important parameter to improve circuit density is the control of overlay during fabrication. The reproducibility of the semiconductor pad position has been evaluated here for 100 similar OTFTs over 9 foils manufactured during a one-hour run. In Figure 8(b) it is shown the position of the OSC corners compared to the center of the designed shape (blue square), extracted for this population of OTFTs through an Automated Optical Inspection

Capture system (ATLASS Observer by INCORE System). Due to the finite resolution of the engraved cells (Figure 8(a)), the distribution on foil of the printed pad corners exhibits a width ranging from 40 µm to 75 µm. This result is comparable to the writing resolution of the engraved cell, which is ± 37.5 µm.

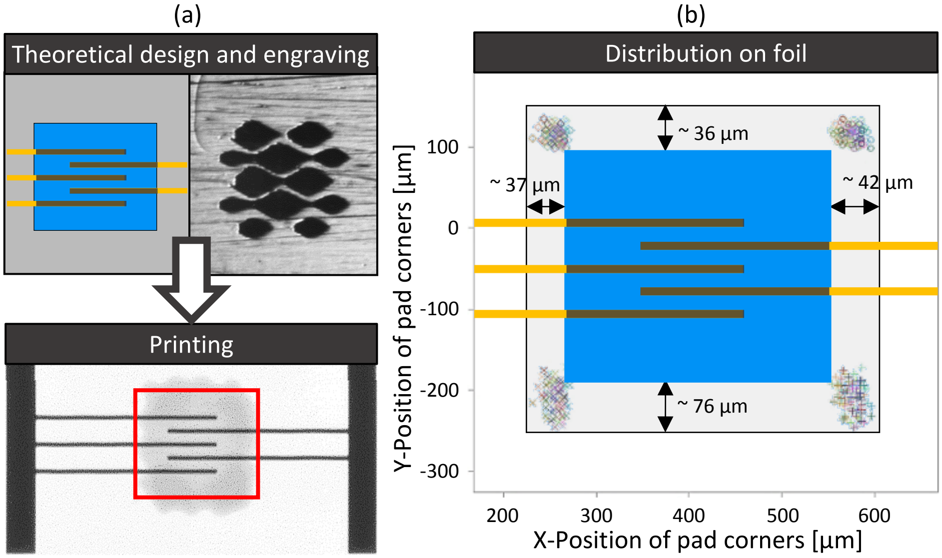


Figure 8. (a) Designed and engraved OSC pattern on printing roll and resulting printed pad on plastic substrate. (b) Distribution of corner positions (symbols) extracted over the same foil from 100 semiconductor pads of the corresponding OTFTs. The S/D electrodes are used as alignment reference.

The registration capability of the printing unit has also been qualified, by monitoring the relative position of each semiconductor pad from foil to foil. Figure 9 shows a registration capability better than ±10 µm for both the printing (X) and transverse directions (Y). This confirms the potential for further downscaling of the printed feature sizes, if the engraving of the cells could be optimized for higher resolutions.

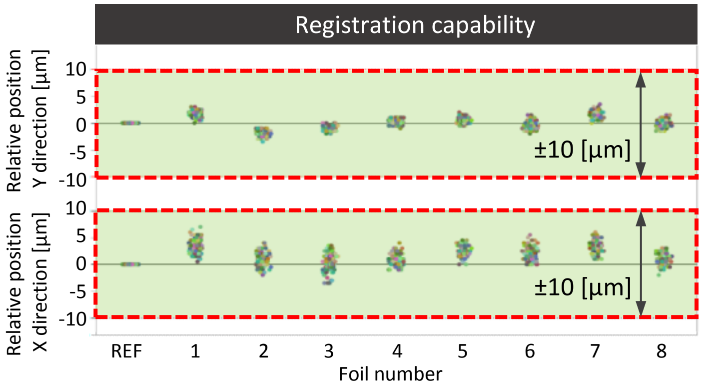


Figure 9. Foil-to-foil registration capability evaluated over 100 TFTs on 9 successive foils.

2.2.3 Dielectric printing

The dielectric printing is also performed by means of a rotogravure technique. Similarly to the semiconductor case, the dielectric printing exploits a stylus engraving technology based on pyramidal cells. The cell parameters (stylus and density) have been here co-optimized together with the dielectric ink formulation to achieve a layer printing with smooth coverage and uniform thickness of about 500 nm. In order to guarantee the access to the S/D layer and its interconnection with the GATE metal layer through VIAs, openings on the dielectric layers are required. The minimization of the VIA size is beneficial to improve the integration density of the technology. In this perspective, the downscaling of the cell engraving resolution allows patterning with high-definition reaching minimum feature sizes of 25 µm (Figure 10).

However, high resolution intrinsically leads to low volume transfer and thus reduced layer thickness in the range of ∼100 nm. Consequently, a more conservative approach employing engraved cells with a resolution of ± 37.5 µm has been chosen to achieve the target dielectric thickness (∼500 nm). In this case, the dielectric opening which can be manufactured at the target layer thickness and with relatively high yield, requires a minimum area of 300 x 300 µm^2.

It is worth noticing, that the printing of the ODL and OSC layer is performed with the same gravure printing unit, leading to the same overlay control performance.

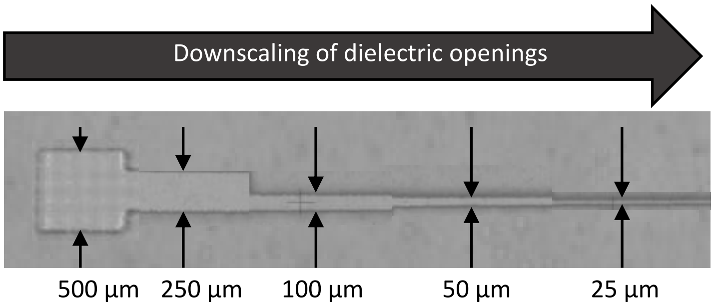


Figure 10. Downscaling of the dielectric openings. Feature size ranging from 500 µm to 25 µm.

2.2.4 Gate electrode printing

Screen printing is a patterning technique which makes use of a screen comprising a mesh of plastic or metal fibers to transfer the ink onto a substrate [77]. The patterns are defined on the screen by filling certain areas of the mash with a blocking stencil. A squeegee is used to bring the mesh in contact with the substrate and press the ink through the openings of the screen, in order to define the desired pattern on the substrate (Figure 11).

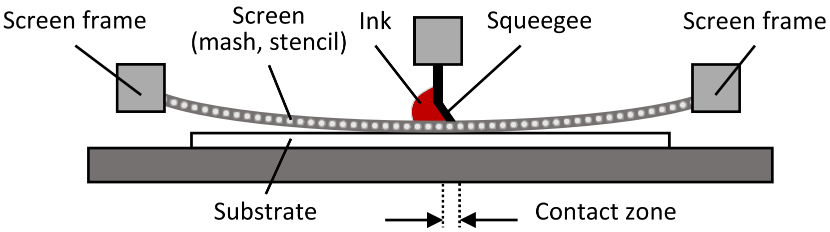


Figure 11. Operating principle of screen-printing technique.

Despite its wide use in the printed electronics, the screen printing has several limitations. In order to achieve a good pattern definition, high viscosity inks are required. However, the printing resolution is determined by the mesh size of the screen. In addition, relatively thick films can be produced since the layer thickness is directly related to the thickness of the screen.

For these reasons, in this work the use of screen-printing has been limited only to patterning of the gate electrode and top-level interconnections. In this way, because of the staggered TG configuration of the OTFTs, the thickness of the gate profile will not interfere with the deposition of other critical layers. The printing of the GATE layer achieves a resolution of 150 µm and a maximum misalignment <±50 µm. The main patterning performance parameters for each layer in the technology stack are summarized in Table 1. Despite the screen-printing approach leads to inferior performance in terms of resolution and overlay control compared to the rotogravure, its use in the specific fabrication flow is preferred, in order to reduce the overall production time. Indeed, as only one gravure machine is available, the fabrication of each gravure printed layer requires the substitution of the engraved roll, which is results in additional lead-time.

Table 1. Summary of the patterning performance parameters for each technology stack layer.

Stack layer	Fabrication technique	Min. feature size [µm]	Registration capability [µm]	Edge roughness [µm]	Thickness [nm]
S/D	Photolithography	6	Reference	< 1	30
OSC	Gravure-printing	75	< ± 10	< 35	45
ODL	Gravure-printing	300	< ± 10	< 35	500
GATE	Screen-printing	150	< ± 50	< 50	6000

2.3 Electrical characterization

The transfer and output characteristics of OTFTs manufactured with the S2S process have been measured in order to provide insight in their electric performance and main device parameters (e.g. threshold and mobility). In this perspective, arrays of OTFTs featuring Transmission Line Model (TLM) layout geometry and different channel lengths have been evaluated in air, dark and at room temperature. The statistical assessment over 100 devices provides a thorough evaluation of the transistor performance and further enables a robust extraction of the parameters for the OTFT modelling (discussed in Chapter 3).

A subset of the measured transfer characteristics obtained for L=800/200/50/10 µm (10 TFTs each) are reported in Figure 12(a).

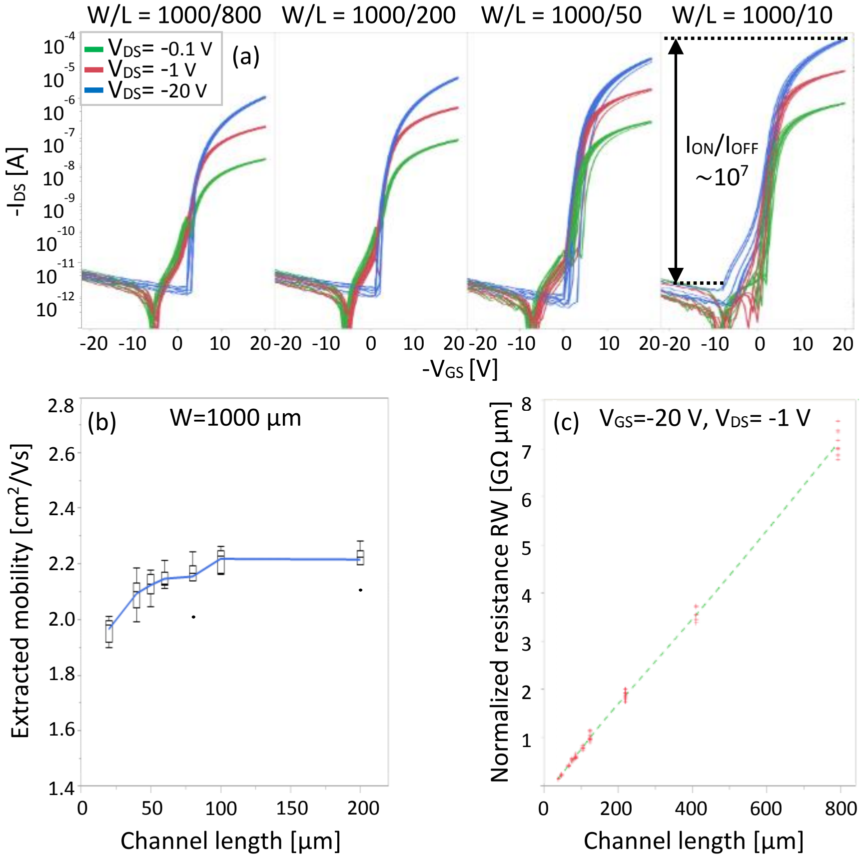


Figure 12. Electrical characteristics extracted from a subset of the 100 OTFTs measured from TLM structures [74]. The measurements are organized in groups of 10 devices for each channel length (W=1000 µm/L =800/200/50/10 µm). (a) Transfer characteristics in linear (V_{DS}=-0.1/-1 V) and saturated regime (V_{DS}=-20 V). (b) Mobility extracted with Y-function approach [79]. (c) Normalized transistor resistance for different channel lengths.

The gate voltage V_{GS} has been swept from +20 V to -20 V and back, with steps of 250 mV at different drain biasing conditions (V_{DS} = -0.1/-1/-20 V). From Figure 12(a), an off-current lower than 5 pA can be observed, which leads to an ON/OFF current ratio of 7 decades for OTFTs with L=10 µm. The small variability of the sub-threshold slope and I_{ON} current highlight the good reproducibility from device to device.

The beneficial impact of the polymer semiconductor (as opposed to small-molecules organic semiconductors, which are typically characterized by larger variability) is demonstrated by the narrow mobility distributions, which are shown in Figure 12(b). The Y-function method has been employed here to remove the contribution of the contact resistance in these measurements [79]. The extracted mobility (>2 cm²/Vs) outperforms conventional amorphous silicon and still enables low variability (<10%). The transfer characteristics also show a good scaling behavior at different channel lengths, suggesting no significant impact of carrier injection issues on the OTFT performance for L>40 µm. In order to confirm and quantify this important parameter for analogue circuit design, the scaling of the normalized total transistor resistance is shown in Figure 12(c), from which the contact resistance contribution can be evaluated to ∼40 MΩ·µm.

Finally, as general indication of the OTFT performance, the main electrical parameters extracted from the TLM structures are summarized in Table 2.

Table 2. Main OTFT electrical parameters

Electrical parameter	Symbol	Value	Unit
Carrier mobility	µ	2.2	[cm²/Vs]
Capacitance per unit area	C_I	∼3.7	[nF/cm²]
Threshold voltage	V_{TH}	-3.5	[V]
I_{ON} · L/W	I_{ON}	$\sim 10^{-5}$	[A]
I_{OFF} · L/W	I_{OFF}	$\sim 10^{-12}$	[A]
I_{ON}/I_{OFF} ratio	I_{ON}/I_{OFF}	$\sim 10^{7}$	-
Subthreshold slope	VSS	0.75	[V/dec]
Normalized contact resistance	R_{CN}	∼ 40	[MΩ µm]

2.4 Yield performance

The evaluation of the device yield performance in the proposed technology [74], highlighted high defectivity due to excessive gate leakage. This issue is typically severe in printed TG device configurations, where the gate dielectric needs to provide both good interface quality with the underlying semiconductor as well as chemical and mechanical resistance to the subsequent printing of the gate electrode.

In order to improve the robustness of the dielectric-gate stack, and thus the overall yield performance, a dielectric printing based on a multilayer approach has been investigated. Individual layers exhibiting thicknesses in the range of 300 nm, have been stacked in different configurations as reported in Figure 13. Moreover, for each configuration the OTFT yield has been evaluated over a population of 500 devices featuring increasing semiconductor areas (S1=0.07 mm^2, S2=0.36 mm^2, S3=1.26 mm^2). In this study, an OTFT is considered faulty if its gate leakage current is > 1nA.

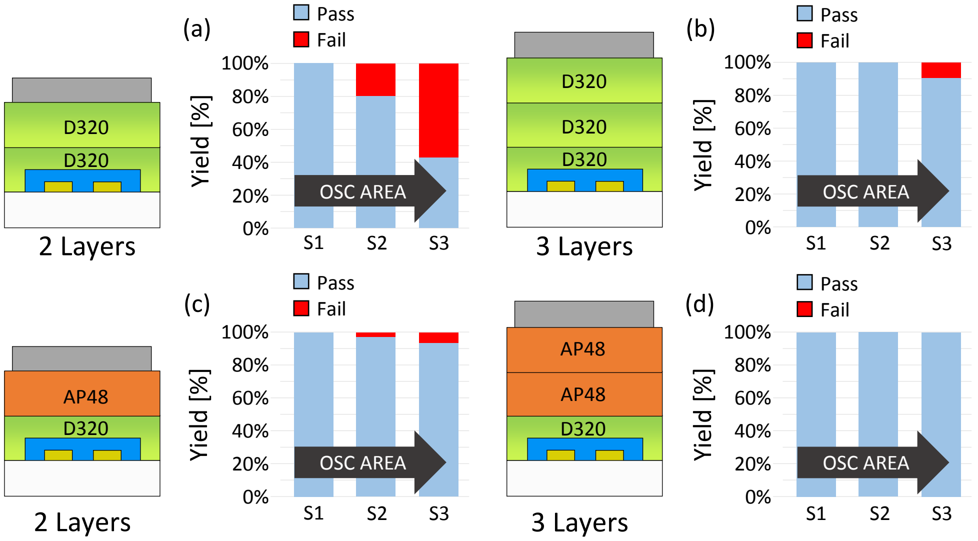


Figure 13. OTFTs yield analysis performed over three groups of transistors characterized by different semiconductor areas (S1, S2, S3), and manufactured with different layer stack configurations [75]. The groups S1, S2 and S3, comprise 100, 200 and 200 OTFTs, respectively. An OTFT is considered faulty if its gate leakage current is > 1nA. (a) Two-layer stack with D320 dielectric. (b) Three-layer stack with D320 dielectric.(c) Two-layer stack with hybrid dielectric D320-AP48.(d) Three-layer stack with hybrid dielectric D320-AP48-AP48.

Despite the two-layer approach, when using the dielectrics D320 (Figure 13(a)), the yield reaches 100% only in the smallest transistors (OSC area S1) and rapidly decreases as the semiconductor area increases. The introduction of a third D320 low-k dielectric layer Figure 13(b) reduces the defectivity but still does not achieve 100% yield (the percentage of defective OTFTS is 10% for the S3 OSC area population). A further increase of the dielectric thickness would be detrimental for device performance. Indeed, this will lead to larger threshold voltages and will reduce the effectiveness of the channel downscaling, due to stronger short channel effects.

In order to mitigate the sensitivity of the devices to gate-leakage defects, without further increasing the overall dielectric thickness, the second D320 low-k dielectric layer has been replaced with a cross-linked polymer, which exhibits improved mechanical robustness. This hybrid dielectric configuration is shown in Figure 13(c). The cross-linkable dielectric polymer (AP48 lisicon® with dielectric constant ε_r=2.5) is also gravure printed with a target thickness in the range of 300 nm and crosslinked by means of UV irradiation at a wavelength of 365 nm, with a dose of 2 J/cm². The comparison between the results reported in Figure 13 (a) and (c), clearly highlights the benefits of this approach towards gate leakage reduction. In order to maximize the device yield, a 3-layer stack configuration has been eventually used in combination with the hybrid dielectric approach, leading to the structure depicted in Figure 13 (d). The yield analysis reported Figure 13(d) demonstrates the successful optimization of the printing process to maximize yield.

The technology yield has been further quantified using a population of 540 devices featuring S3 OSC area, distributed over 6 successive foils. The measured transfer characteristics and gate leakage currents are presented in Figure 14. The yield analysis reveals 100% functional OTFTs, with only one device exceeding the leakage current threshold of 1 nA, leading to 99.8% yield.

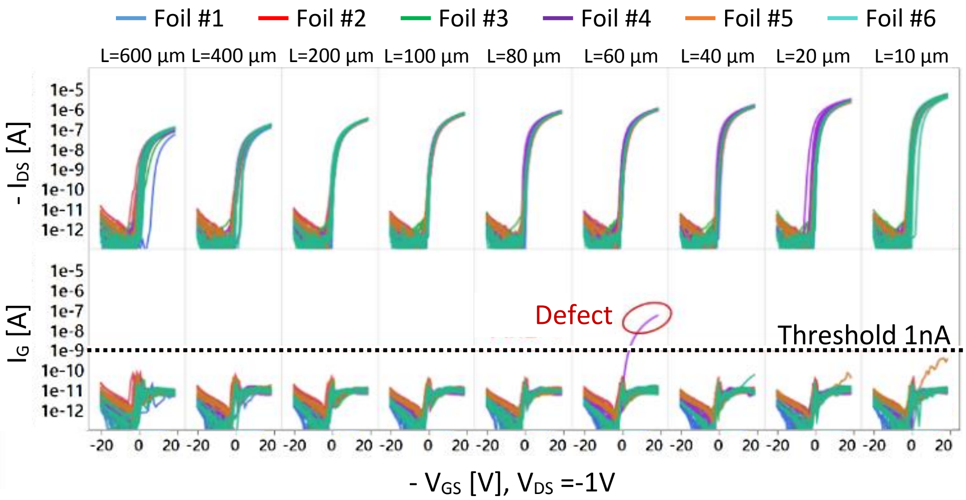


Figure 14. Transfer characteristics in linear regime (V_{DS}=-1V) obtained from a set of 10 devices per channel length L evaluated over 6 successive foils, manufactured with the 3-layer hybrid dielectric stack shown in Figure 13 (d) [75]; all the OTFTs feature channel width W equal to 1000 µm), and the capacitance per unit area C_I is estimated to be ~2.1 nF/cm².

2.5 Parameter variability

The very same measurement database exploited for the device yield analysis has been used to quantify the transistor parameter variability. The outcome of this analysis is further exploited in Chapter 3 to introduce the device parameter variability in the circuit simulator. For the sake of simplicity, the analysis has focused only on the two main OTFT electrical parameters in above-threshold regime, namely the current prefactor β (equal to $\mu \cdot C_I$) and the threshold voltage V_{TH}.

These parameters have been automatically extracted from the transistor transfer curves recorded over the population of 540 devices, distributed over 6 different foils. The Y-function method [79] has been used to remove the contribution of the contact resistance from the mobility extraction. Indeed, especially in devices with short channel lengths (L<40 µm) the contact resistance plays a non-negligible role. It is worth mentioning that the applicability of the Y-function method is restricted to the linear regime and for $|V_{GS}|>>|V_{TH}|$. In addition, the threshold voltage can be estimated as the V_{GS} value at which the Y-function is equal to zero [79]. The values of β and threshold voltage V_{TH} extracted in this way are presented in Figure 15 (a) and (b), respectively. From Figure 15 it can be observed that the multi-layer dielectric fabrication process, introduced to improve the device yield performance, has made more negative the threshold voltage of the transistor, which now exhibits a typical value of about -4.7 V.

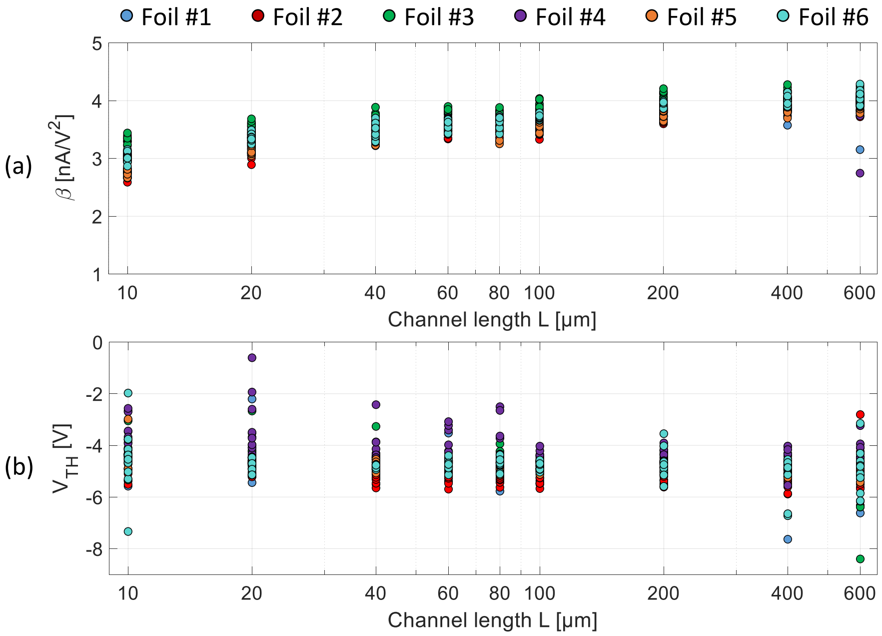


Figure 15. (a) Current prefactor β and (b) threshold voltage V_{TH} distributions extracted with Y-function method [79], from 540 measured OTFTs featuring L ranging from 10 µm to 600 µm (10 devices per length) and W = 1000 µm. The measured OTFT are manufactured over 6 successive foils.

The statistical characterization of the extracted parameters is further used to deduce information on two categories of parameter variability, namely the within-foil and the foil-to-foil variability. The first category is related to the global variations of the electrical parameters of transistors placed on the very same foil. The within-foil variations are extracted from the data of Figure 15 , calculating the standard deviation of the two parameters, respectively σ_β and σ_{VTH}. More in detail, for each foil and each channel length L, the parameter distributions are here subtracted from their mean value, respectively $\overline{\beta}$ and $\overline{V}_{TH}$. This leads to initial datasets of 60 samples for each L, which are further reduced by eliminating the outliers, identified here with the Generalized Extreme Studentized Deviate (GESD) test [80]. The resulting datasets are finally used to compute the standard deviation of β and V_{TH} at the different channel lengths. The outcomes of this statistical analysis are presented in Figure 16 and (b), for β and V_{TH} parameters, respectively. From the results provided in Figure 16(a), it can be deduced that the standard deviation of the β parameter is nearly constant for a large span of channel lengths, and increases as L approaches values larger than 200 µm. The standard deviation trend extracted from the threshold voltage distributions exhibits a negative slope for channel lengths ranging from 10 µm to 40 µm. The trend further fluctuates around a constant value for 40 µm ≤L≤ 400 µm and rises at L=600 µm. Arbitrary fitting functions have been introduced to reproduce the dependence of σ_β and σ_{VTH} with L, in the circuit simulator (further discussed in Chapter 3). In this perspective, the first trend is fitted with a 2nd order polynomial function (Figure 16(a while the approximation of the second trend makes use of two exponential functions (Figure 16(b)).

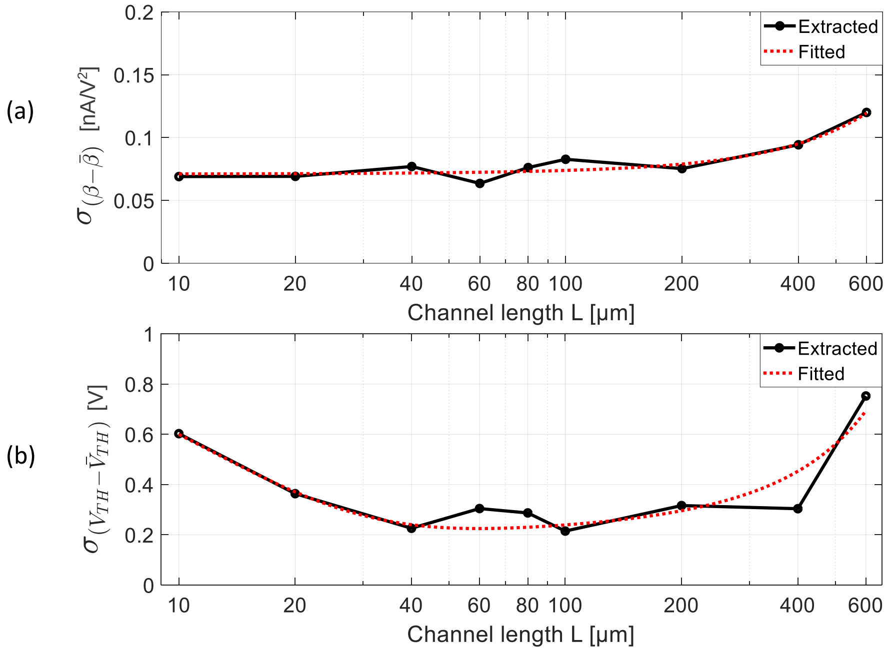


Figure 16. (a) Extracted (black) and fitted (dashed-red) standard deviation distribution of the current prefactor obtained at different channel lengths. (b) Extracted (black) and fitted (dashed-red) trend of the threshold voltage standard deviation, estimated for different device channel lengths.

The foil-to-foil variability is instead related to the variations of the electrical parameters, between transistors placed in different foils. This is here estimated from the overall mean value (regardless channel length) of the β and V_{TH} distributions between foils. The extracted main statistical parameters are reported in Table 3. It is worth mentioning that the distributions of the mean values comprise only 6 samples (foils), therefore leading to a modest estimation accuracy.

Table 3. Main statistical parameters extracted from foil-to-foil distributions of the mean values of β and V_{TH}.

Foil-to-foil parameter variability						
Parameter	Min	Median	Mean	Max	Sigma	Unit
Mean (β)	3.47	3.60	3.60	3.81	0.13	[nA/V^2]
Mean (V_{TH})	-5.00	-4.78	-4.72	-4.06	0.36	[V]

2.6 Conclusions

The gravure-printed unipolar organic transistor technology presented in this Chapter has been developed at CEA on a S2S platform. The printing process has been initially optimized in order to achieve the downscaling of the feature sizes, while ensuring reproducibility and stability of the printing performance. The outcome of this optimization process led to the fabrication of TG staggered OTFTs exhibiting carrier mobility as high as 2.2 cm^2/Vs and featuring a minimum channel length of 10 µm [74]. At this stage, the electric characterizations of the transistors revealed high device failure rates, mainly caused by the poor control of the gate leakage current. Further adjustments of the fabrication process have been implemented at CEA-Liten, in order to improve the device yield performance of the technology. The combined use of a cross-linked dielectric ink and multi-layer printing approach enabled the fabrication of OTFTs with a yield as high as 99.8 % (estimated over a population of 540 devices). Thus, the successful optimization of the fabrication process enabled an OTFT technology characterized by state-of-the art yield performance [75].

Despite the relatively high transistor yield, the circuit complexity (in terms of device count) remains one of the major concerns in the design of systems-on-foil. Circuit architectures which exceed a complexity of a few hundred devices cannot be manufactured with reasonable yield yet, if all these devices need to be functional. This knowledge about the technology is exploited at the system level design phase in Chapters 4 to 7, to derive the most suitable architectures for the target applications.

Furthermore, an investigation of the device parameter variability has been performed on the electrical characteristics obtained from the OTFTs, manufactured with the yield-optimized fabrication process [75]. The results of this analysis have been included in the Process Design Kit of the technology (discussed in Chapter 3), in order to reproduce the effect of the OTFT parameter variability in the circuit simulator and thus, enable the choice of circuit implementations which minimize the risk of soft failures in the system.

3. Process Design Kit

In this chapter the Process Design Kit developed for the gravure-printed unipolar organic transistors is introduced. At first, the models used to describe the transistor behavior (static, dynamic and noise) are presented. Next, the development of the EDA tools and their integration in the commercial framework Cadence Virtuoso ® is discussed. The PDK is further exploited in the Chapters from 4 to 7 to design the four target system on foil demonstrators.

The contents of this chapter have been published in the DATE conference proceedings [81].

3.1 Introduction

The availability of a reliable Process Design Kit (PDKs) for PE technologies is of paramount importance in order to design complex systems on foils. However, Electronic Design Automation (EDA) tools for printed organic technologies are still in their infancy, negatively affecting the evolution of PE. Only few PDKs have been reported in literature to-date [71][73]. The limited research in this field is due to several reasons. First, the constant evolution of the manufacturing steps during the technology advancement requires a regular adjustments of the PDK, reducing its effectiveness. Second, to enable a meaningful simulation of the large OTFT variability, a labor-intensive statistical characterization of the model parameters is required. At last, the modelling of the time-dependent effects, such as bias stress and aging remains extremely challenging.

In this chapter, a novel PDK is presented, specifically tailored for the gravure-printed organic technology developed at CEA-Liten [74]. One of the primary objectives in the development of the PDK, is to provide a versatile set of EDA tools which allow its rapid adaptation to cope with the advancements of the manufacturing process. In this perspective, a new approach based on the definition of a reduced set of technological key parameters is proposed to reduce the overall time required for the PDK adaptation, improving its effectiveness. In addition, the PDK comprises an exhaustive modelling of the OTFT (static, dynamic, noise and variability), extracted by means of numerical fitting on the electrical characterization data described in [74]. The complete PDK has been integrated in the commercial EDA software Cadence Virtuoso®.

The chapter is further organized as follows: at first the development process of the PDK is introduced in Section 3.2. Next, the transistor modelling (static, dynamic, noise and variability) is presented in Section 3.3. The derivation of the Design Rule Manual (DRM) and the definition of the Parametrized Cells (PCells) is discussed in Section 3.4 and 3.5, respectively. The integration of the PDK in the commercial framework Cadence Virtuoso® and the use of its main EDA tools, is further described in Sections 3.5 and 3.6. Finally, some conclusions are drawn in Section 3.7.

3.2 PDK development process

Process Design Kits are typically developed to assist the circuit design flow, providing a simplified interface to the technology platform. Indeed, the device models (transistors, resistors, capacitors, etc…) included in the PDK are exploited to reproduce the behavior of the physical components, enabling circuit simulations in different domains. PCells are used during the layout phase, in order to automatically generate the geometry of the components according to a reduced set of given parameters, reducing the time required for the design. In this scenario, the use of EDA tools further allows automatic verification of the design at different levels of abstraction, starting from the schematic and reaching the post-layout phase. This becomes crucial as the system complexity approaches already several tens of devices. From this perspective, the availability of tools capable to perform Design Rule Checking (DRC) and Layout Versus Schematic (LVS) comparisons enables to highlight potential design errors and violations, ensuring a flawless design flow. In addition, parasitic effects introduced in the layout phase by the circuit interconnections can be accounted for in post-layout simulations by means of Layout Parasitic Extractions (LPEs).

The strategy exploited to develop the PDK [81] for the gravure-printed unipolar organic technology [74] is schematically shown in Figure 17. STEP 1 focuses on the definition of a reduced set of technological constraints, and in their usage for the derivation of the DRM. This knowledge is further exploited to formalize the technology layer stack (technology files) within the Cadence Virtuoso environment (STEP 2). In addition, PCell components (e.g. OTFTs, capacitors and resistors) are made available at this stage, exploiting the layout guidelines contained in the DRM. Next, EDA validation tools such as DRC and LVS can be enabled, since their development mainly requires insight in the design rules and knowledge of the component PCells (STEP 3).

The PDK developed so far is further exploited to assist the design of a Transistor Evaluation Module (TEM) (STEP 4). This mask set comprises several arrays of devices that can be electrically characterized after fabrication (STEP 5). Hence, the obtained measurement database allows the extraction of suitable models to accurately reproduce in the circuit simulator the electrical behavior of the analyzed devices (STEP 6). Furthermore, parasitic effects associated to the routing strategy employed in the circuit layout, can be estimated at this stage. These results are further embedded in equivalent circuit representations which can be generated by means of LPEs, to simulate the impact of the parasitics on the overall circuit performance (STEP 6).

It is worth mentioning that the overall development process (from STEP1 to STEP 6) requires multiple iterations, each time that the fabrication process is subjected to new adaptations.

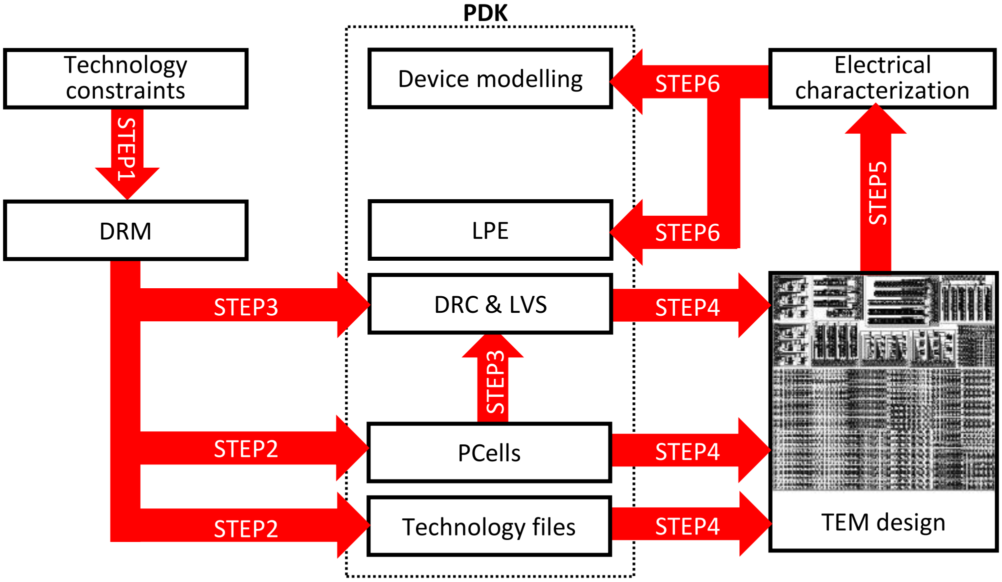


Figure 17. Simplified diagram of the strategy exploited to develop the Process Development Kit for the gravure-printed organic technology.

3.3 OTFT modelling

The availability of an accurate transistor model is a key asset to enable the design of complex analog and mixed signal circuits on foil. The OTFT model described here accounts for both charge transport and carrier injection issues related to the energy barrier at the metal-semiconductor interface. Indeed, despite the use of a staggered OTFT structure, which is beneficial for the carrier injection, the presence of an energy barrier (defined here as contact effect) can still severely impact the performance of analog circuits. In order to enable an accurate OTFT modelling, a specific mask set (TEM) containing several OTFT test structures has been designed. The complete design occupies an area of 126 x 126 mm^2 and comprises about ~1000 OTFTs, featuring L and W scaling, as well as different layout geometries. The TEM has been manufactured with the first generation printed organic technology [74]. The electrical characterizations performed on the structures containing transistors laid-out with TLM geometry and featuring channel lengths ranging from 5 µm to 800 µm (presented already in Section 2.3), have been further used to develop the static OTFT model. After the introduction of the yield-optimized fabrication process, the model parameters have been tuned in order to account for the different behavior of the transistors. In addition, the results of the parameter variability analysis (Section 2.5) have been also included in the static model of the transistor. Finally, models for the dynamic and noise behavior of the OTFTs have been extracted based on measurements of devices and circuits manufactured with the final version of the fabrication process.

3.3.1 Static model

The electrical characteristics of the fabricated OTFTs [74] are reproduced by means of a physical-based analytical model developed by F. Torricelli[1] [75]. The charge transport in the channel is based on a Variable Range Hopping (VRH) transport in a Density of States (DOS) [82]. The DOS is described by a double-exponential function accounting for both deep and tail states [83][84]. In the case of p-type OTFTs, the tail states are located at energies close to the Highest Occupied Molecular Orbital energy level (HOMO) and define the strong accumulation region of operation, while the deep states are located at energies far from the HOMO level and define the subthreshold operation. Since in OTFTs the gate voltage controls the position of the Fermi energy level through the DOS, it is important to account for both deep and tail states in order to provide a unified and accurate OTFT description in all regimes of operation. Following the same approach proposed in [84], the drain current expression due to charge transport into the channel reads for a p-type transistor (1):

$$\mathrm{I_{SD}} = \frac{\mathrm{W}}{\mathrm{L}} \mathrm{K_0}\left(\psi_{\mathrm{SG}}^{\gamma} - \psi_{\mathrm{DG}}^{\gamma}\right) \tag{1}$$

where W and L are the OTFT channel width and length, respectively, K_0 is a pre-factor dependent on physical and geometrical parameters (temperature, energetic disorder, charge spatial localization, and gate-insulator capacitance), $\gamma = 2T_t/T$ is the normalized tail-states energy disorder, and Ψ_{XG} is defined as (2):

$$\psi_{\mathrm{XG}} = \xi\, \mathrm{V_T}\, \mathrm{F}\left[\frac{\mathrm{V_X + V_{TH} - V_G}}{\xi\, \mathrm{V_T}}\right] \tag{2}$$

with

$$\mathrm{F}[\,.\,] = \log\left[1 + e^{(.)}\right] \tag{3}$$

$$\xi = \frac{\gamma^2}{\gamma - 1}\left(1 + \frac{qN_d}{C_I}\right) \tag{4}$$

where C_I is the gate insulator capacitance per unit area, N_d is the total density of deep states per unit surface, V_G, V_D, and V_S are the gate, drain, and source voltages, respectively, V_{TH} is the threshold voltage, $V_T = k_BT/q$ is the thermal voltage, K_B is the Boltzmann constant, q is the elementary charge, and X can be either S or D. Then, according to [82], the channel length modulation and the off-current are included in the drain current model as follows (5):

$$\mathrm{I_{SD}} = \frac{\mathrm{W}}{\mathrm{L}}\left[\mathrm{K_0}\left(\psi_{\mathrm{SG}}^{\gamma} - \psi_{\mathrm{DG}}^{\gamma}\right)\left(1 + \frac{\mathrm{V_{SG} - V_{DG}}}{\mathrm{L\, E_{SAT}}}\right) + \frac{\mathrm{W}}{\mathrm{L}}\frac{\mathrm{(V_{SG} - V_{DG})}}{\mathrm{R_{OFF}}}\right] \tag{5}$$

where E_{sat} is the maximum electric field at the drain side when the OTFT is operated in saturation (i.e. $V_D<V_G-V_{TH}$), and R_{OFF} accounts for the bulk current due to unintentional

---

[1] Fabrizio Torricelli, University of Brescia, Brescia, Italy.

doping of the organic semiconductor (OSC). The model parameters are calculated by fitting the measured transfer characteristic of long-channel OTFTs (L = 800 µm) at $V_{DS} = -0.1$ V with the method reported in [83][84]. The extracted channel model parameters are listed in Table 4.

Table 4. Extracted channel model parameters.

Electrical parameter	Symbol	Value	Unit
Temperature	T	295	[K]
Dielectric capacitance per unit area	C_I	3.7	[nF/cm^2]
Normalized tail-states energy disorder	γ	2.07	-
Threshold voltage	V_{TH}	-3.04	[V]
Total density of deep states per unit area	N_d	2×10^{11}	[cm^{-2}/eV]
Current pre-factor	K_0	1.66×10^{-9}	[A/V$^{\gamma}$]
Off-resistance per unit area	R_{OFF}	2×10^{12}	[Ω/µm^2]
Max. electric field at drain in saturation regime	E_{SAT}	3.6	[V/µm]

Moreover, transistors with channel lengths ranging from 800 µm to 5 µm are evaluated. It is worth mentioning that transistors with a channel length L= 5 µm can be manufactured with the fabrication process described in Chapter 2. However, these geometries exceed the minimum feature size defined for the S/D layer, leading to a large number of defects (S/D shorts) already at the first level of the technology layer stack. The model accurately reproduces the measurements for channel lengths down to 40 µm, while a significant error occurs for shorter channel lengths. This can be ascribed to contact effects [86][87] as confirmed by plotting the L-normalized drain current as a function of channel length. Indeed, the normalized current of short channel transistors is lower than for long-channel devices. According to the analysis presented in [86]-[88], the contact resistance can be ascribed to the limited charge injection at the source contact due to a reversed biased Schottky barrier. At low drain voltages the energy barrier at the metal-semiconductor interface results in a reduced charge accumulation close to the contact region (defined by a length $L_c \approx 1$ µm) while at large V_{SD} a full depletion region from the source edge to the channel is obtained. This behavior resembles a transistor operating in saturation.

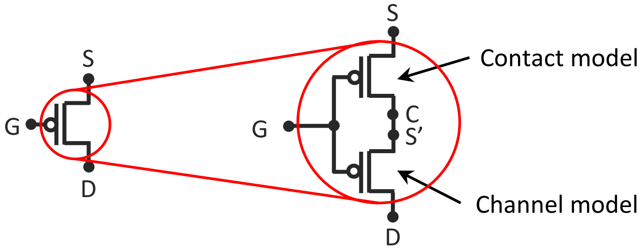


Figure 18. P-type OTFT symbol and its internal static model schematization.

Therefore, we model the contact effects as a transistor with a channel length equal to the contact region L_C, a threshold voltage V_{TC} and electric field E_{SC} (Figure 18) that accounts for the gate-dependent Schottky barrier lowering (6-7):

$$I_C = \frac{W}{L_C} K_C\left(\varphi_{SG}^{\gamma} - \varphi_{CG}^{\gamma}\right)\left(1 + \frac{V_{SG} - V_{CG}}{L_C E_{SC}}\right) \tag{6}$$

$$\varphi_{XG} = \xi V_T F\left[\frac{V_X + V_{TC} - V_G}{\xi V_T}\right] \tag{7}$$

where V_C is the voltage drop at the injecting contact. The electrical characteristics of the OTFTs are modeled as the series of the channel model (2-5) and contact model (6-7). In order to obtain the contact model parameters (i.e. K_C, V_{TC}, E_{SC}) we calculate the contact characteristics by solving, for each set of I_D, V_G and V_D the equation (8):

$$I_{SD}^{meas}(V_G, V_D, V_S) - I_{SD}^{Eq.1}(V_G, V_D, V_S') = 0 \tag{8}$$

where $V_{S'} = V_S - V_C$, and V_C can be calculated by numerically solving (8). By fitting the extracted contact characteristics with the contact model (6-7) we found that V_{TC} can be described with a second-order polynomial function (9)

$$V_{TC} = -[4.5\ 10^{-3}(V_S - V_G)^2 + 0.71(V_S - V_G) + 0.96] \tag{9}$$

and E_{SC}

$$E_{SC} = \frac{0.85 * 20}{|V_S - V_G| + \alpha} \tag{10}$$

where $K_c = 1.1\ 10^{-8}\ A/V^{\gamma}$ and α is an arbitrary small positive constant introduced to avoid singularity in the E_{SC} parameter. The overall model, i.e. the channel model combined with the contact model, is validated in Figure 19 and Figure 20. It accurately predicts (within 10% error) the transfer and output characteristics of short-channel (L = 5 µm) as well as long channel (L = 800 µm) OTFTs with the very same set of physical parameters. The model parameters have been further adjusted after the yield-optimized fabrication process has been introduced.

The transistor model has been coded in VerilogA and integrated in the Cadence Virtuoso® environment. In addition, Monte Carlo simulations have been enabled at this stage, in order to assess the circuit performance in presence of within-foil variability (described as device-to-device mismatch) and foil-to-foil variability (defined as process variation). In this perspective, the current prefactor K_0 as been redefined as (11)

$$K_0 = k_0 \beta \tag{11}$$

where k_0 is a scaling factor and β is the current prefactor defined in Section 2.5. Both forms of variability have been represented here with different statistical distributions of the parameters β and V_{TH}. More in detail, the within-foil variability is modelled in the simulator using Gaussian distributions for β and V_{TH}, having respectively mean values $\overline{\beta}$ and $\overline{V}_{TH}$, associated to the proposed static OTFT model, and standard deviations extracted from Figure 16. As previously mentioned, since these standard deviations assume different values according to the transistor channel length, two arbitrary fitting functions have been defined to reproduce these trends on the circuit simulator respectively given by (12-13):

$$\sigma(\beta - \bar{\beta}, L) = 1.01\ 10^{-7}(L)^2 + 2.01\ 10^{-5}(L) + 0.07 \tag{12}$$

$$\sigma(V_{TH} - \bar{V}_{TH}, L) = 0.96e^{-0.09L} + 0.19e^{2L10^{-3}} \tag{13}$$

Likewise, the foil-to-foil variability is reproduced in the circuit simulator using independent Gaussian distributions of β and V_{TH}, with the parameters as listed in Table 3.

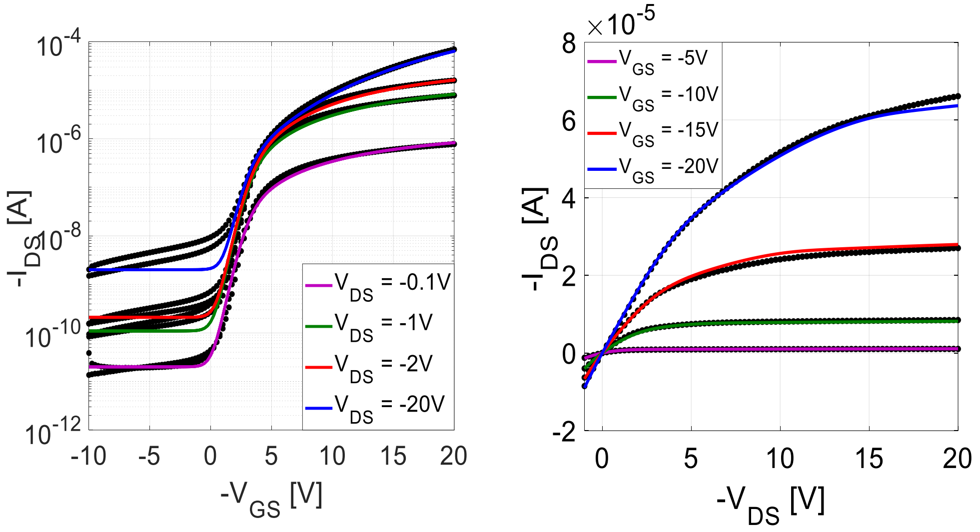


Figure 19. Measured (black points) and modelled (lines) transfer (a) and output (b) characteristics of an OTFT featuring W = 1000 µm, L = 5 µm.

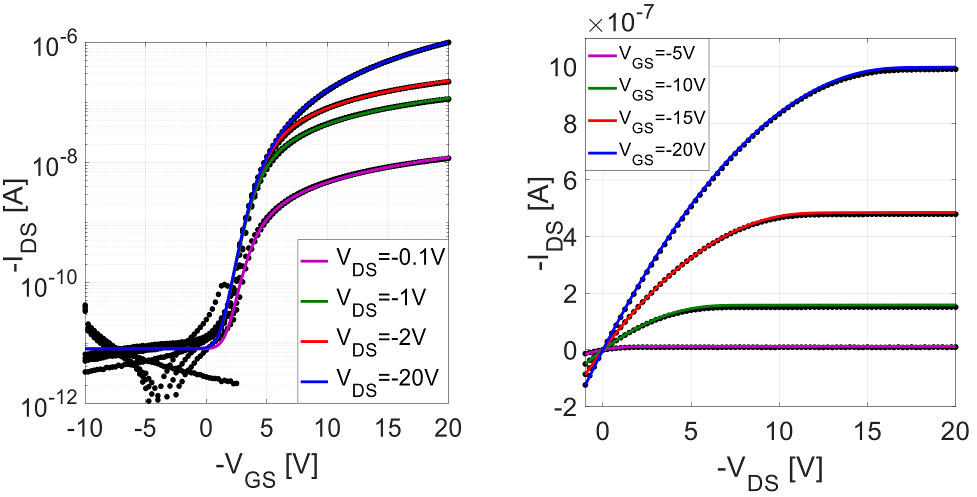


Figure 20. Measured (black points) and modelled (lines) transfer and output characteristics of an OTFT featuring W = 1000 µm, L = 800 µm.

3.3.2 Dynamic model

The dynamic performance of the transistor is a fundamental design constraint in analog and digital circuits. The achievable speed in a circuit is mainly limited by the device parasitic capacitances. These capacitances become even more relevant in the case of printed organic transistors. Indeed, the printing resolution and the control of the overlay are typically in the order of ~µm (Table 1) and thus comparable with the OTFT channel length. As a consequence, the layout geometry of the transistors needs to ensure sufficient overlay margins for each layer stack, leading to relatively large device parasitics.

The proposed dynamic model of the transistor is directly obtained from the static one, by adding the device parasitic capacitances C_{GS} and C_{GD} according to Figure 21. In order to enable this description, the intrinsic capacitances of the transistor have been characterized at different bias operating conditions. The measurement setup consists of an OTFT connected with probe needles and coax cables to a discrete Si Trans-Impedance Amplifier (TIA). The DC and AC currents provided by the organic transistor are translated into voltage by the TIA (Figure 22) and fed to the HP35670A Dynamic Signal Analyzer in order to measure the frequency response. A 10 pF ± 0.01% discrete capacitor C_{CAL} has been introduced to reduce the frequency span of the analysis, accommodating it to the frequency range of the Dynamic Signal Analyzer. In order to investigate the bias dependency of the parasitic capacitances, multiple frequency sweeps have been recorded at different polarization conditions.

This current approach has been preferred to a direct admittance measurement employed in [89], due to the sensitivity of the results to the stray capacitances associated to the measurement setup.

The frequency response of the circuit is analytically derived from the inspection of the small-signal circuit model in Figure 22.

$$-\frac{v_{out}}{R_{FB}} = \frac{i_{TFT}}{v_{in}} = -g_m + j\omega(C_{GX} + C_{CAL}) \tag{14}$$

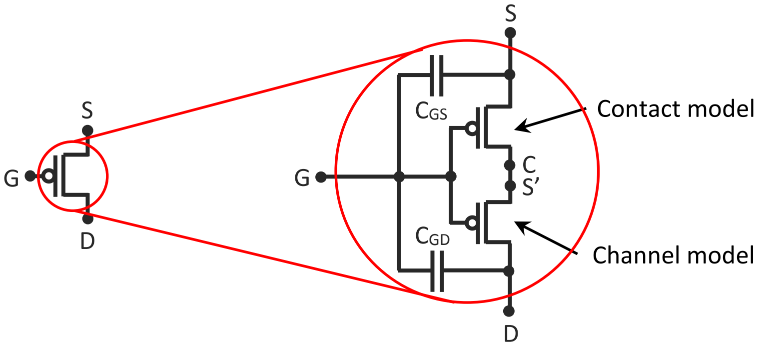


Figure 21. P-type OTFT symbol and its internal dynamic model schematization.

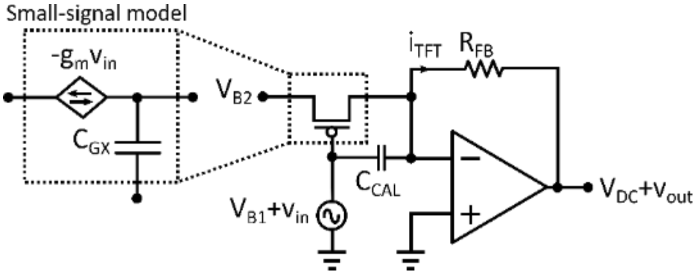


Figure 22. Simplified schematic of the parasitic capacitance measurement setup.

Where g_m is the small-signal transconductance and C_{GX} is the parasitic capacitance between gate and drain (or source according to the bias condition of the transistor). Next, each measured frequency sweep has been approximated with a first-order polynomial fitting and the parasitic capacitance value estimated from the fit. The extracted C-V curves for both C_{GD} and $C_{GS}$are shown in Figure 23.

The measurement results show different behavior for the parasitic capacitances C_{GD} and C_{GS} with the respect to the transistor operation regions. Both parasitic capacitances reach their minimum value when the transistor operates in off-region (Figure 23). Indeed, since the semiconductor is not yet accumulated only the physical overlaps between source/drain and gate electrodes contribute to the capacitance value (Figure 24(b)). As the operating condition of the OTFT reaches the saturation region (V_{SD}>V_{SG}+V_{TH}), the parasitic capacitances partition asymmetrically between C_{GD} and C_{GS}. In this scenario, C_{GD} assumes a value nearly equal to half of the channel capacitance, while C_{GS} exhibits a larger value due to the accumulated semiconductor area in the neighborhood of the source electrode (Figure 24(c)). Finally, in the linear region of operation, the values of both parasitic capacitances rise, due to the increasing

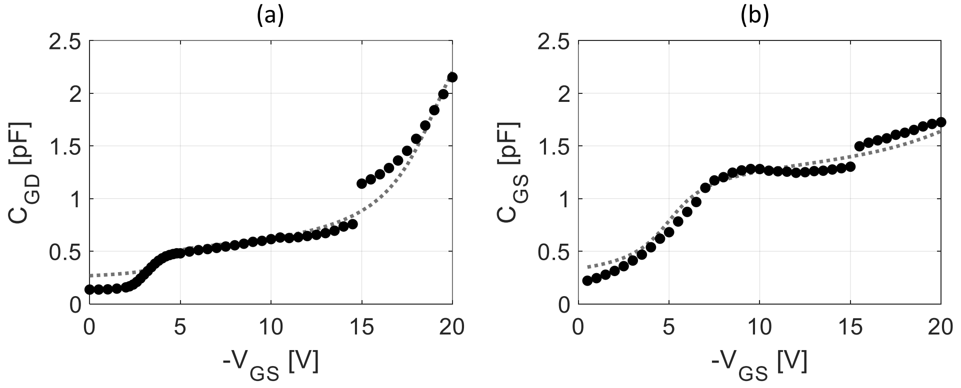


Figure 23. Extracted (black points) and modelled (grey dashed) C_{GD} (a) and C_{GS} (b) capacitances, for different transistor bias conditions. The C-V curves are measured from an OTFT featuring W=500µm, L=80µm, number of fingers NF=1 and C_I=2.6nF/cm^2. Measurements are performed at V_{DS}=-15V.

accumulation degree of the overall semiconductor area (Figure 24(d)). In this case, the parasitic capacitances contributions are determined by the overlap between the gate electrode and the entire semiconductor pad rather than the transistor channel area only. Indeed, this is related to the chosen OTFT layout geometry, in which the OSC is completely enclosed inside the gate electrodes as shown in Figure 24(a). Despite the introduction of larger parasitic capacitances, this layout strategy allows the minimization of potential leakage current paths connecting the source and drain electrodes through the semiconductor, leading to a better control of the transistor off-current.

It should be mentioned here that both C_{DG} and C_{GS} curves presented in in Figure 23 exhibit trend discontinuities for $|V_{GS}|$ approximately equal to 15V. These effects can be ascribed to the bias stress associated to the continuous operation of the transistor during the measurements. Thus, the trend discontinuities occur after the power-off of the measurement setup, required to modify the bias configuration of the transistor between saturation and linear region of operation.

An empirical formula has been used together with numerical data fitting to approximate the parasitic capacitance trends for the different bias conditions, and to scale the parasitics with the device size and number of fingers NF (in multi-finger devices), leading to Equations 15(a-d):

$$C_{GX} = C_{GX1} + C_{GX2} + C_{GX3} \tag{15a}$$

$$C_{GX1} = \begin{cases} \left(\left\lfloor \frac{NF}{2} \right\rfloor + 1\right)\left(\frac{W}{NF} + L_{OV}\right) F_W C_I & \text{for } X=S \\ \left\lceil \frac{NF}{2} \right\rceil \left(\frac{W}{NF} + L_{OV}\right) F_W C_I & \text{for } X=D \end{cases} \tag{15b}$$

$$C_{GX2} = \alpha_{1X}(0.5WLC_I - C_{GX1})\left(\frac{2}{\pi}\text{atan}([V_S - V_G + V_{TH}]\alpha_{2X}) + 1\right) \tag{15c}$$

$$C_{GX3} = \alpha_{3X}(0.5A_{OSC}C_I - \alpha_{1X}0.5WLC_I - C_{GX1})\left(\frac{2}{\pi}\text{atan}([-V_G + V_{TH} - V_D]\alpha_{4X}) + 1\right) \tag{15d}$$

Where F_W is the finger width, L_{OL} is the interconnection overlap per unit length between drain (source) and gate electrodes, A_{OSC} is the total semiconductor area and α_{1X}, α_{2X}, α_{3X}, α_{4X} are fitting parameters. This dynamic OTFT model has been coded in VerilogA and integrated together with the static model in Cadence Virtuoso®.

In this perspective, it should be highlighted that the use of the atan() function in Equations 15(c-d) allows to reproduce the values of C_{GX} at the different bias conditions without introducing discontinuities, preventing convergence issues in the circuit simulator. For the sake of completeness, all the fitting parameters used for the modelling of C_{GD} and C_{GS} are listed in Table 5.

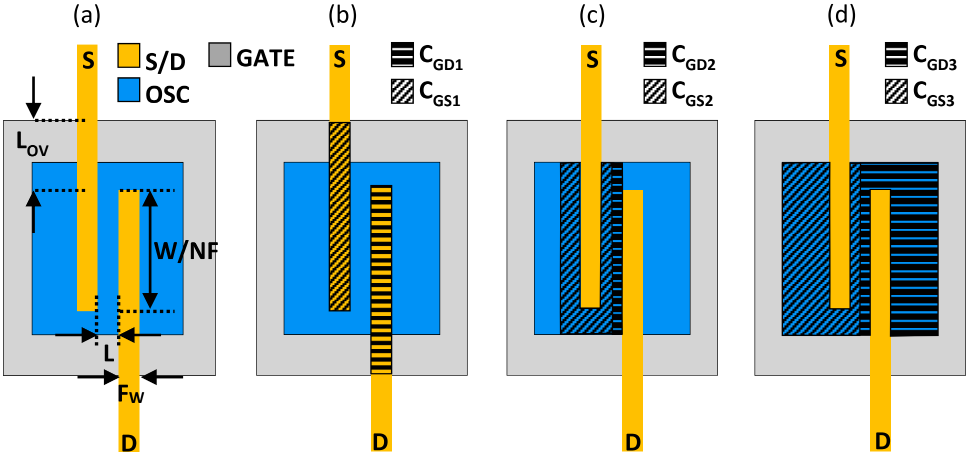


Figure 24. (a) Layout of a generic OTFT with NF=1. (b) Parasitic capacitance contributions C_{GS1} and C_{GD1} introduced by the physical overlap between S/D and GATE electrodes. (c) Parasitic capacitance contributions C_{GS2} and C_{GD2} related to the transistor channel accumulation in saturation region. (d) Partitioning of the parasitic capacitances (C_{GS3} and C_{GD3}) for a transistor operating in linear region.

Table 5. List of fitting parameters used in the proposed dynamic model of the transistor.

Parasitic capacitance C_{GX}	α_{1X}	α_{2X}	α_{3X}	α_{4X}
C_{GD}	0.33	2.01	0.52	0.42
C_{GS}	1.43	0.60	0.34	0.21

3.3.3 Noise model

The noise behavior of field effect transistors is generally modelled with two current contributions I_{nT}^2 and I_{nF}^2, which are related to the thermal and flicker noise, respectively. According to [90], the Power Spectral Density associated to the thermal noise contribution can be estimated from Equation (16):

$$S_{TID} = 4k_B T(2/3g_m) \tag{16}$$

Where k_B is the Boltzmann constant, T is the temperature, and g_m is the transconductance of the transistor. The latter can be obtained as analytical differentiation $\partial I_{SD}/\ \partial V_{SG}$, where I_{SD} is expressed by Equation (5). The resulting formula is given by (17):

$$g_m = K_0 \frac{W}{L} (\xi\, V_T)^{\gamma-1} \gamma \frac{e^{\left(\frac{V_{SG}+V_{TH}}{\xi\, V_T}\right)}}{1+e^{\left(\frac{V_{SG}+V_{TH}}{\xi\, V_T}\right)}} \left[\ln\left(1+e^{\left(\frac{V_{SG}+V_{TH}}{\xi\, V_T}\right)}\right)\right]^{\gamma-1} \tag{17}$$

This formula allows the estimation of g_m in both transistor operating conditions, namely below ($V_{SG} < -V_{TH}$) and above threshold ($V_{SG} > -V_{TH}$). It can be demonstrated that in the former case the Equation (17) reduces to (18),

$$g_{m_{below}} \cong K_0 \frac{W}{L} (\xi\, V_T)^{\gamma-1} \gamma \left[e^{\left(\frac{V_{SG}+V_{TH}}{\xi\, V_T}\right)}\right]^{\gamma-1} \tag{18}$$

while in the latter, the g_m expression becomes (19):

$$g_{m_{above}} \cong K_0 \frac{W}{L} \gamma (V_{SG} + V_{TH})^{\gamma-1} = \gamma \frac{I_{SD}}{V_{SG}+V_{TH}} \tag{19}$$

However, the noise performance in OTFTs is typically dominated mainly by Low-Frequency Noise (LFN). Due to the modest transistor f_T, the LFN contribution is dominant compared to the thermal one. According to [91], the low-frequency noise (also known as 1/f or flicker noise) in polymer thin-film transistor can be described by the mobility fluctuation theory. The expression of the LFN Power Spectral Density (PSD) can be derived using the phenomenological Hooge equation [92][93] and assuming VRH charge transport in the organic semiconductor [63]. In this case, the PSD can be expressed as (20) [63]:

$$S_{FID} = \frac{q\alpha_H I_{SD}^2}{fWLC_I(V_{SG}+V_{TH})} \tag{20}$$

Where f is the frequency, q is the elementary charge and α_H is the Hooge parameter. Noise measurements performed on different circuit architectures have been used to empirically estimate the value of α_H, which is for this technology equal to 0.2.

3.4 Design Rule Manual (DRM)

The design rules are geometrical restrictions used to guide the correct implementation of the circuit layout. These are typically derived from the manufacturing constraints of the technology, and therefore are process dependent. Indeed, the use of new inks or improvements in the printing process often require a redefinition of the design rules.

The reduction of fabrication costs is one of the main objectives in PE. This can be achieved by employing more aggressive design rules which maximize the device integration density, thus minimizing the circuit area occupation. This strategy typically leads as well to the reduction of the parasitic effects, which positively impacts transistor speed. However, these benefits might be obtained at the expense of a lower device yield. Therefore, a trade-off between integration density/transistor speed and yield performance is typically observed.

For these reasons, the formalization of the design rules has a crucial role in the development of the PDK. In this perspective, a reduced set of technological constraints $C_{\#}$ are used here to derive the design rules manual.

- C1 – Layer resolution: defined as the minimum feature size that can be developed on each layer.
- C2 – Layer registration: it refers to the capability of controlling the overlay during the layer printing (Table 1).
- C3 – Pattern overflow: provides an estimation of the edge roughness, introduced by the ink displacement from the nominal design position (Table 1).
- C4 – Safety margin: this parameter is expressed in multiples of C1 and can be used to obtain more conservative design rules.

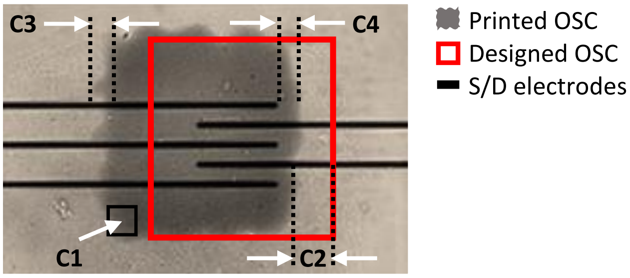


Figure 25. Bottom view of an OTFT fabricated up to the OSC layer. Technological constraints $C_{\#}$ highlighted on the OSC layer. (C1) Minimum layer resolution, corresponding to the writing resolution of the engraved cells. (C2) Maximum pattern misalignment, quantified as displacement of the printed pattern (grey square) from the designed pattern (red square). (C3) Maximum edge roughness. (C4) Safe margin which ensures the overlap of the OSC pattern over the S/D contacts, in presence of layer misalignment.

The optical characterization of a statistically meaningful number of test structures contained in the Process Evaluation Module (PEM) mask set has been used to estimate the values of technological constraints $C_\#$ for this technology.

Similarly to the approach proposed in [94] the formalization of the design rules is further organized according to the three following categories:

- Single-layer rules: define geometrical restrictions limited to shapes belonging to the same layer. For instance, minimum width and minimum spacing rules (Figure 26) are part of this category.
- Two-layer rules: regulate the interaction between shapes placed on two different layers. Distance, overlap and enclosure rules (Figure 26) belong to this group.
- Multi-layer rules: are two-layer rules only valid within a restricted area, which is obtained as logical combination of several layers. Multi-layer rules are used to define transistors and Metal-Semiconductor-Insulator-Metal (MSIM) capacitors.

It is important to remark that all the design rules formalized in the DRM make use of the C1-C4 constraints only. This enables parametric control of the layout geometries as well as rapid adaptation of the design rules with feature size downscaling.

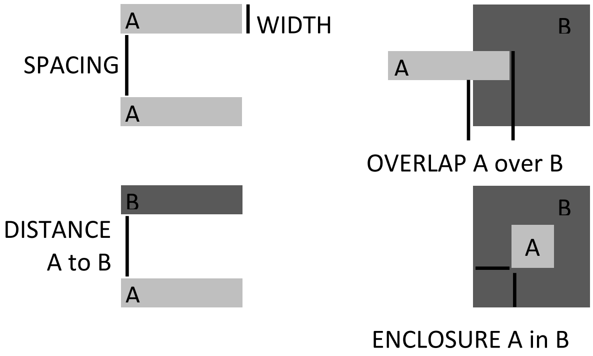


Figure 26. Set of geometrical restrictions used to define design rules.

3.5 Parametrized Cells (PCells)

Parametrized cells have been designed to automatically generate the layout geometry of resistors, capacitors and transistors according to the master cell in which a set of parameters is given. This facilitates the design process during the layout stage, reducing the development time and the risk of design rule violations. Furthermore, the layouts of the PCells are fully adaptive with respect to the C1-C4 parameters. All PCells have been generated and integrated in the CAD framework by means of SKILL® scripts.

The high-resolution photolithography process used to develop the source/drain metal layer can be exploited for the fabrication of resistors with compact footprints. However, due to the relatively low sheet resistance of that layer (~1Ω/sq), only resistance values in the order of kΩ can be manufactured with reasonable yield. The proposed PCell enables the generation of a serpentine fashion layout according to four parameters: resistance value, segment width WR, length LR and spacing SR. The second metal layer (GATE) could be also exploited to fabricate resistors. Indeed, thanks to the higher sheet resistance (~100Ω/sq), larger resistance values could be achieved. However, the lower printing resolution (Table 1) together with the large edge roughness, negatively impact the resistor footprint as well its accuracy, therefore limiting the use of these devices. Metal-Insulator-Metal (MIM) capacitors can be obtained from the overlap of the two metal layers. Metal-Semiconductor-Insulator-Metal (MSIM) non-linear capacitors are also available. The PCells enable the automatic generation of the layout geometry, given the nominal capacitance value. Finally, the OTFT master cell (Figure 27(a)), has been parametrized according to a set of five main parameters, which are: channel width W and length L (Figure 27(b)), number of fingers NF (Figure 27(c)), vertical kv and horizontal kh overlap margins (Figure 27(d)).

It is worth noticing that the technological constraints C1-C4 are also included in all the component master cells as parameters, in order to improve the versatility of the PCells and thus the effectiveness of the PDK.

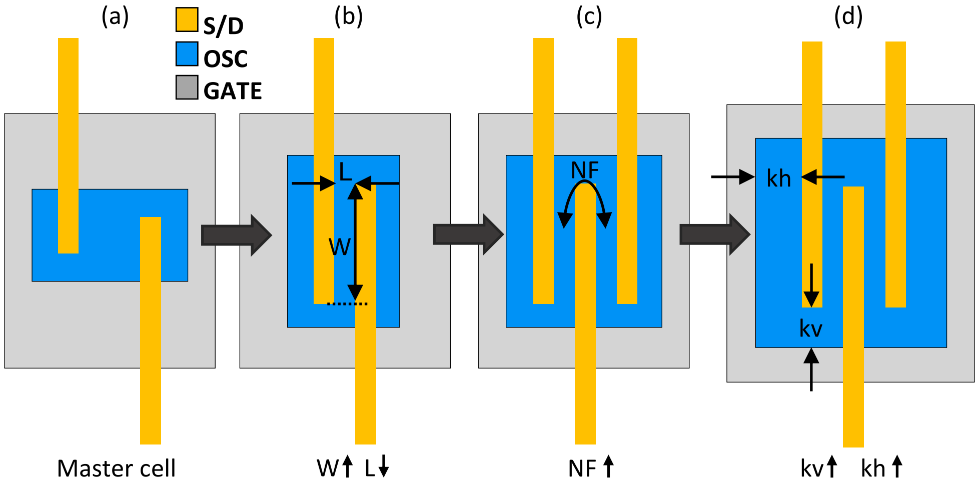


Figure 27. (a) OTFT master cell. (b) OTFT layout parametrized according to W and L. (c) Multi-finger transistor layout obtained for NF=2. (d) Transistor layout with larger OSC/(S/D) overlap margins.

3.6 PDK integration with Cadence Virtuoso® EDA tools

The developed PDK has been further coupled with the Assura™ Diva® EDA tools, provided in Cadence Virtuoso®. Diva® is a set of verification tools belonging to the Assura family, which can be exploited to support the system development along the design flow. Indeed, this set of verification tools is capable to perform physical design checks together with layout versus schematic comparisons. These further allow to find errors and design violations at an early stage during the design process, providing interactive insights to speed up the error diagnosis and correction.

In the perspective of developing complex systems-on-foil, the use of at least three EDA tools is required during the design flow, namely Design Rule Checking (DRC), Layout Versus Schematics (LVS) and layout parasitic extraction (LPE)

3.6.1 Design Rule Checking

The DRC is an interactive EDA tool used to automatically highlight potential violations of the design rules at the circuit layout stage. The proposed PDK exploits the design rule checker provided in the DIVA® software, part of the Cadence® framework. However, the verifications rule file is here required. This has been created by implementing in SKILL® language the design rules already formalized in the DRM.

3.6.2 Layout Versus Schematics

The Layout Versus Schematic tool provided in the DIVA® software has been utilized here for logic comparison between netlists. Given the schematic and layout netlists, the program provides the results of the comparison, according to the directives specified in the LVS rules file. For the scope of the proposed PDK, several features have been included in this file.

The logical matching of the two netlists is not sufficient to prevent errors in the layout design phase. Indeed, device properties must be also checked. This is applied here only on devices such as resistors, capacitors and transistors, for which their respective parameters (resistance, capacitance, W and L) are compared. In case of parameter mismatch between the netlists, a warning message is provided. During the layout phase, the use of the series/parallel interconnection of multiple instances of the same device could be preferred to the placement of a single equivalent components. However, if the same approach is not adopted in the schematic, the netlist comparison fails. A specific functionality has been implemented here to reduce multiple interconnected instances (resistors, capacitors and OTFTs) into a single equivalent component in which the related parameters (Resistance, capacitance, W and L) are adjusted accordingly.

Before an LVS comparison can take place, both the schematic and layout netlists need to be generated. While the former can be automatically generated from the circuit schematic, the latter needs to be extracted from the layout. In order to enable this, a specific EXT rule file has been developed and provided to the software.

3.6.3 Layout Parasitic Extraction

The layout parasitic extraction is performed using the LPE tool, also provided by DIVA®. Similarly to the layout netlist extraction procedure, an additional rule file is here required. The devices defined in the layout with intentional masks (on the virtual layers) are not recognized as potential parasitics and therefore extracted as regular components. A parasitic capacitor is instead extracted each time that an overlap between the two metal layers occurs. The capacitance value is estimated as $A_{OV} C_I$, where A_{OV} is the area of the overlap and C_I the capacitance per unit area. Fringing effects are neglected. Parasitic resistors account for the resistive effects introduced by the routing lines.

The availability of parasitic devices in the extracted netlist enables the possibility to perform post-layout simulations. Indeed, parasitic effects become more and more relevant as PE circuits are manufactured over larger areas.

3.7 Conclusions

In this chapter, the PDK developed for the printed unipolar organic technology has been presented. The proposed PDK includes for the first time in literature a thorough description of the static, dynamic and noise behavior of the OTFT technology. More specifically, for the description of the static transistor behavior, a physical-based analytical model has been developed which exploits the Variable Range Hopping in a Density of States to describe the charge transport in the organic semiconductors. Furthermore, a basic description of the parameter variability of the transistors is included in the static model. This allows to reproduce the effect of within-foil and foil-to-foil variability of the devices in the circuit simulator. This permits to select circuit architectures which are more resilient to the parameter spread, reducing the probability of soft failures in the overall system. Even though this approach improves the trustworthiness of the design flow, further investigations are required to develop a comprehensive study of the sources of variabilities and quantify rigorously global and local device parameter variations.

In order to analyze the dynamic behavior of the OTFT, its parasitic capacitances have been experimentally characterized. An empirical formula has been further defined and fitted to the measurement results to reproduce the dynamic behavior of the transistor. The noise model comprises two contributions, namely thermal noise and LFN, where the latter is typically dominant across the entire OTFT frequency range of operation. An accurate modeling of the device noise performance is crucial in the design of Analog Front-Ends (AFEs) for sensor interface applications, or more in general in Analog Mixed Signal (AMS) systems.

In the perspective of designing complex systems-on-foil, the availability of a PDK which comprises EDA tools for the design flow verification is of paramount importance. However, EDA tools can only be enabled if design rules are defined first. Thus, the formalization of the Design Rule Manual plays a crucial role in the development of the PDK. The strategy proposed in this chapter exploits a reduced set of four technological constraints to derive the DRM. This very same set of constraints are further used to build the component PCells and enable EDA tools for design verification such as DRC, LVS and LPE in a commercial CAD framework. The proposed approach allows to develop the PDK in a bottom-up fashion, starting from the printing manufacturing process and connecting hierarchically all the modules required in the design flow. This increases the versatility of the PDK, while ensuring its rapid adaptation to advancements in the fabrication process.

4. Multi-Stage Organic Line Drivers

In this chapter multi-stage line drivers for matrix addressing applications have been designed and fabricated with the gravure-printed unipolar organic transistors technology. Different transistor-level implementations for the single delay stage have been proposed and the circuit performance is compared by means of simulations. Three typologies of 8-stage organic line drivers have been developed exploiting the proposed delay stages. Measurement results have been further used to provide insight in the yield performance of each line driver architecture, and to select the most robust circuit implementation in the given OTFT technology.

Parts of this chapter have been published in the IEEE Electron Device Letters [75].

4.1 Introduction

Recent advances in the Printed Electronics have brought the attention on organic technologies as potential candidate for the massive production of inexpensive mechanically flexible devices. This could complement the mean-stream silicon technology to enable innovative solutions in the Internet of Things (IoT) market, such as smart sensor arrays or disposable intelligent labels. The architecture of an intelligent label typically comprises a display, row and column drivers, data and timing controllers and a power management unit (Figure 28). Traditionally, row and column drivers are fabricated in silicon mainstream technologies. However, the new capability of manufacturing printed driving circuits is relevant from the application point of view, in order to achieve an overall system cost reduction. Indeed, the integration of the line addressing circuits in fully-printed organic electronic backplanes for active-matrix solutions such as OLED or electrophoretic displays [95][96] and sensing surfaces [97][98], allows to minimize the number of interconnections with the Si-readout electronics, reducing the overall system footprint together with its cost.

The current state-of-the-art counts only few Organic Line Driver (OLD) circuits manufactured with p-type [44],[99] and complementary [47],[100] organic technologies, mainly fabricated with photo-lithography processes. As line driver architectures are typically demanding in terms of circuit complexity, requiring large area and a considerable number of devices, they are less suitable for printed technologies which intrinsically exhibit modest yield performance. In addition, the design of robust digital logics and delay stages with unipolar transistors is extremely challenging due to the large parameter variability and the reduced noise margin of the conventional inverters [101]. Strategies to mitigate these challenges exploiting dual gate devices [46], complementary logic gates [51],[53] or improved inverter architectures [39],[101] have been already demonstrated. However, dual gate devices are typically not available in printed organic technologies while the fabrication of complementary transistors requires more complex manufacturing processes, which typically achieve lower yield performance.

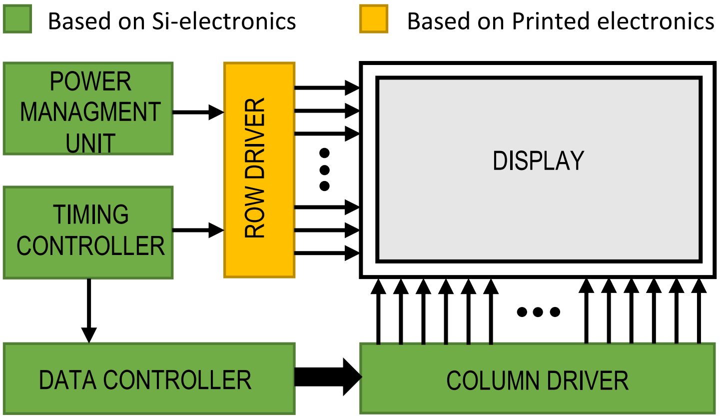


Figure 28. Simplified block diagram of an intelligent label architecture.

Even the use of improved inverter configurations still suffer from several limitations. Pseudo-CMOS inverters [101] and conventional inverters used together with level shifters [39],[101] can be employed to improve the logic gate noise margin, but at the expenses of higher transistor count and additional supply of bias voltages. Besides, the gain that can be achieved with these inverters remains limited by the gain performance of the conventional core inverter. Due to these challenges, multi-stage organic line drivers manufactured with printed organic technologies have not been reported in literature yet, to the best of or knowledge. In order to further assess the potential of the proposed gravure-printed organic technology [75] to bridge this gap, novel organic line driver architectures have been designed, manufactured and characterized in this work.

The Chapter is further organized as follows: an overview of the main unipolar inverter architectures is provided in Section 4.2. The design of several single delay stages is presented and their performance compared in Section 4.3. Next, the design and the experimental characterization of three different 8-stage organic line drivers are discussed in Section 4.4. Finally, conclusions are drawn in Section 4.5.

4.2 Unipolar inverter gate logic

Various inverter topologies have been proposed in literature to address the design challenges of logic gates with unipolar technologies. In this section, a brief summary of the major inverter architectures depicted in Figure 29 is provided, and the simulated performance of the different configurations is compared in Table 6. The behavior of static inverters is compared using the following parameters: the minimum V_{OL} and maximum V_{OH} output voltage, the switching threshold voltage V_M (simply defined as inverter trip point) [102], the input voltages V_{IH} and V_{IL} at which the DC gain of the inverter reduces to -1V/V [102] and the noise margin values N_{MH} and N_{ML} defined according to [102]. The inverter dynamic performance is evaluated instead by means of the AC in-band small signal gain, the rise time T_{RISE} and fall time T_{FALL} (computed from 10% to 90% of the output final value), the propagation delay T_{pHL} (T_{pLH}) associated to a high-to-low (or low-to-high) output voltage transition (computed at the 50% transition points of the input and output signals) [102], the average propagation delay T_p, the average power consumption P_W and the Figure-of-Merit (FOM) expressed by the Energy-Delay Product (EDP). For the sake of completeness, the circuit simulations are performed for all the inverters with an input clock signal swinging from V_{DD} to V_{SS} at a frequency of 1Hz, supply voltages of V_{DD}=18V, V_{SS}=-18V, and an output loading capacitance of 5pF.

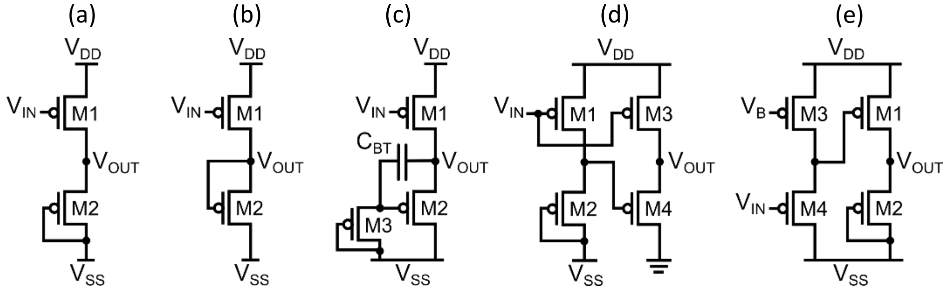


Figure 29. Various inverter topologies designed with unipolar transistors only. (a) Diode-connected inverter, (b) zero-V_{GS} inverter, (c) bootstrap inverter, (d) pseudo-CMOS inverter and (e) diode-connected inverter with level shifter.

Diode-Connected Inverter (DCI): it is widely used in literature [101] and it exploits a diode-connected transistor as load (Figure 29(a)). In order to guarantee the correct functionality of the inverter, the aspect ratio of the driver transistor needs to be N times larger than the one of the load transistor. The absolute value of the DC gain is approximately given by the ratio of the driver and load transconductances [6], and thus by using Equation (17) the gain is proportional to $\sqrt[\gamma]{N}$, with γ the normalized tail-states energy disorder parameter introduced in Chapter 3. However, in the attempt of achieving gain by employing N>1, the DC input-output characteristics of the inverter becomes asymmetric, reducing its noise margin performance. As a result, the simulated gain achieved with this inverter configuration is only ~-2.8V/V (for N=10, Table 6). Furthermore, the choice of N impacts also on the separation between the high and low output voltage level of the inverter. Indeed, for

N<1 the driving current capability of the load transistor prevails the one of the driver, leading to a reduced output voltage swing which affects the correct functionality of the inverter. On the other hand, an aspect-ratio between driver and load transistor of N>1, is detrimental for the dynamic performance of the inverter, resulting in very asymmetric pull-up and pull-down current capabilities, as shown by the simulated T_{RISE} and T_{FALL} listed in Table 6.

Zero-V_{GS} Inverter (ZVI): this architecture (Figure 29(b)) exploits a load transistor connected to have V_{GS}=0V [39][101]. In this case, the load resembles an active load, and thus the inverter DC gain approaches the intrinsic gain of the technology. For the correct functionality of the inverter, the load transistor must be designed N times wider than the driver (assuming the same channel length for both devices). The ratio N determines the minimum output voltage V_{OL} reached by the inverter. A large N is beneficial to increase the separation between V_{OH} and V_{OL}, and thus the noise margin, but is detrimental for the DC gain, which decreases with N. The major drawbacks which limit the use of zero-V_{GS} inverters are the poor inverter noise margin (N_L provided in Table 6) and the weak pull-down current capability (T_{FALL}, Table 6), which severely affects its dynamic performance. The latter effect is exacerbated in implementations with enhancement-mode transistors, for which the zero-V_{GS} inverter is clearly impractical.

Bootstrap Inverter (BTI): this configuration (Figure 29(c)) makes use of a bootstrap capacitance C_{BT} to enhance the output impedance of the load transistor [103][104]. The bootstrap network further introduces a frequency dependent response of the inverter in a band-pass fashion. For DC signals the inverter resembles a diode-connected one, due to the transistor M3 which connects M2 with V_{GD}=0V. At higher frequency, a theoretical in-band gain as high as the intrinsic gain can be achieved with this configuration. However, the capacitance partition C_{BT}, C_{PAR} typically limits the achievable gain to a lower value. This configuration provides higher gain performance compared to the diode-connected inverter and larger pull-down current capability (T_{FALL}, Table 6) with respect to both diode-connected and zero-V_{GS} inverters. In addition, due to the bootstrap capacitance the simulated output voltage approaches the lower voltage supply rail (V_{OL} in Table 6), enhancing the separation between low and high output levels (V_{OH}-V_{OL}). Despite the good dynamic performance, the bootstrap inverter configuration exhibits also several drawbacks: first, a relatively large bootstrap capacitance C_{BT} is required (15 pF employed in the simulations), which could negatively impact yield. Second, the inverter footprint is typically larger than conventional inverters (diode-connected and zero-V_{GS}) due to the higher complexity in terms of transistor count, and again to the capacitance C_{BT}. Third, due to the band-pass behavior, the minimum operating frequency is limited by the first cut-off frequency, which typically falls in the ~Hz range.

Pseudo-CMOS Inverter (PCI): it is based on a diode-connected inverter M1-M2 powered with the supply voltage rails V_{DD} and V_{SS}, followed by a push-pull output stage supplied between V_{DD} and G_{ND} (Figure 29(d)) [101]. The diode-connected inverter is primary used to provide gain, while the output stage improves the overall inverter noise margin, ensures a more symmetric pull-up and pull-down current and improves the output swing (T_{RISE} , T_{FALL}, and V_{OH},V_{OL} in Table 6). Furthermore, the static power consumption required by the push-pull output stage is extremely small: the simulation results provided in Table 6 highlight indeed, a comparable power consumption for the DCI and PCI inverters, leading the latter to attain the best Energy-Delay Product (EDP) among all simulated inverters. The use of different supply rails allows also to mitigate the asymmetric input-output characteristic of the inverter, and enables tunability of the inverter trip point to approximately $V_{DD}/2$. These benefits are achieved in this inverter configuration at the expense of an increased complexity (in terms of transistor count) and thus a larger footprint. Another additional drawback is the requirement of three voltage supplies for the correct functionality of the circuit.

Diode-Connected Inverter with Level Shifter (DCILS): this configuration is used to mitigate the asymmetry of the input-output characteristic in a diode-connected inverter, improving the overall gate noise margin [39]. This is achieved by cascading a level shifter implemented by the transistors M1-M2 in a source follower configuration, at the input of the diode-connected inverter (Figure 29(c)). A proper design of the level shifter allows to adjust the inverter trip point restoring the symmetry of the input-output characteristics (V_M in Table 6). Moreover, simulation results reveal more symmetric noise margins: N_{MH}=9 V, N_{ML}=9.4 V compared to N_{MH}=0.2 V, N_{ML}=29.8 V for the conventional diode-connected inverter. However, the introduction of the level shifter circuit has a negative impact on the speed and power consumption performance. With an increase of about 11% in the total power consumption (compared to the DCI) the propagation delay (T_p, Table 6) drops by a factor 3.5. Therefore, an additional trade-off is introduced in the inverter design between power consumption and speed. Similarly to the PCI, the DCILS implementation requires 4 OTFTs with consequent larger area occupation compared to the inverter configurations requiring only the driver and load transistor.

Table 6. Inverter performance comparison (based on simulations).

Parameter	Unit	DCI	ZVI	BTI	PCI	DCILS
V_M	[V]	7	15	N/A	9.4	0
V_{OL}	[V]	-15	-15.2	-18	0	-15
V_{OH}	[V]	16.1	18	16.2	18	15.3
V_{IL}	[V]	4.4	14.6	N/A	7.2	-5.6
V_{IH}	[V]	15.9	17.3	N/A	12.2	6.3
N_{ML}	[V]	19.4	29.9	N/A	7.2	9.4
N_{MH}	[V]	0.2	0.7	N/A	5.8	9
DC gain	[V/V]	-2.8	-29.6	-2.9	-3.4	-2.4
In-band AC gain	[V/V]	-2.8	-29.6	-11	-3.4	-2.4
T_{RISE}	[µs]	2.7	29.3	2.9	1.8	12.6
T_{FALL}	[µs]	252.6	4.0×10^5	42.4	33.3	328
T_{pHL}	[µs]	26.8	1.4×10^5	23.1	26.7	1.4
T_{pLH}	[µs]	1.8	13.9	2	1.4	10.8
T_p	[µs]	14.3	7.2×10^4	15.5	14	50.9
P_W	[µW]	292	4.8×10^{-2}	272	292	326
EDP	[fJs]	60	2.7×10^5	65.1	57.4	844

4.3 Single delay stages

In this work the base memory element for multi-stage line driver circuits is defined as delay stage. Single delay stages can be implemented with different logic approaches, namely dynamic, static and transmission-gate based. Dynamic logic typically allows more compact implementations compared to static and pseudo-static (based on pass-gate/transmission-gate) approaches [105], requiring a reduced number of gates, thus minimizing sensitivity to hard faults and power consumption. Indeed, the power consumption of logic based on unipolar inverters is typically dominated by the static contributions, associated to the current flowing through driver and load transistors [105]. The dynamic power consumption associated to the charging and discharging of the output capacitance is generally negligible, due to the modest switching frequencies that printed transistors can achieve [74]. Despite these advantages, the dynamic circuits are less robust to excessive gate leakage issues compare to the other approaches, since the information is temporarily stored on capacitances. Therefore, the availability of OTFT technologies exhibiting large I_{0N}/I_{OFF} ratio is of paramount importance in the design of dynamic circuits. Besides, dynamic logic requires a minimum operating frequency in order to ensure correct circuit functionality. The use of static logic can be beneficial to mitigate the sensitivity to excessive leakage issues, enabling architectures that are more robust to leakage, at the expense of complexity (in terms of transistor count) and thus of the overall circuit hard yield performance. A trade-off between hard and soft yield performance can be obtained employing pseudo-static logic. This approach somehow combines the circuit robustness typical of static logic, with the compactness of dynamic implementations.

In this section, the design of four different single delay stages with printed unipolar OTFT technology [75] is discussed and the simulated performance compared in Table 7. The architecture of each proposed delay stage exploits a specific logic strategy, namely dynamic, pseudo-static or static, covering (at high level) all the possible approaches available in literature. The transistor-level implementation aims to simplify the circuit complexity (in terms of device count) in order to maximize the overall circuit yield. To do so, the design of digital circuits is carried out by employing different inverter topologies. This strategy permits to exploit the key features of each inverter typology, in critical points of the circuit, allowing to reduce the number of devices required. In this scenario, two novel dynamic cells have been proposed which require the least number of devices among all the implementations with unipolar organic technologies reported to-date in literature. However, dynamic logic circuits typically suffer from soft failures due to excessive leakage current in the transistors. For this reason, potentially more robust implementations based on pseudo-static and static logics are also investigated. The simulation results obtained for the different delay stages allow to identify the circuit architecture which outperforms the others according to desired requirements such as energy efficiency, speed performance, complexity, area occupation, etc. Circuit simulations are performed using clock and data signals which produce at the output of each cell a 50% duty cycle square waveform at a frequency of 200 Hz. In addition, the output of each cell is fed to a second identical delay stage in order to account for loading effects. All the delay stages employ supply voltages of V_{DD}=18 V, V_{SS}=-18 V.

Table 7. Single delay stage performance comparison (based on simulations)

Parameter	Unit	DyC	SCC	PGC	Static
Number of VIAs		11	9	14	23
Number of devices		12	11	18	32
Area occupation	[cm^2]	0.30	0.43	0.67	1.34
Integration density	[device/cm^2]	40	25	26	23
T_{DLH}	[µs]	56.5	47.2	80	50.1
T_{DHL}	[µs]	301	295.6	150	123.5
T_D	[µs]	178.8	171.4	114.5	86.8
Power consumption	[µW]	223.8	32.5	709.6	$2x10^3$
Energy-Delay Product (EDP)	[pJs]	7.1	0.9	9.3	15.1

Dynamic Cell (DyC): this proposed single delay stage (Figure 30(a)) exploits clocked logic gates [105] to control the propagation of the input D at each rising edge of the clock signals CK and $\overline{CK}$ (Figure 30(b)). This functionality is implemented on the push-pull output stages (M4-M6 and M9-M11) of both bootstrap (M1-M3) and diode-connected (M7-M8) inverters. In this circuit, the switches M5 and M10 cause a reduction of the output voltage swing, which would lead to circuit failures when propagating over multiple stages. This issue is solved here by placing a bootstrap inverter (M1-M3, C1) as first inverter of the cell. This inverter achieves nearly rail-to-rail output voltages using three transistors and a 15 pF bootstrap capacitance, thus allowing to restore the correct signal voltage levels. The output signal of DyC is extracted at node Q_N. For the correct functionality of the cell, complementary clock signals are required. In this perspective, non-overlapping complementary clocks should be used to avoid race conditions, and thus prevent the circuit form failures. However, the skew time introduced during the generation of overlapping clocks with off-the-shelf Si-discrete components is typically much smaller than the propagation delay time of the organic inverters (Table 6). With this restriction, overlapping clocks can still be safely employed for the driving of the delay stage. It is worth noticing that the DyC stage cannot be directly used as D-type Flip Flop (DFF) since low-to-high transitions of the input D are transparent to the output Q_N when the clock signal CK is low. A DyC can be simply modified to implement a DFF by placing two additional switches between M5-M6 and M10-M11, respectively. In the perspective of developing multi-stage line drivers, the use of D-type flip flops to control the propagation of the input signal D is not strictly necessary. As shown in Figure 30(b), this can be also achieved with the proposed DyC simply ensuring a proper synchronization of the input D and clock signals. The proposed cell comprises 11 devices (10 OTFT and a 15pF capacitor) which can be placed in a compact layout arrangement (Figure 33 (a)) leading to an integration density as high as 40 device/cm^2 (Table 7). This is mainly due to the reduced number of routing crossovers required, which typically demand large interconnection area due to the relatively low printing resolution of the GATE layer (Table 1). In terms of energy efficiency, the proposed dynamic cell outperforms the static and pseudo-static architectures as highlighted by the Energy-Delay Product (EDP) which in this case reaches 7 pJs (Table 7).

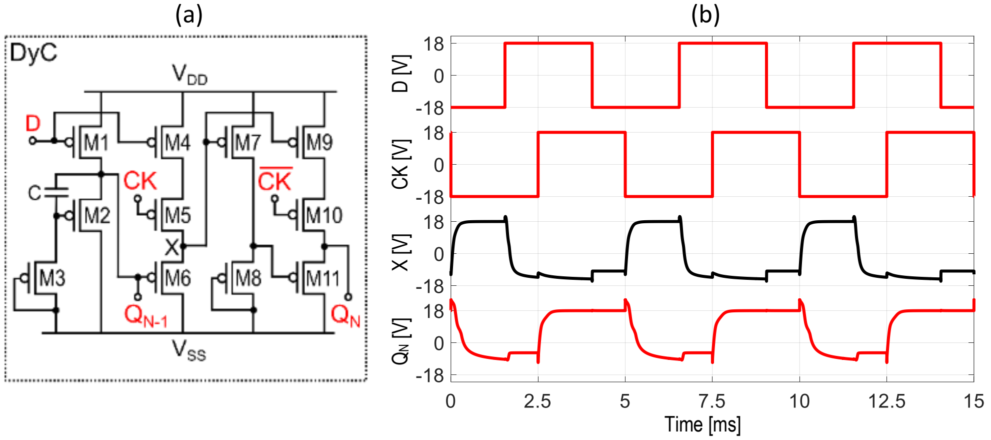


Figure 30. (a) Transistor-level implementation of the proposed Dynamic Cell (DyC). (b) Simulated time evolution of CIN, CK, X and Q_N signals.

Scan Circuit Cell (SCC): it is a single delay stage also based on dynamic logic (Figure 31(b)), which exploits as memory element the capacitive partition between the explicit capacitor C2 and stray capacitance C_P [106]. The scan circuit further requires for its correct functionality, complementary clock signals, the input data CIN and the reset signal RST. The working principle of the cell is briefly explained as follows: CIN is initially assumed high and therefore, M5 pulls the X node towards V_{SS}. In order to maximize the pull-down current capability, a bootstrap inverter (M1-M3, C1) followed by a push-pull output stage (M4-M5), has been preferred to a diode connected inverter (this configuration resembles the PCI). When a high-to-low transition of CIN occurs (Figure 31(b)), the nodes X and Y are both tied to V_{DD} by the transistors M4 and M6, respectively (initialization phase). After the successive low-to-high CIN transition (Figure 31(b)), the X node is tied to V_{SS} and the Y node set to a potential determined by the capacitive partitioning C2, C_P (hold phase). Next, the RST is asserted to

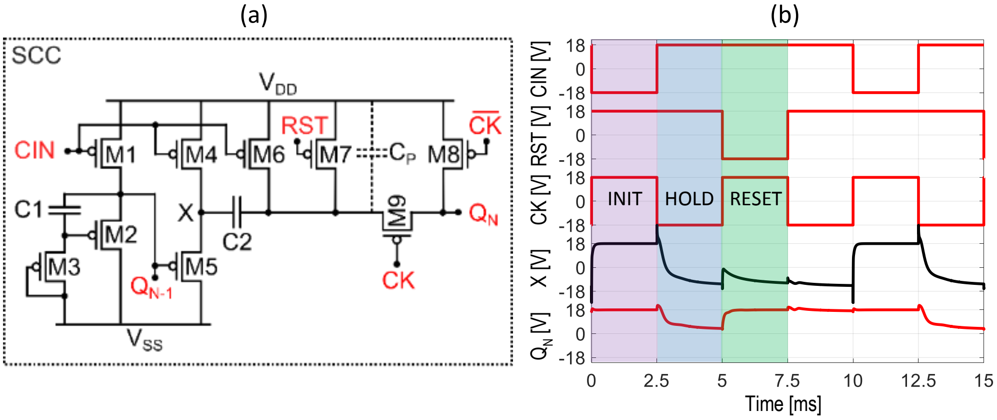


Figure 31. Transistor-level implementation of the proposed Scan Circuit Cell (SCC). (b) Simulated time evolution of CIN, RST, CK, X and Q_N signals.

refresh the memory cell (reset phase). In order to ensure the correct propagation of the output pulse Q_N a proper time synchronization between the signals CIN, RST, CK and $\overline{CK}$, is required. In particular, in order to generate an output signal with 50% duty cycle the initialization and reset phases take place at the same time.

The scan circuit implementation comprises 11 devices per delay stage and requires an area of 0.43 cm^2. Despite its compact layout (Figure 33 (b)), the large capacitance C2 negatively impacts the integration density, which for this structure does not exceed 25 device/cm^2. In order to guarantee sufficient separation between the high and low output levels, the capacitance ratio $C2/C_P$ needs to be maximized. However, a large value of the capacitor C2, intrinsically exposes the circuit to higher probability of failure. Therefore, as trade-off, a capacitance C2 of 60pF has been chosen. In terms of energy efficiency the scan circuit attains the lowest EDP performance (0.9 pJs) compared to all other implementations (Table 7).

Pass-Gate Cell (PGC): in this case the delay stage is a DFF implemented with pseudo-static logic [47]. The schematic of the cell is provided in Figure 32(a). This configuration exploits four switches (M1, M6, M7 and M12) driven with complementary clock signals to control the delay in the propagation of the input D Figure 32(b). The same considerations presented for the DyC and concerning non-overlapping complementary clock signals apply in this case. The memory elements of the cell consist of DCIs which can be dynamically connected in back-to-back configuration (acting as static latches), by means of the transistors M6 and M12. This feature prevents the circuit from failures due to excessive leakage (typical of the dynamic logic). Due to the absence of the complementary n-type OTFT, the four switches are implemented with p-type transistors only. Consequently, the propagation of the input signal D through the pass-gate transistors experiences an amplitude loss of about a threshold voltage V_{TH}. This voltage reduction is fully compensated by the bootstrap inverter M15-M17, C1 placed at the output of the cell. Additionally, to maintain the same polarity of Q_N with the input signal D, the diode-connected inverter M13-M14 is added to the signal chain.

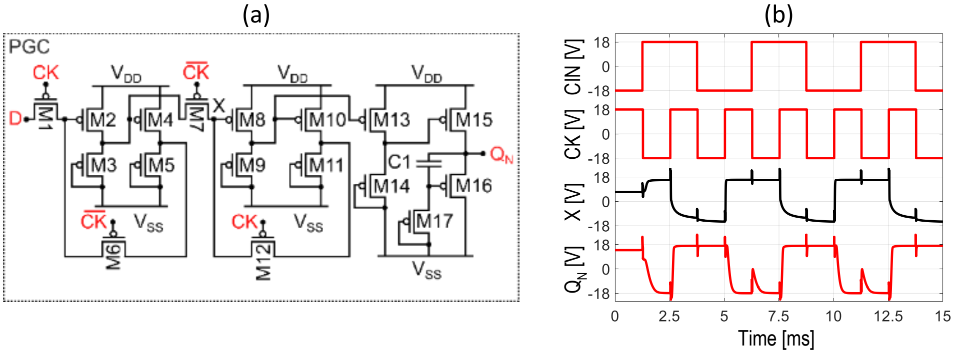


Figure 32. (a) Transistor-level implementation of a Pass-Gate Cell.

This implementation of the PGC requires 18 devices (17 OTFT and a 15 pF capacitor), leading to a cell footprint of 0.67 cm^2. The presence of the pass-gate transistors together with high number of routing crossover reduces the compactness of the layout, leading to an integration density of 26 device/cm^2. Furthermore, the simulation results provided in Table 7 reveal that the designed transmission-gate DFF achieves superior speed performance compared to both dynamic cells (T_D, Table 7). However, this is obtained at the expense of lower energy efficiency.

Static cell: this architecture is typically the most robust to OTFT parameter variations and excessive leakage issues. The schematic of the conventional fully static DFF is provided in [47]. In order to reduce the number of devices required by the static cell, all the logic gates are implemented using diode-connected loads. This strategy leads to a total number of 32 OTFTs arranged in an area of 1.34 mm^2. Due to the large number of interconnections required on the second metal layer (Figure 33 (d)), the integration density for this structure does not exceed 23 device/cm^2.

Fully-static DFF are typically power hungry and less energy efficient compared to other approaches, as highlighted in Table 7. Despite these drawbacks, this architecture achieves the lowest propagation delay (TD= 86.8 μs, Table 7) at the given supply voltage. Therefore, if the speed performance is the main concern in the design of the digital circuit with unipolar OTFTs, the use of static logic employing diode-connected load transistors ensures the best performance. Of course, serious hard yield issues may affect this implementation of the delay stage that requires the highest number of OTFTs.

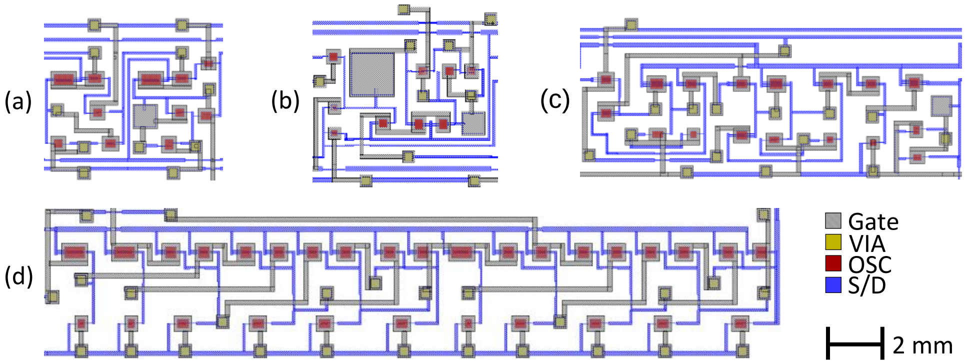


Figure 33. Layout comparison between (a) DyC, (b) SCC, (c) PGC and (d) static single delay stage.

4.4 8-stage Organic Line Drivers

Multi-stage organic line drivers have been designed exploiting the delay stages introduced in the previous section. Since no specific display or sensor matrix was targeted, the number of delay stages has been chosen in order to enable the fabrication of the Organic Line Driver (OLD) circuits with reasonable yield. A rough estimation of the maximum achievable circuit complexity (in terms of device count) for this technology can be obtained by considering the device yield value of 99.8% (discussed in Chapter 2) and assuming a maximum OLD circuit defectivity rate of $\sim$ 30%. This corresponds to architectures which comprise a maximum number of ~ 200 devices. It is important to remark that this result provides only a rough indication. Indeed, the considered device yield value has been assessed for this technology, considering devices (OTFTs only) with constant gate area and calculated over a number of samples which is not sufficient to extract statistically meaningful information.

Three multi-stage OLDs have been designed with different gate logic approaches, in order to investigate the robustness and compare the performance of the different architectures. In this perspective, both proposed dynamic cells (DyC and SCC) and the pseudo-static DFF have been exploited for the implementation of the OLDs. On the contrary, line driver implementations which make use of a fully-static logic have been avoided since they are extremely demanding in terms of complexity. Moreover, according to the previous yield considerations, all the proposed OLD architectures were designed with 8-stages only. In this way, the developed circuit architectures do not exceed complexity of $\sim$200 devices, regardless the chosen topology. It is expected however, that OLDs with larger number of stages could be manufactured maintaining a reasonable yield, as the technology will approach a higher level of maturity. OLDs with the current number of stages could be suitable to develop line addressing solutions for large-area sensor matrix applications, but not for display driving applications, where the number of lines required is in typically significantly higher.

The three versions of the 8-stage line drivers have been designed and laid out exploiting the Process Design Kit developed in Chapter 3. The designed circuits (3 repetitions of the OLD based on DyCs, 4 repetitions of the OLD developed with SCCs and 2 replicas of the OLD realized with PGCs) have been accommodated in a 126 x 126 mm^2 module of the GEN1 mask-set. The photograph of the fabricated module is provided in Figure 34. The design and characterization of each OLD architecture are discussed in detail in the next sections while the comparison of the measured performance is provided in Table 8.

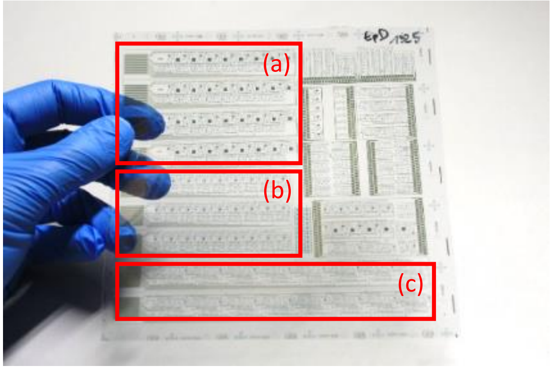


Figure 34. Photograph of the fabricated 126 x 126 mm² module, comprising a total number of 9 line driving circuits. (a) 4 OLDs based on DyCs. (b) 3 OLDs based on SCCs. (c) 2 OLDs based on PGCs.

Table 8. Organic line driver performance comparison (based on measurements)

Parameter	Unit	OLD architecture based on		
		DyCs	SCCs	PGCs
Area occupation	[cm^2]	6.6	9.5	14.8
Integration density	[device/cm^2]	22	16	12
Max. T_D	[µs]	375	525	312.5
Max. T_{RISE}	[µs]	76	78	68.2
Max T_{FALL}	[µs]	834	325.3	267.3
Max V_{OL}	[V]	-11	-6.4	-16
Min V_{OH}	[V]	17	16.9	15
Power consumption	[mW]	3.2	3	11.2
Energy-Delay Product (EDP)[2]	[pJs]	56.2	103.3	136
Number of required devices		148	152	192
Tested structures		15	20	10
Structure yield	[%]	100	65	80
Relative current dev. under tensile strain	[%]	<12	<5	<4

4.4.1 OLD based on DyCs

In this section, an 8-stage line drivers exploiting a cascade of eight DyCs is proposed (Figure 35(a)). Arrays of inverters serve as output buffers, in order to ensure sufficient current capability to drive the output line capacitance (estimated to be 10 pF). A pseudo-CMOS inverter (Figure 35(b)) is preferred to a diode-connected one as output stage, thanks to its better dynamic performance (Table 6), which is achieved here at the expenses of a reduced output swing.

---

[2] Referred to a single delay stage. EDP=Power consumption x T_D^2/Number of OLD stages.

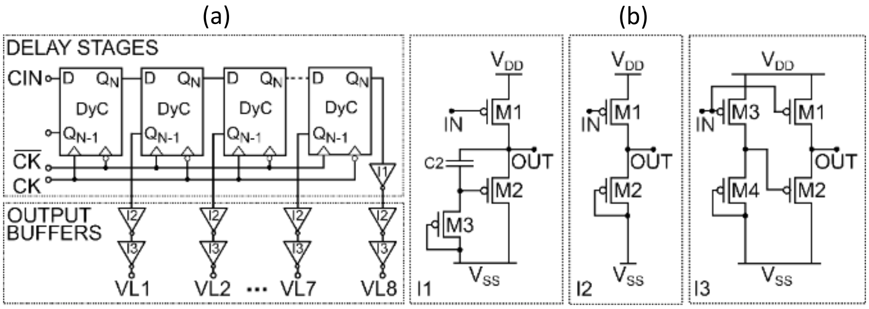


Figure 35. (a) Gate-level implementation of the 8-stage organic line drivers based on DyCs. (b) Transistor-level implementation of the inverters I1, I2 and I3.

The measurements of the 8-stage organic line drivers were performed more than 4 weeks after the foil fabrication, in air and dark conditions. The measurement setup consists of a PCB, provided with Si-interface electronics (developed with off-the-shelf components) and a National Instruments data acquisition board (NI 6259 DAQ) used for the generation of the synchronization signals, and the readout of the line driver output signals. The Si-interface electronics makes use of three comparators to enable the matching of the synchronization signal voltage levels between the DAQ and the foil, and an array of 8 operational amplifiers in feedback configuration to serve as voltage buffer for the readout the OLD output signals. An additional adaptor equipped with a 0.5 mm pitch 18-pin flip-lock connector is used to engage the line driver on foil and connect the latter to the main PCB. The picture of the complete measurement setup is provided in Figure 36.

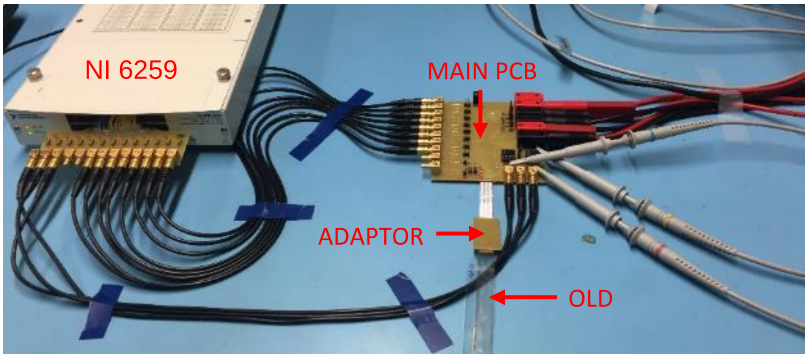


Figure 36. Measurement setup used for the characterization of the line driver circuits.

The OLD is driven with 200 Hz complementary clocks in order to produce 2.5 ms line pulse widths. The time interval between the assertion of the first VL1 and the last VL8 output line is here defined as frame. The generation of the output line signals (VL1-VL8) is initiated in each frame by a pulsed signal (low->high->low) applied on CIN (Figure 37).

The complete system consumes 87.9 µA with a dual supply voltage of ±18 V. The current consumption is nearly equally divided between the sequential logic (44.6 µA) and the output buffers (43.3 µA). The maximum propagation delay measured among the output lines is 375 µs, the largest rise time and fall time read respectively 76 µs and 834 µs, while the minimum output line swing ranges from 17 V to -11 V. The corresponding Energy-Delay Product, calculated for a single delay stage is equal to 56.2 pJs. The output waveforms recorded by the 8-stage organic line drivers are presented in Figure 37.

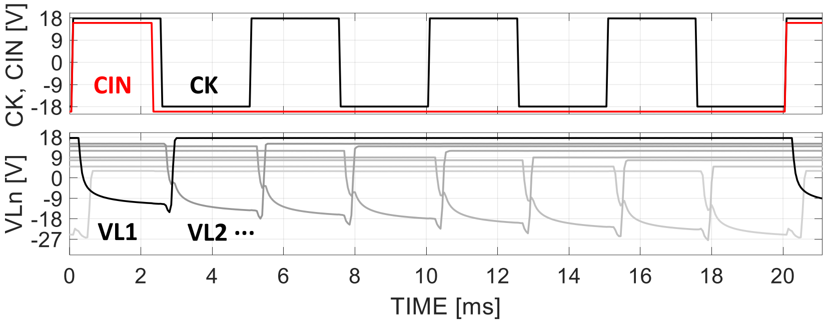


Figure 37. Recorded output signals of the 8-stage line drivers developed with dynamic DyCs. Each output line is displayed with a vertical offset to improve the clarity.

The complete organic line driver architecture (delay stages and output buffers) counts 139 transistors and 9 capacitors, requiring an area of 6.6 cm^2 and leading to an integration density of 22 device/cm^2. The micrograph of the circuit is provided in Figure 38.

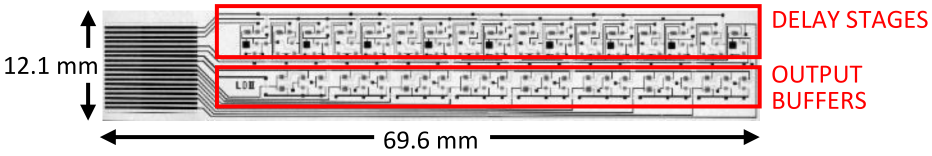


Figure 38. Micrograph of the printed 8-stage organic line drivers based on SCCs.

The correct functionality of the line drivers becomes critical as the clock frequency reduces below ~ 100 Hz, due to soft failures generated by excessive leakage current. At nominal operating frequency, failures in the circuit functionality have been observed when the measurements are performed in light conditions. Indeed, one of the major effects of the light exposure observed on the printed OTFT fabricated in this technology [74] is the increase of leakage current with consequent reduction of the I_{ON}/I_{OFF} ratio.

The hard yield performance of the proposed 8-stage organic line drivers has been also assessed. The functionality of 15 out of 15 line driver circuits has been successfully verified over 5 successive printed foils leading to 100% fully-working structures.

The line driver circuit functionality has been also evaluated under mechanical stress conditions. This is particularly relevant for applications in which the mechanical flexibility of the overall system is required. In this perspective, strain was applied on the circuit, by means of mechanical bending of the plastic substrate over cylindrical plastic supports characterized by different radius (Figure 39(a)). The superficial strain induced on the OTFTs was evaluated according to the formula reported in [107]:

$$s_{\%} = \frac{t_{PEN}}{2R} \tag{21}$$

where, t_{PEN} is the thickness of the substrate (125 µm) and R is the bending radius, ranging in this analysis between 13 mm and 32.5 mm. For the sake of completeness, it should be mentioned that only tensile strain was applied in these characterizations. Compressive strains could be also applied to the sample. However, this would require in the current measurement setup, the introduction of a printed protective layer on top of the technology stack, in order to prevent damages of the electronics due to the contact with the plastic supports. The effects of the mechanical stress on the circuit are evaluated by measuring variation of the total current consumption ΔI_{DD} during the bending condition with the respect to the I_{DD} in flat state (absence of applied strain). The results presented in Figure 39(b) reveal a maximum decrease of the current consumption from its initial value of about 11% along the entire range of analysis. In addition, the current consumption reduction introduced by the mechanical stress is a non-reversible effect. After the application of mechanical stress, the sample is not capable to recover the value of current consumption I_{DD} initially recorded, even in absence of applied strain. Despite the current consumption reduction, the correct functionality of the OLD has been successfully verified in all the tested bending conditions.

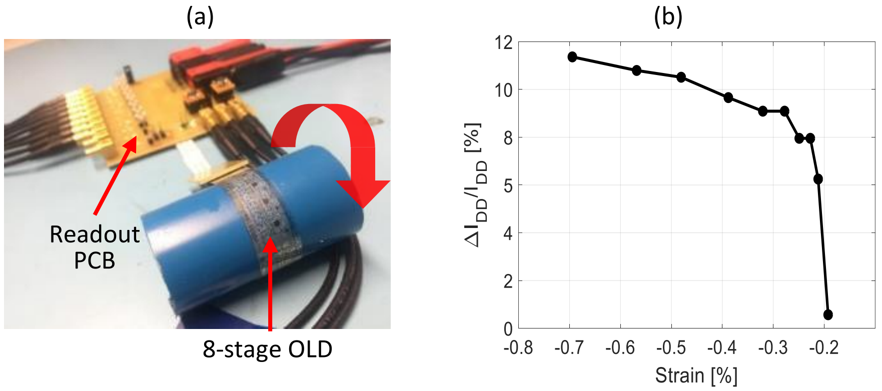


Figure 39. (a) Measurement setup used for the evaluation of the mechanical stress effects induced on an 8-stage organic line drivers in bending condition. (b) Normalized variation of the DyC based OLD total current consumption under mechanical stress (tensile strain).

4.4.2 OLD based on SCCs

This section describes the proposed 8-stage line drivers composed of SCCs, interconnected as shown in Figure 40(a). This configuration allows to automatically generate the RST signal for each cell, without using additional inputs, and thus minimizing the number of external connections with the Si-readout electronics. The arrangement of the SCCs presented in Figure 40(a) permits to realize line driver architectures with an even number of delay stages only. This constraint is introduced by the alternate distribution of the clock signals among the cells, which enables the output lines of successive even (or odd) delay stages only at integer multiples of the clock period. This limitation can be overcome by rearranging the clock signal interconnections within each cell.

The output signal is extracted for each stage at the terminal Q_{N-1} rather than Q_N in order to minimize the loading effects on the latter node. Indeed, as explained in Section 4.3, the SCC exploits a capacitive partitioning between C_2 and the parasitic capacitance C_P as memory element (Figure 31(a)). In order to maximize the separation between the high and low voltage levels, the ratio C_2/C_P needs to be also maximized. In this perspective, the extraction of the output signal at the node Q_N would further increase the loading effects, and thus the requirement for a larger explicit capacitor C_2. The output signal of each delay stage is fed to an array of tapered inverters I_1, and finally connected to a pseudo-CMOS inverter I_2, in order to drive the output line capacitance (estimated to be 10pF) with sufficient current capability.

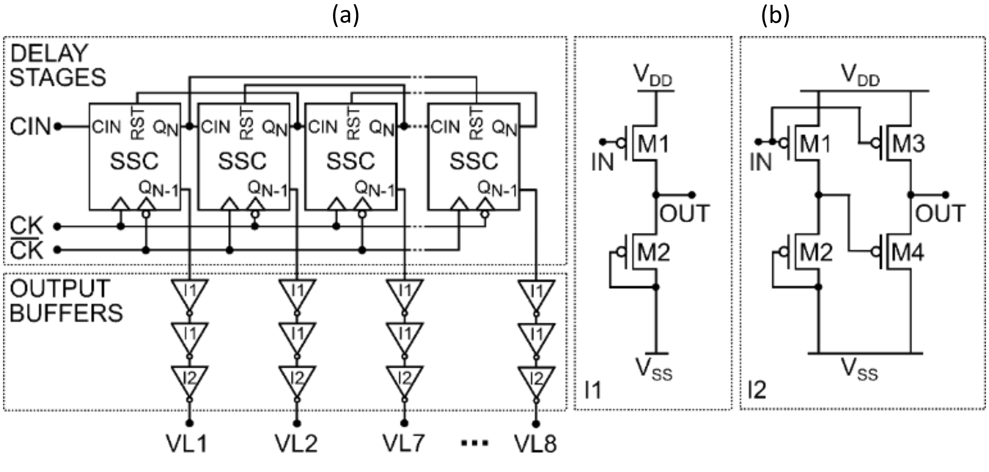


Figure 40. (a) Gate-level implementation of the 8-stage organic line drivers based on SCCs. (b) Transistor-level implementation of the inverters I1 and I2.

The proposed 8-stage organic line drivers have been measured more than 4 weeks after the foil fabrication in air and dark conditions using the very same measurement setup described in Figure 36. Similarly to the DyC based OLD, the circuit is driven by 200 Hz complementary clocks, in order to produce 2.5 ms line pulse widths. The generation of the output line signals (VL1-VL8) is initiated in each frame by applying a pulsed signal (high->low->high) on the input CIN.

The measurement results reveal a current consumption for the entire circuit of about 84.1 µA with a dual supply voltage of ±18 V. More in detail, the sequential logic requires 3.1 µA while the output buffers 81 µA. The use of SCCs allows to build sequential circuit with lower power consumption compared to DyCs based architectures. However, the additional inverter chain required in the output buffer stages, partially reduces this benefit. Indeed, the power consumption of this OLD architecture is mainly determined by the output buffer stages rather than the sequential logic. The maximum propagation delay measured among the output lines is 525 µs, which leads to and EDP of 103.3 pJs (for a single delay stage). In addition, the largest rise time and fall time are respectively 78 µs and 329.3 µs, while the minimum output voltage levels of the lines range from 16.9 V to -6.4 V. The output waveforms recorded by the 8-stage organic line drivers are presented in Figure 41.

Unlike the OLD based on DyCs, this architecture enables the generation of non-overlapping output line VL1-VL8 signals. In other words, between the assertion of two successive output lines VLN and VLN+1 the presence of a blank time interval is always guaranteed. This feature is typically preferred in display driving applications, in order to ensure a good isolation between pixels of adjacent lines, during the writing operations.

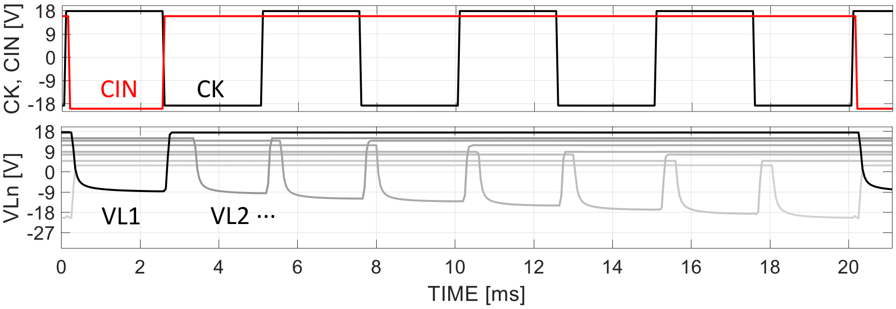


Figure 41. Recorded output signals of the 8-stage line drivers based on SCCs. Each output line is displayed with a vertical offset to improve the clarity.

The implementation of the organic line drivers (delay stages and output buffers) requires 136 transistors and 16 capacitors, distributed over an area of 9.5 cm^2. The micrograph of the circuit is shown in Figure 42.

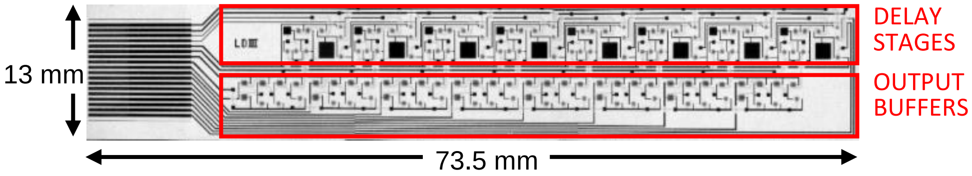


Figure 42. Micrograph of the printed 8-stage organic line drivers based on SCCs.

Differently from the OLD architecture presented in Section 4.4.1, the functionality of the circuit is typically less critical at low clock frequencies (~10 Hz) and under ambient light exposure. Indeed, the dynamic logic relies on the explicit capacitor C_2 which is in this design more than an order of magnitude larger than the stray capacitances of the OTFTs, leading to a higher hold time performance for this dynamic logic.

In term of yield performance, the functionality of 13 out of 20 line driver circuits has been successfully verified over 5 printed foils leading to 65% fully working structures. Despite this architecture exhibits a circuit complexity (in terms of device count) comparable to the DyC based OLD, the circuit defectivity rate reaches 35%. This loss of yield performance could be attributed to defects in the fabrication of the explicit capacitors C_2. Each capacitor requires area ~30 times larger than the average OTFT gate area, which further leads to a larger probability of defect formations.

Mechanical stress tests have been also performed on the proposed OLD. The circuit on foil has been mounted around cylindrical supports featuring different radius ranging from 13 mm to 32.5 mm, in order to induce superficial tensile strain on the printed circuit. In this condition, the average current consumption has been recorded for each value of applied tensile strain. The measurement results are provided in Figure 43.

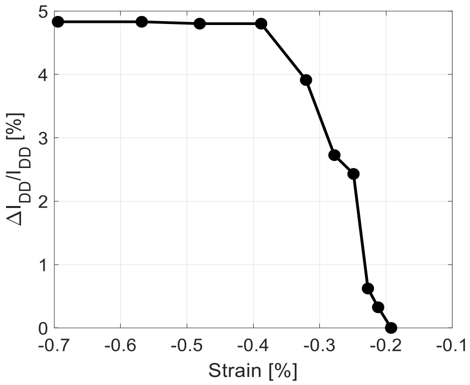


Figure 43. Normalized variation of the SCC based OLD total current consumption under mechanical stress (tensile strain).

The data displayed Figure 43 show a reduction of the overall circuit current consumption associated to the mechanical stress of the OTFTs, which however remains below 5% along the tensile strain span of analysis. Similarly to the case of the OLD based on DyCs, also here the mechanical stress tests produce irreversible effects on the OTFTs. Interestingly, the comparison of the results shown in Figure 39(b) and Figure 43(b), for the two OLD implementations based on DyCs and SCCs, seems to suggest that the latter architecture is less sensitive to mechanical stress (tensile strain). Indeed, the maximum relative current consumption displacement changes nearly 12% in the first case, and 5% in the second. However, since the characterized OLDs belong to different foils, this performance discrepancy could also be introduced by the dissimilar fabrication conditions at which the two samples have been subjected. Further investigations are therefore required to draw conclusions. Also in this case, the correct functionality of the OLD is verified during all the mechanical stress tests.

4.4.3 OLD based on PGCs

An 8-bit shift register can be obtained as cascade of D-type Flip Flops (Figure 44(a)). This digital circuit provides the same logic functionality as a line drivers. The DFF has been implemented exploiting the pseudo-static cell (Figure 32(a)) rather than the static one, because of the lower number of transistor required. However, both approaches are more robust against circuit failures caused by excessive leakage currents. Similarly to the previous OLDs, the proposed 8-stage line drivers combines sequential logic with arrays of inverters used as voltage buffers (Figure 44(a)). The output stage is based on a pseudo-CMOS inverter (I2 component, Figure 44(b)) designed to drive the 10 pF line capacitance. The complete architecture of the proposed OLD is provided in Figure 44(a).

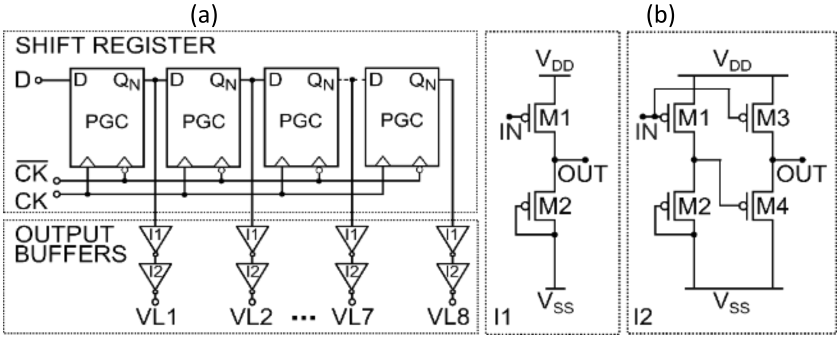


Figure 44. (a) Gate-level implementation of the 8-stage organic line drivers based on PGCs. (b) Transistor-level implementation of the inverters I1 and I2.

The characterization of the 8-stage organic line drivers was performed in air and dark conditions using the measurement setup described in Figure 36, at least 4 weeks after the fabrication of the foils. The circuit is powered with a supply voltage ±18 V and driven by 400 Hz complementary clocks in order to control the signal propagation through the DFF chain and produce output line pulse widths of 2.5 ms. The generation of the output line signals (VL1-VL8) is initiated in each time frame by means of the input signal D.

The total current consumption of the system is 230 µA, nearly equally divided between the sequential logic (116 µA) and the output buffers (114 µA). In terms of dynamic performance the OLD based on PGCs outperforms the implementations based on dynamic logic (Table 8). Indeed, the maximum propagation delay measured among the output lines is 312.5 µs, the largest rise time and fall time read respectively 68.2 µs and 267.3 µs, while the minimum output line swing ranges from 15.7 V to -16 V. However, these benefits are achieved with lower energy efficiency (EDP= 136 pJs). The output waveforms recorded by the 8-stage organic line drivers are presented in Figure 45.

The complete OLD circuit counts 192 devices, of which 184 are transistors and 8 capacitors, placed over an area of 14.8 cm^2. The corresponding integration density is 12 device/cm^2, nearly a factor 2 lower than the DyC based OLD. The micrograph of the circuit is provided in Figure 46.

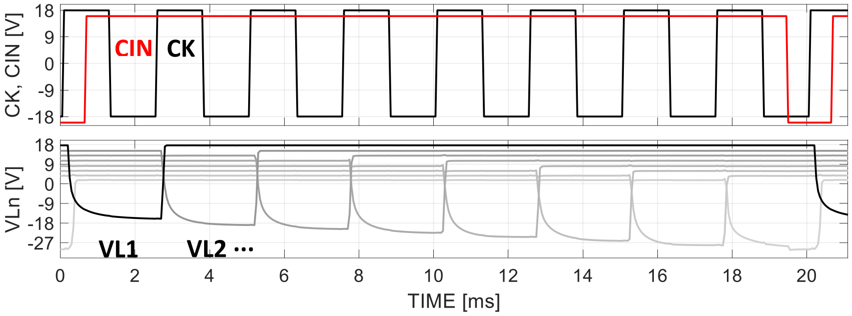


Figure 45. Recorded output signals of the 8-stage line drivers developed with PGCs. Each output line is displayed with a vertical offset to improve the clarity.

Unlike the OLD based on DyCs, this line driver architecture does not suffer from soft failures caused by low clock frequency operation mode or light exposure. Measurements performed in light conditions condition and at low frequency of operation (clock frequency <100 Hz) show no significant impact on the correct functionality of the OLD, further proving the robustness of the circuit to excessive leakage currents. The evaluation of the circuit defectivity due to hard faults reveals that 8 out of 10 line driver circuits are functional leading to 80% fully-working OLDs. Even though the number of analyzed samples does not allow to extract quantitative and statistically meaningful information on the failure rate of the circuit, it should be highlighted that the higher transistor count required by the pseudo-static logic compared to the dynamic ones, has a clear detrimental effect on the overall yield performance.

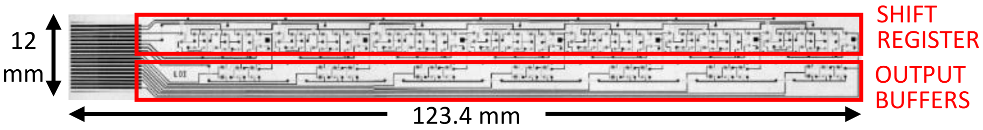


Figure 46. Micrograph of the printed 8-stage OLD based on PGCs.

Likewise for the previous OLDs the impact of the tensile strain induced by the bending of the substrate on the circuit has been also evaluated with the very same measurement setup. The normalized current consumption variation curve extracted at the different tensile strain levels is presented in Figure 47.The measurement results show that the mechanical stress tests cause a maximum relative current consumption reduction < 3.6% along the entire range of analysis, which however does not affect the correct functionality of the circuit. These results are in line with the outcome of the mechanical stress tests performed on the OLD implemented with SCCs (Table 8). For completeness, it should be added that both tested samples belong to the same foil.

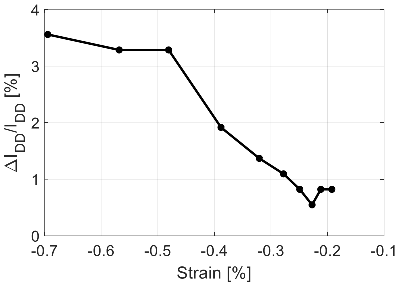


Figure 47. Normalized variation of the PGC based OLD current consumption under mechanical stress.

4.5 Conclusions

In this Chapter has been discussed the design and characterization of multi-stage line driver circuits for matrix addressing applications, developed with printed unipolar organic technologies. Different logic approaches (dynamic, pseudo-static and static) have been investigated to develop single delay stages, which compose the core of line driver architectures. One of the major concern in the design of digital circuits with printed OTFTs is the complexity (in terms of device number) of the architecture. Indeed, printed organic technologies typically achieve modest device yield performance, and therefore to manufacture circuits with reasonable yield, the number of devices utilized needs to be minimized. Towards this achievement, the design of the digital circuits has been here performed here by combining different topologies of inverter implementations within the same functional block. This strategy is here preferred to the classical approach which makes use of the same inverter topology to develop the digital building blocks. This allows to exploit the key features of each inverter configuration in the critical points of the circuit, enabling the reduction of the complexity, power consumption and area occupation. In this scenario, two novel dynamic delay stages (DyC and SCC) have been proposed, which allow compact implementations with a reduced number of devices.

Circuit simulation have been used to compare the electrical performance of the proposed dynamic delay stages with conventional static and pseudo-static architectures. The outcome of this analysis shows that the proposed dynamic logic achieve higher energy efficiency compared to the static and pseudo-static counterparts, due to the reduced number of inverters and thus static current paths active in the circuit. In addition, the minimization of the circuit complexity further leads to smaller circuit footprints which facilitate the integration of the line drivers in matrix-addressing applications such as displays or sensor matrices.

In order to experimentally verify the simulation results obtained for the single delay stage and further assess the potentiality of the OTFT technology, three different multi-stage organic line driver circuits have been designed, manufactured and evaluated. More in detail, two of the developed line drivers make use of dynamic delay stages, while the third architecture is based on pseudo-static cells. Preliminary calculations based on the technology yield analysis provided in Chapter 2, indicate that only circuit architectures employing less than ~ 200 devices can be theoretically fabricated with reasonable yield. For this reason, the OLD number of stages in the OLD was limited to 8.

The evaluation of the line driving circuits further confirm the preliminary results extracted from circuit simulations. Both OLDs based on dynamic logic outperform the pseudo-static one in terms of energy efficiency, area occupation and integration density (Table 8). In particular, with an Energy-Delay Product (EDP) of 56.2pJs (referred to a single delay stage) the OLD architecture based on DyCs is the most energy efficient. On the contrary, even though the second dynamic OLD exploits SCCs which are beneficial towards the overall power consumption reduction, the presence of an additional array of output buffers required to achieve the correct output signal polarity, nullifies this positive effect. This limitation could be mitigated by selecting Q_N as output node of the delay stage, at the expense of larger value of the explicit capacitor C_2 required to compensate the effects of the additional parasitic capacitance introduced.

The proposed OLDs implemented with both dynamic logic schemes are well suited for applications in which the power consumption and area occupation are the main concerns. However, for the correct functionality of the circuits, a minimal operating frequency applies of ~100 Hz and ~10 Hz, for the DyC and SCC versions, respectively. As direct consequence of this constraint, the versatility of both OLDs is reduced. On the other hand, the line driver circuit developed with pseudo-static logic, performs well in terms of speed and output voltage capability without requiring a minimum operating frequency.

From a functionality perspective, the electrical evaluation of the proposed OLD architectures reveal yield values ranging from 65% (for the SCC versions) to 100% (for the DyC versions) as reported in Table 8. The yield performance of the latter architecture is extracted over 15 samples, corresponding to a total number of 2085 working OTFTs. This result is not in contrast with the device yield analysis discussed in Chapter 2. Indeed, the multi-fingered transistors used in this circuit typically require smaller gate area compared to the TLM layouts used for OTFT characterization, and therefore are less prone to defects. These circuits all together can potentially address a 120-rows matrix, enabling e.g. flexible displays featuring Quarter Quarter Video Graphics Array (QQVGA) resolution (160 x 120 pixels).

The 8-stage organic line driver functionality was also evaluated under mechanical stress conditions for each proposed implementation. This information is particularly relevant for applications such as sensor matrices or foldable displays, in which the mechanical flexibility of the overall system is a fundamental aspect. In this perspective, tensile strain was applied on the circuit, by means of mechanical bending of the plastic substrate over cylindrical plastic supports with radius ranging from 13 mm and 32.5 mm. The effects of the mechanical stress on the circuits are evaluated by measuring the variation of the total current consumption ΔI_{DD} during the bending condition with respect to the I_{DD} in absence of applied strain. The measurements results reveal a relative current deviation <12% among the evaluated OLD versions, and obtained with a maximum applied tensile strain value of -0.7%. This current variation however, has no significant effects on the functionality of the circuits, which has been verified during all the tests in bending conditions, making these structures suitable for applications in which the mechanical flexibility of the plastic substrate is actively exploited.

5. Smart temperature sensor on RFID

In this chapter a smart temperature sensor integrated in a passive RFID tag, manufactured with a unipolar printed organic transistor technology will be demonstrated for the first time. The proposed system-on-foil enables the fabrication of inexpensive disposable electronic devices for innovative applications in the cold chain temperature monitoring of food and pharmaceutical products. In order to achieve this, printed resistive temperature sensors have been selected for the temperature sensing, and a time-based frontend interface has been exploited to perform the analog-to-digital signal conversion. The RFID tag is further capable of transmitting the digitized signal to a reader, via an RF communication link at a frequency of 13.56 MHz. In addition, in order to develop a stand-alone system–on-foil, the tag has been equipped with a harvesting circuit for wireless power transfer.

The contents of this chapter will be submitted as a journal publication (currently in preparation).

5.1 Introduction

The availability of mass production processes to fabricate inexpensive electronic devices is a key enabler for the commercial introduction of innovative smart sensing solutions, for applications in the market of healthcare, retail, logistics, etc... In this context, Radio-Frequency Identification (RFID) tags represent a clear example of electronic devices which are largely employed in commercial applications due to their relatively low price. However, despite silicon-based RFID tags can be easily equipped with sensing capabilities and further enriched with several analog and digital functionalities, their use as disposable devices in applications in which the cost is the main concern, remains limited. Silicon-based RFID tags currently cost more than 10-15 $ cents per unit (depending on the production volume). This cost is acceptable for certain applications while for other it is a showstopper.

An attractive solution to potentially bring down the costs of the electronics enabling the fabrication of inexpensive devices, is the use of printed organic materials. Indeed, organic transistors are typically manufactured exploiting low-temperature processes with lower purity levels compared to Si counterpart, which intrinsically lead to the reduction of the fabrication costs. Moreover, organic materials can be processed by solution, enabling the use of printing techniques to manufacture electronics over large areas further bringing down the costs. The compatibility of organic and inorganic materials with additive fabrication processes can be also exploited to integrate sensing functionalities together with the OTFT electronics, leading to smart sensing systems-on-foil. Additional attractive features associated to the low-temperature manufacturing process are the mechanical flexibility and the lightweight which together enable solutions with unprecedented form factors. These features could be exploited to integrate electronic devices e.g. in the outer packaging of commercial products. In this perspective, temperature monitoring solutions for applications such as food or pharmaceutical cold chain monitoring could be potentially developed with fully-printed organic technologies, leading to inexpensive disposable temperature-monitoring devices in the market of healthcare and retail. The possibility of controlling the temperature of perishable goods, from the production until their distribution reducing waste, has a significant social, economic and environmental impact [108].

In this context, the work described in this chapter aims to develop a smart temperature sensor on a passive RFID tag, manufactured with printed organic materials, and to demonstrate for the first time the suitability of system-on-foil solutions based on printed electronics for the application in the monitoring of perishable goods. The temperature ranges of interest for food and pharmaceutical cold chain temperature monitoring applications are not standardized. Hence, in this work the classification introduced in [109] has been used to identify the temperature ranges required for the correct storage of different categories of refrigerated food:

- Frozen food, at -25°C for ice cream, −18 °C for other food
- Cold-chilled food, from 0 °C to 1 °C
- Medium-chilled food, at 5 °C
- Exotic-chilled food, between 10 °C and 15 °C

Further information can be found in the CEN 12380 (1999) legislation, which demands for the refrigerated food temperature measurements an accuracy of ±1°C and resolution ≤ 0.5°C in the temperature range between -25°C and 15°C.

Similarly, for the storage temperature of pharmaceutical products and medical supplies a general classification provided by the World Health Organization (WHO) has been considered here [110]:

- Store frozen: transported within a cold chain and stored at -20°C
- Heat sensitive products that must not be frozen: stored at temperature between 2°C and 8°C
- Keep cool: stored at temperature between 8°C and 15°C.
- Room temperature: stored at temperature between 15°C and 25°C.
- Ambient temperature: stored at the surrounding temperature between 15°C to 25°C or up to 30°C, depending on climate conditions.

The guidelines for storage and transport of time and temperature-sensitive pharmaceutical products provided by the WHO [111], indicate for the monitoring sensors an accuracy performance ≤ ±0.5°C (for electronic devices) and ±1°C or better for alcohol, bi-metal, gas or vapor pressure thermometers.

It is worth mentioning that these guidelines provide an insight of the potential requirements for the target applications. This knowledge is thus used to steer the design of the proposed smart temperature sensor. In particular, a temperature range from 0°C to 30°C, an accuracy ≤±1°C and a resolution better than 0.5°C, have been specified for this work, sufficient to monitor the keeping conditions of most of the products within the target applications, except for the products that require to be frozen.

Despite the use of printed organic technologies is attractive from the application point of view, the development of circuit architectures based on organic transistors for temperature monitoring solutions on RFID tags is not free of challenges. Organic semiconductors are typically affected by performance loss at high frequency of operation, making the design of RF harvesting circuits extremely difficult. Furthermore, the combination of the modest yield and low transistor speed performance reduces the versatility of the RFID architectures. As example, the compatibility of these devices with conventional Near Field Communication (NFC) standards has not been demonstrated yet. The energy harvesting capability of the scavenging circuits is typically modest, leading to severe constrains to the power consumption of the overall system architecture. At last, the absence of current and voltage reference circuits in the literature makes the design of power management units (on RFID) extremely challenging. For these reasons, the current state-of-the-art counts only few systems-on-foil manufactured with organic technologies (or more in general with flexible electronics) for temperature monitoring applications. Temperature sensors providing a single bit information have been demonstrated in [112] and [113]. These smart labels are capable to detect when the environmental temperature exceeds a given set point, storing this information in a non-volatile memory. The temperature threshold sensor developed in [112] has been further embedded in a Si-based RFID tag operating at

13.56 MHz, in order to transmit the stored data to a base station. An Asynchronous Sigma-Delta Modulator (ASDM) has been developed in [114] with a unipolar a-IGZO technology, and used to readout the temperature sensed by two thin-film resistors. However, this architecture requires several bias voltages, which makes its implementation on RFIDs cumbersome.

This Chapter is further organized as follows: an overview of the system-on-foil architecture is provided in Section 5.2. The design of the smart temperature sensor is discussed at system and transistor level in Section 5.3. Measurement results obtained from the manufactured system are presented in Section 5.4. A benchmark with the current state-of-the-art is provided in Section 5.5. Conclusions are drawn in Section 5.6.

5.2 System-on-foil architecture

The block diagram of the proposed RFID system for temperature monitoring applications is presented in Figure 48. The smart temperature sensor system-on-foil exploits Printed Electronics (PE) able to communicate environment temperature readings to a base station reader (based on Si off-the-shelf components) via RFID. The RF wireless communication link is established by means of two inductively coupled antennas, here defined as reader and tag antennas. The reader generates the RF carrier, which is further used by the tag for energy harvesting and for data transmission via backscattering modulation. In order to make the system-on-foil suitable for the target applications, a temperature sensitive element needs to be embedded on the RFID tag. This can also be printed exploiting inorganic materials or organic compounds, reducing both final cost and footprint, and simplifying the system integration. Some Analog Frontend Electronics (AFE) is required to readout the temperature sensor and condition the analog signal for the next step of the data acquisition chain. In order to transform the analog sensor signal in a more robust digital representation, an Analog-to-Digital Converter (ADC) needs to be included in the system. Due to its functionality and circuit complexity (in terms of transistor count), this module represents the core of the RFID tag electronics. The digitized signal produced by the ADC is typically represented in the form of a digital word. Alternatively, a two-level Pulse Width Modulation (PWM) representation is also a possible solution. In order to enable the transmission of the data, a backscattering

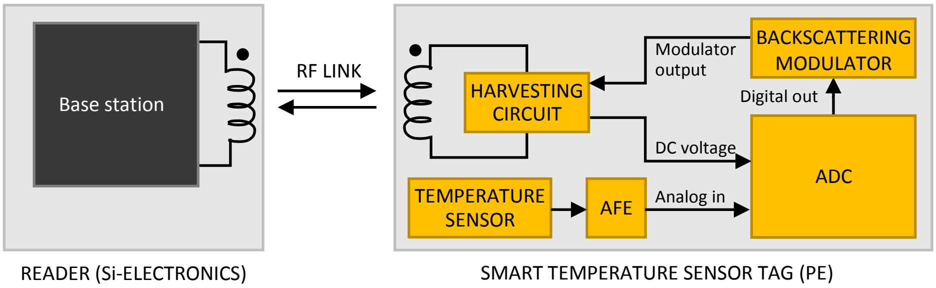


Figure 48. Block diagram of the proposed RFID system, comprising the smart temperature sensor and the base station reader.

modulator circuit is also included in the system. It is worth mentioning that the proposed system is not compliant with standard NFC protocols such as ISO/IEC 14443-A, and therefore a conventional NFC reader cannot be used. This is a direct consequence of the limited yield and speed performance of the OTFT, which at the current state-of-the-art are not sufficient to satisfy these application requirements.

5.2.1 Printed temperature sensors

Several types of temperature sensors fabricated with organic materials have been demonstrated in literature. OTFT based temperature sensors exploit the dependence of the organic semiconductor mobility on temperature [115][116][117]. OTFT-based temperature sensors typically feature modest sensitivity and non-linear response, but enable low-power consumption and compact footprint implementations. Besides, their response is typically dependent on the bias conditions of the circuit, making their use in RFIDs with unregulated supply voltages less attractive. In addition, the large 1/f noise contribution poses limitation on the achievable temperature resolution.

An alternative approach is proposed in [118] to develop organic temperature sensors by exploiting asymmetric Metal Insulator Semiconductor Metal (MISM) capacitor. The presence of the organic semiconductor layer introduces a large positive temperature coefficient in the device capacitance, making the MIMS capacitor suitable for temperature sensing applications. This approach benefits from the simplicity of the device structure, from the large temperature coefficient ($\sim 2 \times 10^{-2}$ °C^{-1}), and from good linearity performance. However, also in this case the sensor response is a function of the bias conditions.

Most of the printed temperature sensors presented in literature are based on resistors manufactured with organic and inorganic materials, which exhibit a resistance dependence with the temperature. In particular, resistors fabricated with metallic inks on flexible substrates can achieve extremely linear behavior, at the expense of typically low Temperature Coefficient (TC$\sim$ 10^{-3} °C^{-1}) [119]. Composite materials such as graphite-Polydimethylsiloxane can be used to fabricate printed resistors with larger positive TC ($\sim$ 10^{-2} °C^{-1}) [120], while inks based on poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS), carbon nanotubes and graphene, allow the development of resistors with negative temperature coefficients [121][122]. The use of printed resistors as temperature sensors provides few advantages: first, despite additional fabrication steps are required, their integration in the OTFT manufacturing process is typically simple, thanks to their compatibility with the printing process. Second, the availability of resistors with different temperature coefficients further enables the use of ratiometric readout circuits which output relies on the ratio of the passive component values. As direct consequence, the accuracy of the temperature measurement depends at first approximation on the resistor ratio, relaxing the accuracy requirements of the AFE. However, unwanted effects such as time drift, hysteresis and supply voltage dependency, might reduce the effectiveness of this approach.

In this work two resistive elements featuring opposite and very different temperature coefficients have been selected for the temperature sensing. Resistors with positive TC can be fabricated with a serpentine geometry by screen-printing a carbon-based ink (Dupont 7292) on 125 µm thick PEN substrate. In this material, the increase of the temperature induces an expansion of the polymer matrix, which affects its charge transport properties and further leads to an increase of the resistance. After the material deposition, an annealing process of 15 minutes at 115°C is necessary to evaporate the solvents present in the inks, and thus allow a good physical cohesion of the material and sufficient adhesion on the substrate. The thickness and the width of printed resistive segments are respectively 7 µm and 500 µm, while the sheet resistance is 10-18 kΩ/□. These resistors exhibit a non-linear temperature dependence, which can be approximated at first order with the relatively large TC $\sim 9\ 10^{-3}\ °C^{-1}$ (within the target temperature range).

The second type of printed resistor utilized in this work features a negative TC in the order of $\sim -6\ 10^{-4}\ °C^{-1}$ (in the target temperature range). These devices are also screen-printed with a serpentine layout on 125 µm thick PEN substrate, using a carbon-based ink (Creative Materials 112-47), which ensures excellent thermal stability performance. Also in this case, the printing is followed by an annealing process of 15 minutes at 115°C on a hot plate. The width of the printed resistive segments is about 570 µm, while the typical thickness value is 14 µm with variations between 10 µm to 16 µm. In these printing conditions, this type of resistor exhibits a typical sheet resistance value of 250 kΩ/□.

5.3 Design of the system-on-foil

The design of the proposed system-on-foil for temperature monitoring applications is further organized in two parts: at first the system architecture is derived and insights for the design of the sub modules are provided. In the second part, the circuit implementation at transistor-level is discussed.

For completeness, it should be mentioned that the OTFT model provided in Chapter 3 does not account for the effects of temperature variations on devices. Similarly, the behavior of the organic semiconductor at high operation frequencies is not included in the transistor model. Therefore, the design and simulations of the system have been done assuming room temperature and low-frequency of operation.

5.3.1 System-level design

The core of the system is the data acquisition chain which comprises the temperature sensors, the AFE and the analog to digital converter. In our case, the last block is replaced by an analog to PWM converter (Figure 48). A time-based interface exploiting a first-order Bang Bang Phase-Locked Loop (BBPLL) sensor to PWM converter [123] has been chosen in this work to interface the resistive temperature sensors and perform the analog to PWM conversion. This time-based interface architecture is highly-digital and offers several advantages in terms of circuit complexity, area occupation, power consumption, robustness against transistor parameter variability and scalability towards smaller channel length OTFT technologies. More specifically, the BBPLL approach is chosen here for its minimalistic needs in terms of hardware complexity, which greatly benefits the circuit yield.

The first-order BBPLL architecture [124] (Figure 49(a)) requires indeed only two oscillators (Sensor Controlled Oscillator (SCO) and Feedback Controlled Oscillator (FCO)) and a binary Phase Detector (PD). These building blocks can be implemented exploiting a small number of digital logic gates, which are typically less sensitive to the OTFT parameter variability than analog circuits. Furthermore, the layouts of these digital blocks can be co-optimized to achieve an overall compact footprint. The BBPLL intrinsically performs a sensor signal-to-PWM conversion, which further allows the use of the output bitstream to drive the backscattering modulator.

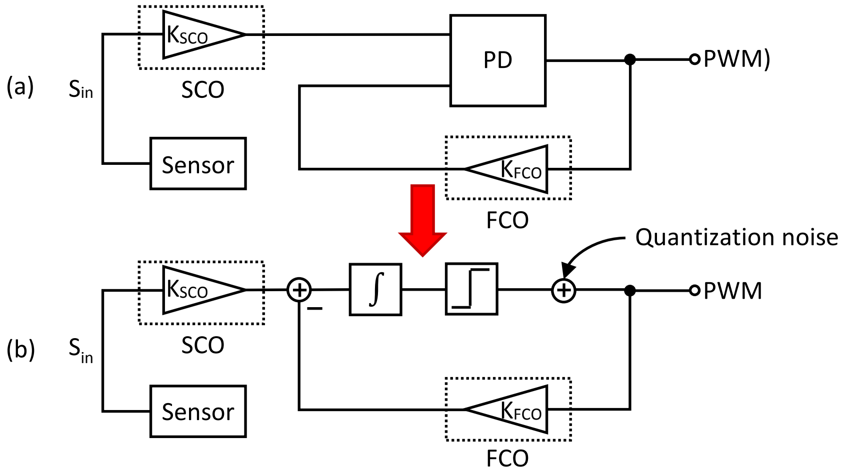


Figure 49. (a) Simplified block diagram of the first-order BBPLL converter and (b) its analogy with first-order synchronous ΔΣ modulator architecture.

This architecture is particularly attractive also from the perspective of low-power consumption. Indeed, the BBPLL benefits from the absence of an N-bit register, otherwise required in architectures such as integrating double slope and Successive-Approximation-Register (SAR) ADCs. As discussed in Chapter 4, sequential logic implemented with unipolar transistor technology is typically power hungry and demanding in terms of area and number of devices.

The conventional BBPLL architecture (Figure 49(a)) makes use of Sensor Controlled Oscillator (SCO) which oscillation frequency f_{SCO} is related to the sensor signal, and a Feedback Controlled Oscillator (FCO) in which the frequency oscillation symmetrically deviates from a reference value f_{FCO} according to the digital output signal of the PD. Therefore, the FCO operates at two frequencies, respectively f_{FCO+} and f_{FCO-}, which also define the lock range of the PLL. The PD measures the phase difference between the SCO and FCO, producing a PWM bitstream. The duty cycle D_T of the output bitstream, contains information on the relative position of f_{SCO} with respect to the frequency lock range (22):

$$f_{SCO} = D_T f_{FCO-} + (1 - D_T) f_{FCO+} \tag{22}$$

Apart from the sensing element (based on the positive TC resistor R_{SENS}) connected here to the SCO, the proposed time-based interface requires two reference oscillation frequencies (f_{FCO+} and f_{FCO-}) with low dependency from temperature and supply voltage variations. According to Eq. (22), the knowledge of the lock range boundaries allows to univocally relate the duty cycle of the output bitstream to the frequency deviation of the SCO, and thus to the temperature variation. The availability of such frequency references source is the key element, to develop system architectures which do not rely on a voltage and current reference circuits. It is clear that the choice of the oscillator typology is crucial. The strategy adopted in this work relies on the desensitization of the circuit performance from the variation of the OTFT parameters. This can be achieved by exploiting passive feedback networks to set the circuit performance, enhancing the robustness against the variability of the transistors. Indeed, passive components are typically more stable than OTFTs and can be manufactured with good reproducibility [55]. In this way, the oscillation frequency, the frequency gain factor K_{XCO} and the stability of both SCO and FCO are determined at first approximation only from passives. As direct consequence, the extension of the PLL lock range needs to be designed to accommodate the frequency deviation of the SCO (mainly dependent on the TC of R_{SENS}) along the temperature span of interest. The negative TC resistor (defined here as R_{REF}) thanks to its low temperature coefficient, is instead employed in the FCO to ensure the stability of the lock range along the temperature range.

While the target temperature range introduces constrains on the BBPLL lock range, the requirement on the temperature resolution affects the conversion time (t_{CONV}) of the smart temperature sensor. Indeed, in BBPLL architectures oversampling can be used to achieve higher conversion resolutions, at the expense of a larger conversion time. Thanks to the inherent integration between frequency and phase implemented in the PD, the system resembles a synchronous ΔΣ modulator (Figure 49(b)) with first-order quantization noise shaping [124]. According to [124] the theoretical achievable Signal to Quantization Noise Ratio (SQNR) can be calculated by (23)

$$\mathrm{SQNR[dB]} = 2.6 + 30\log(\mathrm{OSR}) \tag{23}$$

where OSR is the oversampling ratio defined here as $(f_{SCO}/2)/(2BW)$, being BW the 3dB cut-off frequency of the low-pass filter placed at the reader side, to extract the temperature information from the demodulated bitstream. If a flat moving average filter with a window length equal to t_{CONV} is used for this purpose, the associated cut-off frequency reduces to $BW \approx 0.44/\ t_{CONV}$.

The achievable SNR is in general lower than the SQNR, due to the presence of other noise sources, such as the phase noise of the oscillators. As discussed in [124] the phase noise can be modelled with an equivalent noise source N_{IRPN} at the input of the oscillator. The corresponding integrated output noise of the system is then determined by the sum of the quantization noise and the phase noise contributions. Under the assumption that the phase noise components are the dominant ones and N_{IRPN} is a white noise source, the achievable SNR reduces to [124] (24):

$$\mathrm{SNR[dB]} \cong 20\log\left(\frac{\mathrm{K_{SCO}S_{in}}}{2\mathrm{N_{IRPN}}}\right) + 10\log(\mathrm{OSR}) \quad (24)$$

where S_{in} is the amplitude of the sensor signal (assumed here as sinewave) and K_{SCO} is the frequency gain factor of the SCO. As highlighted by Eq. (24) the SNR increases only 3dB when doubling of the OSR, instead of 9dB improvement as initially predicted by Eq. (23), reducing the benefits of the quantization noise-shaping technique. Interestingly, Eq. (24) further reveals that for a given OSR, the SNR achieved by the BBPLL converter is strongly dependent on the performance of the oscillators.

The design of the temperature-to-duty cycle conversion chain should also minimize the total power consumption. Indeed, the power required for the data conversion needs to be harvested by the tag, rectifying the RF carrier provided by the reader. At the current state-of-the-art, only the Low Frequency (LF) and High Frequency (HF) bands for RFID communication are at reach with organic transistor technologies. Both LF and HF RFID solutions operating respectively at 125 kHz and 13.56 MHz, have been demonstrated with organic technologies [39][56][113][125]. Typically LF RFID tags achieve shorter reading ranges compared to their HF counterparts and require additional care in the fabrication of the antenna, in order to maintain a sufficiently high quality factor, leading to a higher device cost. On the other hand, as the frequency of the RF carrier increases, the efficiency of the harvesting circuit reduces [39][125], posing additional limitations on the power budget for the system. Aiming at a low-cost solution, the RFID tag proposed in this work has been designed to operate in the 13.56 MHz HF band.

The backscattering transmission between the tag and the base station reader is also performed using the RF communication link at 13.56 MHz. The load modulation approach is used, which exploits the variation of the transponder impedance according to the digital code which should be transmitted. The modulation of the impedance can be easily detected from a demodulator placed on the reader. In order to enable backscattering, the load modulator can be placed after the harvesting circuit (Figure 48) at the so called DC side, or directly connected to the tag antenna, at the AC side. The two possible solutions lead to different design constraints. A load modulator placed at the AC side guarantees more versatility, enabling the use of both Amplitude Shift Keying (ASK) and Phase Shift Keying (PSK) modulation. However, the use of OTFTs as switches for the implementation of the backscattering modulator is challenging due to the large voltage amplitude required by the harvesting circuit [39][58], which makes the transistors difficult to be turned-off. The effectiveness of the switches is further reduced by the limited speed of the OTFTs (typical unity-gain frequency is < ~MHz). Even implementations which exploit the modulation of the transistor gate capacitance with the bias conditions are unpractical due to the frequency dependent behavior of the organic semiconductor [89]. All these limitations reduce the applicability of the conventional modulation schemes at the AC side [126], making the design of this circuit extremely challenging. On the other hand, the implementation of the backscattering circuit at the DC side, is typically less critical but it can only be used in combination with ASK modulation techniques. The major drawback of this solution is the poor isolation between the modulator output and the rectified DC voltage (Figure 48). This further leads the tag to self-modulate its rectified supply voltage, which could detrimentally affect the functionality of the core electronics. The solution proposed in this work to alleviate this issue relies on the introduction of a second harvesting circuit which independently supplies the backscattering modulator, improving the isolation between modulator and the rectified DC voltage supplied to the core circuit.

5.3.2 Circuit implementation

BBPLL converter. As previously discussed, the implementation of the oscillators is crucial for the performance of the BBPLL converter. The SCO and FCO are here implemented as astable multivibrators (Figure 50(a)) rather than ring oscillators, due to the reduced performance sensitivity of the latter to transistor parameter variability. The multivibrator makes use of two not-gates (I1, I2) based on diode-connected inverters (Figure 50(b)) and a passive RC feedback network. The resistance-to-frequency transfer characteristic of this oscillator topology exhibits an inverse proportionality law, expressed by Eq. (25):

$$f_{XCO} = \left(2RC\ln\left(-\frac{V_{TRIP}+V_{DD}}{V_{TRIP}-V_{DD}}\right)\right)^{-1} \tag{25}$$

Here V_{TRIP} is the trip point of the two not-gates, and V_{DD} the positive supply voltage. Several conditions need to be verified in order to ensure the validity of Eq. (25): first, both not-gates must exhibit rail-to-rail output voltage swing. Second, the oscillation period $1/f_{XCO}$ should be significantly larger than the propagation delay associated to each gate. Third, the gates I_1 and I_2 need to be able to drive the RC feedback network with small enough output impedance, avoiding loading effects. The first and third conditions are satisfied here by choosing a number of diode-connected inverters which guarantees sufficient voltage gain and by introducing a push-pull output stage in each not-gate, which lowers the output impedance and saturates the output voltage to V_{DD} or G_{ND}. The second condition poses instead the major limitation to the maximum achievable oscillation frequency. Interestingly, Eq. (25) provides also insights on the stability of the oscillation frequency to supply voltage and transistor parameter variations. By choosing the correct size ratio N between driver and load transistors in the diode-connected inverters (Section 4.2), the trip point V_{TRIP} of the not-gates (I_1 and I_2) can be tuned at around 1/2 V_{DD}, further leading to an oscillation frequency which is at first approximation, independent from the supply voltage. Even in presence of Process-Voltage-Temperature (PVT) variations, the weak logarithmic dependence of the f_{XCO} on V_{TRIP} ensures that the frequency deviation remains dominated by the RC product. The choice of this oscillator typology leads to the gate-level schematic of the proposed temperature-to-PWM converter depicted in Figure 51(a).

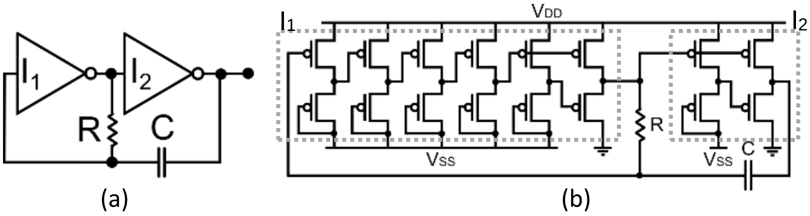


Figure 50. (a) Gate-level schematic of the proposed astable multivibrator oscillator. (b) Transistor level implementation of the oscillator.

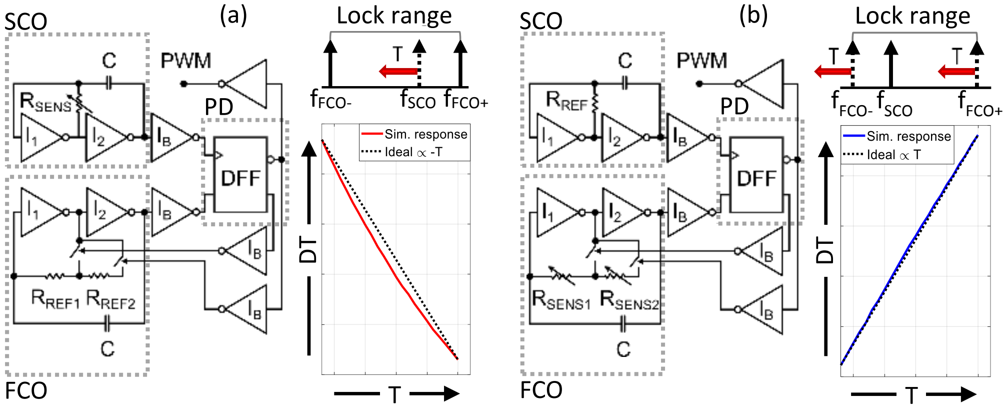


Figure 51. Block diagram of the temperature-to-duty cycle converter, based on the conventional BBPLL architecture (a) and (b) modified architecture with the proposed linearization technique.

The conventional choice of using the sensing element (R_{SENS}) in the SCO and the more temperature-stable negative TC resistors (R_{REF1}, R_{REF2}) in the FCO [124] would result an intrinsic non-linear response ($DT \propto 1/T$) of the full temperature to duty-cycle converter (Figure 51 (a)). The analytical response of the converter can be computed indeed combing (22) and (25) in (26):

$$D_T = \frac{R_{REF1}}{R_{REF2}}\left(\frac{R_{REF1}+R_{REFE2}}{R_{SENS}} - 1\right) \tag{26}$$

To linearize the converter response ($DT \propto T$), it is sufficient to exchange the position of the resistors in the oscillators (Figure 51(b)). In this way the SCO serves as temperature-stable reference oscillator, while the lock range controlled by the FCO shifts jointly with the temperature variation, and the transfer characteristic is effectively linearized, simplifying the calibration process (Figure 51 (b)). In this case, the response of the converter is given by (27):

$$D_T = \frac{R_{SENS1}}{R_{SENS2}}\left(\frac{R_{SENS1}+R_{SENS2}}{R_{REF}} - 1\right) \tag{27}$$

In the configuration shown in Figure 51(b), the lock range is defined by the ratio of the two positive TC resistors, nominally 11 MΩ and 27 MΩ at 0°C. The extension of the lock range is designed to ensure the correct functionality of the BBPLL converter over the target temperature range. Two switches are used to dynamically change the resistors in the feedback network, allowing the FCO to run at f_{FCO+} or f_{FCO-} depending on the feedback value. The SCO employs a negative TC resistor having a nominal value of 37 MΩ at 0°C. Both oscillators are equipped with a 330 pF capacitor C. As long as the BBPLL remains in the lock condition, both oscillators operate at a nearly constant average oscillation frequency of 37 Hz. Moreover, according to circuit simulation results, for conversion time $t_{CONV} \leq 2$ s, the noise performance of the BBPLL converter are still dominated by the quantization noise contribution. For a conversion time of 2 s the converter achieves a simulated SNR of 48.5dB, which is in line with the value predicted by Eq. (23). In these conditions, the simulated temperature resolution of the converter is 0.124 K_{RMS}. Bootstrapped inverters I_B (Figure 51(b)) are employed as drivers for the feedback switches and as voltage translators to interface the oscillators to the phase detector, thanks to their high gain performance and the rail-to-rail output swing. The binary PD is implemented with a D-type Flip Flop (DFF) based on pseudo-static approach (Figure 32(a)). This topology provides a good trade-off between complexity, speed, current consumption and reliability. As analyzed in Chapter 4, despite fully dynamic implementations are superior in several aspects, their functionality at low operation frequency could become critical, exposing the circuit to potential soft failures. One of the major design specifications for the PD refers to the propagation delay. In order to prevent the introduction of non-linear components in the BBPLL temperature-to-duty cycle response, the propagation delay of the DFF needs to be designed sufficiently smaller than the period of the clock signal.

The complete BBPLL requires 69 OTFTs and 7 capacitors, occupying an area of 756 mm^2.

Radio-Frequency section: in order to relax the fabrication process of the entire prototype, a conventional off-chip antenna manufactured on FR-4 substrate and compatible with an ISO credit card size (5 x 8 cm^2) has been here selected. The antenna features a 3 turn rectangular geometry, an equivalent inductance of L_{ANT}=1.08 µH, a parallel capacitance of C_{ANT}=1.32 pF and a DC resistance of R_{ANT}=1.65 Ω (Figure 52), which further lead to an unloaded quality factor of Q=55.8 at the operating frequency of 13.56 MHz.

The schematic of the RF section of the proposed smart temperature sensor tag, is shown in Figure 52. The harvesting circuit (Figure 52) comprises four half-wave rectifiers to independently generate the dual supply voltages for the converter and the backscattering modulator. The rectifiers are here implemented with diode-connected transistors.

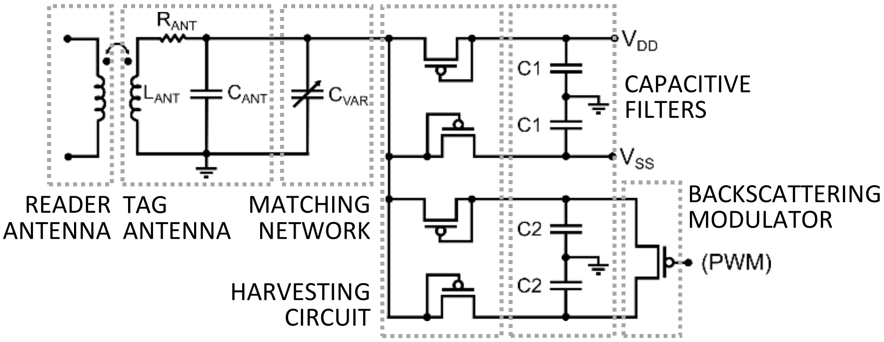


Figure 52. Transistor level schematic of the tag RF section.

Despite rectifier architectures based on threshold cancellation techniques lead to a substantial performance improvement [58], conventional diode rectifiers are typically more reliable, and therefore their use is preferred here. The transistors employed in the rectifiers have been overdesigned, in order to accommodate the performance loss of the organic semiconductor which typically occurs at high frequency of operation [39]. A capacitive filter implemented with off-the-shelf SMD film capacitors (C1=20 nF, C2= 1 nF) is added at the outputs of each rectifier, to reduce the voltage ripple of the unregulated DC voltage. The availability of two independent filters can be exploited to mitigate the effects of the supply voltage modulation introduced by the backscattering transmission. A discrete capacitive matching network is also required at the input of the rectifier circuit to tune the resonance frequency of the LC tank at 13.56 MHz. For this purpose, the required equivalent capacitance is analytically calculated to be 130 pF. The equivalent input capacitance of the rectifier circuits provides a significant contribution to this capacitance value. The total stray capacitance of each rectifier can be estimated from the C_{GS} of the diode-connected transistors operating in the saturation region. However, this estimation is typically inaccurate. Indeed, as reported in literature [89], the OTFT gate capacitance typically decreases at relatively high frequency of operation. Therefore, in order to correctly tune the resonance frequency of the tag, a 60 pF discrete variable capacitor C_{VAR} has been also included in the matching network and placed in parallel to the tag antenna.

At last, a simple implementation is proposed for the backscattering modulator (Figure 52). An OTFT operating as a switch is connect between the supply voltage rails dedicated to the modulator, and further driven by the PWM signal produced by the BBPLL converter. The switch provides an addition current path which is used to modulate the power consumption of the tag, and thus its equivalent resistance referred to the reader side, according to the converter output bitstream.

5.4 Measurement results

The proposed smart temperature sensor has been fabricated with the gravure-printed OTFT technology presented in Chapter 2. In order to simply the characterization of the sub modules of the system, the BBPLL converter and the RF section (comprising the harvesting circuit and the backscattering modulator) have been laid out in separated structures and included in the same mask set. A PCB manufactured on FR-4 substrates has been designed to interface the flexible electronics with both types of printed resistors and the tag antenna. The photograph of the prototype is provided in Figure 53.

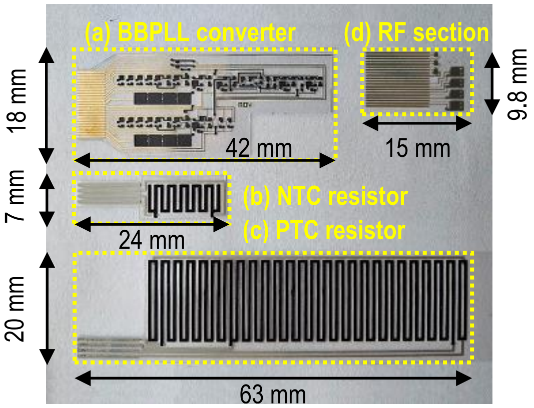


Figure 53. Photograph of the proposed printed system-on-foil. (a) BBPLL converter, (b) negative TC resistor, (c) positive TC resistor and (d) RF section comprising the harvesting circuit and the backscattering modulator.

The printed resistors, BBPLL converter and RF section (excluding the tag antenna) require a cumulative area of 23.3 cm^2.

Stability of the oscillation frequency: the frequency stability of the proposed typology of oscillators to power supply and temperature variations has been validated at first. The circuit has been equipped with a negative TC resistor and accommodated in a cavity between two aluminum plates which also contains a PT1000 platinum Resistance Temperature Detector (RTD) used here as temperature reference thermometer. This structure has been placed on a thermal controlled chuck which is further connected to the Temptronic TP0314B in order to perform temperature sweep characterizations. A plastic coverage has been applied on the device under test in order to realize a chamber provided with dry air purge system, used to reduce the moisture and prevent condensation issues at low measurement temperatures.

The frequency deviations recorded from a supply voltage and a temperature sweeps are presented respectively in Figure 54(a) and (b). The measurement results reveal that the symmetric variation of the supply voltage from ±15 V to ±21 V, induces at room temperature a maximum relative deviation on the oscillation frequency of only 1%. Similarly, the variation of the temperature over the target range, affects the oscillator circuit with a frequency deviation of about 5.1%, partially caused by the resistance variation of the negative TC printed resistor.

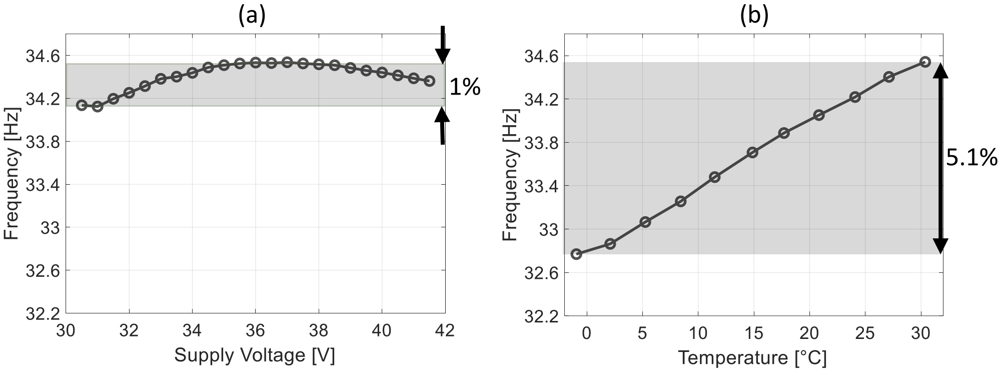


Figure 54. Measured oscillator frequency dependence to (a) supply voltage and (b) temperature variations.

Smart temperature sensor: the measurement setup proposed for the evaluation of the oscillator performance has been also used to characterize the BBPLL converter. An external power supply has been utilized to provide the dual supply voltage required by the circuit. The average current consumption recorded at room temperature with a supply voltage of ±18 V is equal to 56 µA, which leads to an average power consumption of 2 mW.

In these conditions, the Power Spectral Density (PSD) extracted from the recorded output bitstream of the converter is shown in Figure 55 (a). The converter's noise floor is dominated by the phase noise of the oscillators, while a first-order noise shaping due to the BBPLL is clearly recognizable. In order to remove the effects of the ambient temperature on the output bitstream, the resolution was determined from the difference between two successive measurements, according to a two-sample Allan deviation. The measured sensor resolution is plotted versus conversion time in Figure 55 (b). These measurement results clearly show that the impact of the quantization noise on the resolution becomes dominant for integration time < 4 s. For a conversion time of 2 s the proposed smart temperature sensor achieves a resolution of 270 mK$_{RMS}$, which leads to a resolution Figure of Merit (FoM) of 281 µJK^2.

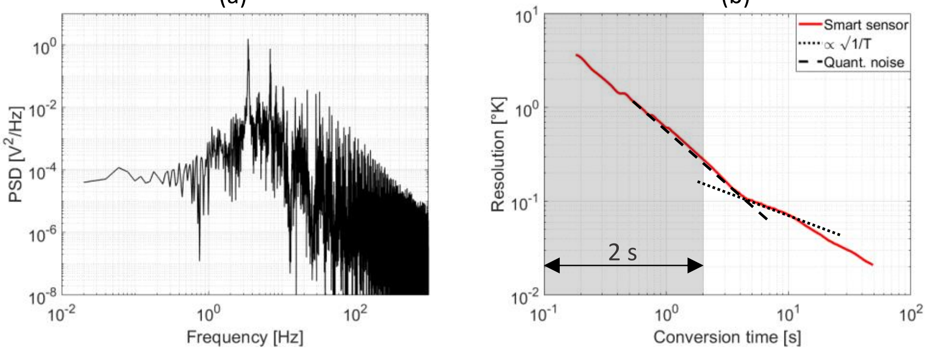

(a) (b)

Figure 55. (a) Power spectral density extracted from the output bitstream. (b) Temperature resolution (red) versus conversion time of the proposed smart temperature sensor. Impact of different noise contributions on the temperature resolution: quantization noise (black dashed line) and thermal noise (dotted black line). In the inset, the parameter T is the temperature.

As discussed in Section 5.3.2 the frequency dependence of the oscillators and thus the converter response, are mainly determined by the temperature-to-resistance characteristic of the printed sensors. However, the printed resistors employed in this work exhibit a non-linear response. In addition, both resistors and capacitors required in the oscillator feedback networks are subjected to parameter spread. Therefore, in order to remove the systematic sensor non-linearity and improve the overall accuracy of the smart temperature sensor, multi-point calibration techniques need to be applied.

To correct the systematic non-linearity introduced by the sensing elements, the knowledge of both printed resistor characteristics is required. Hence, 8 samples of each resistor type manufactured during the same campaign have been characterized in the temperature range between 0°C and 30°C, with steps of 3°C. Next, in order to remove the effect of the parameter spread, one of the measured positive TC resistor curves has been assumed as reference and used to correct the offset and gain error (first-order linear fit) of the others. The same procedure has been applied to the negative TC resistors. The results for the positive and negative TC resistors are presented in Figure 56 (a) and Figure 57(a), respectively. The corresponding average curves extracted from these data sets have been reproduced by means of fourth-order polynomial fitting. The results are provided for both resistors in Figure 56 (b) and Figure 57(b). The polynomial expressions describing the temperature-to-resistance relationship of R_{SENSX} and R_{REF}, have been substituted in (27) and used in combination with multi-point calibration to improve the sensor accuracy. After systematic non-linearity correction and two-point calibration (at 3°C and 27°C), the proposed temperature sensor achieves a 3σ inaccuracy of ±1.6°C (Figure 58(a)), evaluated over a population of 15 samples, manufactured in the same campaign. The 3σ inaccuracy can be further reduced to ±1.2°C (Figure 58(a)) by allowing the use of a third calibration point (at 15°C). It is worth noticing that the temperature range of analysis has been here slightly reduced (3°C - 27°C) due to the parameter spread associated to the feedback networks of the oscillators, which affects the correct functionality of the converter at the extremes of the lock range.

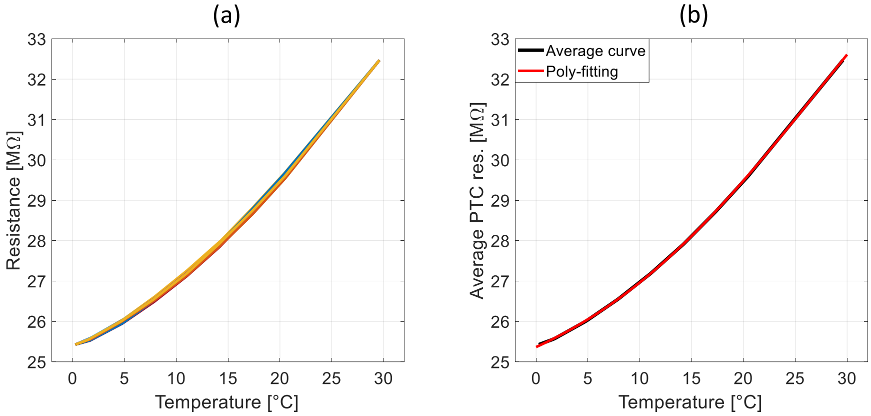


Figure 56. (a) Measured resistance versus temperature characteristics of 8 positive TC printed resistors, after first-order linear fit. (b) Corresponding average resistance (black) and its fourth-order polynomial fit (red) versus temperature curves.

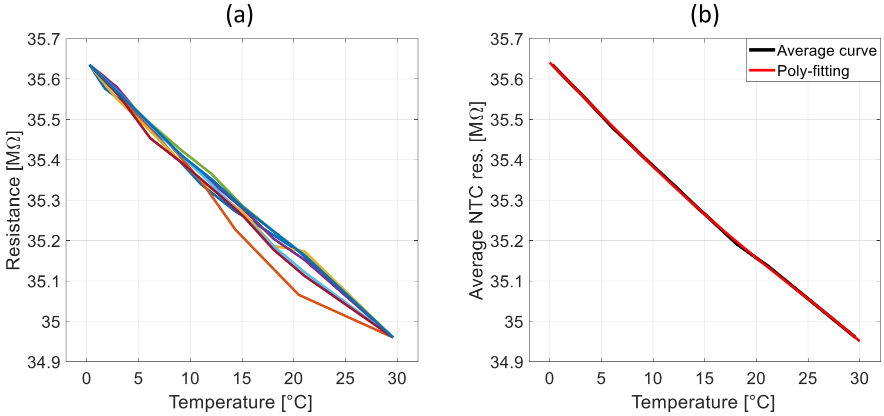


Figure 57. (a) Measured resistance versus temperature characteristics of 8 negative TC printed resistors, after first-order linear fit. (b) Corresponding average resistance versus temperature curve and its fourth-order polynomial fit (red) versus temperature curves.

However, in the perspective of using the smart temperature sensor on an RFID tag with un-regulated supply voltages, the sensitivity of the overall systems to the supply variations needs also to be evaluated. Hence, the response of the very same smart temperature sensor has been characterized over the target temperature range and at different supply voltages, which are respectively ±15 V, ±18 V and ±21 V (Figure 59(a)). After systematic non-linearity correction and 3-point calibration, the relative temperature error has been calculated assuming the characteristics recorded at ±18 V as reference. The measurements results are shown in Figure 59 (b). The outcome of this analysis reveals that when the smart sensor is operated with large supply voltage variations, the maximum relative error in the temperature readings can exceed 3°C. Indeed, lowering the supply voltage down to ±15 V causes a significant reduction of the overdrive voltages of the feedback switches, which leads to higher R_{ON} values. This effect is further exacerbated by the reduction of the carrier mobility which occurs at a relative low temperature. As consequence, the converter response suffers from offset and gain error with respect to the reference characteristic (recorded at a supply voltage of ±18 V). On the other hand, the increase of the converter supply voltage to ±21 V, leads to a relative error curve with opposite sign, while the converter performance is less affected. For a wide temperature range the converter response closely follows the reference curve with a maximum absolute value of the relative temperature error of 0.5°C, which approaches 1°C only at the lower boundary of the target temperature range. In order to further reduce the sensitivity of the converter to the supply variations, a lower R_{ON} value of the feedback switches would be required, in order to accommodate the reduction of the semiconductor carrier mobility occurring at relative low temperature. It should be highlighted however, that the transistor model introduced in Chapter 3 does not account for the effects of the temperature variation on the device performance yet.

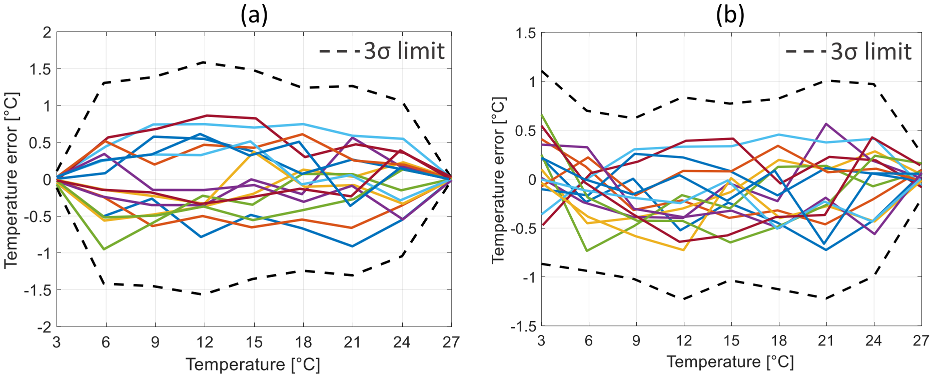


Figure 58. Inaccuracy of 15 measured smart printed temperature sensor after systematic non-linearity removal and (a) 2-point calibration, (b) 3-point calibration.

Smart temperature sensor on RFID: as a proof of concept, the smart temperature sensor together with the RF section has been also evaluated via wireless communication. The tag and reader antennas have been placed at a relative distance of about 2 cm. The resonance frequency of the tag has been centered on the HF band (13.56 MHz) by means of the variable capacitance C_{VAR} (Figure 52), and the amplitude of the RF carrier regulated to reach 65 $V_{PEAK\text{-}TO\text{-}PEAK}$ at the input of the tag harvesting circuit. This voltage level ensures at room temperature a rectified DC voltage of ±18 V. The reader is equipped with an envelope detector followed by an active bandpass filter to perform ASK signal demodulation, selecting the signal bandwidth of interest (1Hz - 500Hz) and providing voltage amplification (11V/V).

A typical PWM signal demodulated by the reader and recorded during the characterization of the sensor is shown in Figure 60(a). It is worth mentioning, that in order to correctly perform the temperature readout, the system requires about 4 s.

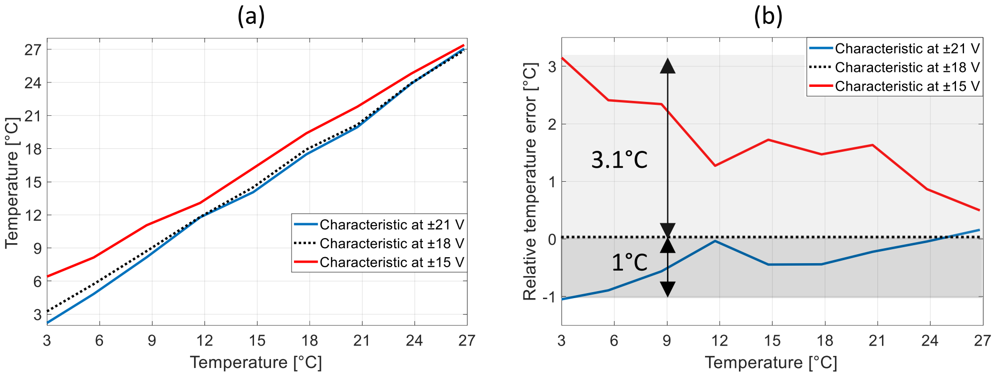


Figure 59. (a) Temperature characteristics of the same smart temperature sensor, respectively measured at a supply voltage ±15 V, ±18 V and ±21 V. The characteristics are corrected with systematic non-linearity compensation and 3-point calibration performed on the curve recorded at supply voltage ±18 V, assumed here as reference. (b) Corresponding relative temperature error with respect to the reference characteristic.

This time depends on the time constants of the capacitive filters placed after the rectifiers to suppress the ripple of the supply voltage induced by the backscattering transmission, and on the conversion time. Indeed the settling time required by the supply voltage is about 2 s, while 2 additional seconds are required to readout the temperature with the target resolution.

The results of the sensor characterization performed via wireless communication link are presented in Figure 60(b) after systematic non-linearity correction and multi-point calibration. The inaccuracy achieved with two and three-point calibration is respectively ±0.7°C and ±0.5°C, both in line with the results provided in the previous paragraph.

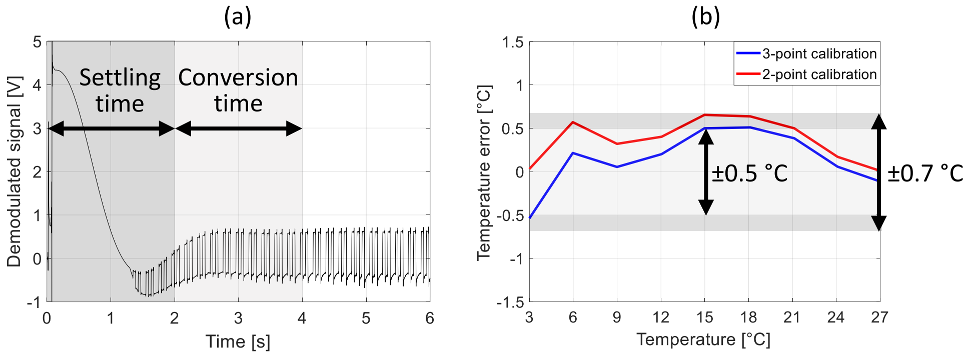


Figure 60. (a) Demodulated PWM signal recorded at the reader side during the sensor characterization. (b) Inaccuracy of the smart temperature sensor on RFID, extracted after systematic non-linearity removal and 2-point (red) and 3-point calibration (blue).

5.5 Benchmark

To the author's knowledge, all published temperature sensor interfaces based on printed TFTs published to-date provide a 1 bit digital output [112] [113] (Table 9). These devices are based on Write-Once-Read-Many (WORM) architecture, capable to detect when the environmental temperature exceeds a fixed threshold value, recording this status in a 1 bit memory. However, these systems-on-foil are not compatible with applications which require dynamic temperature monitoring. This work presents for the first time a printed smart sensor capable of sensing the environmental temperature, converting it in a digital representation based on binary PWM, which further enables a robust wireless transmission via RF link at 13.56MHz. Compared to prior state-of-the art, this work makes use of printed organic electronics to develop both the smart temperature sensor and its RF section, comprising the harvesting circuit and the backscattering modulator. The use of the BBPLL converter allows to reduce the overall system complexity (in terms of transistor count) of 2.5x compared to one of the previous works based on OTFT technologies ([112], Table 9). Similar improvement is expected also in comparison with [113], in which however the number of OTFTs required by the architecture is not provided.

An interesting performance benchmark is obtained by comparing the temperature sensor proposed in this work with the one presented in [114], which is instead developed with a unipolar a-IGZO technology (Table 9). Both temperature sensors exploit a temperature-to-duty cycle converter architecture, which generate PWM output bitstreams. The converter presented in [114] requires 27x smaller area, operates over a larger temperature range and achieves a resolution FoM 5x better than the solution proposed in this work. However, the system in [114] is based on an a-IGZO TFT technology developed with high-resolution photolithography processes, which allows to largely reduce the feature sizes and the stray capacitances of the devices. Further advantages are associated to the carrier mobility of the IGZO semiconductor which is nearly 7 times better than the printed organic semiconductor employed in this work (Table 9). Despite these benefits, the converter architecture proposed in [114] is less suitable for integration in a RFID solution, due to the need of several biasing signals. In addition, from application perspective, the use of the a-IGZO technology, intrinsically leads to higher costs compare to the printed electronics.

Table 9. Smart temperature sensor performance summary and comparison to prior literature.

Parameter	Unit	This work		[112]	[113]	[114]
Technology		Unipolar Organic		Unipolar Organic***	Complementary Organic	Unipolar a-IGZO
Patterning method		Gravure		Lithography	Inkjet/gravure	Lithography
Carrier mobility	cm^2/Vs	2.2		N.A.	0.1	14
L_{MIN}	µm	10		5	35	15
Architecture		BBPLL		WORM	WORM	ADSM*
Number of TFTs		76		180	N.A.	N.A.
Embedded in RFID		Yes		Yes	No	No
RF communication	MHz	13.56		13.56	N.A.	N.A.
Output type		PWM		Digital Word	Digital Word	PWM
Temperature range	°C	3 - 27		20 - 100	0 - 80	0 - 70
Conversion time	s	2		N.A.	N.A.	0.1
Resolution	mK$_{RMS}$	270		N.A.	N.A.	540
Calibration points		2	3	N.A.	3	N.A
Inaccuracy (3σ)	°C	±1.6	±1.2	±10*	N.A.	±2.3*
Current consumption	µA	56		N.A.	N.A.	100
Supply voltage	V	36		20	28	20
Power consumption	mW	2		N.A.	N.A.	2
Area occupation	mm^2	2331		N.A.	N.A.	27.9**
Resolution FoM	µJK^2	291		N.A	N.A.	58

* Min/Max
** ADSM only
***In combination with Si-readout electronics

5.6 Conclusions

To the author's knowledge, this work presents for the first time in literature a smart temperature sensor on RFID, fabricated with a gravure-printed OTFT technology and potentially suitable for temperature monitoring in cold chain applications. The system is capable of sensing the environment temperature, converting it to a robust binary representation, and further transmitting the data to a base station reader, using ASK modulation on a 13.56 MHz RF communication link. Printed resistive sensors enable the temperature sensing, while the analog to PWM conversion relies on a BBPLL time-based interface. The design methodology and the proposed circuit implementation provide a simple but effective approach to mitigate the effects of the OTFT parameter variability on the system performance. The smart sensor achieves a resolution of 270 mK$_{RMS}$ with 2 s conversion time, a resolution FoM of 291 µJK^2 and a 3σ inaccuracy of ±1.6 °C from 3 °C to 27 °C, after systematic non-linearity removal and 2-point calibration. By using a third calibration point the 3σ inaccuracy can be lowered down to ±1.2 °C. Furthermore, the temperature reading performed by using the smart temperature sensor on a passive RFID tag, has been also demonstrated. The dependence of the sensor performance on supply variations, typical of unregulated RFID devices, has been considered at design stage, by developing a robust system architecture. Measurement results reveal however, that the sensor inaccuracy is partially impacted by the variation of the supply voltage and that an optimized sizing of the transistors employed in the feedback control network could further improve the immunity of the system to the supply variations.

These results demonstrate that printed electronics can be potentially used to fabricate inexpensive smart sensing devices for temperature monitoring applications, in which reduced temperature range and modest resolution and inaccuracy performance are required. In particular, the resolution and temperature range achieved by the proposed temperature sensor are suitable for most of the temperature monitoring applications for food and pharmaceutical products in cold chain. The operational temperature range of the proposed smart sensor-on-foil is defined by the extension of the PLL lock range, which however can be tuned by modifying the ratio of the positive TC resistors or by using sensing elements with lower sensitivity. In both cases, the extension of the operating range is achieved at the expense of the temperature resolution. Better resolution performance can be obtained by exploiting a larger OSR, which is however traded for longer conversion time or in the perspective of OTFT technology downscaling, by increasing the reference frequency of the SCO. The inaccuracy performance instead do not fully comply yet with the considered regulations.

6. Large-area proximity sensing surface

In this chapter a first-ever fully-printed large-area proximity sensing surface fabricated with organic materials which includes an AFE per pixel is presented. The core of the sensing surface is a 5x10 active sensor matrix obtained by lamination of printed organic pyroelectric sensors on foil (frontplane) with printed organic frontend electronics (backplane). The frontend electronics is used here to provide sensor signal amplification and unambiguous pixel addressing in order to maximize the SNR and reduce the pixel crosstalk. The proposed system-on-foil could be exploited to improve the safety in environments where humans and robots are cooperating or to develop artificial electronic skin for novel human-machine interaction applications.

Part of the content of this chapter has been published in [127]. However, the major results of the system evaluation provided in this chapter are intended to be submitted for journal publication (currently in preparation).

6.1 Introduction

Recent advances in printed electronics have brought the attention on the potential use of organic materials to fabricate innovative flexible and stretchable electronic skins for Human Machine Interface (HMI) and Human-Robot Interaction (HRI) applications. Indeed, organic materials can be processed at low-temperature, enabling the use of lightweight mechanically flexible plastic substrates, which could be further shaped to achieve the form factors required by these applications. Moreover, printing techniques can be employed in the fabrication process to achieve an overall cost reduction, allowing the electronics and the sensing elements to economically cover large-area surfaces while keeping the costs low. The possibility of manufacturing inexpensive distributed electronics is one of the major advantages of printed electronics compared to conventional Si counterparts. In addition, the availability of new sensing materials could further extend the sensing capabilities of e-skins to temperature and proximity sensing.

Even if these features make printed electronics attractive from the application point of view, only few printed large-area sensing surfaces embedding sensor arrays and active frontend electronics have been reported in the literature [128][129][130][131][132]. In most of these works the frontend electronics perform active-matrix addressing functionalities only. From the system architecture perspective, active matrix-addressing solutions are preferred to passive ones, due to their intrinsic higher sensor signal isolation between pixels. This permits unambiguous selection of the matrix pixels, which further facilitates the post processing of the acquired data. In order to fully exploit these advantages, the availability of OTFT technologies with high I_{ON}/I_{OFF} ratio and low noise performance, is of paramount importance. Even though simple and effective, the use of active-matrix addressing electronics only is not free from limitations. Sensing surfaces distributed over large-area are intrinsically susceptible to coupling with interference signals. These can introduce significant errors in the reconstruction process as the amplitude of the interferers can become comparable to the sensor signal levels. Additional limitations in the applicability of the active-matrix addressing architectures arise when the printed electronics is employed in combination with sensors producing a charge signal. Indeed, due to the relatively large feature sizes of the OTFTs, unwanted effects such as charge injection and clock feedthrough could severely affect the sensor signal integrity, leading to large errors during the readout process. It is also important to remark that the design of the active-matrix addressing electronics typically results in a trade-off between readout speed, signal integrity and achievable signal-to-noise ratio. Several of these limitations can be removed or partially mitigated by introducing in each pixel Analog Frontend Electronics (AFEs), at the cost of a higher circuit complexity (in terms of number of devices). The integration of AFEs in the matrix pixels can be used to achieve sensor signal amplification, improve the immunity to interferers and pixel crosstalk, and enhance the achievable SNR, employing noise reduction techniques such as chopping or correlated-double sampling.

In this scenario, a sensing surface suitable for infrared human proximity detection fabricated with printed organic materials and equipped with AFE in each pixel, has been demonstrated in this work for the first time in literature. This type of sensing surfaces is expected to play an important role to improve e.g. the safety in HRI applications. Indeed, current state-of-the-art industrial manipulators typically operate for safety reasons in separated environments from human workers. The use of inexpensive e-skins placed on the industrial manipulators and further provided with proximity sensing capabilities, could be used to increase the level of security (collision avoidance) and improve the interaction modalities. This would relax the constraint of physical separation between robots and humans, even in unstructured environments, leading to significant cost reductions for industry [133].

This Chapter is organized as follows: the system-on-foil architecture is presented in Section 6.2. The system level design of the large-area proximity sensing surface and its transistor level implementation is discussed in Section 6.3. Section 6.4 deals with the system integration, while measurement results are provided in Section 6.5. Conclusions are drawn in Section 6.6.

6.2 System-on-foil architecture

The simplified block diagram of the proposed proximity sensing surface is shown in Figure 61. The system-on-foil is built by lamination of a matrix of proximity sensors printed on foil (defined here as frontplane) with a second plastic sheet (called here backplane) containing the printed OTFT electronics (Figure 61). This approach allows to relax the fabrication process constraints for both sensors and electronics, preserving the mechanical flexibility of the final system. In addition, the availability of distributed large-area electronics is here exploited to enable the active addressing of the matrix. The pixel selection could be potentially driven by dedicated line drivers based on OTFTs on the periphery of the matrix, minimizing the number of interconnection with the Si-readout electronics and thus, leading to an overall cost reduction. The readout of the sensor matrix and digitalization of the analog outputs is performed with Si-electronics, based here on off-the-shelf components.

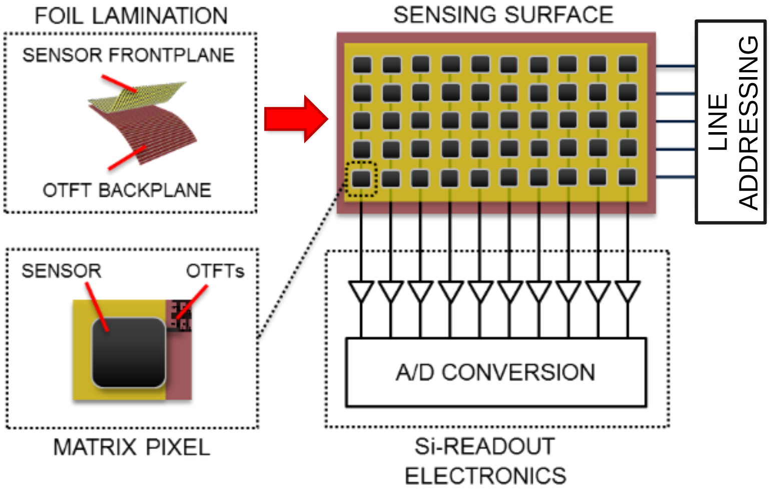


Figure 61. Block diagram of the proposed printed proximity sensing surface

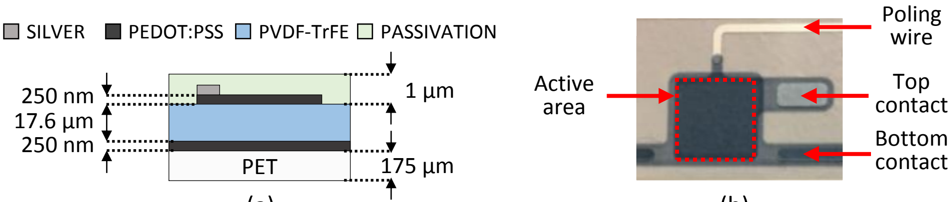
6.2.1 Printed proximity sensors

Previous works reported in literature have already demonstrated human proximity detection achieved by means of printed flexible sensors [131][132][137]. Widely used proximity sensors exploit the capacitive coupling between sensor and the target object [134][135]. The sensor typically contains single or multiple electrodes which are isolated and interact with the object placed in proximity of the sensor, forming a dynamic capacitor. Thanks to the simplicity of the structure, capacitive proximity sensors can be fabricated on plastic substrates exploiting simple printing processes, with reasonable yield and low-cost even over large-areas. Nevertheless, these sensors exhibit several limitations, which reduce their versatility and usability in the target applications. Indeed, the sensor surface is typically in the cm^2 range, limiting the achievable spatial resolution in matrix arrangements. The sensitivity of these proximity sensors is also typically low, leading to relatively short ranges of detection (~cm). At last, one of the major challenges for the use of capacitive sensors is associated to their sensitivity to variations of the shape, size and material of the target object, which could lead to erroneous detections.

Another category of sensors largely investigated in literature for human proximity sensing is based on Infra-Red (IR) pyroelectric devices. Several works have demonstrated that pyroelectric detectors can be fabricated by using poly-vinylidene fluoride (PVDF) polymer [138],[139],[140], alone or in combination with trifluoroethylene (TrFE), leading to ferroelectric PVDF-TrFE copolymers [131],[132],[136],[141]. Thanks to their higher pyroelectric coefficient compared to other polymers, fast response and processability from solutions, these polymers are well-suited for low-cost large-area array implementations. Moreover, these sensors are only sensitive to time-dependent temperature variations, which are further converted into electrical currents thanks to the pyroelectric response. However, this limitation does not reduce the usability of these sensors in the target applications, since the proximity detection is typically associated to moving heat sources. For these reasons, in this work the sensing frontplane is based on printed pyroelectric detectors, manufactured at Johanneum Research, Graz, Austria.

These sensors are screen-printed on 175 µm thick flexible PET substrates featuring an A3 format size (420 x 297 mm^2). The sensor layer stack and a photograph of a typical manufactured device are provided in Figure 62 (a) and (b), respectively. The bottom contact of the sensor is printed at first, using PEDOT:PSS material, with a typical thickness of 250 nm and an approximate sheet resistance of 100 Ω/□. A solution containing ferroelectric copolymer PVDF-TrFE in a ratio 70:30 mol% is used in the screen-printing process of the 17.6 µm thick sensor active layer. Successively, the top electrode of the sensor is also screen-printed using PEDOT:PSS ink, leading to a layer thickness and sheet resistance comparable to the ones of the bottom layer. In order to access the top sensor electrode while ensuring low contact resistance, an additional metal layer based on silver ink is introduced in the stack. The interconnection lines exhibit a thickness of about 1 µm and a resistance per square of 0.1Ω/□. The sensor stack is finalized by printing a 1 µm thick polymer-based protection layer which guarantees passivation of the last metal layer, and enables an insulation when laminated with the backplane electronics.

Printed PVDF:TrFE contains crystalline domains of PVDF carrying electrical dipole moments which are randomly oriented in an amorphous matrix of TrFE, os they don’t exhibit macroscopic ferroelectricity. In order to use the device as transducer, the crystalline domains must be aligned using a strong external electric field. This is achieved in the poling process, by applying an electric field close to the saturation field strength of the ferroelectric material of about 100 to 150 V/µm, which results in a reproducible permanent polarization (also “remnant polarization”) of the dipoles equivalent to a dielectric displacement D in the range of 50 mC/m² [132].



(a) (b)

Figure 62. (a) Cross-section of the pyroelectric sensor fabricated at Johanneum Research. (b) Photograph of a typical pyroelectric sensor manufactured with the discussed fabrication process.

It is worth mentioning that in order to use these devices for human proximity detection the sensor needs to be directly exposed to IR radiation, avoiding optical interaction with the plastic substrates. Indeed, as reported in [142] and [143] both PEN and PET substrates exhibit large spectral absorbance in the Long Wavelength Infra-Red (LWIR) range (8 µm - 15 µm), which is where significant parts of the human radiation spectrum lies [144]. As a direct consequence, the sensitivity of the sensors in this wavelength span would be severely reduced, making their use in the target applications unpractical. This limitation poses an important constraint to the system-on-foil lamination process.

In order to design backplane electronics suitable for the readout of the sensor frontplane, an equivalent model of the pyroelectric sensor is required. According to [145] it is possible to derive an equivalent thermal (Figure 63 (a)) and electrical model (Figure 63(b)) of the pyroelectric sensor, which describes the relationship between the power of the incident radiation on the detector and the charge generated. The incident power on the detector can be described by (28), under the assumption of a sinusoidal modulated light beam at angular frequency ω:

$$P(j\omega) = A_S P_0 e^{j\omega t} \tag{28}$$

where P_0 is the maximum value of irradiance and A_S is the active area of the sensor. From the inspection of the thermal circuit presented in Figure 63(a), the heat capacitance H and the thermal conductance G_T can be used to compute the temperature difference across the PVDF layer (29):

$$\eta P(j\omega) = H\frac{\partial T_{PVDF}}{\partial t} + G_T T_{PVDF} \tag{29}$$

where η is the emissivity of the pyroelectric element. The expression of $\mathrm{T_{PVDF}}$ can be extracted from Eq. (29), after combining it with Eq. (28), further leading to (30):

$$\mathrm{T_{PVDF}(j\omega)} = \frac{\eta \mathrm{P}}{\mathrm{G_T + j\omega H}} \qquad (30)$$

Equation (30) shows that the temperature difference increases with the absorbed incident radiation power, and decreases at high angular frequencies, due to the thermal time constant introduced by H and G_T. The charge Q_S developed across the detector is proportional to $\mathrm{T_{PVDF}}$ as expressed by (31):

$$\mathrm{Q_S(j\omega)} = \mathrm{p_{pyro} A_S T_{PVDF}} \qquad (31)$$

where p_{pyro} is the pyroelectric coefficient of the detector. The expression of the current signal I_S generated by the sensor (Figure 63(b)) can be calculated by combining Eq. (28) and (30) with (31), and differentiating with respect to time:

$$\mathrm{I_S(j\omega)} = \mathrm{j\omega} \frac{\mathrm{p_{pyro} A_S} \eta \mathrm{P}}{\mathrm{G_T + j\omega H}} \qquad (32)$$

Interestingly, Eq. (32) reveals that the pyroelectric sensor can be electrically modelled as a current source which produces a non-zero output signal only if subjected to time-varying excitation signals. The remaining components of the sensor electrical model (Figure 63(b)) are respectively the sensor capacitance C_E and its leakage conductance G_E.

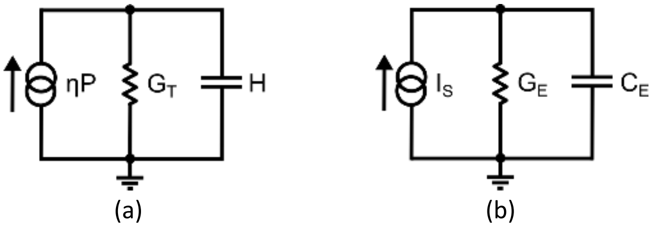


Figure 63. (a) Thermal and (b) equivalent electrical model of a pyroelectric sensor.

It is important to highlight here that the performance of the detector depends on both its thermal and electrical characteristics, which are determined by the chosen materials, geometries and feature sizes. The main parameters of the pyroelectric sensor employed in this work are listed in Table 10.

Table 10. Main parameters of the employed pyroelectric sensor.

Parameter	Symbol	Value	Unit
PVDF-TrFE layer thickness	t_0	17.6	µm
Capacitance per unit area	C_0	0.45	nF/cm^2
Leakage resistance per unit area	R_0	~300	$G\Omega*cm^2$
Pyroelectric coefficient	p_{pyro}	42	$\mu C/(Km^2)$

6.3 Design of the system-on-foil

The design of the proposed proximity sensing surface is here organized in two parts: at first the system architecture is derived and insight for the design of the system sub modules is provided. In the second part, the circuit implementation is discussed.

6.3.1 System-level design

The core of the proposed system architecture is the active-matrix of pyroelectric sensors. The first step for the design of the system-on-foil, is the definition of the number of matrix elements and their physical dimensions. The proposed active-matrix employs 5 (rows) x 10 (columns) elements arranged with a pitch of 1 cm on both directions in a 5 x 10 cm^2 area. The chosen spatial resolution of the matrix is comparable to prior e-skins reported in literature for the target HRI applications [146][147][148], while the number of elements has been restricted in the first place to 50 due to limited area available in the mask set dedicated to the backplane electronics.

Sensor multiplexing architecture: in order to fully exploit the advantages of the distributed OTFT electronics in the readout of the matrix, its elements need to be multiplexed. Indeed, this strategy allows to significantly reduce the number of interconnections with the Si-readout electronics, and thus the overall system costs, further enabling potential up-scaling of the sensing surface. Only two conventional approaches, Time-Division Multiplexing (TDM) and Frequency-Division Multiplexing (FDM), have been considered here, due to the limited architecture complexity (in terms of transistor count) that the OTFT technologies can implement with reasonable yield. The main properties of TDM and FDM multiplexing are listed for comparison in Table 11. In order to enable TDM, the backplane electronics need to be equipped with an analogue multiplexer (AMUX) and a line addressing circuit (discussed in Chapter 4), which drives the matrix element selection performed by the AMUX. The circuit implementation of the AMUX is generally very compact requiring only pass-gate transistors in each matrix pixel, which makes this architecture very attractive for solutions which require low circuit complexity (in terms of device count). In addition, the availability of OTFT technologies with large I_{ON}/I_{OFF} ratio intrinsically ensures good isolation between pixels preventing severe cross-talk issues. However, the simplicity of the circuit implementation introduces for the TDM a tradeoff between number of sensors and noise level, and thus lower achievable SNR. Indeed, if the readout frame rate is fixed by the application requirements, the bandwidth of the AMUX increases linearly with the number of multiplexed channels M, and so does the noise power, if the matrix pixels are not equipped with individual filters (Table 11). It is also clear that in this architecture all the pass-gate transistors operate at the same switching speed, which could become extremely demanding for the OTFTs if a large amount of elements needs to be aggregated at relatively high frame rates. Moreover, if the AMUX directly connects sensors to readout electronics in a charge couple mode [127] the recorded signals could experience an amplitude reduction of a factor M, associated to the duty cycled characteristic of the TDM. In other words, if the current provided by the sensor is integrated by the CSA only during the AMUX addressing time rather than in continuous mode, the integration time is duty cycled and thus the amplitude of the output voltage reduced by a factor M. Both, amplitude reduction and noise folding issues can be mitigated by introducing Analog Frontend Electronics (AFEs) in each pixel, which provides local signal amplification and decouples the sensor from the readout stage placed after the AMUX. This leads however to additional trades-off between the embedded AFE functionalities and the number of devices employed in the AFE of each pixel.

The FDM technique can be used to aggregate multiple channels in the frequency domain rather than in the time domain. In this perspective, the base bandwidth of each sensor signal can be up-converted and accommodated in different non-overlapping carrier frequencies. To do so, active or passive mixers can be used, leading to different design constraints in terms of power consumption, speed and circuit complexity. A guard band is typically placed between adjacent channels in order to maintain spectral separation and mitigate cross-talk issues. Unlike TDM, with the FDM the bandwidth of each up-converted channel remains the same as the bandwidth of the base band signal, and therefore no-aliasing of wideband noise can occur during the multiplexing operation. However, if the spectrum of the base band signals is not limited before multiplexing, the superposition of M multiple channels increase the noise floor by a factor M, and thus reduces the achievable SNR (Table 11). In order to exploit FDM techniques, more complex readout architectures are typically required with respect to the TDM case. Conventional readout architectures require for each channel a bandpass filtering at first, followed by a down-conversion before the analog to digital conversion can take place. A significant disadvantage of the FDM approach is the additional circuitry required to generate the different carrier frequencies, especially if implementations with OTFTs technologies are considered. Due to the limited speed and yield performance of the organic transistors, the implementation of these functional blocks remains extremely challenging. Alternatively, these blocks could be incorporated in the Si-readout electronics, requiring M additional interconnections with the system-on-foil (Table 11).

Table 11. Comparison between time and frequency division multiplexing techniques.

Parameter	TDM	FDM	
Multiplexed elements	M	M	
Output interconnections	1	1	
Multiplexer complexity	Low	Medium	
Si-readout electronic complexity	Low	High	
Driving signals required for multiplexing*	M	M	
Driving signal generation	On foil	On foil	On Si
Driver circuit complexity	High	High	High
Driver synchronization signals*	2 (CK, D)	1 (CK)	M
Pixel crosstalk	Low	Medium	
Noise level dependency on # of multiplexed elements	$\sqrt{\mathrm{M}}$	$\sqrt{\mathrm{M}}$	

*From Si to flexible electronics

For the reasons explained above, in this work the multiplexing of the matrix elements is performed in a TDM fashion. The multiplexing of 5 elements at a time takes place in the matrix backplane by using pass-gate transistors, which are further grouped per row (Figure

64(a)) and driven by a 5-stage line driver. The latter can be designed employing one of the architectures presented in Chapter 4, and is therefore not further discussed in this chapter. In this scenario, the matrix rows are sequentially scanned while the 10 columns are simultaneously recorded. A simplified timing diagram of the matrix readout which includes the waveforms of the main synchronization signals is provided in Figure 64(b).

Pyroelectric sensors employed in proximity detection applications are typically acquired at sampling rate in ~Hz range [132][146]. Similarly, in this work, the bandwidth BW of interest for proximity sensing has been assumed between 1 Hz and 10 Hz. A matrix readout frame rate F_{RATE} as high as 100 frame/s has been targeted in order to prove the potential for future up-scaling of the system-on-foil.

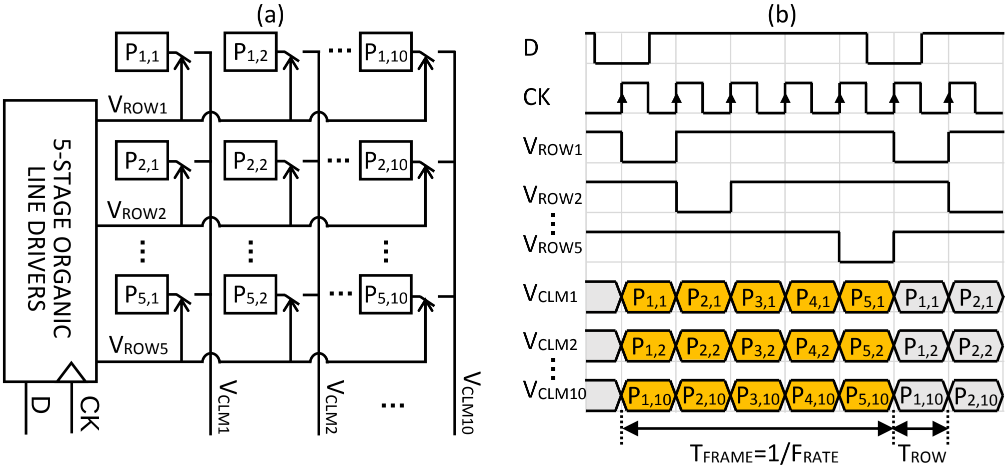
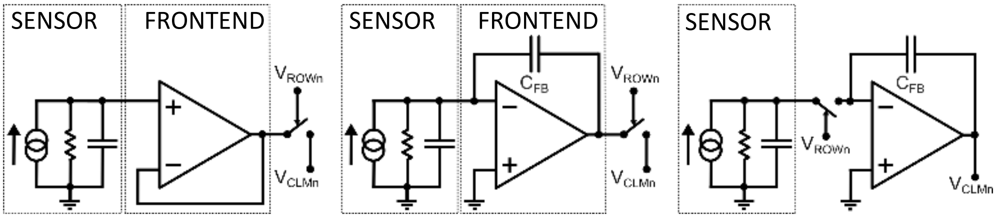


Figure 64. (a) Time division multiplexing architecture employed in the proposed proximity sensing surface. (b) Simplified time diagram of the matrix readout.

Matrix pixel design: after choosing the multiplexing strategy, the sensor active area and the frontend electronics can be designed. Pyroelectric sensors are typically readout in voltage or current mode. The voltage mode makes use of a voltage follower with a very high input resistance, in order to readout the pyroelectric sensor without introducing significant loading effects (Figure 65(a)). The main advantage of this readout technique is the simple implementation required. However, the capability of amplifying the sensor signal in the pixel could be attractive to maintain a high level of signal integrity, especially in large area applications where the system is easily exposed to coupling with interferers. For this reason, a voltage amplifier would be preferred over a voltage follower in the frontend electronics. However, this choice would lead to two additional design limitations. First, closed-loop configurations should be used to set the gain of the amplifier with passive feedback networks in order to counteract the effects of the OTFT parameter variability on the frontend performance and to remove the necessity of periodically calibrating the backplane electronics. Second, in order to implement a closed-loop voltage amplifier in each pixel, differential architectures (op-amp like) rather than single-input ones (inverter-based) should be used, requiring significantly higher circuit complexity (in term of device number) and thus reducing the attractiveness of the voltage readout mode.

Alternatively, pyroelectric sensors can be readout in current mode, by means of a Charge Sensitive Amplifier (CSA) (Figure 65(b)). Thanks to the virtual ground provided by the CSA, the charge generated by the sensor can be collected on the feedback capacitance C_{FB}, which if smaller than the sensor capacitance, enables the amplification of the sensor voltage signal. It should be mentioned that this approach is valid only as long as the time constant introduced by the feedback network C_{FB} R_{FB} remains smaller or comparable to the electrical time constant of the sensor, introduced by C_E and G_E. In these conditions, the output voltage produced by the CSA is proportional to the charge generated by sensor, and thus to the incident irradiance, enabling the proximity detection based on the amplitude of the recorded signals. In this work, a readout based on the current mode has been chosen. Indeed, this approach allows to perform sensor signal amplification within the matrix pixel, employing passive feedback networks to regulate the closed-loop gain. However, the main drawback of the use of CSAs in the pixel frontend electronics is related to the still large number of devices required for their implementation which leads to potentially high failure rates.



(a) (b) (c)

Figure 65. (a) Pyroelectric sensor voltage mode readout. (b) Pyroelectric sensor current mode readout. (c) Pyroelectric sensor readout in current mode after analog multiplexing.

In this perspective, a significant system complexity reduction could be achieved by using a CSA placed after the AMUX, which performs the readout of one sensor at a time (Figure 65(c)). This readout strategy has been investigated in [127]. The noise analysis reveals that this readout architecture could be effectively employed for the readout of pyroelectric sensor arrays, prior aggregated by the AMUX in a TDM fashion. This study further highlights that the noise level of the frontend electronics is however dominated by the noise source (considered here as wideband noise) associated to the AMUX switch, placed between the sensor and the CSA. This limits the achievable SNR, which further worsen if the low frequency noise source associated to the OTFTs would be considered. Furthermore, the effects of the charge injection and clock-feedthrough introduced by the AMUX switching action can be so large that the unwanted injection of charge becomes comparable with the charge provided by the sensor. It is thus clear that the charge injected by the AMUX needs to be accounted at the design stage to avoid the saturation of the amplifier. In this way, the contribution introduced by these unwanted charge injections, can be systematically removed during the post processing by means of calibration. Nevertheless, operational instability such as bias stress and time drift of the OTFT electrical parameters could lead to significant readout errors making the applicability of the calibration technique unpractical.

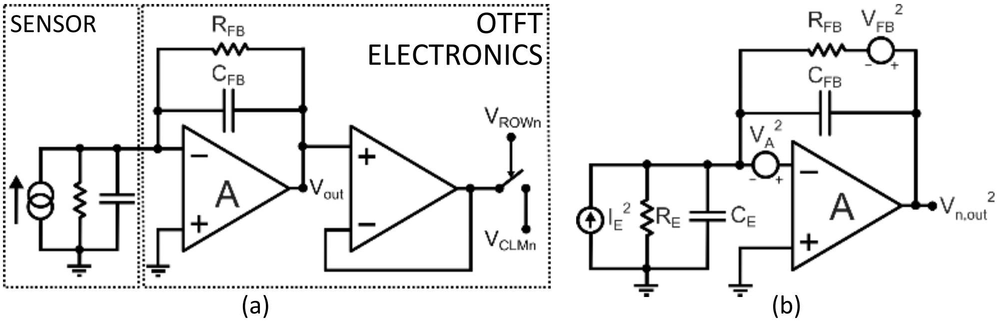


Figure 66. (a) Block-level schematic of the proposed matrix pixel. (b) Equivalent noise model used for the analysis of the frontend noise performance.

Considering all the trade-offs discussed till here in this Section, in this work the chosen system architecture embeds CSAs in the Analog Frontend Electronics (AFE) of each pixel, and exploits the TDM strategy for the element aggregation. In order to shield the CSA from unwanted charge injection occurring during the active-matrix addressing, a voltage buffer is also placed in the pixel. The block-level schematic of the matrix pixel is depicted in Figure 66(a).

As mentioned before, the use of a CSA for the readout of each sensor allows to mitigate the effect of the noise level increase associated to the TDM aggregation (Table 11). In the considered architecture, the noise folding (in base band) is mainly introduced by the voltage buffer. Thanks to the signal amplification provided by the CSA, it is possible to relax the noise specifications of the following stages of the readout chain. In this way, the impact of the voltage buffer on the noise performance of the frontend electronics can be minimized. To achieve this a signal voltage amplification of α =10 has been assumed here to be sufficient. As a consequence, the ratio between the sensor and the feedback capacitance is set equal to α. The core amplifier of the CSA must provide an open-loop gain A >> α. Indeed, by considering the CSA output voltage (33) calculated in the frequency domain from inspection of the circuit in figure (a):

$$V_{out}(j2\pi f) \cong -I_S\left(\frac{j2\pi f C_E R_E+1}{A R_E}+\left(\frac{A+1}{A}\right)\frac{j2\pi f C_{FB} R_{FB}+1}{R_{FB}}\right)^{-1} \tag{33}$$

and assuming also a frequency f, at the same time larger than $1/(2\pi R_E C_E)$ and $1/(2\pi R_{FB} C_{FB})$, Eq. (33) reduces to (34):

$$V_{out}(j2\pi f) \cong -I_S/\left(\frac{j2\pi f C_E}{A}+\left(\frac{A+1}{A}\right)j2\pi f C_{FB}\right) \tag{34}$$

By substituting $C_{FB}=C_E/\alpha$ and considering A>> α, Eq. (34) simplifies to (35):

$$V_{out}(j2\pi f) \cong -\alpha\frac{I_S}{(j2\pi f C_E)} \tag{35}$$

Which shows that the magnitude of the output voltage results α times larger than the voltage produced by the sensor without the CSA. Hence, an additional requirement for the design of the CSA is here obtained by assuming A≥50 V/V.

At this point it is possible to proceed with the sizing of the sensor active area. To do so an analytical study of the frontend noise performance is required. Following the approach provided in [127] an equivalent noise model of the sensor and frontend electronics has been derived (Figure 66(b)). More in detail, I_E^2 is the wideband noise current contribution associated to the electrical leakage conductance of the sensor, V_A^2 represents the voltage-input referred noise power spectral density of the amplifier and V_{FB}^2 is the wideband noise voltage component related to R_{FB}. For completeness, it should be mentioned that the noise contribution associated to the thermal agitation of charges in the pyroelectric material has not been considered here, since its impact is typically negligible compare to the other sources of noise [145]. From inspection of the circuit in Figure 66(b) it is possible to derive the output-referred noise power spectral density (36):

$$\mathrm{V_{n,out}^2} \cong \mathrm{V_A^2}\left(1+\frac{\mathrm{C_E}}{\mathrm{C_{FB}}}\right)^2+\left(\mathrm{V_{FB}^2}+\frac{\mathrm{A}^2}{(1+\mathrm{A})^2}\left(\frac{\mathrm{R_E R_{FB}}}{\mathrm{R_E+R_{FB}}}\right)^2\mathrm{I_E^2}\right)\left|\frac{1}{1+\mathrm{j}\pi\mathrm{f}\mathrm{R_{FB}C_{FB}}}\right|^2 \tag{36}$$

Where R_{FB} and C_{FB} represent respectively the resistance and capacitance of the CSA feedback network while C_E and R_E are the sensor capacitance and leakage resistance ($1/G_E$). By integrating Eq. (36) over the frequency f and rearranging the results, the integrated output noise $\overline{\mathrm{V_{n,out}^2}}$ reads (37):

$$\overline{\mathrm{V_{n,out}^2}} \cong \overline{\mathrm{V_A^2}}\left(1+\frac{\mathrm{C_E}}{\mathrm{C_{FB}}}\right)^2+\frac{\mathrm{K_bT}}{\mathrm{C_{FB}}}\left(1+\frac{\mathrm{A}^2}{(1+\mathrm{A})^2}\frac{\mathrm{R_E R_{FB}}}{(\mathrm{R_E+R_{FB}})^2}\right) \tag{37}$$

With K_b the Boltzmann's constant, T the temperature expressed in Kelvin and $\overline{\mathrm{V_A^2}}$ the integrated input-referred noise of the amplifier. Since the CSA preserves the charge between input and output, Eq. (37) can be used to compute the equivalent input-referred noise charge $\overline{\mathrm{Q_n^2}}$, leading to Eq. (38):

$$\overline{\mathrm{Q_n^2}} \cong \overline{\mathrm{V_A^2}}(\mathrm{C_{FB}^2}+\mathrm{C_E^2})+\mathrm{C_{FB}K_bT}\left(1+\frac{\mathrm{A}^2}{(1+\mathrm{A})^2}\frac{\mathrm{R_E R_{FB}}}{(\mathrm{R_E+R_{FB}})^2}\right) \tag{38}$$

It can be demonstrated that as long as the gain of the amplifier is A≥1 V/V the term $\frac{\mathrm{A}^2}{(1+\mathrm{A})^2}\frac{\mathrm{R_E R_{FB}}}{(\mathrm{R_E+R_{FB}})^2}$ is always smaller than 1/4, and therefore the following upper bound can be defined for the equivalent input-referred noise charge (39):

$$\overline{\mathrm{Q_n^2}} \leq \overline{\mathrm{V_A^2}}(\mathrm{C_{FB}^2}+\mathrm{C_E^2})+\frac{5}{4}\mathrm{C_{FB}K_bT} \tag{39}$$

By combining Equations (28)-(31), the achievable SNR can be calculated from Eq. (39) as follows (40):

$$SNR \geq \mathrm{Q_S^2}\Big/\overline{\mathrm{Q_n^2}} = \frac{(\mathrm{p_{pyro}A_S})^2\left|\frac{\eta\mathrm{P}}{\mathrm{G_T}+\mathrm{j}\omega\mathrm{H}}\right|^2}{\overline{\mathrm{V_A^2}}(\mathrm{C_{FB}^2}+\mathrm{C_E^2})+\frac{5}{4}\mathrm{C_{FB}K_bT}} \tag{40}$$

The thermal conductance G_T can be considered at first approximation, proportional to the bottom electrode area [149], which is also roughly equal to the sensor area A_S, leading to $G_T=G_0A_S$, where G_0 is a suitable scaling factor. Eq. (40) can be further manipulated by introducing the ratio α between the feedback and sensor capacitances, and rewriting C_E according to the sensor capacitance per unit area (Table 10). Finally, by assuming that the cut-off frequency introduced by the thermal constant is lying at a sufficiently higher frequency than the signal bandwidth of interest B, the expression of the SNR reduces to (41):

$$\mathrm{SNR} \geq \frac{\mathrm{p_{pyro}}^2 \eta^2 \mathrm{P_0}^2}{\left(\frac{\alpha+1}{\alpha}\right)^2 \overline{\mathrm{V_A^2}} \mathrm{C_0^2} + \frac{5\ \mathrm{C_0}}{4\alpha \mathrm{A_S}} \mathrm{K_b T}} \tag{41}$$

Eq. (41) reveals that if the noise of the amplifier is the dominant noise component, the active area of the sensor can be downscaled without lowering (at first approximation) the achievable SNR. This is typically the case in CSA implementations based on OTFTs, since these devices suffer from large low-frequency noise. The minimization of the sensor active area is preferable since it reduces the device thermal time constant, and potentially enables a higher integration density. However, the minimum sensor area which can be used in the matrix pixel is further limited by the feedback capacitance C_{FB}, which by design is α smaller than the sensor capacitance. Indeed, as soon as the C_{FB} approaches the value of the parasitic capacitance at the input of the amplifier, the functionality of the CSA is affected. Thus the feedback capacitance should be chosen to be larger than the parasitic capacitance at the input of the amplifier

Considering this trade-off in the design of the CSA feedback network, a C_{FB}=6 pF is selected, which for the given ratio α leads to a sensor capacitance of 60 pF and thus to an active area of 0.37 x 0.37 cm^2. Following the system specifications for the signal bandwidth B, the closed-loop cut-off frequency of the CSA (introduced by the feedback network) needs to be designed < 1 Hz. Thus assuming a target cut-off frequency of 0.1 Hz this requires a R_{FB} > 300 GΩ.

For clarity, a summary of the main system specifications is provided in Table 12.

Table 12. Main system specifications for the proposed proximity sensing surface.

Parameter	Symbol	Value	Unit
Matrix elements		5 x 10	
Matrix pitch		1	cm
Pyroelectric sensor active area	A_S	0.37 x 0.37	cm^2
Bandwidth of the sensor signal	B	1 – 10	Hz
Row addressing time (TDM)	T_{ROW}	2	ms
Matrix frame readout time	T_{FRAME}	10	ms
Matrix frame rate	F_{RATE}	100	frame/s

Funnel array design: the proposed system-on-foil could be complemented with an array of micro-optic lenses in order to enhance the directivity and increase the sensitivity of each pyroelectric sensor. Indeed, suitable lenses could be used to enhance sensitivity by focusing the IR radiation on the sensitive part of the pixel, and avoiding illumination of the pixel area dedicated to the backplane electronics.

Considering the arrangement of lens arrays in this system, it is clear that the presence of a spacer is necessary to hold the optics at several mm distance from the system-on-foil, and focus the incident radiation on the sensors. Such a large distance would require the fabrication of stretchable lens array in order to maintain the alignment between the lenses and the sensors in bended conditions. Furthermore, considerable losses associated to the absorption properties of the material employed for the lenses in the IR spectrum could significantly limit the effectiveness of this solution. In order to tackle these issues, this chapter proposes a solution based on light guiding funnels rather than a micro-optic lens arrays.

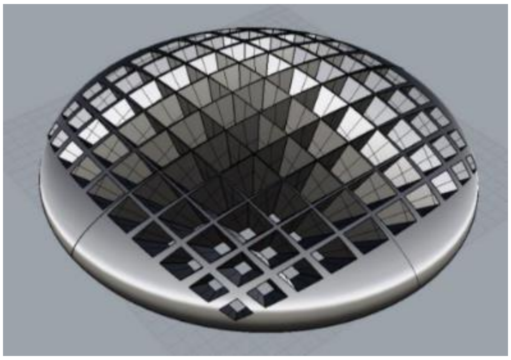


Figure 67. 3D model of the proposed funnel array structure.

The design of the funnel array has been performed at Joanneum Research. Simulations have been used to compare the performance between the different structures and further optimize the design of the selected strategy. For the design of the funnel array it is assumed that the reflection of the incident radiation is close to 100%. This can be obtained by applying a metal coating finishing on the structure after fabrication. The 3D model of the proposed funnel array is depicted in Figure 67.

Raytracing simulations have been performed assuming a 1 x 1 cm^2 Lambertian radiant source (at wavelength λ=10 µm) placed at 30 cm from the array. Simulation results show that the intensity of the maximum irradiance in the pixels is x5 higher compared to the intensity achieved in the same pixels without the funnel. Moreover, the designed funnel array could enable the detection of objects placed even at an angle ϕ=80° from normal incidence (Figure 68). The proposed array exhibits a simulated Half Power Beam Width (HPBW) of 30°, a feature which can be further exploited to enhance the directional sensitivity of the proximity sensing surface. Indeed, the simulated HPBW of a generic proximity sensor of the matrix not equipped with the funnel array, reads 85°.

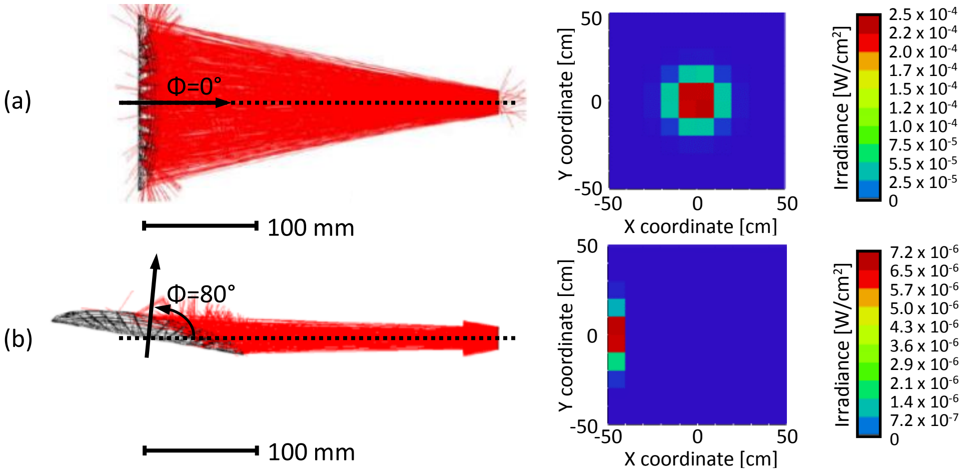


Figure 68. Results of raytracing simulations: (a) normal incidence and (b) incidence at φ=80°.

6.3.2 Circuit implementation

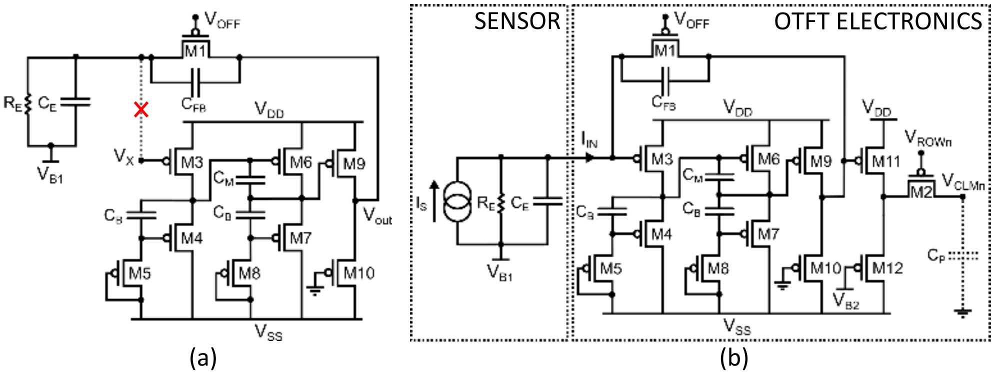
In the proposed system-on-foil, the matrix backplane electronics comprises an AMUX implemented with pass-gate transistors, and a CSA per pixel. Since all the matrix pixels are identical, this section will only focus on the circuit implementation of the generic nth pixel.

The core of the pixel OTFT electronics is the voltage amplifier required in the CSA (Figure 66(a)). For its implementation, a single-ended inverter-based amplifier has been preferred to a differential one, in order to achieve the lowest possible transistor count. Indeed, in this type of large-area sensing surface, maintaining a low circuit complexity is crucial, to enable the fabrication of matrices with a reduced number of faulty pixels. As analyzed in the previous section, one of the main specifications for the design of the voltage amplifier is the voltage gain $A \geq 50$ V/V. However, in order to achieve the target performance of the CSA, the gain specification needs to hold over the entire bandwidth of interest BW.

The design of high-gain voltage amplifiers with unipolar technologies is typically challenging due to the lack of the complementary devices. Since active load transistors are not available, conventional diode-connection or zero-V_{GS} configurations are typically used. The analysis of the unipolar inverters provided in Chapter 4 highlights that the design of reliable high-gain inverters is typically unpractical with both configurations, due to the gain limitations in the diode-connected inverter and the low-speed performance and high sensitivity to parameter variability in the zero-V_{GS} inverter. A potential circuit technique which overcomes these limitations is proposed in [81]. The circuit makes use of a voltage feedback to boost the output impedance of the main gain stage (inverter), which further allows to theoretically reach the intrinsic gain of the OTFT technology. Even though this solution was successfully demonstrated inside a CSA in [81], its use in the proposed large-area sensing surface suffer from two major drawbacks. First, the effectiveness of the impedance boosting technique reduces as the OTFTs exhibit pronounced contact effects [81].

Second, since the biasing of this circuit is in voltage domain, it is very sensitive to OTFT variations, making this approach unsuitable for large-area solutions.

The solution proposed in this work for the implementation of the voltage amplifier is depicted in Figure 69(a). The amplifier exploits a cascade of two bootstrapped inverters M3-M7, each one equipped with C_B=30 pF capacitor, which together allow to achieve a gain as high as 170 V/V or 44.6 dB, for a Gain-Bandwidth product of 580 Hz. However, as discussed in Chapter 4, the gain performance of this inverter topology degrades at relatively low operating frequency, behaving at DC conditions as a diode-connected inverter. In order to guarantee a high gain even at an operating frequency in the ~Hz range, the diode-connected transistors M5,M8 have been designed with W=100 μm and L= 800 μm. In this way, the doublets associated to the networks C_B, M5 and C_B, M8 fall approximately at 0.08 Hz. A unity-gain diode-connected inverter (M8-M9) is additionally placed after the gain stages to achieve a low-output impedance and provide the correct output signal polarity. The stability of the amplifier in closed-loop configuration (operating as CSA) has been achieved by means of a Miller compensation technique applied to the second gain stage, introducing the capacitor C_M=5 pF (Figure 69(a)). The simulated open-loop frequency response of the amplifier is presented in Figure 70(a).



(a) (b)

Figure 69. (a) Voltage amplifier implementation and $\beta_{FB}=V_x/V_{out}$ network for the closed-loop CSA configuration. (b) Transistor-level implementation of the proposed matrix pixel electronics.

In order to use this amplifier as a CSA, a passive feedback network R_{FB},C_{FB} needs to be added as shown in Figure 66(a). This network contains a first-order low-pass filter with a cut-off frequency that has been designed to be at ~0.1Hz. Given the feedback capacitance C_{FB}=6 pF (previously designed), the cut-off frequency specification requires a resistor R_{FB} ~ 300 GΩ. This extremely large resistor value has been implemented using the transistor M1 (W=100 μm, L=200 μm) operating in OFF region (Figure 69(a)). Obviously, this pseudo-resistor is very sensitive to parameter variability, and therefore the external bias voltage V_{OFF} can be accessed from outside the matrix to globally adjust the cut-off frequency of the feedback network if needed.

According to (Figure 69(a)), the CSA feedback network together with the equivalent sensor impedance forms a signal partitioning $\beta_{FB}=V_x/V_{out}$. From the Bode stability criterion, the Phase Margin (PM) needs to be evaluated at the frequency f_C at which the open loop amplification chain ($A\beta_{FB}$) reaches the unity gain. This relationship expressed in dB unit, leads to Eq. (42)

$$20\log[A(f_C)] + 20\log\ [\beta_{FB}(f_C)] = 0 \tag{42}$$

By rearranging Eq. (42) and introducing the inverse transfer function $1/\beta_{FB}$, the gain crossover frequency f_C can be determined as (43):

$$20\log[A(f_C)] - 20\log\ [1/\beta_{FB}(f_C)] = 0 \tag{43}$$

This result is used in Figure 70(a) to graphically identify the gain crossover frequency and the Phase Margin (PM) of the open-loop amplification chain. According to the circuit simulations these are respectively equal to f_C=43.6 Hz and PM=89.4° (Figure 70(b)). This result ensures a sufficient margin for the stability of the circuit in closed-loop configuration. The frequency response in magnitude and phase of the corresponding closed-loop CSA is plotted in Figure 70 (c) and (d), respectively. The output of the CSA is connected to an additional diode-connected inverter (M11-M12) which prevents charge injection by the transistor M2 (Figure 69(b)) during the pixel addressing operation in the capacitance C_{FB}. This stage serves also to drive the parasitic matrix column capacitance (estimated to be C_{PAR}=10 pF) with sufficient current capability, in order to ensure a proper settling of the output voltage within T_{ROW} (Table 12). In these conditions, simulation results show a settling time of 780 µs is required to achieve an error <1% over the steady state value. The schematic of the complete pixel OTFT electronics is depicted in Figure 69(b).

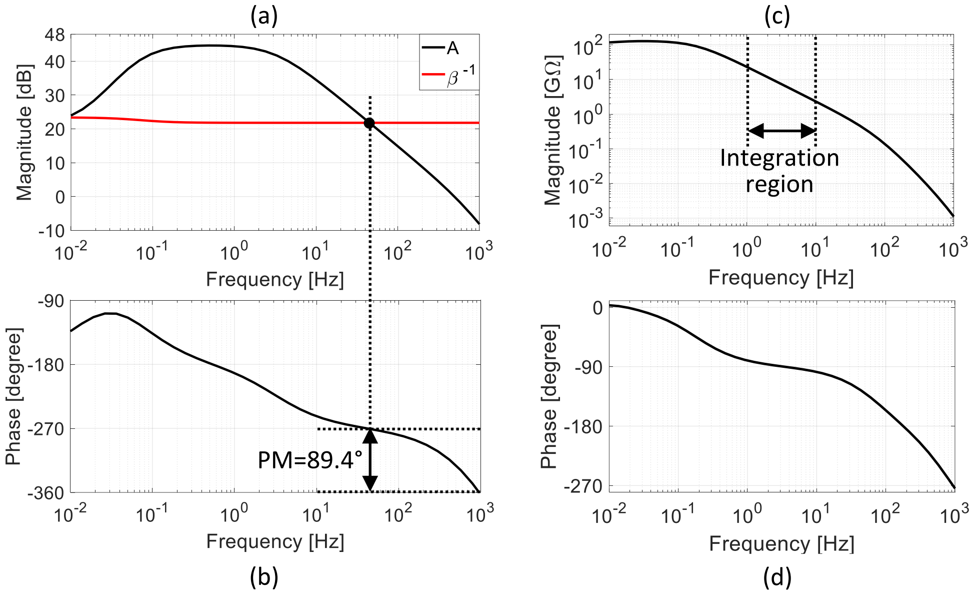


Figure 70. (a) Simulated open-loop frequency response in magnitude (a) and phase (b) of the amplifier A (black) and 1/β_{FB} feedback network. Simulated frequency response in magnitude (c) and phase (d) of the proposed CSA.

The noise performance of the pixel OTFT electronics is determined at first approximation by the noise level of the CSA. More specifically, the noise floor is dominated by the 1/f noise contributions of the devices placed in the first gain stage (M3-M4, Figure 69(a)).

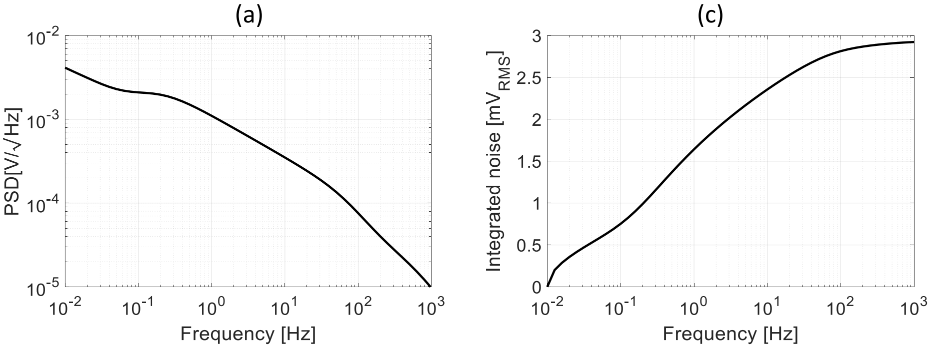


Figure 71. (a) PSD of the pixel OTFT electronics. (b) Integrated output-refereed voltage noise versus bandwidth.

According to the simulated output Noise Power Spectral Density provided in Figure 71(a), the integrated output-referred noise of the pixel electronics is 2.9 mV_{RMS} in the bandwidth 0.01 Hz – 1 kHz (Figure 71(b)). This simulated noise performance of the pixel OTFT electronics is achieved with an estimated current consumption of 2.9 µA and a supply voltage of ±18 V.

The proposed pixel OTFT electronics requires 16 devices, of which are 12 OTFTs and 4 are capacitors. In this scenario, the probability P_{PIXEL} of fabricating a fully-functional matrix pixel (backplane only) can be roughly calculated assuming that the AMUX and the AFE should be both fully working at the same time, leading to (44):

$$\mathrm{P_{PIXEL}} = \mathrm{P_{AFE}P_{AMUX}} \tag{44}$$

where P_{AFE} and P_{AMUX} are respectively the probabilities that the manufactured AFE and AMUX are fully working. Since each implemented AFE circuit requires 15 devices (from Figure 69(a), excluding the transistor M2), and the AMUX comprises 1x5 transistors, Eq. (44) can be rewritten as (45):

$$\mathrm{P_{PIXEL}} = \mathrm{P_{DEV}}^{20} \tag{45}$$

where P_{DEV} is the probability of fabricating a working device. By substituting P_{DEV} with the yield analysis results discussed in Chapter 2, the estimation provided by Eq. (45) leads to 96% expected fully-functional pixels. It should be remarked that for the reasons mentioned in Chapter 4, this estimation can only provide a rough indication of the circuit yield.

6.4 System integration

As discussed in Section 6.2, the proposed printed proximity sensing surface comprises a frontplane (sensors) and a backplane (OTFTs) which are laminated together. The lamination needs to guarantee the electrical interconnections between the sensors and the electronics, even in bending conditions, and ensures the mechanical stability of the system. Since both sensors and electronics are fabricated with additive processes on flexible plastic substrates, the electrical interconnection of the two foils can be obtained by means of physical contact between pads that are not covered with passivation layer. In order to facilitate this operation, adhesive conductive microdots have been sandwiched between frontplane and backplane (Figure 72(a)). An insulating black adhesive sheet has been pre-patterned by means of laser cut and also glued between sensors and electronics (Figure 72(a)), to improve the mechanical stability of the system, while allowing the electrical interconnection of the foils.

Unfortunately, the system-on-foil obtained with this layer stack would not be suitable yet for proximity sensing applications. Indeed, in this arrangement the pyroelectric sensors are not directly exposed to the infrared radiation, due to the presence of the backplane PEN substrate, which further causes a large radiation absorption in the wavelength range of interest (8 µm-15 µm) making the use of these sensors unpractical. To tackle this issue, the areas of the backplane substrate which overlay with the pyroelectric sensors have been laser-cut before lamination (Figure 72(b)). This method further reduces the available pixel area for the OTFT electronics, which now is about 60% of the pixel area (Figure 72(b)), posing additional limitations on the potential downscaling of the matrix pitch. The lamination procedure is finalized by gluing a second insulating black adhesive which is here used as light shielding layer for the electronics. This is important as discussed in the Section 6.3, for the correct operation of the voltage amplifier A the cut-off frequency of the high-pass filter networks M5-C_B and M8-C_B (Figure 69(a)) needs to be set at ~ 0.1Hz, requiring extremely large transistor off-resistances. Similar considerations apply to the transistor M1 placed in the feedback network of the CSA (Figure 69(b)). Direct exposure of the OTFTs to ambient light, would significantly increase the transistor off-current, which leads to degradation of the frontend performance. Therefore, the shielding layers helps to mitigate this problem.

For better clarity, a summary of the lamination process is provided in Figure 72(a).

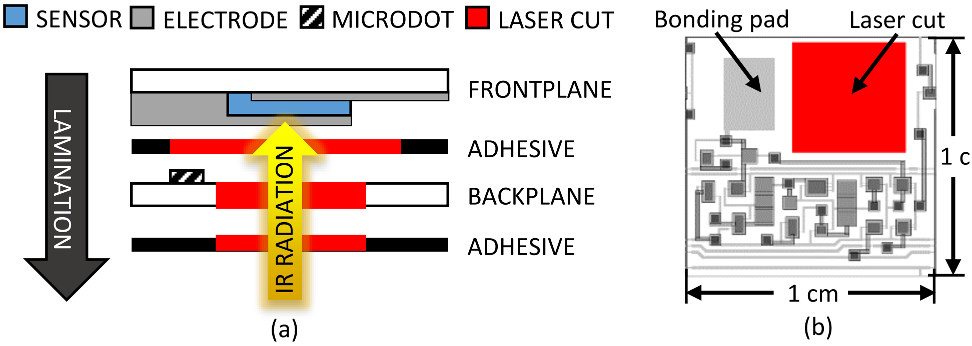
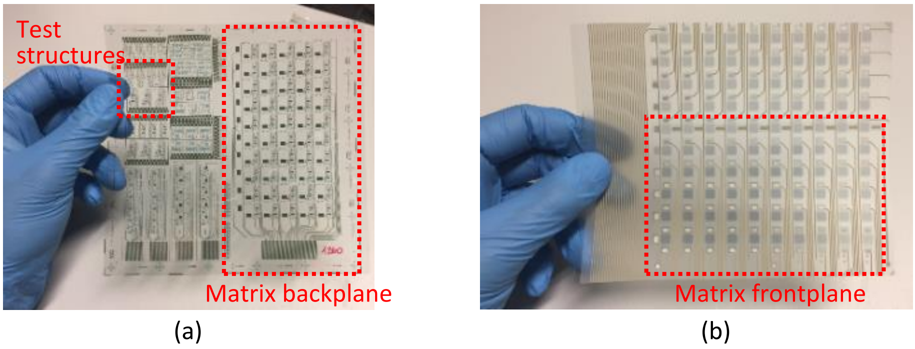


Figure 72. (a) Lamination process: cross-section view of the proposed system-on-foil. (b) Layout (top view) of the OTFT electronics of a generic matrix pixel.

6.5 Measurement results

The designed matrix backplane has been fabricated with the manufacturing process discussed in Chapter 2 on a 126 x 126 mm^2 module area, obtained from the partitioning of the GEN1 plastic substrate (Figure 73(a)). The sensing frontplane (Figure 73(b)) has been manufactured and the pyroelectric sensors individually poled according to the process described in Section 6.2.



(a) (b)

Figure 73. (a) Fabricated module comprising the backplane matrix electronics and AFE test structures. (b) Manufactured array of pyroelectric sensors forming the matrix sensing frontplane.

The designed funnel array (Figure 67) has been manufactured by means of a 3D printing process at Joanneum Research (Figure 74(a)). In order to achieve 100% Long-Wavelength Infrared (LWIR) reflectivity, the structure has been metallized with sputtered aluminum (Figure 74(b)). It should be mentioned that the funnel array developed with this process is not mechanically flexible. This limitation could potentially be overcome by employing flexible materials such as Polydimethylsiloxane (PDMS) in combination with a 3D printed mould. However, the current funnel design exhibits deeply undercut structures which are difficult to extract from the mould and it is not currently possible to metallize structure of PDMS by common metal deposition methods. Therefore, the design of the structure should be optimized taking into account the fabrication limitations, in order to achieve the target mechanical and optical properties while ensuring reasonable production yield.

(a) (b)

Figure 74. (a) 3D printed funnel array before (a) and after (b) metallization coating.

AFE characterization: the electrical performance of the AFE circuit employed in the matrix pixel has been assessed first. These measurements have been performed on test structures (Figure 73(a)) which contain the very same matrix AFE circuits, identical at both schematic and layout level. Following the strategy described in [81], the CSA circuit has been characterized in frequency domain, exploiting the schematic depicted in Figure 75(a). In this configuration, the circuit under test operates as band-pass voltage amplifier, providing an in-band gain equal to (46):

$$H_V = -\frac{A}{\left(1+A\frac{C_{FB}}{C_E}\right)} \tag{46}$$

By substituting the ratio $C_E/C_{FB} = \alpha$ and manipulating, Eq. (46) reduces to (47):

$$H_V = -\frac{A\alpha}{(\alpha+A)} \tag{47}$$

Hence, if A>>α, the closed-loop voltage gain of the amplifier depicted in Figure 75(a) becomes approximately $H_V \cong -\alpha$, namely equal in absolute value to the capacitance ratio. The knowledge of this ratio can be further used to assess the gain performance of the CSA. As discussed in [81], the frequency response of the CSA (here defined as H_{CSA}), can be derived from H_V by using the following relationship (48):

$$H_{CSA} \cong H_V \cdot \frac{R_S}{j\omega C_S R_S+1} \tag{48}$$

Where R_S is the leakage resistance of the discrete capacitor C_S.

The frequency response of the circuit in Figure 75(a) has been measured by means of the HP35670 Dynamic Signal Analyzer. The source signal is provided by the analyzer and fed to the circuit by using a discrete series capacitance C_S=68pF ± 5% (AVX 0805 MLCC) as shown in Figure 75(a). This discrete capacitor is used here in place of the pyroelectric sensor to simplify the electrical characterization process. It should be mentioned here that the value of C_S differs from the value of C_E calculated at design stage. Indeed, preliminary measurements performed on the frontplane highlighted that the pyroelectric sensors exhibit a typical capacitance of nearly ~70 pF, deviating about 10 pF from the initial design value.

A discrete Si voltage buffer amplifier is introduced between the circuit under test and the Dynamic Signal Analyzer, in order to mitigate the loading effects of the measurement setup. The frequency response of the circuit is measured by using a 20 mVpeak input sine sweep. The outcome is presented in Figure 75(b). The measurement results show a typical bandpass response, with an in-band gain of 12V/V, a first cut-off frequency at f_{C1}=0.11 Hz and a second cut-off frequency at f_{C2}=62Hz. By substituting in Eq. (48) the measured H_V, C_S=68 pF and R_S=100 GΩ, the estimated response of the CSA is 28.1 GΩ at a frequency of 1 Hz. This result is slightly higher than the simulated performance (Figure 70(b)) mainly due to the larger ratio α.

The linearity performance of the circuit has been evaluated using a 25 mV_{RMS} input single-tone test at 5 Hz. This input signal amplitude is chosen in order to reach the maximum expected output voltage swing of the circuit.

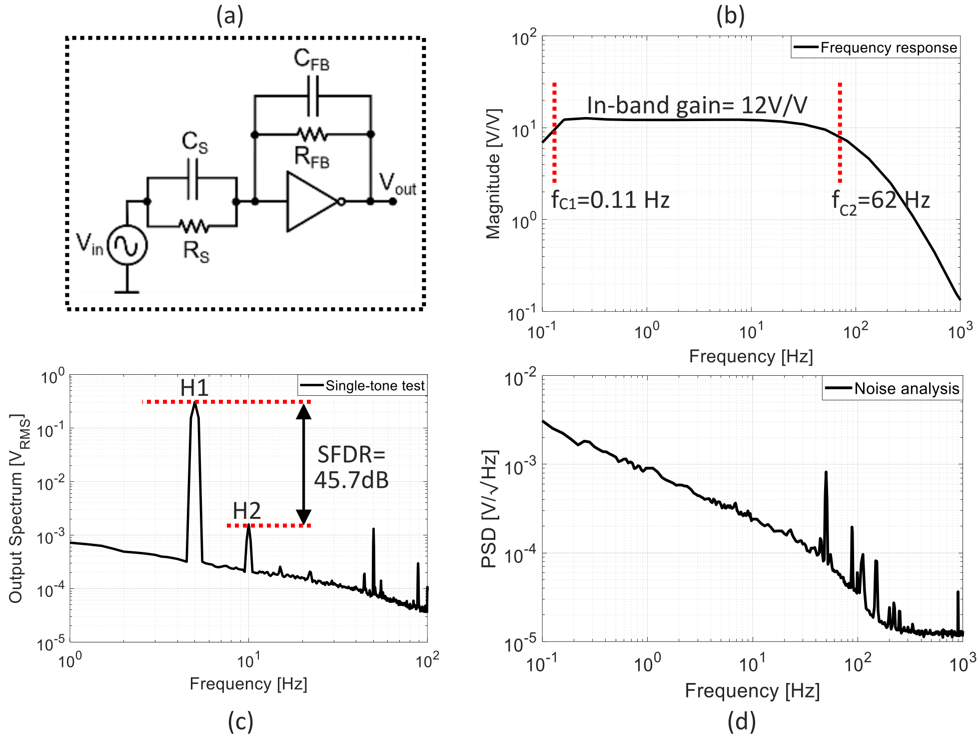


Figure 75. (a) Simplified schematic of the test circuit used for the electrical performance evaluation of the AFE. (b) Frequency response, obtained with 20 mV_{peak} input sine sweep. (c) Output spectrum recorded with a 25 mV_{RMS} input single-tone at 5 Hz (Hanning window, averaging factor=100). (d) Noise PSD of the output-referred voltage noise. The integrated output-referred noise voltage in the bandwidth 0.1 Hz-1 kHz is equal to 2.3 mV_{RMS}.

Indeed, 3 pC charge is delivered by the pyroelectric sensor as a human approaches it at $\sim$ 10 cm distance, according to the estimation method discussed in [81]. This determines an AFE output voltage swing comparable with the one achieved with the linearity measurement test. The recorded output spectrum is presented in Figure 75(c). The circuit linearity performance is limited by the contribution of the second harmonic (H2), a result that is not surprising in a single-ended implementation leading to a Spurious Free Dynamic Range (SFDR) of 45.7 dB.

The noise performance of the AFE has also been evaluated. It is worth noticing that, the noise transfer functions of the circuit under test in this configuration and of the CSA in its final application are equivalent. Therefore, the noise measurement results can be directly extended to the CSA case, without further transformations. The recorded output-referred noise Power Spectral Density (Figure 75(d)) reveals that the noise floor is dominated by the 1/f noise contribution. By integrating the PSD over the bandwidth of analysis (0.1 Hz - 1 kHz), the output-referred noise of the circuit reads 2.3mV_{RMS}. Despite the different capacitance ratio, the measured integrated output-referred noise is relatively close to the value predicted in simulation (Figure 70(d)). The integrated noise can also be referred to the input of the CSA in terms of Equivalent Noise Charge (ENC), multiplying it by the feedback capacitance value C_{FB}=6 pF. The corresponding ENC is 12.5 fC or 86.2 ke$_{RMS}$, which further leads to a maximum SNR of 47dB (assuming a maximum charge delivered by the sensor equal to 3 pC).

This AFE performance is achieved with a current consumption of 1.5 µA and supply voltages of ±18 V. For completeness, the bias voltages V_{B1}, V_{B2} and V_{OFF} are respectively +10 V, -9V and +10V.

Matrix backplane evaluation: similarly to the evaluation of the single AFE electronics, the functionality check of the pyro-matrix backplane is performed by using characterizations in the frequency domain.

The frequency response of the AFE contained in each pixel in the backplane is measured by using the test circuit depicted in Figure 75(a). In this case, the AMUX is statically addressed in order to select the desired pixel and the excitation applied to AFE electronics by means of a test probe (Figure 76(a)). A Printed Circuit Board (PCB) is used to connect the matrix backplane with the readout electronics based on off-the-shelf components. Each matrix column voltage V_{CLM} is connected one at a time to a Si voltage buffer amplifier and further fed to the HP35670 Dynamic Signal Analyzer. A simplified diagram of the measurement setup is provided in Figure 76(a). An image of the measurement setup employed for the backplane functionality check, is depicted in Figure 76(b).

In order to identify correctly working pixels (at backplane level), the following criteria are adopted:

- Cut-off frequency $f_{C1} < 1$ Hz
- Cut-off frequency $f_{C2} > 10$ Hz
- In-band gain ≥ 10 V/V

The results of the functionality checks performed over four matrix backplanes manufactured in different batches are presented in Figure 77. The measurement database contains electrical characterizations recorded over a population of 200 pixels. The outcome of the functionality check activity reveals 36 non-correctly working pixels over 200 measured, which corresponds to a defectivity rate of 18%. The pixel failures can be further divided in hard faults (13 pixels, defined as "fail" in Figure 77) and soft faults (26 pixels, defined as "near" in Figure 77). All the AFE circuits which belong to the soft failure category do not satisfy only the specification on f_{C1}, which falls instead in the Hz range. The cause of this defect can be ascribed to excessive off-current in the transistor M5, M8, M1 which are responsible for the low-frequency behavior of the circuit. Interestingly, the pixels affected by soft faults are also spatially correlated as clearly shown in Figure 77 and mainly distributed along the printing direction. Conversely the hard faults seem to be randomly distributed along the foils with the exception of the Foil#3, in which the failure affects the entire column. In the latter case, the faulty column could be also caused by a random defect occurred e.g. in the AMUX circuit, which however affects the functionality of all aggregated pixels. If in the defectivity rate are included only the hard defects, the yield of the matrix backplanes approaches 93.5%. Even though the extracted yield cannot be considered statistically relevant due to the reduced number of samples analyzed, its value is relatively close to the estimation provided in Section 6.3.

The frequency responses of the fully-working pixels are all plotted in Figure 78(a). The distribution of the extracted in-band gain provided in Figure 78 (b) reveals a mean value of 12.7 V/V with a standard deviation of 2 V/V. Differently, the distribution of the cut-off frequency f_{C2} (Figure 78 (c)) is characterized by a relatively larger spread. In this case the mean value is 96 Hz, while the standard deviation reaches 48.5 Hz. These results are of course compatible with the gain desensitization caused by the closed-loop CSA topology.

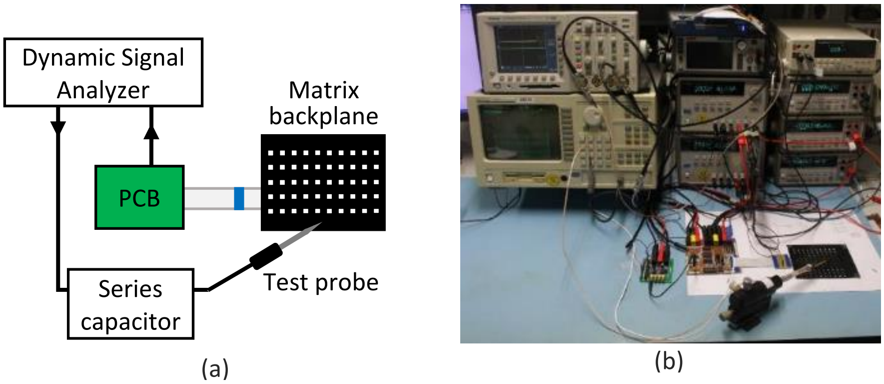
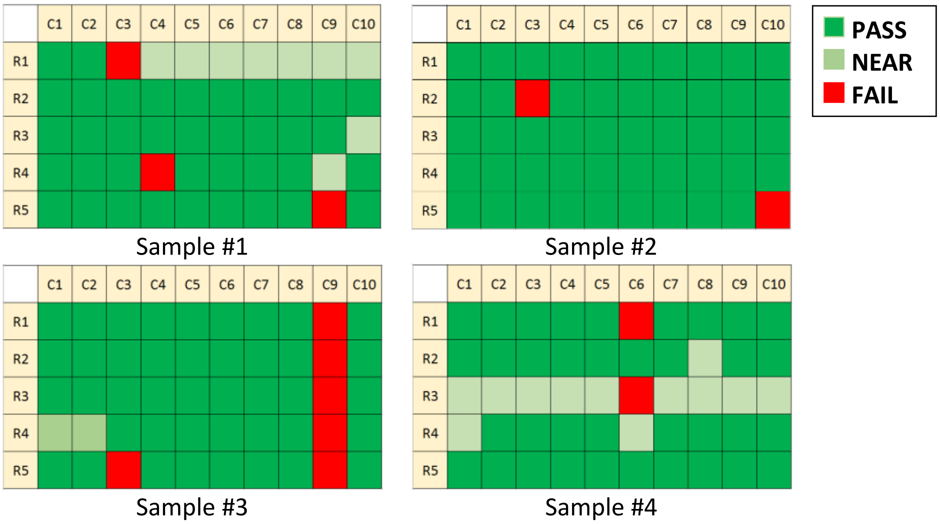


Figure 76. (a) Simplified diagram of the measurement setup used for the matrix backplane functionality check. (b) Image of the measurement setup employed during the backplane functionality check activity.



🟩 PASS
▨ NEAR
🟥 FAIL

Sample #1

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟥	▨	▨	▨	▨	▨	▨	▨
R2	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
R3	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	▨
R4	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩	▨	🟩
R5	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩

Sample #2

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
R2	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟩	🟩	🟩
R3	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
R4	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩
R5	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥

Sample #3

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩
R2	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩
R3	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩
R4	▨	▨	🟩	🟩	🟩	🟩	🟩	🟩	🟥	🟩
R5	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟩	🟥	🟩

Sample #4

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩
R2	🟩	🟩	🟩	🟩	🟩	🟩	🟩	▨	🟩	🟩
R3	▨	▨	▨	▨	▨	🟥	▨	▨	▨	▨
R4	▨	🟩	🟩	🟩	🟩	▨	🟩	🟩	🟩	🟩
R5	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩	🟩

Figure 77. Functionality maps of four different matrix backplanes. The position of each pixel within the matrix is identified by the row number (R yth*) and column number (C x*th*).*

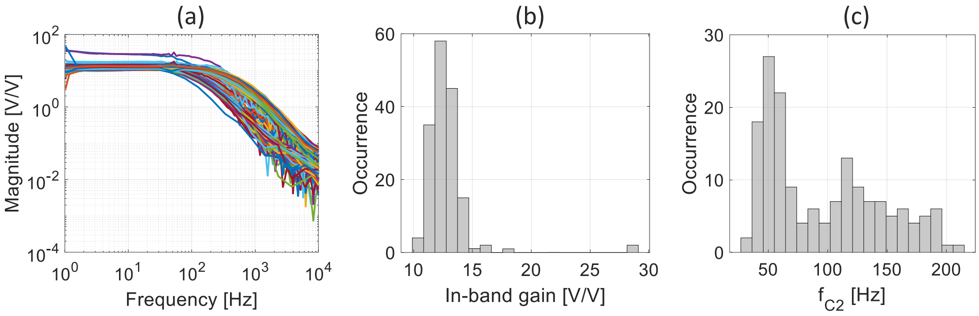
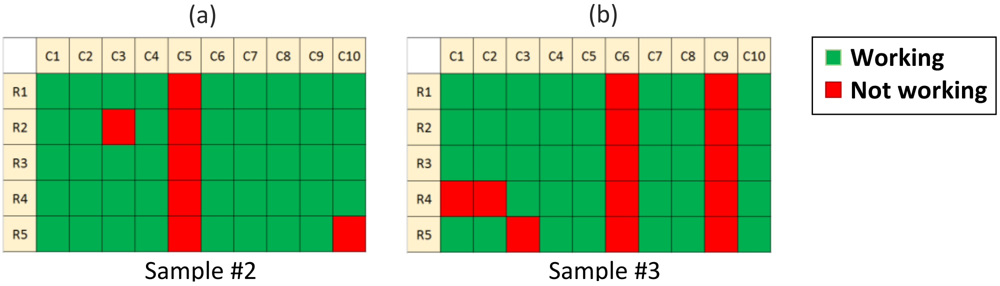


Figure 78. (a) Frequency responses recorded from the 163 working pixels. (b) Histogram of the in-band gain distribution, mean value μ=12.7 V/V and standard deviation σ=2 V/V. (c) Histogram of the amplifier second cut-off frequency f_{C2} *distribution. The mean value of the distribution is μ=96 Hz, while the standard deviation is σ=48.5 Hz.*

Evaluation of the system-on-foil: the two backplanes with highest pixel yield, namely Sample #2 and #3 have been laminated with the sensing frontplanes (both featuring 100% sensor yield) in order to create two proximity sensing matrix prototypes. After the lamination was completed, each prototypes suffered of an additional non-working column, respectively C5 and C6 (Figure 80). The picture of the prototype based on sample #2 is shown in Figure 80. Thanks to its higher pixel yield, this prototype has been further used for the characterization process.



(a)

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟩
R2	🟩	🟩	🟥	🟩	🟥	🟩	🟩	🟩	🟩	🟩
R3	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟩
R4	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟩
R5	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟩	🟩	🟥

Sample #2

(b)

	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R1	🟩	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟥	🟩
R2	🟩	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟥	🟩
R3	🟩	🟩	🟩	🟩	🟩	🟥	🟩	🟩	🟥	🟩
R4	🟥	🟥	🟩	🟩	🟩	🟥	🟩	🟩	🟥	🟩
R5	🟩	🟩	🟥	🟩	🟩	🟥	🟩	🟩	🟥	🟩

Sample #3

🟩 **Working**
🟥 **Not working**

Figure 79. Functionality map of prototypes after lamination process. 5 new pixel failures occurred in both samples #2 (R1-5, C5) and samples #3 (R1-5, C6) compared to the initial backplane yield.

The proposed system-on-foil has been qualitatively evaluated by means of proximity tests performed in two different scenarios:

- Multiple human hand approaches from different directions and at different distances from the pyro matrix.
- Tracking of a localized and movable heat source.

In both experiments the prototype is placed at a distance of about 40 cm from the source. The prototype is readout at the target frame rate of 100 frames/s, and the column output voltages are recorded by means of the National Instrument Data Acquisition board NI 6259 DAQ.

Figure 80. Proximity sensing surface obtained after lamination process. (a) Front view. (b) Back view

A real time visualization software has been also developed, in order to display the proximity detection during the experiments.

A human hand approach is presented in Figure 81. The operator hand is approaching at a distance of about 40 cm from the prototype. The experiment is repeated in similar fashion, after introducing the funnel array on the sensing surface (Figure 82). The use of the funnel array is expected to enhance the directivity of the proximity detection (as discussed in Section 6.3). However, this is not clearly demonstrated in this experiment (Figure 82), since the heat source is not localized.

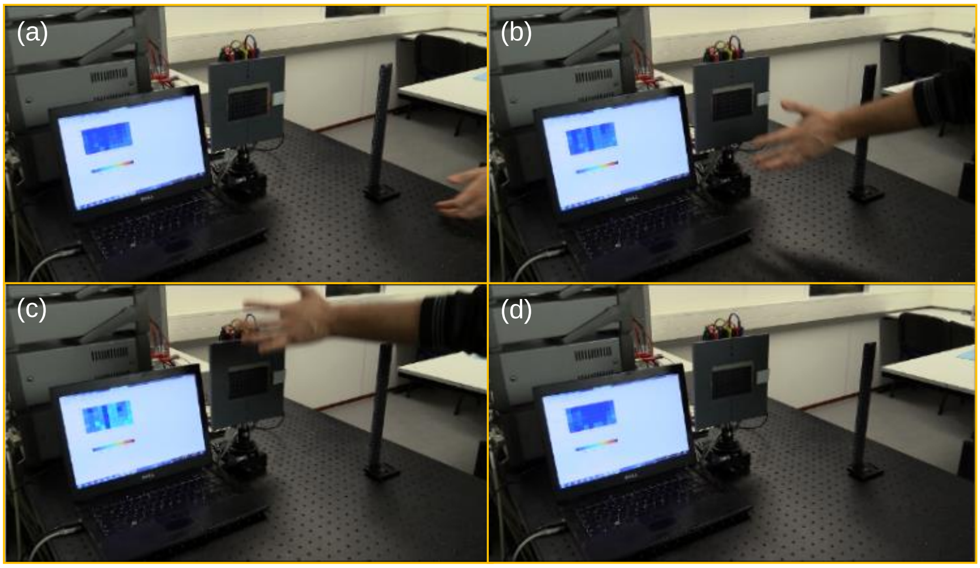


Figure 81. Operator hand approach at about 40 cm from the prototype. The time evolution of the video frames are indicated by the letters a-b-c-d.

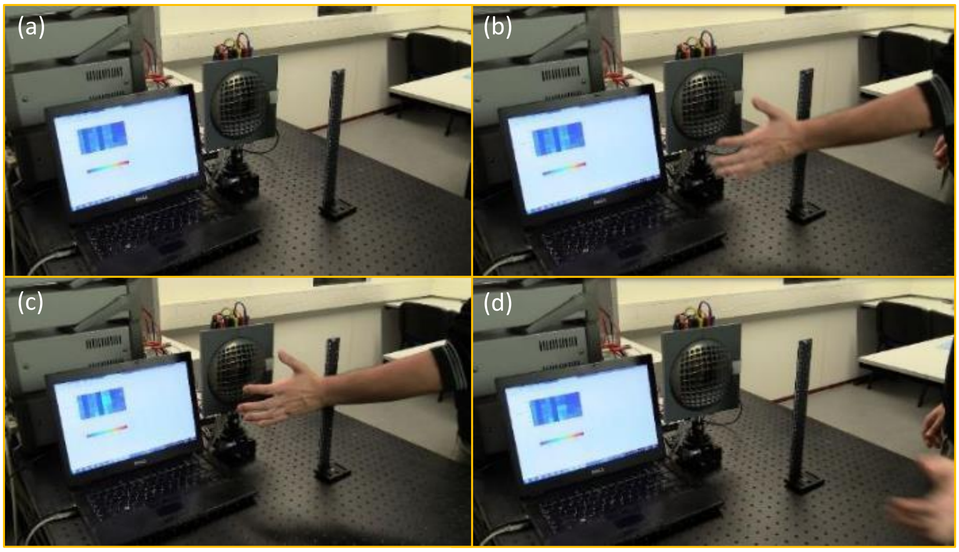


Figure 82. Operator hand approach at about 40 cm from the prototype. The prototype is equipped with the funnel array. The time evolution of the video frames are indicated by the letters a-b-c-d.

In the second experiment, a soldering iron is used as localized heat source. The heat source is placed at about 40 cm from the matrix and moves in the direction parallel to the sample. The recorded proximity detections are shown in Figure 83 and Figure 84, where the prototype is equipped without and with the funnel array. This experiment qualitatively proves the effectiveness of the funnel array, in the enhancement of the detection directivity.

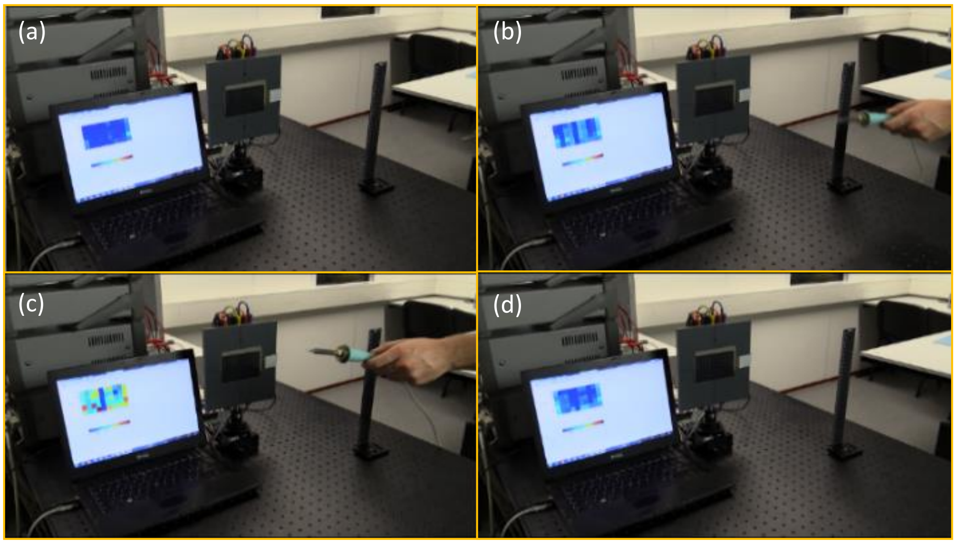


Figure 83. Approach of a soldering iron used as heat source, placed at a distance of 40 cm from the prototype. The time evolution of the video frames are indicated by the letters a-b-c-d.

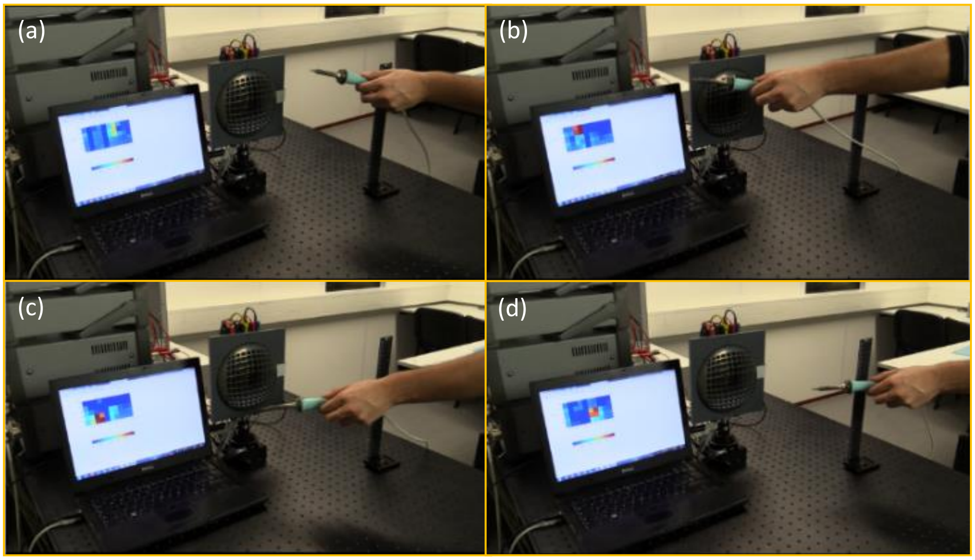


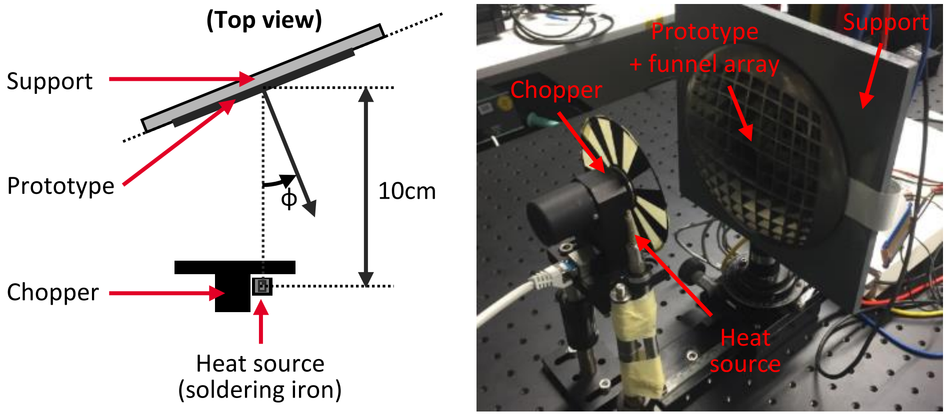
Figure 84. Approach of a soldering iron used as heat source, placed at a distance of 40 cm from the prototype equipped with the funnel array. The time evolution of the video frames are indicated by the letters a-b-c-d.

In order to quantify the improvement in directivity detection provided by the use of the funnel array, a more rigorous characterization has been performed.

The measurement setup developed for this evaluation exploits a controlled heat source placed at 10 cm distance from the prototype accommodated on a plastic support, and a rotary stage to control the relative angular position ϕ of the sensing surface with respect to the source (Figure 85(a)).

A soldering iron (Weller MT301 tip) together with its temperature control unit (Weller MT1500) is used to realize the temperature controlled heat source. During the experiments the soldering iron tip is maintained at a constant at a constant temperature of 454°C. A 10 blade optical chopper has been used to modulate the IR radiation of the heat source. A THORLABS MC1000 controller is used to drive the optical chopper. The 10 blade optical chopper together with its controller allow to achieve a minimum modulation frequency of 20 Hz. However, in order to mitigate the frequency folding introduced by the aliasing of the harmonic components beyond the Nyquist frequency, the modulation frequency has been further reduced. By obscuring 8 chopper blades the modulation frequency has been lowered down to 4 Hz.

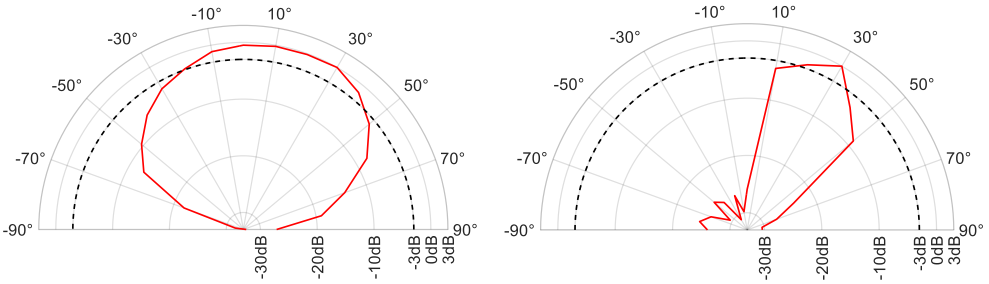
A simplified diagram and a photograph of the measurement setup are provided in Figure 85(a) and Figure 85(b), respectively. The normalized detection diagram is measured by sweeping the angular position ϕ of the prototype, from -90° to 90° with steps of 10°. In Figure 86(a) and (b) are compared the directivity detection patterns recorded on pixel R3, C6 using the prototype respectively equipped with and without the funnel array. It is worth noticing that in both recorded detection patters the angle which corresponds to the maximum detection value does not coincide with the normal incidence (0°). This could be caused by a residual angular offset of the rotary stage, misaligned positioning of the heat source and sensing surface and potential asymmetries of the sensing frontplane and funnel array. The measurement results clearly show also that the funnel array gives an improvement of the



(a) (b)

Figure 85. (a) Simplified diagram and (b) photograph of the measurement setup used in the directivity detection evaluation.

directivity. The outcome presented in Figure 86(a) reveals that the proximity sensing capability of the single element exhibits a HPBW of approximately 70°. The insertion of the funnel array allows to increase the directivity of the sensing elements leading to a HPBW of about 20° (Figure 86(a)), significantly improving the directivity of the detection. On the contrary, the sensitivity improvement highlighted by the simulation results has not been experimentally observed. This is mainly caused by the poor coverage of the metallization coating applied on the funnel array, which introduces large losses in the guided radiation.



(Prototype without funnel array)

(a)

(Prototype with funnel array)

(b)

Figure 86. Normalized directivity detection pattern recorded by using the prototype equipped without (a) and with (b) the funnel array.

The main indicators of the system performance are listed in Table 13.

Table 13. Main performance indicators of the proposed proximity sensing surface.

	Parameter	Symbol	Value	Unit
Frontend				
	Gain @ 1 Hz		28.1	GΩ
	Bandwidth	f_{C1}-f_{C2}	0.11-62	Hz
	SFDR (at expected maximum output swing)		45.7	dBc
	ENC		86.2	ke$_{RMS}$
	SNR* (bandwidth 0.1 Hz – 1 kHz)		47	dB
	Supply voltage	V_{DD}, V_{SS}	±18	V
	Power consumption		54	µW
	Area		0.5	cm^2
	Required number of devices		16	
	Yield		82	%
Matrix				
	Number of elements		5x10	
	Readout frame rate	F_{RATE}	100	Hz
	Proximity detection distance		~40	cm
	HPBW detection angle**		70 │ 20	°
	Supply voltage	V_{DD}, V_{SS}	±18	V
	Power consumption***		3.2	mW
	Area***		50	cm^2

*For a maximum amplitude sensor signal of 3pC

**Respectively without and with funnel array

***Excluding the 5-stage line drivers

6.6 Conclusions

To the best of the author's knowledge, this work demonstrates for the first time in literature a fully-printed large-area proximity sensing surface manufactured with organic materials, which embeds AFE in each pixel. The system-on-foil integrates a matrix of pyroelectric sensors screen-printed on foil (frontplane) laminated with a second flexible substrate (backplane) containing a corresponding matrix of AFE manufactured with OTFTs. The developed proximity sensing surface features 5 x 10 elements, distributed over an area of 5 x 10 cm^2 with 1 cm pitch arrangement. In order to enhance the sensitivity and directivity of the pyroelectric sensors a funnel array has been also designed and manufactured exploiting a 3D printing process.

The electronics embedded in each matrix pixel perform the readout of the sensor in current mode by using a dedicated CSA and further enables the pixel aggregation in a TDM fashion. The proposed AFE circuit requires in each pixel a circuit complexity of 16 devices (12 OTFTs and 4 capacitors). The experimental characterization of multiple matrix backplanes highlights that the performance of the proposed circuit architecture is robust against hard failures and device parameter viability. Indeed, an average defectivity rate of 18% is extracted over a population of 200 pixels. Improvements in the device yield performance of the current OTFT technology could potentially enable a further system upscaling while ensuring reasonably low pixel defectivity. The highest number of fully-working pixels recorded among the analyzed matrix backplanes is 48 out of 50, which corresponds to 768 fully-functional devices (576 OTFTs and 192 capacitors). This result attains the largest circuit complexity (in terms of device count) ever achieved by a printed OTFT circuit to date.

The proposed system-on-foil has been successfully used for proximity detections of human hand approaches from different directions and for position tracking of a localized movable heat source. In both scenarios proximity detections at a distance of about 40 cm from the source have been investigated by exploiting the sensing surface on foil equipped with and without the funnel array.

These results demonstrate that printed electronics can be potentially used to fabricate low-cost solutions suitable for human proximity sensing applications, where large-area coverage and detection distance in the range of ~ 0.5 m are the main requirements. The availability of this type of proximity sensing surfaces is expected to play an important role to increase the level of security (collision avoidance), improve the interaction modalities and significantly reduce the costs in HRI applications.

7. Hybrid PE/Si pressure sensing surface

In this Chapter is presented for the first time in literature a system architecture suitable for pressure sensing applications, which integrates Si-IC electronics (based on Si-65 nm technology) with a System-in-Package (SiP) manufactured with printed organic materials. The use of printed organic technologies enables low-cost large-area distributed pressure sensing capability, while the Si-IC electronics perform the SiP readout, control the sensor aggregation and the signal digitalization, using the minimum number of interconnections and allowing a compact footprint. The core of the SiP is a 5x3 active matrix of printed organic pressure-sensitive sensors on foil (frontplane), laminated with a second flexible substrate containing printed frontend electronics (backplane). The pixel frontend electronics make use of a transconductor to perform high-speed sensor aggregation and voltage-to-current conversion for the direct interconnection with the Si-IC electronics. The proposed system-on-foil is designed to achieve large dynamic range in force/pressure measurements together with a fast response, in order to further extend the versatility of the solution. The availability of low-cost large-area pressure sensing devices which can be directly interfaced to conventional Si-based platforms is expected to be a key enabler for innovative applications in the markets of domestic ambient monitoring, automotive and smart buildings to give some examples.

Part of the content of this chapter has been published in [97]. The major results provided in this chapter are intended to be submitted for journal publication (currently in preparation).

7.1 Introduction

Organic materials offer an attractive solution to develop large-area systems-on-foil for distributed sensing applications. The use of the conventional printing techniques developed for the graphic industry could enable the fabrication of electronics on plastic substrates at very low cost per unit area. This advantage together with the mechanical properties of the substrate (lightweight, flexible or even stretchable) could be exploited to create inexpensive electronic solutions for applications which require sensing capabilities and large area coverage.

Potential large-area pressure sensing solutions manufactured with organic materials could be employed in automotive safety monitoring applications such as car crash tests to record the applied force profiles during impact. Plastic substrates are especially suited for pressure sensing applications, as they are rugged and can tolerate bending and large compressive forces. In this scenario, thanks to their mechanical properties, systems-on-foil could be accommodated between the main supporting barrier and the deformable aluminum honeycomb prior to each car crash test. From application perspective, the availability of thin, lightweight, large-area pressure sensing surfaces-on-foil could replace the bulky, heavy and discrete force meters currently in use.

In the current state-of-the-art, it has been shown already that active matrices based on organic transistors can detect the spatial pressure distribution in several applications, such as electronic artificial skin [128][129], and tactile sensors [130][131]. In these applications, high sensitivity and fast response have been the main objectives. However, the possibility of achieving a high dynamic range required to determine impact force and pressure measurements has not been proven yet. Moreover, the use of printed organic electronics in direct combination with CMOS IC technologies could enlarge the usability and versatility of the Printed Electronics (PE) for new classes of applications embodying what can be called “hybrid electronics”. Customized ICs could be designed to interface the SiP using efficient readout architectures, embedding signal processing functionalities and further enabling connectivity via dedicated wireline/wireless transceivers to the outside world. The direct interconnection of the two systems potentially allows to completely avoid the use of interface electronics based on discrete components, leading to lightweight solutions with extremely compact footprints. However, interfacing PE with SI-ICs is not free from challenges. Printed OTFTs typically feature large threshold voltages which prevent their use at low voltage supply. Conversely, the supply voltages of most recent silicon technologies are limited at around one volt. Thus, in order to directly interconnect the two technologies in a safe way, several constraints introduced by the large voltage mismatch need to be accounted for in the design of the system architecture. If the two subsystems are DC coupled in the voltage domain, their respective input/output voltage levels need to be aligned in order to prevent saturation (or even damages) of the input stage on the silicon chip. Alternatively, the bias voltage of the two subsystems could be decoupled by means of high-pass filters, which however requires large area and is prone to defects. The voltage swing of the organic circuits should also to be limited in order to avoid overvoltage and thus potential damages of the Si-input stage. This situation further worsens due to the large parameter variability and reliability issues of the OTFTs which makes the design of the electrical interface challenging. At last, the large OTFT stray capacitances together with the large voltage swing of the clock signals are typically responsible for high level of charge injections, which can saturate or even damage, the input stage of the silicon chip. For these reasons, it is clear that the design of the interface electronics is crucial for the successful integration of both subsystems.

As a second important point, the number of interconnects between the Si chip and the PE foil should be minimized, to keep the area and the cost of the SI chip to a minimum. This objective can be reached exploiting the printed electronics to reduce the number of interconnections needed to interface the multiplicity if sensors integrated in the sensing surface.

In this context, the work described in this chapter aims to demonstrate the feasibility of hybrid solutions (SiP + Si-IC) for pressure sensing applications, embedding printed OTFTs and Si-mainstream electronics in a single system. As proof of concept, the design of the system has been developed assuming its potential use in car crash test application scenarios. Information on the instrumentation for impact tests specified by the Society of Automotive Engineers (SAE) in J211-1 [151], has been used in this work to define the application requirements. According to [151], the recording of the impact forces on the barriers requires a Channel Frequency Class (CFC) of 60 Hz. The minimum sampling frequency required to acquire the sensor signals during impact tests is 10 x CFC, which in this case leads to f_S=600 Hz. In addition, the digitalization process requires an Effective Number of Bits (ENOB) of 10 bit, leading to a minimum SNR requirement of 62 dB. The peak forces at which the barrier is subjected are not uniquely defined since they depend on the impact conditions (front, rear or side), the mass and the structure of the vehicle, the speed of the moving mass, etc… For this reason, the maximum applicable force on each pressure sensor has been assumed in this work equal to 100 kN. This assumption is reasonable, since experimental results previously reported in literature [152][153] reveal cumulative peak forces of $\sim$100 kN, recorded in impact tests with deformable barriers.

This Chapter is further organized as follows: the hybrid PE/Si sensing system architecture is presented in Section 7.2. The system level design of the SiP and Si-IC is discussed in Section 7.3, together with their circuit level implementations. Section 7.4 describes the system integration, while Section 7.5 provides the measurement results obtained from the system evaluation. Conclusions are drawn in Section 7.6.

7.2 Hybrid PE/Si sensing system architecture

The simplified block diagram of the proposed hybrid PE/Si pressure sensing system is shown in Figure 87. The SiP comprises arrays of pressure sensors printed on foil (defined here as frontplane) laminated with OTFT electronics fabricated on plastic substrate (called here backplane) (Figure 87). Similarly to the case of the proximity sensing surface presented in Chapter 6, this approach allows to fabricate both sensors and OTFT electronics independently, without introducing additional constraints on the manufacturing processes and preserving the mechanical properties of the system-on-foil. The availability of the OTFT distributed electronics is here exploited to perform active addressing of the matrix elements and to potentially integrate AFE circuits within each pixel. A customized Si-IC is connected to the SiP to perform the matrix readout, the analog signal digitalization and the generation of the synchronization signals for the line driving circuit (Figure 87). The latter can be implemented either with OTFTs or discrete Si electronics, depending on the chosen pixel aggregation strategy and the performance required. The possibility of aggregating multiple matrix elements is extremely important in order to minimize the interconnection with the Si-IC and thus, further reduce the overall system cost.

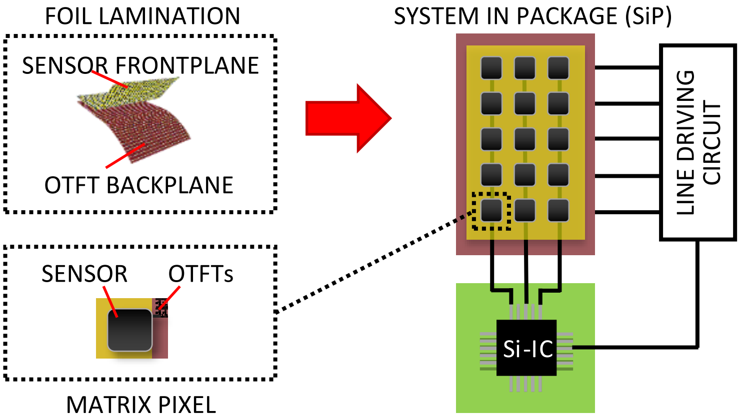


Figure 87. Block diagram of the proposed hybrid PE/Si pressure sensing system

7.2.1 Printed pressure sensors

The sensors employed in this work are based on the ferroelectric polymer PVDF-TrFE, which exhibits piezoelectric properties. The organic materials, fabrication and poling processes discussed in Chapter 6 for the proximity sensors, have been used here without modifications to develop the pressure sensors. As already reported in literature, sensors based on the ferroelectric polymer PVDF-TrFE exhibit both pyroelectric and piezoelectric response, making them suitable for proximity and pressure/impact force detection. In addition, the characteristics of printability over large-area, robustness at mechanical stress [97], low cost and good uniformity, together with the relatively large sensitivity of the polymer, make this sensor a good candidate for the target pressure sensing applications. Indeed, previous works reported in literature has already demonstrated tactile and pressure sensing recognition [131] using sensors manufactured with the discussed fabrication process.

The working principle of the sensor is briefly discussed as follows. If the material is deformed by an external applied force, positive and negative charge separation occurs within the sensitive material due to its piezoelectric characteristic. Thus, on the two opposite surfaces of the material a potential difference will be formed. In quasi static conditions, the total charge Q_E delivered by the sensor is in first order approximation proportional to the piezoelectric coefficient d_{33} and the force F_N applied along the 3-axis direction which is perpendicular to the sensor surface [154]:

$$\mathrm{Q_E = d_{33} F_N} \tag{49}$$

Consequently, the voltage V_E generated across the sensor capacitance C_E is given by (50):

$$\mathrm{V_E = \frac{d_{33} F_N}{C_0 A_S}} \tag{50}$$

Where C_0 and A_S are the capacitance per unit area and the active area of the sensor, respectively. The sensor can be modelled with the same equivalent electrical circuit proposed for the proximity sensor (Figure 63(a)). In this case the current I_S provided by the sensor is obtained by differentiating in time Eq. (49), leading to (51):

$$\mathrm{I_S = \frac{\partial(d_{33}\, F_N)}{\partial t}} \tag{51}$$

The main parameters of the piezoelectric sensor employed in this work are listed in Table 14.

Table 14. Main parameters of the employed piezoelectric sensor.

Parameter	Symbol	Value	Unit
PVDF-TrFE layer thickness	t_0	17.6	µm
Capacitance per unit area	C_0	0.45	nF/cm^2
Leakage resistance per unit area	R_0	~300	GΩ*cm^2
Piezoelectric coefficient	d_{33}	32	pC/N

7.3 Design of the hybrid PE/Si system

The proposed system architecture combines an active-matrix of pressure sensors on foil (SiP) based on printed organic materials with dedicated Si-IC readout electronics. In this section, the design of both subsystems will be discussed at system level and the circuit implementation of the SiP also provided. The transistor-level implementation of the Si-IC is already exhaustively reported in [155] and therefore not further discussed in this work.

7.3.1 System level design

System in Package (SiP): the proposed active-matrix architecture features 5 (rows) x 3 (columns) pressure sensing elements, organized with a symmetric pitch of 2.75 cm in an area of 8.25 x 13.75 cm^2. This matrix pitch value has been chosen in order to relax the mechanical constraints for the integration of the system-on-foil in conventional barriers employed in car crash tests. The number of matrix elements is instead dictated by the available area in the mask set used to develop the OTFT electronics. It is worth mentioning that the printed organic electronics required by all the prototypes and tests structures described in the Chapters 4-7 have been fabricated on the same GEN1 substrate.

In order to efficiently exploit the active-matrix addressing functionality, multiple pressure sensitive elements M needs to be aggregated by means of multiplexing techniques. For the advantages already discussed in Chapter 6, a system architecture based on a Time-Division Multiplexing (TDM) technique is preferred (Figure 88(a)). In this way, all the 5 elements belonging to each matrix column are multiplexed by an AMUX within a time frame T_{FRAME} (Figure 88(b)). A 5-stage line driver is therefore required to perform the pixel selection. The matrix readout frame rate F_{RATE}=1/ T_{FRAME} needs to be chosen larger or at least equal to the sampling frequency f_S specified for each sensor in the application requirements. However, in order to demonstrate the possibility of future upscaling of the active matrix allowing the aggregation of 8x more elements, the system has been designed to operate at a maximum frame rate of F_{RATE}=5 kframe/s. It is important to notice that in these conditions, the AMUX needs to ensure a proper settling of the output signal within T_{ROW}=40 µs[3]. In other words, the OTFTs used to implement the AMUX need to operate at a switching speed close to their unity-gain frequency (f_T~200 kHz).

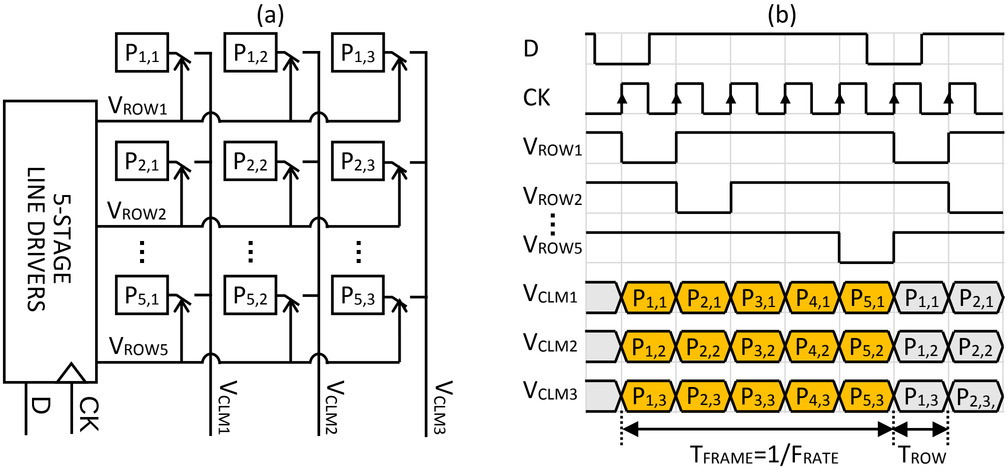


Figure 88. (a) Time division multiplexing architecture employed in the proposed pressure sensing active matrix. (b) Simplified time diagram of the matrix readout.

From these considerations, it is also clear that the implementation of the 5-stage line driving circuit in the backplane electronics is unpractical. Therefore in this work, a solution based on discrete off-the-shelf components has been adopted.

Matrix pixel design: at this point, the sensor active area and the frontend electronics can be designed. Similarly to the pyroelectric sensors, piezoelectric sensors exhibit very high impedance. Therefore, the same considerations discussed in Chapter 6 on the choice of the readout electronics apply also for this category of sensors. However, in this case an additional application requirement should be taken into account. If Eq. (49) is evaluated for the maximum applied force specified for the target applications, the peak charge delivered by the piezoelectric can be estimated to be 3.2 µC. By introducing this value in Eq. (51), and further assuming a sensor active area as large as the matrix pixel size (2.75 x 2.75 cm^2), the voltage generated at its terminals would approximately reach ~900 V! This would

---

[3] $T_{ROW}=T_{FRAME}/M$

permanently damage the OTFTs, since the absolute maximum source-gate voltage that the transistors can withstand before breakdown is typically 90 V. In this scenario, a printed capacitor could be introduced in the frontend electronics and placed in parallel to sensor, in order to reach an equivalent capacitance ≥ $10C_E$ which would decrease the output voltage within the safe limit. However, the fabrication of capacitors as large as $\sim$ 30 nF with reasonable yield and within the available pixel area is unfeasible in the current manufacturing process. It is clear that conventional high impedance voltage readouts are not applicable in this case.

Alternatively, the piezoelectric sensor could be readout in current mode. Even though Trans-Impedance Amplifiers (TIA) could be potentially integrated in the matrix pixel, the large peak currents generated by the sensors should be handled by the OTFTs, which should be therefore designed with extremely large channel widths, potentially resulting in low circuit yield. An indication of the peak current provided by the sensor can be roughly estimated by using Eq. (51) in combination with a sinusoidal approximation of the applied force ($F_N=F_0\sin(2\pi f_0 t)$), leading to (52):

$$\mathrm{I_{S\_MAX}} = \mathrm{d_{33}F_0 2\pi f_0} \qquad (52)$$

Where F_0 and f_0 are respectively the maximum amplitude and frequency of the mechanical excitation. By substituting the values of F_0 and f_0 defined by the application requirements (F_0= 100kN, f_0=CFC=60Hz), the estimated peak current is I_{S_MAX}=1.2 mA. A typical OTFT fabricated in the current technology with minimum channel length L=10 µm and operating in saturation region with an overdrive voltage of 15 V would require a channel width W=2.2 cm to sustain such current. This is clearly unpractical from the yield point of view, especially in the perspective of using such devices in large-area matrix backplanes.

The solution proposed in this work is based on the use of a resistor R in parallel to the sensor in order to provide a low-impedance path (Figure 89(a-c)). If the resistance value is correctly chosen, no passive integration of the current occurs on the sensor capacitance within the bandwidth of interest, and therefore the voltage across the sensor can be limited within a safe range. Typical resistance values are in the ~kΩ range, making the integration of the resistor R feasible with a compact footprint in the S/D metal layer of the OTFT backplane. This approach intrinsically transfers the sensor current to an output voltage across the resistor, and thus requires a frontend electronics which perform the readout in high impedance voltage mode. In these conditions, the sensed voltage is proportional to (51) and hence the applied force/pressure can be determined after digitalization by means of numerical integration. An important conclusion can be drawn here: according to (51) the amplitude of the sensor signal is independent from the sensor area, while the wideband noise components associated to the leakage and R resistances lead to and integrated noise power of $V_N^2=K_BT/C_E$. In order to maximize the achievable SNR, the area of the sensor capacitance should be maximized. However, the dominant noise components which typically limit the SNR performance are associated to the frontend electronic architecture. In this perspective, the pressure sensor active area has been arbitrary chosen equal to 1.8 x 1.8 cm^2. As demonstrated in [97], the frontend electronics can be reduced to a simple active matrix-addressing architecture (Figure 89(a)). Even though extremely simple, this solution is affected by pixel crosstalk issues which introduce large errors in the readout. The second solution proposed in [97] employs a voltage buffer using 2 OTFTs in a follower configuration, to readout the voltage across the resistor R Figure 89(b). This approach mitigates the pixel crosstalk issues at the expense of relatively large power consumption. In the perspective of the SiP/Si-IC integration, this solution exhibits a severe drawback which prevents its use in the architecture. Indeed, the large parameter variability of the OTFTs could largely affect the bias condition of the frontend electronics, making the matching of the voltage levels between the two technologies extremely challenging.

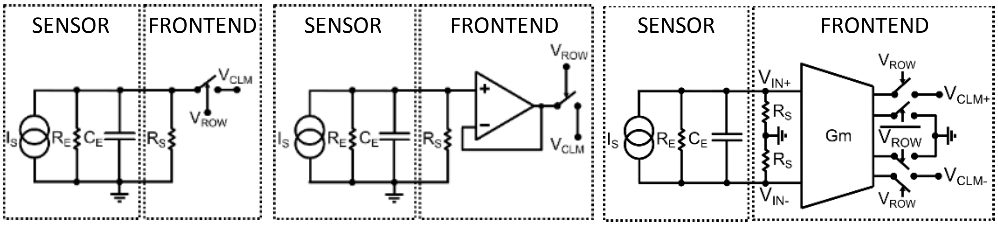
The frontend electronics proposed in this work exploit instead a transconductance amplifier (Gm stage) to perform a voltage-to-current (V/I) conversion (Figure 89(c)). This is here implemented using a fully differential architecture in order to improve the immunity to common mode interferences and thus the signal integrity of each pixel. Moreover, fully differential implementations have the potential to reduce the generation of large nonlinear even-order harmonics, and thus DC offset contributions which otherwise could introduce significant errors during numerical integration. The resistor R is also divided in two components (Figure 89(c)) in order to provide a differential signal at the input of the transconductor. A current steering approach is used to perform the pixel selection with high-speed switching performance. The current mode readout allows to remove one of the major limitations in the integration of the two sub-systems associated to the voltage level matching. Indeed, the first stage of the Si-IC subsystem can be used to provide a virtual ground node, which maintains the output of the transconductor at a safe and stable potential and enables safe operation of the Si IC too.

Table 15. Main system specifications for the proposed pressure sensing surface.

Parameter	Symbol	Value	Unit
Matrix elements	M x N	5 x 3	
Matrix pitch		2.75	cm
Pyroelectric sensor active area	A_S	1.8 x 1.8	cm^2
Bandwidth of the sensor signal	CFC	60	Hz
Sensor Signal-to-Noise Ratio (SNR)	SNR	≥62	dB
Row addressing time (TDM)	T_{ROW}	40	µs
Matrix frame readout time	T_{FRAME}	200	µs
Matrix frame rate	F_{RATE}	5	kframe/s

In order to guarantee the correct co-operation of both sub-systems, it is necessary to ensure that the sink and source currents will not saturate the Si-IC stage, even in presence of the large charge injection introduced by the switching action of the active-matrix addressing circuit. Since the matrix addressing circuit is constrained by the readout speed specifications, the size and thus the capacitances of the OTFTs in this circuit cannot be reduced, and therefore the unwanted injected charge should be accommodated by the first Si-IC stage.

For better clarity the block-diagram of the proposed matrix pixel is shown in Figure 89(c) while the main system specifications are listed in Table 15.



(a) (b) (c)

Figure 89. Block diagram of the matrix pixel and SiP/Si-IC interface electronics. (a) Voltage mode interface based on active matrix addressing circuit. (b) Voltage mode interface based on frontend electronics and matrix addressing circuit, both implemented with OTFTs. (c) Current mode interface based on fully differential Gm stage and current steering analog multiplexer, both implemented on the matrix backplane electronics.

Si-IC system level design: in all the pixels of the generic nth matrix column, the differential outputs of each Gm stage are connected together in order to perform element aggregation. Next, each matrix column is directly connected to the silicon chip for readout, data conversion and data transfer to the base station. In order to enable the readout of the matrix columns, N differential input channels needs to be placed in the Si-IC (Figure 91(a)). In order to demonstrate the system upscaling, by using multiple pressure sensing surfaces at the same time, 6 differential input channels have been included in the Si-IC. Each channel employs a fully differential Trans-Impedance Amplifier (TIA) to measure the current provided by the aggregated Gm stages. Moreover, a Common Mode Feedback (CMFB) circuit needs to be introduced at the input of each TIA (Figure 91(b)) to remove the DC current component of the transconductor while ensuring a correct common mode bias voltage V_{CM} at the input of the TIA, in order to maximize its output dynamic. Moreover, the CMFB should guarantee a relatively fast settling of the TIA input common mode each time that a new pixel is addressed, absorbing large part of the charge injected by the current steering circuit placed in the matrix pixel after the Gm stage. Despite this, a large amount of residual differential charge could still be introduced in the TIA, due to the asymmetric behavior of the two transconductor branches caused by the poor device matching properties of the OTFTs. It should be highlighted that a wideband CMFB circuit placed at the input of the TIA negatively affect the noise performance of the Si-IC readout chain. For this reason, a trade-off between power consumption and noise performance needs to be reached in the design of this stage.

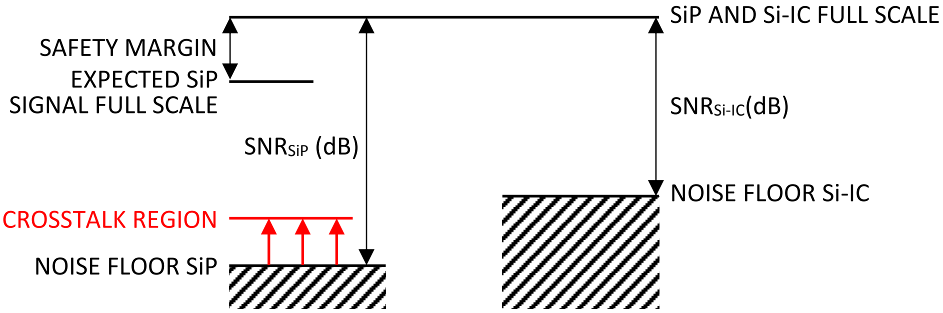
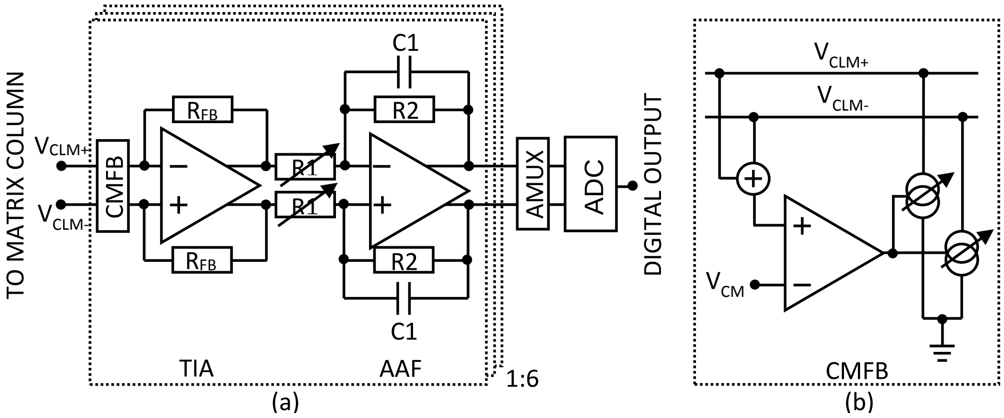


Figure 90. Relative position of the full scale and noise floor level of both SiP and Si-IC subsystems.

Significant current mismatches between the output branches of each transconductance amplifier due to the large parameter variability typical of printed OTFTs need also to be accounted for. These appear at the input of the TIA as an unwanted differential signal added to the sensor signal, which can be systematically removed only by means of calibration. For this reason, the TIA should be designed to achieve a dynamic range larger than the application requirement, in order to accommodate the current provided by the Gm stage even in presence of large mismatch. The choice of the TIA feedback resistor value is instead constrained in the first place by the amount of charge injected during the multiplexing operation. As mentioned above, during the pixel addressing a significant amount of injected charge could still reach the TIA, and thus the feedback resistor R_{FB} should be sized to prevent saturation of the amplifier. This design constraint further entails that the gain gm of the transconductor needs to be maximized, in order to increase the TIA output swing and relax the frontend noise requirements.

After the TIA, an Anti-Aliasing Filter (AAF) is introduced to prevent noise folding due to the sampling required for the data conversion. The cut-off frequency of the antialiasing filter is set at approximately 250 kHz in order to allow a proper settling of the output voltage within T_{ROW}=40 µs. The AAF provides also adjustable voltage amplification in order to ensure that the maximum signal amplitude approaches the full scale of the Analog-to-Digital Converter (ADC). In this perspective, a safety margin of about 4 dB has been assumed to prevent the saturation of the ADC, in presence of current mismatch and performance spread of the Gm stage (Figure 90). Next, an AMUX is used before the ADC to aggregate the outputs of the AAFs belonging to the different columns in a TDM fashion. Finally, the output of the AMUX is fed to the 12 bit Successive Approximation Register (SAR) ADC (with an ENOB=10.3 bit) based on the architecture proposed in [156]. For completeness, in this work the ADC full scale is determined as the maximum RMS value of the sinusoidal signal (in) that the converter can handle without reaching saturation.

The block diagram of the proposed Si-IC architecture is shown in Figure 91(a).



(a) (b)

Figure 91. (a) Simplified block diagram of the proposed silicon IC architecture. (b) Block diagram of the CMFB module.

7.3.2 SiP circuit implementation

The backplane electronics comprise in each pixel two shunt resistors R_S, a GM stage and 4 OTFTs used to implement the current steering AMUX (Figure 92). The resistance value of both shunt resistors has been chosen equal to R_S= 2kΩ. This value together with the estimated maximum sensor peak current (I_{S_MAX}=1.2 mA) leads to nearly V_{IN} =5 V (differential peak-to-peak voltage). In addition, the relatively low R_S value can be integrated in the S/D metal layer with a compact footprint. The Gm stage consists of a basic differential pair and a tail bias current. Source degeneration techniques are not exploited here to stabilize the gm of the differential pair against process variations, since the achievable transconductance value typically does not exceed a few µS. Indeed, in order to make effective use of such techniques, the gm value should be significantly reduced, and large degeneration resistors would be required. The implementation of the latter devices in the S/D or GATE metal layers is extremely cumbersome and therefore pseudo-resistors or OTFTs operating in the linear region should be employed. Hence, in this configuration the gm of the driver transistors can be maximized at the expense of larger power consumption. Moreover, the channel length of the drivers is chosen equal to 40 µm rather than the minimum feature size, since the spread of the transistor parameters is minimum at this L (Figure 16). It should be remarked that the current mismatch appears at the TIA (on the Si chip) as a differential signal which cannot be rejected by the input CMFB circuit. As a consequence, the output dynamic range of the TIA would be negatively affected.

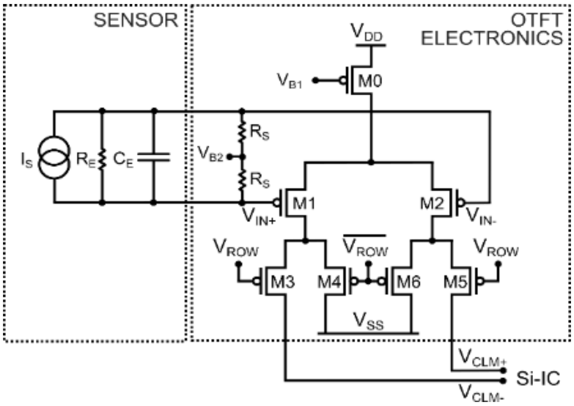


Figure 92. Schematic of the matrix pixel comprising the sensor electrical equivalent model, the shunt resistors R_S, the backplane frontend electronics (M0-M2) and the active-addressing circuit (M3-M6).

For further sizing the differential pair, additional constraints posed by the application requirements should be considered. Due to the large Low Frequency Noise (LFN) components of the OTFTs and the relatively large signal bandwidth required from the application, it is reasonable to assume that the achievable SNR is mainly limited by the 1/f noise contributions associated to the frontend electronics. In this case, by assuming the differential output current provided by the Gm stage equal to gmV_{IN} (with V_{IN} the differential input RMS voltage and gm calculated according to Eq.(19)) and by integrating the PSD of the 1/f OTFT noise component (Eq. (20)) over the frequency interval f_1,f_2 the achievable SNR is given by Eq. (53):

$$\mathrm{SNR} = \frac{\gamma^2 \mathrm{WLC_I V_{IN}}^2}{2q\alpha_H(V_{SG}+V_{TH})\ln(f2/f1)} \tag{53}$$

By extracting $(V_{SG} + V_{TH})$ from Eq. (19) and substituting in Eq. (53), the expression of the SNR reduces to (54):

$$\mathrm{SNR} = \frac{gm}{I_{SD}}\frac{\gamma \mathrm{WLC_I V_{IN}}^2}{2q\alpha_H \ln(f2/f1)} \tag{54}$$

Equation (54) reveals that biasing the differential pair in order to achieve large gm/I_{DS}, is beneficial for the SNR. However, it should also be mentioned that the non-linearity introduced by the transconductor should also be considered and its contribution minimized in order to prevent large errors in the signal reconstruction. Since source degeneration techniques are not applicable in this architecture, the adopted solution relies on the biasing of the transconductor differential pair with large overdrive voltages.

According to [157] this technique can be used to mitigate the impact of the 3rd order harmonic generated by the non-linearity of the amplifier, which is typically also the dominant component in differential architectures. In this scenario, a relatively large overdrive voltage of 9 V has been chosen, which further leads to a 3rd order Harmonic Distortion coefficient (HD3) defined according to [157] of 40 dBc (simulated at the estimated maximum output swing). Next, by using Eq. (53) and assuming f1=1 Hz, f2=250 kHz (equal to the AAF cut-off frequency), according to the application requirement, a minimum SNR of 62 dB should be guaranteed. This value decreases to 58 dB if the safety margin on the ADC full scale is considered (Figure 90). The required SNR can be achieved with a minimum channel width W=150 µm. In reality, the SNR value slightly deviates from the estimation due to the noise components introduced by the active addressing circuit and to the residual noise folding contributions associated to the first order low pass AAF response. For the given W and overdrive voltage, the gm value of M1 and M2 does not exceed 0.25 µS. As a consequence, part of the current signal dynamic range could be comparable or even dominated by the off-current contributions of the OTFTs placed in the active-matrix addressing circuit, potentially causing large errors in the readout. Indeed, as discussed in Chapter 4, the OTFT off-current is sensitive to environmental conditions (e.g. light exposure) and can drift during time. This makes the use of calibration techniques to systematically remove the unwanted current contributions unpractical. In order to mitigate these issues and preserve the signal integrity, both transistors M1,M2 (Figure 92) have been sized with a channel width W=4000 µm. In these conditions, each driver transistor of the Gm stage exhibits a simulated transconductance value of gm= 2.6 µS which is 3 dB lower than its initial value, at a frequency of f_C=41 kHz, yet well above the bandwidth specified in application requirements. The Gm stage is biased with a tail current of 28 µA leading to a simulated achievable SNR of approximately 76 dB (in the bandwidth 1Hz – 250 kHz), which is more than sufficient for the given application requirements. It is clear however, that the design of proposed pixel electronics aims to maximize the signal integrity at the cost of larger power consumption.

Since the circuit performance is not desensitized from the OTFT parameter variability, the matrix backplane requires a gm calibration prior to its use in the target application. Even though the calibration of each pixel is typically expensive and cumbersome, this is in any case required in order to account for the piezoelectric coefficient variability of the pressure sensors. A first-order calibration of the entire acquisition chain could be performed at once by using drop tower tests in combination with reference force meters [97]. In this case, the force excitation should engage with an applied force uniformly distributed over the entire pressure sensing surface.

Finally, four current switches are connected to the outputs of the transconductance amplifier following the arrangement shown in Figure 92. The transistors M3,M5 enable the pixel readout when the row selection signal V_{ROW} is asserted, while steering the output currents to V_{SS} by means of M4,M6 during in the remaining time. The bleeding current paths provided by the transistors M4, M6 enable high speed current switching performance in exchange for large power dissipation. This trade-off is necessary here to meet the required frame rate specifications. In this conditions, circuit simulations reveal a settling time of T_{SET}=17.6 µs required for the Gm output currents to achieve a marginal error <5% from the steady state value.

For completeness, the proposed pixel electronics require the following supply and bias voltages: V_{DD}=35 V, V_{SS}=0 V, V_{B1}=17 V, V_{B2}=5 V. In addition, the complementary signals V_{ROW} and $\overline{V_{ROW}}$ used for the pixel addressing should swing between ±18V.

The implementation of the proposed pixel backplane electronics requires 7 OTFTs and 2 resistors, which are accommodated in an area of approximately 0.5 cm^2. Following the approach proposed in Chapter 6, it is possible to determine a rough estimation of the matrix pixel yield (backplane only). Indeed, by using Eq. (44) the probability of a fully functional pixel is associated to the probability that both frontend electronics and active-matrix addressing circuit are fully working. Since the implementation of the pixel electronics requires 9 devices while the AMUX devices contained in the 4 remaining rows are 8 (only 2 OTFTs in a pixel are effectively connected to the matrix column), the probability of obtaining a fully functional pixel is given by Eq. (55)

$$\mathrm{P_{PIXEL}} = \mathrm{P_{DEV}}^{17} \tag{55}$$

where P_{DEV} is equal to the transistor yield value for this technology. Thus, in the proposed architecture is expected that about 96% of the matrix pixels will be fully functional. It is important to remark that for the same considerations discussed in Chapter 6, this estimation can only be used to obtain a rough indication of the circuit yield performance.

7.4 System integration

As discussed in Section 7.2, the proposed system-on-foil consists of a sensing frontplane laminated with backplane OTFT electronics. The foil lamination needs to guarantee stable electrical interconnections between the two submodules, even under mechanical stress (impact tests, etc...). Since both sensors and OTFT electronics are fabricated with additive processes starting from plastic substrates, the electrical interconnection of the two foils can be obtained by means of physical contact between the sensor electrodes (not covered by a passivation layer) and the bonding pads developed on the backplane (Figure 93(b)). In order to maintain a mechanically stable connection, conductive adhesive microdots have been sandwiched between frontplane and backplane as shown in Figure 93(a). An insulating black adhesive sheet has been pre-patterned by means of laser cut and glued between sensors and electronics to improve the mechanical stability of the system, while allowing the electrical interconnection of the foils (Figure 93(a)). The lamination procedure is finalized with a second black adhesive sheet used as light shielding layer for the OTFT electronics. As discussed in the previous chapters, by exposing the OTFTs to ambient light, the transistor off-current increases dramatically, significantly reducing the achievable I_{ON}/I_{OFF} ratio, and thus negatively impacting on the performance of the frontend electronics.

For clarity, a summary of the lamination process is provided in Figure 93(a) while the layout of a generic matrix pixel (backplane only) is shown in Figure 93(b).

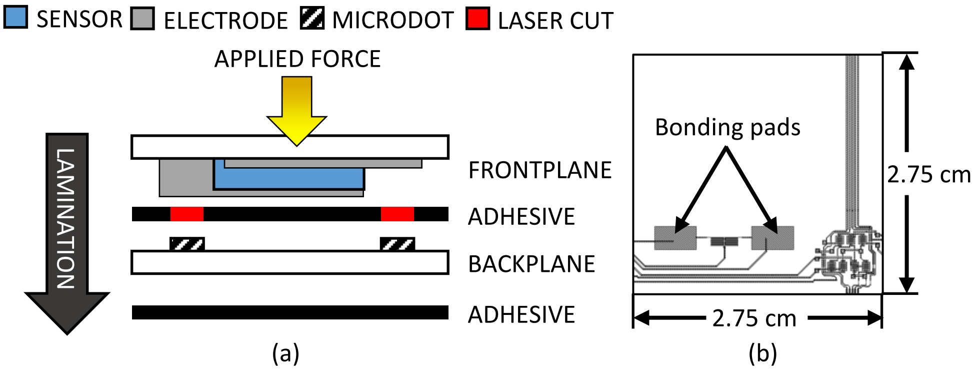


Figure 93. (a) Lamination process: cross-section view of the proposed system-on-foil. (b) Layout (top view) of the OTFT electronics of a generic matrix pixel.

7.5 Measurement results

The backplane of the proposed pressure sensing matrix has been developed on a 126 x 126 mm^2 plastic submodule area (Figure 94(a)) with the fabrication process presented in Chapter 2. The matrix frontplane (Figure 94(b)) has been manufactured and the pressure sensors individually poled using the process described in Section 6.2. At last, the micrograph of the Si-IC fabricated with a standard 65nm CMOS technology process is presented in Figure 94(c).

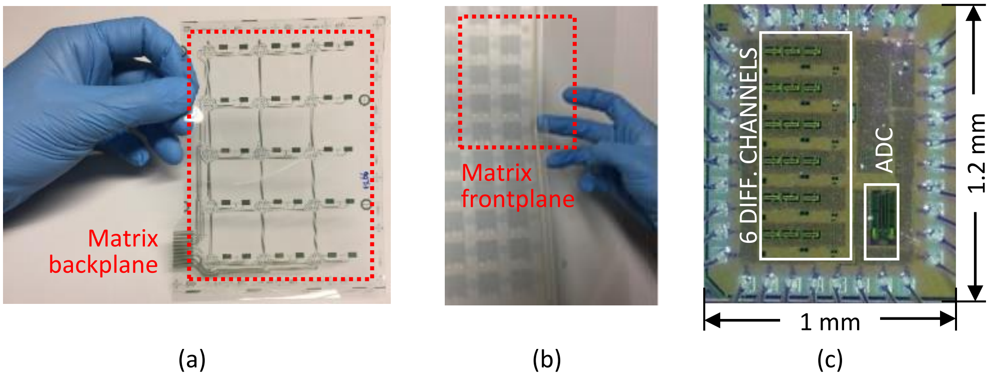


Figure 94. (a) Fabricated module containing the matrix backplane electronics. (b) Manufactured array of piezoelectric sensors (matrix frontplane). (c) Micrograph of the Silicon chip.

Pixel backplane characterization: the electrical performance of the electronics contained in the matrix pixel has been evaluated at first. Frequency domain characterizations have been used to assess respectively the small signal gain of the Gm stage, its linearity performance and obtain an indication of the frontend electronics noise level. For these characterizations the pixel backplane electronics have been connected to the readout circuit based on discrete off-the-shelf components as shown in Figure 95(a). The input signal used in the frequency characterization is provided by the HP3588A Spectrum Analyzer and further fed to a Single-ended-to-Differential (S2D) conversion module which is applied to the input of the pixel electronics. These interconnections require the use of test probes which directly land on the bond pads of the pixel (Figure 93(b)). The current readout is performed by two discrete TIAs which outputs are combined by means of a Differential-to-Single-ended (D2S) converter and connected to the spectrum analyzer. For completeness, each TIA uses an AD8066ARZ operation amplifier in combination with a feedback resistor of 300 kΩ. The small signal AC response of the pixel backplane electronics has been evaluated using an input sine-sweep signal with amplitude V_S=100 mV_{PEAK}. During this characterization, the signals V_{ROW} and $\overline{V_{ROW}}$ are held to constant bias voltages, respectively -18 V and +18 V. The measurement results presented in Figure 95(b) show a transconductance gain value of gm=2 µS and cut-off frequency of f_C=29 kHz, deviating from simulation results by -20% and -30%, respectively. These discrepancies could be caused by OTFT parameter variability but to a lesser extent by printing process issues such as misalignment and finite engraving resolution of the OSC layer (discussed in Chapter 2). In the two latter cases, the printed transistors might feature different ratios between C_{GD} and C_{GS} parasitic capacitances, which also modifies the loading impedances in the circuit nodes and thus the speed performance. Another possible cause of the low cut-off frequency value could be related to the reduction of the organic semiconductor mobility which typically occurs at relatively high frequency of operation.

The noise performance of the pixel backplane electronics has been also evaluated with the same measurement setup. In this case, the single-ended-to-differential converter placed at the input provides only the bias voltage for the transconductor differential pair, while no AC signal is applied. Also in this case, the four current switches are driven with bias voltages in order to permanently enable the pixel to be readout. The recorded Noise Power Spectral Density is provided in Figure 95(c). The measurement results clearly highlight that in the frequency range of analysis the noise corner frequency is not yet detected and that the 1/f noise contributions of the OTFTs are the dominant noise components. The integrated output-referred current noise over the entire analyzed bandwidth is equal to 0.88 nA_{RMS} which for the measured gm value leads to a maximum SNR of 82 dB. These results are obtained with a total current consumption of 31.6 µA. The achieved SNR is approximately 6 dB higher than the simulated one. However, in order to properly compare the two results, the measured noise PSD should be integrated over a larger frequency range. Unfortunately, due to the bandwidth limitation of the spectrum analyzer the frequency span of the analysis has been restricted to 1 Hz – 100 kHz.

The characterization in time domain has been used to evaluate the speed performance of the current steering active addressing circuit. In this case the measurement setup has been modified in the following way: first, both single-ended-to-differential and differential-to-single-ended converter have been removed and the inputs of the Gm stage were connected to opposite bias voltages in order to unbalance the differential pair. Next, the outputs of the two TIAs have been recorded with the National Instrument data acquisition board NI 6259 DAQ running at a sampling rate of 500 ksample/s. In addition, the board is also used to generate the line addressing signal (T_{ROW}=400 µs in this analysis) for pixel selection. However, in order to match the voltage level (±18V) required for the complementary row enable signals V_{ROW} and $\overline{V_{ROW}}$, two comparators based on off-the-shelf components have been used as interfacing electronics. The differential signals recorded at the outputs of the TIAs during the addressing operation is presented in Figure 95(d). The settling time T_{SET} required by the differential output signal to reach a marginal error $\delta<5\%$ (from the steady state value) is for this sample equal to $T_{SET}=16$ µs which is in good agreement with the simulation results.

For completeness, all the measurements (unless otherwise specified) are performed using the following bias voltages: $V_{DD}=35$ V, $V_{SS}=0$ V, $V_{B1}=17$ V, $V_{B2}=5$ V.

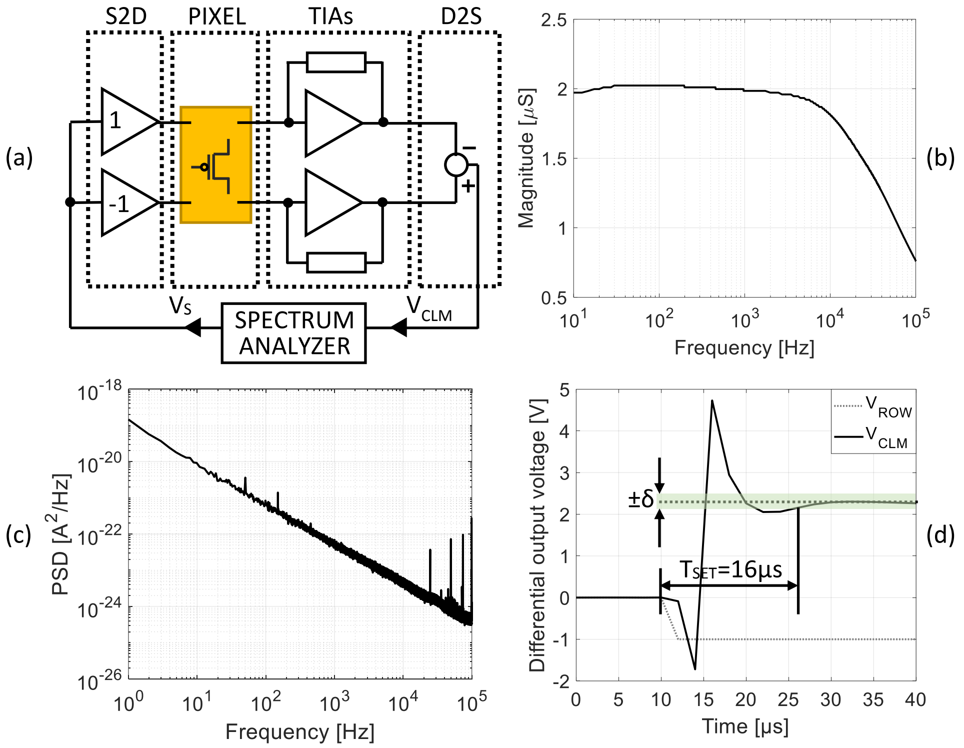


Figure 95. (a) Simplified block diagram of the measurement setup used for the characterizations in the frequency domain. (b) Frequency response of the pixel backplane electronics. (c) Output refereed noise PSD of the pixel backplane electronics (rectangular window, averaging factor=100). The spurious harmonics visible in the PSD are due to the interference coupled with the measurement setup. (d) Transient response of the pixel selection and settling time required by the differential output voltage to reach a marginal error $\delta<5\%$ from the steady state value. The signal V_{ROW} has been normalized to improve the clarity.

Complete matrix backplane characterization: all the pixels of 4 different matrix backplanes manufactured within the same campaign have been characterized in static conditions as well as in dynamic ones (in frequency and time domain). In this perspective, four main indicators have been extracted from the measurement dataset, which are: bias current $I_B=2I_0$ and current mismatch ΔI_0 (between branches) of the Gm stage, transconductance gm of the pixel electronics and the time T_{SET} required by the differential output signal to reach an error smaller than 5% from the steady state value. The two measurements setups used for these characterizations have been already described in the previous section.

All the analyzed pixels are fully-functional with the exception of 3 (connected to the same column) which have been damaged during the foil handling. Even accounting these as faulty, the matrix pixel yield (only backplane) remains as high as 95%, which appears to be in line with the prediction provided in Section 7.3.2. However, due to the limited amount of analyzed sample it is not possible to drawn a conclusion. Each defect-free matrix backplane corresponds to 135 fully-functional devices of which 105 are OTFTs and 30 resistors.

From the soft–yield point of view, the performance of the proposed pixel electronics is expected to be relatively sensitive to the OTFT parameter variability, since specific desensitization techniques have not been applied. This can be clearly observed in Figure 96(a) where the distribution of the total circuit bias current is provided. Indeed, while the mean value of the distribution (μ_{IB}=30.9 µA) is relatively close to the simulated one, the extracted standard deviation reads σ_{IB}=4.5 µA, which is nearly 15% of the mean value.

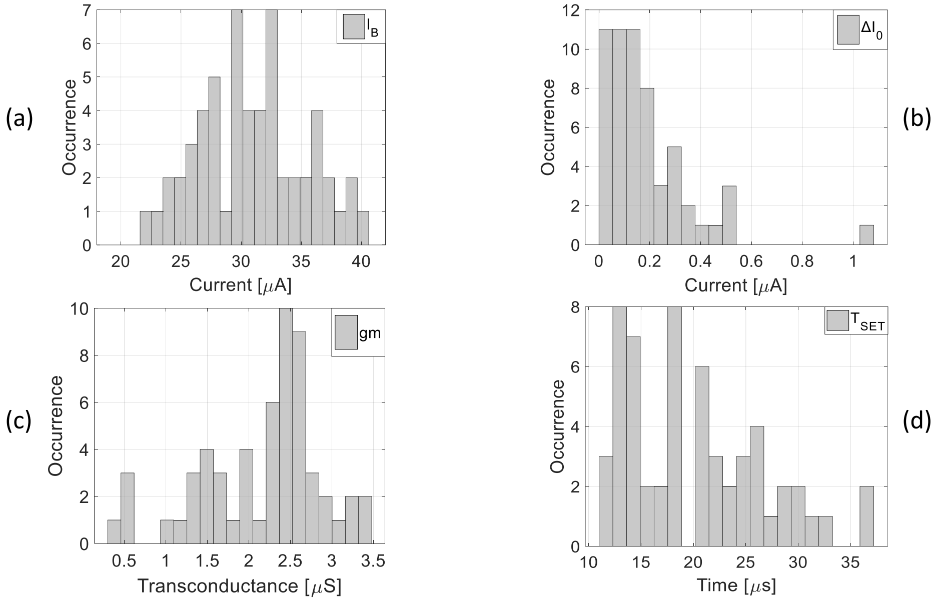


Figure 96. Statistical characterization of 57 pixels measured over 4 successive foils. (a) Histogram of the Gm stage total bias current I_B, the mean value of the distribution is μ_{IB}=30.9 µA and the standard deviation σ_{IB}=4.5 µA. (b) Histogram of the Gm current mismatch ΔI_0. Mean value $\mu_{\Delta I0}$=184 nA and and standard deviation $\sigma_{\Delta I0}$=180 nA. (c) Histogram of the Gm transconductance gain. Mean value μ_{gm}=2.1 µS and standard deviation σ_{gm}=722 nS. (d) Histogram of the output settling time required to reach a marginal error <5% from the steady state value. Mean value μ_{TSET}=20 µs and standard deviation σ_{TSET}=6.5 µs.

This relatively large spread of the bias current is expected to have a significant impact on the variability of Gm stage transconductance gain.

The distribution of the current mismatch between the two branches of the transconductor has been also accessed and the histogram of its extracted distribution is provided in Figure 96(b). The main statistical indicator extracted from the distribution, such as mean value $\mu_{\Delta I0}$ and standard deviation $\sigma_{\Delta I0}$ are respectively 184 nA and 180 nA. Even though $\mu_{\Delta I0}$ and $\sigma_{\Delta I0}$ are comparable, it is interesting to highlight that the average current mismatch is only 0.5% of the bias current mean value μ_{IB}. In this perspective, the design of the transconductor differential pair probably benefits from the use of the 40 µm channel length transistors (due to their low global parameter variability) and from the relatively large channel area.

Characterizations in the frequency domain have been used to extract the Gm transconductance gain for each analyzed pixel. The distribution obtained from the measurement database exhibits a mean value μ_{gm}=2.1 µS and a standard deviation $\sigma_{\Delta I0}$=722 nS, which is approximately 35% of μ_{gm}. The histogram of the distribution is also depicted in Figure 96(c). The gm of the transconductor suffers from a relatively large parameter spread. This is caused in large part by the variability of the tail current I_B, but also by the parameter spread of the OTFT in differential pair.

The last indicator chosen for the evaluation of the backplane electronics performance is the settling time T_{SET}. This parameter is of paramount importance especially in large-area applications exploiting active-matrix addressing circuits. Indeed, knowledge of the time required by the output to settle within a specified maximum error band ±δ, allows to estimate also the maximum frequency at which the multiplexer can operate. The histogram of the T_{SET} parameter is provided in Figure 96(d). The mean value and standard deviation extracted from the parameter distribution are respectively μ_{TSET}=20 µs and σ_{TSET}=6.5 µs. From Figure 96(d) it can be also observed that all the recorded pixel output signals can be readout with a settling error <5% using a row addressing time T_{ROW}=40 µs, further verifying the target frame rate specification.

Si-IC characterization: for the evaluation of the Silicon chip performance three main indicators have been investigated. First, the frequency response of a generic acquisition channel has been recorded. A differential current sine sweep has been used at the input of the acquisition chain to evaluate its frequency response across the frequency range 10 Hz - 1 MHz, while the differential output voltage is sampled and convertered with the on-chip ADC. During this characterization the AMUX (Figure 91(a)) is statically controlled to select only the channel under test and the gain of the AAF is set to the maximum. The measurement results provided in Figure 97(a) shows a maximum gain of the acquisition chain equal to 101.1 kΩ while the 3 dB cut-off frequency of the AAF falls at approximately 220 kHz. This gain performance corresponds in nominal conditions (Gm stage transconductance equal to 2.6 µS) to a maximum differential output swing of 1.3 V, which is relatively close to the full scale of the ADC (1.98 V). It should be remarked that this voltage mismatch is due to the safety margin (of 4 dB) introduced at the design stage.

The noise performance of the Si-frontend has been also evaluated. In this case, the AMUX channel selection has been performed at the nominal operational frequency, reaching a potential sampling rate of 5 ksample/s (per pixel). The recorded input-referred current noise PSD is presented in Figure 91(b). The integrated input-referred current noise in the bandwidth 1 Hz - 2.5 kHz is equal to 8.5 nA_{RMS}, which corresponds to an SNR of 64.2 dB leading to an ENOB of 10.3 bits, as targeted in the application requirement.

At last, the linearity performance of the acquisition chain has been assessed by means of a single tone test at 110 Hz with a differential amplitude of 18 µA. The recorded output spectrum shown in Figure 91(c) reveals a Spurious Free Dynamic Range of 62 dBc, limited in the first place by the third harmonic of the fundamental signal. Thus, it is expected that the linearity performance of the complete system (SiP+Si-IC) will be mainly determined by the matrix backplane electronics.

For completeness, the measured total current consumption of the Si-IC is approximately 1.5 mA with a supply voltage of 1.2 V.

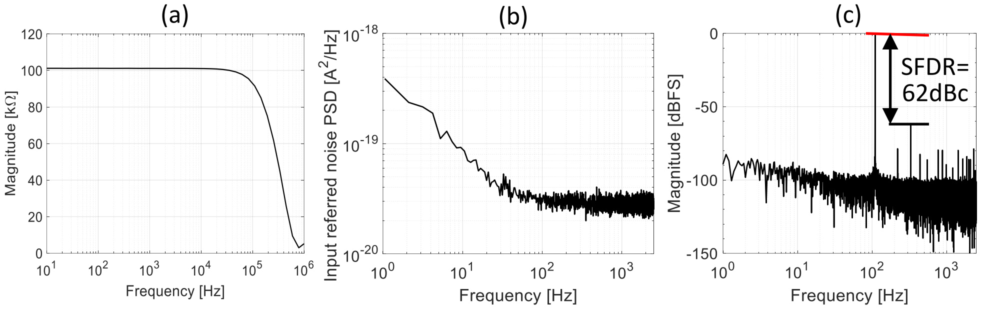


Figure 97. Performance evaluation of a generic acquisition channel of the Silicon chip. (a) Frequency response. The DC gain and 3 dB cut-off frequency are respectively equal to 101 kΩ and 220 kHz. (b) Input-referred current noise PSD (rectangular window and averaging factor=200). The integrated-input referred noise in the bandwidth 1 Hz-2.5 kHz is equal to 8.5 nA_{RMS} (c) Output spectrum obtained with a single tone test at a frequency of 110 Hz and differential amplitude of 18 µA. The extracted SFDR is equal to 62 dBc (Hanning window and averaging factor=1).

Complete system characterization (SiP+Si-IC): the performance of the complete system comprising the SiP and the Si-IC has been evaluated at first by using one of the matrix backplanes previously analyzed. The measurement setup consist of the matrix backplane connected through an interfacing PCB to the Silicon chip and a Digilent Nexys Video Artix-7 FPGA board used for the ADC digital output readout and data storage. Test probes are here used to access the matrix pixel electronics. The columns of the matrix backplane are directly connected to the Si-IC, while discrete off-the-shelf components are used to implement the 5-stage line drivers and to enable matching of the voltage levels with the SiP. The photograph of the measurement setup is provided in Figure 98.

In this configuration, the frequency response of a generic matrix pixel frontend has been measured by using one of the Silicon chip acquisition channels. The measurement results are provided in Figure 99(a). The frontend electronics exhibit a transconductance gain of 1.18 µS and a 3 dB bandwidth of 34 kHz. Even though the transconductance value is nearly a factor 2 smaller than the average measured value (2.1 µS), this result is still compatible with the outcome of the analysis provided in Figure 96(c). Similarly, also the bandwidth of the organic frontend slightly deviates from simulations and previously reported measurement results. Both effects can be attributed to OTFT parameter variability as well as aging effects.

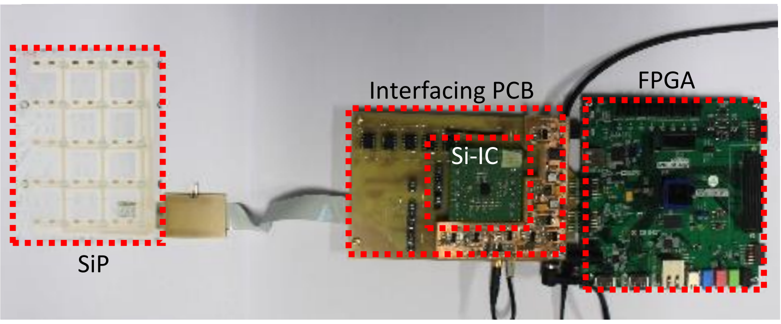


Figure 98. Photograph of the measurement setup used for the evaluation of the complete system SiP+Si-IC.

Next, the noise performance of the entire acquisition chain (SiP+Si-IC) has been investigated. For simplicity, the measured output-referred voltage noise PSD has been referred to the input of the Si-IC. From the experimental results presented in Figure 99(b) it can be clearly observed that the noise level of the complete system (red curve) is slightly higher than the previous case in which the Silicon chip only was connected (black curve). This result suggests that the noise floors of the two subsystems are in this case somewhat comparable, or that other sources of noise introduced by the measurement setup are currently reducing the SNR performance of the complete system. However, as demonstrated by the results of the characterization provided in Figure 95(c), the noise floor of the backplane electronics is well below the noise floor of the Si-chip. Therefore, the SNR reduction is most likely caused by noise sources related to the measurement setup. The integration of the input-referred current noise PSD of Figure 99(b) leads to an SNR value equal to 60.2 dB which further corresponds to an ENOB of 9.7 bit.

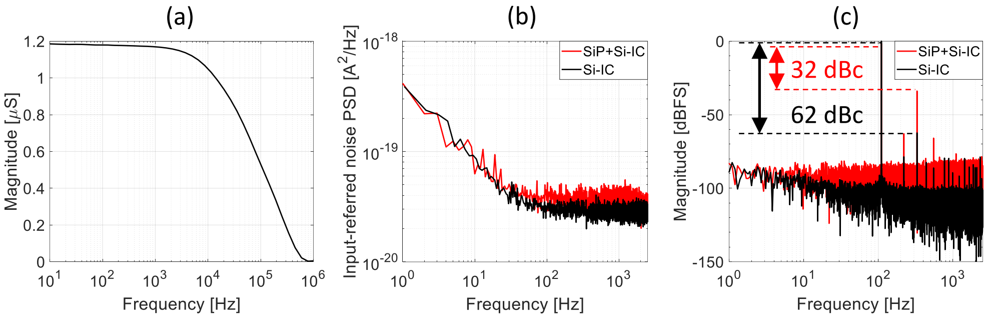


Figure 99. Performance evaluation of the complete acquisition chain (SiP+Si-IC). (a) Frequency response. The measured DC gain of the organic frontend electronics is equal to 1.18 μS, while its 3 dB cut-off frequency is 34 kHz. (b) Comparison between the current noise PSD (referred to the input of the IC) recorded with (red) and without (black) the SiP (rectangular window and averaging factor=100). (c) Output spectrum obtained with single tone test at a frequency of 110 Hz using the complete system (red) and the Si-IC only (black). The extracted SFDR is in the first case 32 dBc and 62 dBc in the second (Hanning window and averaging factor=1).

The linearity performance of the complete system has been also evaluated. A single tone test at a frequency of 110 Hz and differential amplitude of ±2.5 V has been applied at the input of the pixel frontend electronics. It is worth mentioning that a single tone test at 110 Hz has been used in this case in order to be consistent with the Si-IC characterization, even though the frequency range of analysis falls beyond the bandwidth specified by the application requirements. The output spectrum provided in Figure 98 (c) reveals a SFDR of the complete acquisition chain equal to 32 dBc, which is about 9 dB worse than the simulated one. As mentioned above and clearly visible in Figure 98 (c), the linearity performance is mainly determined by the flexible circuit, and thus this discrepancy could be related to the large parameter spread of the OTFTs which further affects the biasing of the organic circuit.

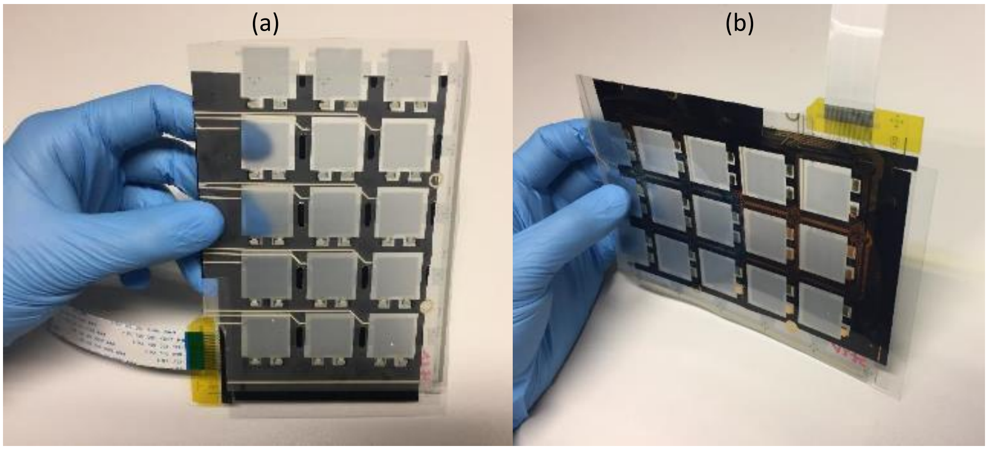
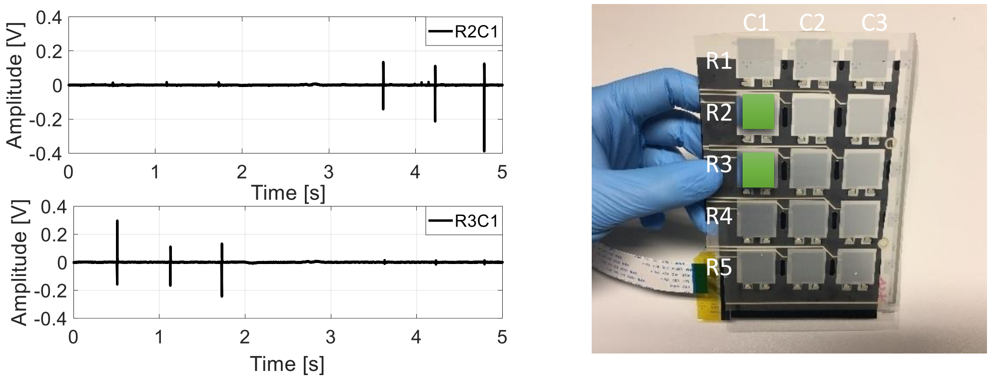


Figure 100. Large-area pressure/impact force sensing surface prototype. Top (a) and bottom (b) view.

At last, the functionality of the system as large area impact matrix sensing surface has been experimentally demonstrated. The sensor frontplane (Figure 94(a)) and the matrix backplane (Figure 94(b)) electronics have been laminated according to the procedure described in Section 7.4. The photograph of the prototype is provided in Figure 100. Differently from the proximity sensing surface discussed in Chapter 6, the lamination process was not responsible for any pixel failures, leading to an element matrix yield of 100%. Thanks to the larger matrix pitch and simpler assembly process, the lamination of this prototype is typically less challenging than the proximity sensing surface one. The prototype functionality check has been performed by means of hammering tests on individual pixels of the matrix.

These functionality tests have been recorded with the Si-readout electronics based on off-the-shelf components and already developed for the time domain characterizations provided in Figure 96(d). Indeed, at the time when the pressure sensing surface functionality check was performed, the Si-IC subsystem was not yet finalized. The matrix was scanned at the nominal frame rate of 5 kframe/s, and the three differential output signals (V_{CLM1-3}) were sampled and converted by means of the NI 6259. Finally, the output signals have been demultiplexed and the offset voltages subtracted by means of calibration.

The signals recorded from two pixels of the same column during a hammering test are provided in Figure 101(a). This test consisted of three consecutive hits on the pixel identified by the coordinate R3C1 (Figure 101(b)), followed by with three additional excitations applied on the pixel R2C1. The sequence of the impact forces can be clearly distinguished from the noise floor of the time evolution signals provided in Figure 101(a). Moreover, it can be observed that the impact forces applied on a pixel are also detected (with a minor amplitude) on the other one. This is probably due to the shear forces caused by the impact as well as vibration of the measurement setup support rather than by the electrical cross talk between pixels. In the perspective of employing the prototype in the target application, both effects can be mitigated by introducing the system-on-foil in the mechanical structure proposed in [97].



(a) (b)

Figure 101. (a) Hammer impact tests performed on the proposed pressure sensing surface. The first three mechanical excitations are applied on the pixel R3C1 and the three successive on the pixel R2C1. (b) Pixel identification convention (system on-foil-top view).

It is clear however, that a more quantitative characterization of the proposed pressure sensing surface, in combination with the Si-IC readout electronics is required. This could be performed by exploiting a drop tower setup in which the impact tests are recorded (at the same time) with the proposed system and with commercial force meters as discussed in [97]. At the moment of the manuscript preparation these tests are still ongoing and therefore further results cannot be provided.

For clarity, the main indicators of the system performance are summarized in Table 16.

Table 16. Main performance indicators of the proposed pressure sensing surface.

	Parameter	Symbol	Value	Unit
SiP frontend	Matrix elements			
	Gain	gm	2	µS
	Bandwidth		29	kHz
	Settling time (at marginal error <5%)	T_{SET}	16	µs
	Integrated input referred current noise		0.88	nA_{RMS}
	SNR (bandwidth 1 Hz – 100 kHz)		82	dB
	Power consumption		1	mW
	Supply voltage	V_{DD}	35	V
	Area		0.5	cm^2
	Required number of devices		9	
	Yield performance (over 60 samples)		95	%
Si-IC back end				
	Gain		101.1	kΩ
	Bandwidth		220	kHz
	Integrated input referred current noise		8.5	nA_{RMS}
	SNR (bandwidth 1 Hz – 2.5 kHz)		64.2	dB
	SFDR (@ 18 µA diff. inp. curr. amplitude)		62	dBc
	Power consumption*		1.8	mW
	Supply voltage	$V_{DDSi\text{-}IC}$	1.2	V
	Area*		1.2	mm^2
SiP + Si-IC				
	Number of elements		3x5	
	Gain (entire acquisition chain)		480	V/A
	Bandwidth		2.5	kHz
	Matrix readout frame rate	F_{RATE}	5	Kframe/s
	Integrated input referred current noise		13.6	nA_{RMS}
	SNR (bandwidth 1 Hz – 2.5 kHz)		60.2	dB
	Dynamic range		56.2	dB
	SFDR (@ 5 V diff. input voltage amplitude)		32	dBc
	Power consumption**		16.8	mW
	Total area		113.5	cm^2

*Of the complete Si-IC

**Excluding the 5-stage line drivers

7.6 Conclusions

This work demonstrates for the first time in literature the integration of a customized Si-IC fabricated with a standard 65nm CMOS process with a low cost System in Package (SiP) for large-area pressure sensing applications, developed with printed organic materials. The SiP contains printed piezoelectric sensors connected in a 5 x 3 matrix arrangement by the frontend OTFT electronics. The direct interconnection of the two subsystems is typically challenging due to the very different operating voltage of the OTFTs and Si-IC electronics, which require respectively V_{DD}>20 V and $V_{DDSi\text{-}IC}$<1.2 V. The solution proposed in this work overcomes this problem by using a current mode readout approach, which maintains the nodes of the interface electronics at a safe potential thanks to the virtual ground provided by the input stage of the Si-IC. The current signal collected by the Si-IC is further conditioned and digitized with a 12 bit SAR ADC inside the chip.

The matrix pixel fronted electronics are equipped with a fully differential Gm stage to convert the sensor signal from voltage to current domain and four current steering switches to achieve high speed multiplexing. The measured Gm stage performance achieves a gain of about 2 µS, a cut-off frequency of 29 kHz, and an SNR of 82 dB (in the bandwidth 1 Hz – 100 kHz) achieved with a power consumption of 1 mW. The settling time required by the differential output signals to reach a marginal error <5% of the steady state value is typically <40 µs, thus demonstrating matrix readout frame rate as high as 5 kframe/s. The results of the statistical characterizations of the pixel frontend electronics reveal spread of the main performance indicators of 20% - 30% from the mean value. The acquisition channel of the Silicon back end electronics achieve a typical gain performance of 101.1 kΩ with a 3 dB bandwidth of 220 kHz and an SNR of 64.2 dB (ENOB=10.3 bit), achieved with a power consumption of 1.8 mW. The SNR performance reduce to 60.2 dB (ENOB=9.7 bit) when the SiP is also connected. This loss of performance is attributed to noise sources introduced by the measurement setup. At last, the linearity performance of the complete system is limited by the SiP, achieving an SFDR of 32 dBc (with a full-scale input signal), limited by the third harmonic of the fundamental signal.

Preliminary mechanical tests have been also performed and impact force detections have been successfully demonstrated with the proposed system-on-foil. The availability of such pressure sensing surfaces could be used for applications in the markets of automotive, environment monitoring and smart buildings, where large-area coverage, large dynamic range of forces and relatively high readout frame rate are requires. Moreover, the approach proposed for the interconnection of the SiP with the Si-IC, could be further extended to new classes of smart sensing solutions enabling the fabrication of low cost electronic devices, with unprecedented mechanical properties and reduced footprint thanks to the minimum number of discrete components required.

8. Conclusions

New design methodologies and circuit solutions have been proposed and demonstrated to tackle two of the major challenges in circuit design with printed organic technologies, which are the large parameter variability and the limited yield. The main idea relies on the use of circuit techniques which systematically desensitize the circuit performance from the OTFT parameter variations. Jointly, the circuit implementations aim also to minimize the number of required devices in order to maximize the overall circuit and system yield. These techniques have been further used to demonstrate robust systems-on-foil for a new class of smart sensing applications which benefit from the mechanical flexibility and large area-coverage achieved at a low price.

The fundamental enabler for the development of these new design methodologies is a deep investigation of the OTFT technology weaknesses together with the printed process capabilities. The effectiveness of the design methodologies and circuit implementations can be assessed using suitable simulations. Moreover, in order to enable the design of complex systems-on-foil, a Process Design Kit (PDK) specifically tailored to the gravure-printed organic transistor technology has been developed. The PDK includes for the first time in literature a thorough description of the static, dynamic and noise behavior of an OTFT technology. The formalization of the design rules is also a crucial point in the development of the PDK. The proposed strategy allows compact descriptions with a set of only four technological parameters, which further enables quick adaptation to the advances of the technology. EDA tools such as DRC, LVS and LPE have been also enabled to assist the design flow with automatic verifications. The PDK has been integrated in the commercial framework Cadence Virtuoso®. Complex hybrid systems comprising printed organic transistors and mainstream Silicon-electronics can be now designed, simulated and automatically verified within the very same software environment.

The methodology proposed for the design of digital circuits with unipolar printed technologies exploits the combination of different inverter topologies within the same functional block. Compared to the classical approach which uses only one basic inverter topology, this strategy allows to exploit the key features of each inverter configuration in the critical points of the circuit, enabling the reduction of complexity (in terms of transistor count), power consumption and area occupation, while ensuring correct functionality. This methodology has been used to design three different 8-stage line driver circuits (based on respectively dynamic and pseudo-static logics) for display and matrix addressing applications. Multistage line drivers circuits fabricated with unipolar printed organic technologies have not been demonstrated before in the literature, probably due to the reliability issue associated to the relatively large number of devices required for their implementation. The results of the statistical analysis reveal that the yield performance is different for the three configurations starting from a minimum of 65% and reaching 100% for one of the implementations based on dynamic logic. The yield performance of the latter architecture is extracted over 15 samples, meaning that the addressing of a 120-row matrix suitable e.g. for flexible displays featuring Quarter Quarter Video Graphics Array (QQVGA) resolution (160 x 120 pixels) can be enabled by printed electronics. This architecture achieves also the best performance in terms of energy efficiency, area occupation, integration density and number of transistors required among the analyzed configurations.

The methodology proposed for the design of digital circuits has been also used to develop an inexpensive disposable smart sensor on RFID for temperature monitoring applications. The temperature sensing relies on resistive printed temperature sensors, while the signal conditioning exploits a highly digital architecture based on a BBPLL time-based interface. The proposed ratiometric sensor readout provides a simple but effective approach to mitigate the effects of the OTFT parameter variability on the system performance. The experimental results demonstrated that the system-on-foil is capable of sensing the environment temperature between 3 °C and 27 °C, converting it into a robust digital representation, and further transmitting the data to a base station reader, using ASK modulation on a 13.56 MHz RF communication link. In addition, the harvesting circuit enables the energization of the tag from the RF carrier. The smart sensor requires a conversion time of 2 s to achieve a resolution of 270 mK_{RMS}, leading to a resolution FoM of 291 μJK^2. A 3σ inaccuracy of ±1.6 °C is obtained in the temperature range from 3 °C to 27 °C, after systematic non-linearity removal and 2-point calibration. By using a third calibration point the 3σ inaccuracy can be lowered down to ±1.2 °C. Even though the immunity of the system performance from supply variations, typical of unregulated RFID devices, has been considered at the design stage the measurement results show that the inaccuracy performance is still partially impacted. As a future work, the development of voltage regulators based on unipolar organic transistor could be exploited to further improve the performance of the smart sensor. To the author’s knowledge, this work presents for the first time in literature a smart temperature sensor on RFID, fabricated with a gravure-printed OTFT technology and potentially enabling temperature monitoring in cold chain applications.

Analog design techniques for the development of robust large-area sensor matrices have been also investigated. The first proposed system-on-foil demonstrates for the first time in literature, a 5 x 10 fully-printed large-area proximity sensing surface integrating Analog Frontend Electronics in each pixel. This solution exploits local signal amplification (within the matrix pixel) using a reduced number of devices. Closed loop amplifier configurations obtained with passive feedback networks have shown to tolerate large OTFT parameter spread without significantly affecting the frontend electronic performance. A TDM technique has been used to aggregate multiple pixels and thus reduce the number of interconnections with the Silicon readout electronic. The results of the statistical analysis performed over 200 pixels, reveal an average defectivity rate of 18% which proves the robustness against hard failures and device parameter viability of the architecture. The highest number of fully-working pixels recorded among the same matrix backplane is 48 out of 50, which corresponds to 768 fully-functional devices. This result attains the largest circuit complexity (in terms of device count) ever achieved by a printed OTFT circuit to date. Proximity detections at 100 frame/s of human hand approaches from different directions up to 40 cm distance and position tracking of a localized movable heat source have been demonstrated. These results prove that printed electronics can be potentially used to fabricate low-cost solutions suitable for human proximity detection which could increase the level of security (collision avoidance), improve the interaction modalities and significantly reduce the costs in HRI applications.

At last, a design approach suitable to develop analog and mixed signal systems which integrate two heterogeneous technologies has been explored. The proposed hybrid system integrates a low cost large area sensing surface (System-in-Package (SiP)) manufactured with organic materials and a custom Si-IC fabricated with a 65 nm standard Silicon CMOS process. The impact test/pressure sensing capability of the SiP has been successfully demonstrated combining a 3 x 5 matrix of piezoelectric sensors (frontplane) with distributed organic fronted electronics (backplane). The implementation of a current steering analog multiplexer in the backplane electronics enables high speed matrix pixel aggregation and a significant reduction of the readout interconnections. Measurement results show that the frame rate as high as 5 kframe/s can be achieved. The outcome of the statistical yield analysis highlights that the pixel electronics benefit from simple and compact circuit implementation, reaching a defectivity rate as low as 5%. On the contrary, the spread of the main frontend performance indicators is relatively large (20% - 30% from the mean value) since no desensitization techniques have been applied. The voltage-to-current conversion performed in the pixel frontend electronics allows to realize a current mode interface, removing the major limitations in the direct interconnection of the two subsystems, which is the very different operating voltage of the OTFTs and Si-IC. The integration and the successful readout of the matrix backplane at the nominal frame rate with the Si-IC has been also demonstrated. The complete system achieves an SNR performance of 60.2 dB (ENOB=9.7 bit) and an SFDR of 32 dBc (at the estimated maximum input signal amplitude), with a total power consumption of 16.8 mW. This system is expected to enable low cost solutions for pressure sensing applications which require large-area coverage, large dynamic range of force detection and relatively high readout frame rate. Moreover, the approach proposed for the design of hybrid PE/Si-IC systems, could be further extended to new classes of smart sensing solutions with unprecedented form factors and reduced cost thanks to the minimum number of Si/PE interconnections needed.

Bibliography

[1] G. Moore “Cramming more components onto integrated circuits”, Electronics, vol. 1, no. 8, April 1965.

[2] G. Moore “Progress in Digital Integrated Electronics”, IEEE International Electron Device Meeting, vol. 21, pp. 11-13. 1, February 1975.

[3] R.H. Dennard, F.H. Gaensslen, V.L. Rideout, E. Bassous, A.R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions”, IEEE Journal of Solid State Circuits, vol. 9, no. 5, pp. 256–268, October 1974.

[4] C. Mack, “The Multiple Lives of Moore’s Law”, IEEE Spectrum, vol. 52, no. 4, pp. 31-37, April 2015.

[5] Semiconductor Industry Association *et al*, “International Technology Roadmap of Semiconductors (ITRS)”, chapter on Emerging Research Devices (ERD), International Roadmap Committee, 2011.

[6] V. Pecunia, M. Fattori, S. Abdinia, H. Sirringhaus, E. Cantatore,”Organic and amorphous-metal-oxide flexible analogue electronics”, Series: Elements in Flexible and Large-Area Electronics, Cambridge University Press, Cambridge, United Kingdom, May 2018.

[7] H. Sirringhaus, “25th anniversary article: organic field-effect transistors: the path beyond amorphous silicon”, Adv. Mater., vol. 26, no. 9, pp. 1319–35, Mar. 2014.

[8] R.S. Howell et al., “Poly-Si thin-film transistors on steel substrates”, IEEE Electron Device Letter, vol. 21, no.2, pp. 70-72, February 2000.

[9] S. An et al., “2.8-inch WQVGA Flexible AMOLED Using High Performance Low Temperature Polysilicon TFT on Plastic Substrates” SID Symposium Digest of Technical Papers, vol. 41, no. 1, pp. 706-709, May 2010.

[10] H. H. Hsu et al., “High mobility InGaZnO thin film transistor using narrow-bandgap titanium-oxide semiconductor as channel capping layer,” 72nd Device Research Conference, June 2014.

[11] P. G. Bahubalindruni et al., “Influence of Channel Length Scaling on InGaZnO TFTs Characteristics: Unity Current-Gain Cutoff Frequency, Intrinsic Voltage-Gain, and On-Resistance,” J. Disp. Technol., vol. 12, no. 6, pp. 515–518, Jun. 2016.

[12] M. Nikolka et al., “Unprecedented operational and environmental stability of high-mobility conjugated polymer field-effect transistors achieved through the use of molecular additives,” 2016.

[13] F. Ante et al., “Low-voltage metal-gate top-contact organic thin-film transistors and complementary inverters with submicron channel length”, IEEE Device Research Conference, University Park, PA, USA, 2009.

[14] W. Xiong, et al., “A 3-V, 6-Bit C-2C Digital-to-Analog Converter Using Complementary Organic Thin-Film Transistors on Glass”, IEEE Journal of Solid-State Circuits, vol.45, no. 7, July 2010.

[15] S. Jacob, et al., “High performance printed N and P-type OTFTs for complementary circuits on plastic substrate”, Proceedings of the 42nd European Solid State Device Research Conference (ESSDERC 2012), Firenze, Italy, September 2012.

[16] M. Guerin, A. Daami, S. Jacob, E. Bergeret, E. Bènevent, P. Pannier, R. Coppard: High gain fully printed organic complementary circuits on flexible plastic foils, IEEE Transaction on Electron Device, vol. 99, pp 1-7, August 2011.

[17] J. Liu, et al., “Flexible Low-Power Organic Complementary Inverter Based on Low- k Polymer Dielectric” IEEE Electron Device Letters, vol.38, no. 10, October 2017.

[18] A. Spanu, et al., “Organic FET device as a novel sensor for cell bioelectrical and metabolic activity recordings” 2013 6th International IEEE/EMBS Conference on Neural Engineering (NER), 2013.

[19] D. Khodagholy, T. Doublet, P. Quilichini, M. Gurfinke, P. Leleux, A. Ghestem, E. Ismailova, T. Herve , S. Sanaur, C. Bernard & G. G. Malliaras. “In vivo recordings of brain activity using organic transistors”. Nature Communications, March 2013.

[20] P. Heremans et al., “Mechanical and Electronic Properties of Thin-Film Transistors on Plastic, and Their Integration in Flexible Electronic Applications,” Adv. Mater., vol. 28, no. 22, pp. 4266–4282, 2016.

[21] Hang Huang, et al., “Inkjet-Printed In-Ga-Zn Oxide Thin-Film Transistors with Laser Spike Annealing”, Journal of Electronic Materials, vol. 46, no.7, pp. 4497-4502, July 2017.

[22] G.Grau et al.,"Fully High-Speed Gravure Printed, "Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation", Advanced Electronic Materials, vol.2, no. 4, April 2016.

[23] Junfeng Sun et al.,"Proving Scalability of an Organic Semiconductor To Print a TFT-Active Matrix Using a Roll-to-Roll Gravure", ACS Omega, vol. 2, no. 9, pp. 5766-5774, 2017.

[24] Y. Takeda et al.,"Organic Complementary Inverter Circuits Fabricated with Reverse Offset Printing" Advanced Electronic Materials, vol.4, no.1, 2018.

[25] J. Rockenberger et al., “Printed, self-aligned, top gate thin film transistor”, US8796125 B2, 2014.

[26] M. G. Kane, et al., “Analog and digital circuits using organic thin-film transistors on polyester substrates,” IEEE Electron Device Lett., vol. 21, no. 11, pp. 534–536, Nov. 2000

[27] N. Gay and W. J. Fischer, “OFET-based analog circuits for microsystems and RFID-sensor transponders,” 6th Int. IEEE Conf. Polym. Adhes. Microelectron. Photonics, Polytronic 2007, Proc., no. 0, pp. 143–148, 2007.

[28] H. Marien, et al., “An analog organic first-order CT ΔΣ ADC on a flexible plastic substrate with 26.5dB precision,” in ISSCC Dig. Tech. Papers, pp. 136–137, February 2010,

[29] M. Guerin, et al., “High-gain fully printed organic complementary circuits on flexible plastic foils,” IEEE Trans. Electron Devices, vol. 58, no. 10, pp. 3587–3593, October 2011.

[30] I. Nausieda, et al., “Mixed-signal organic integrated circuits in a fully photolithographic dual threshold voltage technology,” IEEE Trans. Electron Devices, vol. 58, no. 3, pp. 865–873, Mar. 2011.

[31] H. Marien et al., “A mixed-signal organic 1kHz comparator with low VT sensitivity on flexible plastic substrate”, Proceedings of ESSCIRC, Athens, Greece, September 2009.

[32] D. Raiteri et al. “A synchronous rail-to-rail latched comparator based on double-gate organic thin-film-transistors”, Proceedings of the ESSCIRC (ESSCIRC), Bordeaux, France, September 2012.

[33] R.W.Wanjau et al., “Design of a high gain organic comparator for use in low-cost smart sensor systems”, 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), Glasgow, UK, July 2015.

[34] D. M. Taylor et al., “Organic digital logic and analog circuits fabricated in a roll-to-roll compatible vacuum-evaporation process,” IEEE Trans. Electron Devices, vol. 61, no. 8, pp. 2950–2956, August 2014.

[35] M. Torres-Miranda et al., “High-Speed Plastic Integrated Circuits: Process Integration, Design, and Test”, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 7, no.1, pp. 133-146, October 2016.

[36] B. Yoo et al., “Organic Complementary D Flip-Flops Enabled by Perylene Diimides and Pentacene”, IEEE Electron Device Letters, vol.27, no. 9, September 2006.

[37] T. Yokota, T. Sekitani, Naoya Take, U. Zschieschang, et al. “Sheet-Type Flexible Organic Active Matrix Amplifier System Using Pseudo-CMOS Circuits with Floating-Gate Structure. IEEE Trans. Electron Devices, vol. 59, no.12, pp. 3434-3440, December 2012.

[38] T. Sekitani et al., “Ultraflexible organic amplifier with biocompatible gel electrodes”, Nature Communications 7 - 11425, pp. 1-11, April 2016.

[39] E. Cantatore and et al., “A 13.56-MHz RFID system based on organic transponders,” IEEE J. of Solid state Circuits, vol. 42, pp. 84-92, 2007.

[40] K. Myny and et al., “An inductively coupled 64b organic RFID tag operating at 13.56MHz with a data rate of 787b/s,” IEEE Int. Solid-State Circuits Conf. Dig. of Tech. P., pp. 290-291, 2008.

[41] K. Myny and et al., “A 128b organic RFID transponder chip, including manchester encoding and ALOHA anti-collision protocol, operating with a data rate of 1529b/s,” IEEE Int. Solid-State Circuits Conf. Dig. of Tech. P., pp. 206-207, 2009.

[42] R. Blache, J. Krumm, and W. Fix, “Organic CMOS circuits for RFID applications,” in ISSCC Dig. Tech. Papers, Feb. 2009, pp. 208–209.

[43] M. Jung et al., “All-printed and roll-to-roll-printable 13.56-MHz operated 1-bit RF tag on plastic foils,” IEEE Trans. Electron Devices, vol. 57, no. 3, pp. 571–580, Mar. 2010.

[44] G. Gelinck and et al., “Flexible active-matrix displays and shift registers based on solution-processed organic transistors,” Nature Material, vol. 3, pp. 106-110, 2004.

[45] P. van Lieshout and et al., “A flexible 240x320-pixel display with integrated row drivers manufactured in organic electronics,” IEEE Int. Solid-State Circuits Conf. Dig. of Tech. P., pp. 578-579, 2005.

[46] D. Raiteri et al., “Positive-feedback level shifter logic for large-area electronics,” IEEE J. of Solide-State Circuits, vol. 49, no. 2, pp. 524-535, 2014.

[47] A S. Abdinia et al., “Organic CMOS line drivers on foil,” Journal of Display Technology, vol. 11, no. 6, pp. 564-569, June 2015.

[48] K. Myny and et al., “An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil,” IEEE J. of Solid-State Circuits, vol. 47, no. 1, pp. 284-291, 2012.

[49] D. Raiteri and et al., “An organic VCO-based ADC for quasi-static signals achieving 1LSB INL at 6b resolution,” IEEE Int. Solid-State Circuits Conf. Dig. of Tech. P., pp. 108-109, 2013.

[50] W. Xiong and et al., “A 3V 6b successive-approximation ADC using complementary organic thin-film transistors on glass,” IEEE Int. Solid-State Circuits Conf. Dig. of Tech. P., pp. 134-135, 2010.

[51] D. E. Schwartz and T. N. Ng, “Comparison of static and dynamic printed organic shift registers,” IEEE Electron Device Lett., vol. 34, no. 2, pp. 271–273, February 2013.

[52] E. Ramon et al., “Development of a simple manufacturing process for all-inkjet printed organic thin film transistors and circuits,” IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol.7, no.1, pp. 161-170, March 2017.

[53] S. Abdinia et al., “Design of analog and digital building blocks in a fully printed complementary organic technology”, Proceedings of the ESSCIRC (ESSCIRC), Bordeaux, France, September 2012.

[54] J. Chang et al., “Fully printed electronics on flexible substrates: High gain amplifiers and DAC,” Organic Electron., vol. 15, no. 3, pp. 701–710, Mar. 2014.

[55] S. Abdinia et al., “A 4b ADC manufactured in a fully-printed organic complementary technology including resistors,” in ISSCC Dig. Tech. Papers, pp. 106–107, Feb. 2013.

[56] J. Minhun et al., "All-Printed and Roll-to-Roll-Printable 13.56-MHz-Operated 1-bit RF Tag on Plastic Foils," IEEE Transactions on Electron Devices, vol. 57, pp. 571-580, 2010

[57] R. A. Street et al., "From Printed Transistors to Printed Smart Systems", Proceedings of the IEEE, vol. 103, pp. 607-618, 2015.

[58] V. Fiore et al., “An integrated 13.56-MHz RFID tag in a printed organic complementary TFT technology on flexible substrate,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 62, no. 6, pp. 1668–1677, Jun. 2015.

[59] Y.J. Kwon et al., “Inkjet-Printed Organic Transistors Based on Organic Semiconductor/Insulating Polymer Blends”, Materials, vol. 9, no. 8, pp. 1-16, August 2016.

[60] K. Fukeda et al., “Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films”, Nature communications 5, article number 4147, 2014.

[61] G. Grau et al., “Fully High-Speed Gravure Printed, Low-Variability, High-Performance Organic Polymer Transistors with Sub-5 V Operation”, Advanced Electronics Materials, vol.2, no.4, pp.1-8, January 2016.

[62] Y. Taked et al., “Organic Complementary Inverter Circuits Fabricated with Reverse Offset Printing”, Advanced Electronic Materials, vol. 4, no. 1, pp-1-5, January 2018.

[63] O. Marinov et al., “Flicker noise due to variable range hopping in organic thin-film transistors”, 21st International Conference on Noise and Fluctuations, Toronto, Canada, June 2011.

[64] G. Giusi et al., “Correlated Mobility Fluctuations and Contact Effects in p-Type Organic Thin-Film Transistors”, IEEE Transactions on Electron Devices, vol. 63, no. 3, pp.1239-1245, March 2016.

[65] C.C. Enz et al., “Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization”, Proceedings of the IEEE, vol. 84, no. 11, pp. 1584-1614, November 1996.

[66] S. E. Burns et al., “Inkjet Printing of Polymer Thin-Film Transistor Circuits”, MRS Bulletin, vol. 28, no. 11, pp. 829-834, November 2003.

[67] S. H. Kim et al., “Damage-free hybrid encapsulation of organic field-effect transistors to reduce environmental instability”, Journal of Materials Chemistry, vol. 22, pp. 7731-7738, January 2012.

[68] N. Wrachien et al., “Visible Light and Low-Energy UV Effects on Organic Thin-Film Transistors”, IEEE Transaction on Electron Devices, vol. 59, no.5, pp. 1501-1509, May 2012.

[69] P. Bobbert et al., “Operational Stability of Organic Field-Effect Transistors”, Advanced Materials, vol.24, no. 9, pp. 1146-1158, February 2012.

[70] S. Sambandan, “High-Gain Amplifiers with Amorphous-Silicon Thin-Film Transistors”, IEEE Electron Device Letter, vol.29, no. 8, pp. 882-884, September 2008.

[71] J. Zhou et al, “Fully-Additive Printed Electronics: Process Development Kit”, Proceeding IEEE International Symposium on Circuits and Systems, Aug. 2016.

[72] T. Ge and J. Zhou, “A fully-additive printed electronics process with very-low process variations (Bent and unbent substrates) and PDK”, IEEE International Symposium on Circuits and Systems, May 2017.

[73] L. Shao et al, “Process Design Kit for Flexible Hybrid Electronics”, 23rd Asia and South Pacific Design Automation Conference, 2018.

[74] M. Charbonneau et al, ”A Large-Area Gravure Printed Process for P-type Organic Thin-Film Transistors on Plastic Substrates” 2018 48th European Solid-State Device Research Conference (ESSDERC), Dresden, Germany, September 2018.

[75] M. Fattori et al., “A gravure-printed organic TFT technology for active-matrix addressing applications”, IEEE Electron Device Letters, vol. 40, no. 10, pp. 1682-1685, October 2019.

[76] J. S. Chang et al., “A Circuits and Systems Perspective of Organic/Printed Electronics: Review, Challenges, and Contemporary and Emerging Design Approaches”, IEEE Journal of Emerging and Selected Topics in Circuits and Systems, vol. 7, no.1, March 2017.

[77] H. Klauk, “Organic Electronics – Materials, Manufacturing, and Applications”, Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, August 2006.

[78] J. Sun et al.,"Proving Scalability of an Organic Semiconductor To Print a TFT-Active Matrix Using a Roll-to-Roll Gravure", ACS Omega vol. 2, no. 9, pp. 5766-5774, 2017.

[79] G. Ghibaudo, “New method for the extraction of MOSFET parameters”, Electronics Letters, vol. 24, pp. 543-545, 1988.

[80] B. Rosner, “Percentage Points for a Generalized ESD Many-Outlier Procedure” Technometrics, vol. 25, no. 2, pp. 165-172, May 1983.

[81] M. Fattori et al., “Circuit Design and Design Automation for Printed Electronics”, 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, March 2019.

[82] F. Torricelli, “Charge Transport in Organic Transistors Accounting for a Wide Distribution of Carrier Energies - Part I: Theory,” IEEE Trans. Electron Devices, vol. 59, no. 5, pp. 1514-1519, May 2012.

[83] F. Torricelli et al, “Charge transport in organic transistors accounting for a wide distribution of carrier energies - Part II: TFT modelling,” IEEE Trans. Electron Devices vol. 59, pp. 1520–1528, 2012.

[84] F. Torricelli et al., “Unified drain-current model of complementary p- and n-type OTFTs,” Organic Electronics, vol. 22, pp. 5-11, Mar. 2015.

[85] S. Abdinia et al, “Variation-based design of an AM demodulator in a printed complementary organic technology,” Organic Electronics, vol. 15, pp. 904-912, 2014.

[86] I A. Valletta et al, “Contact effects in high performance fully printed pchannel organic thin film transistors,” Applied Physics Letters, vol. 99, no. 23, pp. 233309-1–233309-4, Dec. 2011.

[87] M. Rapisarda et al, “Analysis of contact effects in fully printed p-channel organic thin film transistors,” Organic Electronics, vol. 13, pp. 2017-2027, 2012.

[88] L. Mariucci et al, “Current spreading effects in fully printed p-channel organic thin film transistors with Schottky source–drain contacts,” Organic Electronics, vol. 14, pp. 86-93, 2013.

[89] T. Zaki et al, “Accurate Capacitance Modelling and Characterization of Organic Thin-Film Transistors”, IEEE Transactions on Electron Devices, vol. 61, pp. 98-104, Jan. 2014.

[90] B. Razavi, “Design of Analog CMOS Integrated Circuits”, Boston, MA, USA: McGraw-Hill, 2001.

[91] O. Marinov et al, “Low-frequency noise in polymer thin-film transistors”, Circuit, Devices and Systems, vol.151, pp. 466-472, 2004.

[92] F.N. Hooge, “1/f noise id no surface effect”, Physics Letter A, vol. 29, no. 3, pp. 139-140, April 1969.

[93] F.N. Hooge, “1/f Noise sources”, IEEE Transactions of Electron Devices, vol. 41, no.11, pp. 1926-1935, November 1994

[94] M. Mashayekhi et al, “Inkjet Printing Design Rules Formalization and Improvement” Journal of Display Technology, vol. 11, pp. 658–665, August 2015.

[95] M. Mizukami et al, “Flexible Organic Light-Emitting Diode Displays Driven by Inkjet-Printed High-Mobility Organic Thin-Film Transistors”, IEEE Electron Device Lett., vol. 39, no.11, January 2018.

[96] G. S. Ryu, M. W. Lee, and C. K. Song, “Printed flexible OTFT backplane for electrophoretic displays” J. Inf. Display, vol. 12, no. 4, pp. 213–217, Dec. 2011

[97] M. Fattori et al, “Organic Pressure-Sensing Surfaces Fabricated by Lamination of Flexible Substrates” IEEE Transactions on Components, Packaging and Manufacturing Technology, vol.8, no. 7, Jul. 2018.

[98] Y. Kato et al, “A large-area, flexible, ultrasonic imaging system with a printed organic transistor active matrix” in Proc. IEDM, San Francisco, USA, Dec. 2008.

[99] P. van Lieshout et al., “A flexible 240 320-pixel display with integrated row drivers manufactured in organic electronics,” in Proc. ISSCC, 2005, pp. 578–579.

[100] B. Crone et al., “Large-scale complementary integrated circuits based on organic transistors,” Nature, vol. 403, pp. 521–523, Feb. 2000.

[101] T. C. Huang et al, “Design for Low Power and Reliable Flexible Electronics: Self-Tunable Cell-Library Design”, Journal of display technology, vol. 5, no.6, Jun. 2009.

[102] J. M. Rabaey et al., “Digital Integrated Circuits, A Design Perspective”, Chapter 3, pp. 108-119, Prentice Hall 1996, Upper Saddle River, New Jersey, USA.

[103] M. I. Elmasry, “Digital MOS Integrated Circuits”, IEEE Press, Institute of Electrical and Electronics Engineers, New York, USA, 1981.

[104] H. N. Raval et al., “Solution-Processed Bootstrapped Organic Inverters Based on P3HT With a high-k Gate Dielectric Material”, IEEE Electron Device Letter, vol. 30, no. 5, pp. 484-486, May 2009.

[105] Y. Suzuki et al, “Clocked CMOS calculator circuitry,” IEEE Journal of Solid State Circuits, vol. 8, pp. 462–469, Dec. 1973.

[106] T. Moy et al., “Thin-film circuits for scalable interfacing between large area electronics and CMOS ICs,” in Device Res. Conf. Dig. Tech. Papers, pp. 271–272, June 2014.

[107] T. Sekine et al., “Highly stable flexible printed organic thin-film transistor devices under high strain conditions using semiconducting polymers”, Japanese Journal of Applied Physics, vol. 54, no. 4, March 2015.

[108] Food and Agriculture Organization of The United Nations, “Food wastage footprint. Full-cost accounting” Final report, 2014.

[109] J. Fernie, L. Sparks, “Logistics and retail management: Insights into current practice and trends from leading experts”, London and Sterling, VA, 2004.

[110] J. Snow, Inc./DELIVER in collaboration with the World Health Organization, “Guidelines for the Storage of Essential Medicines and Other Health Commodities” Arlington, VA, 2003.

[111] World Health Organization, “Model guidance for the storage and transport of time- and temperature-sensitive pharmaceutical products”, Technical Report Series, No. 961, pp. 324-372, 2011.

[112] R. Ganesan, et al, “Design of an organic electronic label on a flexible substrate for temperature sensing”, proceeding of the ESSCIRC, pp. 423-426, Sep. 2013.

[113] T. N. Ng, et al, “Printed dose-recording tag based on organic complementary circuits and ferroelectric memories”, Scientific Reports, Aug. 2015.

[114] C. Garripoli et al., “An a-IGZO asynchronous delta-sigma modulator on foil achieving up to 43dB SNR and 40dB SNDR in 300Hz bandwidth”, IEEE International Solid-State Circuits Conference (ISSCC), February 2017, San Francisco, California, 2017, pp. 260-261.

[115] S. Jung et al., “Temperature sensor using thermal transport properties in the subthreshold regime of an organic thin film transistor”, Applied Physic Letters 90, 062105, 2007.

[116] T. Someya et al., “Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes”, Proceedings of the National Academy of Sciences, vol. 102, no. 35, pp. 12321-12325, August 2005;

[117] D. Da He et al., “An integrated organic circuit array for flexible large-area temperature sensing”, IEEE International Solid-State Circuits Conference (ISSCC), February 2010, San Francisco, California, 2010, pp. 142-144.

[118] R. Agarwal et al., “An Organic Temperature Sensor Based on Asymmetric Metal Insulator Semiconductor Capacitor With Electrically Tunable Sensing Area”, IEEE Sensors Letters, vol. 2, no. 1, March 2018.

[119] F. Molina-Lopez et al., “Large-area compatible fabrication and encapsulation of inkjet-printed humidity sensors on flexible foils with integrated thermal compensation”, Journal of Micromechanics and Microengineering, vol. 23, pp. 1-11, January 2013.

[120] W. P. Shih et al., “Flexible Temperature Sensor Array Based on a Graphite-Polydimethylsiloxane Composite” Sensors, vol. 10, no. 4, pp. 3597-3610, April 2010.

[121] H. Al-Mumen et al., “Design, fabrication, and characterization of graphene thermistor”, 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, Suzhou, China, April 2013.

[122] T. Vuorinen et al., “Inkjet-Printed Graphene/PEDOT:PSS Temperature Sensors on a Skin-Conformable Polyurethane Substrate”, Scientific Reports, vol. 6, article number 35289, pp. 1-8, October 2016.

[123] G. Gielen, et al, “Time-Based Sensor Interface Circuits in CMOS and Carbon Nanotube Technologies”, IEEE TCAS I, vol. 63, pp. 557-586, Mar. 2016.

[124] J. Van Rethy, et al, “Performance Analysis of Energy-Efficient BBPLL-Based Sensor-to-Digital Converters”, IEEE TCAS I, vol. 60, pp. 2130-2138, Aug. 2013.

[125] R. Rotzoll, et al., “13.56 MHz organic transistor based rectifier circuits for RFID tags,” in Proc. Mater. Res. Soc. Symp., 2005, I11.6.1-6.

[126] J. P. Curty et al., “Design and Optimization of Passive UHF RFID Systems”, New York, USA, Springer, 2007.

[127] M. Fattori, et al., “Flexible pressure and proximity sensor surfaces manufactured with organic materials”, 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Vieste, Italy, June 2017.

[128] T. Someya, et al., “A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications,” Proc. Nat. Acad. Sci. USA, vol. 101, pp. 9966–9970, July 2004.

[129] G. Schwartz, et al., “Flexible polymer transistors with high pressure sensitivity for application in electronic skin and health monitoring”, Nature Communications 4, 2013.

[130] T. Yokota, et al., “Sheet-Type Flexible Organic Active Matrix Amplifier System Using Pseudo-CMOS Circuits with Floating-Gate Structure”. IEEE Trans. Electron Devices, vol. 59, no.12, pp. 3434-3440, December 2012.

[131] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause et al, “An All-Printed Ferroelectric Active Matric Sensor Network Based on Only Five Functional Materials Forming a Touchless Control Interface,” Advanced Materials, vol. 23, no. 18, pp. 2069-2074, May 2011.

[132] H. Gold et al., “Flexible Single-Substrate Integrated Active-Matrix Pyroelectric Sensor” Physica Status Solidi, Rapid Research Letters (RRL), July 2019.

[133] V. J. Lumelsky, “Sensitive skin”, IEEE Sensor Journal, vol.1, no. 1, pp. 41- 51, June 2001.

[134] K.I. Nomura et al., “A flexible proximity sensor formed by duplex screen/screen-offset printing and its application to non-contact detection of human breathing”, Scientific Reports, vol. 6, pp. 1-12, January 2016.

[135] H. S. Han et al., “A Highly Sensitive Dual Mode Tactile and Proximity Sensor Using Carbon Microcoils for Robotic Applications”, 2016 IEEE International Conference on Robotics and Automation (ICRA), pp. 97-102, Stockholm, Sweden, May 2016.

[136] G. Scheipl et al., “Fabrication, characterization and modeling of PVDF based organic IR-sensors for human body recognition”, IEEE SENSORS 2009 Conference, pp. 1252-1255, Christchurch, New Zealand, October 2009.

[137] Y. C. Hu et al., “Flexible Proximity Key-Panel”, 8th Annual IEEE International Conference on Nano/Micro Engineered and Molecular Systems, pp. 606-609, Suzhou, China, April 2013.

[138] N. Fujitsuka et al., “Monolithic Pyroelectric Infrared Image Sensor Using PVDF Thin Film”, International Conference on Solid-state Sensors and Actuators, pp. 1237-1240, Chicago, USA, June 1997.

[139] T. David Binnie et al., “An Integrated 16 × 16 PVDF Pyroelectric Sensor Array”, IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, vol. 47, no. 6, pp. 1413-1420, November 2000.

[140] S. A. Pullano et al., “A Pyroelectric Sensor for System-on-a-Chip”, 40th Annual Northeast Bioengineering Conference (NEBEC), Boston, MA, USA, April 2014.

[141] X. Chen et al., “A Flexible Piezoelectric-Pyroelectric Hybrid Nanogenerator Based on P(VDF-TrFE) Nanowire Array”, IEEE Transactions on Nanotechnology, vol. 15, no. 2, pp. 295-302, March 2016.

[142] K. Foroutani et al., “Preparation of conductive flexible films by in situ deposition of Polythiophene nanoparticles on polyethylene naphthalate”, Materials Science in Semiconductor Processing, vol. 18, no. 1, pp. 6-14, February 2014.

[143] S. G. Prasad et al., “Structural and Optical Investigations of Radiation Damage in Transparent PET Polymer Films”, International Journal of Spectroscopy, pp. 1-7, March 2011.

[144] W. L. Yu et al., “The Experiment Study on Infrared Radiation Spectrum of Human Body”, Proceedings of the IEEE-EMBS International Conference on Biomedical and Health Informatics (BHI 2012), pp. 752-754, Hong Kong and China, January 2012.

[145] A. Hossain et al., “Pyroelectric Detectors and Their Applications”, IEEE Transactions on Industry Applications, vol. 27, no. 5, pp. 824-829, September 1991.

[146] D. Hughes et al., “A Robotic Skin for Collision Avoidance and Affective Touch Recognition”, IEEE Robotics and Automation Letters, vol. 3, no. 3, pp. 1386-1393, July 2018.

[147] F. Xia et al., “Tri-Mode Capacitive Proximity Detection Towards Improved Safety in Industrial Robotics”, IEEE Sensors Journal, vol. 18, no. 12, pp. 5058-5066, June 2018.

[148] H. Hasegawa et al., “Net-Structure Proximity Sensor: High-Speed and Free-Form Sensor With Analog Computing Circuit”, IEEE/ASME Transactions on Mechatronics, vol. 20, no. 6, pp. 3232-3241, December 2015.

[149] H.J. Weller et al., “Low-noise charge sensitive readout for pyroelectric sensor arrays using PVDF thin film”, Sensors and Actuators A Physical, vol. 85, pp. 267-274, February 2000.

[150] M. Kaltenbrunner, et al., “An ultra-lightweight design for imperceptible plastic electronics”, Nature 499, pp. 458-463, 2013.

[151] Society of Automotive Engineering (SAE) J211-1, “Instrumentation for Impact Test, Part 1, Electronic Instrumentation”. March 1995.

[152] K. Digges et al., “Measurements of vehicle compatibility in front-to-side crashes”, The National Crash Analysis Center, The George Washington University, USA, 2001.

[153] Y. Kitagawa et al., “Evaluation of Vehicle Body Stiffness and Strength for Car to Car Compatibility” Proceeding of 2001 SAE International Body Engineering Conference & Exposition, October 2001.

[154] J. Hillenbrand et al., "Piezoelectricity in cellular electret films," in IEEE Transactions on Dielectrics and Electrical Insulation, vol. 7, no. 4, pp. 537-542, August 2000.

[155] J. Fijn, “Design of flexible sensors exploiting organic and Si IC technologies”, Pd Eng Thesis, Eindhoven University of Technology, Eindhoven, Netherlands, 2019.

[156] P. J. A. Harpe et al., “A 3nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5fJ/conv-step ADC,” 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, pp. 382–384, 2015.

[157] W. Sansen, “Distortion in elementary transistor circuits,” IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 46, no. 3, pp. 315–325, March 1999.

List of Publications

1 M. Fattori, E. Cantatore, G. Pauer, T. Agostinelli, H. Gold, “A fast printed pressure and impact force sensing surface”, 9th International Exhibition and Conference for the Printed Electronics Industry (LOPEC 2017), Munich, Germany, March 2017.

2 M. Fattori, E. Cantatore, G. Pauer, T. Agostinelli, B. Stadlober, H. Gold, “Flexible pressure and proximity sensor surfaces manufactured with organic materials”, 7th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Vieste, Italy, June 2017.

3 M. Fattori, S. Abdinia, G. Pauer, B. Stadlober, H. Gold, J. Socratous, F.Torricelli, E. Cantatore, “Organic Pressure-Sensing Surfaces Fabricated by Lamination of Flexible Substrates”, IEEE Transactions on Components, Packaging and Manufacturing Technology, March 2018.

4 M. Fattori, J. A. Fijn, E. Cantatore, M. Charbonneau, “A fast printed pressure and impact force sensing surface”, 10th International Exhibition and Conference for the Printed Electronics Industry (LOPEC 2018), Munich, Germany, March 2018.

5 V. Pecunia, M. Fattori, S. Abdinia, H. Sirringhaus, E. Cantatore,”Organic and amorphous-metal-oxide flexible analogue electronics”, Series: Elements in Flexible and Large-Area Electronics, Cambridge University Press, Cambridge, United Kingdom, May 2018.

6 M. Fattori, J. A. Fijn, E. Cantatore, “Large-Area Organic Pressure Sensing Surfaces Manufactured on Flexible Substrates”, PRORISC 2018 conference, Enschede, The Netherlands, June 2018.

7 M.Charbonneau, D.Locatelli, S.Lombard, C. Serbutoviez, L. Tournon, F.Torricelli, S.Abdinia, E.Cantatore, M. Fattori, ”A Large-Area Gravure Printed Process for P-type Organic Thin-Film Transistors on Plastic Substrates” 2018 48th European Solid-State Device Research Conference (ESSDERC), Dresden, Germany, September 2018.

8 M. Fattori, J.A. Fijn, L. Hu, E. Cantatore, F. Torricelli, M. Charbonneau, “Circuit Design and Design Automation for Printed Electronics”, 2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), Florence, Italy, March 2019.

9 M. Fattori, J. Fijn, P. Harpe, M. Charbonneau, S. Lombard, K. Romanjek, D. Locatelli, L. Tournon, C. Laugier, E. Cantatore, “A gravure-printed organic TFT technology for active-matrix addressing applications”, IEEE Electron Device Letters, vol. 40, no. 10, pp. 1682-1685, October 2019.

10 M. Fattori, J. Fijn, C., A. Mendes da Costa Junior, M. Charbonneau, E. Cantatore “Printed Organic Smart Temperature Sensor for Food Monitoring Applications achieving 270 mK_{RMS} Resolution”, in preparation.

11 M. Fattori, S. Cardarelli, J. Fijn, M. Charbonneau, H. Gold, J. Socratous, E. Cantatore “Fully-Printed Organic Sensing Surface for IR Proximity Detection Applications”, in preparation.

12 J. Fijn, M. Fattori, E. Genco, M. Charbonneau, H. Gold, J. Socratous, E. Cantatore “A Pressure Sensor Active Matrix based on Printed Organic - Si Hybrid Electronics”, in preparation.

Summary

Circuit Design for Low-Cost Smart Sensing Applications Based on Printed Flexible Electronics

The development of electronics is still led nowadays by the Moore’s law trend, which makes possible increasingly more dense integrated circuits, and enables ever improved functionality while keeping costs basically unchanged. Moore’s developments, however, are not the only propulsive force in the development of electronics. “More than Moore (MtM)” trends aim to integrate in a system functional diversification based on the simultaneous use of heterogeneous technologies that do not scale in accordance with Moore’s law, in order to enable novel applications. In this framework, for instance, large-area technologies can expand the application of electronics beyond miniature integrated circuits, to provide large-area interfaces, like displays. Interestingly, large-area electronics can also be manufactured on flexible substrates to make possible unprecedented applications like foldable displays, or flexible sensing surfaces, or biomedical instrumentation that can adapt to the shape of the body. Printing electronics on large foils is also possible, adding to the attractiveness of flexibility the advantage of ultra-low production costs and enormous potential throughput.

Despite the recent advancements of printed electronic technologies, their use in commercial products remains up to date very limited. Technology challenges such as limited yield, large transistor variability, and poor electrical performance, still prevent printed systems on foil from commercial exploitation. However, several of these limitations can be tackled and mitigated at the circuit design level. In this perspective, the main research question addressed in this work is to create new design methodologies and circuit topologies specifically suited for printed organic technologies, which are able to improve the robustness of the printed circuits, enabling their use to enable innovative market applications.

In Chapter 2 the printed organic TFT (OTFT) technology used in this work is introduced in a bottom-up fashion, starting from the printing capabilities and reaching the device fabrication process. The OTFT electrical characterizations and the technology yield analysis are also reported.

Chapter 3 discusses the development of a Process Design Kit (PDK) for the printed organic technology. First, the OTFT models (static, dynamic and noise) are derived. Next, the methodology developed to define the technology Design Rule Manual (DRM) is introduced. The integration of the PDK in a commercial Computer Aided Design (CAD) framework is also discussed.

Chapter 4 focuses on the design and characterization of multi-stage line drivers for matrix addressing applications manufactured with the gravure-printed unipolar organic transistors technology. Different transistor-level implementations for the single delay stage have been proposed and the circuit performance is compared by means of simulations. Three typologies of 8-stage organic line drivers have been developed exploiting the proposed delay stages. Measurement results have been further used to provide insight in the yield performance of each line driver architecture, and to select the most robust circuit implementation in the given OTFT technology.

Chapter 5 presents the design and evaluation of a smart temperature sensor integrated in a passive RFID tag, manufactured with a unipolar printed organic transistor technology. The proposed system-on-foil enables the fabrication of inexpensive disposable electronic devices for innovative applications in the cold chain temperature monitoring of food and pharmaceutical products. In order to achieve this, printed resistive temperature sensors have been selected for the temperature sensing, and a time-based frontend interface has been exploited to perform the analog-to-digital signal conversion. The RFID tag is further capable of transmitting the digitalized signal to a reader, via an RF communication link at a frequency of 13.56 MHz. In addition, in order to develop a stand-alone system–on-foil, the tag has been equipped with a harvesting circuit for wireless power transfer.

Chapter 6 deals with the design of a fully-printed large-area proximity sensing surface fabricated with organic materials. The core of the sensing surface is a 5x10 active sensor matrix obtained by lamination of printed organic pyroelectric sensors on foil (frontplane) with printed organic frontend electronics (backplane). The frontend electronics is used here to provide sensor signal amplification and unambiguous pixel addressing in order to maximize the SNR and reduce the pixel crosstalk. The proposed system-on-foil could be exploited to improve the safety in environments where humans and robots are cooperating or to develop artificial electronic skin for novel human-machine interaction applications.

Chapter 7 presents the design and evaluation of a system suitable for pressure sensing applications, which integrates Si-IC electronics (based on Si-65 nm technology) with a system on foil manufactured with printed organic materials. The use of printed organic technologies enables low-cost large-area distributed pressure sensing capability, while the Si-IC electronics performs readout, sensor aggregation and signal digitalization, using a minimum number of interconnections and allowing a compact footprint. The core of the flexible system is a 5x3 active matrix of printed organic pressure-sensitive sensors on foil (frontplane), laminated with a second flexible substrate containing printed frontend electronics (backplane). The pixel frontend electronics make use of a transconductor to perform high-speed sensor aggregation and the voltage-to-current conversion for the direct interconnection with the Si-IC electronics. The proposed system-on-foil is designed to achieve large dynamic range in force/pressure measurements together with a fast response, in order to further extend the versatility of the solution. The availability of low-cost large-area pressure sensing devices which can be directly interfaced with conventional Si-based platforms is expected to be the key enabler for innovative applications in the markets of domestic ambient monitoring, automotive and smart building, to give some examples.

Finally, conclusions are drawn in Chapter 8: new design methodologies and circuit solutions have been proposed and demonstrated in this work to tackle the two major challenges in circuit design with printed organic technologies: the large parameter variability and the limited yield. The main idea relies on the use of circuit techniques which systematically desensitize the circuit performance from the OTFT parameter variations. Jointly, the circuit implementation aims also to minimize the number of required devices in order to maximize the overall circuit and system yield. These techniques have been further used to demonstrate robust systems-on-foil for four innovative smart sensing applications which benefit from the mechanical flexibility and large area-coverage achieved at a low price by the printed electronics approach.

Acknowledgements

…And finally I have arrived to the most important part of this dissertation. This section is dedicated to all the people who supported me during these 4 years: without your help I would not have made this far.

My PhD experience started in February 2015, when Arthur and Marion invited me for an interview. At that time I knew very little about microelectronics (I have to say that the situation has not improved much after 4 years) and thus I was very surprised to hear that they wanted me to join the MSM group for a PhD position. Therefore, I would like to thank Arthur and Marion for giving me this unique opportunity.

A very big thank you to my promoter Eugenio, who has guided me during this whole period. He taught me a lot about research, microelectronics and of course English grammar (you know the Italians…). He even tried with the Dutch language but it did not really work out (again, you know the Italians...). At this point I should also mention that during the period of my PhD which was characterized by a large number of setbacks, Eugenio has always provided me his full support, motivating me and convincing me that at some point the desired results will arrive. And indeed, he was right. I would also like to thank Pieter for all the interesting discussions, and for his valuable support during the writing of this manuscript.

A special thank goes to my colleagues "The Nest Hunters" who have made the office an amazing environment to work. I will never forget our trips to Berlin and Copenhagen, the dinners together, the Carnival evenings, the ProRISC conference 2018, the bike trips, etc… The first person in this list that I would like to thank is Camilo (also known as the Boss[4]). I remember, he invited me to celebrate his birthday on the very first day of my PhD. Years later I reminded him about that event, how our friendship started with the cake I ate at his birthday… However, instead of being happy he was upset, still wondering why I hate his cake (yes I had some problems to pronounce the h, you know the Italians…). I can't say I was very happy when he graduated and left the group, because afterwards Eugenio decided to reserve for me Camilo's early morning meeting slot. Then there is Carmine, my first Italian deskmate famous for living in a different time zone and for his "Oh allora". He knew everything about girls, microelectronics and football. I will never forget the time when we were playing football at the sportcentrum and Carmine kept on screaming in Italian for an hour "PASSA! PASSA! OH OH AL CENTRO!!!" to the poor Maoqiang who never really understood what to do. Carmine has been also the companion of endless but extremely valuable discussions in the office. Nevertheless, it seems that these discussions and the low pitch voice of Carmine, were not really appreciated by the rest of the people of the room 7.085. The next on the list is Lamberto[5] (one of those who was not really happy with the chit chatting in Italian). I will use this opportunity to apologize to him for not being able to correctly pronounce his surname "Duipmans" (you know the Italians...), in 4 years. And

---

[4] Title earned in 2015 while rescheduling with authority his meeting with Eugenio

[5] Some dutch people find their name cuter in Italian.

maybe I should also apologize for all pranks he has been a victim of (one day he even found his bike about to be sold on Marktplaats). I would like to thank also Debby (Mitra) for reminding me every single day of my PhD that organic transistors and my circuits won't work. Despite this, and despite his accent/way of speaking which took me 6 months to decrypt and yet I have not fully understood, Debby has been an important person for me in the office. Thank you for all the Cadence/Matlab related problems you helped me fixing and all the discussions we had on circuits based on p-MOS transistor only[6]. A special mention goes also to Carlos Antonio Mendes Da Costa Junior (or in short Carlos+Junior= Carlinho). Brazilian of origin, with Italian roots and a German attitude of working, a real nightmare for me to work with ☺. Carlinho is also one of those who did not like Italians conversing in the room, although at the very end he got used to that (or he simply gave up). Another very important member of the group that I would like to thank is Martin (for the record known as "Petite velo" or "French *****"). He taught us a lot about the French language and more specifically the way you are supposed to speak[7]. Among other things with Martin I shared a passion for vinyl records, a large number of wine bottles and the common interest for Brooklyn Nine-Nine. All in all, he is a nice guy even though he is French! After Martin, I would like to thank Debby 2 for daily enriching the atmosphere of the office with his amazing stories through all the 4 years. I truly believe that the legend of the Bangladeshi Tiger will continue to fascinate for centuries…The last members of the Nest Hunters group I would like to thank are in order Giustino[5], Gonenc, Ashwin, James, Piyush and Genchino. With Giustino, I have been working for about two years of my PhD. During this period we both worked hard to ensure a successful outcome of the ATLASS project, and I am glad he was my team mate in this adventure. Cooperating together has not always been easy (We zijn allebei een beetje koppig) but it has surely been a lot of fun. James shared our office for about a year and without any doubt he is the best Chinese officemate I have ever had[8]. Even though James is an excellent photographer, he lacks some skills using the self-timer of the camera[9]. A special thank goes to Piyush (and Giustino) for motivating me to do some sports (Running, cycling, squashing, playing football…). Finally I want to thank Genchino for his great contribution to my dissertation and above all for the "caciocavallo impiccato" we designed and successfully taped-out last week.

My appreciation also goes to the rest of the members of the IC group, starting from the current head Peter Baltus. A special thanks to Margot and Rainier for their prompt support on technical and non-technical matters.

Among the people involved in my PhD project, I would like to express my deep gratitude to Micael and its team at CEA for their hard work and great effort in the development of the transistor technology and to Herbert for his valuable support in the technical discussions. I

---

[6] The circuit were re-drawn with nMOS transistors for pity on Debby.

[7] For a demonstration feel free to contact Debby.

[8] And the only one ☺

[9] #Camilo's farewell dinner

would also like to thank Gernot, Lars and Josephine for their contribution in the development of the ATLASS demonstrators.

Beside the working environment, I also want to thank all the people who have supported me during these years. I would like to start with Daniela my former housemate. Thank you for revealing my true name Marione, for teaching me that Rieti belongs to Abruzzo and for always encouraging me with sentences like “Marione you look pale, I have my doubts you are going to make it to the end of the PhD”. My appreciation goes also to Bibi, Teresa, Ema and Luca for their active part in all the parties at Havensingel 70. I also want to mention Sergio my last housemate at Havensingel. Thank you for considering me, your best Italian housemate you have ever had[8]!

E poi ci sono gli abitanti del regno di Eindhoven... Quelli del ponte di qua, a cominciare da Sua maestà, re Giacomo I da Conegliano, e Sua Altezza regina, Claudia Calabrona. Un abbraccio a entrambi per aver mantenuto la PAX a Eindhoven con quei terroni del ponte di là e per aver introdotto la cavallina ad UNO. Giacomi grazie anche per le casse di vino e per il costante impegno nel perculare Basilio e Chicco. Nel dubbio sempre forza Juve e CR7. Ci sono poi i due ribelli del ponte di la, Basilio[10] (for the record also known as Bafuggi) e Viviana anche detta Scrocchiarella. Basilio è un numero 10, uno di quelli della leva calcistica del ‘68: fan sfegatato della Lazio (ha l’aquilotto pure sul vetro del pandino), non perde un derby Lazio-Roma dal 1953, uno cosi ottimista che Tonino Guerra gli spicciava casa a confronto. Ovviamente se scherza Basix! Basilio è della Magica, uno che cerca l’avventura, leale, altruista insomma un amico vero. Uno che se lo chiami alle 23:00 di sabato sera per chiedergli un passaggio fino all’aereoporto di Amsterdam per il giorno dopo alle 6:00 ti dice: “Mortacci tua ******!!! ******!!! ****! Ci vediamo domani!”. Viviana invece è una con cui NON puoi giocare ad UNO. Comunque vada, con una cavallina lei ti appiopperà un +2+2+2+2 seguito da un paio di +4 [11]. Anche quando sei li con una carta in mano che assapori la vittoria (sempre che tu abbia prima detto “UNO!” altrimenti lei ti ricorderà di prendere due carte addizionali in amicizia) lei ha la carta per mischiare il mazzo.. Grazie Viviana, dopo 4 anni ancora non vinco una partita... Tra quelli del ponte di qua c’è anche la coppia Gabriele-Mandy. Gabriele, meglio conosciuto come Maestro, è calabrese, parla alla stessa velocità di Carmine e viene dal piano 9 del FLUX. Ricordo con piacere le sue sortite dal piano 8 e le pistolettate. Maestro, ma che bella l’uscita in bici di 140 km in Belgio che quasi sembrava la coppa Cobram! Nei primi 10 km, tutti in salita Gabriele andava una spada[12]... Poi la crisi di fame, a 80 km dal traguardo il Maestro era sul punto di chiamare un’ambulanza. Poi il pranzo con la lasagna e la svolta fino a casa. Che faticaccia! Daje Maestro, torna presto alla TUe! Mandy instead (known also as Mendina, Mendozzi or Mendy according to Chicco) is the Italian of the couple. Always synchronized with the Italian Time Zone[13] (UTC-2), almost proficient in Italian but with very little understanding of my jokes. I thank you both very much for the amazing time

---

[10] Dal greco βασιλευς(basileus) che vuol dire "re" (cosi finalmente la smetti co sta storia)

[11] Allowed only in the Italian rules.

[12] Tipycal expression from Abruzzo which means going like a charm

[13] The same time zone of Carmine

spent together, for the nice dinners at your place and for the “dutch experience”[14] at your birthday party. Maestro non è che mo senti autorizzato a fa u billu, vedi de statte carmo... Tra le new entry del gruppo di quelli del ponte di qua c’è anche Giogina (o Gufetta depending on the situation). A lei va un grazie di cuore per non aver fatto nulla... e un grazie anche per il prestito del letto che ho già acquisito per usucapione. Giorgina è una grade campionessa (mancata) di squash che ha smesso di sfidarmi non appena ha perso la prima partita (il galletto ha abbassato la cresta)[15]. In suo favore però, devo anche menzionare un paio di outstanding victories..Va be non fa la matta, non te monta la testa mo.. Daje Gufetta, rimani a Eindhoven che qua se sta meglio, che ce fai co Rometta tua! Altra recente new entry del gruppo è Sergigno (o semplicemente Sergio), pseudonimo di Edoardo Paoles. Reatino d’origine, a 25 anni ha già vissuto in Bracciano City[16], Germania, Stati Uniti e Olanda, un giramunnu[17] come direbbe Gufetta. Un grazie va anche a te Sergigno per tutti i lavoretti impossibili che trovi solo tu: biciclette con malattie rare tipo 1 su 1000000, installazione di lavastoviglie non su misura e in posti scomodi, etc... Quando vieni a casa cosi proviamo la bottiglia di Whisky che mi hai regalato? Mi sa che se non ti sbrighi la trovi vuota. Infine, tra gli abitanti del regno del ponte di qua vorrei anche ringraziare Michele, Irene, Federico e Laura. Irene, grazie per i mille tips sulla Grecia, ottima destinazione. Certo che se fosse stato per Michele saremmo finiti a Canosa a piantare patate! Oh Cumpa, si tu Michè, la vuoi smettere di risponde “No No!” e fa battute senza senso quando ti chiedo qualcosa? Dai su tanto non ti esce bene! Una menzione speciale va anche a Federico l’uomo con i tappi per le orecchie piu cari del mondo. Che dici ce la fai a passare a trovarmi a casa visto che abitiamo a 70 metri in linea d’aria l’uno dall’altro? Laura, mi raccomando pensaci tu... PS: il fragolino che mi hai regalato a Maggio era ottimo, altro che i cicciolі di Federico… The last members of the Eindhoven’s group I would like to thank are Jon, Rongling and Felix. Thank you guys for the amazing evenings spent together, the board games, the super delicious duck cooked by Rongling (that I and Chicco ate almost entirely alone), Felix’s concert and the bike trips (Jon also participated to the Cobram Cup).

Un grazie sincere va anche a tutti gli amici dell’Erasmus, Gigia, Anna, Marco Blanca, Veronica, Stefano, Pippo, Lorenzo, Valerio e Liberato che hanno reso quell’esperienza fantastica gettando le basi per un Eindhoven 2.0.

Il mio grazie di cuore va ai miei amici di Campoloniano con i quali sono cresciuto e che, per una ragione o per un’altra, sono adesso sparsi in tutta Europa. Grazie a tutti voi per aver condiviso con me mille avventure (vacanze ad Albadriatica e in Sardegna, cene con fiumi di vino a Biscottino, tendate a San Vittorino e Antrodoco (l’ultima quasi mortale), pizzate matte a casa di Riccio, Kebab con 3X extra piccante alle 24:00, corse alla fontanella (dopo il Kebab), vacanze in bici, concerti, serate passate a vedere le stelle cadenti, campi estivi, Via Crucis e tanto altro...). Grazie Giandomenico, Daniele, Riccardo, Martina, Betta, Federica T, Federica

---

[14] It consists of starting the party eating the dessert

[15] Typical italian expression which literally means: “the rooster has lowered his crest”

[16] Metropolis located in the middle of Italy

[17] Globe throttle

F, Beatrice, Marco Zanna, Alessandro, Livio, Andrea, Riccardino, Eleonora, Massimello, Andrian, Giada, Sara, Federica C, Antonio e ovviamente Aldo. Spero di tornare presto e festeggiare tutti insieme come ai vecchi tempi. PS: Giandomenico (conosciuto ad Eindhoven anche come Pecorino o semplicemente Pecos) ormai trasferisciti ad Eindhoven tanto stai sempre qua... Porta anche un po' di quei guanti anti taglio fighi. PS2: Daniele (alias Stupidillu) considera che quando leggerai questo commento sarà troppo tardi, ti staremmo già portando alle montagne russe. PS3: Riccardo o Riccio o Caciotta (valido solo ad Eindhoven), non ride troppo che a te, te tocca la barca... PS4: Aldo, al momento della scrittura della tesi non ne sono ancora sicuro, ma credo tu ce l'abbia fatta a laurearti prima di me. Grande!!!

Visto che ormai siamo arrivati a Rieti vorrei anche ringraziare i miei professori dell'Istituto Tecnico Industriale C. Rosatelli, ed in particolare: Sergio Pantaloni, Gabriella Gallo, Agostino (Ugo) Giovannelli, Alessandro Pettinari e Annamaria Renzi. Un affettuoso abbraccio va anche ai miei ex compagni di classe Marco, Ardit e Andrian.

Ancora un po' di ringraziamenti sparsi: un grazie di cuore va a Tiziano, fedele amico da tanti anni ormai. Di Italiano lui però ne parla poco... d'altronde viene da Mozza! Grazie Simacchio per non ricordarti mai di me e dei tuoi coinquilini dell'Aquila ma sempre e solo del fratello buono. Un grazie al mitico Antonio Astorino, compagno insieme a Chicco di mille battaglie durante i 4 anni passati insieme all'Università degli Studi dell'Aquila. Un abbraccio a Chiara per le chiacchierate infinite ed a volte anche senza senso. Grazie Irinel per il tuo supporto nonstante la lontananza. Ecco, magari se ti ricordassi del fuso orario che ci divide mi eviteresti i messaggi e le chiamate alle 3 di notte ☺! Ti aspetto presto in Europa... Daje!

Sono quasi alla fine dei ringraziamenti prometto..

Il Grazie piu grande di tutti va poi ai miei genitori, Agnese e Pino. Grazie per avermi sempre appoggiato incodizionatamente e sostenuto in tutte le mie scelte, nonostante la distanza e nonostante tutto. Questo traguardo è sopratutto merito vostro. Mamma, ora però gna che te impari un po de inglese eh, mica te posso sempre tradurre io! Caro Pino, per te invece è arrivata la fama internazionale, da quando i nostri incontri di Wrestling sono stati trasmessi in tutto il mondo (Ops...). In fondo, non sei altro che un piccolo Rey Mysterio senza maschera. Pronto per il prossimo match?

Della famiglia fa parte anche Stefano, il fratello buono. Grazie per le mille passioni che mi hai trasmesso fin da quando eravamo piccoli. Per arrivare fin qui, ho seguito in parte anche il tuo esempio. Questo non significa che durante la prossima uscita in bici ti lascerò vincere. Lo sai che la musica è cambiata ormai da un pezzo, sei vecchio! Un ringraziamento speciale va anche ad Alessandra con i migliori auguri (dallo Zio d'Olanda[18]) per Aurora, la prossima new entry in famiglia! Un abbraccio va anche a zia Rita, Antonio, zio Daniele, zia Anna e ovviamente a nonna Anita! I would like also to thank the other part of the family which is located in Belgium. Lut, Guy and Sam, thank you for the super nice time we spent together (and more is yet to come), for me it really feels like being at home.

---

[18] Che secondo il fratello buono ha gli stessi soldi dello zio d'America, ma si trova solo a 2 ore di volo da Rieti.

The last person on the list that I would like to thank is my girlfriend Anke. I can’t thank her enough for being next to me, side by side in the last years. The PhD period hasn’t been easy for us. The distance between us, together with the misbalance of the workload which resulted in much less time to spend together. In spite of all these, we managed to make it work. Since few months we are finally living together, in Eindhoven. I know moving to the Netherlands has been a very big step for you, and not free from challenges. I am deeply grateful to you for taking this step in the relationship. Thanks for being there, I am sure that even during these difficult times we had created some beautiful memories that we can look back together.

…Chicco state carmooo!.. Ah, mo non me so dimenticato de te.. Abbassa a cresta! Sono più di 10 anni ormai che percorro la stessa strada con Simone Cardarelli (in arte Chicco). Ci siamo conosciuti durante la triennale a L’Aquila, poi l’Erasmus ad Eindhoven, Sint Jorislaan e infine il PhD alla TUe. Chicco è il Soggetto #1, stravagante, a tratti smemorato e sconclusionato ma anche super creativo, skillato (ha anche imparato il Reatino)... quasi un genio direi... se non fosse per la storia di quella serranda, le mille e una volta che Chicco prima di partire con la bici la lega con la catena e la rislega di nuovo, per tutte le volte che mi domanda la stessa cosa ogni giorno della settimana, etc... Ma Chicco è cosi, lo si sà, il compagno di mille avventure: dalle corse in bicicletta sull’autostrada, agli arrosticini con la genziana fatta in casa, alle partite a squash, ai concerti, fino alle corse da pazzi senza senso. Chicco grazie di tutto. Raccolgo il tuo invito a sposarci. Facciamo a Luglio 2020? Tanto lo so che te lo dimenticherai sicuramente, perciò Anke puoi stare tranquilla ☺!

Curriculum Vitae

Marco Fattori was born on 11-05-1990 in Rieti, Italy. After finishing the technical high school in 2009 at C. Rosatelli in Rieti, Italy, he studied electronic engineering at Università degli Studi dell'Aquila, Italy. In 2014 he received the M.Sc degree cum laude in electronic engineering. From March 2015 he started a Ph.D. project at in the Integrated Circuits group, department of Electrical Engineering, Eindhoven University of Technology (TUE), Eindhoven, The Netherlands of which the results are presented in this dissertation.