Expanding the toolbox of atomic scale processing

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PROEFSCHRIFT

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General Introduction

This introductory chapter provides an overview of the current trends in data generation that is ushering in a global transition to "the data economy." The chapter then introduces the concept of artificial intelligence (AI) and briefly discusses where AI is currently being or will be used to tackle the upcoming explosion in data generation. The chapter then outlines how AI entails new approaches in data processing and storage that cannot be handled by current computational systems. This leads to the need for novel device technologies consisting of nanoscale features and three-dimensional (3D) architectures, as shown by the images above. The images consist of 3D trench-shaped and nano-sized structures that illustrate two contrasting scenarios. For the image on the left,[1] nanoscale films of a conductive material (platinum) are present only at the vertical trench sidewalls while for the image on the right,[2] nanoscale films of an insulating material (silicon nitride) are present only at the horizontal top and bottom regions of the trenches. Obtaining films of such materials with such small thicknesses only at specific regions of small 3D objects summarizes most of the challenges that this dissertation seeks to address. The chapter then introduces plasma-enhanced atomic scale processing techniques, which form the core aspect of this dissertation, and how materials processing using these techniques can be used for addressing the aforementioned challenges. The chapter concludes by providing a brief overview on the rest of this dissertation. This chapter is followed by a more in-depth chapter that explains the devices needed for the AI era and where atomic scale processing is or will be used to fabricate those devices. Together, these two chapters should provide a good platform in facilitating the reader to comprehend the motivation behind and results of this dissertation.

"Data are to this century what oil was to the last one: a driver of growth and change. If data are the new oil, chips are the internal-combustion engines that turn them into something useful." – *The Economist*.[3,4]

1.1 The data economy and the advent of artificial intelligence

The world is currently on course for undergoing a transition to the so-called data economy.[3,4] It is estimated that about 33 zettabytes (i.e., 33×10^{21} bytes) of data have been generated globally in the year 2018 (see Figure 1); or about 12 gigabytes per day for every single person on the planet.[5] Consumers are currently generating data by using devices such as desktop computers or portable smartphones to, e.g., interact with friends and family through social media, order goods and services online, track personal activities in real-time even while asleep, etc. Corporations across the globe are leveraging this data to improve productivity, improve client experience and customer support, access new markets and derive new sources of competitive advantage.[5]

Data generation and their subsequent analytics has ushered in the creation of new and disruptive business models, services, politics, etc. For instance, it is remarkable to note that the world's largest ride-sharing or taxi cab service provider owns no vehicles (Uber) while the world's largest lodging or accommodation service provider owns no real estate (Airbnb).[6] What such businesses own and operate on is basically a large amount of data on the demand and supply side for their respective services; e.g., data on passengers and drivers for personal transportation, and data on guests and hosts for personal accommodation in the respective cases of Uber and Airbnb.[3] Besides the staggering quantity of data generated, the type of data generated has also become more diverse. Data are no longer simply piles of digital information, such as databases of the name, age, address, etc. They also consist of real-time flows of unstructured data, such as the videos and photos generated by users of social media networks, the stream of data from numerous sensors of an aircraft, etc.[3] A good proportion of the economy today depends on data and this dependence will only increase down the road with the advent of 5G network infrastructures and the Internet of Things (IoT).[7,8] The IoT has been predicted to connect over 200 billion smart data-generating objects to the internet by 2020,[8] which is expected to contribute to the creation of a massive 175 zettabytes of data by 2025 (see Figure 1).[5] From augmented/virtual reality (AR/VR) headsets to autonomous cars, agricultural drones and intelligent robots, a wide variety of applications are expected to become new sources of an ever-increasing real-time flow of data.[8,9] Many of these wearable and mobile applications will have limited resources in terms of available device area (form-factor) and power source (e.g., battery capacity). As a result, there is currently a need for extracting relevant information from this abundance of data in a fast, accurate and energy-efficient manner.
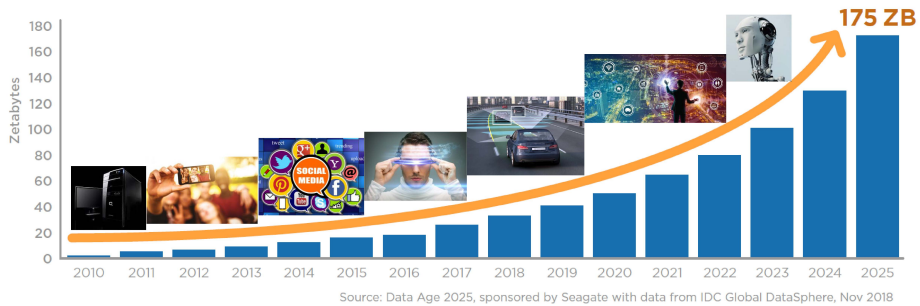
Figure 1. Measured and estimated quantities of global data generation on an annual basis (in zettabytes or 10^{21} bytes) from the year 2010 to 2025. The inset images provide an approximate timeline of the various sources of data creation ranging from (left to right) standalone desktop computers, portable smartphone devices, social media activity, augmented/virtual reality (AR/VR) applications, autonomous cars, the Internet of Things (IoT) and intelligent robots.[3,5,7,8,10–14]

Artificial intelligence (AI) has emerged as a potential technology for addressing the onset of the data economy. AI is a general term for software encompassing a broad set of algorithms that mimic human cognition or perception.[15] On a high level, a classification is made between narrow AI and artificial general intelligence (AGI). Narrow AI consists of highly scoped machine-learning solutions that target a specific task, such as understanding a language or finding patterns in large datasets.[10,15] Narrow AI is currently responsible for all the real-world examples of AI in use or development: image and speech recognition, spam filters, search engines, product and movie recommendations, etc.[10,15] Narrow AI also has the potential to enable promising future applications such as autonomous cars, tools for rapid scientific discovery and digital assistants for quick medical image analysis of emergency ward patients.[15] AGI refers to the use of machine learning to handle a broad range of cognitive tasks. Such systems, were they to exist, would successfully perform any intellectual task that a human could perform and would learn to carry it out dynamically as humans do. Whether such systems should exist in the future or forever remain in the fictional realm of James Cameron's "*The Terminator*"[16] is currently being debated, but interest in them continues nonetheless. Businesses increasingly need to make fast decisions to remain competitive and are therefore, on the lookout for AI based solutions that can analyze a large amount of data in real-time instead of just storing large quantities of data in the cloud for retrospective analysis.

1.2 Paradigm shift in device architectures

AI workloads are different from the tasks most of our current computers are built to perform. They involve prediction, inference and intuition based on accessing and processing large amounts of data. However, conventional computing systems built using the classic Von Neumann architecture are unfortunately not suited for such tasks.[17] This

is because systems designed using this architecture consist of a microprocessor (central processing unit, CPU) for performing logic operations that is physically separated from memory units for data storage on a short-term (dynamic random access memory, DRAM) and long-term (hard disk/solid state drive, HDD/SSD) basis.[18] Processing a set of data stored in the memory involves a sequence of steps in which the data is first transferred from the memory to the CPU, then processed by the CPU and finally sent back to the memory for storage.[19] This leads to a significant quantity of data moving back and forth between the physically separate logic processor and memory units over bandwidth-limited and energy-inefficient electrical connections (bus).[17] It has been reported that up to 40% of the power consumed by modern computing systems is wasted simply in transferring data back and forth instead of doing anything with it.[20]

Historically, advances in computational capabilities have been attained in terms of faster data processing rates enabled by the miniaturization of semiconductor transistors, which are the building blocks of logic processors. When simple two-dimensional (2D) areal scaling of transistors no longer increased processing speed, the use of innovative techniques enabled continued improvements in terms of higher power efficiencies and a lower cost per device.[21] Examples include the implementation of new material stacks and the shift to three-dimensional (3D) device geometries.[21] Although logic processors have improved significantly over the past few decades, improvements in memory have mostly taken place in the form of a higher storage density, i.e., the ability to store more data in less space, rather than faster data transfer rates. This has happened most notably for SSD devices by utilizing the third dimension, similar to logic transistors, for stacking memory cell layers. Consequently, the logic processing device has been relegated to spending an increasing amount of time simply waiting for data to be fetched from memory. In effect, a logic processor is limited in its data processing rate by the speed at which data gets transferred from the memory device, a phenomenon well-known as the Von Neumann bottleneck.[17] Since AI workloads operate on a large amount of data, there is a need for not only processing the data faster but also for accessing a large amount of data in a quick and energy-efficient manner. As a result, new approaches to computing AI workloads are currently being sought that can overcome the memory bottleneck.

One of the initial approaches that are currently being undertaken involve the use of accelerator devices instead of just CPUs for the data-heavy AI workloads. Accelerators include devices such as graphics processing units (GPU), tensor processing units (TPU), intelligent processing units (IPU), application specific integrated circuits (ASIC), field programmable gate arrays (FPGA), etc.[22,23] Such devices incorporate heterogeneous integration of functionally diverse integrated circuits that are specialized to handle particular tasks.[24] They consist of numerous specialized logic cores, all working in

parallel on specific tasks, whereas conventional CPUs have only a few all-purpose cores that tackle computing tasks sequentially.[22,23] Parallel processing solves part of the Von Neumann bottleneck by breaking down calculations and distributing processing among specialized components, such that the device can work on different parts of the workload at the same time and in an energy-efficient manner.[22,23] Another approach relies on improving the data transfer rates between short-term/temporary memory (DRAM) and long-term/permanent memory (HDD, SSD). This can be performed by means of emerging memory devices, such as phase change, magnetorestive and resistive switching random access memories (PCRAM, MRAM, RRAM).[24,25] These devices make use of a reversible change in the properties of materials to store data.[24,25] All three are non-volatile memories meaning that they do not require power to retain data, unlike volatile DRAM, and have data access speeds and storage densities lying in between those of DRAM and SSD.[24,25]

More on-chip approaches for tackling the memory bottleneck involve monolithic 3D memory integration, replacing low density and volatile embedded memory with high density and non-volatile memory, adopting non-Von Neumann architectures through processor and memory co-location.[19,24–26] Monolithic 3D memory integration involves stacking memory dies directly on top of logic processor dies and interconnecting them by means of dense and short through-silicon-vias (TSVs).[24] This reduces the distance between processor and memory units that can improve data transfer rates while also enabling areal device scaling. Static random access memory (SRAM) currently serves as the on-chip or embedded memory in logic processor units. SRAM has a low density that prevents it from storing large amounts of data while its volatile nature consumes a lot of power. Replacing SRAM with higher density and non-volatile memories, such as the three emerging memories mentioned earlier, would enable faster access to a large amount of data while lowering energy consumption. A radically new approach involves transitioning to a non-Von Neumann architecture where data processing can be carried out at the same physical location as where the data is stored.[19,26] Such an emerging concept that relies on the physical properties of memory devices for both storing and processing information is known as "in-memory computing" or "computational memory".[19,26] The essential idea is not to treat memory as a passive data storage entity, but to exploit the physical attributes of the memory devices to actively process the data where it is stored. Or in other words, the same memory device can be used to simultaneously store input data, process it and then store the final output, yielding significant improvements in processing rates and energy-efficiency. Functional in-memory computing devices have been demonstrated using the emerging non-volatile memories mentioned earlier.[19,26] To sum up, a broad range of new devices and novel device architectures are needed to deliver the performance and functionality gains for enabling next-generation computing in the AI era.

1.3 Materials processing in a changing device landscape

The emerging devices and novel device architectures needed for addressing the data explosion in the AI era are based on multi-material stacks having atomic scale dimensions and 3D features. As a result, the fabrication of such devices calls for processing techniques that retain precise control over the thickness and properties of functional materials during either deposition or etching on both planar and 3D substrates. Techniques such as atomic layer deposition (ALD)[27,28] and atomic layer etching (ALE)[29,30] can enable atomic scale growth and etch control, respectively, during materials processing for device fabrication (see Figure 2). Furthermore, the increase in the quantity and type of materials involved together with the presence of 3D features during device fabrication and in final device architectures have simply raised the complexity of making such devices. This has led to the need for supplementing existing materials deposition and etching techniques with novel approaches in selective processing on both planar and 3D substrate topographies.

1.3.1 Plasma-enhanced atomic scale processing

ALD is a cyclic deposition process based on sequential and self-limiting reactant dose steps for synthesizing thin-films in a layer-by-layer manner, as illustrated in Figure 2a. The general aim of the surface reactions during ALD is to create stable (i.e., non-volatile) reaction products that result in material addition or growth. On the other hand, ALE can be considered as the etch counterpart of ALD. ALE is also a cyclic process based on sequential and self-limiting reactant dose steps, during which films are removed layer by layer, as outlined in Figure 2b and c. The main aim of the surface reactions during ALE is to create volatile reaction products that culminate in material removal or etching. For ALD, the self-limiting surface reactions during the separate reactant exposures confer excellent film uniformity on large area substrates and unparalleled conformality on high-aspect-ratio 3D substrates, as shown in Figure 2d and e.

In conventional thermal ALD, the energy needed for surface reactions to proceed is typically provided by substrate heating. An alternate source for part of the required energy can be obtained by using an energy enhanced ALD method known as plasma-enhanced atomic layer deposition, or plasma ALD.[31] In plasma ALD, the substrate is exposed to species generated by a plasma during one of the reactant exposure steps of the ALD cycle.[28,31] These species constitute a mixture of highly reactive atomic and molecular neutrals (plasma radicals), photons, ions and electrons. The substrate is typically grounded (see Figure 2a) during the plasma exposure step of ALD that yields ion energies upto about 30 eV (at sufficiently low pressures in remote inductively coupled plasma systems)[28] and therefore, causes the ions to play a relatively minor role during film deposition. The highly reactive radicals generated during plasma ALD can
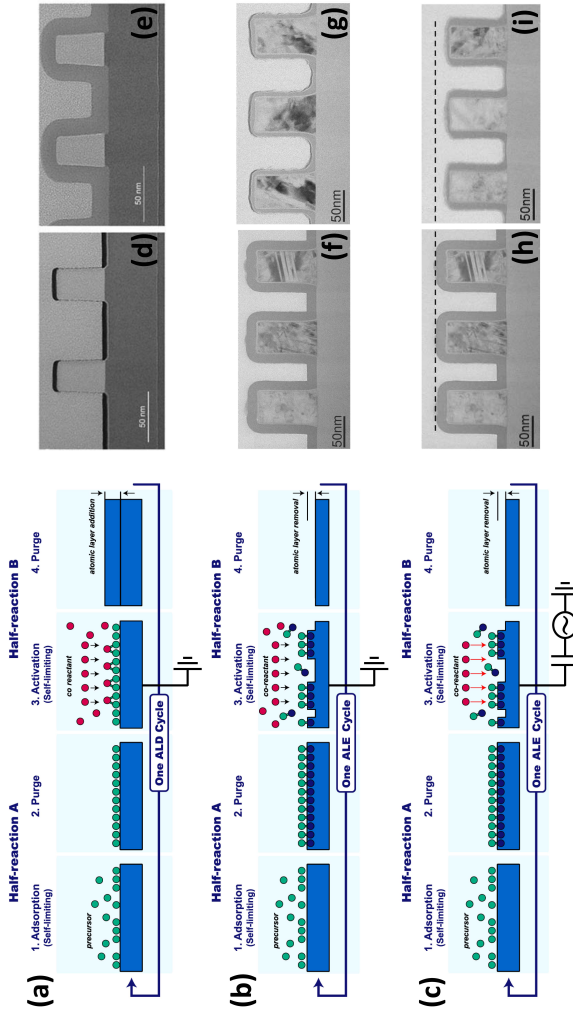
Figure 2. Schematic representation of one complete, generalized cycle of **(a)** conformal atomic layer deposition (ALD) **(b)** isotropic atomic layer etching (ALE) and **(c)** anisotropic ALE. The depicted processes consist of two half-reactions A and B and the total cycle is divided into four process steps. Step 1 is the "adsorption step" and step 3 is the "activation step" where the surface is exposed to reactants, here defined as "precursor" in step 1 and "co-reactant" in step 3. A plasma is used as the co-reactant in step 3 that leads to the impingement of isotropic radicals and anisotropic ions (indicated by arrows) on the surface. Steps 2 and 4 are "purge steps". The cycles, and hence the process steps, are repeated multiple times when depositing or etching a film. Every cycle adds or removes an atomic layer to or from the film for ALD and ALE, respectively. The substrate in **(a)** and **(b)** is grounded during the plasma exposure step leading to prominently radical-driven conformal deposition and isotropic etch processes, respectively, while the substrate in **(c)** is biased using an RF power supply connected through a blocking capacitor during the plasma exposure step. RF substrate biasing enhances ion energy and leads to an energetic ion-driven anisotropic etch process in **(c)**. Cross-sectional TEM images of 3D trench nanostructures **(d)** before and **(e)** after conformal plasma ALD of SiO_2,[53] **(f)** before and **(g)** after isotropic plasma ALE of SiN_x,[33] **(h)** before and **(i)** after anisotropic plasma ALE of SiN_x.[36] Conformal ALD adds film to all surfaces of 3D trenches while isotropic ALE removes film from all surfaces. Anisotropic ALE removes films only from the planar top and bottom surfaces of the 3D trench nanostructures while leaving films on the vertical sidewalls intact.

provide an alternate source for part of the energy required during film growth.[31] The high reactivity of these plasma species therefore, allows access to a parameter space such as low temperature deposition environments. Furthermore, controlling material properties during film growth at a particular temperature is typically carried out by varying either the substrate material or the reactants needed for film deposition. In case of plasma ALD at any given temperature, the various parameters of plasma operating conditions (e.g., reactant gas, flow rate, pressure, power, direct/remote source configuration, etc.) allow greater freedom in processing conditions for accurately controlling the growth and material properties of thin-films.[28]

Similar to the case of thermal ALD, the energy needed for surface reactions to proceed during the sequential and self-limiting reactant dose steps in thermal ALE are provided by substrate heating. This leads to uniform film removal on large-area planar substrates and isotropic material removal on 3D substrates (see Figure 2f and g), which is the counterpart of conformal material deposition by ALD (see Figure 2d and e). A plasma can again be used to provide an alternate source for part of the energy required during film removal. However, depending on which of the plasma species – radicals or ions – drives the process, films can be removed in either an isotropic or an anisotropic manner on 3D substrates during plasma ALE.[32]

When plasma ALE processes are radical-driven, whereby ions have low energies (e.g., at high pressures[33] and/or on grounded substrates, see Figure 2b) that lie below material sputtering thresholds, films are removed isotropically from 3D substrates as depicted in Figure 2f and g. In case of ion-driven plasma ALE processes, ion energies are enhanced (e.g., on RF biased substrates, see Figure 2c) beyond the sputtering thresholds of the modified surface layer formed in the preceding precursor dose step, provided the enhanced ion energies lie below the sputtering thresholds of the underlying bulk material.[29,30,34,35] This condition prevents spontaneous etching of the bulk material and enables a self-limited etching process.[29,30,34,35] Only the films located at regions perpendicular to the ion trajectory on 3D substrates (e.g., planar top and bottom regions of 3D trench nanostructures) are removed in an anisotropic or directional manner,[29,30,34,35] as shown in Figure 2h and i.[36] In this regard, anisotropic plasma ALE can be considered to be a means for carrying out selective atomic scale processing on 3D substrate topographies (i.e., topographically selective processing, see next section), such that films situated on surfaces parallel to the ion trajectory (e.g., vertical sidewalls of 3D trench structures) are left intact. The classification of plasma ALE processes into radical-driven isotropic and ion-driven anisotropic processes on 3D substrates is one of the key differences with plasma ALD. It also suggests that the implementation of an analogous ion-driven regime during plasma ALD on 3D substrate topographies could provide new opportunities for selective processing.

1.3.2 Topographically selective processing on 3D substrates

As mentioned before, the increased complexity in fabricating new devices consisting of various layers of nanoscale materials and 3D features has led to the need for expanding the portfolio of current deposition and etching techniques with novel approaches in selective processing. Different categories of selectivity during film growth on a patterned planar substrate composed of different surface materials have been defined in the literature as area-, phase-, microstructure or chemical composition-selective deposition.[37] In area-selective deposition using gas-phase reactants on a patterned planar substrate composed of, e.g., two different surface materials, film growth occurs only on the surface area of one substrate material and not on the other, as illustrated in Figure 3a. The selectivity arises from a difference in the interfacial reactions between the different surface material areas of the patterned substrate and the gas phase reactants that the substrate is exposed to.[37] For example, an area-selective ALD process for In_2O_3:H was recently demonstrated by Mameli *et al.*[38] on a patterned planar substrate consisting of OH-terminated and H-terminated Si surface areas. The In_2O_3:H film grew only on the OH-terminated Si surface areas and not the H-terminated surface areas.[38]

In phase-selective deposition, films with different material phases (e.g., crystalline/amorphous) are grown simultaneously and selectively on the different surface areas of the different materials that form a patterned substrate. Similar to phase-selective deposition, films with different microstructures (e.g., void-rich/deficient, large/small grain size, etc.) or different chemical compositions (e.g., impurity rich/deficient, over/under stoichiometric, etc.) may be deposited simultaneously on the different surface areas of the different materials that form a patterned substrate. This ultimately leads to microstructure- or chemical composition-selective deposition. For instance, a case for microstructure-selective deposition may be inferred from recent work reported in the literature where ALD of TiO_2 was performed on a patterned substrate composed of Al_2O_3 and SiO_2 surface regions.[39] The authors reported on the simultaneous growth of TiO_2 films on both regions of the patterned substrate with the selective formation of large grains on the Al_2O_3 and small grains on the SiO_2 surface regions.[39] Since the categories of phase-, microstructure-, and chemical composition-selective deposition have been defined based on the inherent differences in material properties ensuing from growth on a patterned substrate, one could argue that these cases are simply different examples of one common selective deposition process. As a result, the aforementioned cases of simultaneous film growth with different material properties can be collectively represented by a single term, namely material property-selective deposition. This is illustrated schematically in Figure 3b.
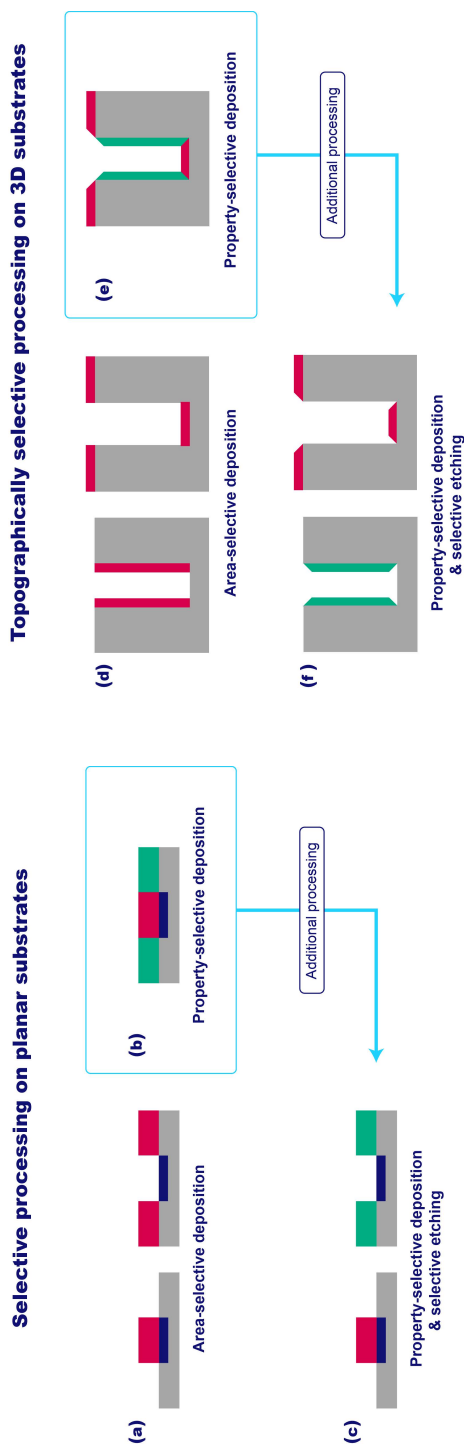
Figure 3. Schematic illustration of selective processing on planar substrates and topographically selective processing on three-dimensional (3D) substrates composed of trench-shaped nanostructures. **(a)** Area-selective deposition of films on different surface regions of a patterned planar substrate composed of different surface materials. **(b)** Material property-selective deposition of a film simultaneously on the different surfaces of the patterned planar substrate, where film regions with different colors denote material having different properties, e.g., phase, microstructure, chemical-composition, etc. Note that films with different material properties are shown over here to have the same thickness and growth rate, which may or may not be the case in reality. **(c)** Material property-selective deposition followed by selective etching of films having different material properties on the different surfaces of the patterned planar substrate. **(d)** Area-selective deposition of films on the differently oriented surface regions (planar top and bottom regions, vertical sidewalls) of the 3D trench-shaped substrate. **(d)** Area-selective deposition of films on the differently oriented surface regions on the differently oriented surfaces of the 3D trenches, where film regions with different colors denote material having different properties, e.g., phase, microstructure, chemical-composition, etc. Note that films with different material properties are shown over here to have the same thickness and growth rate, which may or may not be the case in reality. **(f)** Material property-selective deposition followed by selective etching of films having different material properties on the differently oriented surfaces of the 3D trenches. The selective etching can be performed by additional processing (e.g., wet- or dry-etch treatment) either post-deposition or during deposition (e.g., combining selective deposition and selective etch steps in a sequential process cycle). Note that the tapered corners of the films in **(e)** and **(f)** serve to indicate an approximate example of how the properties of films at those corners might evolve during growth under the influence of energetic and directionally impinging species.

The process of area-selective deposition has come to be well-understood as the occurrence of film growth on one surface with respect to another, where the difference between the two starting surfaces are characterized by the corresponding differences in their material properties. In this regard, material property-selective deposition can be intuitively understood as the occurrence of film growth on two different starting surfaces, each with different material properties, which induce differences in the properties of films growing concurrently on those surfaces. In principle, films obtained on a patterned planar substrate by such material property-selective deposition processes have the potential to undergo further processing in a selective context. For instance, these films can be subjected to an appropriate post-deposition processing step, such as a wet- or dry-etch treatment. This additional processing may very well be carried out during the deposition itself, e.g., in a cyclic process that sequentially combines selective deposition and selective etch steps. These approaches could in principle, selectively etch films from one region of the patterned substrate while leaving films grown on the other regions intact (or vice-versa) based on the inherent differences in film properties at those regions. This is illustrated schematically in Figure 3c. Such methods could potentially enable films to be obtained only at the desired areas of a patterned planar substrate if, for instance, area-selective bottom-up deposition processes for obtaining the films selectively at those desired areas do not exist. For example, the final feature layouts depicted in Figure 3a after area-selective deposition resemble the respective layouts depicted in Figure 3c. This could be achieved by conducting a selective etch treatment in an additional processing step after or during property-selective deposition depicted by the layout in Figure 3b.

With regard to the cases discussed above for patterned planar substrates having different surface materials, selective deposition can also be carried out in an analogous fashion on 3D substrates having different surface orientations. This is illustrated in Figure 3d-f where the 3D substrates consist of trench-shaped nanostructures in which the surface planes of vertical sidewalls are perpendicularly aligned to the corresponding planes of the planar top and bottom trench regions. Figure 3d illustrates area-selective deposition on the vertical sidewalls or the horizontal top and bottom regions of the trench structures. An example of such a process was recently demonstrated by Bent and co-workers[1] where they performed area-selective ALD of Pt on 3D trench nanostructures. The Pt film was reported to grow only on the vertically oriented sidewall surfaces of the trench nanostructures and not on the horizontally oriented (i.e., planar) top and bottom surface regions of the trench structures.[1] From a conceptual point of view, this could also be interpreted as a case of anisotropic deposition. It could very well be considered as the ideal or most extreme case of non-conformal film growth on a 3D substrate. Such an approach for growing films in an anisotropic and area-selective manner on 3D substrates with different geometries or surface orientations has been

termed as topographically selective deposition.[1] Conversely speaking, any materials processing technique carried out on a 3D substrate, be it deposition or etching, could be considered to be topographically selective if there is an anisotropic characteristic associated with it. In this regard, typical ion-driven etch processes, such as reactive ion etching (RIE) or directional plasma ALE, performed on 3D substrates could be considered as topographically selective etch processes. By the same reasoning, one could also expect the cases of material property-selective deposition (discussed earlier for a planar substrate) to bring about topographically selective deposition when performed on a 3D substrate. Going back to the case of area-selective ALD of Pt on 3D trench nanostructures, the anisotropic film growth during ALD was achieved by selectively treating the planar surface regions of the 3D trench nanostructures using anisotropic ion implantation of fluorocarbon species. This led to the creation of an ultrathin hydrophobic surface layer only at the planar trench regions which inhibited growth of Pt films at those regions, thereby yielding topographically selective deposition at the vertical sidewalls.[1]

George and co-workers[40] recently demonstrated a topographically selective deposition process on 3D trench nanostructures that was complementary to the results reported by Bent and co-workers.[1] The former reported area-selective deposition on the planar top and bottom surfaces of 3D trench nanostructures using electron-enhanced ALD of BN.[40] Electron-enhanced ALD itself is an emerging concept whereby deposition is carried out using sequential and self-limiting exposures of electrons and a precursor.[40] Dangling bonds have been reported to form at surfaces undergoing electron exposure through the process of electron stimulated desorption, after which the dangling bonds facilitate precursor adsorption and hence, film growth.[40,41] For a 3D trench, the dangling bonds should, in principle, form only at the planar top and bottom trench surfaces aligned perpendicular to the directional electron flux and not on the vertical sidewalls aligned parallel to the same electron flux. This strategy of selective dangling bond formation was reported to enable topographically selective deposition of BN on the 3D trench nanostructures in terms of area-selective film growth on the planar trench surfaces.[40] This case of anisotropic deposition reported by George and co-workers[40] using ALD is a typical outcome of the widely-used continuous, flux-dependent and line-of-sight based deposition processes (e.g., physical vapour deposition, PVD), which offer no precise growth control. The sequential and self-limiting process of ALD, which offers atomic scale growth control, has been historically adopted to prevent such anisotropic or non-conformal film deposition. However, as mentioned before, the increased complexity in manufacturing future devices consisting of various multi-material layers across planar and 3D layouts calls for atomic scale processing techniques that are also selective in nature.

Figure 3e illustrates topographically selective deposition in terms of simultaneous growth of films with different material properties at the differently oriented surfaces of 3D trench nanostructures. Similar to the case discussed earlier for patterned planar substrates, films obtained on 3D trench nanostructures in such a material property-selective manner also have the potential to undergo additional processing in a selective context. Exposing these films to an appropriate post-deposition processing step, e.g., wet- or dry-etch treatment, could in principle, lead to topographically selective film etching. Likewise, the additional processing could also be performed during deposition, e.g., in a cyclic process that sequentially combines selective deposition and selective etch steps. For instance, film regions could be selectively etched from the planar surfaces of the 3D trenches while those at the vertical sidewalls are left intact (or vice-versa), based on inherent differences in the properties of films formed at those differently oriented regions by material property-selective deposition. Analogous to the case for planar substrates, such methods have the potential to yield films only at the desired surface orientations of 3D substrates if, for instance, area-selective deposition processes for obtaining the films only at those desired surfaces do not exist. This is illustrated in Figure 3f. It shows that the final feature layouts formed upon conducting a topographically selective etch treatment on the layout obtained after or during property-selective deposition in Figure 3e resemble the respective layouts obtained in Figure 3d by area-selective deposition. An example of material property-selective deposition on 3D substrates can be inferred from the work conducted by Agarwal and co-workers[42] for plasma ALD of SiC_xN_y on 3D trench nanostructures. Film deposition was followed by a wet-etch treatment, which resulted in the selective removal of SiC_xN_y film regions on the vertical trench sidewalls while those on the planar top and bottom trench surfaces remained behind, similar to the layout illustrated in Figure 3f. This was attributed to the anisotropic nature of mild ion bombardment during plasma exposure (on a grounded substrate) which was speculated to densify film regions selectively at the planar trench surfaces.[42] It consequently made the film regions growing at those planar trench regions comparatively more wet-etch resistant than the film regions formed on the vertical sidewalls. Based on these observations, one could infer that topographically selective deposition of SiC_xN_y films was attained on the 3D trench nanostructures in terms of microstructure-selective growth of low density films at the sidewalls and high density films at the planar top and bottom trench surfaces.

The examples discussed above clearly elucidate how the impingement of directional species before or during film growth by ALD on 3D substrates are key to performing topographically selective deposition. Besides these examples reported in academia, several examples have also been reported by industrial sources that can be considered to lie under the umbrella of topographically selective processing on 3D substrates, as shown in Figure 4. A recent report from ASM shows how films were

obtained by topographically selective processing only at planar regions of 3D trench nanostructures and not its sidewalls.[2] Another example from ASM showed the opposite result whereby films were obtained only at vertical sidewalls after topographically selective processing.[43] Similar examples have also been reported recently by Tokyo Electron.[21,44] Films obtained in such a manner at specific surface orientations have been reported to serve purposes such as horizontal or vertical etch stop layers during device fabrication.[2,21] These examples highlight how the industry is currently looking at new ways for selective materials processing in the 3rd dimension as 3D features become the norm in both device fabrication and final device architectures. Quoting Clark and co-workers,[21] "Ultimately integration engineers would like to have a variety of processes to choose from including selective, non-selective, isotropic, and anisotropic processes for both functional and sacrificial materials, and all with atomic level thickness and variability control, representing an area ripe for new innovations." On this accord, topographically selective processing on 3D substrates are needed to address upcoming challenges in transferring next-generation device technologies from the lab to the fab.
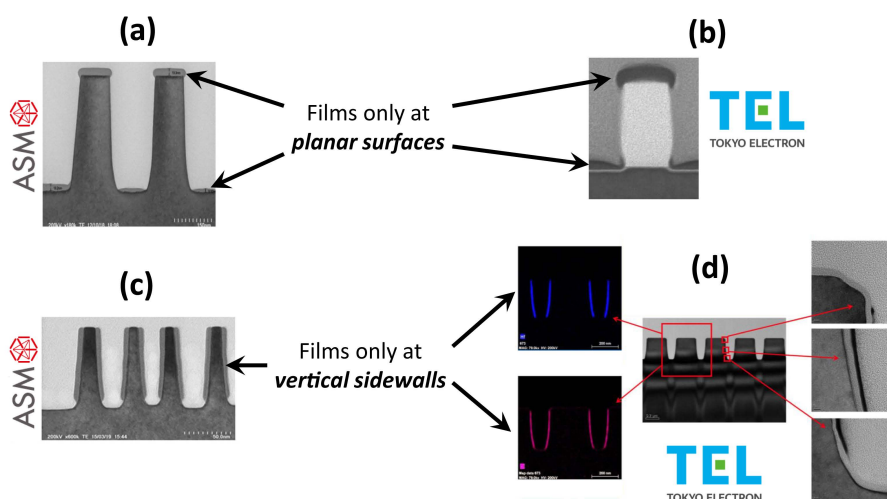
Figure 4. Cross-sectional images of films obtained either on **(a), (b)** planar surface orientations or **(c), (d)** vertical surface orientations of 3D trench-shaped nanostructures after topographically selective processing.[2,21,43,44] The films in **(a)** and **(c)** consist of SiN_x while those in **(b)** consist of TiO_x. The films in **(d)** denote HfO_2 and Al_2O_3.

1.4 Aim of this research

As evident from the discussion in the previous two sections, the impingement of directional species during both ALD and ALE processes can have an influence on the resulting film properties, especially when films are added or removed from 3D

substrates. In case of plasma-enhanced atomic scale processing, the ion flux impinging on the substrate constitute one of the directional species that can play a significant role.[45,46] While the plasma radical flux can enable conformal film deposition or isotropic film etching through their high reactivity and non-directional nature, the additional energy delivered to a deposition surface by the kinetic energy of a directional ion flux can influence the material undergoing processing. The extent to which ion-surface interactions can influence a material, during both deposition and etching, also depends on other factors such as the mass, reactivity, impingement rate (or flux) and dose (or net flux integrated over time) of ionic species incident on the film surface.[45,47–51] Based on the values of these parameters, various physical, chemical or combined physicochemical processes can occur at the surface and sub-surface regions of the film as the ions transfer energy and momentum during deposition or etching. Furthermore, the concurrent arrival of energetic ions and reactive radicals at a surface has been reported in the literature to bring about synergistic ion-radical processes during both deposition and etching.[45,46,52] Given the multitude of factors that can play a role during ion-surface interactions, it is not a trivial or straightforward task to anticipate and understand the role of ions during materials processing.

The effects of ion-surface interactions have been the subject of detailed investigation during plasma-enhanced chemical and physical vapor deposition, which are continuous deposition techniques that do not have precise or atomic scale growth control. Ion-surface interactions have also been extensively investigated for plasma-based dry etching processes such as reactive ion etching, which is also a continuous and flux dependent etching technique offering no atomic scale precision during material removal. The role of ions are currently undergoing intense scrutinization for the case of sequential and self-limiting plasma ALE. As explained in the previous sections, plasma ALE can lead to both isotropic and anisotropic processes on 3D substrates, which are primarily the result of how the energy of directional ionic species impinging on a substrate are controlled during film etching. This leads to an important question that acted as a key driving force behind the research conducted in this dissertation – "*What is the role of ions during plasma ALD on 3D substrate topographies*?"

This dissertation investigates plasma-enhanced atomic scale processing of functional materials and the role of ions during these processes on planar and 3D substrate topographies, relevant for next-generation device technologies.

1.5 Outline of chapters

Chapter 2 begins by providing an overview of patterning techniques that have been and are going to be used to continue device scaling. It then presents an outline of the state-of-the-art and next-generation devices which are or will undergo scaling on the basis of

two categories – logic and memory devices. This paves the way for understanding the challenges involved in fabricating these devices. The chapter concludes by elucidating some of the key challenges associated in current and future device fabrication from the perspective of materials deposition and etching, and how atomic scale processing techniques can already address or are well poised to address those challenges.

Chapter 3 provides an overview on the basics of controlling ion energy and flux characteristics in a remote plasma processing system. It elucidates how a substrate exposed to a plasma can be biased to acquire a negative average potential, which controls the potential of the sheath formed between the plasma and the substrate. The chapter explains how this control over the sheath potential eventually renders control over the ion energies during plasma processing. The chapter concludes by providing an overview of the research reported in the literature where ion energies have been controlled during plasma ALD.

Chapter 4 presents a new plasma ALD process for SiN_x developed using a novel organosilane precursor and nitrogen plasma. As will be discussed in Chapter 2, dense and wet-etch resistant SiN_x films that can be synthesized at temperatures <400 °C serve as spacers or encapsulation layers for protecting sensitive device components; e.g., gate stacks in 3D transistors or magnetic tunnel junctions in emerging magnetoresistive memories. Chapter 4 outlines how SiN_x films with a high density and low impurity content were obtained using the process developed in this work at low temperature environments. Depositions were carried out first on planar substrates and then on high aspect ratio 3D substrates consisting of trench-shaped nanostructures to investigate SiN_x film conformality and wet-etch resistance. Sources limiting conformality on 3D substrates were identified and attributed to factors occurring during nitrogen plasma exposure. Identification of factors associated with plasma processing conditions is a prerequisite for addressing the challenge of growing conformal SiN_x on 3D substrates by plasma ALD. The chapter concludes by providing experimental evidence of wet-etch resistant SiN_x films grown on 3D trench nanostructures at a substrate temperature <400 °C using the plasma ALD process developed in this work.

Chapter 5 presents the investigation pertaining to the effects of ion energy control with substrate biasing on the properties of films deposited on both planar and 3D substrates. This technique was demonstrated to significantly enhance the versatility of plasma ALD processes by enabling control over a diverse range of material properties during deposition. A commercial 200-mm remote plasma ALD system equipped with RF substrate biasing was used to control the ion energy during the plasma exposure step. The chapter provides an extensive characterization of the effects of substrate biasing spanning six different materials with dielectric or conductive properties (oxides and nitrides of Ti, Hf, and Si), relevant for a wide variety of applications. This work is the first

to report on the effects of ion energy control during plasma ALD of nitride based materials. The chapter also presents the first experimental investigation on the effects of ion energy control during plasma ALD on 3D substrates. The chapter concludes by providing an overview of the exciting opportunities afforded by this technique, such as topographically selective processing on 3D substrates, for advancing practical applications of atomic scale processing.

Chapter 6 deals with the measurement of ion flux-energy distribution functions (IFEDFs) of a variety of different plasmas typically used in plasma ALD. Insights from such measurements are essential for understanding how a given plasma ALD process at different operating conditions can be influenced by energetic ions. The chapter outlines an extensive overview of IFEDFs measured using a retarding field energy analyzer (RFEA) for different operating conditions (source power, pressure) and substrate configurations (grounded and RF biased). It then presents the analyses of film properties spanning three different materials (dielectric or conductive) in terms of the ion energy and flux characteristics derived from IFEDFs. The results of this chapter have provided a better understanding of the relation between energetic ions during plasma ALD and the resulting material properties. This work is notably the first to directly correlate the properties of different materials grown using plasma ALD and the characteristics of energetic ions measured experimentally using a RFEA.

Chapter 7 reviews past research efforts on ALE and identifies the key defining characteristics of this currently re-emerging field in analogy to ALD, which is the more mature and mainstream deposition counterpart of ALE. Subsequently, parallels were drawn between ALE and ALD from which lessons and concepts were elucidated with the aim for advancing the field of ALE.

Chapter 8 concludes by summarizing the contents of this dissertation and provides an outlook for future research exploring the role of energetic ions during plasma-enhanced atomic scale processing.

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Atomic Scale Processing for Addressing the Challenges of Current and Emerging Device Technologies
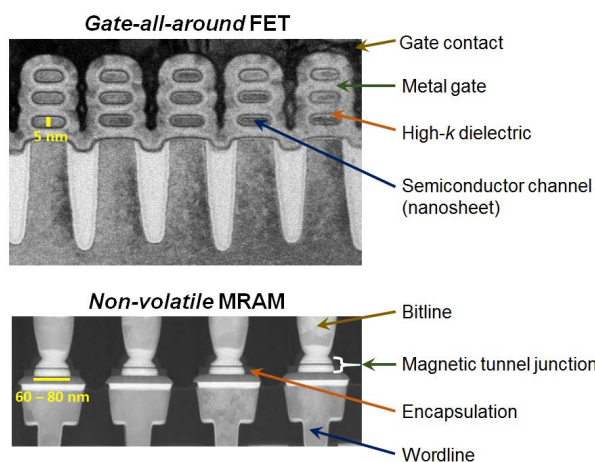
Recently, a gate-all-around field effect transistor (FET) and a non-volatile magnetoresistive random access memory (MRAM) were reported by IBM[1] and Intel,[2] respectively. These devices are intended for being used in next-generation semiconductor integrated circuits (ICs). The images above are taken from the aforementioned reports which illustrate cross-sectional details of the (top) transistor logic device consisting of nanosheet semiconductor channels and the (bottom) memory device consisting of magnetic tunnel junctions. The key to fabricating such devices with nanoscale dimensions involves using processing techniques that enable material deposition and/or etching with atomic scale precision. In this chapter, we first present an overview of current and upcoming multiple patterning techniques that enable continuation of device scaling. It is followed by a brief overview on the state-of-the-art and next-generation semiconductor logic and memory devices. This paves the way for understanding the challenges involved in fabricating these devices and how atomic scale processing techniques – such as atomic layer deposition and atomic layer etching – can be used to address those challenges. To put things in perspective, the challenges discussed in this chapter need to be addressed for improving the smartphones currently lying in our pockets or for enabling self-driven cars in the upcoming era of artificial intelligence.

The perennial demand for faster, smaller and more advanced devices necessitates constant innovation from the micro- and nano-electronics industries. At the very core of these devices lies semiconductor based integrated circuits (ICs): building blocks of logic processors (or central processing units, CPUs) and memory chips found in computing systems ranging from hand-held smartphones to communications satellites. In 1965, Gordon Moore published an article noting that the number of electronic components, known as semiconductor transistors, that could be crammed into an IC chip of fixed area was doubling approximately every two years.[3] This exponential increase has come to be known as Moore's law. Although this was empirical and based on only six years of data available between 1959 (when the first semiconductor IC was fabricated) and 1965, the miniaturization of semiconductor transistors over the past five decades has followed the basic tenet of Moore's law (see Figure 1).[4] This scaling of devices has played a major role in bringing about the digital revolution that has had a lasting impact on the development of modern civilization.

This chapter begins by providing an overview of the techniques that have been and are going to be used to continue device scaling. It then presents an outline of the state-
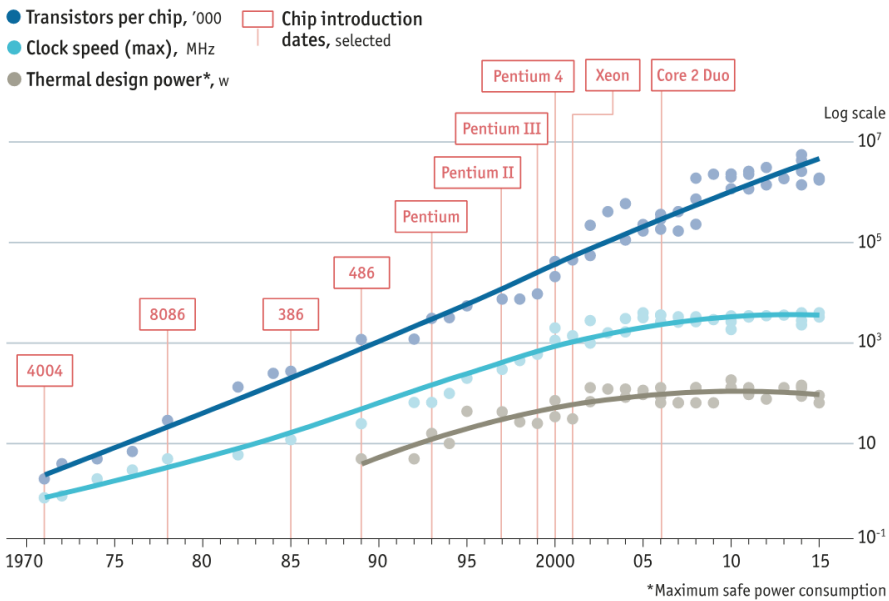
Figure 1. A log scale plot showing the transistor count (x1000) for a constant die (or chip) area, maximum transistor switching frequency (or clock speed in MHz), maximum rate at which heat energy generated by the transistor die is designed to dissipate under any workload by the cooling system (thermal design power in W), as a function of time (in years since 1970). The plot also indicates when selected logic processors from Intel (designated by their brand nomenclature) manufactured in high volume were introduced in the commercial market.[4]

of-the-art and next-generation devices that are or will undergo scaling on the basis of two categories – logic and memory devices. Finally, the chapter elucidates some of the key challenges associated in the fabrication of these devices from the perspective of materials deposition and etching, and how atomic scale processing techniques can already address or are well poised to address those challenges.

2.1 Device scaling with multiple patterning

For a long time, one of the main ways through which semiconductor IC devices were scaled involved improving the capability of photo-lithography based patterning techniques to create constantly smaller feature dimensions.[5] This technique is outlined in Figure 2. A substrate is first coated with a light sensitive material called a photoresist. Light is then directed at the photoresist through a patterned mask of transparent and opaque areas, called a photomask. This allows the photomask pattern to be imaged on the photoresist such that some of its regions are exposed to light while others are not. In case of a positive photoresist, the exposed regions are degraded by the incident light. These regions can be removed e.g., by dissolving in a solvent, while the unexposed regions remain behind. This results in a pattern of features left standing on the wafer surface whose shape is determined by the photomask pattern. The wafer with the patterned photoresist features at the surface then undergoes anisotropic etching, e.g., using a plasma ion-driven anisotropic etch step. This removes the bare regions of the underlying layer while the regions directly beneath the photoresist features remain intact. After this, any remaining photoresist material can be selectively removed with respect to the target material leaving behind patterned features of the target material. The lateral dimensions of these features are determined by the corresponding dimensions of the patterned photoresist.

(a) *Photoresist deposition*   **(b)** **Light exposure under photomask**   **(c)** **Develop and remove** *exposed photoresist*   **(d)** **Etch final pattern**
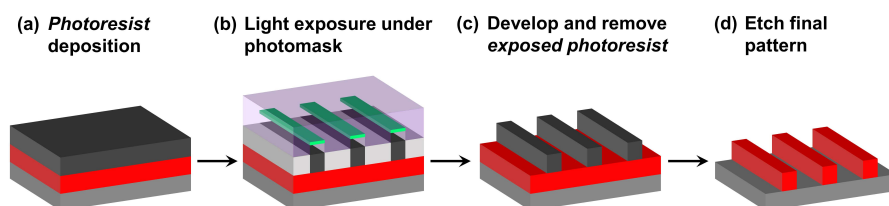
Figure 2. Patterning using conventional photo-lithography with a photomask and positive photoresist.

Current IC chip designs have smaller and denser features than can be created cost-effectively using available immersion photo-lithography tools employing 193 nm wavelength light. To overcome the limitations of photo-lithography, multiple patterning schemes have been implemented based on multiple lithography steps or self-aligned patterning techniques that enable continuation of device scaling. The simplest type of

multiple patterning is double patterning which simply doubles the density of patterned features. A frequently used double patterning scheme involves repeating a step sequence composed of a light exposure followed by an anisotropic etch two times. This is also known as a litho-etch-litho-etch process (LELE). It allows the transfer of a given photomask pattern to two adjacent layers of hardmasks on a wafer over a span of two identical lithography based patterning sequences. Triple patterning (LELELE), quadruple patterning (LELELELE) and so forth simply involves repeating the patterning sequence for the required iterations. Although 13.5 nm wavelength EUV technology has become available for photo-lithography as a possible alternative, cost and throughput compared to 193 nm immersion lithography combined with multiple patterning are still prohibitive to replace most process steps.[6–8]

A patterning technique that has been recently utilized for scaling semiconductor device dimensions is self-aligned multiple patterning. Step sequences for two such patterning schemes are shown in Figure 3.[9–13] In the first scheme, a feature known as a mandrel (termed *mandrel 1* in Figure 3.I.a) is pre-defined using a lithography step. A material is then deposited as a conformal layer on the pre-defined mandrel (Figure 3.I.b). This conformal layer is subsequently etched back using an anisotropic etch process such that the portion of the layer covering the mandrel is removed while the portions on the two sidewalls of the mandrel remain (Figure 3.I.c). The mandrel is then removed using a subsequent etch step leaving two sidewall spacers for each mandrel (Figure 3.I.d). The free-standing spacer structures are then used to transfer the pattern formed by the spacers to the underlying layer using an anisotropic etch step (Figure 3.I.e). The lateral dimensions of the etched features (termed as *mandrel 2* in Figure 3.I.e) are defined by the lateral dimensions of the free-standing structures in the previous step. Since there are two spacers for each mandrel, the feature density of the initial pattern is doubled in the subsequent pattern. Stopping the patterning scheme at this step would lead to a process known as self-aligned double patterning (SADP). Continuing the patterning scheme by repeating the aforementioned spacer formation and pattern transfer steps (Figure 3.I.f to i) again doubles the feature density. Altogether, the density of the initial pattern gets increased by a factor four, thereby resulting in self-aligned quadruple patterning (SAQP). Hence, a characteristic feature of the self-aligned multiple patterning technique is that pattern density can be increased by simply repeating the spacer formation and pattern transfer steps. Although this technique often requires extra processing steps, a key advantage is that it avoids variations caused by mask misalignment that can arise during LELE based double patterning. Since the critical dimensions are defined by spacer formation and mandrel removal, stringent process control for the deposition and etch steps that determine spacer dimensions is of utmost importance.
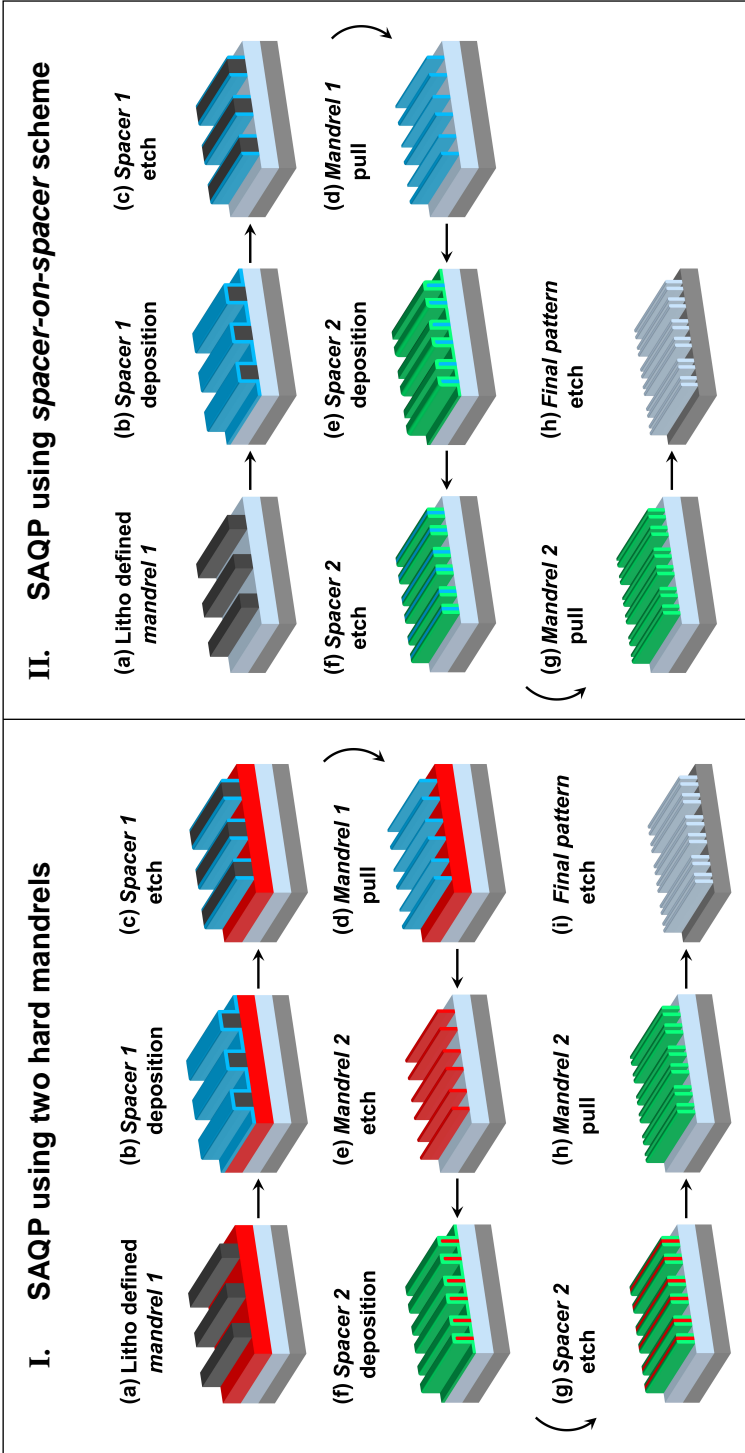
Figure 3. Schematic of self-aligned quadruple patterning (SAQP) processes **I. (a)-(i)** with two hard mandrels and **II. (a)-(h)** employing a spacer-on-spacer scheme. The mandrels are the patterned features that define where the sidewall spacers are subsequently situated. For both SAQP schemes, conformal thickness and smooth features are needed to enable correct target pattern reproduction

In the standard SAQP process described above, two hard mandrels are used as sacrificial materials to obtain the desired pattern at the target layer. An alternative approach for SAQP is shown in Figure 3.II using a *spacer-on-spacer* scheme.[12,13] In this approach, free-standing spacer structures are again obtained by anisotropically etching a material deposited conformally on a pre-defined mandrel that is subsequently removed (Figure 3.II.a to d). Instead of transferring the pattern formed by the free-standing features (termed *spacer 1* Figure 3.II.d) to the underlying layer, a second material is deposited as a conformal spacer layer (termed *spacer 2* in Figure 3.II.e) on the features of *spacer 1* (thus leading to *spacer-on-spacer*). This conformal layer is then etched back anisotropically such that the layer portion on top of *spacer 1* is removed while the layer portions on the sidewalls of *spacer 1* remain (Figure 3.II.f). *Spacer 1* is then removed selectively in a subsequent etch step with respect to the sidewalls and the underlying layer (Figure 3.II.g) leaving two free-standing features of *spacer 2* for each feature of *spacer 1*. The pattern formed by these features of *spacer 2* is then transferred to the underlying layer using an anisotropic etch step (Figure 3.II.h). As before, the lateral dimensions of the final pattern are defined by the lateral dimensions of the free-standing spacers formed in the previous step. The advantage of SAQP using the *spacer-on-spacer* scheme is that fewer sacrificial layers and processing steps are needed which result in lower costs and better throughput. While SADP using one hard mandrel with current 193 nm immersion lithography can achieve a pitch resolution of ~40 nm, SAQP with two hard mandrels can achieve a pitch resolution of ~20 nm. With such small feature dimensions, minimizing variability of the associated deposition and etch steps for spacer formation is of crucial importance.

2.2 Logic devices

Any electronic computing system requires two basic information sets – instructions (or programs) and the data to program with. The information sets are represented using the two-value binary numeral system where the smallest unit of information, known as a bit, is either a "0" or "1".[14] In electronic computing systems, these bits are a manifestation of the two-state characteristics of electrical circuits, e.g., high/low voltages applied to a transistor, or ON/OFF currents passing through it. A transistor therefore, serves as a switch that allows alternating between two bit states. A planar metal oxide semiconductor field effect transistor (MOSFET) device is shown in Figure 4a.[15,16] It has two doped semiconductor regions called the source and the drain which are separated by a region of oppositely doped semiconductor called the substrate. An n-channel MOSFET (or NMOS) has an n-type semiconductor source and drain separated by a p-type semiconductor substrate while a p-channel MOSFET (or PMOS) would have the opposite doping in the source, drain and substrate regions. The semiconductor material is usually silicon although other semiconductor materials having more mobile

charge carriers can also be implemented, e.g., Ge or III-V compound semiconductor channel.[17–19] A thin layer of insulating material, e.g., SiO_2, lies on top of the region between the source and the drain. This layer is covered by a conductive electrode called the gate. The insulating layer is termed as the gate oxide. For typical operating conditions, the source and the substrate are grounded while a positive voltage is applied to the drain. The drain p–n junction is reverse biased in these conditions and no current flows between the drain and the substrate. Since the bias across the source p–n junction is zero, there is also no current flowing from the substrate to the source. Consequently, there is no current flow between the source and the drain, and the transistor is in the OFF state akin to an open switch. For an NMOS, when a sufficiently large positive voltage is applied to the gate, an electron-rich layer known as the channel is formed beneath the gate oxide. The channel forms a continuous electron pathway between the source and the drain that allows current to flow between these two electrodes. The transistor is then in the ON state and is analogous to a closed switch. The region beneath the electron-rich channel consists of holes that have been repelled away by the positive voltage applied to the gate. These holes are the majority charge carriers in p-type semiconductors. An ideal transistor has zero current flow when it is OFF, zero resistance when it is ON and is capable of switching instantly from the OFF to the ON state, and vice versa.

Logic circuits composed of transistors in a CPU function as the brain of an IC device by executing instructions and processing data with mathematical operations.[20] Besides increasing the density on a chip of constant area, scaling the dimensions of transistors have other incentives that can improve their functionality. In 1974, Dennard and co-workers published a seminal paper in which they demonstrated the benefits of scaling.[21] They concluded that a small transistor can be switched between ON and OFF states with less power and at a higher frequency (or clock speed) than a larger one. This meant that a larger number of faster transistors could be used in the same IC chip area without needing more power or generating more waste heat (see Figure 1). This held true for some time until the late 1990s after which scaling transistors no longer made them more energy-efficient. This is because as a transistor grows smaller, a residual current begins to leak through the channel even when it is switched OFF, which wastes power and generates more heat. This lowers device performance and many modern chips must either run below their maximum switching speeds or even periodically switch parts of themselves OFF to avoid overheating. As a result, it was no longer worth increasing the transistor clock speed which hit a ceiling from about 2003 onward (see Figure 1). Since then, device scaling has continued through the implementation of clever techniques that can deliver improved performance, within reasonable power limits, at a manufacturable chip area and with a reduced cost per device.[22] This combined approach to power, performance, area, and cost (PPAC) scaling is the current norm within the

(a) Planar FET

(b) 3D *fin*FET

(c) 3D *gate-all-around* FET
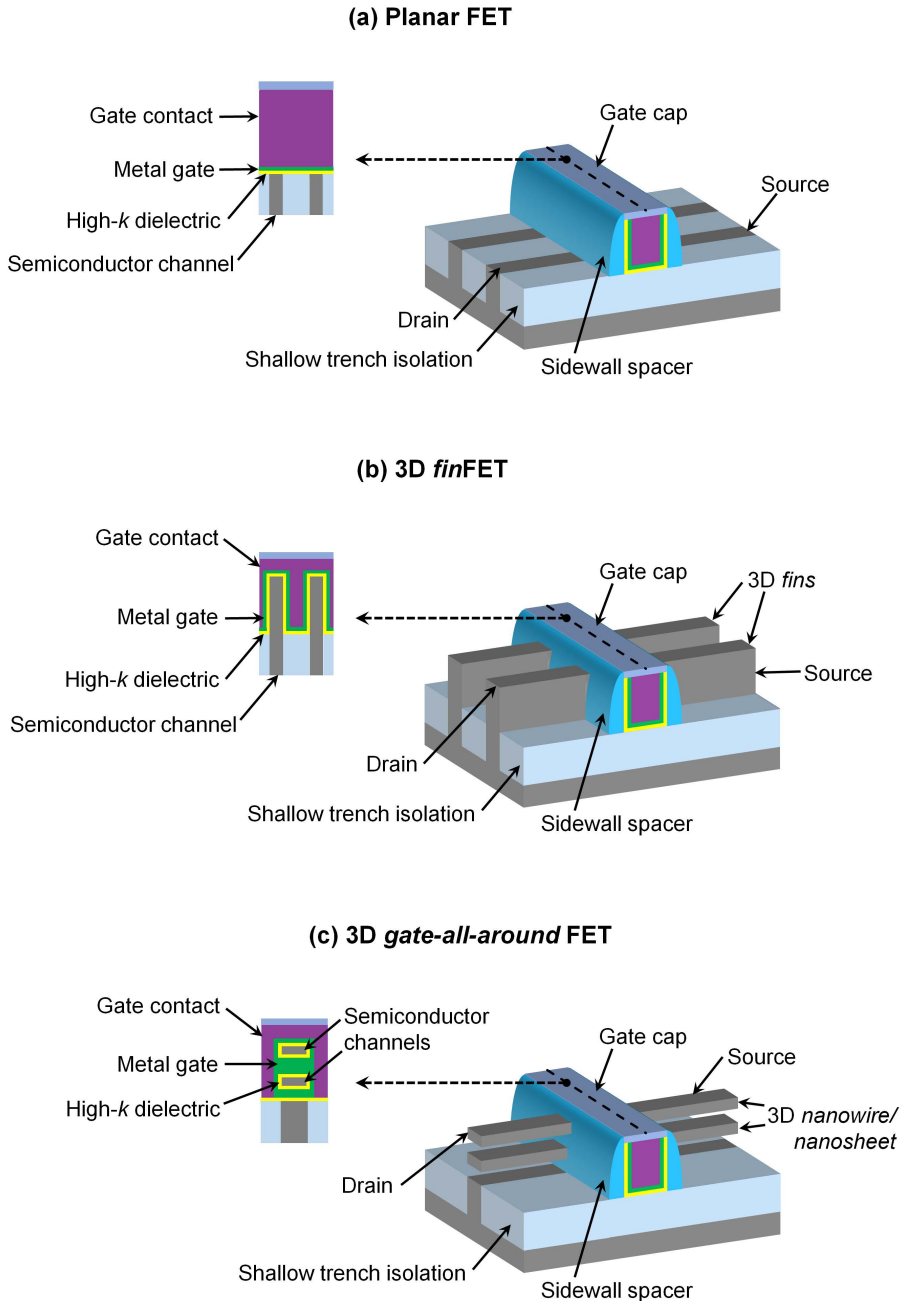
Figure 4. Schematic of **(a)** a planar field-effect-transistor (FET), **(b)** three-dimensional (3D) *fin*FET and **(c)** 3D *gate-all-around* FET. Schematic cross-sections are also shown for each FET illustrating details of the semiconductor channel and high-k-metal-gate stack when viewing the gate stack in a direction parallel to the channel.

semiconductor industry that has yielded state-of-the-art logic processors comprising billions of transistors on a single die.[22,23] One of the early strategies involved strain engineering whereby the silicon in the source and drain regions was mixed with germanium.[24] This physically squeezed (or compressed) the silicon in the channel region that altered its crystalline and hence, electrical properties. This improved hole mobility in the PMOS channels which lowered channel resistance and waste heat generation (i.e., improved energy efficiency). Conversely, subjecting NMOS channels to tensile stress improved electron mobility. A subsequent technique involved the adoption of new functional materials for the gate stack – a high-*k* gate dielectric (e.g., HfO_2) and metal gates with optimum work function (e.g., TiN gate for PMOS, TiAlN gate for NMOS).[25,26] This lowered leakage current from the tunneling of electrons between the gate and the channel through the previous gate oxide layer (SiO_2) that was a comparatively lower *k* dielectric.[25] Although these new materials helped staunch a main source of leakage current, continued device scaling to a gate length below 30 nm caused the leakage between the source and the drain to become a significant issue when the transistor was in its OFF state.

A way to regain control over channel current flow was to incorporate a new design architecture by raising the channel above the plane of the silicon substrate. This led to the formation of a 3-dimensional "*fin*" structure that is characteristic of the 3D *fin*FET design, which is shown in Figure 4b.[16,27–30] The gate wraps around the fin on three sides of the raised 3D channel, instead of only across one side of a planar 2D channel. This allows the gate to have a better electrostatic control of the electric field in the channel, which reduces leakage current between source and drain. An additional benefit is the need for a lower gate voltage to switch the transistor which lowers power consumption. State-of-the-art logic processors are manufactured using the 3D *fin*FET design. An evolution of this 3D design architecture is the 3D *gate-all-around* FET which is shown in Figure 4c.[1,31,32] In this device, the gate electrode is wrapped around all of the sides of the channel region. This enhances the electrostatic control of the electric field in the channel provided by the aforementioned 3D *fin*FET design which can further improve transistor energy-efficiency and reduce power consumption. The electrostatic control of the channel by the gate is so efficient in such *gate-all-around* architectures that it is even possible to fabricate a MOSFET device without forming p–n junctions between the source, the channel region and the drain. Such "junctionless" multigate transistors have the potential to greatly simplify the fabrication process of MOSFET devices.[33]

2.3 Emerging non-volatile memory devices

While logic circuits process instruction and/or data sets, memory circuits store these information sets awaiting processing.[14] The data is stored in the form of bits in a memory cell that can again be represented by the two-state characteristics of an electrical circuit, e.g., charged/discharged state of a capacitor, orientations of a magnetic domain in

ferromagnetic components, etc.[14,34] Memory is a quite generic term with different meanings depending on the context. The Von Neumann architecture used in modern computing systems introduced a distinction between primary (or main) memory, for storage of instructions to be executed and data being processed, and secondary memory for mass storage of both instructions and data not needed in the short term.[35] This distinction follows an arrangement called memory hierarchy, shown in Figure 5, which is based on the locality (i.e., proximity to CPU) and performance of memories in terms of their capacity and access time (i.e., read/write latency).[34,36,37] Plus, the distinction between memory and storage can also be considered to be quite fluid. More functional classifications distinguish between whether memories are volatile or non-volatile, static or dynamic, random or sequential, of a high or low endurance, bit-alterable and bit-addressable. If the data in memory is retained through application of constant power, then it is termed as volatile whereas non-volatile memories can retain data even after the power is turned off.[38] When a memory cell undergoes data leakage (e.g., slow discharge of a capacitor), it needs to be periodically refreshed (i.e., read and re-written) to retain the stored data.[39] This is known as a dynamic memory and it consumes extra power and requires high endurance (i.e., can undergo many write/erase cycles before device failure)[40] in contrast to static memories that do not need to be refreshed. Random access memories allow data to be read or written in the same amount of time irrespective of the physical location of data in memory. It is therefore faster compared to sequential access memory where the data is read in the order that it was stored. A bit-alterable memory is one in which stored data can be directly overwritten with new data without requiring the existing data to be erased beforehand.[41] A bit-addressable memory allows access to individual bits of data instead of only larger datasets composed of multiple bits.[34,42] Current baseline memory technologies include static random access memory (SRAM), dynamic random access memory (DRAM) and flash memory while hard disk drives are used for long term mass storage of data. Modern computing systems make use of a hierarchy of these different memories to achieve an optimal trade-off between cost, performance and memory capacity (Figure 5).[36]

Lying at the top of the memory hierarchy is the SRAM which forms the integrated or embedded memory components of the CPU (e.g., on-chip registers, cache) and is fabricated concurrently with the logic circuits.[43] It is located closest to the logic processor and is used to store the most frequently accessed instructions and data. This together with the static nature of SRAM gives it the fastest possible operation speed (read/write latency ~ 1/1 ns, see Table 1)[44,45] that is achieved by using six FETs to form a two-state flip-flop configuration for storing data bits. However, this configuration makes SRAM occupy a large portion of the chip area, which consequently lowers the bit density (number of bits that can be stored per unit chip area) and makes it the most expensive memory. Therefore, most of the data awaiting processing is stored off-chip in a different memory device known as DRAM. This constitutes the main memory of a

Non-volatile
Random access
Low latency
High bit-density
High endurance
Long retention
Bit-alterable
Bit-addressable
Low cost
....

On-chip (embedded)

Off-chip

New memory needed

SRAM (registers, cache)

DRAM (main memory)

2D/3D NAND Flash, NOR Flash (secondary long term memory)

Hard disk drive (long term mass storage)

Volatile

Non-volatile

Increasing latency & capacity

Increasing cost

Figure 5. Memory hierarchy depicting the multiple categories of memory found in modern computing systems to achieve an optimal trade-off between cost, performance and capacity. It outlines the need for new on-chip and off-chip memory technologies with the necessary characteristics required to fulfill the demands of future embedded or stand-alone electronic device applications.

Table 1. Key device parameters and performance metrics comparing various volatile and non-volatile memory technologies[44–46,58,142]

	SRAM	DRAM	PCRAM	STT-MRAM	RRAM	Flash	HDD
Volatility	Volatile		Non-volatile				
Access	Random					Sequential	
Bit-alterable	Yes					No	Yes
Bit-addressable	Yes					No	Yes
Read latency	~ 1 ns	~ 30 ns	~ 20-50 ns	~ 2-20 ns	< 50 ns	~ 50 ns	~ 3 ms
Write latency	~ 1 ns	~ 50 ns	~ 50-120 ns	~ 2-20 ns	< 100 ns	> 1 ms	~ 10 ms
Write energy	~ 1 fJ	~ 10 fJ	~ 10 pJ	~ 1 pJ	~ 1 pJ	~100 pJ	~ 0.5 µJ
Endurance	> 10^{16} cyc	> 10^{16} cyc	10^{10} cyc	10^{15} cyc	10^9 cyc	10^5 cyc	> 10^{16} cyc

computing system and is located in a separate chip connected to the CPU. The memory cell in DRAM consists of a dielectric sandwiched between two metals, i.e., a capacitor configuration where data is stored in terms of the charged/discharged state of a capacitor. This allows DRAM to have a significant advantage over SRAM in terms of memory density and cost. However, it has a comparatively higher access time (read/write latency ~30/50 ns, see Table 1)[45] compared to SRAM since, in addition to being located in a separate chip, DRAM is a dynamic memory that needs to be periodically refreshed to overcome capacitor leakage currents. Furthermore, both DRAM and SRAM are volatile memories that require a power supply at all times to hold on to their information state. This is acceptable for stand-alone devices with a dedicated power source but places a significant drain on the battery of portable electronic devices. The advent of such devices, e.g., laptops, smartphones, tablets, etc., led to the need for a non-volatile memory with a large bit density and low latency. Although hard disk drives can, in principle, serve the purpose of non-volatile information storage, they are very slow (read/write latency ~10/10 ms, see Table 1)[37,46] owing to sequential data access on a mechanically rotating disk, which also makes the device susceptible to failure.

Solid-state drives based on flash memory technology e.g., NAND or NOR flash, are devoid of any mechanically moving parts and are non-volatile devices where information is stored in terms of the presence/absence of trapped charges. Flash memory cells are based on a layer stack constituting a floating layer (metal or dielectric) sandwiched between two layers of a blocking and tunneling dielectric.[47] This stack is inserted between the gate contact and semiconductor channel of a transistor device (replacing the metal gate layer with optimum work function and the gate dielectric layer, discussed in the previous section). When a current flows across the channel from the source to the drain, applying a voltage on the gate contact causes the mobile charge carriers to tunnel through the tunneling dielectric and be trapped in the floating layer. The trapped charges allow information to be retained even when the power is switched off and confer flash memories with non-volatility. The bit density per unit chip area for planar flash memory is comparable to that of DRAM but can be significantly increased by stringing together memory cells in the third dimension, e.g., 3D NAND flash. Over there, memory cells are added in series by going vertically upwards in a columnar fashion instead of out to the side in horizontal rows. However, charge transport via tunneling is responsible for gradually wearing out the tunnel dielectric because of trap creation and interfacial damage. As a result, there might be charge trapping/untrapping in the tunneling dielectric or undesired charge flowing into/from the storage layer which lowers flash memory endurance. To account for limited endurance, all writing algorithms are based on a sequence of write/erase pulses followed by a verify operation. This sequence proceeds until the expected amount of charge is correctly transferred to/from the storage layer.[47] As a result, flash memories are sequential instead of

random access. Without write and verify algorithms, it would be very difficult to control the actual amount of charge transferred to/from the storage layer and multi-level cell architectures for flash memory would not be feasible. This causes flash memories to have a very high write latency ($\sim$ 1 ms)[45,46] while its read latency ($\sim$ 50 ns)[45] is comparable to that of DRAM (see Table 1). Furthermore, flash memories contain information organized in pages and blocks, where a block is the smallest erasable unit and it contains multiple logical pages. A page is the smallest addressable unit for reading and writing data and is composed of multiple data bits.[48] Hence, flash memories are significantly slower than SRAM or DRAM and are neither bit-alterable nor bit-addressable, so they do not provide the performance generally required for main memory. The non-volatility, high bit density and subsequently low cost of flash memory has led to its adoption in virtually all portable electronic devices. However, the advent of artificial intelligence (AI) and rise in data-intensive workloads spanning a broad spectrum of applications – such as the internet of things (IoT), virtual/augmented reality (VR/AR), big data analytics, autonomous vehicles, etc.[23,49–53] – demand not only faster processing of a large amount of data but also a faster access to it. This is driving the need for a new memory in both embedded and off-chip platforms that can overcome the limitations of flash and combine it with the advantages of SRAM and DRAM (Figure 5). Such an all-purpose optimum memory is yet to be defined but out of several emerging technologies, three are vying closely for that contention. These include phase change random access memory (PCRAM), magnetoresitive random access memory (MRAM) and resistive switching random access memory (RRAM), which are schematically illustrated in Figure 6a, b and c, respectively. All three memories are non-volatile, low latency, random access, bit-alterable and bit-addressable memories that do not require periodic refreshing and have a high endurance (compared to flash).

PCRAM makes use of a reversible phase transformation between the high-resistance amorphous state and the low resistance crystalline state of a phase change material (PCM) to store information.[54] A PCM layer, e.g., chalcogenide glass composed of an alloy of germanium–antimony–tellurium (GeSbTe or GST), is sandwiched between two electrodes (Figure 6a) and the phase transformation is triggered by Joule heating and cooling of the material in a controlled manner using electrical current pulses. To attain the amorphous phase, the bulk or a portion of the PCM is first melted and then quenched rapidly by applying a large electrical current pulse for a short time period. The amorphous region of the PCM has a high resistivity corresponding to the OFF state ("0" bit) of the memory cell. For obtaining the crystalline phase that has a low resistivity corresponding to the ON state ("1" bit) of the memory cell, a comparatively lower electrical current pulse is applied to anneal the amorphous region of the PCM at a temperature between the crystallization temperature and the melting temperature. This is performed for a time period long enough to crystallize the PCM layer. To read the
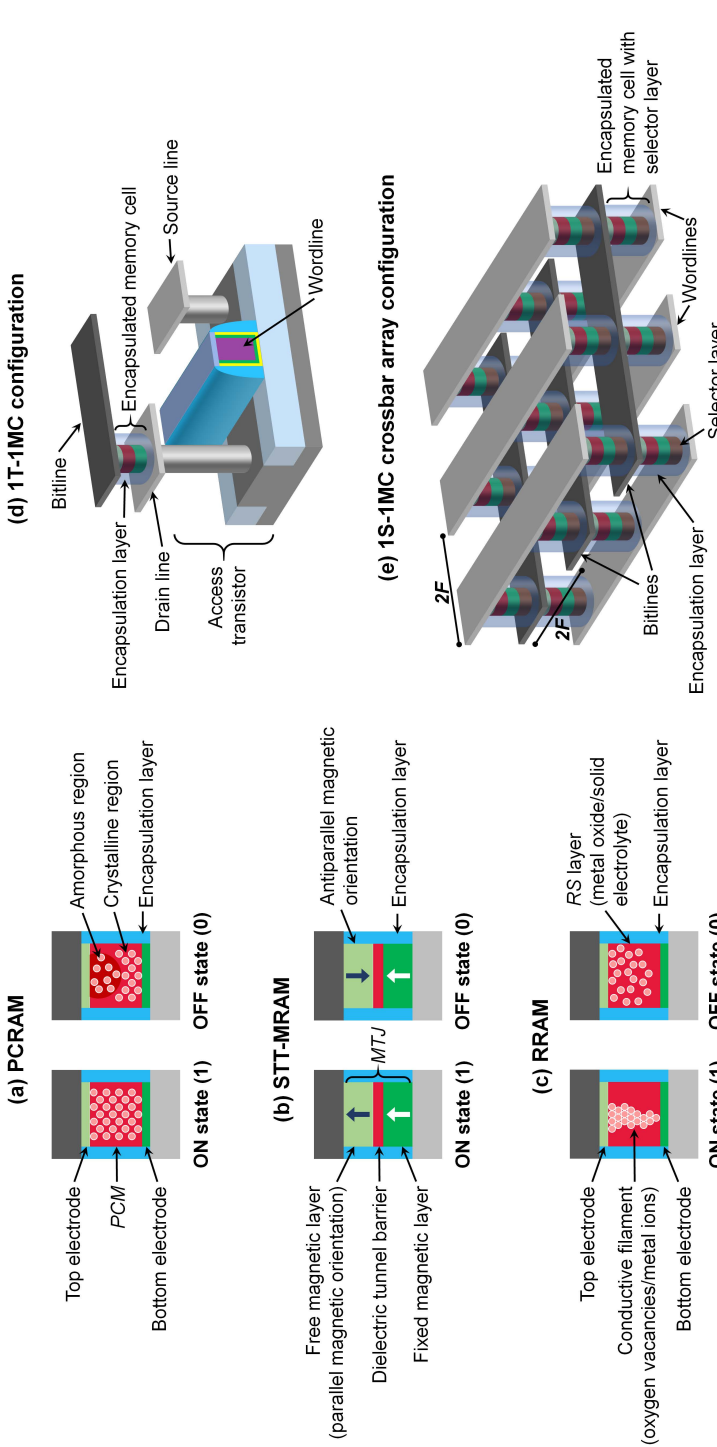
Figure 6. Schematic cross-sections illustrating details of **(a)** phase change random access memory (PCRAM), **(b)** spin-transfer-torque magnetoresistive random access memory (STT-MRAM) cell with a magnetic tunnel junction (MTJ) and **(c)** resistive switching random access memory (RRAM) cell with a resistance switching (RS) layer in their "ON" and "OFF" states representing stored bits of "1" and "0", respectively. Schematic of encapsulated non-volatile memory cells constituting either a PCM, MTJ or RS layer in a **(d)** one transistor-one memory cell (1T-1MC) configuration and a **(e)** one selector-one memory cell (1S-1MC) crossbar array configuration in a 3D stacked two-layer cell architecture where cell dimensions are indicated in terms of the bitline pitch (2F) and wordline pitch (2F).

state of the PCM layer, the resistance of the cell is measured by passing an electrical current small enough not to disturb the currently programmed state. Compared to SRAM or DRAM, PCRAM has a lower endurance, higher latency and higher energy consumption that makes it less attractive as a replacement for these two memories (see Table 1).[44–46,55] Although the write operation of PCRAM consists of an inherent wear-out mechanism of the PCM due to movement of atoms during phase transformation, it still has a much better endurance ($\sim 10^{10}$ cycles) and faster access times (read/write latency ~20-50/50-120 ns) compared to flash memory (see Table 1).[44,55,56] It is currently the most mature out of the three emerging non-volatile memory technologies to date and has been recently adopted for commercial high-volume manufacturing.[57]

MRAM relies on the tunnel magnetoresistance switching effect between the mutually parallel and antiparallel magnetic orientations of ferromagnetic layers in a magnetic tunnel junction (MTJ) as a means for storing information. The MTJ consists of an ultrathin dielectric layer (e.g., MgO) that acts as a tunnel barrier sandwiched between two ferromagnetic metal layer stacks (Figure 6b). To perform a write operation, the direction of magnetic alignment of one ferromagnetic layer stack (free layer composed of e.g., Ru/Ta/CoFeB stack) can be altered by using a magnetic field (field-driven MRAM) generated by an electric current, or by using the spin-transfer-torque effect (STT-MRAM) generated by a spin-polarized electric current.[56,58] A spin-polarized current can generate a torque to switch the magnetic moment of a ferromagnetic layer through the transfer of angular momentum, thus reorienting its magnetic alignment.[56,58] The direction of magnetic alignment of the other ferromagnetic layer stack (pinned layer composed of e.g., CoFeB/Ru/CoFe/PtMn/Ta) remains unchanged during this operation.[56] When the magnetic alignments of the two ferromagnetic layers are not parallel (i.e., antiparallel) to each other, the MTJ has a high resistance that leads to a low tunneling current through the tunnel barrier and corresponds to the cell's OFF state ("0" bit). The parallel magnetic orientation of the two ferromagnetic layers has a low resistance that leads to a higher tunnel current and corresponds to the memory cell's ON state ("1" bit). In order to perform a write operation in STT-MRAM, a high voltage bias is applied to the bitline generating a current that switches the device between parallel and antiparallel states by the STT mechanism.[58] A positive voltage bias leads to switching from an antiparallel to a parallel state while a negative voltage bias reverses the states. A lower bias voltage is used to perform a read operation by measuring the magnetoresistance of the MTJ which refers to the percentage change in resistance between parallel and antiparallel magnetization alignment of the ferromagnetic layers in a MTJ. Although STT-MRAM has endurance and latency approaching those of SRAM and needs only one transistor per bit compared to six per bit for SRAM, the write current density and consequently, write energy is still quite high for embedded memory applications (see Table 1).[44] Still, it is thus far the only non-volatile memory technology

(besides hard disk drives) to have very high endurance since there is no inherent magnetic wear-out mechanism for switching magnetic orientations, unlike PCRAM or RRAM (see below) where atoms migrate during write operations.[58] However, an electrical wear-out mechanism consisting of the dielectric breakdown of the tunnel barrier exists which can be avoided by keeping the write voltage across this barrier sufficiently low. STT-MRAM has also been reported to be a mature non-volatile memory technology that is soon going to enter high-volume manufacturing.[59–61]

The term RRAM can be considered to be an umbrella nomenclature for any non-volatile memory device where information is stored by switching between the high and low resistance states of an active material (or stack of materials) by inducing a change in its properties.[34] In this regard, one could even consider both PCRAM and MRAM to be subsets of a non-volatile RRAM device.[45] However, RRAM has been generally used in the literature to refer to non-volatile memory cells composed of a dielectric layer, such as a metal oxide or a solid electrolyte, sandwiched between two conducting electrodes to form a metal-insulator-metal (MIM) stack (Figure 6c).[62–64] The basic working principle of a RRAM device is the reversible formation and rupture of electrically conductive pathways, in the form of atomically thin filaments that shunt the two electrodes through the dielectric layer on applying a voltage bias on those electrodes.[62–64] In metal oxide RRAM, the filaments are formed by the migration of oxygen vacancies in the oxide layer (e.g., Ta_2O_5)[65] while in conducting bridge RRAM, the filaments are formed by the dissolution of an active electrode (e.g., Cu or Ag) in an oxide or chalcogenide based solid electrolyte (e.g., GeS_2).[34] In general, a one-time high voltage bias electroforming step needs to be applied on a pristine RRAM device for the creation of conductive filaments, composed of either oxygen vacancies or metal ions, in the dielectric layer. The connection of the two electrodes by these filaments through the dielectric gives the resistance switching layer a low resistivity that corresponds to the ON state ("1" bit) of the memory cell. The rupture of filamentary pathways in the dielectric material connecting the two electrodes give the resistance switching layer a high resistance that corresponds to the OFF state ("0" bit) of the memory cell. For a unipolar RRAM, the high and low resistance states are written by controlling the applied voltage amplitude and not the polarity, such that both resistance states can be written at the same bias polarity.[62–64] For a bipolar RRAM, the resistive switching is performed by varying the bias voltage polarity where the low resistance state can be written at one bias polarity while the high resistance state can be written using the reverse bias polarity.[62–64] RRAM is known to undergo cycle-to-cycle and device-to-device variation owing to the stochastic nature of the conductive filament formation process. Research is currently focused on the formation of filaments in a controlled and deterministic manner in order to improve the viability of RRAM as an embedded non-volatile memory.[44] On the other hand, the energy consumed in storing data in RRAM is lower than that of PCRAM while its

endurance and latency are on par with those of PCRAM (see Table 1).[44] Furthermore, metal oxide RRAM can also be easily integrated with logic circuitry and manufactured using existing CMOS fabrication processes without the need for any special equipment or materials.

These non-volatile memory devices are generally located between an array of two orthogonal interconnects – representing memory address lines known as the bitline and the wordline – lying in upper and lower planes that are parallel to each other.[34,43,66] A memory cell is accessed by applying voltages to its corresponding bitline and wordline. However, the memory cells that are not accessed can form a large number of sneak paths in parallel with the path through the selected cell.[34,54,66–68] This can lead to the flow of leakage current through those sneak paths during memory access that can compromise the information being read/written. In order to account for the impact of sneak paths, memory access or selector devices need to be inserted at every junction in series with the memory cell. This is usually performed using an access transistor which leads to the one transistor-one memory cell (1T-1MC) configuration shown in Figure 6d.[34,43,45,69] Note that in the 1T-1MC configuration, the memory cell lies in the vicinity of the bitline and wordline crossover point. This configuration leads to the memory density to be limited by the dimensions of the access transistor.[45,54] A means of increasing the density is to make use of a one selector-one memory cell (1S-1MC) crossbar array configuration shown in Figure 6e.[34,45,54,66–69] Unlike before, memory cells in series with selector devices are placed directly at the intersection point of the bitline and wordline crossbar array. To enable functional memory operation, key requirements for selector devices include providing a strong asymmetric or non-linear electrical behavior that allow access to the targeted cell in the memory array without affecting or being affected by the other cells. Asymmetry can be provided by rectifying diodes while non-linearity can be obtained by non-ohmic transport mechanisms (e.g., tunneling[67,70]) or volatile switching phenomena (e.g., ovonic threshold switch,[71] Mott transition switch[72]). Provided the memory cell is not larger than the width of each line or the space between, assumed equal to F which is the minimal feature size usually given by the lithography resolution, then the line pitch (width of a line and the space between lines, Figure 6e) is $2F$ giving an effective memory cell area of $4F^2$. This yields the smallest possible single layer memory cell footprint.[34,43,66,68,69] The 1S-1MC crossbar array makes it feasible to stack multiple 2D memory cell layers in a 3D architecture. Doing so results in the minimal feature size being reduced further to $4F^2/n$ where n is the number of stacking layers. This allows stacked 3D 1S-1MC crossbar arrays to be a promising architecture for high density and large capacity non-volatile memory devices that could compete with large, high-density 3D NAND flash memory applications. However, a drawback associated with stacked 3D crossbar arrays is that the cost per bit does not usually scale with the increasing number of layers since it requires critical process steps, e.g., lithography and

etching of metal lines and via contacts for each additional memory layer.[68] This introduces extra process complexity and increases the fabrication cost. The maximum number of stacking memory layers yielding a cost-effective 3D crossbar memory device has been reported to be about eight.[73] In contrast, a single critical lithography and etching step is used to define memory cells on different layers of a 3D NAND flash memory device.[74] Consequently, stacked 3D 1S-1MC crossbar arrays face challenges in competing with 3D NAND flash solely based on cost. It is now generally agreed that the vision of an all-purpose 'universal memory' is not realistic. Application-driven design requires the optimization of performance at each level of the memory hierarchy which necessitates trade-offs in device characteristics. Therefore, the trade-off between cost, performance and capacity of the emerging non-volatile memory technologies will determine their implementation in future embedded and stand-alone device applications where they will either replace or supplement existing technologies in the memory hierarchy.[46]

2.4 Key challenges from a deposition perspective

Although multiple patterning using LELE and SADP has been used for device scaling since the 22 nm *fin*FET logic node to overcome technological limitations of 193 nm immersion photo-lithography,[75] SAQP is being used for scaling devices to the upcoming 10 nm logic node even though it involves extra steps and longer cycle times.[76] This is mostly due to the challenges involved in using EUV photo-lithography which could, in principle, pattern the critical dimensions (CD) of features in the state-of-the-art 14 nm logic node in fewer steps compared to SAQP. These include low EUV source power, high system maintenance downtime, high line edge and line width roughness (LER/LWR) in photoresist patterns from EUV photon shot noise, difficulty in obtaining defect free EUV masks and EUV-transparent, robust pellicles, etc.[6–8,77] All these contribute toward making feature patterning using EUV lithography systems highly challenging and much more expensive to use (on a per wafer basis) than 193 nm immersion lithography tools for high-volume manufacturing.[22] It is speculated that EUV lithography is likely to be implemented in future sub-10 nm logic nodes mostly in patterning cuts and vias in a single step on pre-patterned features obtained using SAQP, thereby reducing the costs incurred in multiple patterning.[22,78,79]

As mentioned before, a key requirement for self-aligned multiple patterning is the deposition of spacer material, typically SiO_2, with a conformal sidewall thickness profile on pre-defined features, essential for transferring patterns to the underlying layer with high fidelity.[80] The spacer deposition typically has to occur at low temperature because temperature sensitive materials are generally used where the residual stress of the deposited spacer also needs to be taken into account.[81] Thermal and plasma-enhanced

atomic layer deposition (ALD) are well-known methods for growing thin films with excellent growth control that yield conformal films on surfaces with three-dimensional (3D) features.[82–84] Thermal ALD of SiO_2 is challenging and generally requires high temperatures, while plasma ALD of SiO_2 is a comparatively faster and simpler process that can be performed at a low temperature.[85,86] It is interesting to note that the use of plasma ALD for self-aligned multiple patterning has currently become the biggest of all individual ALD markets, indicating the importance of its role in the continuation of device scaling.[87] There are many possible processing schemes for SAQP due to the increased number of steps and the involvement of several sacrificial layers of different materials. Figure 7 shows images of two general SAQP process schemes, described in the previous section, where plasma ALD was used to deposit conformal spacer layers twice in each scheme.

In the SAQP using two hard mandrels scheme (Figure 7.I.a-g), plasma ALD of SiO_2 was used to obtain two conformal spacers ($\sim$16 nm for the first and $\sim$10 nm for the second) on two etched hard mandrel features (amorphous carbon and amorphous silicon).[9–11] The final features obtained after SAQP had a line CD, CD non-uniformity (CDU) and LWR of 7 nm, 0.5 nm, and 1.2 nm, respectively, which is comparable to the specifications (line CD, CDU and LWR of 7 nm, 0.5 nm and 1.4 nm, respectively) required for the corresponding parameters in next-generation 7 nm *fin*FET logic nodes.[9] Instead of using two ALD SiO_2 spacers on two hard mandrels, ALD SiN_x has also been used as the second spacer on the second hard mandrel (amorphous silicon) for such an SAQP scheme, indicating the flexibility of materials that can be used in this process.[81] Furthermore, in SAQP using the *spacer-on-spacer* scheme (Figure 7.II.a-f),[12,13] either thermal or plasma ALD of TiO_2 was used to deposit the second spacer on free-standing structures of the first spacer obtained after etching back a conformal layer of SiO_2 deposited directly on an organic mandrel by plasma ALD. The final feature pattern was obtained by removing the first spacer (SiO_2) selectively with respect to the second spacer (TiO_2) and the underlying layer (amorphous Si), and then transferring the pattern formed by the free-standing structures of the second spacer to the underlying layer. It was found that using plasma ALD to deposit the second TiO_2 spacer instead of thermal ALD yielded smoother final features (in terms of lower line width/edge roughness, LWR/LER).[13] Furthermore, the first SiO_2 spacer was deposited directly on an organic photoresist at room temperature, indicating how plasma ALD becomes the go-to method for providing low temperature processing environments.[13] Compared to the standard SAQP scheme using two hard mandrels, the advantage conferred by the spacer-on-spacer approach includes avoiding the use of any sacrificial layers and the need for fewer processing steps, which has been reported to lower production costs by more than 25%.[13]
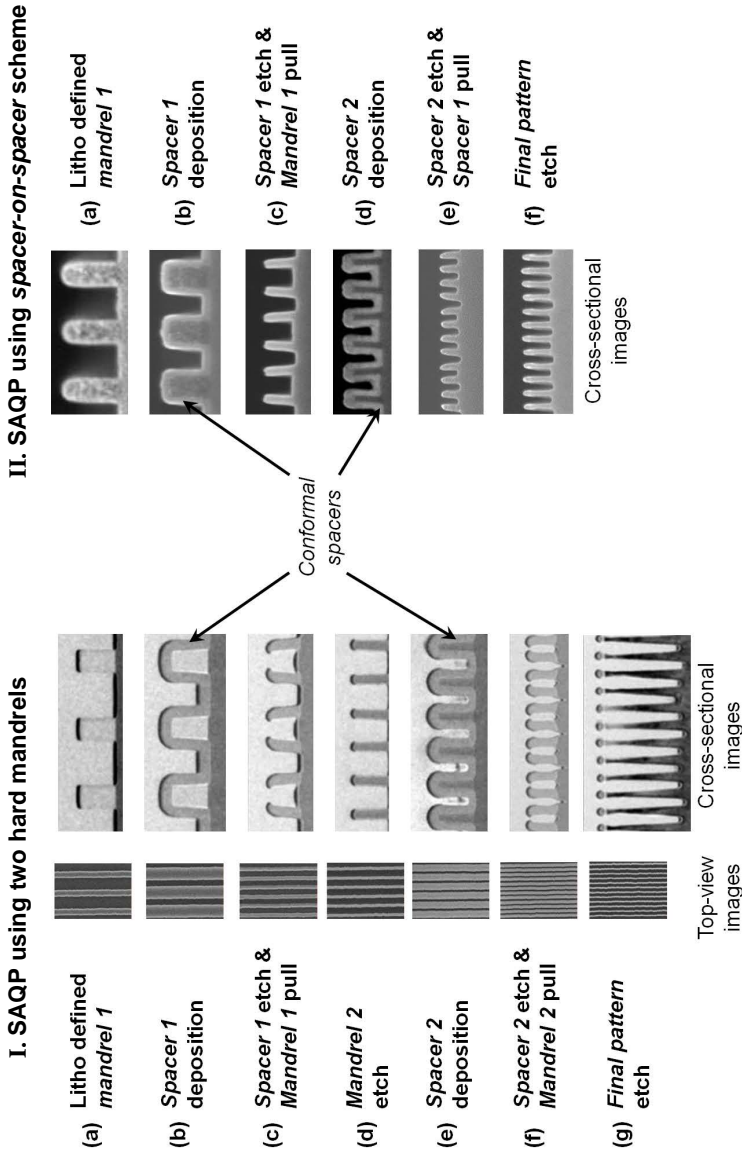
Figure 7. I.(a)-(g) Top-view and cross-sectional images depicting the steps employed in a self-aligned quadruple patterning (SAQP) process using two hard mandrels.[9-11] The top-view images illustrate the formation of smooth features (low critical dimension non-uniformity, CDU; low line width roughness, LWR) at each step of the patterning process. **II.(a)-(f)** Cross-sectional images depicting the steps employed in a SAQP process using spacer-on-spacer scheme.[12,13] Steps **I.(b)**, **I.(e)**, **II.(b)** and **II.(d)** denote how deposition of conformal spacers on the sidewalls of patterned features form a crucial aspect of these processes.

As mentioned in the previous section, one of the techniques used to continue transistor scaling involved adopting an ultrathin layer of a high-*k* dielectric material (e.g., HfO$_2$) as a replacement for the traditionally used SiO$_2$ gate dielectric. A key feature of using SiO$_2$ as the gate oxide was that an ultrathin layer (~1.2 nm) of high quality material could be obtained simply by high temperature thermal oxidation of the silicon substrate, whereas a high-*k* dielectric layer of comparable thickness needs to be deposited on the silicon substrate. Several methods such as reactive sputtering and metal organic chemical vapor deposition (MOCVD) were explored for growing high-*k* oxide layers on silicon.[25] However, these continuous deposition processes did not provide adequate thickness control necessary for growing layers 1 – 3 nm thick in a uniform manner on large area substrates. These processes also yielded oxide layers on silicon with a high interface defect density that trapped charges during transistor operation, thereby inducing variations in the threshold voltage needed to switch the transistors.[25] This resulted in an undesired phenomenon where the devices behaved differently every time they were switched. All these factors contributed to the need for implementing a processing technique that could deposit a few nanometers of a high-*k* dielectric film uniformly over large area substrates and with sufficiently low interface defect density.

Being a deposition technique capable of angstrom level thickness control, ALD made its debut in CMOS chip fabrication by enabling uniform growth of ultrathin high-*k* dielectric films over large area substrates and with very low interface defect density, thus improving device performance.[25] Later on, as transistor scaling entered the third dimension with the advent of *fin*FET architectures where 3D silicon *fins* constituted the semiconductor channel, another key attribute of ALD that enabled conformal layers on 3D topographies became indispensable for growing ultrathin high-*k* dielectric films. Figure 8a shows a cross-sectional image of the gate stack in a 14 nm node commercial *fin*FET device viewed parallel to the semiconductor channel.[88,89] An ALD grown 1 – 2 nm thick layer of high-*k* dielectric (HfO$_2$) can be observed to conformally wrap around the tapered silicon fin. At this point, it is also worth noting that the shift to a high-*k* metal gate stack also involved the use of a metal gate with optimum work function (e.g., TiN gate for PMOS or TiAlN gate for NMOS) as replacement for doped polycrystalline silicon.[45,90] The metal layers for optimizing work function could be grown by means of sputtering for planar FETs. However, the shift to *fin*FETs necessitated the use of ALD for also growing conformal metal gate films (1 – 2 nm thick) on 3D architectures.[90–94] Thermal ALD has generally been used to grow the high-*k* dielectric and metal gate layers to avoid creating potential electronic defects arising from the use of plasma ALD. However, cases have been reported where good device performance was achieved using plasma ALD, e.g., growth of a HfO$_2$/Al$_2$O$_3$ stack as the high-*k* dielectric by plasma ALD on InGaAs high-mobility channel planar FET.[95,96] Furthermore, the high-*k* metal gate stack is typically grown after the dopants have been implanted to form the S/D regions,

(a) Parallel to channel

(b) Perpendicular to channel
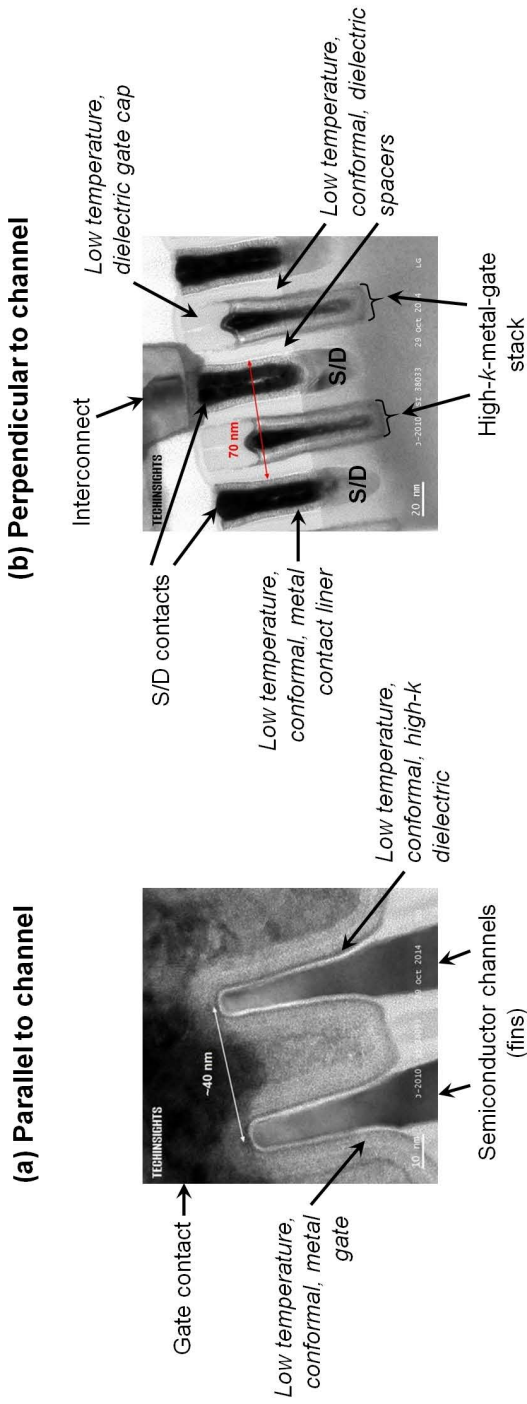
Figure 8. Cross-sectional images of a 14 nm node *fin*FET device[88,89] as viewed (**a**) parallel to the semiconductor channels and (**b**) perpendicular to the semiconductor channels (*fins*). Image (**a**) shows the need of depositing conformal layers of high-*k* dielectric and metal gate films on the semiconductor fin. Image (**b**) depicts the need for depositing conformal layers of thin metal contact liner on the source/drain (S/D) regions of the fin and conformal, thin dielectric spacers on the sidewall regions of the high-k-metal gate stack. Image (**b**) also shows the need for depositing a dielectric cap on top of the gate stack in a gapfill process. All these materials have to be deposited in low temperature (< 400 °C) environments.

in a technique known as the *gate-last* process.[92,97] As a result, the high-*k* metal gate stack requires a low temperature ($< 400\,^\circ$C) processing environment in order to prevent interlayer diffusion of dopants or interfacial reactions between layers at elevated temperatures.[97,98] Plasma ALD can fulfill this requirement by enabling film growth at low temperature owing to the high chemical reactivity of the plasma species.[83]

Figure 8b shows a cross-sectional image of the gate stack in the same 14 nm node commercial *fin*FET device viewed perpendicular to the semiconductor channel.[88] It illustrates additional functional layers that are currently grown or have the potential to be grown by low temperature plasma ALD processes for state-of-the-art or next-generation *fin*FET devices, respectively.[99] These include gate spacers, gate caps and S/D contact liners.[99] The gate spacers are dielectric layers (e.g., SiN_x, SiO_2) on the sidewalls of the gate stack.[92] They serve multiple purposes that range from preventing shorts between the gate contact and S/D contacts to being a barrier against oxygen ingress and dopant out-diffusion.[92,100–103] They also provide a constant spacing of the source and drain of the transistor independent of transistor pitch and prevent any etch damage to the gate stack during subsequent processing steps.[92,100–103] All these require the spacer films to be highly conformal and etch resistant.[100–102] The gate caps are also dielectric layers (e.g., SiN_x) grown on top of the gate contact that also prevent shorts between the gate contact and S/D contacts.[104,105] Together with the gate spacers, they act as etch stop layers protecting the gate stack when S/D contacts are formed by the self-aligned contact etching technique (discussed later).[104,105] These spacer and capping layers have generally been deposited using thermal or plasma-enhanced chemical vapor deposition (PECVD).[92,99,106] However, as feature dimensions become smaller and more densely packed in next-generation (≤ 10 nm) transistor nodes, plasma ALD has been reported as a potential candidate for obtaining gate spacers and capping layers in those scaled devices.[92,99,106] The S/D contact liners are conductive layers (e.g., TiN_x) that act as diffusion barriers preventing migration of contact metal atoms (e.g., W, Co) while also maintaining low resistance pathways for current flow between the contact and the S/D regions.[98,99,105,107] Plasma ALD has also been reported as a potential candidate for growing such layers owing to the high densities and low resistances obtained for contact liner films deposited with this technique at low temperature.[83,98]

Figure 9a, b and c show cross-sectional images of PCRAM, STT-MRAM and RRAM devices, respectively, illustrating functional layers discussed before (see previous section and Figure 6). Figure 9 also illustrates the presence of a particular layer common to all three devices, namely the dielectric encapsulation layer (e.g., SiN_x, SiO_2) for the memory cell,[108–110] The encapsulation layer, similar to the gate spacer discussed above, is a relatively thin conformal layer grown on the memory cell sidewalls that protects those cells during subsequent processing steps and aids in electrically isolating cells from

each other. In order for these emerging memory devices to be easily integrated with logic circuitry and manufactured using existing CMOS fabrication techniques, a low temperature processing environment ($< 400\ ^{\circ}$C) again forms a key requirement for encapsulating memory cells. As a result, the memory cell encapsulation layers are currently grown or have the potential to be grown by low temperature plasma ALD.[99,111,112] For the commercial PCRAM device having a 1S-1MC 3D crossbar array configuration shown in Figure 9a, low temperature plasma ALD has been reported for growing SiO_2 as the conformal dielectric encapsulation layer for the memory cell columns consisting of the PCM and selector layers.[99] TEM analyses recently reported by TechInsights reveal a bitline pitch of about 40 nm for this device, based on which the thickness of the conformal encapsulation layer can be estimated to be about 5 nm.[113] After the memory cell columns have been encapsulated, gaps (with aspect ratio $\sim$ 12 : 1 estimated from Figure 9a) remain between adjacent cell columns which are subsequently filled with a dielectric. The dielectric gapfill has also been reported to be grown using a low temperature SiO_2 plasma ALD process.[99] This serves to electrically and thermally isolate the PCMs in adjacent cells during read/write operations based on joule heating.[108]

Figure 9b shows encapsulation of a patterned MTJ stack in a STT-MRAM device using a conformal dielectric encapsulation layer, estimated to be about 5 nm in thickness.[114] An MTJ encapsulation layer of comparable thickness is also visible in the cross-sectional TEM image of an MRAM device shown at the beginning this chapter (see abstract image).[2,61] In addition to protecting the MTJ stack during subsequent processing steps, the encapsulation layer needs to inhibit diffusion of metal atoms along the interface between the MTJ and the encapsulation layer itself in order to prevent undesired shorts.[109] As a result, MTJ encapsulation at low temperature ($< 400\ ^{\circ}$C) is desired using SiN_x or similar dielectric compounds with good film adhesion and strong interfacial bonds, which prevent metal atom migration along the dielectric–metal interfaces.[109] The need for growing such thin films at low temperature makes plasma ALD a suitable choice for encapsulating MTJ stacks in next-generation MRAM devices.

Figure 9c also illustrates encapsulation of a memory cell using a conformal SiN_x layer in a commercial metal oxide based RRAM device where the resistive switching layer consists of an oxide layer stack (Ta_2O_5/TaO_x) with oxygen vacancies.[65,115] For this case, the encapsulation serves to prevent diffusion of oxygen into the memory cell in addition to preventing shorts between the top and bottom electrodes by metal atom migration.[65,115] The device shown in Figure 9c has been reported to consist of a memory cell having a lateral dimension of 117 nm, based on which the encapsulation layer thickness can be estimated to be about 43 nm.[115] Although such a thick layer can be obtained using plasma-enhanced CVD, 5 to 20 nm thick SiN_x layers have been reported

for encapsulating RRAM memory cells with dimensions < 20 nm.[116] Plasma ALD can therefore, be deemed as a suitable process for conformal encapsulation of such RRAM memory cells with smaller dimensions at low temperature.
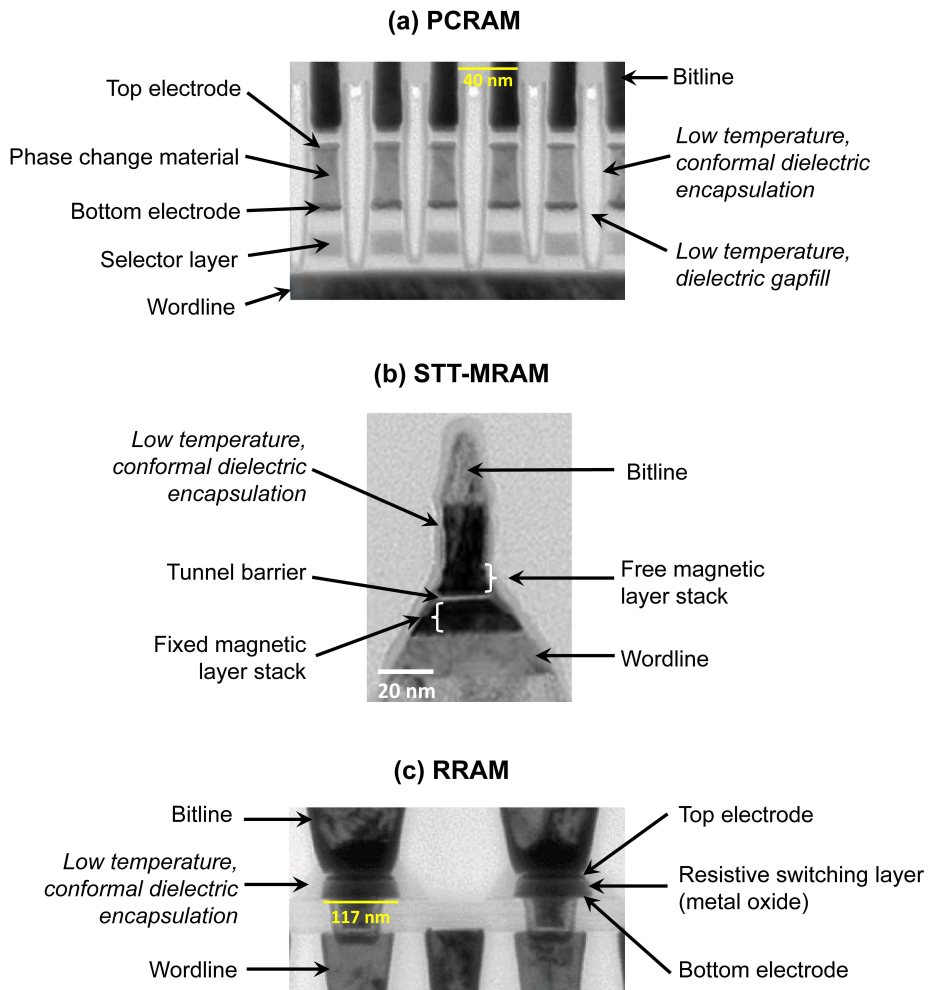
Figure 9. Cross-sectional images of **(a)** phase change random access memory (PCRAM) device in a one selector-one memory cell (1S-1MC) configuration,[113] **(b)** spin-transfer-torque magneto-resistive random access memory (STT-MRAM) device[114] in a one transistor-one memory cell (1T-1MC) configuration and **(c)** resistive random access memory (RRAM) device[65,115] in a 1T-1MC configuration. All images show the need for depositing low temperature (< 400 °C), conformal dielectric encapsulation layers for the respective memory cell stacks. For PCRAM, there is an additional need for a low temperature dielectric gapfill deposition process between the densely packed columns consisting of the memory cell + selector layer. The yellow scale bars have been added based on data regarding the indicated dimensions in the literature.

2.5 Key challenges from an etching perspective

As discussed before, EUV lithography is likely to be implemented in the fabrication process of next-generation sub-10 nm logic nodes, mostly for patterning linear cuts and circular vias in a single step.[22,78,79] A key issue that needs to be addressed when using EUV involves mitigating the high roughness of the patterned features (i.e., either the exposed and developed photoresist or its underlying layers after subsequent pattern transfer) originating from EUV photon shot noise.[6,7,77] The roughness is a manifestation of the crevices and protuberances formed on the sidewalls of the patterned features.[117] A measure for the roughness is usually expressed by the parameters LER or LWR for line-shaped patterns and local critical dimension uniformity (LCDU) for hole-shaped patterns, where LCDU is defined as the distribution of hole CD over a small distance.[117,118] Figure 10a and c show line- and hole-shaped photoresist patterns formed by EUV lithography and the corresponding values of the LWR and LCDU, respectively, reported for those patterns.[118,119]

One of the ways to improve (i.e., reduce) LWR and LCDU reported in the literature is to employ a combined passivating deposition and anisotropic etch process, either as an additional smoothening/corrective step right after photoresist exposure and development (Figure 2c), or during regular pattern transfer to the underlying layer (Figure 2d).[117,118,120] This can be carried out by means of a conventional dry etching technique such as reactive ion etching (RIE) that is driven by anisotropic, energetic ion and isotropic radical fluxes impinging on a target material.[121,122] The ions and radicals can be generated in a plasma where the use of low pressures (such that ion mean free path >> plasma sheath thickness) makes the ions directional while substrate biasing enhances the ion energy.[121,123] Using a passivating gas (e.g., fluorocarbon) to generate the plasma during RIE creates isotropic radicals that can deposit a passivating polymer layer on the EUV patterned features.[121,123] However, the passivating layer preferentially accumulates in the hollow crevices at the sidewalls of the rough EUV patterned features since those crevices do not undergo anisotropic ion bombardment.[117,120] The energetic and anisotropic ions bombard only the exposed regions of the passivating layer deposited on protruding features at the sidewalls of the patterned material.[117,120] This activates the reaction between the passivating polymer and underlying material leading to the formation of a volatile etch product, which has been reported to lower LER/LWR/LCDU of the EUV patterned features.[117,118,120,121,124]

Conventional dry etching techniques such as RIE are continuous and simultaneous etch processes.[122,124] It means that the etch rate is proportional to the process time during which radical adsorption (passivation) and energetic ion-induced activation (etching) occur concurrently, driven by the flux of these species impinging on the surface.[122,124,125] The concurrence or simultaneity prevents the passivation and etching

(a) After EUV lithography

LWR
4.5 nm

(c) After EUV lithography

LCDU
2.6 nm

(b) After pattern transfer with etch

LWR
2.9 nm

**(d) After photoresist smoothening
with etch**

LCDU
1.4 nm
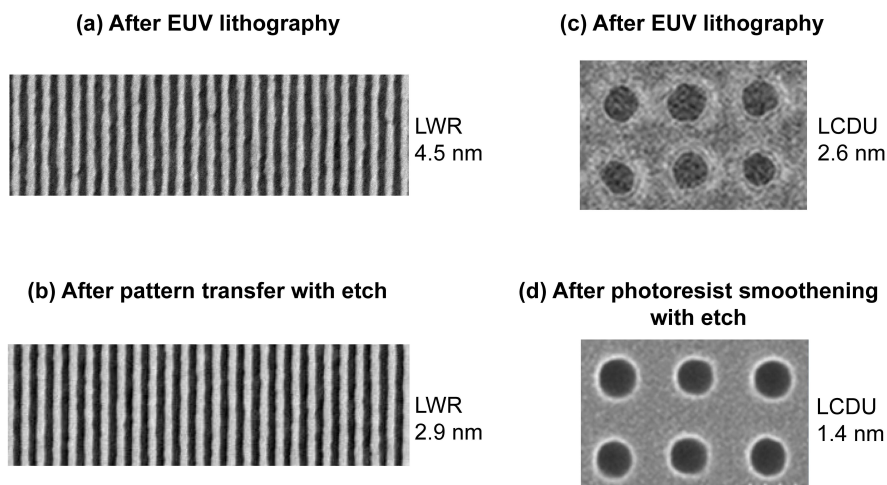
Figure 10. Top-view images[119] of **(a)** photoresist pattern of line-shaped features with a line width roughness (LWR) of 4.5 nm obtained using an extreme ultraviolet (EUV) lithography exposure step, **(b)** pattern transferred to underlying layer using an etch step forming linear features with a LWR of 2.9 nm, **(c)** photoresist pattern of hole-shaped features with a local critical dimension uniformity (LCDU) of 2.6 nm obtained using an EUV lithography exposure step, **(d)** photoresist pattern obtained after treatment with an etch step yielding holes with LCDU of 1.4 nm. The images illustrate the need for an etch process that leads to patterns with smoother features and improved uniformity.

events to be decoupled from each other, leading to diminished control over the etch rate and processing conditions.[122,124,125] For patterning the small CDs during fabrication of sub-10 nm logic nodes, the height of the photoresist features formed after EUV exposure and development needs to be small ($\sim$25 nm) in order to increase the mechanical stability of the patterned features and prevent them from collapsing.[125–128] This leaves a low budget in terms of the photoresist thickness available for use as a hard mask to transfer patterns to the underlying layers.[127,128] Although the use of RIE right after EUV exposure and development or during pattern transfer to the underlying layer has been reported to lower feature roughness, the process yields a low photoresist etch selectivity (with respect to the underlying layer).[118,120,122,125,129] This leads to a significant reduction in photoresist height (to $\sim$ 9 nm) and the formation of tapered photoresist profiles by RIE, which prevents reliable and high-fidelity transfer of pattern CDs to the underlying layer.[120,122,125,129] Furthermore, the flux dependency of RIE results in higher etch rates for low as opposed to high aspect ratio features, a phenomenon well-known as aspect-ratio dependent etching (ARDE).[121] This leads to variation in lithography-defined features depending on their location, e.g., over- or under-etched trenches/holes at low or high aspect ratio patterns, respectively.[121] All these factors

have contributed to the need for an etching technique that can lower EUV pattern roughness while enabling reliable and high-fidelity pattern transfer.

Atomic layer etching (ALE) is a technique that has the potential for overcoming the pitfalls of conventional (i.e., continuous and simultaneous) etching techniques.[122,130] Figure 10b and d show line- and hole-shaped photoresist patterns formed after pattern transfer and photoresist smoothening, respectively, by anisotropic plasma ALE.[118,119] The images quantitatively illustrate how ALE can reduce LWR and LCDU for the line- and hole-shaped patterns, respectively, obtained after EUV exposure and development.[118,119] As the sequential and self-limiting counterpart of plasma ALD, plasma ALE processes can decouple radical adsorption (passivation) and energetic ion-induced activation (etching), thereby enabling precise etch control and enhancing freedom over processing conditions.[122,124,130] The use of anisotropic plasma ALE has been reported to improve the etch selectivity of EUV patterned photoresists (with respect to the underlying layer), which substantially reduces loss of photoresist thickness while yielding highly symmetric, square-shaped profiles.[118,120,122,125,129] This has been reported to yield lower LER/LWR/LCDU for the EUV patterned features compared to those obtained using conventional etching techniques.[118,119,125,126,129] The decrease in patterned feature roughness by ALE was also reported to occur without significantly altering their CDs, unlike the case for conventional etching techniques which decreased both the feature roughness and CDs.[118,125] Furthermore, the self-limiting nature of ALE processes implies that they are flux independent, which prevents any ARDE and therefore, process variation.[121,122,130] All these factors effectively demonstrate how ALE can benefit patterning via EUV lithography when it is eventually adopted for fabrication of sub-10 nm transistor devices.

As mentioned earlier, the gate stacks in logic devices are covered with a capping layer on top and spacers on the sidewalls using a dielectric material, usually SiN_x, which prevents any short between the gate contact and the S/D contacts. [123,131] The SiN_x cap and spacers also act as etch stop layers protecting the gate stack when S/D contact trenches are opened between the gate stacks using a technique known as self-aligned contact (SAC) etching.[123,131] This technique involves etching a dielectric oxide gapfill, usually SiO_2, between the gate stacks with a high selectivity to the SiN_x gate cap and spacers in order to form trench shaped openings that reveal the S/D regions.[123,131] These trench openings are subsequently filled with a metal (e.g. W, Co) to form the S/D contacts.[98,105] Figure 11a and b show cross-sectional images of SACs grown on the S/D regions of previous and next-generation 22 nm and 10 nm node *fin*FET devices, respectively.[104] The tapered corners of the capping layer on top of the gate stack in Figure 11a indicate the use of a low selectivity SAC etching process that led to erosion of SiN_x at the top corners while SiO_2 was being etched. The SAC etching has generally

been carried out by a conventional anisotropic etch process, such as RIE using an inert and fluorocarbon gas mixture.[131] As discussed before, the continuous and simultaneous nature of RIE are known to confer a low selectivity during material etching, which is more clearly illustrated in Figure 11c that shows tapered corners at the SiN_x trench openings formed after RIE of SiO_2 gapfill.[131] The 22 nm node *fin*FET devices were reported to have a 90 nm contacted gate pitch (Figure 11a).[104] This pitch was large enough to tolerate the formation of tapered gate caps arising from low selectivity anisotropic RIE processes since a sufficient thickness of SiN_x was left remaining to prevent any short between the gate and S/D contacts. However, the upcoming 10 nm node *fin*FET devices have been reported to have a narrower contacted gate pitch of 54 nm without any tapered gate caps (Figure 11b).[105] Based on the absence of any tapered gate caps in these tighter pitches it can be speculated that a low selectivity anisotropic RIE process was most likely not implemented for SAC etching, since it would not leave behind a sufficiently thick insulating SiN_x cap for preventing electrical shorts. Honda *et al.* have reported an anisotropic plasma ALE process for SAC etching where SiO_2 gapfill can be removed with a high selectivity to SiN_x that yields trench openings without any tapered corners, as shown in Figure 11d.[131] They reported that the decoupling of radical adsorption and energetic ion-induced activation during plasma ALE conferred a more selective SiO_2 etch process (with respect to SiN_x) than conventional anisotropic RIE.[131] These results indicate how highly selective anisotropic ALE has the potential to replace conventional RIE processes for SAC etching during the fabrication of next-generation sub-10 nm logic nodes.

Besides highly selective anisotropic etching, the fabrication of future device architectures such as *gate-all-around* FETs also require highly selective etching processes that can remove material in an isotropic fashion. Figure 11e shows cross-sectional images of stacked columns consisting of alternate layers of semiconductor (Si), with a reported thickness of 5 nm, and sacrificial material (SiGe) used in the fabrication of *gate-all-around* nanosheet FETs (see abstract image).[1] A chemical etch treatment using vapor phase HCl was employed to selectively and isotropically etch SiGe (with respect to Si) in order to release the Si layers, as shown in Figure 11f, which serve as the nanosheet channels in the *gate-all-around* FET device.[1] However, the use of vapor phase HCl for isotropic etching of sacrificial layers has been reported to alter the shape of the released channel due to Si reflow.[132] Recent work reported by different authors have successfully demonstrated new routes for selective and isotropic removal of materials by ALE on 3D substrates (e.g., trench nanostructures, nanowires).[133–136] Shinoda *et al.* have reported isotropic ALE of SiN_x selective to SiO_2 and W selective to both TiN as well as SiO_2.[133,134] The ALE processes were based on the formation of a modified surface layer using radicals from a hydrofluorocarbon plasma followed by desorption of the modified layer via thermal annealing activated using infrared radiation.[133,134] Sherpa *et al.* have

(a) SAC in 22 nm node *fin*FET

Nitride cap — Oxide gapfill — S/D contact — Gate contact

90 nm — Nitride spacer

(b) SAC in 10 nm node *fin*FET

Nitride cap — Nitride spacer — Gate contact — S/D contact

Oxide gapfill — 54 nm

(c) After low selectivity directional etch

(d) After high selectivity directional etch

(e) Before selective isotropic etch

Sacrificial material layers

Semiconductor channel layers — 5 nm

(f) After selective isotropic etch

Released semiconductor channels — 5 nm

Figure 11. Cross-sectional images of **(a)** self-aligned contacts (SAC) on source/drain (S/D) regions of previous generation 22 nm node *fin*FETs showing contact openings with tapered corners (indicated by white arrows),[104] **(b)** SAC on S/D regions of upcoming 10 nm node *fin*FETs showing contact openings without tapered corners (indicated by white arrows).[105] Cross-sectional images of nitride based trench openings formed after removing an oxide gapfill using directional etch processes[131] **(c)** with low selectivity to nitride leading to corner erosion, **(d)** with high selectivity to nitride leading to corner retainment. Images **(a)-(d)** illustrate how tapered gate caps from low selectivity directional etch processes were acceptable for SACs in *fin*FET nodes with a larger pitch, whereas any tapered gate caps in the denser features of *fin*FET nodes with a smaller pitch are not acceptable since they could lead to undesired electrical shorts between the S/D contact and the gate contact. Cross-sectional images[1] of **(e)** stacked columns consisting of alternate layers of semiconductor channel material and sacrificial material before undergoing etch treatment, **(f)** semiconductor channels released after sacrificial material layers are removed using an etch treatment. The images illustrate the need for an etch process that selectively removes the sacrificial material with respect to the semiconductor channel material in an isotropic fashion, thus enabling the released channels to be wrapped with high-*k*-metal-gate layers needed to fabricate *gate-all-around* FETs. The yellow scale bars have been added based on data regarding the indicated dimensions in the literature.

shown isotropic ALE of SiN$_x$ selective to SiO$_2$ based on the formation of a modified surface layer using radicals from a hydrogen plasma followed by removal of the modified layer using radicals from a fluorine containing plasma.[135] Mameli *et al.* have demonstrated isotropic ALE of ZnO selective to SiO$_2$ and HfO$_2$ based on the production of volatile Zn(acac)$_2$ using acetylacetone that left behind carbonaceous species on the material surface which conferred self-limitation.[136] The carbonaceous species were subsequently combusted using an oxygen plasma.[136] Recently, an isotropic ALE process of InGaAs selective to InAlAs has been demonstrated by del Alamo and co-workers to create suspended InGaAs nanosheet structures, suitable for use as semiconductor channels in *gate-all-around* FETs.[137] Although an isotropic ALE process for SiGe selective to Si is yet to be demonstrated, the results discussed above indicate how ALE could provide an alternative to conventional chemical etch treatments for isotropic and selective removal of materials.

As discussed earlier, the next group of non-volatile memory devices after PCM poised to enter high-volume manufacturing are MRAM devices.[59,60] However, the fabrication of dense MRAM arrays has been plagued by a critical challenge related to patterning hard-to-etch magnetic and noble metals, such as Co, Fe, Pt, etc. and their alloys, that are key to making MTJs.[138] The use of ion beam milling as a patterning technique for such metals has been reported to yield functional MRAM devices having 28 nm MTJs at a 5F pitch without any electrical shorts, as shown in Figure 12a.[55,138,139] However, shorting across the MTJ caused by sidewall redeposition of non-volatile and conductive etch products from ion beam milling has been reported for the same 28 nm MTJs when spaced closer to each other at a smaller 2F pitch.[139] Recently, the use of

(a) Without redeposition after etch

(b) With redeposition after etch

No electrical short

Free magnetic layer stack (metal)

Redeposited metal

Fixed magnetic layer stack (metal)

Electrical short

Tunnel barrier (dielectric)
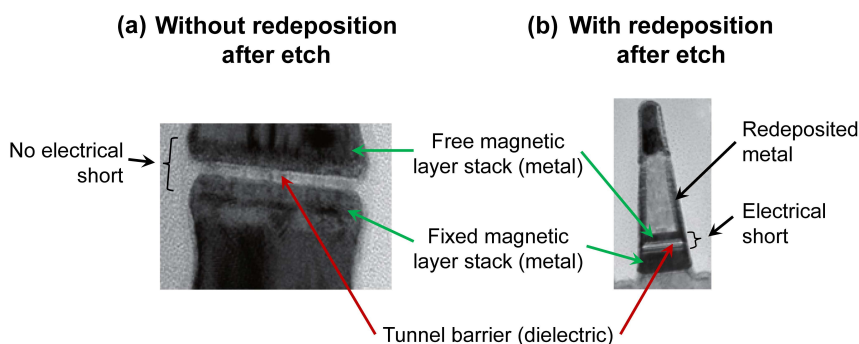
Figure 12. Cross-sectional images of a magnetoresistive random access memory (MRAM) devices[139] consisting of free and fixed magnetic metal layer stacks separated by a dielectric tunnel barrier (magnetic tunnel junction, MTJ) fabricated using a metal etch process **(a)** without any metal redeposition on MTJ sidewalls after etch and **(b)** with metal redeposition on MTJ sidewalls after etch. The images illustrate the need for a metal etch process that does not redeposit conductive metal on the sidewalls of the MTJ stack which would lead to undesired electrical shorts between the free and fixed magnetic metal layer stacks, thus causing device failure.

sequential acetylacetone or hexafluoroacetylacetone exposure followed by ion bombardment in an oxygen plasma was shown to provide an anisotropic ALE process for Co in the gas phase.[140,141] The use of such a gas-phase process to etch Co in a controlled and directional manner demonstrates the potential of ALE for patterning conductive and magnetic metals in MTJ stacks without any redeposition, critical for fabricating denser MRAM devices.

2.6 Conclusions

Fabricating state-of-the-art and next-generation logic and memory devices entails overcoming numerous challenges. The scaling of such devices involves making use of self-aligned multiple patterning techniques. These require deposition processes that yield nanoscale and conformal films (e.g., SiO_x, SiN_x, TiO_x) on 3D substrates with excellent growth control. Functional components of logic devices, e.g., present generation *fin*FETs and next-generation *gate-all-around* FETs, consist of multi-material gate stacks comprised of 3D architectures. These stacks need to be encapsulated with conformal, etch-resistant and nanoscale dielectric spacers (SiO_2, SiN_x). The metal contacts at the source/drain regions of these FETs require nanoscale, conductive liners (e.g., TiN_x). Emerging memory technologies such as PCRAM, MRAM and RRAM consist of sensitive memory cell stacks that need to be isolated from each other by dielectric gapfills (e.g., SiO_2) in dense crossbar array configurations. They also need to be protected from subsequent processing environments by conformally encapsulating the memory cell stacks with dielectric films (e.g., SiN_x, SiO_2). Thermal and plasma ALD are atomic scale processing techniques that can address these aforementioned challenges from the perspective of materials deposition.

EUV lithography will be implemented for patterning features in sub-10 nm logic device nodes. The patterns generated by EUV typically entail a high degree of roughness, which needs to be mitigated for patterning features with a high fidelity. Upcoming logic nodes have contacts that need to be made using highly selective anisotropic etching techniques, which prevent electrical shorts between gate and source/drain contacts. Future *gate-all-around* FETs will have nanowire/nanosheet based channels that need to be released using highly selective isotropic etching processes. Furthermore, the MTJs of emerging STT-MRAM devices need to be patterned using an anisotropic etch technique that does not create non-volatile etch products. Such products can get redeposited on MTJ sidewalls creating shorts that lead to device failure. Thermal and radical-driven plasma ALE has been reported to enable highly selective isotropic etching while ion-driven plasma ALE leads to highly selective anisotropic etching. These techniques can be used to address the aforementioned challenges involved in logic and memory device fabrication from the perspective of materials etching.

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Controlling Ion Energy and Flux Characteristics in a Remote Plasma Processing System

This chapter provides an overview on the basics of controlling ion energy and flux characteristics in a remote plasma ALD system. An example of such a system is shown in the photo above depicting a commercial Oxford Instruments FlexAL reactor equipped with substrate biasing for processing large-area Si wafers. The chapter explains how a substrate undergoing plasma exposure can be biased to acquire a relatively large negative average potential compared to the plasma. The chapter then elucidates how controlling this potential difference between the plasma and the substrate imparts control over the ion energies during plasma processing. The chapter concludes by providing an overview of the research reported in the literature where ion energy control has been thus far implemented during plasma ALD.

An increasing number of reactor configurations are currently being used for processing materials at the atomic level by plasma ALD/ALE. From the perspectives of plasma generation and the substrate undergoing processing, these reactors can be distinguished into two broad categories, typically denoted in the literature as direct plasma or remote plasma processing systems.[1,2] For the case of direct plasma reactors, the substrate on which processing takes place is located within the main plasma zone and is involved in plasma generation. For a remote plasma processing system, the substrate undergoing processing is situated outside of the main plasma generation zone, such that the plasma generation and substrate conditions are more or less independent of each other.

This chapter begins by presenting a brief overview on the basic characteristics of a plasma generated for materials processing. It outlines how the flux of a particular species – the ions – generated by the plasma can deliver energy to a substrate when it is electrically isolated (i.e., floating) or grounded during plasma exposure. The chapter then elucidates how the ion energy brought to a substrate in a remote plasma reactor can be controlled rather independently of the impinging ion flux by means of substrate biasing during plasma exposure. The chapter concludes by providing a short discussion on the results reported in the literature for plasma ALD with ion energy control.

3.1 Plasma basics

A plasma is an ionized gas consisting of free and charged particles (electrons and ions) together with other electrically neutral gas-phase species. It is generated and sustained when a gas is provided with sufficient energy such that it becomes partly or fully ionized.[3] For the confined, laboratory-scale low pressure plasmas employed in materials processing that are the focus of this work, the degree of ionization is very low, typically within the range of 10^{-6} to 10^{-3}.[1] The energy required to create and maintain these low pressure processing plasmas in a confined reactor is typically provided in the form of alternating electric fields generated by an external power source.[4] On macroscopic length scales (typically > 1 mm) in an electropositive plasma (consisting of positive ions and negative electrons as the charged species), the ion density (n_i) equals the electron density (n_e). The balance between positively and negatively charged species leads to the so-called quasi-neutral state in the plasma bulk.[1] A dominant characteristic of such low pressure plasmas is that the electrons are not in thermal equilibrium with the ions and other gas phase species. The applied electric fields accelerate the light electrons (mass - m) to higher velocities, and hence higher kinetic energies than the comparatively heavier ions (mass - M). Assuming a Maxwell-Boltzmann energy distribution, the mean electron temperature (T_e), which is a measure for the electron kinetic energy, is around 3.5 x 10^4 K ($\sim$ 3 eV) while the ion and gas temperatures (T_i and

T_{gas}, respectively) remain low at around 300 to 500 K ($\sim$ 0.02 to 0.04 eV) in the plasma bulk.[1] Electrons in the high-energy tail of the distribution have energies exceeding the gas ionization energy threshold and are able to ionize the gas-phase species through inelastic collisions. As such, the hot electrons are able to maintain a balance between the generation of charged species in the plasma bulk and their loss by recombination in the bulk and/or transport to the boundaries of the plasma.[3] The recombination in the plasma volume occurs mainly at very high pressures while it is negligible at low pressures where most charged species recombine at the walls of the plasma reactor. Besides ionization, the high energy electrons can also dissociate and excite the gas species through electron-impact inelastic collisions. This leads to the formation of atomic and molecular neutrals (known as plasma radicals) together with photon emission by excited species.

For a plasma in contact with a material surface, a transition region known as the sheath lies between the plasma and the surface. The sheath forms owing to the large difference in mobilities of electrons and ions that arises from their significantly different masses. This causes the more mobile electrons to reach a material surface faster than the ions upon plasma exposure, which means that the plasma potential (V_p) is always higher than the potential of any material surface (V_{sub}) exposed to it. This difference in potential across the sheath ($\Delta V_{sh} = V_p - V_{sub}$) denotes the presence of an electric field in that region pointing toward the surface. The electric field repels electrons from and accelerates ions toward the surface. Charge conservation dictates that the electron and ion fluxes balance each other at a steady state of plasma exposure. When a surface retards a Maxwellian distribution of electrons such that only those with energy greater than the sheath potential barrier ΔV_{sh} can surmount it, the electron flux (Γ_{es}) arriving at the surface is given by[4]

$$\Gamma_{es} = \frac{1}{4} n_o \left(\frac{8kT_e}{\pi m}\right)^{\frac{1}{2}} . exp\left[-\frac{e(\Delta V_{sh})}{kT_e}\right] \qquad \text{Eq. 1}$$

where n_o is the plasma density given by n_e or n_i in the plasma bulk (i.e., $n_o = n_e = n_i$), e is the elementary charge constant and k is the Boltzmann constant. The corresponding electron current density is $J_{es} = e\Gamma_{es}$.

The sheath edge corresponds to the point till which the quasi-neutral state of the plasma holds.[3] However, the sheath is a space-charge region where n_e exceeds n_i that violates quasi-neutrality.[3] This is because within the sheath, both n_e and n_i decrease but at different rates as the charged particle fluxes approach a surface undergoing plasma exposure. As mentioned earlier, n_e decreases because electrons are repelled by the surface while n_i decreases in order for the ions to maintain current continuity as they are accelerated toward the surface. A stable positive space-charge sheath can only

form if n_i begins to exceed n_e at the sheath edge, according to the Bohm criterion.[3] For this to occur, n_i has to decrease more slowly than n_e and the ions must enter the sheath with a minimum velocity known as the Bohm velocity, $u_B \geq (kT_e/M)^{1/2}$. Therefore, a quasi-neutral presheath region develops between the plasma and the sheath where n_e and n_i decrease at the same rate and where ions get accelerated to (at least) u_B by a potential drop of (at least) $kT_e/2e$ across the presheath.[4,5] The electron and ion densities (n_{es} and n_{is}) at the sheath-presheath interface relative to those at the plasma-presheath interface are $n_{es} = n_{is} = n_s = exp(-0.5)n_o = 0.61n_o$. As a result, the ion flux (Γ_{is}) arriving at the surface is given by[4]

$$\Gamma_{is} = n_s u_B = 0.61 n_o \left(\frac{kT_e}{M}\right)^{\frac{1}{2}} \qquad \text{Eq. 2}$$

A key aspect denoted by this equation is that the ion flux impinging on a surface is determined by n_o and T_e unlike the electron flux which has an additional dependence on ΔV_{sh}. The corresponding ion current density is $J_{is} = e\Gamma_{is}$.

For the rudimentary case of a floating substrate immersed in a plasma where $V_{sub} = V_f$ (i.e., not grounded or biased with a power supply), the potential across the sheath is given by $\Delta V_{sh} = V_p - V_f$. Here V_f is defined as the voltage at which the electron and ion fluxes impinging on the surface of a floating object balance each other resulting in zero net current. V_f is shown in Figure 1a which schematically illustrates a typical current density-voltage (J-V) charactersitic for a substrate undergoing plasma exposure. Such a characteristic is usually obtained from measurements conducted using a Langmuir probe immersed in a plasma, provided the probe has sufficiently small dimensions and does not perturb the plasma during those measurements.[5] Figure 1a also shows the electron saturation current density ($J_{es,sat}$) when V_{sub} reaches V_p, i.e., for $\Delta V_{sh} = 0$ V. At this condition, $\Gamma_{es,sat} = (1/4)n_o[(8kT_e)/(\pi M)]^{1/2}$ using Eq. 1, and therefore, $J_{es,sat} = e\Gamma_{es,sat}$. The corresponding ion saturation current density ($J_{is,sat}$) is obtained when V_{sub} attains values lower than V_f. The value of $J_{is,sat}$ is the same as that of J_{is} since the ion flux to a surface is independent of the sheath voltage, unlike the electron flux. Based on the definition of V_f, equating the expressions in Eq. 1 and 2 leads to the well-known relationship for the potential difference across a sheath formed on a floating substrate[4]

$$\Delta V_{sh} = V_p - V_f = \frac{kT_e}{2e} + \frac{kT_e}{2e} ln\left(\frac{M}{2\pi m}\right) \qquad \text{Eq. 3}$$

This equation indicates that $V_p - V_f$ depends on T_e and M and is typically reported in the literature to be a few multiples of kT_e/e.[1] Note that when the substrate is
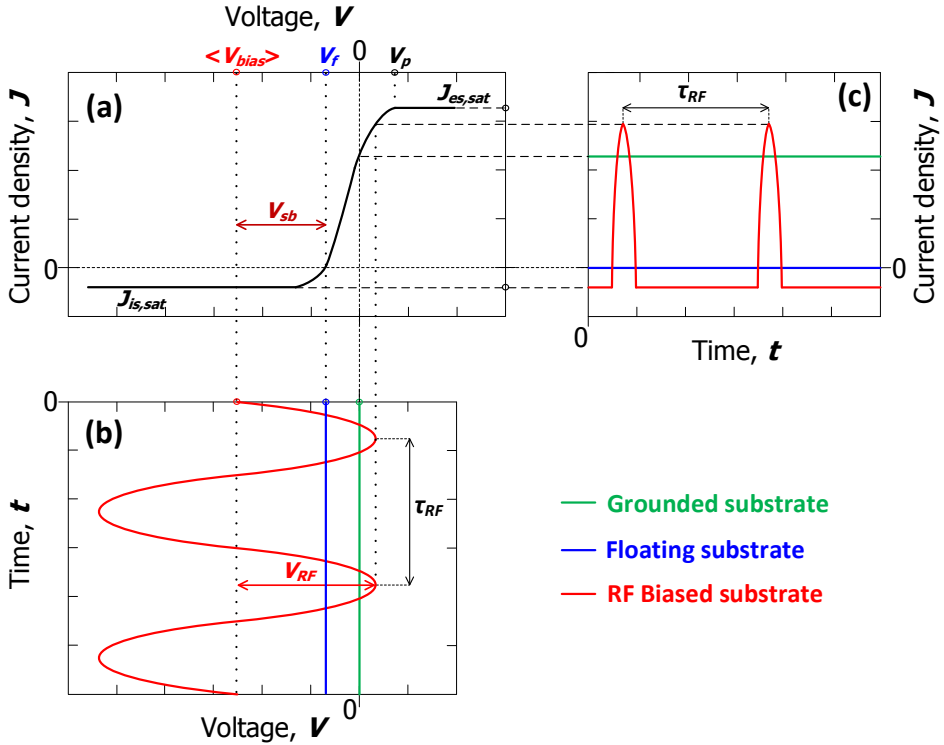
Figure 1. (a) Schematic illustration of a current density-voltage (J-V) characteristic showing the ion and electron saturation current densities ($J_{is,sat}$ and $J_{es,sat}$) with plasma and floating potentials (V_p and V_f), typically obtained from Langmuir probe measurements in the plasma bulk. **(b)** Schematic illustration of a voltage-time (V-t) characteristic typically obtained using an oscilloscope connected to the substrate stage via a high-voltage probe. It shows the development of time-invariant voltage waveforms for grounded and floating substrates and a time-varying voltage waveform (with period, τ_{RF}, amplitude, V_{RF}) for an RF biased substrate at steady state. The RF biased substrate voltage consists of a time-invariant DC voltage component ($\langle V_{bias} \rangle$) and a time-varying sinusoidal AC voltage component. RF bias voltages applied to a substrate through a blocking capacitor shifts V_f by a factor called the self-bias voltage (V_{sb}) which leads to the formation of $\langle V_{bias} \rangle$ at steady state. **(c)** Schematic illustration of a current density-time (J-t) characteristic typically obtained using an oscilloscope connected to the substrate stage through a current probe. It shows the development of time-invariant current-density waveforms for grounded and floating substrates that draw non-zero and zero net currents, respectively, at steady state. It also shows the temporal behavior of the current-density waveform (with period τ_{RF}) for an RF biased substrate at steady state. The current-density remains mostly constant at a negative value during one RF cycle (denoting a net ion current) and acquires positive values in the short instances where the time-varying voltage waveform in **(c)** attains positive values (denoting a net electron current). The integrated area under the current-density waveform over one RF cycle is zero, which indicates no net current flows during one RF cycle.

grounded, i.e., V_{sub} = 0 V, the electron and ion fluxes do not balance each other resulting in a non-zero net current (see Figure 1a).

The energy gained by ions traversing the plasma sheath also depends on the thickness of the plasma sheath, s, and the collisional mean free path of the ions, $\lambda_{i,mfp}$, which is the average distance travelled by ions before undergoing collisions with other gas-phase species. At sufficiently low pressures, $\lambda_{i,mfp}$ can attain values much larger than s, such that the ions can be accelerated anisotropically (by the directional electric field) across the entire sheath without undergoing collisions with other gas-phase species. For a collisionless Child-Langmuir sheath,[6] s is given by the expression

$$s = \frac{4}{3} \left(\frac{\epsilon_o kT_e}{0.61 n_o e^2} \right)^{\frac{1}{2}} \left(\frac{e\Delta V_{sh}}{2kT_e} \right)^{\frac{3}{4}}$$

Eq. 4

where ϵ_o is the permittivity of free space and the rest of the symbols denote parameters stated before. Although the expression in Eq. 4 indicates that s increases with ΔV_{sh}, the sheath remains collisionless as long as s is significantly less than $\lambda_{i,mfp}$. For a collisionless plasma sheath, the kinetic energy of ions (E_i) brought to a floating or a grounded surface is given by

$$E_i = e\Delta V_{sh} = \begin{cases} e(V_p - V_f) & \text{; floating substrate} \\ eV_p & \text{; grounded substrate} \end{cases}$$

Eq. 5

The equation above shows that the kinetic energy of ions arriving at the surface of a material after being accelerated in the sheath is significantly higher than that of ions in the plasma bulk. Various factors related to processing conditions and reactor configurations can influence the ion energy. These include, but are not limited to, the gas pressure, type of plasma source (remote/direct), reactor geometry (symmetry or asymmetry of grounded, floating, or powered electrodes), substrate stage configuration (grounded, floating, or biased substrate stage), etc. For the plasmas generated in a remote plasma processing system, as illustrated in Figure 2a, the kinetic energy of ions impinging on a grounded substrate (Figure 2b) is typically < 30 eV.[1] However, by implementing proper control over the aforementioned factors, ion energies of the order of a few hundred eVs can be obtained.[1]

3.2 Ion energy control with RF substrate biasing in remote plasma reactors

In a remote plasma processing system, e.g., an inductively-coupled-plasma (ICP) reactor shown in Figure 2a, the plasma source generating radicals and ions is located at a distance away from the substrate stage. This allows the plasma and substrate conditions to be varied fairly independently of each other. An AC power supply typically operating at a radio frequency (RF) of 13.56 MHz can be used to form time-varying electric fields
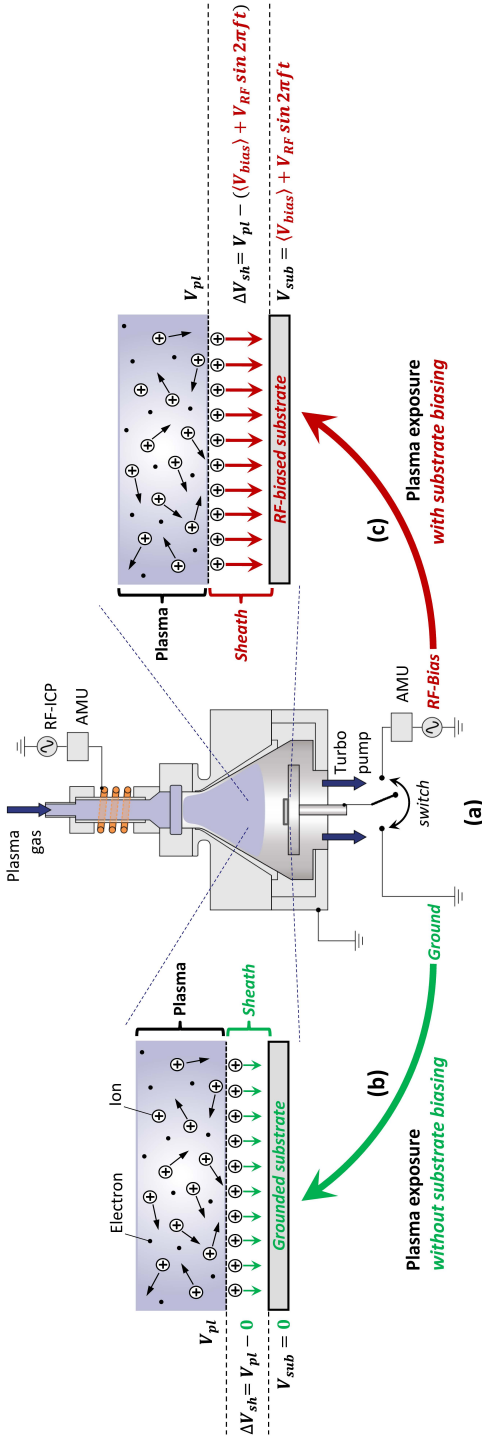
Figure 2. Schematic of **(a)** a remote plasma processing system equipped with substrate biasing where the plasma exposure step can be performed **(b)** without substrate biasing, i.e., on a grounded substrate, and **(c)** with substrate biasing. A radio-frequency power supply, RF-ICP, connected to a copper coil wrapped around a dielectric tube generates a remote inductively-coupled-plasma. The substrate table can be connected by an electrical switch either to ground or to a second RF power supply, RF-Bias, that enables substrate biasing. Both RF power supplies are connected to the system via automated matching units, AMU, consisting of inductive and capacitive components. The magnified schematics illustrate features of a space-charge region called the sheath formed between an electropositive plasma, consisting of positive ions and negative electrons as the charged species, and a substrate that is either grounded in **(b)** or RF-biased in **(c)**. The sheath potential, ΔV_{sh}, is the difference between the plasma potential, V_{pl}, and the substrate potential, V_{sub}. Ions are accelerated across the sheath by ΔV_{sh} leading to a directional flux of positive ions (provided ion mean free path significantly exceeds sheath thickness) impinging on the substrate with kinetic energy proportional to ΔV_{sh}. For the grounded substrate in **(b)**, V_{sub} is at zero potential, so ΔV_{sh} equals V_{pl}. For the RF biased substrate in **(c)** at steady state, V_{sub} acquires a time-averaged DC voltage component, $\langle V_{bias}\rangle$, and an AC voltage component, $V_{RF} \sin 2\pi f t$, that varies in time, t, with frequency, f, and amplitude, V_{RF}. $\langle V_{bias}\rangle$ acquires negative values which increases ΔV_{sh} to higher values compared to that for a grounded substrate. This increases the sheath thickness and kinetic energy of ions impinging on the RF-biased substrate in **(c)**, as illustrated by the wider sheath region and more intense arrows for ions in that region, respectively.

that can generate and sustain the plasma. The plasma species flux impinging on the substrate is usually controlled by varying the remote plasma source power.

If the system is equipped with substrate biasing, that is, by tuning the impedance between substrate stage and ground or by connecting the substrate stage to an additional AC power supply (see Figure 2c), then the substrate potential can be set or biased to have a non-zero value ($V_{sub} \neq 0$ V).[7] When a sinusoidal RF voltage signal (varying in time, t, with frequency, f, and amplitude, V_{RF}) is applied to the substrate stage through a blocking capacitor, time-varying voltages develop on the substrate such that in the first RF cycle, $V_{sub} = V_{RF} \sin 2\pi f t$. This denotes the presence of alternating electric fields formed above the substrate that change direction at 13.56 MHz. The light electrons in the plasma can instantaneously respond to these rapidly changing electric fields whereas the heavier ions cannot. As a result, a significantly larger flux of electrons compared to ions are accelerated toward the substrate during the first cycle of the applied RF bias signal.[8–11] Since the substrate stage is biased through a blocking capacitor, the excess electron flux will gradually charge it up negatively over subsequent RF cycles causing the substrate voltage to acquire a negative time-invariant DC component. This indicates the presence of a time-invariant DC component for the electric field formed above and directed toward the substrate, which the heavier ions are now able to follow. The time-invariant electric field component initiates directional ion acceleration toward the substrate (provided the sheath is collisionless) and electron repulsion away from it. A steady state is eventually reached when the electron and ion fluxes balance each other over one RF cycle. The voltage of an RF biased substrate at this steady state is then given by $V_{sub} = \langle V_{bias} \rangle + V_{RF} \sin 2\pi f t$. This can be visualized in Figure 1b, which illustrates the voltage versus time (V-t) characteristics of a grounded, floating and RF biased substrate at steady state, typically obtained using an oscilloscope connected to the substrate stage via a high-voltage probe. It shows that a grounded or floating substrate has a constant zero or negative potential, respectively, while an RF biased substrate at steady state has two components; namely a time-invariant DC voltage component, $\langle V_{bias} \rangle$, and a time-varying AC voltage component, $V_{RF} \sin 2\pi f t$. Note that $\langle V_{bias} \rangle$ acquires negative values at a steady state. This is because applying RF bias voltages to the substrate stage through a blocking capacitor gradually charges it up negatively over the first few RF cycles until a constant negative $\langle V_{bias} \rangle$ is reached at steady state.

The potential across the sheath formed between a plasma and an RF biased substrate at steady state can be written as $\Delta V_{sh} = V_p - (\langle V_{bias} \rangle + V_{RF} \sin 2\pi f t)$. This shows that the time-varying RF bias voltage causes the sheath potential to oscillate with an amplitude V_{RF} about a mean value given by the time-averaged DC component of $V_p - \langle V_{bias} \rangle$. The electron flux toward the substrate is modulated by the time-varying potential barrier arising from the oscillating sheath. On the other hand, since the ion flux is independent of ΔV_{sh}, it remains unaffected by the RF sheath oscillation. This is illustrated by the temporal behavior of the current density for an RF biased substrate in

Figure 1c. It shows the current-density versus time (J-t) characteristics of a grounded, floating and RF biased substrate at steady state, typically obtained using an oscilloscope connected to the substrate stage through a current probe. For an RF biased substrate, the ions are continuously collected at a constant rate while electron collection occurs in short bursts only during those instances when the oscillating substrate voltage attains positive values while approaching V_p (see Figure 1b). Charge conservation is maintained since the integrated electron and ion current densities over one RF cycle is zero. Similar to Eq. 1, the expression for the electron flux ($\Gamma_{es,RF}$) arriving at the surface after overcoming the oscillating sheath potential barrier at an RF biased substrate is given by

$$\Gamma_{es,RF} = \frac{1}{4}n_o\left(\frac{8kT_e}{\pi m}\right)^{\frac{1}{2}} exp\left[-\frac{e\left(V_p-(\langle V_{bias}\rangle+V_{RF}\sin 2\pi ft)\right)}{kT_e}\right] \qquad \text{Eq. 6}$$

Since the ion flux arriving at a surface in contact with a plasma is determined by n_o and T_e and not by ΔV_{sh}, the expression for the ion flux ($\Gamma_{is,RF}$) impinging on the surface of an RF biased substrate is identical to that in Eq. 2. As mentioned before, the electron and ion fluxes over one RF cycle (having a time period $\tau_{RF} = 1/f$) cancel each other out at steady state. This means that the time-averaged electron and ion fluxes over the RF cycle should balance, which is expressed as

$$\frac{1}{\tau_{RF}}\int_0^{\tau_{RF}}\Gamma_{es,RF}\,dt = \frac{1}{\tau_{RF}}\int_0^{\tau_{RF}}\Gamma_{is,RF}\,dt \qquad \text{Eq. 7}$$

Substituting the terms in Eq. 6 with the appropriate terms from Eq. 2 and 6 and solving for $V_p - \langle V_{bias}\rangle$ leads to[4,8,10,12–15]

$$V_p - \langle V_{bias}\rangle = \frac{kT_e}{2e} + \frac{kT_e}{2e}\ln\left(\frac{M}{2\pi m}\right) + \frac{kT_e}{e}\ln B_o\left(\frac{eV_{RF}}{kT_e}\right) \qquad \text{Eq. 8}$$

The parameter $B_o(eV_{RF}/kT_e)$ in Eq. 8 is a zero order modified Bessel function originating from the time-averaged integral of an exponential function having a sinusoidal component,[4,10,12,14,15] i.e., $(1/\tau_{RF})\int_0^{\tau_{RF}} exp[eV_{RF}/kT_e.\sin(2\pi t/\tau_{RF})]dt$. The first two terms on the right hand side of Eq. 8 can be replaced using $V_p - V_f$ as per Eq. 3. Incorporating this change leads to

$$\langle V_{bias}\rangle = V_f - \frac{kT_e}{e}\ln B_o\left(\frac{eV_{RF}}{kT_e}\right) \qquad \text{Eq. 9}$$

The expression above indicates that applying RF bias voltages to a substrate via a blocking capacitor (at steady state) is equivalent to a shift in V_f by the factor $(kT_e/e)\ln B_o(eV_{RF}/kT_e)$, which is sometimes termed as the *self-bias voltage*, V_{sb}.[12,13] This is shown schematically in Figure 1a and b. When $V_{RF} \gg kT_e/e$, an approximation can be made that allows the modified Bessel function to be expressed differently, such that $B_o(eV_{RF}/kT_e) \approx (kT_e/2\pi eV_{RF})^{1/2}.exp(eV_{RF}/kT_e)$.[4,10,14,15] Implementing this change in Eq. 9 leads to

$$\langle V_{bias} \rangle = V_f - V_{RF} - \frac{kT_e}{2e} ln \left(\frac{kT_e}{2\pi e V_{RF}} \right)$$ Eq. 10

Therefore, for a collisionless plasma sheath, the mean kinetic energy of ions, $\langle E_i \rangle$, delivered to a substrate biased using a time-varying RF voltage signal can be stated as

$$\langle E_i \rangle = e \langle \Delta V_{sh} \rangle = e(V_p - \langle V_{bias} \rangle) = e(V_p - V_f) + eV_{RF} + \frac{kT_e}{2} ln \left(\frac{kT_e}{2\pi e V_{RF}} \right)$$ Eq. 11

In the expression above, $e(V_p - V_f)$ and the logarithmic term have values of the order of kT_e (see Eq. 3). Therefore, Eq. 11 indicates that as long as T_e remains unchanged with biasing and $eV_{RF} \gg kT_e$, $\langle E_i \rangle$ has an approximately linear relationship with eV_{RF}.[10,15,16] This expression serves to illustrate that in a remote plasma processing system equipped with RF substrate biasing, the ion energy delivered to a material surface can be controlled (enhanced) independently of the ion flux by tuning (increasing) the amplitude of the applied RF bias signal (provided T_e stays constant and $eV_{RF} \gg kT_e$).

   At this point, it is worth noting that recent investigations of remote ICP reactors employing RF substrate biasing clearly demonstrate how, under certain conditions, some of the bias power contributes toward heating electrons near the substrate.[17–20] This causes plasma parameters such as T_e, n_o, and consequently, the ion flux to be affected by RF substrate biasing during plasma exposure.[17–20] Furthermore, the equations above and the (J-V) characteristics illustrated in Figure 1 were given on the basis of measurements typically reported using a Langmuir probe. The active regions of such probes have dimensions that are negligible compared to the plasma volume and consequently, do not perturb the plasma parameters. This may not be the case for an RF biased substrate holder/table in a remote ICP system capable of processing large-area substrates (e.g., 200 mm Si wafers). These factors indicate that for practical remote ICP systems, control of the ion energy may not be ideally independent of the ion flux when applying RF bias voltages during plasma exposure. Yet, for the purpose of processing materials at the atomic level, implementing RF substrate biasing in a remote plasma ALD system serves as a reliable means for ion energy control, provided the ion flux is not significantly influenced during plasma exposure.

3.3 Literature on plasma ALD with ion energy control

The role of energetic ions has been extensively investigated in the literature for conventional flux-controlled deposition processes, such as physical vapor deposition (PVD) and plasma-enhanced chemical vapor deposition (PECVD), that lead to continuous film growth.[21] However, relatively fewer studies have been reported for the surface-controlled process of plasma ALD that yields self-limited and controlled film growth.

The first experimental investigation on the role of ions during plasma ALD was conducted by Profijt *et al.*[7,22] in previous work conducted within our group. They looked into the effects of enhancing oxygen ion energies during plasma ALD on the growth and material properties of aluminum oxide, titanium oxide and cobalt oxide.[7,22] The films were deposited in a home-built remote plasma ALD tool equipped with substrate biasing where $\langle V_{bias} \rangle$ was controlled either by adjusting the impedance between the substrate and ground, or by varying V_{RF} of an RF voltage signal applied to the substrate.[7,23] Enhancing ion energies with substrate biasing during the plasma exposure step of ALD was observed to have significant effects during film growth that were material and/or process-specific. Increasing bias voltages during oxygen plasma exposure increased the growth rate and oxygen content of aluminum oxide films while lowering their mass density.[7] The residual stress of the deposited films was also observed to be altered from tensile to compressive with the use of substrate biasing. The growth rate, density and oxygen content of titanium oxide films deposited with substrate biasing during oxygen plasma exposure showed a similar behavior as aluminum oxide.[7,22] An additional effect was observed in case of titanium oxide where its crystalline phase could be gradually tailored from anatase to rutile with increasing $\langle V_{bias} \rangle$.[7,22] For cobalt oxide, the growth rate decreased and the film density increased at higher $\langle V_{bias} \rangle$ while the films became slightly oxygen deficient.[7]

In a separate study, Ratzsch *et al.*[24] reported on the inhibition of crystal growth by lowering the ion energy during plasma ALD of titanium oxide. In that work, a customized substrate configuration was employed where a metal grid was placed over an electrically insulated substrate during film deposition using an oxygen plasma exposure step. Films were grown in separate runs without and with a positive DC bias voltage applied to the grid (with respect to the substrate) during the oxygen plasma step. The positive DC bias lowered the voltage across the sheath formed between the plasma and the grid. This repelled (or decelerated) the incoming ions from the plasma and therefore, lowered the kinetic energy of ions impinging on the underlying substrate. It culminated in the inhibition of crystal grain nucleation during film deposition, which would otherwise take place when no bias voltage (i.e., 0 V) was applied to the grid causing the ions to impinge on the substrate with a relatively higher kinetic energy.

Iwashita *et al.*[25] reported a different approach for controlling the ion energy during plasma ALD of titanium oxide in a direct capacitively coupled plasma (CCP) reactor with electrodes in a parallel-plate configuration. Over there, the impedance between the substrate and ground was adjusted during oxygen plasma exposure by tuning the reactance of an inductor connected to the electrode on which the substrate was placed. This allowed the substrate potential to be varied which in turn varied the kinetic energy of the impinging ions during film deposition. A correlation was observed between the film properties and the ion energy where a higher ion energy resulted in films with a lower refractive index and a higher wet-etch rate (in dilute hydrofluoric acid). In another study carried out by the same authors using the same reactor configuration, plasma ALD

of metallic titanium films were reported with ion energy control during a plasma exposure step using an argon and hydrogen gas mixture.[26] The film growth rate per ALD cycle increased while the residual stress changed from tensile to compressive as a function of the ion energy. However, the resistivity and mass density of the films were observed to be independent of the ion energy during plasma exposure.

To the best of our knowledge, the aforementioned work have been the only ones reported in the literature so far which actively investigated the role of ion energy during plasma ALD. They show that oxide based films grown using an oxygen plasma have formed the primary basis of investigation for plasma ALD with ion energy control. All results have been reported for film deposition only on small-area planar substrates and by applying substrate biasing for the entire duration of the plasma exposure step. Other material categories (e.g., nitrides), plasmas (e.g., hydrogen plasma, nitrogen plasma), substrate dimensions (e.g., large-area 200 mm Si wafers), substrate architectures (e.g., 3D trench-shaped nanostructures) and bias duty cycles (e.g., different bias duration during plasma exposure time) had yet to be investigated for plasma ALD with ion energy control. Furthermore, experimental analyses of ion energy characteristics (e.g., ion-flux energy distribution functions) for different reactive plasmas, process conditions (e.g., plasma pressure, plasma source power) and substrate configurations (biased/non-biased) in the same plasma reactor is seldom reported in the literature. To the best of our knowledge, studies are frequently reported using inert argon plasma for etch reactors and has not been reported for dedicated and commercially available remote plasma ALD systems. These factors have been taken into account during the course of this research. The subsequent chapters of the dissertation report the results obtained during plasma exposure without and with RF substrate biasing in a commercial remote plasma ALD system that allows for processing large-area substrates.

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Atomic Layer Deposition of Wet-etch Resistant Silicon Nitride using Di(sec-butylamino)silane and N_2 Plasma on Planar and 3D Substrate Topographies
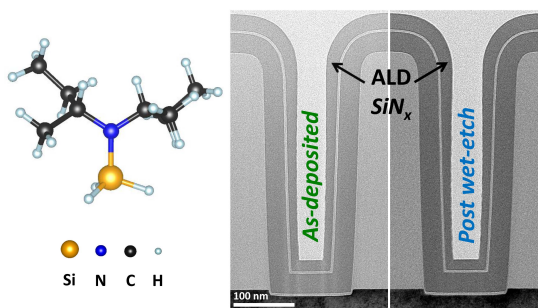
Silicon nitride (SiN_x) films serve a variety of applications in both device manufacturing and final device architectures. In many cases, a low temperature (< 400 °C) deposition process is desired which yields high quality SiN_x films that are etch resistant and also conformal when grown on three-dimensional (3D) substrate topographies. In this chapter, a new plasma-enhanced atomic layer deposition (PEALD) process for SiNx is presented that was developed using a mono-aminosilane precursor, Di(Sec-ButylAmino)Silane (DSBAS, $SiH_3N(^sBu)_2$, see image above), and N_2 plasma. Material properties have been analysed over a wide stage temperature range (100 – 500 °C) and compared with those reported in previous work. Dense SiN_x films (~ 3.1 g/cm^3) with low C, O and H contents were obtained on planar substrates when deposited at low substrate temperatures (< 400 °C). The developed process was also used for growing SiN_x films on high aspect ratio (4.5 : 1) 3D trench nanostructures to investigate film conformality and wet-etch resistance (in dilute hydrofluoric acid, HF : H_2O = 1 : 100). The conformality was below typically desired levels and is attributed to the combined role played by nitrogen plasma soft saturation, radical species recombination and/or ion directionality during SiN_x deposition on 3D substrates. Yet, very low wet-etch rates ($\leq$ 2 nm/min) were observed at all trench regions of the most conformal film deposited at a low substrate temperature < 400 °C (see image above), which confirmed that the process is applicable for depositing high quality SiN_x films on both planar and 3D substrate topographies.

4.1 Introduction

Silicon nitride (SiN$_x$) is a widely used material in both front and back end-of-the-line (FEOL/BEOL) processes of semiconductor device manufacturing.[1,2] It regularly serves as hard masks and etch stop layers in critical processing techniques, such as spacer defined patterning[3–5] and self-aligned contacts.[6,7] A key application of SiN$_x$ films is spacers[8–10] for the high-k metal gate (HKMG) stack in both planar FET and state-of-the-art 3D finFET[11–13] architectures in CMOS nanoelectronics. These spacer films serve multiple purposes such as being a barrier against oxygen ingress and dopant out-diffusion while preventing any etch damage during subsequent processing steps.[14,15] They also provide a constant spacing of the source and drain of the transistor, independent of transistor pitch.[8,16] All these require the SiN$_x$ films to be highly conformal and etch resistant in dilute hydrofluoric (HF) acid (HF : H$_2$O = 1 : 100).[8,14,15] However, the use of the HKMG stack requires a low temperature (~400 °C) processing environment in order to prevent interlayer diffusion or interfacial reactions from occurring at elevated temperatures.[17] Processing of SiN$_x$ at even lower temperatures (~250 °C) is required for applications in emerging memory devices, such as encapsulation[18] for magnetic tunnel junctions (MTJ) in MRAMs,[19–21] where metal atom migration at high temperatures can lead to device degradation.[21–24] SiN$_x$ has been traditionally deposited using low-pressure chemical vapour deposition (LPCVD) or plasma-enhanced chemical vapour deposition (PECVD) processes.[25] LPCVD generally yields conformal SiN$_x$ films with low wet-etch rates (WERs <1 nm/min)[15] in dilute HF but only at high temperatures (>700 °C).[14] Using PECVD can lower the process temperatures to ~400 °C but the SiN$_x$ films exhibit a reduced conformality on 3D structures and/or imprecise film thickness control.[25] Thermal and plasma-enhanced atomic layer deposition (ALD, PEALD) are well known methods for depositing high quality thin films with excellent growth control.[26–29] However, growing highly conformal (>95%) and wet-etch resistant (WER <1 nm/min) SiN$_x$ films in high aspect ratio structures (HARS) at low deposition temperatures (<400 °C), is not trivial to achieve, not even with ALD.[30] Table 1 provides a brief summary of SiN$_x$ ALD processes reported in the literature.

ALD of SiN$_x$ has been frequently reported employing chlorosilane precursors (such as SiCl$_4$, SiH$_2$Cl$_2$, Si$_2$Cl$_6$, and Si$_3$Cl$_8$) in combination with co-reactants such as NH$_3$, NH$_3$ plasma, or N$_2$H$_4$.[15,31–37] Some of these processes have also reported on the attainment of highly conformal (>80%) SiN$_x$ films when deposited on 3D substrates.[15,36,37] However, these processes generally require high temperatures for depositing high quality films as indicated by the low densities (<2.7 g/cm^3)[31,33,37] and high WER values (>10 nm/min)[15,36] reported for low temperature (<400 °C) growth conditions. Furthermore, halide containing precursors can lead to excessive particle formation, undesired incorporation of chlorine impurities, corrosive reaction by-products and incompatibility with metal

substrates.[30,38] The use of silane or aminosilane precursors during PEALD can offer a halide-free deposition route.[38] King[25] employed both PECVD and PEALD processes to grow silicon nitride films on 3D trench structures (aspect ratio, AR ~3.5 : 1) using silane (SiH_4) combined with N_2 plasma at low temperature (<400 °C). Film quality obtained was relatively low as indicated by the low mass densities (≤2.7 g/cm^3) while a conformality ≤50% was reported for the two processes. No WER values in dilute HF were reported. Triyoso et al.[14] carried out PEALD of SiN_x using trisilylamine ($N(SiH_3)_3$) combined with an H_2/N_2 intermixed plasma. The process yielded high quality films, represented by low WERs (≤1.5 nm/min) in dilute HF at deposition temperatures ≤400 °C. Good conformality was reported with side/top ratios of ~80% but the 3D structures used were of a relatively low AR (~2 : 1). Trench structures with a higher AR (~5.5 : 1) used by Park et al.[39] gave a side/top ratio of ~73% for PEALD of SiN_x using a trisilylamine-derivative precursor ($N(SiHN(CH_3)_2CH_3)_2Si(CH_3)_3$) and N_2 plasma. WERs between 4.55 and 0.23 nm/min were reported but in a more diluted HF solution (HF : H_2O = 1 : 500). Recent work by Weeks et al.[40] reported a SiN_x PEALD process using neopentasilane ($Si(SiH_3)_4$) and N_2 plasma where they obtained films with low WER (~3 nm/min) in dilute HF but with low film densities (2.21 g/cm^3) for the optimized conditions. They also deposited SiN_x films on 3D trench structures with different AR values, observing a decrease in sidewall film thickness with depth inside the trench. Sidewall/top film thickness ratio was observed to be ~50% (within 200 nm of the top of the trench), similar to that of King,[25] irrespective of trench AR or increase in precursor dose (from 1 to 3 s) and plasma exposure (from 2 to 15 s).[40] They also observed soft saturation of GPC as a function of N_2 plasma exposure time which indicates long cycle times similar to that of King[25] could be needed for saturation.
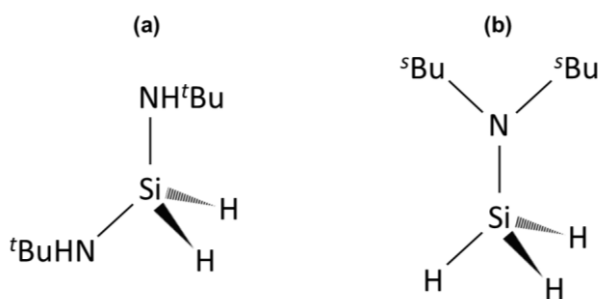
Figure 1. Schematic illustrations depicting the chemical constituents of **(a)** BTBAS and **(b)** DSBAS precursor molecules.

In previous work conducted within our group, Knoops et al.[16] developed a SiN_x process employing a Bis(*Tert*-ButylAmino)Silane (BTBAS, $SiH_2(NH^tBu)_2$) precursor, depicted in Figure 1a, in combination with a remote N_2 plasma. High quality SiN_x films were deposited having reasonable impurity contents ([C] <10 at. % and [O] <5 at. %).

Table 1. Overview of SiN$_x$ material properties reported in the literature for films deposited with ALD using various precursors and co-reactants. The selected reports are chosen based on data available for film conformality on 3D substrate topographies and/or wet-etch resistance (in dilute hydrofluoric acid, HF : H$_2$O = 1 : 100) of SiN$_x$ at planar and 3D surfaces when deposited at temperatures ≤400 °C. A "-" indicates data not reported.

Precursor	Co-reactant	Mass density (g/cm^3)	3D substrate aspect ratio	Conformality (Side/Top ratio in %)	Wet-etch rate (nm/min)		Reference
					Planar surface	3D sidewall surface	
SiCl$_4$, SiH$_2$Cl$_2$, Si$_2$Cl$_6$, Si$_3$Cl$_8$	NH$_3$, NH$_3$ plasma, N$_2$H$_4$	<2.7[a]	≥2 : 1[b]	>80[b]	>10[c]	-	15,31–37
SiH$_4$	N$_2$ plasma	2.7	~3.5 : 1	≤50	-	-	25
N(SiH$_3$)$_3$	H$_2$/N$_2$ plasma	2.8	~2 : 1	~80	≤1.5	-	14
N(SiHN(CH$_3$)$_2$CH$_3$)$_2$Si(CH$_3$)$_3$	N$_2$ plasma	-	~5.5 : 1	~73	≤4.55[d]	-	39
Si(SiH$_3$)$_4$	N$_2$ plasma	2.21	≥6 : 1	~50	~3	-	40
SiH$_2$(NH^{t}Bu)$_2$	N$_2$ plasma	2.9	-	-	~0.2	-	16
SiH$_3$N(^{s}Bu)$_2$	N$_2$ plasma	≤3.1	4.5 : 1	≤50	0 to 2	1 to 6	This work[e]

[a] Data available only for references 31,33,37 [b] Data available only for references 15,36,37 [c] Data available only for references 15,36,37
[d] Wet-etch rate reported using dilute HF solution with HF : H$_2$O = 1 : 500 [e] For substrate temperatures <400 °C

Moreover, the H content was relatively low ([H] <11 at. %) and a low WER (~0.2 ± 0.5 nm/min at 400 °C) was obtained in dilute HF solution.[16] Insights provided by Ande et al.[41] later demonstrated that the growth rate of SiN_x using BTBAS is strongly reduced when NH_3, $N_2 + H_2$ or H_2 plasmas were used. This explained the choice of using an N_2 plasma over other H-containing plasmas as the co-reactant during PEALD with BTBAS. In other studies related to this work, Knoops et al.[42] identified parameters governing the quality of SiN_x films deposited using BTBAS and N_2 plasma while Bosch et al.[43] investigated the surface chemistry of that process with in-situ infrared spectroscopy. They demonstrated that t-butylamine (NH^tBu) ligands remained on the surface after BTBAS adsorption and that these ligands get dissociated into fragments (C, H and N species) during the subsequent N_2 plasma step. Redeposition of these fragments on the growing film surface leads to significant impurity contents in the deposited SiN_x films which could be minimised by lowering the residence time of the plasma species.[42] This residence time was, therefore, identified as a key parameter governing film quality.[42] A high pumping capacity, together with adequately high gas flows and/or low plasma pressures, was demonstrated as a means for reducing the residence time of the species, which lowers redeposition and hence, improves film quality (i.e., low WER ~0.5 nm/min).[42] Based on these results, another route for minimising redeposition can be hypothesized that may lead to high quality SiN_x films. Since the dissociation of ligands remaining on the surface after precursor adsorption was shown to cause redeposition, reducing or (ideally) eliminating the presence of such ligands on the surface before plasma exposure could, in principle, reduce or eliminate redeposition. Since the use of a *bis*-aminosilane precursor (with two amino ligands) has been shown to leave amino ligands on the surface,[43] the use of a *mono*-aminosilane precursor (with one amino ligand) could, in principle, leave fewer or (ideally) no amino ligands on the surface after precursor adsorption. As a result, comparatively fewer ligands would dissociate during plasma exposure after a *mono*-aminosilane precursor dose, thereby reducing impurity redeposition and improving film quality.

In order to validate this hypothesis, a new PEALD process for SiN_x was developed and studied in this work using the *mono*-aminosilane precursor Di(*Sec*-ButylAmino)Silane (DSBAS, $SiH_3N(^sBu)_2$)[38,44–46] and N_2 plasma. The DSBAS molecule contains only one amino ligand, as depicted in Figure 1b. Material properties of SiN_x films deposited on planar substrate topographies have been compared with those obtained in our previous work[16] for films deposited using BTBAS and N_2 plasma. High quality films with low [C], [O] and [H] levels and a high film density (~3.1 g/cm³) were obtained on planar substrates at low substrate temperature (<400 °C) using DSBAS and N_2 plasma. WERs in dilute HF reported for SiN_x ALD processes discussed above are for films deposited on planar substrate topographies, which is not representative for assessing etch resistance within the 3D topographies incorporated in state-of-the-art

device architectures. The process developed in this work with DSBAS was used to deposit SiN$_x$ films on high aspect ratio (4.5 : 1) trench nanostructures in order to investigate film conformality and HF-etch resistance at different regions (planar and vertical sidewall) of the 3D substrate, relevant for modern device fabrication. Film conformality was observed to be low (≤50%) but comparable to values obtained for similar processes[25,40] reported in the literature. Yet, very low WERs were obtained at different regions of the trench nanostructures for the films deposited at low substrate temperature (<400 °C), confirming that the process is applicable for growing HF-etch resistant SiN$_x$ on both planar and 3D substrate topographies.

4.2 Experimental details

PEALD of SiN$_x$: PEALD of SiN$_x$ was performed using an Oxford Instruments FlexAL reactor.[47] It is equipped with a remote inductively coupled (ICP) plasma source, which was operated at 600 W of radio frequency power at 13.56 MHz and controlled by an automated matching network. The source consists of a water-cooled copper coil wrapped around a cylindrical alumina plasma tube. A base pressure in the reactor chamber of $\sim$10^{-6} Torr was obtained using a turbo pump. A butterfly valve in front of the turbo pump controlled the effective pumping speed and functioned as an automated pressure controller (APC). The chamber wall temperature was set to 150 °C, except for instances where the deposition temperatures were below 150 °C, during which the wall was set to the deposition temperature. Due to poor thermal contact in vacuum, the actual temperature of the substrates (wafer, coupon – see ***ALD film growth*** section) were lower than the set temperature of the substrate stage/table. This set temperature (henceforth referred to as stage temperature), can be fixed to a value between 25 and 500 °C. An estimation of the actual substrate temperature as a function of stage temperature is given in Appendix 4 (Table A4.1). All substrates underwent a thirty minute heating step prior to commencing deposition in order to ensure substrate temperature stabilization. DSBAS (assay ≥99.3%, see Appendix 4, Table A4.2), synthesized and provided by Air Products and Chemicals Inc., was used as the precursor and held at a bubbler temperature of 40 °C. During precursor dosage, DSBAS was vapour drawn into the reaction chamber using Ar (25 sccm, purity 99.999%) as a carrier gas in the delivery line, with the APC valve completely closed. A reaction step was employed immediately after precursor dosage with the APC valve set to 10° to reduce the effective pumping speed and maximize precursor usage by confining it within the chamber. Setting the APC valve to 10° (i.e., almost closed) was necessary because a continuous flow of inert N$_2$ gas (50 sccm, purity 99.9999%) was passed through the alumina plasma tube during all process steps in order to reduce precursor adsorption on the inner surfaces of the tube during precursor dose and reaction steps. For both purge steps, the APC valve was fixed to a 90° valve position (i.e., fully open) for maximum pumping while

50 sccm of N_2 gas flowed through the alumina tube. The precursor delivery lines were heated to 70 °C to prevent precursor condensation and were purged with 100 sccm of Ar to remove any residual gas from previous ALD cycles.

PEALD process conditions: Based on the saturation curves for precursor dosage and plasma exposure obtained during process development using DSBAS and N_2 plasma (see **ALD film growth** section), the following step sequence was chosen as a standard PEALD recipe for SiN_x: 1 s delivery line purge, 100 ms DSBAS dose time, 3 s reaction time, 1 s precursor purge time, 2 s pre-plasma time (gas stabilization prior to plasma ignition), 10 s plasma exposure time and 1 s plasma purge time. 100 sccm N_2 gas flow and 12 mTorr pressure conditions were used for the plasma exposure step. These are outlined in Table 2. The standard PEALD recipe used for the previously reported PEALD process using BTBAS and N_2 plasma[16] are also outlined in Table 2 for comparison. For investigating conformality, additional runs using extended precursor dose times of 500, 1000 and 2000 ms and plasma exposure times of 20, 40 and 80 s were performed. These additional runs were initially based on previous Monte Carlo simulations on conformality by Knoops et al.[48] and then further extended based on the results observed. Extended precursor purge time of 3 s and plasma purge time of 2 s were also implemented for the additional conformality runs in order to account for any CVD component that could arise in the extended PEALD recipes.

Table 2. Standard process parameters for the previously developed BTBAS process[16] and the DSBAS process developed in this work.

Process parameters	Precursor	
	BTBAS	**DSBAS**
Bubbler temperature (°C)	50	40
Precursor dose time (ms)	150	100
Plasma (N_2) exposure time (s)	10	10
Precursor reaction step (s)	3	3
Precursor purge time (s)	1	1
Plasma purge time (s)	1	1
Plasma (N_2) pressure (mTorr)	40	12
Plasma (N_2) gas flow (sccm)	100	100

4.3 Material analysis and characterization

SiN$_x$ films were deposited on planar c-Si substrates with a thin native oxide layer ($\sim$1.5 nm) for developing the PEALD process. The optical properties and film thickness of the deposited layers on c-Si substrates were measured using spectroscopic ellipsometry (SE). Ex-situ SE measurements were conducted using a J.A. Woollam Variable Angle SE with a VB-400 Control Module and an HS-190 Monochromator (1.2 – 6.5 eV). In-situ SE measurements were performed in vacuum at an incidence angle of 70° (1.2 – 5 eV). The optical model used consisted of a silicon substrate, $\sim$1.5 nm native oxide, and a silicon nitride layer fitted with a Cauchy dispersion relation in the optically transparent region for SiN$_x$ (1.2 – 4 eV). The surface roughness was assumed negligible for these PEALD films. Rutherford backscattering spectrometry (RBS) and elastic recoil detection (ERD) measurements were used to determine the film composition (stoichiometry) and mass density of SiN$_x$ deposited on planar c-Si substrates. The RBS and ERD measurements with subsequent data simulations were performed by AccTec B.V. and Detect 99 using a 1.8 – 2 MeV helium-ion beam. The areal densities of the elements were determined from raw data simulations. SiN$_x$ film composition on the planar c-Si substrates was also investigated with X-ray Photoelectron Spectroscopy (XPS) measurements using a Thermo Scientific K-Alpha spectrometer equipped with a Al Kα X-ray source (hv = 1486.6 eV). Note that the sensitivity factors, which are required for obtaining elemental concentrations, were previously determined for the XPS system used. Depth profiles were measured by sputtering with Ar$^+$ ions.

For investigating film conformality and wet-etch resistance on 3D substrate topographies, SiN$_x$ layers were deposited using PEALD on coupons containing high aspect ratio trench nanostructures (width $\sim$100 nm, height $\sim$450 nm, AR = 4.5 : 1) and analysed with cross-sectional TEM. These 3D nanostructures were created[37] by first depositing a thick SiO$_2$ film on a Si wafer using PECVD, that was subsequently etched into trench structures. The SiO$_2$ trench structures were then coated with a SiN$_x$ layer using high-temperature CVD, on which a SiO$_2$ layer was deposited using ALD. Coupons containing these trench based HARS were prepared and provided by Lam Research. A JEOL 2010F ultrahigh-resolution scanning TEM at 200 kV was employed to obtain cross-sectional images of the SiN$_x$ films deposited on the 3D trench nanostructures. The films were coated with a layer of spin-on epoxy to protect them from damage during sample preparation for TEM cross-sectional imaging. The samples were then placed on a Cu TEM grid, after which an energetic ion beam was used to mill and polish the samples at 30 kV, 100 pA and 5 kV, 40 pA, respectively. SiN$_x$ film thickness was measured at three regions of several trench nanostructures in the sample, namely at the planar *top* and *bottom* regions together with the vertical *bottom-side* region (see **Conformality** section, Figure 6A) by counting pixels in the TEM image. Conformality was determined by taking

the ratio of SiN$_x$ film thicknesses at the *bottom-side* and *bottom* of the trench to that at the *top* of the trench. The conformality values reported are the average of the results obtained across several trench nanostructures with the same aspect ratio. Uncertainties reported for the values were based on both the accuracy of the measurement and the variation between measurements conducted across several trench nanostructures of the same sample.

For obtaining wet-etch rates (WER) of films at planar and vertical surfaces of the 3D substrates, coupons containing the trench nanostructures with SiN$_x$ films deposited using PEALD were dipped in a dilute HF solution (HF : H$_2$O = 1 : 100) for 30 seconds. Two samples for TEM cross-sectional imaging were prepared from the same coupon, one before and one after the chemical wet-etch treatments. TEM measurements were conducted at the three aforementioned regions across several trench nanostructures of the same as-deposited and post wet-etch samples. The WERs at the aforementioned trench regions were determined by comparing the as-deposited and post wet-etch film thicknesses at those regions. The WER values reported are the average of the results obtained across several trench nanostructures with the same aspect ratio. Uncertainties reported for the values were based on both the accuracy of the measurement and the variation between measurements conducted across several trench nanostructures of the same sample. The WER and conformality values obtained using TEM for SiN$_x$ deposited on trench nanostructures were used as a basis for determining film quality and thickness uniformity at planar and vertical surfaces of the 3D substrates. Potential depletion of the etchant inside the trench was not taken into account in these experiments.

4.4 Results

4.4.1 PEALD of SiN$_x$ on planar substrates

ALD film growth: Growth per cycle (GPC) as a function of precursor dose time and plasma exposure time measured using in-situ SE are shown in Figure 2a and b, respectively. GPC as a function of precursor purge and plasma purge times are also shown in Figure 2c and d, respectively. An apparent saturation for the GPC (~0.08 Å) can be observed in Figure 2a for the precursor dose time. The GPC using DSBAS is relatively low (<0.1 Å) and its rapid stagnation as a function of dose time suggests that the precursor quickly occupies the available reactive surface sites. Contrary to this apparent saturation behaviour, the GPC as a function of N$_2$ plasma exposure time shows a soft saturation behaviour (Figure 2b). This differs from the corresponding trend of GPC for the SiN$_x$ PEALD process developed by Knoops *et al.*[16] using BTBAS. The GPC in that process peaked for short N$_2$ plasma exposure times and then gradually decreased to a
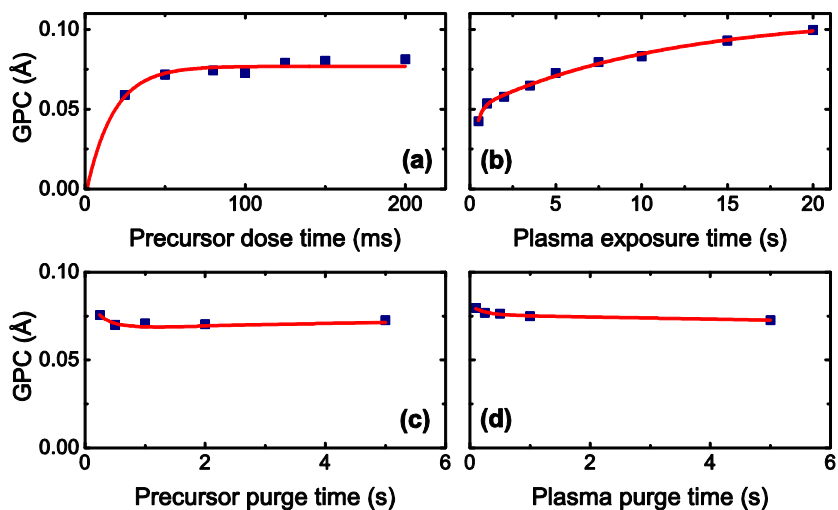
Figure 2. Growth per cycle (GPC) as a function of precursor dose time **(a)**, plasma exposure time **(b)**, precursor purge time **(c)**, and plasma purge time **(d)**. The default precursor dose, plasma exposure and purge times were 100 ms, 5 s and 5 s, respectively. The red lines serve as a guide to the eye.
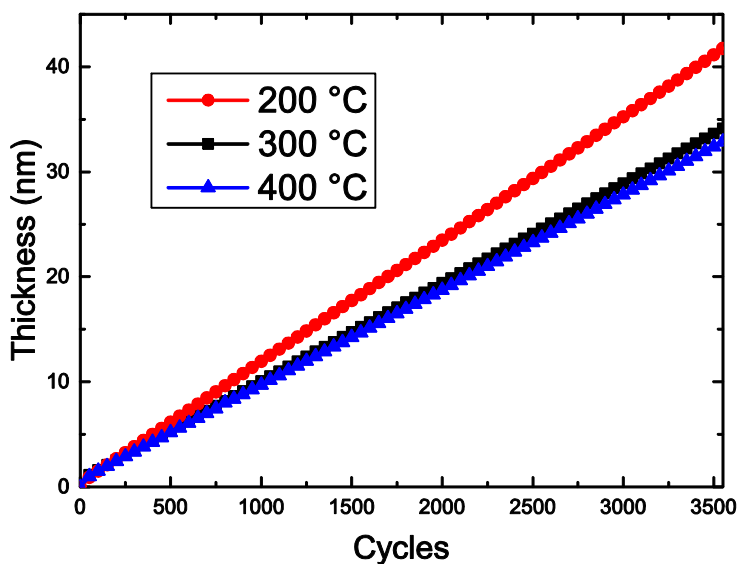
Figure 3. Film thickness as a function of the number of ALD cycles, as measured with in-situ spectroscopic ellipsometry (SE) for three different stage temperatures (200, 300 and 400 °C).

constant value as the plasma exposure times were increased. Despite the non-ideal soft saturation observed using DSBAS, SiN$_x$ film growth was linearly dependent on the number of ALD cycles, while showing almost no nucleation delay, depicted in Figure 3. The slope of the plots is observed to decrease with temperature indicating a lower GPC at higher temperatures (see below).

On the basis of these exploratory saturation experiments, a standard process was defined whose parameters were outlined in Table 2. Ideally, all process parameters are chosen assuming that the GPC saturates at a particular value. From Figure 2, it can be observed how a precursor dose time of 100 ms and purge times of 1 s can be expected to yield saturated film growth. The observed soft saturation of the GPC as a function of the plasma exposure time implies that very long exposures (≥20 s) would result in film growth closer to saturation. This would result in long cycle times (≥30 s) which, considering the already low GPC, would eventually lead to a long deposition time (~20 hours) to grow SiN$_x$ films of ~30 nm (roughly the target thickness required for accurate material characterization via RBS, see Table 3). As a result, a plasma exposure time of 10 s was chosen for the standard process to obtain a feasibly productive cycle time (~20 s).

Effect of substrate temperature: SiN$_x$ film growth using DSBAS and N$_2$ plasma has been confirmed over a wide range of stage temperatures between 100 and 500 °C. This approximately corresponds to lower actual substrate temperatures[16] ranging between 100 and 360 °C (see Table 3 and Appendix 4, Table A4.1). Film growth and material properties have been characterised at several temperatures in this range. The results are outlined in Table 3 and graphically depicted in Figure 4. The growth properties are presented in terms of both the film thickness deposited per cycle (Figure 4a) and the number of silicon atoms deposited per nm^2 per cycle (Figure 4b). The material properties are shown in terms of the N/Si ratio (Figure 4c), mass density (Figure 4d) and impurity content (Figure 4e and f). Note that the results obtained using DSBAS in this work are presented in Figure 4 with the results obtained in previous work for SiN$_x$ deposited using BTBAS and N$_2$ plasma[16] in order to facilitate comparison between the material properties of films grown using the two processes.

Figure 4a shows how DSBAS yielded a fairly low, but constant film GPC (~0.1 Å) at various stage temperatures, with the exception of 100 °C where the GPC was higher (~0.2 Å). This increase in GPC is partly attributed to an increased impurity content ([C], [O] and [H]) at lower stage temperatures, as observed in Figure 4e and f. Figure 4b shows the number of deposited Si atoms per nm^2 per cycle, denoted as GPC [Si] (Si at./nm^2). Since the only source of silicon is the one Si-atom present in both precursor molecules, GPC [Si] can be considered as a more quantitative measure of precursor adsorption.

Table 3. GPC, refractive index at 2 eV, mass density, and elemental composition of ~30 nm thick SiN$_x$ films deposited using standard 100 ms DSBAS precursor dose and 10 s N$_2$ plasma exposure times at 12 mTorr N$_2$ plasma pressure and various stage temperatures (100 – 500 °C). Typical uncertainties are given in the first row. Bulk Si$_3$N$_4$ has a refractive index of 2.02 and a mass density of 3.2 g/cm^3.[49]

Stage temperature (°C)	Estimated actual substrate temperature (°C)	GPC (Å)	Refractive index	RBS					ERD
				Mass density (g/cm³)	#Si at. per nm² per cycle	N/Si	[C] at. %	[O] at. %	[H] at. %
100	100 ± 20	0.19 ± 0.02	1.86 ± 0.05	2.3 ± 0.1	0.43 ± 0.02	1.9 ± 0.1	11 ± 2	2 ± 1[a]	11 ± 1
200	180	0.12	1.93	2.7	0.37	1.4	3	3	8
300	240	0.10	1.98	2.9	0.35	1.3	2	3	5
400	310	0.09	1.99	3.1	0.35	1.4	2	1	5
500	360	0.10	1.97	3.1	0.37	1.5	<d.l.[b]	<d.l.[b]	5

[a] XPS measurements showed this film had a high level of oxygen at the surface, which is likely due to the low mass density of the film that leads to significant post-deposition oxidation (see Appendix 4, Figure A4.1).
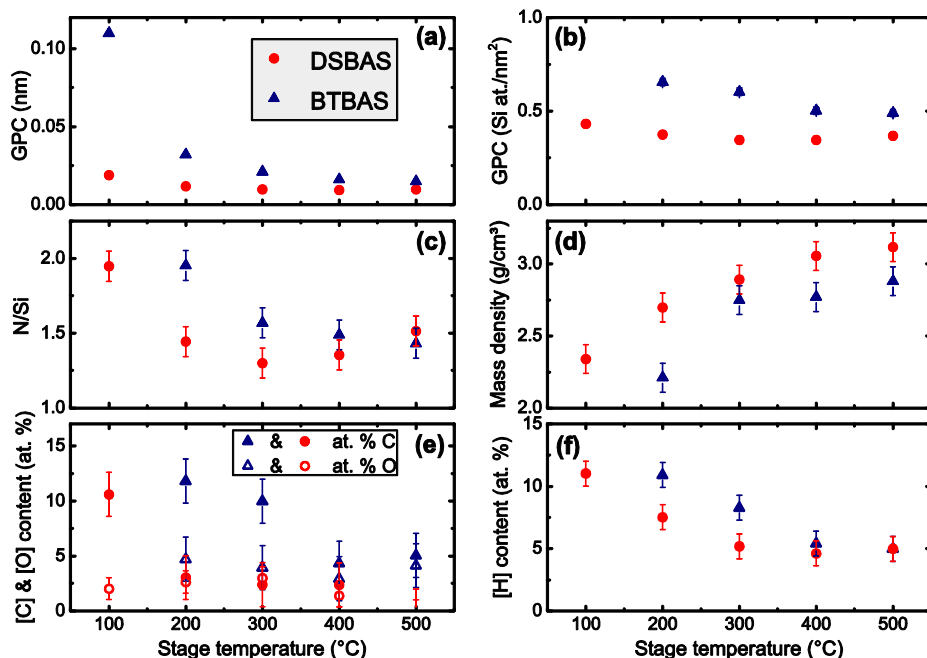[b] Values below detection limit (d.l.) of 2% for [C] and 1% for [O].

Figure 4. Material properties of SiN$_x$ films deposited using DSBAS compared to those obtained previously using BTBAS.[16] Growth-per-cycle (GPC) in terms of thickness **(a)**, GPC in terms of the number of deposited silicon atoms per ALD cycle **(b)**, the nitrogen to silicon ratio N/Si **(c)**, the mass density **(d)**, the contents of carbon [C] and oxygen [O] in atomic % **(e)**, and hydrogen content [H] in atomic % **(f)** as a function of stage temperature. Note that deposition conditions differ slightly for the BTBAS and DSBAS data series, primarily because of a difference in plasma pressure (12 mTorr for DSBAS, 40 mTorr for BTBAS). Results in **(a)** have been obtained via Spectroscopic Ellipsometry (SE), in **(b)**-**(e)** via Rutherford Backscattering Spectrometry (RBS) and in **(f)** via Elastic Recoil Detection (ERD).

Like GPC, the values for GPC [Si] using DSBAS remain fairly unchanged at ~0.4 Si at./nm^2 with an increasing stage temperature. Both GPC and GPC [Si] are observed to be higher using BTBAS compared to those obtained using DSBAS at the standard conditions investigated for the two precursors. The differences are more pronounced at lower stage temperatures, while at 500 °C they have been greatly reduced. The fairly unchanging trend in GPC and GPC [Si] exhibited by DSBAS differs from the trend observed for films grown using BTBAS where GPC and GPC [Si] monotonically decrease as a function of increasing stage temperature.

From Figure 4c, it can be observed that the N/Si ratio for films deposited using DSBAS is very close to that of stoichiometric Si$_3$N$_4$ (1.33), especially at 300 and 400 °C (1.3 and 1.4, respectively). At both low (≤200 °C) and high (500 °C) stage temperatures, more nitrogen-rich SiN$_x$ films were deposited. The highest mass density of 3.1 g/cm^3 was

obtained at a stage temperature of 500 °C, as seen in Figure 4d, even though the film was more nitrogen-rich in composition at that temperature. The highest obtained density is very close to the mass density of bulk Si$_3$N$_4$ (∼3.2 g/cm^3).[49] The high refractive indices, close to 2.0, measured using ex-situ SE at stage temperatures >300 °C (shown in Table 3) also indicate high film quality.

The high quality is further corroborated by the low impurity content ([C], [O] and [H]) of the DSBAS grown films, especially at stage temperatures >200 °C. At 500 °C, both [C] and [O] levels have decreased to values below the detection limit of 2% and 1%, respectively. However, at 100 °C, the [C] and [H] levels were significantly higher (11% for both) compared to those at higher temperatures (>200 °C), as observed in Figure 4e and f, respectively. The film density at 100 °C is quite low (∼2.3 g/cm^3) which is most likely due to the aforementioned high [C] and [H] levels together with post-deposition oxidation that the films may have undergone upon exposure to the atmosphere.

With respect to the high quality of films obtained previously using the BTBAS process, it can be concluded that the film quality yielded by the DSBAS process is generally very high. The density, N/Si ratio and refractive index values of the DSBAS grown films tend to be closer to those of bulk Si$_3$N$_4$ compared to BTBAS grown films, with an exception for the higher N/Si ratio at 500 °C. The N/Si ratio trend for DSBAS differs from that for BTBAS which shows a monotonic decrease in N/Si as a function of increasing stage temperature, as observed in Figure 4c. For the conditions investigated, it can be concluded that using DSBAS as a precursor for PEALD of SiN$_x$ yields denser films with lower impurities, and hence, higher quality films at all stage temperatures compared to using BTBAS as the precursor.

To verify whether SiN$_x$ film composition remained uniform throughout the entire layer of the deposited films, depth profiles were measured using alternating XPS measurements and Ar$^+$ ion sputter steps. The constant N and Si atomic contents, as observed in Figure 5, indicate a uniform film stoichiometry (i.e., constant N/Si ratio) throughout the entire film thickness. Elevated [C] and [O] levels can be observed near the film surface, indicating some surface contamination takes place after the deposited films are exposed to the atmosphere.

Effect of plasma pressure: As mentioned before, the residence time is a key parameter that can influence the redeposition effect and hence, govern growth properties and material quality during PEALD.[42] Since the residence time was shown to depend on plasma pressure, which was not the same for the two processes compared, the effect of similar plasma pressures on material properties of both BTBAS and DSBAS grown SiN$_x$ films was investigated (at stage temperature of 200 °C). These results are outlined in

Table 4**.** The films deposited using DSBAS show higher refractive indices and lower impurity contents at both 12 and 40 mTorr, compared to the films deposited using BTBAS at similar pressures. Furthermore, the GPC using BTBAS increases significantly when the plasma pressure is increased from 13 to 40 mTorr, whereas the GPC using DSBAS remains unaffected. The [C] of the films deposited using both precursors increases with pressure, indicating elevated impurity content at higher plasma pressure.
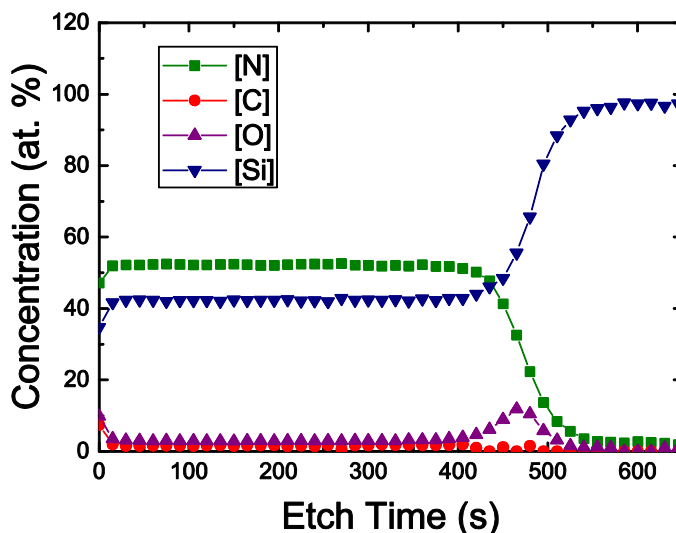

Figure 5. Depth profile of a SiNx film deposited using DSBAS and N_2 plasma at a stage temperature of 400 °C, as determined by XPS. Minor oxidation and C contamination levels can be observed near the film surface. The native oxide layer present on the c-Si substrate shows up as an elevated O content at ~450 s.

4.4.2 PEALD of SiNx on 3D substrates

Conformality: TEM images of as-deposited SiNx layers grown on 3D trench nanostructures (AR = 4.5 : 1) using DSBAS and N_2 plasma are shown in Figure 6 and their corresponding deposition conditions are outlined in Table 5. SiNx film thicknesses measured at the *top*, *bottom-side* and *bottom* regions of the trench together with film conformality (as % of film thickness at the *top*) are also depicted in Figure 6 and Table 5. In the first experiment, the film was deposited on 3D trench nanostructures using the standard recipe of 100 ms DSBAS dose and 10 s N_2 plasma exposure at 500 °C stage temperature and 12 mTorr plasma pressure. These standard conditions yielded bottom-side and bottom conformalities of 30% and 51%, respectively, as shown in Figure 6A.

Using Monte Carlo simulations, Knoops *et al.*[48] showed that in order to reach 100% conformality in HARS, generally higher precursor doses and/or longer plasma exposures

Table 4. GPC, refractive index at 2 eV, mass density and elemental composition of $\sim$30 nm thick SiN$_x$ films deposited at a stage temperature of 200 °C using standard dose times of 100 or 150 ms for the DSBAS or BTBAS precursor steps, respectively. All films were deposited using 10 s N$_2$ plasma exposure times but at different pressures in the reactor during plasma exposure. Typical uncertainties are given in the first and second rows, unless otherwise noted. A "–" means not measured.

Precursor	N$_2$ plasma pressure (mTorr)	GPC (Å)	Refractive index	XPS			Mass density (g/cm^3)	#Si at. per nm^2 per cycle	RBS			ERD
				N/Si	[C] at. %	[O] at. %			N/Si	[C] at. %	[O] at. %	[H] at. %
BTBAS	13	0.24 ± 0.02	1.91 ± 0.05	1.6 ± 0.2	6 ± 2	5 ± 2	–	–	–	–	–	–
BTBAS	40	0.32	1.83	1.7	9	5	2.2 ± 0.1	0.66 ± 0.02	2.0 ± 0.1	12 ± 1	4 ± 1	11 ± 1
DSBAS	12	0.12	1.93	1.2	4	4	2.7	0.37	1.4	3 ± 2	3	8
DSBAS	40	0.12	1.89	1.2	5	7	2.7	0.37	1.5	6	4	8
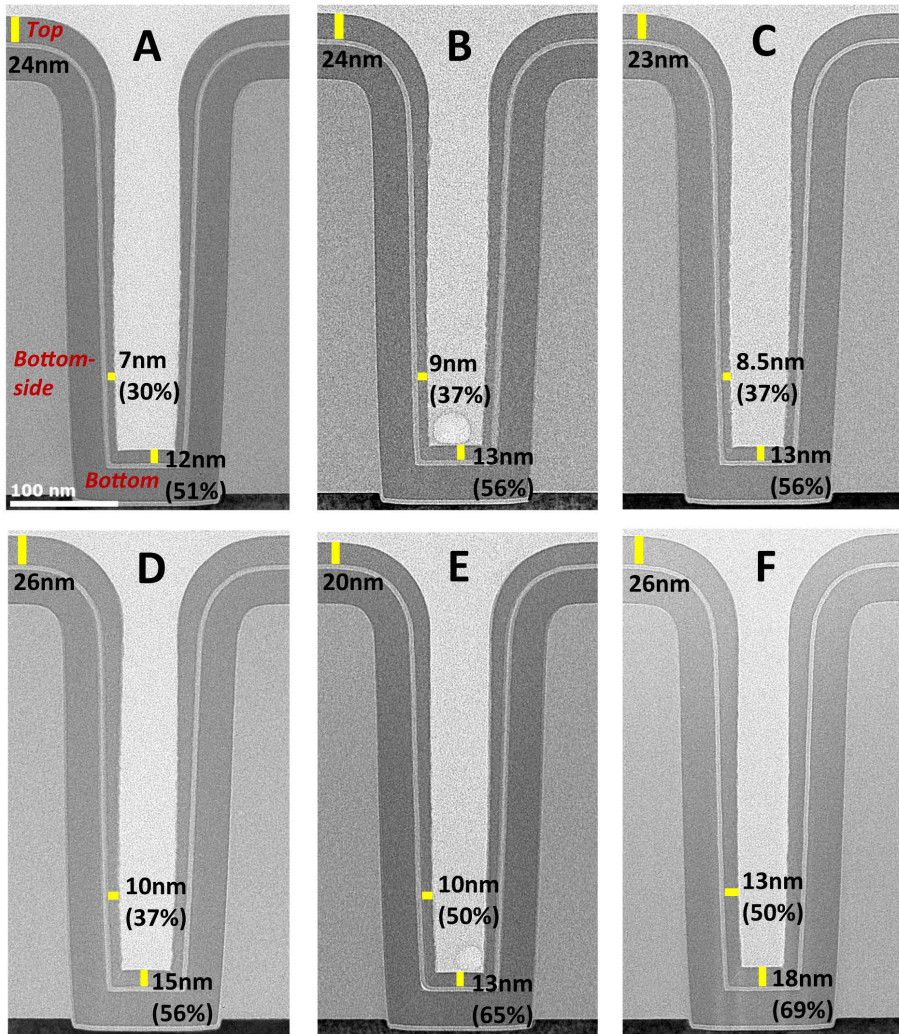
Figure 6. TEM images (A, B, C, D, E and F) of as-deposited SiN$_x$ layers grown on 3D trench nanostructures (AR = 4.5 : 1) using DSBAS and N$_2$ plasma at 500 $^\circ$C stage temperature and 12 mTorr plasma pressure. The deposition conditions for each image are outlined in Table 5. SiN$_x$ film thicknesses for all depositions are measured at three regions of the trench – Top, Bottom-side and Bottom – as indicated in image (A). SiN$_x$ film conformality at the bottom-side and bottom regions of the trench are indicated as a percentage of film thickness at the top in all images.

are needed compared to those used for obtaining saturation on planar substrates. Based on this and the low film conformalities exhibited by the standard recipe, extended precursor dose and/or plasma exposure times were used to deposit SiN$_x$ films on the 3D trench nanostructures (Figure 6B to F). The conformalities improved slightly to 37% and

Table 5. Conformality and wet-etch rates of SiN$_x$ films grown on coupons containing 3D trench nanostructures (AR = 4.5 : 1) using DSBAS and N$_2$ plasma at 500 °C stage temperature and 12 mTorr plasma pressure. The wet-etch rates are reported for SiN$_x$ films located at planar (*top, bottom*) and vertical (*bottom-side*) regions of the 3D substrate topographies after 30 s dip in an etchant solution of dilute hydrofluoric acid (HF : H$_2$O = 1 : 100). Typical uncertainties, which are based on both the accuracy of the measurement and the variation between measurements conducted across different trenches of the same coupon, are given in the first row.

TEM image	Precursor dose time (ms)	Plasma exposure time (s)	TEM thickness at the *Top* (nm)	As-deposited conformality (% of *Top*)		Wet-etch rate (nm/min)		
				Bottom-side	*Bottom*	*Top*	*Bottom-side*	*Bottom*
A	100	10	24 ± 1	30 ± 5	51 ± 5	0 ± 1	1 ± 1	0 ± 1
B	100	20	24	37	56	0	1	0
C	500	10	23	37	56	0	6	2
D	500	20	26	37	56	0	3	1
E	1000	40	20	50	65	2	3	1
F	2000	80	26	50	69	0	2	1

56% at the bottom-side and bottom, respectively, in accordance with the simulations[48] when extending either the precursor dose to 500 ms (Figure 6C), or the plasma exposure to 20 s (Figure 6B), or both simultaneously (Figure 6D). Doubling both the precursor dose to 1000 ms and plasma exposure to 40 s (Figure 6E) significantly improved bottom-side and bottom film conformalities to 50% and 65%, respectively. This trend of continued improvement in film conformality by extending the durations of both PEALD half cycles was the reason to further double the precursor dose and plasma exposure times to 2000 ms and 80 s, respectively (Figure 6F). However, no further improvements were observed as film conformalities of 50% and 69% were obtained at the bottom-side and bottom regions of the trench, respectively, which was also the most conformal film obtained in this work.

Wet-etch rate: WERs for SiN$_x$ films deposited on 3D trench nanostructures using DSBAS and N$_2$ plasma at 500 °C stage temperature (<400 °C actual substrate temperature) and 12 mTorr plasma pressure are outlined in Table 5. The WER values were determined by comparing the as-deposited and post wet-etch film thicknesses at the three trench regions depicted in Figure 6A. The deposited SiN$_x$ films seem to be highly etch resistant at the planar top and bottom regions of the trench as indicated by small or insignificant WER values (≤2 ± 1 nm/min) observed at those regions (Table 5). These low WERs indicate the deposition of high quality SiN$_x$ films on planar or horizontal surfaces of the 3D trench nanostructures, as observed in Figure 6. This is also corroborated by the high mass density (3.1 g/cm^3) exhibited by the film deposited on a planar c-Si substrate using the standard deposition condition (100 ms DSBAS, 10 s N$_2$ plasma), as outlined in Table 3. Additional RBS measurements were conducted for two SiN$_x$ films deposited on planar c-Si substrates using extended conditions (500 and 1000 ms DSBAS, 20 and 40 s N$_2$ plasma, respectively) which also showed high mass densities (~3.1 g/cm^3) and near-stoichiometric N/Si ratios (~1.4) for both films. This corroborates the low WERs that were also observed for SiN$_x$ films deposited on 3D trench nanostructures using the extended deposition conditions. It is noted that the mass densities of the two SiN$_x$ films deposited on planar c-Si substrates using extended precursor dose and plasma exposure conditions remained high even though slightly elevated [C] and [O] levels (~4% for both) were observed for the films at those conditions.

The WERs observed at the bottom-side region of the trench are somewhat higher than those at the two planar trench regions for all SiN$_x$ films, indicating a reduced HF-etch resistance at the vertical trench surfaces. However, they are small in absolute magnitude (≤3 nm/min) indicating a high HF-etch resistance for all SiN$_x$ films for both planar and vertical surfaces. Only the film deposited using 500 ms DSBAS dose and 10 s N$_2$ plasma exposure (Table 5, TEM image C) is an exception. The bottom-side WER for this particular film is significantly high (~6 nm/min) and the film was deposited after
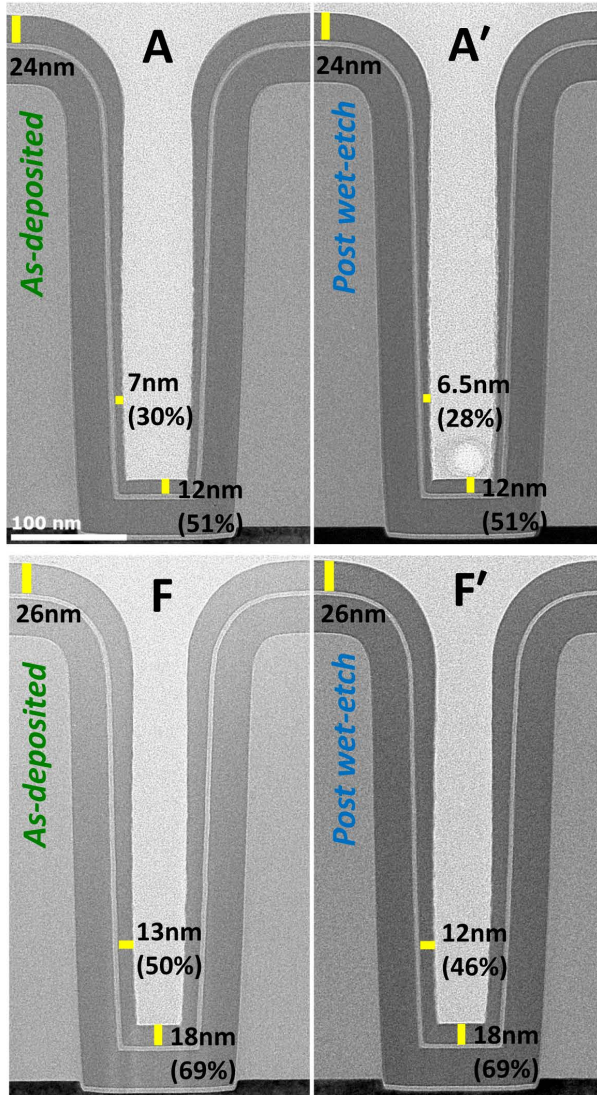
Figure 7. TEM images of (A, F) as-deposited and (A', F') post wet-etch (in 30 s dilute HF) SiNₓ films grown on 3D trench nanostructures (AR = 4.5 : 1) using DSBAS and N₂ plasma at 500 °C stage temperature and 12 mTorr plasma pressure. The deposition conditions for images (A) and (F) are outlined in Table 5. SiNₓ film conformality at the bottom-side and bottom regions of the trench are indicated as a percentage of film thickness at the top in all images.

extending only the precursor dose time from 100 to 500 ms in the standard recipe, without extending the plasma exposure time. When the plasma exposure time was also extended from 10 to 20 s for the extended 500 ms precursor dose (Table 5, TEM image D), the WER was seen to decrease (~3 nm/min). This indicates that an increased

precursor dose requires a corresponding increase in plasma exposure in order for the SiN_x films to retain their etch resistance at the vertical surfaces within a 3D structure. A high film quality was observed in general with the lowest WERs (≤2 nm/min) exhibited by the standard (100 ms DSBAS, 10 s N_2 plasma) and the most extended (2000 ms DSBAS, 80 s N_2 plasma) deposition conditions, as seen in Figure 7. The most extended deposition condition resulted in optimum SiN_x having both low WERs and the highest conformality on 3D trench nanostructures in this work. WERs at the regions inside a trench nanostructure (bottom-side and bottom) were always higher than the region at the trench entrance (top). Although any potential depletion of etchant inside the trench was not taken into account, the comparatively higher WERs at the regions inside the trench ensured etchant penetration to the bottom of the trench nanostructures. Furthermore, non-existence of lower WERs at the regions inside the trench indicated the absence of any delay in wetting of the etchant on the film surfaces within the trench. Therefore, the wetting of the etchant was assumed to occur instantaneously relative to the large timescale (30 s) of the etch treatment.

4.5 Discussion

PEALD of SiN*$_x$ *on planar substrates: The results on planar substrates indicate that high quality SiN_x films with properties relatively close to that of bulk Si_3N_4[49] can be obtained using DSBAS as the precursor for PEALD of SiN_x. This is demonstrated by stoichiometric N/Si ratios (between 1.3 and 1.5), high mass densities (>2.9 g/cm^3) and low impurity contents ([C] <2% , [O] <3% and [H] ~ 5%) exhibited by the SiN_x films deposited at stage temperatures between 300 and 500 °C.

In Figure 2b, the GPC as a function of N_2 plasma exposure time was seen to exhibit soft saturation using DSBAS as the precursor for depositing SiN_x. The GPC was modelled by fitting two exponential functions involving two different time constants, $\tau_1 \approx 0.3$ s and $\tau_2 \approx 11$ s (see Appendix 4, Equation A4.1). This indicates that the creation of reactive sites slowed down but did not completely stop with increase in N_2 plasma exposure time. The exact nature of these reactive surface sites is not clear at the moment. Previous studies conducted using density functional theory (DFT) have shown that precursor adsorption is promoted on undercoordinated surface sites, such as nitrogen dangling bonds.[41] Both experimental results and first-principles calculations reported by Ande et al.[41] indicated that the use of an N_2 plasma can generate such undercoordinated surface sites, which are speculated to be the reactive sites on which DSBAS adsorption occurs in this work. Similar soft saturation of GPC as a function of N_2 plasma exposure has been recently reported by Weeks et al.[40] for PEALD of SiN_x using neopentasilane and trisilylamine as precursors. Both precursor molecules are terminated by silyl (SiH_3) groups which could give rise to a Si-H$_x$ terminated surface after precursor adsorption.

The DSBAS molecule also consists of a silyl group (and one amino (N(^{s}Bu)$_2$) ligand, as shown in Figure 1b) in addition to exhibiting a similar soft saturation behaviour during N$_2$ plasma exposure. Based on these similarities, it could be speculated that DSBAS precursor adsorption following an N$_2$ plasma step results in a surface closely resembling a Si-H$_x$ terminated surface, which is generated by the two aforementioned SiH$_3$ terminated precursors. Such a surface could be generated by the one-step elimination of the sole amino ligand during DSBAS adsorption that has been reported to occur for ALD processes employing this precursor.[38,50]

On the other hand, when BTBAS was used as the precursor for depositing SiN$_x$ in previous work,[16] the GPC as a function of N$_2$ plasma exposure time exhibited a different behaviour from soft saturation. The GPC was reported to undergo an initial rapid overshoot followed by a gradual decrease to a constant (or saturated) value as the N$_2$ plasma exposure time was increased.[16] Unlike the DSBAS molecule which has one amino ligand and a silyl group, the *bis*-aminosilane BTBAS molecule consists of two amino (NH^{t}Bu) ligands and a silanediyl (SiH$_2$) group, as shown in Figure 1a. DFT studies on the surface chemistry of BTBAS during ALD have shown that it involves the sequential elimination of primary and secondary NH^{t}Bu ligands,[51,52] while DSBAS undergoes the elimination of just one N(^{s}Bu)$_2$ ligand.[38,50] Experimental studies on the surface chemistry of the SiN$_x$ ALD process employing BTBAS and N$_2$ plasma[43] confirmed that a part of the amino ligands are liberated as gas-phase NH$_2^t$Bu species during BTBAS adsorption while a part remains on the surface as NH^{t}Bu. Consequently, BTBAS precursor adsorption can be considered to generate a more amino ligand terminated surface compared to a more Si-H$_x$ (or conversely, amino ligand deficient) surface hypothesised earlier for DSBAS. Previous work by Knoops et al.[42] and recent investigation by Bosch et al.[43] demonstrate that the amino ligands remaining on the surface after a BTBAS precursor step get dissociated into reactive fragments (e.g., C$_2$N$_2$, C$_3$H$_8$, HCN, etc.) during the subsequent N$_2$ plasma step. These fragmented ligand species can then be redeposited as impurities on the growing film surface, which is manifested as the initial rapid overshoot in GPC reported for BTBAS,[16] but not observed in this work for DSBAS. As a result, the NH^{t}Bu terminated surface after BTBAS adsorption could undergo a more prominent redeposition effect during N$_2$ plasma exposure compared to the more amino ligand deficient surface speculated for DSBAS. This may explain the lower total GPC (Figure 4a), smaller impurity content ([C] and [H], Figure 4e and f) and consequently higher film density (Figure 4d) observed for SiN$_x$ films deposited using DSBAS compared to previous results obtained using BTBAS.

The one-step ligand elimination process for DSBAS[38,50] entails overcoming a single energy barrier compared to the two-step counterpart process for BTBAS[51,52] where two energy barriers need to be overcome. The sequential two-step ligand elimination for

BTBAS may be incomplete at low temperatures causing more NH^{t}Bu ligands to remain on the surface after BTBAS dosage. Conversely, fewer amino ligands may be left on the surface after a precursor dose step using DSBAS instead of BTBAS, with the difference becoming more prominent on decreasing the stage temperature. The more amino ligands remaining on the surface after precursor adsorption, the greater the extent of ligand fragmentation during plasma exposure and the larger the effect of redeposition. Species that redeposit on the surface can be again removed by the plasma, and these redeposition and removal processes occur continuously until the fragmented species are flushed out of the reaction chamber.[42] High temperatures could be speculated to enhance the removal process by facilitating thermal desorption of redeposited species while low temperatures could have the opposite effect and lead to more impurity redeposition. This may account for the significantly higher impurity contents ([C] and [H], Figure 4e and f) observed at low stage temperatures (< 300 °C) using BTBAS that results in a much lower film density (Figure 4d) and a more elevated total GPC (Figure 4a) compared to DSBAS. Conversely, thermally enhanced desorption of redeposited species and/or a more complete two-step ligand elimination process may occur for BTBAS at high temperatures (>300 °C), which lowers redeposition and leads to SiN$_x$ film properties approaching those observed for DSBAS.

PEALD of SiN$_x$ on 3D substrates: SiN$_x$ films deposited on 3D trench nanostructures (AR = 4.5 : 1) using standard DSBAS and N$_2$ plasma conditions (Table 5, TEM image A) yielded sub-optimal bottom-side and bottom conformalities (30% and 51%, respectively, Figure 6A). This indicates that the film GPCs at the bottom-side and bottom regions of the 3D trench nanostructures were significantly lower than the GPC at the top. Increase in precursor dose and/or plasma exposure times were subsequently implemented with the aim of ensuring film GPC, and consequently film thickness, were the same at all regions of the trench nanostructures. Simultaneously extending both precursor dose and plasma exposure conditions (Table 5, TEM images D and E) seemed to offer a route towards improving bottom-side and bottom film conformalities (Figure 6D and E). However, this trend did not continue at a certain point when further extension in both precursor dose and plasma exposure times (from 1000 to 2000 ms and 40 to 80 s, respectively) no longer improved bottom-side and bottom conformalities (Figure 6E and F). This observation can potentially be explained by the combined role played by three factors during SiN$_x$ deposition on such 3D substrates.

A part of the reason could be due to the previously mentioned aspect of soft saturation observed for the GPC as a function of N$_2$ plasma exposure time. A continued increase in SiN$_x$ film growth rate was observed when increasing the N$_2$ plasma exposure time to 40 and 80 s. This may cause the GPC at the top to exceed those at the bottom-side and bottom regions of the trench nanostructures, thereby yielding non-conformal

films. Another reason could be due to the recombination of growth species at the vertical surfaces near the top of the trench. The ALD process developed in this work for depositing SiN_x is an N_2 plasma based process whereby atomic N radicals generated in the plasma are deemed as important contributors towards film growth.[25] These charge-free N radical species are isotropic or non-directional in nature, which means that they can collide and recombine at the vertical surfaces of the trench nanostructures before reaching the bottom regions of the trench. Kessels et al.[53,54] estimated the recombination loss probability of N radicals on SiN_x surfaces to be of the order of $\sim 10^{-2}$. Knoops et al.[48] identified that recombination losses of plasma radicals at the surfaces within a HARS during PEALD can lower the radical flux at the bottom regions of the HARS. This means that the flux of growth species comprised of N radicals is reduced at the bottom regions of the 3D trench nanostructures, which causes film GPC in those regions to be lower than that at the top. This GPC discrepancy between the top and bottom regions of the trench lowers film conformality. Finally, anisotropic ion bombardment which is a distinct feature of plasma ALD processes at such low pressures[27] can also play a role behind the low conformalities. N_2^+ ions generated in the plasma are charged species that are accelerated vertically downwards by the plasma sheath formed above the substrate. This vertically directed or anisotropic nature of N_2^+ ion bombardment can preferentially generate more reactive sites on the planar or horizontal surfaces of 3D trench nanostructures than on the vertical sidewalls. Therefore, the GPCs at the planar surfaces exceed those at the vertical ones which subsequently lowers film conformality within the 3D trench nanostructures. Similar low conformalities were also observed by King[25] and Weeks et al.[40] who also used N_2 plasma for PEALD of SiN_x on 3D trench nanostructures. Both works also attributed the low conformalities to the anisotropic nature of N_2^+ ion bombardment.

Despite the low conformalities, high quality SiN_x films were obtained which was demonstrated by the low WERs exhibited by nearly all the films deposited on 3D trench nanostructures. The WERs at the vertical trench sidewalls are slightly higher than those at the planar or horizontal trench surfaces. This could be due to the anisotropic nature of N_2^+ ion bombardment, which preferentially improves film properties at horizontal surfaces more than those at vertical ones. The trade-off between high conformality and high quality (i.e., low WERs, high density) observed for SiN_x films deposited on 3D substrate topography in this work seems to be a generally observed phenomenon for ALD processes of SiN_x.[55,56] Processes employing chlorosilane precursors and NH_3 gas or NH_3 plasma report films having high conformality but low film quality (i.e., high WERs, low density),[15,36,37] whereas those using an organosilane precursor and N_2 plasma report films with the properties reversed.[25,40] The latter is consistent with the results obtained in this work.

4.6 Conclusions

A new PEALD process for SiN$_x$ was developed using Di(Sec-ButylAmino)Silane (DSBAS, SiH$_3$N(^{s}Bu)$_2$) and N$_2$ plasma. Material properties were analysed over a wide stage temperature range (100 – 500 °C) and compared with those obtained in our previous work for SiN$_x$ deposited using Bis(Tert-ButylAmino)Silane (BTBAS, SiH$_2$(NH^{t}Bu)$_2$) and N$_2$ plasma. High quality films were obtained on planar substrates using DSBAS and N$_2$ plasma, with the best films showing high density (~3.1 g/cm^3) approaching that of bulk Si$_3$N$_4$ and low [C], [O] and [H] impurity levels at low substrate temperature (<400 °C). DSBAS, having one amino ligand and a silyl group, is hypothesized to leave a more amino ligand deficient surface after precursor adsorption compared to BTBAS that has two amino ligands and a silanediyl group. As a result, a lower redeposition effect during the subsequent N$_2$ plasma step could take place for DSBAS which could account for the denser SiN$_x$ films having lower impurity contents compared to those obtained previously using BTBAS. The process developed using DSBAS was also used for depositing SiN$_x$ films on high aspect ratio (4.5 : 1) 3D trench nanostructures. Film conformality is not yet at desired levels of >95% and is attributed to the combined role played by nitrogen plasma soft saturation, radical species recombination and/or ion directionality during SiN$_x$ deposition on 3D substrates. However, high quality films were obtained on the 3D substrates as demonstrated by the low or insignificant wet-etch rates (WER ≤2 nm/min) observed at the top, sidewall and bottom trench regions of the most conformal film deposited at low substrate temperature (<400 °C). These observations are in line with similar results reported in the literature employing organosilane precursors and N$_2$ plasma for ALD of SiN$_x$ on 3D substrates.

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Appendix *4*

Table A4.1. The relation between stage temperature and substrate (planar c-Si wafers, coupons containing 3D trench nanostructures) temperature estimated via in-situ spectroscopic ellipsometry measurements and modelling.

Stage temperature (°C)	Wafer temperature (°C)	Coupon temperature (°C)
100	100 ± 20	-
200	180	-
300	240	-
400	310	-
500	360	310 ± 30

Table A4.1 shows the estimated actual wafer and coupon (containing 3D trench nanostructures with aspect ratio 4.5 : 1) temperatures for a range of set-point temperatures for the substrate stage/table inside the Oxford Instruments FlexAl reactor. The estimated temperatures are given for a process pressure of 12 mTorr which was the standard pressure used in this work. Note that the estimates were based on in-situ spectroscopic ellipsometry (SE) and the known temperature dependence of silicon was used for the ellipsometric determination of the temperature (J.A. Woollam temperature dependent ellipsometry model for silicon). Throughout Chapter 4, the stage temperature has been used unless otherwise mentioned.

Table A4.2. An overview of the purity and characteristics of the materials used in this work. The purity is defined via an assay by gas chromatography (GC), which means that a certain percentage of the volatile material which was eluted through the GC column was DSBAS.

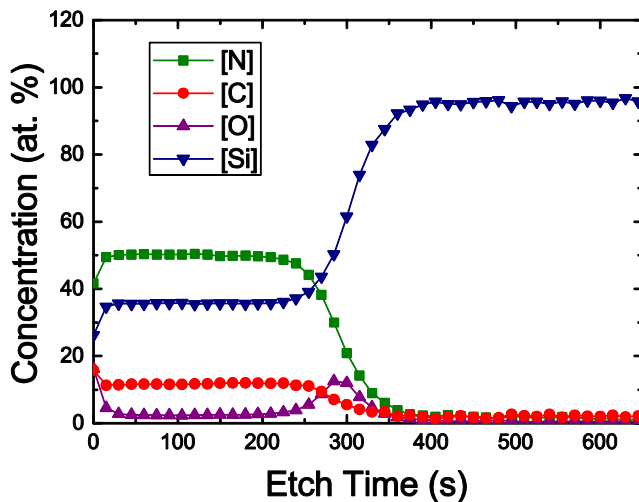| Material	Assay by GC
DSBAS	≥ 99.3 %
BTBAS	≥ 98.5 %

Figure A4.1. Depth profile of a SiNₓ film deposited using DSBAS and N₂ plasma at a stage temperature of 100 °C, as determined by XPS. Major oxidation and C contamination levels can be observed near the film surface. The native oxide layer present on the c-Si substrate shows up as an elevated O content at ~284 s.

Figure A4.1 shows that both [O] and [C] levels at the SiNₓ film surface are approximately 16 at. % for the film deposited at 100 °C stage temperature using 100 ms DSBAS precursor dose and 10 s N₂ plasma exposure conditions. This is significantly higher compared to the [O] and [C] levels at the SiNₓ film surface of approximately 10 and 7 at. %, respectively, for the film deposited at 400 °C stage temperature using 100 ms DSBAS precursor dose and 10 s N₂ plasma exposure conditions (see Figure 5 of Chapter 4).

Model of GPC as a function of N₂ plasma exposure time

The GPC as function of the plasma exposure time (in Figure 2b of article) showed soft saturation. The data was fitted with the following expression:

$$\text{GPC} = A_1 \left(1 - e^{-\frac{t}{\tau_1}} \right) + A_2 \left(1 - e^{-\frac{t}{\tau_2}} \right) \qquad \text{Eq. A4.1}$$

similar to the procedure employed by Knoops et al.[1] when fitting the GPC as a function of the N₂ plasma exposure time using the BTBAS precursor. In this function, A_1 and A_2 are derived weighing parameters with values $A_1 = 0.05$ and $A_2 = 0.06$, $\tau_1 = 0.3$ s and $\tau_2 = 11.0$ s. The adjusted R-square value, a measure of the accuracy of the fitting model, is 0.995.

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5

Tuning Material Properties of Oxides and Nitrides by Substrate Biasing during Plasma-Enhanced Atomic Layer Deposition on Planar and 3D Substrate Topographies
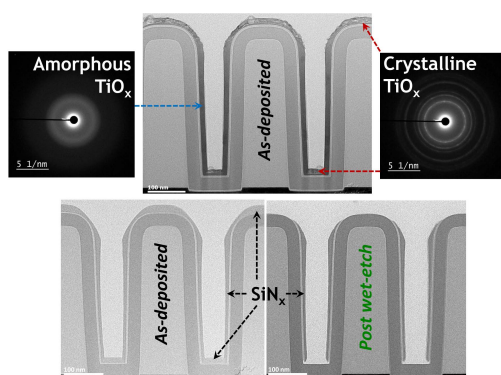
Oxide and nitride thin-films of Ti, Hf and Si serve numerous applications owing to the diverse range of their material properties. It is therefore imperative to have proper control over these properties during materials processing. Ion-surface interactions during plasma processing techniques can influence the properties of a growing film. In this work, we investigated the effects of controlling ion characteristics (energy, dose) on the properties of the aforementioned materials during plasma-enhanced atomic layer deposition (PEALD) on planar and 3D substrate topographies. A 200 mm remote PEALD system equipped with substrate biasing was used to control the energy and dose of ions by varying the magnitude and duration of the applied bias, respectively, during plasma exposure. Implementing substrate biasing in these forms enhanced PEALD process capability by providing two additional parameters for tuning a wide range of material properties. Furthermore, PEALD on 3D trench nanostructures with biasing induced differing film properties at different regions of the 3D substrate. On the basis of the results presented herein, prospects afforded by the implementation of this technique during PEALD, such as enabling new routes for topographically selective processing on 3D substrates (see images above), are discussed.

5.1 Introduction

The ubiquity of thin-films in emerging nanotechnology applications[1] together with device scaling using 3-dimensional (3D) architectures[2,3] place stringent requirements on nanoscale processing techniques used in thin-film deposition. Atomic layer deposition (ALD) is a well-known method for obtaining ultrathin films with precise growth control.[4] It is a cyclic deposition process based on sequential and self-limiting reactant dose steps for synthesizing thin-films in a layer-by-layer manner. The self-limiting surface reactions during the separate reactant exposures lead to excellent film uniformity on large area substrates and unparalleled conformality on high-aspect-ratio 3D nanostructures. In conventional thermal ALD, the energy needed for surface reactions to proceed is provided by substrate heating. An alternate source for the required energy can be obtained by using an energy enhanced ALD method known as plasma-enhanced atomic layer deposition (PEALD).[5] In PEALD, the substrate is exposed to species generated by a plasma during one of the reactant exposure steps of an ALD cycle.[5,6] These species constitute a mixture of highly reactive atomic and molecular neutrals (plasma radicals), photons, ions and electrons. The highly reactive plasma species generated during PEALD can provide an alternate source of the energy required for film growth. The high reactivity of the plasma species therefore, allows access to a parameter space such as low temperature deposition environments. Tuning material properties during film growth at a particular temperature is typically performed by varying either the substrate material or the reactants needed for film deposition. For PEALD at any given temperature, the various parameters of plasma operating conditions (e.g., reactant gas, flow rate, pressure, power, direct/remote source configuration, etc.) allow greater freedom in processing conditions for tuning the growth and material properties of thin-films.[6]

Apart from the contribution of highly reactive plasma radicals toward film growth during PEALD, the ions generated by the plasma can also play a significant role during film deposition.[5,6] Ion-surface interactions during plasma exposure are a characteristic feature of plasma-enhanced deposition techniques.[7–10] Additional energy can be provided to the deposition surface by the kinetic energy of ions impinging on the substrate. While plasma radicals can enable film growth through their high reactivity, the additional energy delivered to the deposition surface by ion bombardment can influence a wide range of material properties of the growing film. Examples reported in the literature include tailoring of the optical refractive index, electrical conductivity, mechanical stress, mass density, crystalline structure, morphology, surface roughness etc..[9,11,12] The limit to which ion-surface interactions can modify such properties depends on the energy, mass, reactivity, impingement rate (or flux) and dose (or net flux integrated over time) of ionic species impinging on the film surface.[7–9,13,14] Based on

the values of these parameters, various physical, chemical or combined physicochemical processes can occur at the surface and sub-surface regions of the film as the ions transfer energy and momentum during deposition.

The use of an inert gas (e.g., argon) leads to predominantly physical processes which include, but are not limited to, surface or bulk atom displacements, sub-surface implantation of incident ions or displaced surface atoms, desorption of adsorbed surface impurities from reactor background, etc.[8,9,14] The use of reactive gases (e.g., oxygen or hydrogen) involves an additional chemical or physicochemical component where the reactive ions can undergo chemical reactions forming, either stable products leading to film growth, or volatile products leading to film removal.[8,10] However, the processes and trends of property modulation also depend on many inherent characteristics of the growing film such as the bond energy, bond type (i.e., ionic, covalent or metallic), crystallization temperature, free energy difference between crystalline and amorphous phases and/or a combination of several of these parameters.[14–17] Given the multitude of factors that can play a role during ion-surface interactions, it is not a trivial or straightforward task to anticipate the trends in film characteristics as a result of varying the ion characteristics during deposition. Furthermore, the effects of ion-surface interactions have been extensively investigated in the literature for conventional flux-controlled processes,[18] such as physical vapour deposition (PVD) and plasma-enhanced chemical vapour deposition (PECVD), that lead to continuous film growth. In the surface-controlled process[18] of PEALD where self-limiting film growth occurs by sequential doses of a precursor and plasma activated co-reactant, ion-surface interactions only occur during the plasma exposure step of a PEALD cycle. Consequently, only the characteristics of those ionic species generated during plasma activation of the co-reactant can affect film properties in PEALD. These effects may or may not be different from those occurring in continuous growth process like PECVD in which both the precursor and co-reactant contribute species to the mixture of ions formed during deposition.

The first experimental investigation on the role of ions during PEALD was reported by Profijt *et al.*[19,20] in previous work conducted within our group. They looked into the effects of enhancing oxygen ion energies during PEALD on the growth and material properties of aluminum oxide, titanium oxide and cobalt oxide.[19,20] The films were deposited in a home-built remote plasma ALD tool equipped with substrate biasing. In a remote plasma source configuration, the ion energy can be controlled during plasma exposure by varying (or biasing) the substrate potential, either by adjusting the impedance between the substrate and ground, or by applying a voltage signal on the substrate.[19] Enhancing ion energies with substrate biasing during the plasma exposure step of PEALD was observed to have significant effects during film growth that were

material and/or process-specific. Increasing bias voltages during oxygen plasma exposure increased the growth rate and oxygen content of aluminum oxide films while lowering their mass density.[19] The residual stress of the deposited films was also observed to be altered from tensile to compressive with the use of substrate biasing. The growth rate, density and oxygen content of titanium oxide films deposited with substrate biasing during oxygen plasma exposure showed a similar behavior as aluminum oxide.[19,20] However, an additional effect was observed in case of titanium oxide where its crystalline phase could be gradually tailored from anatase to rutile with increasing bias voltages.[19,20] For cobalt oxide, the growth rate decreased and the film density increased at higher bias voltages while the films became slightly oxygen deficient.[19] The aforementioned results were demonstrated for film deposition only on planar substrates having a small area (1×1 inch pieces of Si wafer) and by applying substrate biasing for the entire duration of the plasma exposure step.

In this work, we continued the research on the role of ions during PEALD by analyzing the effects of enhanced ion energies on the material properties of films grown on both planar and 3D substrate topographies. The ion energy was enhanced during plasma exposure using a commercial remote plasma ALD system (Oxford Instruments FlexAL) equipped with radio-frequency (RF) substrate biasing. The effect of enhancing oxygen ion energies during PEALD of titanium oxide was re-investigated in this system on large area substrates (200 mm) using a different titanium precursor with additional material characterization, compared to the previous work conducted by Profijt *et al*.[19,20] This provided further insight on the effects of ion energy control during PEALD of titanium oxide. Additionally, the effects of varying the dose of higher energy ions on the growth and material properties of titanium oxide was also investigated. The effects of ion-surface interactions on material properties during PEALD were investigated for two more oxides, namely hafnium oxide and silicon oxide. Furthermore, the scope of our research on the role of ions during PEALD was expanded by looking into the effects of ion-surface interactions for another group of materials, namely the nitrides of titanium, hafnium and silicon deposited using different plasmas (i.e., hydrogen, argon/hydrogen and nitrogen). The oxides and nitrides of these three elements form dielectric or conductive materials that are used in a variety of applications ranging from optics,[21–23] photocatalysis,[24–26] sensors,[27,28] solar cells,[29–31] nano and microelectromechanical systems (NEMS/MEMS),[32–34] semiconductor logic and memory nodes,[35–41] self-aligned multiple patterning,[42,43] etc.. The diverse range of applications that are heavily reliant on the properties of these materials highlights the necessity for precise control over those properties during film deposition. Enhancing ion energies with substrate biasing during PEALD on planar substrates was observed to have pronounced effects on the growth and material properties of the aforementioned thin-films. A comprehensive analysis of these properties was undertaken by characterizing the growth rate, mass

density, refractive index (for dielectric materials), resistivity (for conductive materials), residual stress and surface roughness of the films deposited on planar substrates. The role of ion energy control on film microstructure and crystallinity was also investigated. The effect of enhanced ion energies on the thickness uniformity of materials deposited on large area planar substrates (200 mm Si wafer) was also investigated compared to previous work carried out on smaller substrates.[19,20] Owing to the material and/or process specific effects of substrate biasing observed in previous work, an empirical investigation comprised of an extensive characterization of film properties spanning six different materials was undertaken in this work. It was observed that substrate biasing can enhance the versatility of PEALD processes by providing two additional parameters (magnitude, duration/duty cycle of bias) for tuning a wide range of material properties. Furthermore, biasing during PEALD on 3D trench nanostructures effectively delineated the role of directional ion bombardment by inducing differing film properties at different (planar and vertical) regions of the 3D substrate. These results demonstrate the potential of substrate biasing during PEALD in enabling routes toward topographically selective[3] processing on 3D substrates.

5.2 Applying substrate bias during PEALD cycles

In a remote plasma ALD reactor configuration, the plasma source generating radicals and ions is located at a distance away from the substrate stage thus allowing the plasma and substrate conditions to be varied quite independently of each other. The ion flux impinging on the substrate can be increased by increasing the source power. When the substrate is exposed to the plasma, a positive space charge layer called the sheath is formed between the plasma and the substrate due to the difference in mobilities of the heavy ions and light electrons in the plasma. The voltage across the sheath (ΔV_{sheath}) is the difference between the plasma potential (V_p) and the substrate potential (V_{sub}). The sheath voltage repels electrons from the substrate into the plasma and accelerates ions towards the substrate resulting in so-called ion bombardment. At sufficiently low pressures, the ion mean free path is larger than the plasma sheath thickness, so the ions are accelerated over the full sheath width without undergoing collisions. This collisionless plasma sheath condition leads to the highly directional or anisotropic nature of ion bombardment. Typical sheath thicknesses for processing plasmas are on the order of $10^{-4} - 10^{-2}$ m, and therefore, the sheath does not follow the profile of 3D structures (e.g., trenches and vias) with micro- or nano-scale dimensions. As a result, directional ions accelerated through a collisionless sheath will mainly collide with substrate surfaces parallel to the sheath, e.g., the planar top and bottom surfaces of a 3D trench nanostructure and not its vertical sidewalls. The energy (E_i) of directional ions impinging on planar substrate surfaces is proportional to the sheath voltage, as shown in the following equation

$$E_i = q(\Delta V_{sheath}) = q(V_p - V_{sub})$$ Eq. 1

where q is the charge of an ion (assuming an electropositive plasma). When the substrate is placed on a grounded reactor table, it is at zero potential ($V_{sub} = 0$ V), so the sheath voltage equates to the plasma potential. Equation 1 indicates that the ion energy can be enhanced by increasing the sheath voltage. If the system is equipped with substrate biasing, i.e., by tuning the impedance between substrate table and ground or by connecting the substrate table to an additional power source, then the substrate potential can be set or biased to have a non-zero value ($V_{sub} \neq 0$ V).[19] When a sinusoidal radio-frequency (RF) voltage signal is applied to the substrate through a blocking capacitor, it acquires a negative average or DC offset value such that the net flux of ions and electrons to the substrate stage over one RF cycle is zero. The negative DC offset or time-averaged substrate bias voltage ($V_{sub} = -\langle V_{bias} \rangle$) can be increased by increasing the amplitude of the bias signal applied to the substrate table. This causes ΔV_{sheath} to increase which in turn enhances E_i, thus allowing the ion energy to be controlled during plasma exposure.

In order to perform PEALD with substrate biasing, an existing process can be modified by applying a bias on the substrate table during the plasma exposure step. The step sequences of the PEALD processes without and with substrate biasing are shown in Figure 1. The substrate bias can be applied for the whole duration (bias duty cycle = 100%, Figure 1b) or a part of the duration (0% < bias duty cycle < 100%, Figure 1c) of the plasma exposure step. For example, during a plasma exposure step of 10 s, the bias can be active for all 10 s (Figure 1b) or half of this duration (5 s) by applying it in an interleaved manner either at the beginning, middle or end (Figure 1c) of the plasma exposure step. Varying the duration of the applied bias translates to changing the dose or fluence[13,14,44] (i.e., particle flux integrated over time) of higher energy ions impinging on the substrate. Substrate biasing during PEALD can also be implemented in many other configurations (see Figure A5.1 and A5.2 in Appendix 5).

5.3 Experimental details

PEALD process conditions: Film deposition using PEALD was performed in an Oxford Instruments FlexAL reactor equipped with substrate biasing (Figure 2). The reactor consists of a radio-frequency (RF) power supply (13.56 MHz, up to 600 W) connected to a water-cooled copper coil wrapped around a cylindrical alumina tube to generate an inductively-coupled-plasma (ICP). This remote RF-ICP source generates the radicals and ions during the plasma exposure step of PEALD. For the specific FlexAL configuration, an additional external RF power supply (13.56 MHz, up to 100 W) can be connected to the reactor table that allows for substrate biasing (up to $\langle V_{bias} \rangle \approx$ −350 V at ~10 mTorr)
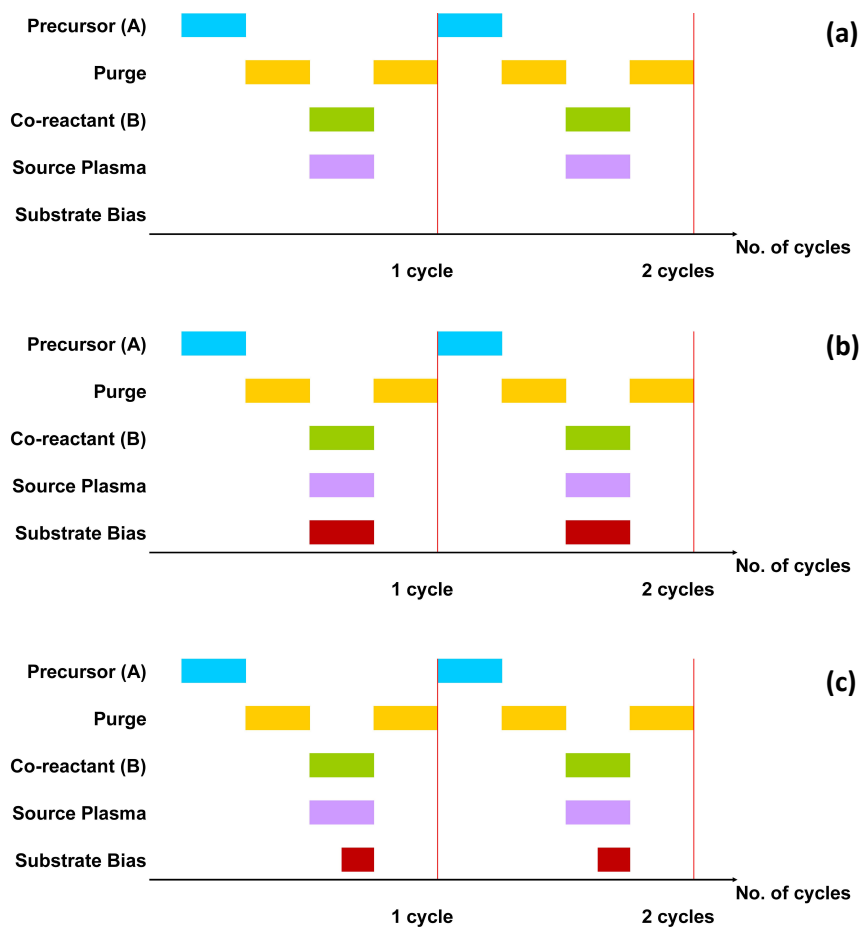
Figure 1. Step sequence for two-step *[AB]ₙ* plasma ALD cycles **(a)** without any substrate biasing during plasma exposure where the substrate table is grounded (Source Plasma "ON", Substrate Bias "OFF", bias duty cycle = 0%) **(b)** with substrate biasing during plasma exposure where the bias is applied for the full duration of the plasma exposure step (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%) and **(c)** with interleaved substrate biasing where the bias is applied for a fraction of the plasma exposure step (Source Plasma "ON", Substrate Bias "ON", 0% < bias duty cycle < 100%). *A* refers to the precursor dose step, *B* the co-reactant or plasma gas exposure step and *n* is the number of ALD cycles.

during plasma exposure. Both RF power sources were connected to the system via automated matching networks consisting of inductive and capacitive components. The FlexAL system provides a readout for $\langle V_{bias} \rangle$ when applying an RF bias signal during plasma exposure. Additionally, an oscilloscope was connected to the reactor table via a high-voltage probe from which sinusoidal RF bias voltage waveforms developing on the table could be measured. These oscilloscope measurements were used to independently verify $\langle V_{bias} \rangle$ readouts from the FlexAL system (within ± 5V). A base

pressure in the reactor chamber of $\sim 10^{-6}$ Torr was obtained using a turbo pump. A butterfly valve in front of the turbo pump controlled the effective pumping speed and functioned as an automated pressure controller. The chamber wall temperature was set to 150 °C while the substrate stage temperature was set between 150 and 500 °C. All substrates underwent a thirty minute heating step prior to commencing deposition in order to ensure substrate temperature stabilization. The precursor delivery lines were heated to 70 °C to prevent precursor condensation. The oxides and nitrides of Ti, Hf and Si were deposited without and with substrate biasing. The precursors, plasma gases and other PEALD process conditions for depositing the six materials are shown in Table 1. Existing PEALD processes for these six materials[30,40,41,45–48] were used for the runs without any biasing where the substrate table was grounded during the plasma exposure step. For the runs performed with substrate biasing, the PEALD processes were modified by applying an RF bias signal to the substrate table during the plasma exposure step. PEALD step sequences without (Figure 1a) and with substrate biasing (Figure 1b and c) were implemented. Details regarding PEALD process conditions are further outlined in Appendix 5.
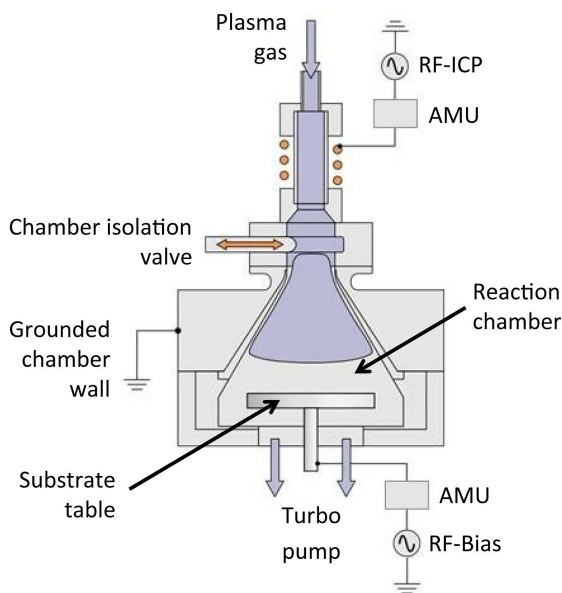

Figure 2. Schematic of an Oxford Instruments FlexAL system equipped with substrate biasing. A radio-frequency inductively-coupled-plasma (RF-ICP) source acts as the remote plasma generator allowing control over the flux of radicals and ions impinging on the substrate. A second RF power supply (RF-Bias) connected to the substrate table enables substrate biasing which allows control over the ion energy. Both RF power sources are connected to the system via automated matching units (AMU) consisting of inductive and capacitive components.

Table 1. PEALD process conditions for the materials deposited with and without substrate biasing during plasma exposure.

Material	TiO_x	TiN_x	HfO_x	HfN_x	SiO_x	SiN_x
Precursor	TDMAT[a]		TDMACpH[b]		BDEAS[c]	DSBAS[d]
Bubbler temperature (°C)	60		60		50	40
Precursor delivery	Bubbled with 100 sccm Ar		Bubbled with 100 sccm Ar		Vapor drawn	
Stage temperature (°C)	150 & 300	200	150	450	200	500
Precursor dose time (ms)	200	200	400	4000	175	500
Precursor reaction step (s)	-	-	-	-	1	3
Precursor purge time (s)	3	3	2	2	3	2
Plasma gas	O_2	$Ar + H_2$	O_2	H_2	O_2	N_2
Plasma gas flow (sccm)	100	10 + 40	100	100	100	100
Plasma pressure (mTorr)	9	6	15	30	15	11
RF-ICP power (W)	200	100	400	100	200	600
Plasma exposure time (s)	10	10	8	10	5	20
Plasma purge time (s)	3	4	3	4	2	3
⟨V_{bias}⟩ or average bias voltage (V)	0 to -254	0 to -255	0 to -280	0 to -210	0 to -295	0 to -103
Bias during plasma	All 10 s, Last 5 s	Last 5 s	Last 4 s	All 10 s, Last 5 s	All 5 s	Last 10 s

[a] TDMAT – $Ti(NMe_2)_4$ [b] TDMACpH – $CpHf(NMe_2)_3$ [c] BDEAS – $SiH_2(NEt_2)_2$ [d] DSBAS – $SiH_3N(^sBu)_2$

5.4 Thin-film characterization on planar and 3D substrates

Unless otherwise stated, the planar substrates used for depositing films with and without substrate biasing were single side polished (SSP) c-Si (100) substrates having a thin native oxide layer (~1.5 nm) for dielectric materials and SSP c-Si (100) substrates having a thick thermal oxide layer (~450 nm) for conductive materials. Film thicknesses between ~20 and ~80 nm were deposited for material characterization on planar substrates (except for SiO_x films which were ~200 nm). The optical properties and film thickness of the deposited layers on c-Si substrates were measured by means of spectroscopic ellipsometry (SE) using a J.A. Woollam M2000D rotating compensator ellipsometer (1.2 – 6.5 eV). SE measurements were also used to determine the thickness uniformity of films deposited on 200 mm planar c-Si wafers with and without substrate biasing by mapping film thickness at several locations across the wafers. For SiO_x and SiN_x films deposited with and without substrate biasing, the optical model used consisted of a silicon substrate, ~1.5 nm native oxide and the deposited layer parameterized with a Cauchy dispersion relation.[41,48] A similar three layer optical model was used for analyzing the ellipsometry data of TiO_x and HfO_x films grown with and without biasing where the deposited layer was parameterized using two Tauc-Lorentz oscillators.[19,49] For TiN_x and HfN_x, different models were used for the films deposited with and without biasing. The optical model used for the films grown without biasing consisted of a silicon substrate, ~450 nm thermal oxide and the deposited layer parameterized using one Drude, one Lorentz and one Tauc-Lorentz oscillator.[30] The TiN_x and HfN_x films deposited with biasing were parameterized using one Drude and two Lorentz oscillators.[49]

The root-mean-squared (RMS) surface roughness and mass density of the films deposited on planar substrates were analyzed using X-ray reflectometry (XRR) performed using a Bruker AXS D8 Advance system in the grazing incidence geometry with a Cu Kα x-ray source (radiation wavelength of 0.154 nm).[23] The thicknesses of the deposited films were also obtained with XRR which were in good agreement with the corresponding values obtained using SE. The residual stress levels of the deposited films were determined by means of wafer-curvature measurements at room temperature. A KLA-Tencor FLX 2320 system was used to determine the curvature of 3 inch double side polished (DSP) c-Si (100) wafers before and after deposition of the films. Based on the difference in curvature, the residual stress of the films deposited with and without substrate biasing was calculated using the Stoney equation.[19,23] A sign convention was used where positive values represented tensile and negative values represented compressive residual stress. Rutherford backscattering spectrometry (RBS) and elastic recoil detection (ERD) measurements were used to determine the composition (stoichiometry) of films deposited on planar SSP c-Si substrates with ~1.5 nm native

oxide. The RBS and ERD measurements with subsequent data simulations were performed by the company Detect 99 using a 1.8 – 2 MeV helium-ion beam. The areal densities of the elements were determined from raw data simulations. The crystallinity of films deposited on planar c-Si substrates was analyzed using grazing incidence x-ray diffraction (XRD). The measurements were performed in a PANalytical X'pert PRO MRD with a Cu Kα x-ray source (radiation wavelength of 0.154 nm) operated at an incidence angle of 0.5°. A JEOL ARM 200 transmission electron microscope (TEM) operated at 200 kV was used to analyze the microstructure of films deposited on planar TEM windows. These windows consisted of ~15 nm Si_3N_4 membranes coated with 5 nm of SiO_2 grown using ALD. This ensured a SiO_2 starting surface while maintaining transparency to the electron beam. Both bright-field TEM (BF-TEM) and high-angle-annular-dark-field scanning TEM (HAADF-STEM) modes were employed to characterize the samples in plan-view. Electrical sheet resistance measurements of conductive films deposited on c-Si substrates with ~450 nm thermal oxide were performed at room temperature using a Signatone four-point probe (FPP) in combination with a Keithley 2400 Source Measurement Unit (SMU) that acted as both current source and voltage meter. The electrical resistivity was obtained from the slope of the generated I-V curve and the film thickness deduced from the SE measurements.

For investigating material properties on 3D substrate topographies, films were deposited with and without substrate biasing during PEALD on coupons containing high aspect ratio trench nanostructures (width ~100 nm, height ~450 nm, AR = 4.5 : 1) and analyzed with cross-sectional TEM. These 3D nanostructures were created[41] by first depositing a thick SiO_2 film on a Si wafer using PECVD, that was subsequently etched into trench structures. The SiO_2 trench structures were then coated with a SiN_x layer using high-temperature CVD, on which a SiO_2 layer was deposited using ALD. Coupons containing these trench nanostructures were prepared and provided by Lam Research. A JEOL 2010F ultrahigh-resolution scanning TEM at 200 kV (Nanolab Technologies) was employed to obtain cross-sectional images of the films deposited on the 3D trench nanostructures. The films were coated with a layer of spin-on epoxy to protect them from damage during sample preparation for TEM cross-sectional imaging. The samples were then placed on a Cu TEM grid, after which an energetic ion beam was used to mill and polish the samples at 30 kV, 100 pA and 5 kV, 40 pA, respectively. The deposited film thickness was measured at three regions of several trench nanostructures in the sample, namely at the planar *top* and *bottom* regions together with the vertical *bottom-side* region (see Figure A5.3 in Appendix 5) by counting pixels in the TEM image. Conformality was determined by taking the ratio of film thicknesses at the *bottom-side* and *bottom* of the trench to that at the *top* of the trench. The conformality values reported are the average of the results obtained across several trench nanostructures with the same aspect ratio. For obtaining wet-etch rates (WER) of silicon nitride films at

planar and vertical surfaces of the 3D substrates, coupons containing the trench nanostructures with films deposited with and without substrate biasing were dipped in a dilute hydrofluoric acid solution (HF : H_2O = 1 : 100) for 30 seconds. Two samples for TEM cross-sectional imaging were prepared from the same coupon, one before and one after the chemical wet-etch treatments. TEM measurements were conducted at the three aforementioned regions across several trench nanostructures of the same as-deposited and post wet-etch samples. The WERs at the aforementioned trench regions were determined by comparing the as-deposited and post wet-etch film thicknesses at those regions. The WER values reported are the average of the results obtained across several trench nanostructures with the same aspect ratio. Uncertainties reported for the values were based on both the accuracy of the measurement and the variation between measurements conducted across several trench nanostructures of the same sample. Potential depletion of the etchant inside the trench was not taken into account in these experiments.

5.5 Results

5.5.1 PEALD of oxides on planar substrates

Titanium oxide (TiOx): The growth and material properties of TiO_x films deposited on planar substrates at 300 °C were investigated for $\langle V_{bias} \rangle$ between 0 V and -254 V applied during the O_2 plasma exposure step. Figure 3 shows these properties in terms of the growth per cycle (GPC), refractive index, mass density, residual stress and surface roughness expressed as a function of $\langle V_{bias} \rangle$ applied during plasma exposure. The solid symbols are for films deposited with $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s plasma exposure step (bias duty cycle = 100%, Figure 1b) while the hollow symbols denote films deposited with $\langle V_{bias} \rangle$ applied in an interleaved manner, i.e., during the last half (5 s) of the 10 s plasma exposure step (bias duty cycle = 50%, Figure 1c). outlines additional growth and material properties from RBS analysis for the films deposited with and without substrate biasing. The growth properties are outlined in terms of the number of titanium and oxygen atoms deposited per nm^2 per cycle (GPC [Ti] and GPC [O], respectively) while the material properties are outlined in terms of the O/Ti ratio and impurity content ([H] and [C] at. %). The crystalline properties of the TiO_x films are depicted in Figure 4 which shows grazing incidence XRD patterns for films deposited at 300 °C with $\langle V_{bias} \rangle$ ranging from 0 V to -254 V. Figure 4a denotes patterns for $\langle V_{bias} \rangle$ applied for the entire 10 s O_2 plasma exposure step while Figure 4b shows results for $\langle V_{bias} \rangle$ applied during the last half (5 s) of the 10 s plasma exposure step. The microstructure of the TiO_x films can be visualized in Figure 5 which shows plan-view HAADF STEM images for films deposited on planar TEM windows at 300 °C with and without substrate biasing.
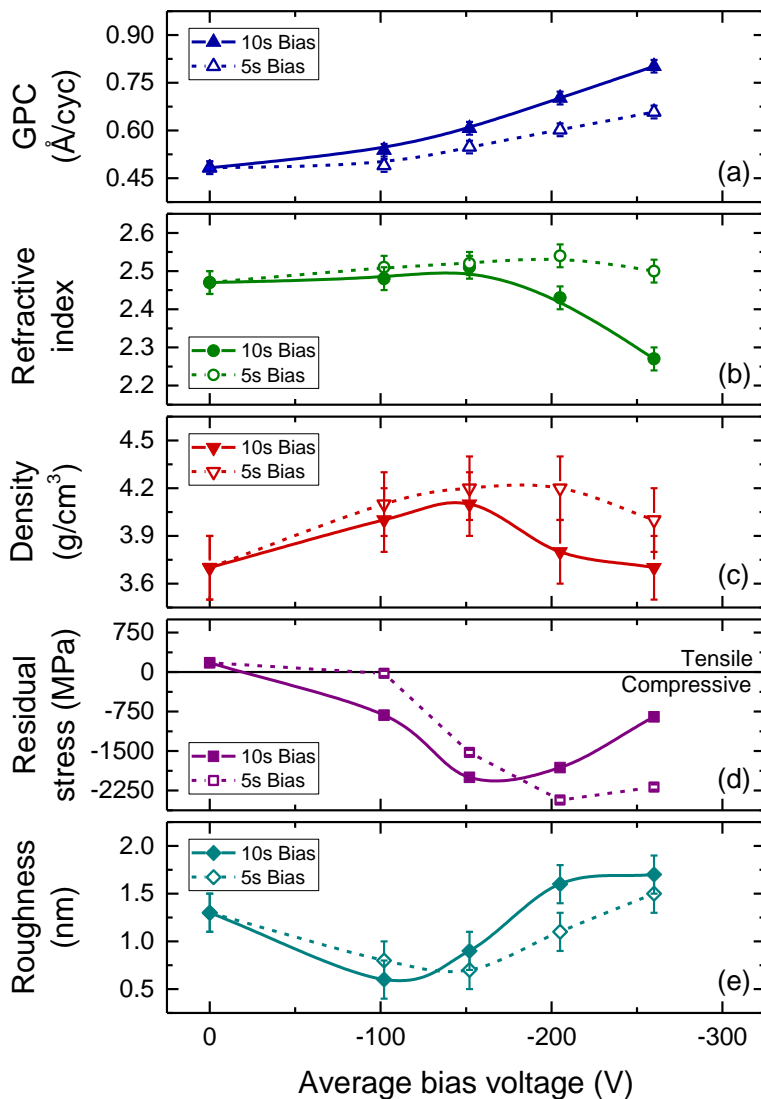
Figure 3. (a) Growth per cycle (GPC), **(b)** refractive index, **(c)** mass density, **(d)** residual stress and **(e)** RMS surface roughness of titanium oxide films deposited at 300 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied for the entire duration and last half (5 s) of the 10 s O_2 plasma exposure step.

Table 2. GPC (film thickness per cycle and number of atoms deposited per nm² per cycle) and elemental composition of titanium oxide films deposited at 300 °C with and without bias voltages applied during the O$_2$ plasma exposure step. For the films deposited with biasing during plasma exposure, data are shown for average bias voltages, $\langle V_{bias} \rangle$, applied during the whole (10 s) and the last half (5 s) of the 10 s O$_2$ plasma step. Typical uncertainties are given in the first row.

$\langle V_{bias} \rangle$ (V)	Bias duration during 10 s O$_2$ plasma step (s)	GPC (Å/cycle)	GPC [Ti] (#Ti at. per nm² per cycle)	RBS			ERD
				GPC [O] (#O at. per nm² per cycle)	O/Ti	[C] at. %	[H] at. %
0	No bias	0.48 ± 0.02	1.35 ± 0.03	2.72 ± 0.05	2.0 ± 0.1	< d.l.ᵃ	3 ± 7
-152	All 10	0.61	1.62	3.47	2.2	< d.l.	3
	Last 5	0.55	1.50	3.07	2.0	< d.l.	3
-205	All 10	0.70	1.71	3.85	2.3	< d.l.	3
	Last 5	0.60	1.61	3.67	2.3	< d.l.	3

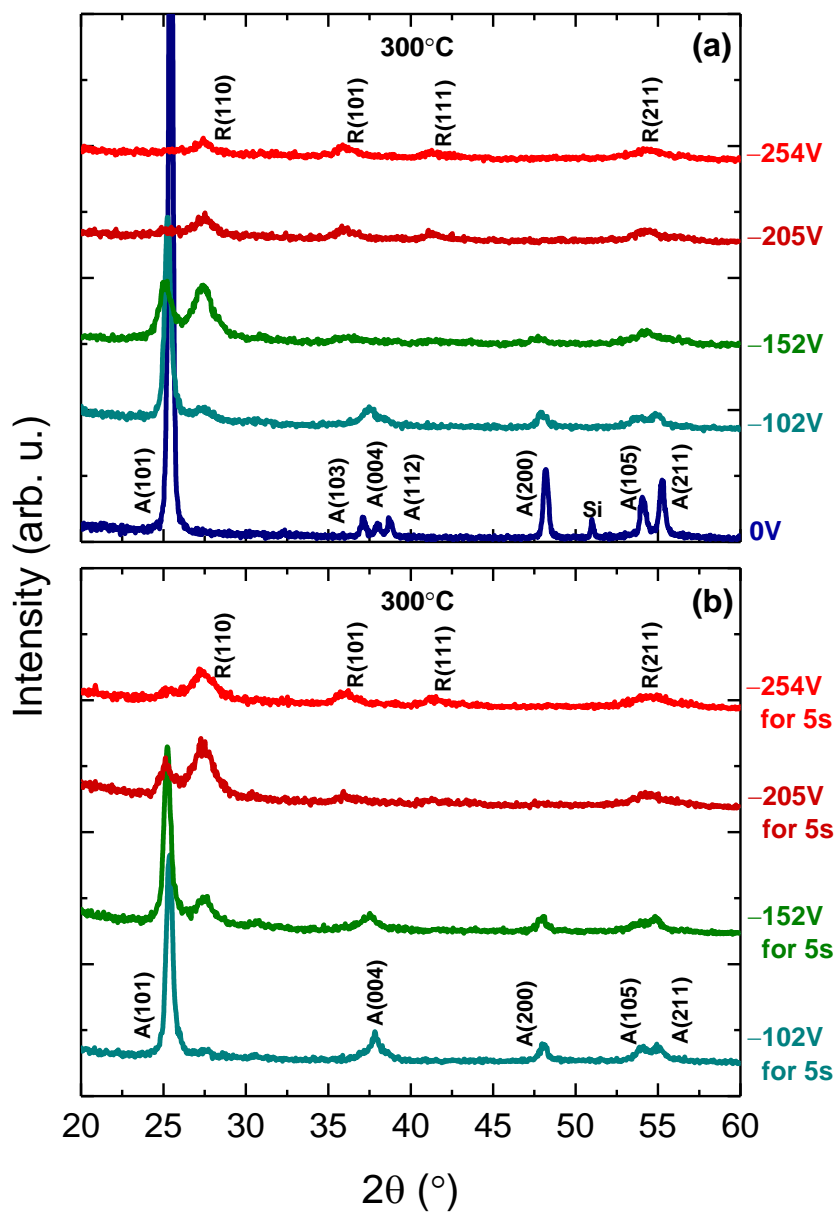ᵃ Values below detection limit (d.l.) of 8 at. % for [C]

Figure 4. Grazing incidence X-ray diffractograms for titanium oxide films deposited at 300 °C with average bias voltages, $\langle V_{bias} \rangle$, ranging from 0 V to -254 V applied for the **(a)** entire duration and **(b)** last half (5 s) of the 10 s O_2 plasma exposure step. Peaks corresponding to the anatase and rutile phase are denoted with "A" and "R", respectively.
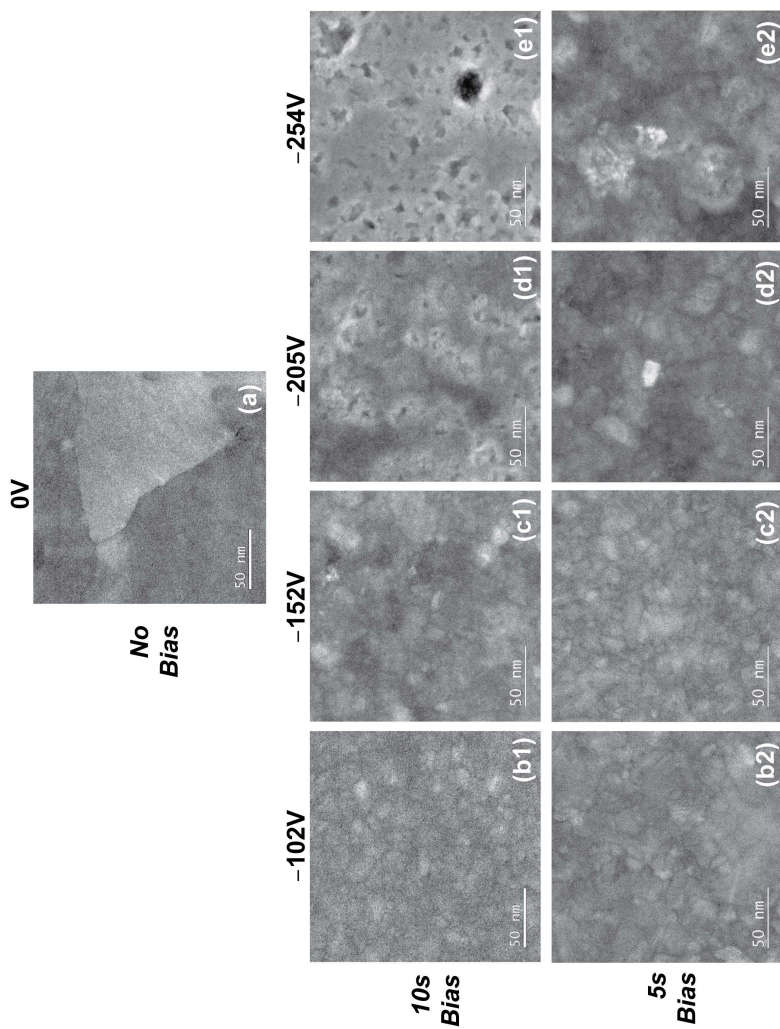
Figure 5. Plan-view high angle annular dark-field (HAADF) STEM images for titanium oxide films deposited at 300 °C with **(a)** 0 V, **(b1)**, **(b2)** -102 V, **(c1)**, **(c2)** -152 V, **(d1)**, **(d2)** -205 V, **(e1)**, **(e2)** -254 V average bias voltages, $\langle V_{bias} \rangle$. Images **(b1)**, **(c1)**, **(d1)** and **(e1)** denote $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s O_2 plasma exposure step while images **(b2)**, **(c2)**, **(d2)** and **(e2)** represent $\langle V_{bias} \rangle$ applied for the last half (5 s) of the 10 s plasma exposure step.

No substrate bias: In the absence of substrate biasing during plasma exposure, (i.e., grounded substrate or $\langle V_{bias} \rangle = 0$ V, bias duty cycle = 0%, Figure 1a) the film had a GPC of 0.48 ± 0.02 Å (Figure 3a) which is similar to the growth rate reported by Wei *et al.*[50] for TiO_x deposited at the same temperature using TDMAT and O_2 plasma. The values obtained for the refractive index and mass density were 2.47 ± 0.03 and 3.7 ± 0.2 g/cm[3] (Figure 3b and c), respectively, which is comparable to the values reported in the literature for the anatase phase of TiO_x.[51] This film was found to have a tensile residual stress (Figure 3d) which was also reported for TiO_x deposited at 300 °C in previous work.[32]. An O/Ti ratio of 2.0 ± 0.1 (Table 2) was observed for this film indicating the formation of stoichiometric TiO_2 for deposition without any $\langle V_{bias} \rangle$. Low impurity contents in terms of [H] and [C] (3 ± 7 at. % and < 8 at. %, respectively) were obtained in all films (Table 2). The XRD pattern for the film deposited without biasing (Figure 4a) shows diffraction peaks that correspond to the anatase phase of TiO_2. The intense and narrow (101) peak indicates the presence of a highly crystalline TiO_2 film with large anatase crystal grains. This is confirmed by the complementary information from the TEM image for the film deposited without biasing (Figure 5a) which shows a compact or void-free microstructure with lateral grain sizes of the order of ∼150 nm.

Effect of bias magnitude: For the 10 s bias duration condition (bias duty cycle = 100%, Figure 1b), the GPC showed a monotonic increase with increasing $\langle V_{bias} \rangle$ and reached a value of 0.80 ± 0.02 Å at -254 V (Figure 3a). This is also reflected in the GPC [Ti] and GPC [O] values which increased to 1.71 ± 0.03 Ti and 3.85 ± 0.05 O at./nm[2], respectively, at -205 V applied for all 10 s of plasma exposure (Table 2). The trends for refractive index, mass density and residual stress can be categorized into two stages composed of an initial buildup to a maximum followed by a gradual decrease with increasing $\langle V_{bias} \rangle$. In the first stage, the refractive index and mass density reached peak values of 2.51 ± 0.03 and 4.1 ± 0.2 g/cm[3], respectively, as $\langle V_{bias} \rangle$ was increased to -152 V (Figure 3b and c). The corresponding behavior of the residual stress for TiO_x in the first stage consisted of a change from tensile to compressive on applying a bias to the substrate, denoted by negative values on the vertical axis of Figure 3d. This stress evolution from tensile to compressive is similar to that frequently reported in the literature for thin-film deposition using energetic particle bombardment.[19,52–55] The compressive stress reached a maximum as $\langle V_{bias} \rangle$ was increased to -152 V, similar to the peaking of refractive index and mass density with biasing at the same voltage. The maximization of compressive stress for deposition using energetic particle bombardment has been reported in the literature to be related to the formation of bombardment induced point defects such as interstitials in the film bulk.[52–55] Under conditions of intense ion bombardment during film growth, the implantation of the energetic ions and/or the formation of subsurface interstitial atoms resulting from ion-surface interactions that push deposited atoms into the film bulk (i.e., recoil implantation or forward sputtering

of knock-on atoms generated by ion-surface collisions) can increase atomic packing of the growing film.[52–55] This raises compressive stress as well as the mass density which scale with the concentration of those point defects.[52–55] The O/Ti ratio for the film deposited using -152 V applied for 10 s of plasma exposure was observed to increase to 2.2 ± 0.1 (Table 2) indicating the formation of an oxygen rich film during energetic oxygen ion bombardment. The excess oxygen can be speculated to be present as interstitial species which could stimulate an increase in compressive stress while also contributing towards elevating mass density and refractive index observed when increasing $\langle V_{bias} \rangle$ up to -152 V. Applying and steadily increasing $\langle V_{bias} \rangle$ to -152 V cause the anatase diffraction peaks in the XRD patterns (Figure 4a) to gradually decrease in magnitude while new peaks corresponding to the rutile phase of TiO_2 appeared. This is similar to the results obtained in previous work conducted in our group where the crystalline phase of TiO_x films, grown using different precursors[19,20] in a home-built plasma ALD tool equipped with substrate biasing, could be transformed by varying $\langle V_{bias} \rangle$ during the O_2 plasma step. TiO_x is known to have a higher refractive index and mass density in the rutile compared to the anatase phase.[51] Therefore, besides the effect of a higher interstitial content on material properties, the observed increase in GPC, refractive index, material density and compressive stress could also be caused by phase transformation, or more specifically, the formation of denser rutile crystallites in the mixed phase (anatase + rutile) TiO_x films obtained using $\langle V_{bias} \rangle$ up to -152 V (Figure 4a). The deposited films were observed to retain a compact and void-free microstructure for $\langle V_{bias} \rangle$ up to -152 V (Figure 5b1 and c1). However, based on estimates of lattice fringe areas in magnified TEM images (see Figure A5.4b1 and A5.4c1 in Appendix 5), lateral grain sizes of ~20 nm were observed in the bias deposited films which were nearly an order of magnitude smaller than the grains formed without biasing.

For $\langle V_{bias} \rangle$ beyond -152 V applied for all 10 s of plasma exposure, the GPC (Figure 3a), GPC [Ti], GPC [O] and O/Ti ratio (Table 2) continued to increase but the refractive index and mass density entered their second stage where they rapidly decreased, reaching values of 2.27 ± 0.03 and 3.7 ± 0.2 g/cm³, respectively, at -254 V (Figure 3b and c). Furthermore, increase in $\langle V_{bias} \rangle$ beyond -152 V also initiated the second stage in residual stress behavior. The compressive stress began to decrease, similar to the trends in refractive index and mass density as $\langle V_{bias} \rangle$ was increased to -254 V (Figure 3d). The anatase diffraction peaks in the XRD patterns completely disappeared and only rutile diffraction peaks remained (Figure 4a). The intensities and widths of these peaks became lower and broader, respectively, on increasing $\langle V_{bias} \rangle$ beyond -152 V indicating an increase in the degree of disorder or amorphization of the film microstructure. This onset of amorphization induced by highly energetic ion bombardment has also been reported in the literature[14,55,56] and it could play a role in lowering the refractive index

and mass density of the films. Furthermore, the relaxation of compressive stress on increasing $\langle V_{bias} \rangle$ beyond -152 V suggests that the yield strength of the material could have been exceeded under such intense ion bombardment which could then lead to plastic deformation.[14,54,57,58] These aforementioned trends in material properties were in line with the appearance of voids in the film microstructure for TiO$_x$ deposited with $\langle V_{bias} \rangle$ greater than -152 V (Figure 5d1 and e1). The void fraction increased with increasing $\langle V_{bias} \rangle$ which could also play a role in compressive stress relaxation together with decreasing refractive index and mass density. The surface of TiO$_x$ films initially became smoother with biasing as the RMS roughness decreased at -102 V (Figure 3e). This could be due to a combined effect of phase transformation, material densification and/or coalescence at grain boundaries due to enhanced mobility of surface species induced by energetic ions[55] during film growth. The roughness increased with further increase in $\langle V_{bias} \rangle$ to -254 V, which could be attributed to the onset of void incorporation and/or ion bombardment induced surface damage.[55] The trends in RMS surface roughness obtained from XRR were corroborated with additional measurements performed using atomic force microscopy (see Figure A5.5 and A5.6 in Appendix 5). Altogether, the results above demonstrate how the growth and material properties of TiO$_x$ films deposited using TDMAT and O$_2$ plasma can be tuned by altering the magnitude of $\langle V_{bias} \rangle$ applied with a 100% duty cycle during the plasma exposure step of PEALD.

Effect of bias duration/duty cycle: When $\langle V_{bias} \rangle$ having the same magnitude but different duty cycle were applied during the O$_2$ plasma exposure step (i.e., the last 5 s of the 10 s plasma exposure, bias duty cycle = 50%, Figure 1c), differences were observed in the variation of TiO$_x$ film properties. The GPC again showed a trend of increasing with $\langle V_{bias} \rangle$, but at a slower rate than the 10 s bias condition reaching a comparatively lower value at -254 V (Figure 3a). This was also the case for GPC [Ti] and GPC [O] values (Table 2) which increased to comparatively lower values at -205 V applied for the shorter 5 s of plasma exposure. The refractive index and mass density of the films also increased with biasing for the shorter 5 s condition, but were consistently higher than the corresponding values for films deposited using the same $\langle V_{bias} \rangle$ applied for a longer duration of 10 s (Figure 3b and c). The refractive index and mass density for the 5 s bias condition reached higher maximum values at a higher $\langle V_{bias} \rangle$ of -205 V compared to the corresponding peaks at -152 V obtained using the 10 s bias condition (Figure 3b and c). The residual stress of the TiO$_x$ films again changed from tensile to compressive for the 5 s bias condition and also reached a higher maximum at a higher $\langle V_{bias} \rangle$ of -205 V compared to the maximum obtained at -152 V using the 10 s bias condition (Figure 3d). The O/Ti ratio for the film deposited using -205 V applied for the shorter duration of 5 s was 2.3 ± 0.1 (Table 2) which again indicates the formation of an oxygen rich film during energetic oxygen ion bombardment. Since compressive stress

tends to scale with the concentration of point defects such as interstitials,[52–55] the higher fraction of excess oxygen in the film grown with -205 V applied for the shorter duration of 5 s could explain why it had a higher compressive stress, mass density and refractive index compared to the film grown with -152 V applied for 10 s. It is worth noting that the use of -102 V for the shorter duration of 5 s yielded TiO_x that was approximately stress-free in nature as evidenced by the insignificant value of -25 ± 50 MPa measured for that film.

Furthermore, TiO_x films deposited using the 5 s bias condition retained a compact and void-free microstructure up to a higher $\langle V_{bias} \rangle$ of -205 V (Figure 5b2, c2 and d2) compared to the -152 V ceiling for obtaining similar void-free films using the 10 s bias condition (Figure 5b1 and c1). Increasing $\langle V_{bias} \rangle$ beyond -205 V using the 5 s bias condition led to a decrease in both refractive index and mass density together with compressive stress relaxation (Figure 3b, c and d), similar to the trends observed for the 10 s bias condition beyond -152 V. This can again be attributed to the incorporation of voids in the film microstructure (Figure 5e2) and/or the onset of plastic deformation[14,54,57,58] for TiO_x deposited at -254 V using the 5 s bias condition. The TiO_x film surface initially became smoother with biasing using the 5 s condition, similar to the 10 s condition. However, the lowest RMS roughness was now at -152 V applied for the last 5 s (Figure 3e) compared to -102 V applied for all 10 s of plasma exposure. Further increase in $\langle V_{bias} \rangle$ beyond -152 V using the 5 s bias condition increased surface roughness. Similar to the delayed changes observed in the aforementioned properties, the anatase to rutile phase transformation using the 5 s bias condition also occurred at a slower rate compared to the 10 s bias condition (Figure 4b). It is worth noting that for the 10 s bias condition, using -152 V leads to a combined anatase and rutile mixed phase with the most intense R(110) peak (Figure 4a) whereas for the 5 s condition, a similar mixed phase with the most intense R(110) peak is observed at -205 V (Figure 4b). It seems that for PEALD of TiO_x with substrate biasing, optimum material quality in terms of a high refractive index, high density and compact microstructure is obtained for films with a mixed phase content having the highest R(110) peak intensity and no voids. Varying the duration of the applied bias translates to changing the dose or fluence (i.e., particle flux integrated over time) of energetic ions impinging on the substrate. The dose or fluence of energetic ions has also been reported in the literature as a parameter that can have significant effects on material properties.[13,14,44] Altogether, these results effectively demonstrate how the growth and material properties of TiO_x films deposited using TDMAT and O_2 plasma can be tuned, not only by varying the magnitude of $\langle V_{bias} \rangle$, but also by changing the duration or duty cycle of $\langle V_{bias} \rangle$ applied during the plasma exposure step.

Effect of substrate bias at lower deposition temperature: Figure 6 shows selected area electron diffraction patterns and plan-view HAADF STEM images for TiO_x films deposited at a lower temperature of 150 °C with and without substrate biasing applied during 10 s of O_2 plasma exposure. For the film deposited without any $\langle V_{bias} \rangle$, the diffuse rings in the electron diffraction pattern (Figure 6a1) and the absence of crystal lattice fringes in the plan-view HAADF STEM image (Figure 6a2) indicate the mainly amorphous nature of the film. However, the appearance of sharp rings (Figure 6b1) and crystal lattice fringes (Figure 6b2) indicate the presence of polycrystalline material in the film deposited with $\langle V_{bias} \rangle$ of -205 V. This is confirmed by the appearance of diffraction peaks corresponding to the rutile phase of TiO_x in the grazing incidence XRD pattern for the film deposited with -205 V at 150 °C (see Figure A5.7 in Appendix 5). Profijt et al.[20] reported a similar result for TiO_x deposited at 200 °C using $Ti(Cp^{Me})(NMe_2)_3$ as the precursor. Their film deposited without biasing was amorphous while applying -100 V bias during the whole duration of the O_2 plasma exposure yielded crystallinity, evidenced by the R(110) diffraction peak in the XRD pattern. The results obtained in this work using a different precursor (TDMAT) effectively reproduce the phenomenon of inducing crystalline material formation with substrate biasing at a comparatively lower temperature that would typically yield amorphous films.
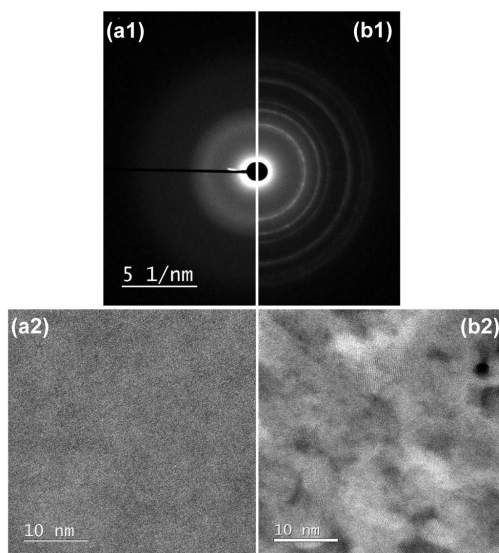

Figure 6. (a1), **(b1)** Selected area electron diffraction patterns and **(a2)**, **(b2)** plan-view high angle annular dark-field (HAADF) STEM images for titanium oxide films deposited at 150 °C. Panels **(a1)** and **(a2)** are for the film deposited without substrate biasing ($\langle V_{bias} \rangle$ = 0 V) while panels **(b1)** and **(b2)** are for the film deposited with substrate biasing ($\langle V_{bias} \rangle$ = -205 V) applied during 10 s of the O_2 plasma exposure step.

Hafnium oxide: The growth and material properties of HfO_x films deposited on planar substrates at 150 °C were investigated for $\langle V_{bias} \rangle$ between 0 V and -280 V applied during the O_2 plasma exposure step. Figure 7 shows these properties in terms of the GPC, refractive index, mass density, residual stress and surface roughness expressed as a function of $\langle V_{bias} \rangle$ applied during plasma exposure. The crystalline properties of the HfO_x films can be analyzed in Figure 8 which shows grazing incidence XRD patterns for films deposited with $\langle V_{bias} \rangle$ ranging from 0 V to -280 V. Additional information regarding the crystallinity and film microstructure can be obtained in Figure 9 which shows selected area electron diffraction patterns and plan-view HAADF STEM images for HfO_x deposited on planar TEM windows with and without substrate biasing.

For deposition without any bias voltage, the film had a GPC of 1.03 ± 0.02 Å and a refractive index of 2.04 ± 0.03 (Figure 7a and b) which are comparable to the values reported by Sharma *et al.*[47] for HfO_x deposited using TDMACpH and O_2 plasma at the same temperature. The film was observed to have a mass density of 9.0 ± 0.2 g/cm^3 (Figure 7c). The lack of diffraction peaks in the XRD pattern (Figure 8) indicate the formation of amorphous HfO_x deposited without biasing. This is confirmed by diffuse rings in the electron diffraction pattern (Figure 9a1) and absence of lattice fringes in the HAADF STEM image (Figure 9a2). A void rich amorphous matrix is also revealed in the HAADF STEM image which could explain the low mass density and refractive index of this film when compared to bulk HfO_x.[59,60] The film had a tensile residual stress of 770 ± 50 MPa (Figure 7d) which is comparable to that reported for HfO_x in previous work.[23]

When substrate biasing was implemented during plasma exposure, the GPC showed a slow increase with $\langle V_{bias} \rangle$ up to -204 V (Figure 7a). Further increase in $\langle V_{bias} \rangle$ to -280 V led to a rapid increase in GPC. The refractive index and mass density showed a two stage behavior where they initially increased with $\langle V_{bias} \rangle$ reaching a maximum of 2.09 ± 0.03 and 9.7 ± 0.2 g/cm^3, respectively, at -152 V (Figure 7b and c) which are closer to the values for bulk HfO_x.[59,60] Applying and steadily increasing $\langle V_{bias} \rangle$ led to the appearance of diffraction peaks in the XRD patterns (Figure 8) corresponding to lattice planes of monoclinic HfO_x. The phenomenon of crystalline material formation with substrate biasing at low temperature discussed previously for TiO_x was also effectively demonstrated in case of HfO_x. Increasing $\langle V_{bias} \rangle$ to -152 V led to higher diffraction peak intensities and narrower peak widths indicating the presence of a higher crystalline fraction and/or formation of larger crystal grains.[61] Therefore, the observed increase in GPC, refractive index and mass density with $\langle V_{bias} \rangle$ can be initially attributed to the formation of crystalline material at -113 V followed by an increase in crystalline content and/or grain size at -152 V. The increase in refractive index and mass density with biasing could in principle, also be due to a reduction in void content observed for the film grown without biasing. A similar increase in film crystallinity, refractive index and mass density
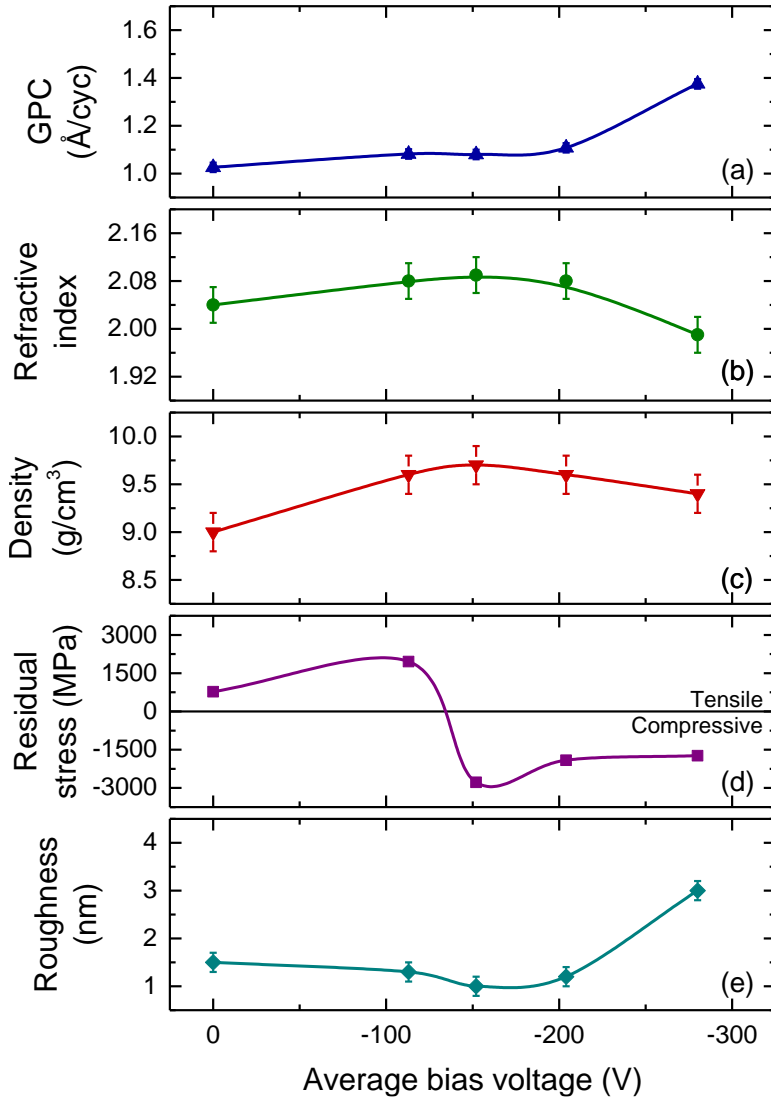
Figure 7. (a) Growth per cycle (GPC), **(b)** refractive index, **(c)** mass density, **(d)** residual stress and **(e)** RMS surface roughness of hafnium oxide films deposited at 150 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied during the O_2 plasma exposure step.
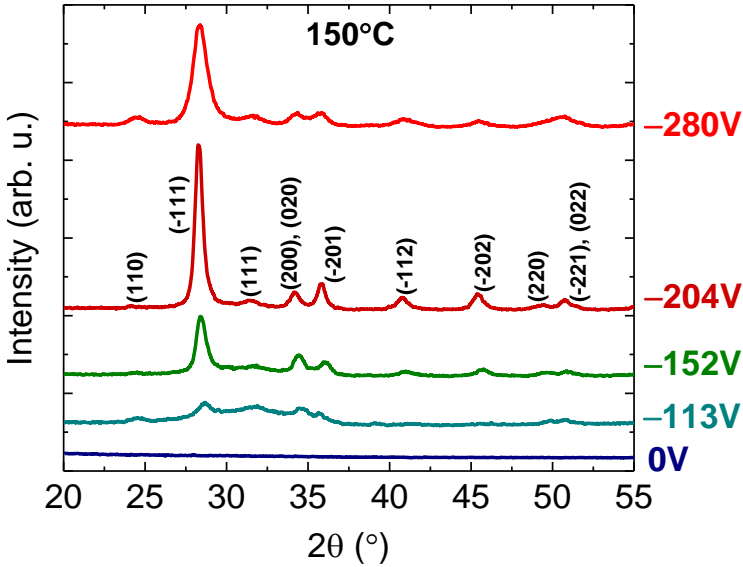
Figure 8. Grazing incidence X-ray diffractograms for hafnium oxide films deposited at 150 °C with average bias voltages, $\langle V_{bias} \rangle$, ranging from 0 V to -280 V applied during the O_2 plasma exposure step. Peaks corresponding to lattice planes in monoclinic hafnium oxide are indicated.

of HfOₓ films was reported by Sharma *et al.*[47] due to an increase in substrate temperature. Therefore, the results obtained in this work demonstrate that enhancing the ion energy during PEALD of HfOₓ provides an alternate route for tuning such properties. Unlike the previous case of TiOₓ or any other material investigated in this work, the residual stress of HfOₓ showed a three stage behavior. In the first stage, the tensile residual stress of the HfOₓ films increased with $\langle V_{bias} \rangle$ to 1960 ± 50 MPa at -113 V (Figure 7d). This is in contrast to the trend exhibited by TiOₓ which showed a change in stress from tensile to compressive when applying a similar $\langle V_{bias} \rangle$. The difference in stress behavior could be due to the difference in initial microstructure of the two films grown without biasing. TiOₓ deposited at a higher temperature (300 °C) yielded a highly crystalline and void free film whereas HfOₓ deposited at a lower temperature (150 °C) consisted of a void rich amorphous matrix. Therefore, when applying a similar $\langle V_{bias} \rangle$ around -100 V, TiOₓ changed from one void free crystalline state to another whereas HfOₓ transitioned from a disordered and porous amorphous matrix to a more ordered crystalline structure, with perhaps a lower void content. Further increase in $\langle V_{bias} \rangle$ led to the second stage in stress behavior where HfOₓ went from a tensile maximum at -113 V to a compressive maximum at -152 V (Figure 7d). This may again be related to another change in film microstructure. In this case, HfOₓ transitioned from a less crystalline film with small grains at -113 V to a comparatively more crystalline film with larger grains and possibly, an even lower void content at -152 V. The surface roughness of the films

also showed a two stage behavior with substrate biasing**.** The films initially became smoother on increasing $\langle V_{bias} \rangle$ as the RMS roughness decreased to a minimum at -152 V (Figure 7e). This could again stem from coalescence at the grain boundaries[47,55] due to enhanced mobility of surface species induced by energetic ions during film growth, similar to the case of TiO$_x$.

For $\langle V_{bias} \rangle$ beyond -152 V, the refractive index and mass density entered their second stage where they now decreased with substrate biasing (Figure 7b and c). On the contrary, increasing $\langle V_{bias} \rangle$ to -204 V led to a more intense and narrower (-111) diffraction peak in the XRD pattern (Figure 8). This, combined with the decrease in refractive index and mass density of HfO$_x$ at -204 V suggests the formation of a more crystalline film with larger grains and a porous microstructure. This is confirmed by the electron diffraction pattern and HAADF STEM image in Figure 9. Sharp rings corresponding to monoclinic HfO$_x$ (Figure 9b1) and crystal lattice fringes (Figure 9b2) reaffirm polycrystalline material formation using $\langle V_{bias} \rangle$ of -204 V while the dark regions (Figure 9b2) provide evidence of a void rich microstructure. Applying $\langle V_{bias} \rangle$ above -204 V led to a gradual decrease in peak intensities and broadening of peak widths in the XRD patterns (Figure 8). This indicates a decrease in crystallinity or material amorphization[14,55,56] under intense ion bombardment. The trend in residual stress
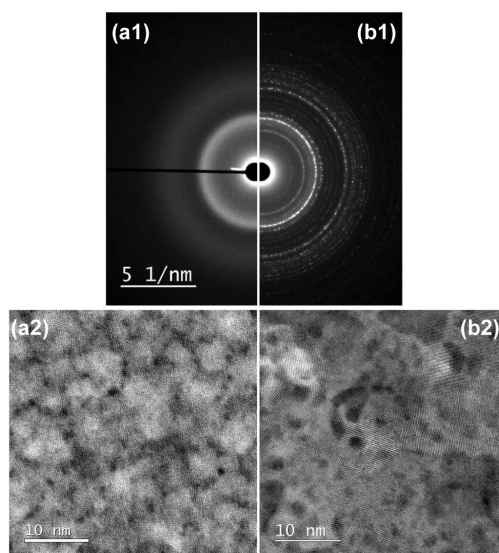

Figure 9. (a1), **(b1)** Selected area electron diffraction patterns and **(a2)**, **(b2)** plan-view high angle annular dark-field (HAADF) STEM images for hafnium oxide films deposited at 150 °C. Panels **(a1)** and **(a2)** are for the film deposited without substrate biasing ($\langle V_{bias} \rangle$ = 0 V) while panels **(b1)** and **(b2)** are for the film deposited with substrate biasing ($\langle V_{bias} \rangle$ = -204 V) applied during the O$_2$ plasma exposure step.

entered its third stage for $\langle V_{bias} \rangle$ exceeding -152 V due to the onset of compressive stress relaxation (Figure 7d). A rise in RMS roughness was observed on increasing $\langle V_{bias} \rangle$ to -280 V (Figure 7e) implying that the trend for surface roughness had transitioned to its second stage. These trends for HfO_x deposited using $\langle V_{bias} \rangle$ beyond -152 V are similar to those observed earlier for TiO_x films grown using high $\langle V_{bias} \rangle$. As a result, the degradation of TiO_x properties due to increase in film void content, plastic deformation[14,54,57,58] and ion bombardment induced surface damage[55] at high $\langle V_{bias} \rangle$ could also hold true for HfO_x deposited using similar conditions. Further analysis regarding the effects of biasing on HfO_x microstructure, composition and deposition at a higher temperature will be reported in a subsequent publication.

Silicon oxide (SiO_x): Figure 10 shows the GPC, refractive index, mass density, residual stress and surface roughness of SiO_x films deposited at 200 °C as a function of $\langle V_{bias} \rangle$ applied during the O_2 plasma exposure step. For the deposition performed without biasing during plasma exposure the film had a GPC of 1.02 ± 0.02 Å, refractive index of 1.45 ± 0.03, mass density of 2.3 ± 0.2 g/cm^3 and RMS surface roughness of 1.0 ± 0.2 nm, similar to those reported in previous work by Dingemans *et al.*[48] In contrast with the tensile residual stress observed for TiO_x and HfO_x deposited without biasing, a compressive residual stress of -96 ± 50 MPa was observed for SiO_x deposited without biasing, similar to that reported previously for SiO_x deposited at the same temperature.[23] When implementing substrate biasing during the O_2 plasma exposure step, the GPC showed a monotonic decrease with increasing $\langle V_{bias} \rangle$ and reached a value of 0.62 ± 0.02 Å at -295 V (Figure 10a). This is in contrast to the trends in GPC observed earlier for TiO_x and HfO_x but similar to the monotonic decrease in GPC observed for cobalt oxide reported by Profijt *et al.*[19] It serves to demonstrate how the trends in growth properties as a function of $\langle V_{bias} \rangle$ can be material specific. The refractive index of SiO_x was observed to increase slightly to 1.47 ± 0.03 by applying $\langle V_{bias} \rangle$ of -111 V, but did not increase beyond this value with further increase in biasing. The mass density was observed to remain fairly unchanged with biasing with a slight increase to 2.4 ± 0.2 g/cm^3 using $\langle V_{bias} \rangle$ of -295V. The residual stress of the SiO_x films remained compressive when deposited with substrate biasing and reached a maximum value of -280 ± 50 MPa at -111 V. Further increase in $\langle V_{bias} \rangle$ did not lead to any significant change in the compressive stress. The RMS surface roughness also remained fairly constant when using $\langle V_{bias} \rangle$ to deposit SiO_x films. Unlike the significant variations in growth and material properties observed for TiO_x and HfO_x previously, the results for SiO_x showed significant variation in the growth rate but a very small change in material properties as a function of $\langle V_{bias} \rangle$ during plasma exposure. Further analysis of film OH content, optical transmission losses, wet-etch resistance, etc. will be reported in a subsequent a publication that will provide more insight on the effects of substrate biasing during PEALD of SiO_x.
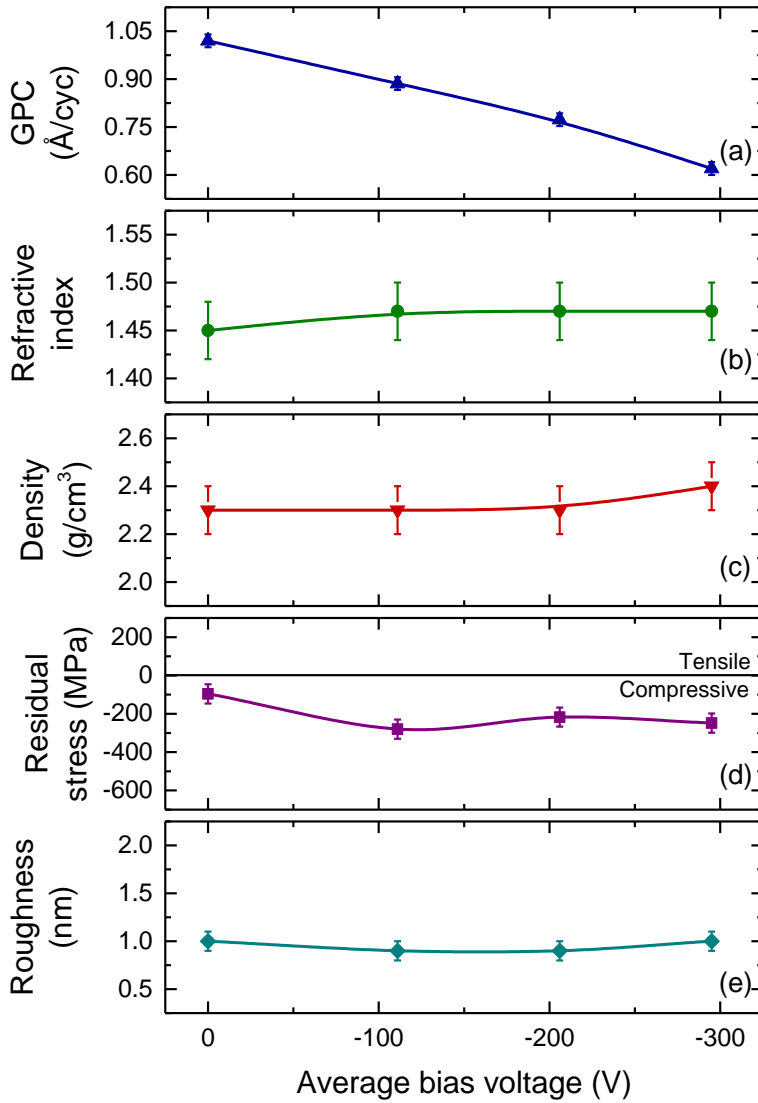
Figure 10. (a) Growth per cycle (GPC), **(b)** refractive index, **(c)** mass density, **(d)** residual stress and **(e)** RMS surface roughness of silicon oxide films deposited at 200 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied during the O_2 plasma exposure step.

5.5.2 PEALD of nitrides on planar substrates

Titanium nitride (TiN$_x$): The growth and material properties of TiN$_x$ films deposited on planar substrates at 200 $^\circ$C was investigated for $\langle V_{bias} \rangle$ between 0 V and -255 V applied during the Ar+H$_2$ plasma exposure step. Figure 11 shows these properties in terms of the GPC, resistivity, mass density, residual stress and surface roughness expressed as a function of $\langle V_{bias} \rangle$ applied during plasma exposure. outlines additional growth and material properties from RBS analysis for the films deposited with and without substrate biasing. The growth properties are outlined in terms of the number of titanium, nitrogen and oxygen atoms deposited per nm^2 per cycle (GPC [Ti], GPC [N] and GPC [O], respectively) while the material properties are outlined in terms of the N/Ti ratio and impurity content ([C], [Ar] and [H]). Note that both Ti and N species in the deposited TiN$_x$ films originated from the precursor itself while the reductive Ar+H$_2$ plasma resets the surface by the formation of amino ligands to enable precursor adsorption in the subsequent cycle.[40] The crystalline properties of the TiN$_x$ films are depicted in Figure 12 which shows grazing incidence XRD patterns for films deposited with $\langle V_{bias} \rangle$ ranging from 0 V to -255 V. The microstructure of the TiN$_x$ films can be observed in Figure 13 which shows plan-view HAADF STEM images for films deposited on planar TEM windows with and without substrate biasing.

For film deposition without any biasing, a GPC of 0.47 ± 0.02 Å was obtained (Figure 11a) which is comparable to that reported for TiN$_x$ deposited using TDMAT and Ar+H$_2$ plasma at this temperature.[46] The film had a resistivity of 1960 ± 60 μΩcm and a mass density of 3.9 ± 0.2 g/cm^3 (Figure 11b and c, respectively). Compared to the resistivity and density of bulk TiN$_x$, the higher resistivity and lower density of the TiN$_x$ film grown without biasing hint toward the presence of impurities[40,46] and/or void incorporation at grain boundaries.[62,63] This is partly confirmed by the high [O] and [H] impurity contents of 28 ± 5 at. % and 10 ± 7 at. %, respectively, for this film leading to a non-stoichiometric N/Ti ratio of 0.63 ± 0.06 and a GPC [O] value of 0.92 ± 0.05 O at./nm^2 (Table 3). The GPC [O] is significant when compared to the GPC [Ti] and GPC [N] values (Table 3). No inert argon gas or detectable carbon impurities were incorporated in this film (Table 3). For deposition involving highly reactive materials such as Ti, Hf, Nb, etc., the partial pressure of the vacuum species (e.g., background water, oxygen) can influence the amount of impurity incorporation (e.g., up to tens of an atomic percent of oxygen) in the deposited film.[30,54,64,65] Assuming a partial pressure of $\sim$10^{-8} Torr for background impurities (for the base pressure of $\sim$10^{-6} Torr in the FlexAL system) corresponds to an impingement rate of about $\sim$ 0.5 impurity atoms per nm^2/s on the growing film surface.[54,66] A plasma exposure time of 10 s can therefore, lead to the incorporation of $\sim$ 0.5 impurity at./nm^2 in the film (assuming a sticking coefficient of 1) which is of the same order as the GPC [O] value obtained for the TiN$_x$ film grown without biasing. Another reason for
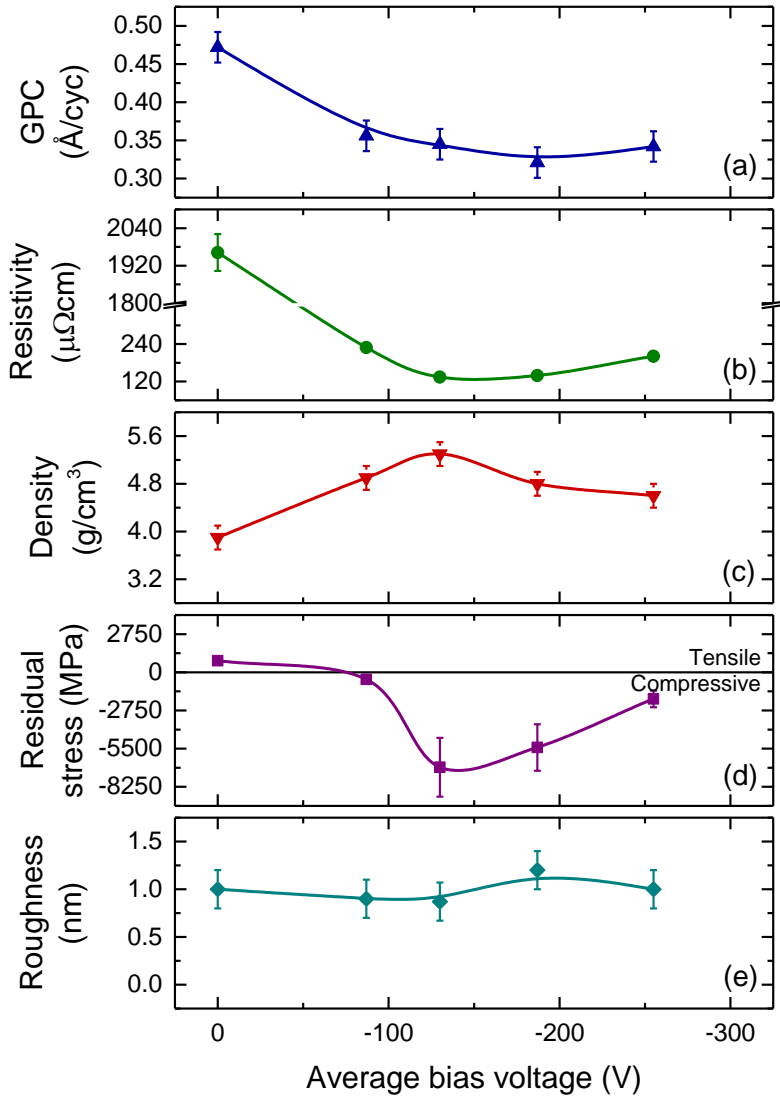
Figure 11. (a) Growth per cycle (GPC), **(b)** resistivity, **(c)** mass density, **(d)** residual stress and **(e)** RMS surface roughness of titanium nitride films deposited at 200 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied during the Ar+H₂ plasma exposure step.
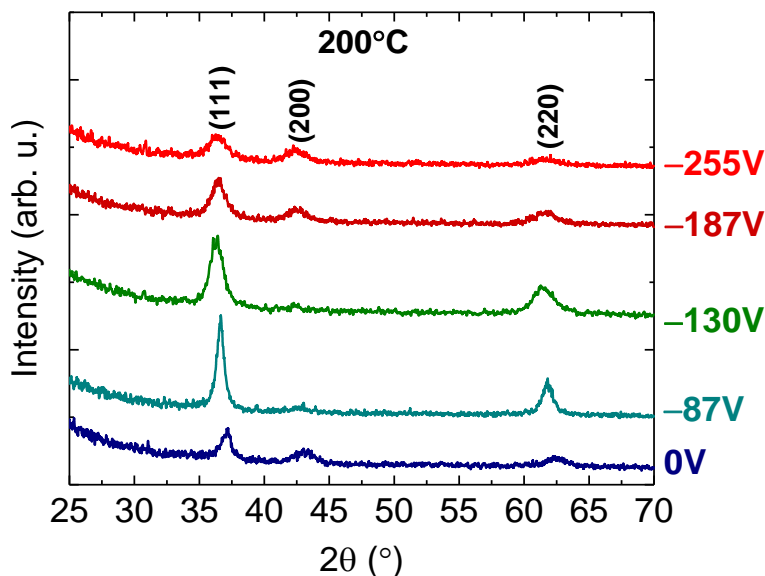
Figure 12. Grazing incidence X-ray diffractograms for titanium nitride films deposited at 200 °C with average bias voltages, $\langle V_{bias} \rangle$, ranging from 0 V to -255 V applied during the Ar+H$_2$ plasma exposure step. Peaks corresponding to lattice planes in cubic titanium nitride are indicated.

the significant [O] content could be due to oxidation of the film upon exposure to the environment. The film was observed to have a tensile residual stress (Figure 11a) similar to that reported for TiN$_x$ in previous work.[67] The XRD pattern for this film (Figure 12) shows diffraction peaks that correspond to cubic TiN$_x$. The fairly small peak intensities and broad peak widths indicate the presence of small crystal grains. This was confirmed by complementary information in the magnified plan-view HAADF STEM image of the film (see Figure A5.8a in Appendix 5). It showed small lateral grain sizes of the order of ~5 nm based on estimates of lattice fringe areas. A loosely packed microstructure consisting of crystalline grains with porous regions in between was also revealed. The small grain size together with intergranular voids observed in the TEM image could also contribute toward the high resistivity and low density of the TiN$_x$ film deposited without biasing.

When substrate biasing was applied during the last half (5 s) of the 10 s Ar+H$_2$ plasma exposure step, the trends in GPC, resistivity, mass density and residual stress again consisted of two stages as observed earlier for the transition metal oxides. In the first stage, the GPC decreased with substrate biasing and reached a minimum value of 0.32 ± 0.02 Å at $\langle V_{bias} \rangle$ of -187 V (Figure 11a). This decrease in GPC for TiN$_x$ is unlike the trends in GPC observed for the transition metal oxide films discussed previously, but similar to that observed for SiO$_x$. This again illustrates how the trends in growth

Table 3. GPC (film thickness per cycle and number of atoms deposited per nm² per cycle) and elemental composition of titanium nitride films deposited at 200 °C with and without average bias voltages, $\langle V_{bias} \rangle$, applied during the Ar+H_2 plasma exposure step. Typical uncertainties are given in the first and second rows unless otherwise stated.

$\langle V_{bias} \rangle$ (V)	GPC (Å/cycle)	RBS							ERD	
		GPC [Ti] (#Ti at. per nm² per cycle)	GPC [N] (#N at. per nm² per cycle)	GPC [O] (#O at. per nm² per cycle)	N/Ti	[O] at. %	[C] at. %	[Ar] at. %	[H] at. %
0	0.47 ± 0.02	1.22 ± 0.03	0.76 ± 0.10	0.92 ± 0.05	0.63 ± 0.06	28 ± 5	< d.l.[a]	0 ± 0.06	10 ± 7
-130	0.35	1.46 ± 0.01	1.18 ± 0.04	0.10 ± 0.02	0.80 ± 0.03	3 ± 2	< d.l.	0.20 ± 0.05	3 ± 3
-255	0.34	1.18	1.17	0.06	1.0	2	12 ± 3	0.77	2

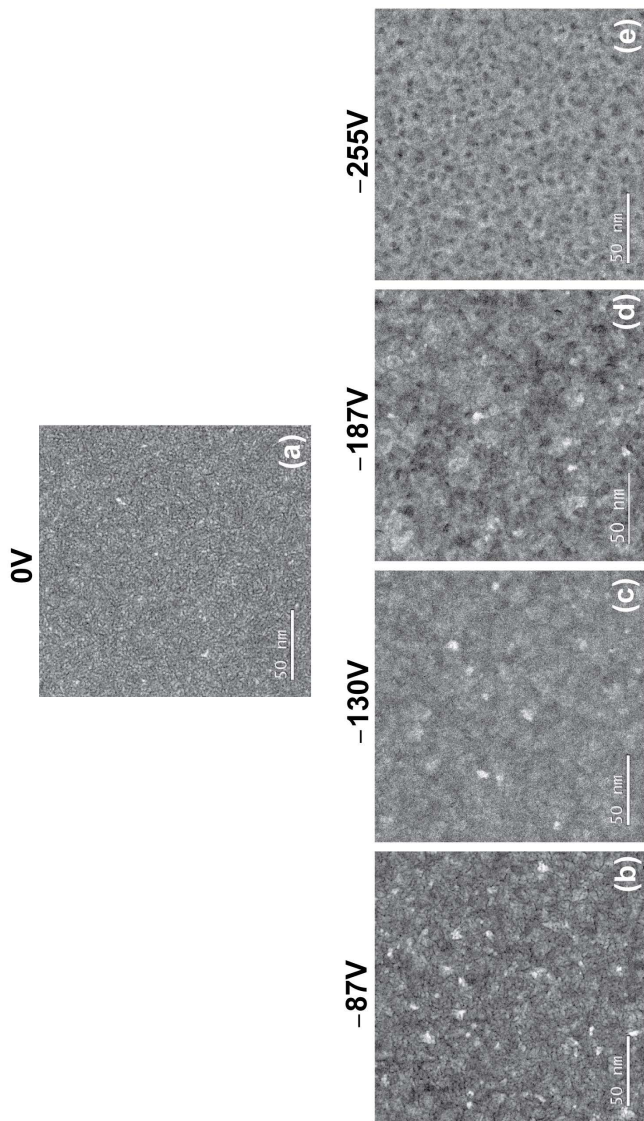[a] Values below detection limit (d.l.) of 8 at. % for [C]

Figure 13. Plan-view high angle annular dark-field (HAADF) STEM images for titanium nitride films deposited at 200 °C with **(a)** 0 V, **(b)** -87 V, **(c)** -130 V, **(d)** -187 V and **(e)** -255 V average bias voltages, $\langle V_{bias} \rangle$, applied during the Ar+H$_2$ plasma exposure step.

properties as a function of $\langle V_{bias} \rangle$ can be material specific. The reduction in film GPC coincided with a nine fold decrease in GPC [O] with biasing at -130 V (Table 3). The large decrease in GPC [O] outweighed the comparatively smaller increase in GPC [Ti] and GPC [N] at -130 V (Table 3). As a result, a large reduction in the film [O] content to 3 ± 2 at. % and a simultaneous increase of the N/Ti ratio to 0.8 ± 0.03 (Table 3) was observed when $\langle V_{bias} \rangle$ was increased to -130 V. The [H] content also decreased significantly to 3 ± 3 at. % while any carbon impurities that may have been incorporated using -130 V still remained below the detection limit (Table 3). The significant decrease in [O] and [H] impurity contents and improvement in TiN_x stoichiometry was reflected in an order of magnitude lower resistivity and a higher mass density of 134 ± 5 μΩcm and 5.3 ± 0.2 g/cm^3 (Figure 11b and c), respectively, at -130 V. Energetic ion bombardment during deposition of TiN_x[68] and other nitrides[11,69] has been reported to improve material purity by removing adsorbed oxygen/OH species from the growing film surface originating from background impurities in the vacuum environment. Therefore, the large reduction in [O] and [H] impurity content by energetic ion bombardment during Ar+H$_2$ plasma exposure with biasing can contribute towards lowering GPC while improving film density and electronic conductivity.

The residual stress behavior of the TiN_x films in the first stage changed from tensile to compressive on applying $\langle V_{bias} \rangle$ to the substrate (Figure 11d). The compressive stress reached a maximum as $\langle V_{bias} \rangle$ was increased to -130 V, analogous to the minimum in resistivity and maximum in mass density obtained at the same $\langle V_{bias} \rangle$. The stress evolution from tensile to compressive for deposition of TiN_x using energetic particle bombardment could be due to the interplay of several factors discussed in the literature.[62,63,70] A part of the reason could be due to the change in film composition when increasing $\langle V_{bias} \rangle$ up to -130 V leading to the formation of cleaner TiN_x films that have a higher bulk density compared to pure TiO_2 or contaminated $TiN_xO_yH_z$. Another factor that could play a role is inert argon gas incorporation, even below 1 at. %, at interstitial positions which has been reported in the literature to induce significant compressive stress.[62,70] This is in agreement with the small but measurable quantity of 0.20 ± 0.05 at. % for [Ar] in the highly compressive TiN_x film deposited using -130 V (Table 3). Analysis of film crystalline properties revealed that applying $\langle V_{bias} \rangle$ initially led to more intense and narrower (111) and (220) peaks while suppressing the (200) peak, as observed in the XRD pattern for -87 V (Figure 12). This suggests the presence of a more crystalline material with larger grains which was corroborated by the magnified HAADF STEM image of the film deposited using -87 V (see Figure A5.8b in Appendix 5) . It showed increased lateral grain dimensions of the order of ~10 nm and a more closely packed film microstructure with a reduced void fraction. However, further increase in $\langle V_{bias} \rangle$ to -130 V led to a gradual decrease in intensity and broadening of the (111) and (220) peaks in the XRD pattern while the (200) peak slowly

reappeared (Figure 12). Although this seems to suggest a decrease in the crystalline order and/or grain size, the TEM image of the film deposited at -130 V (Figure 13c) revealed a very compact TiN_x film with a void-free microstructure that retained grain dimensions of ~10 nm (see also Figure A5.8c in Appendix 5). The presence of a void-free microstructure with large crystal grains for TiN_x deposited using -130 V could also be another factor behind the high electronic conductivity, mass density and compressive stress discussed earlier for this film. The discrepancy between XRD and the rest of the results could be due to the highly compressive stress measured in this film which can also play a role in diffraction peak broadening[61–63] of XRD patterns besides a decrease in crystal grain size and/or volume fraction.

For $\langle V_{bias} \rangle$ greater than -130 V, the GPC continued to decrease till a voltage of -187 V beyond which it entered its second stage and started to rise (Figure 11a). The GPCs for films deposited using $\langle V_{bias} \rangle$ of -130 V and -255 V were comparable to each other (Table 3). The values for GPC [Ti], GPC [N] and GPC [O] decreased when $\langle V_{bias} \rangle$ was increased from -130 V to -255 V (Table 3). Although the N/Ti ratio became unity when $\langle V_{bias} \rangle$ was increased to -255 V which seemingly suggested growth of stoichiometric TiN_x, the [C] and [Ar] contents became significantly large reaching values of 12 ± 3 at. % and 0.77 ± 0.05 at. %, respectively, at that voltage (Table 3). The elevated [C] and [Ar] impurities could partly explain the rise in film GPC when $\langle V_{bias} \rangle$ was increased from -187 V to -255 V. The [H] content did not change significantly when $\langle V_{bias} \rangle$ was increased beyond -130 V (Table 3). The trends in resistivity and mass density also entered their second stage when using $\langle V_{bias} \rangle$ larger than -130 V with the resistivity becoming larger and the mass density decreasing. Furthermore, increase in $\langle V_{bias} \rangle$ beyond -130 V also initiated the next stage in residual stress behavior with a relaxation of the compressive stress (Figure 11d), similar to the trends in resistivity and mass density. For the (111) and (220) diffraction peaks in the XRD pattern, the intensities and widths became significantly smaller and wider, respectively, while the (200) peak became more prominent on increasing $\langle V_{bias} \rangle$ beyond -130 V (Figure 12). These observations were in line with the onset of amorphization induced by highly energetic ion bombardment,[14,55,56] similar to the cases of TiO_x and HfO_x discussed earlier, and could contribute in lowering the electronic conductivity and mass density of the TiN_x films. Furthermore, the relaxation of compressive stress on increasing $\langle V_{bias} \rangle$ beyond -130 V also indicates that the yield strength of the material could have been exceeded under intense ion bombardment leading to plastic deformation.[14,54,57,58] These aforementioned trends in material properties were concomitant with the re-appearance of voids in the film microstructure for TiN_x deposited with $\langle V_{bias} \rangle$ greater than -130 V (Figure 13d and e). The void fraction increased with increasing $\langle V_{bias} \rangle$ which could also play a role in compressive stress relaxation together with decreasing conductivity and mass density. Other factors that could contribute towards relieving

compressive stress include bubble formation from excess argon incorporation[62,71] and change in composition to TiN_xC_y owing to the significant carbon impurity content seen for the film deposited using -255 V. The RMS roughness of the TiN_x film surface seemed to remain fairly constant (around ~1 nm) when using $\langle V_{bias} \rangle$ during the plasma exposure step.

Hafnium nitride (HfN_x): Figure 14 shows the GPC, resistivity, mass density, residual stress and surface roughness of HfN_x films deposited at 450 °C as a function of $\langle V_{bias} \rangle$ applied during the H_2 plasma exposure step. All films were deposited with $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s plasma exposure step (solid symbols) apart for a film deposited at $\langle V_{bias} \rangle$ of -210 V applied during the last half (5 s) of the 10 s plasma exposure step (hollow symbols). For the deposition without substrate biasing during plasma exposure, the film had a GPC of 0.35 ± 0.03 Å and a resistivity of (90 ± 7) $\times 10^4$ μΩcm (Figure 14a and b) which are comparable to the values reported by Karwal *et al.*[30] for HfN_x deposited using TDMACpH and H_2 plasma at the same temperature. The low film conductivity was attributed to a high oxygen impurity content of 15 at. % that got incorporated in the film mainly during deposition due to background water present in the ~10^{-6} Torr vacuum environment of the ALD system,[30] similar to what was speculated previously for TiN_x. The HfN_x film deposited without biasing was also observed to have a mass density of 10.1 ± 0.2 g/cm^3, tensile residual stress of 1786 ± 50 MPa and an RMS surface roughness of 2.5 ± 0.2 nm (Figure 14c, d and e).

For the 10 s bias duration condition (bias duty cycle = 100%, Figure 1b), the GPC showed a monotonic increase with increasing $\langle V_{bias} \rangle$ (Figure 14a). This is in contrast to the initial dip followed by a gradual rise in GPC as a function of $\langle V_{bias} \rangle$ observed earlier for TiN_x, but similar to the corresponding trends for TiO_x and HfO_x. However, the film resistivity, mass density and residual stress showed a two stage behavior with increasing $\langle V_{bias} \rangle$, similar to the trends seen before for TiN_x. The use of substrate biasing during the plasma exposure step was observed to trigger a drastic improvement in the electronic properties of HfN_x through a reduction in film resistivity by two orders of magnitude (Figure 14b). For the 10 s bias duration condition, increasing $\langle V_{bias} \rangle$ led to an initial decrease in film resistivity that reached a minimum value of (33 ± 7) $\times 10^2$ μΩcm at -130 V. The mass density initially increased slightly with biasing and reached a peak at the same voltage (Figure 14b). In the initial stage, the residual stress changed from tensile to compressive on applying $\langle V_{bias} \rangle$ during plasma exposure. The compressive stress reached a maximum of -2004 ± 50 MPa on increasing $\langle V_{bias} \rangle$ to -130 V, similar to the minimization of resistivity and peaking of mass density at the same voltage. The RMS surface roughness of the films was observed to decrease slightly with biasing (Figure 14e). For $\langle V_{bias} \rangle$ beyond -130 V applied for 10 s of plasma exposure, an increase in film resistivity, reduction in mass density and relaxation of the compressive
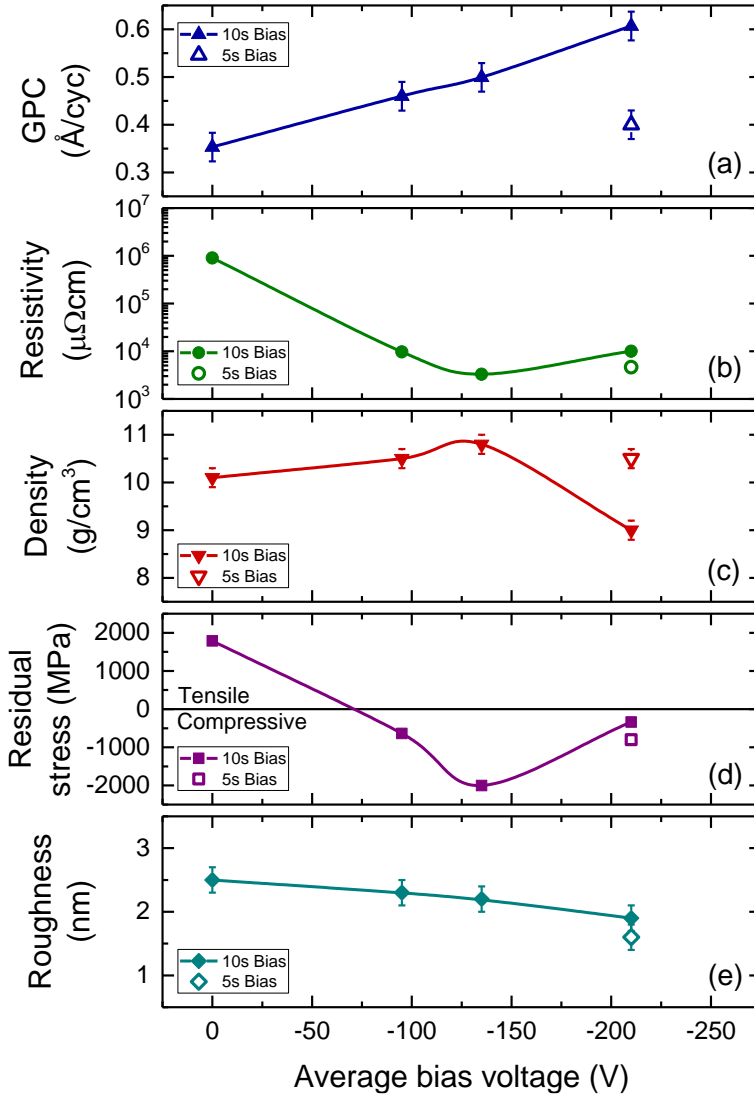
Figure 14. (a) Growth per cycle (GPC), **(b)** resistivity, **(c)** mass density, **(d)** residual stress and **(e)** RMS surface roughness of hafnium nitride films deposited at 450 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied for the entire duration and last half (5 s, only for $\langle V_{bias} \rangle$ = -210 V) of the 10 s H_2 plasma exposure step.

stress (Figure 14b, c and d) signaled a transition to the second stage of HfN$_x$ property variation with substrate biasing. Given the similar trends in material properties for PEALD of TiN$_x$ and HfN$_x$ with substrate biasing, factors that could contribute toward the initial rise in film conductivity, mass density and compressive stress include a reduced oxygen content, improved stoichiometry (i.e., N/Hf ratio closer to 1), enhanced grain size and/or crystalline content, reduced void content and grain boundary density, all induced by energetic ion bombardment. Similarly, for $\langle V_{bias} \rangle$ beyond -130 V, the onset of ion bombardment induced amorphization,[14,55,56] plastic deformation,[14,54,57,58] void creation and/or carbon impurity incorporation could play roles in lowering film conductivity, mass density and compressive stress.

Using $\langle V_{bias} \rangle$ of the same magnitude but different duration/duty cycle during plasma exposure (bias duty cycle = 50%, Figure 1c) created a difference in the way that the growth and material properties of HfN$_x$ were altered, similar to the case observed earlier for TiO$_x$. The growth rate of the HfN$_x$ film deposited using -210 V applied during the last half (5 s) of the 10 s H$_2$ plasma exposure step was significantly lower than the corresponding value obtained using the longer bias duration of 10 s (Figure 14a). A lower resistivity and higher mass density were obtained for the film deposited with the shorter 5 s bias duration compared to the corresponding values of the film grown with the longer 10 s bias duration for the same $\langle V_{bias} \rangle$ magnitude of -210 V (Figure 14c). Similarly, the compressive stress at -210 V was higher when implementing the shorter bias duration of 5 s during H$_2$ plasma exposure (Figure 14d). The surface was also smoother in case of the film grown using 5 s of bias (Figure 14e). These results again demonstrate how altering the bias duration/duty cycle leads to a varying dose or fluence (i.e., particle flux integrated over time) of energetic ions impinging on the substrate, which can provide an alternative route for tuning material properties[13,14,44] during PEALD. Further analysis on the effects of ion energy control with substrate biasing during PEALD of HfN$_x$ will be reported in a subsequent publication.

Silicon nitride (SiN$_x$): The growth and material properties of SiN$_x$ films deposited on planar substrates at 500 °C was investigated for $\langle V_{bias} \rangle$ between 0 V and -103 V applied during the last half (10 s) of the 20 s N$_2$ plasma exposure step. Figure 15 shows these properties in terms of the GPC, refractive index, mass density, residual stress and surface roughness expressed as a function of $\langle V_{bias} \rangle$ applied during plasma exposure. Table 4 outlines additional growth and material properties from RBS analysis for the films deposited with and without substrate biasing. The growth properties are given in terms of the number of silicon and nitrogen atoms deposited per nm^2 per cycle (GPC [Si] and GPC [N], respectively) while the material properties are outlined in terms of the N/Si ratio and impurity content ([O], [C] and [H] at. %).
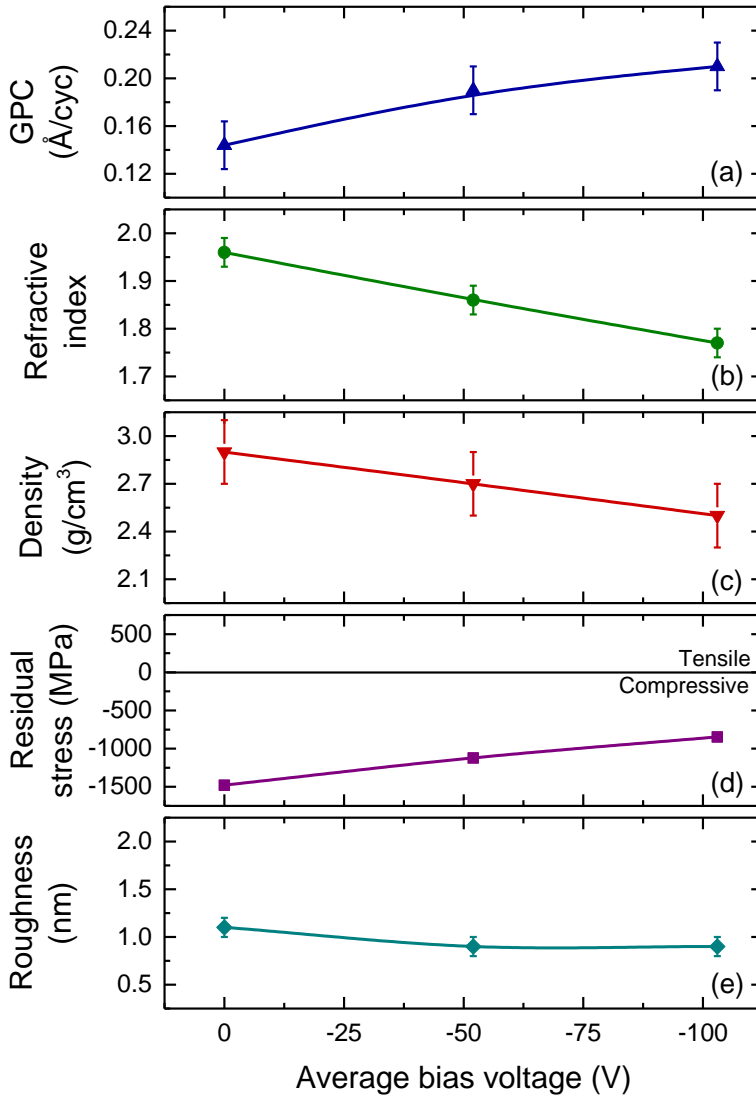
Figure 15. (a) Growth per cycle (GPC), **(b)** refractive index, **(c)** mass density, **(d)** residual stress and **(e)** RMS roughness of silicon nitride films deposited at 500 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied during the N₂ plasma exposure step.

Table 4. GPC (film thickness per cycle and number of atoms deposited per nm² per cycle) and elemental composition of silicon nitride films deposited at 500 °C with and without average bias voltages, $\langle V_{bias} \rangle$, applied during the N₂ plasma exposure step. Typical uncertainties are given in the first row unless otherwise stated.

		RBS					ERD
$\langle V_{bias} \rangle$ (V)	GPC (Å/cycle)	GPC [Si] (#Si at. per nm² per cycle)	GPC [N] (#N at. per nm² per cycle)	N/Si	[O] at. %	[C] at. %	[H] at. %
0	0.14 ± 0.02	0.55 ± 0.02	0.79 ± 0.04	1.4 ± 0.1	2 ± 2	< d.l.[a]	4 ± 3
-103	0.21	0.53	0.91	1.7	10	8 ± 3	6

[a] Values below detection limit (d.l.) of 8 at. % for [C]

In the absence of substrate biasing during plasma exposure, the film had a GPC, refractive index and mass density of 0.14 ± 0.02 Å, 1.96 ± 0.03 and 2.9 ± 0.2 g/cm³ (Figure 15a, b and c), respectively. These values are comparable to the results reported in our previous work[41] for SiNₓ deposited using DSBAS and N₂ plasma at the same temperature. The residual stress of this film was found to be compressive in nature (Figure 15d) similar to that reported previously for SiNₓ deposited at a comparable temperature.[72] The nature of the stress for SiNₓ is unlike the tensile stresses observed earlier for the transition metal compounds deposited without biasing but similar to the compressive stress obtained for SiOₓ. An N/Si ratio of 1.4 ± 0.1 was observed for this film (Table 4) indicating the formation of nearly stoichiometric Si₃N₄ (N/Si ratio of 1.33) for deposition without any biasing. Low impurity contents in terms of [O], [C] and [H] (2 ± 2 at. %, < 8 at. % and 4 ± 3 at. %, respectively) were measured for this film (Table 4) indicating the formation of high quality SiNₓ.

For deposition with substrate biasing, the GPC showed a monotonic increase with $\langle V_{bias} \rangle$ (Figure 15a). Although GPC [Si] remained fairly unchanged, the increase in GPC could be partly explained by an increase in GPC [N] that reached a value of 0.91 ± 0.04 N at./nm² at -103 V (Table 4). This indicated the formation of a nitrogen rich film with increase in $\langle V_{bias} \rangle$ which was corroborated by a higher N/Si ratio of 1.7 obtained for deposition using -103 V (Table 4). The refractive index and mass density showed a monotonic decrease with $\langle V_{bias} \rangle$ (Figure 15b and c). The trends in refractive index and mass density were accompanied by a relaxation of the compressive stress as a function of $\langle V_{bias} \rangle$ (Figure 15d). The film surface became slightly smoother as the RMS roughness decreased with increasing $\langle V_{bias} \rangle$ (Figure 15e). The impurity contents increased with $\langle V_{bias} \rangle$ as observed by the elevated [O], [C] and [H] values at -103 V (Table 4). The simultaneous decrease in refractive index, mass density and compressive stress

together with an increase in the impurity content indicate that energetic ion bombardment through substrate biasing during PEALD of SiN_x degrades its material properties on planar substrates. These monotonic trends in refractive index, mass density and residual stress of SiN_x deposited using relatively small $\langle V_{bias} \rangle$ ($\leq$ -100 V) are unlike any of the trends observed previously for other materials investigated in this work. It suggests that even the slightest increase in ion energies during N_2 plasma exposure could induce plastic deformation,[14,54,57,58] excess nitrogen content, N_2 gas bubble formation,[14,73] and/or void incorporation which could then be factors responsible for film quality degradation. This sort of material degradation was also observed in the other materials (except SiO_x) but only when using comparatively higher $\langle V_{bias} \rangle$ ($\geq$ -130 V), indicating the presence of higher ion energy thresholds for degradation in those materials.

5.5.3 Thickness uniformity on 200 mm substrates

The thickness uniformity of films on large-area planar substrates (200 mm c-Si wafers) was investigated for all six oxides and nitrides deposited with and without substrate biasing. Note that the results obtained were not from optimized precursor dose and plasma exposure times intended for attaining the best uniformities but serve to demonstrate the role of substrate biasing on thickness uniformity during PEALD on large-area substrates. The thickness non-uniformity was defined as the ratio of the standard deviation in thicknesses measured at several points across the wafer to the average thickness of all data points measured. The values obtained are expressed as percentages in Table 5. The results show that for most cases the thickness uniformity of films on 200 mm substrates improved when using substrate biasing during PEALD, except for HfO_x and SiN_x where the uniformity remained fairly unchanged. For TiO_x deposited with biasing, the change in thickness non-uniformity was also observed to depend on the duration or duty cycle of the bias applied during O_2 plasma exposure. The use of a longer bias duration (10 s) increased non-uniformity to 2.8% whereas the same $\langle V_{bias} \rangle$ applied for a shorter bias duration (5 s) decreased non-uniformity to 2.0% relative to the non-uniformity of the film grown without biasing (2.3%). The two transition metal nitride films deposited without biasing had the highest thickness non-uniformities on 200 mm planar substrates (7.5% for TiN_x, 9.4% for HfN_x). The use of substrate biasing during PEALD of these two nitrides led to the most significant improvements in thickness uniformity among all the materials. For TiN_x deposited using -187 V, the thickness non-uniformity decreased to 6.6% while for HfN_x deposited using -210 V (applied for the entire duration of the 10 s H_2 plasma exposure step), the thickness non-uniformity decreased to 7.7%. Interestingly, when HfN_x was deposited using the same $\langle V_{bias} \rangle$ but a lower bias duration of 5 s, the thickness non-uniformity

decreased to an even lower value of 6.7%. These results demonstrate that both the ion energy and the dose of higher energy ions can play roles in altering film uniformity.

Table 5. Thickness uniformity of films deposited on 200 mm planar c-Si wafers without and with average bias voltages, $\langle V_{bias} \rangle$, applied during plasma exposure steps.

	No substrate bias (%)	With substrate bias (%)	$\langle V_{bias} \rangle$ (V)
Titanium oxide	2.3	2.8 [a] , 2.0 [b]	-205
Hafnium oxide	4.6	4.6	-152
Silicon oxide	1.1	0.7	-200
Titanium nitride	7.5	6.6	-187
Hafnium nitride	9.4	7.7 [a] , 6.7 [b]	-210
Silicon nitride	3.5	3.6	-103

[a] Substrate biasing applied for the entire duration of the plasma exposure step
[b] Substrate biasing applied for the last half of the plasma exposure step

5.5.4 PEALD on 3D substrates

Titanium oxide (TiOₓ): The cross-sectional TEM image of a TiO$_x$ layer on 3D trench nanostructures is shown in Figure 16. The film was deposited at 150 °C using -205 V applied during the entire duration of the 10 s O$_2$ plasma exposure step. Film conformalities of 84% and 100% were measured at the bottom-side and bottom regions of the trench, respectively (see Figure A5.9 in Appendix 5). As discussed before, an increase in film GPC was observed during PEALD of TiO$_x$ with substrate biasing on planar substrates. This can cause film GPCs at the planar top and bottom surfaces of the 3D trench nanostructure to exceed the GPC at the vertical bottom-side region and thereby yield a lower conformality at that region of the 3D substrate. Furthermore, the effect of enhanced ion energies is also visible in Figure 16 in terms of the different morphologies of the TiO$_x$ film at planar and vertical surfaces of the 3D trench nanostructures. Previously, it was shown that for PEALD of TiO$_x$ on a planar substrate at 150 °C, an amorphous film was obtained when the deposition was performed without substrate biasing (Figure 6a1 and a2). However, using -205 V during the 10 s O$_2$ plasma exposure step resulted in the formation of polycrystalline TiO$_x$ (Figure 6b1 and b2) in the rutile phase (see Figure A5.7 in Appendix 5) on a planar substrate. As a result, the TiO$_x$ film regions formed at planar top and bottom surfaces of the 3D trench nanostructures in Figure 16 can be assumed to consist of polycrystalline grains formed in the rutile phase while the TiO$_x$ film deposited at the vertical sidewall surface regions can be considered
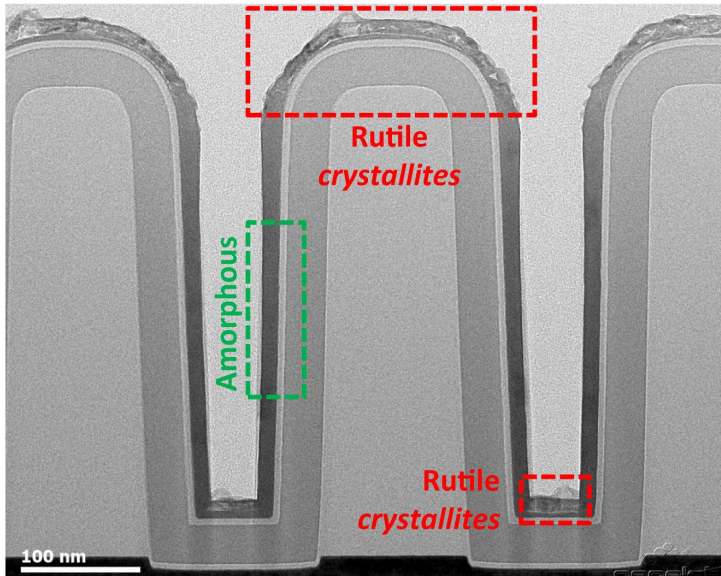
Figure 16. Cross-sectional TEM image of titanium oxide film on 3D trench nanostructures (AR = 4.5 : 1) deposited at 150 °C with an average bias voltage ($\langle V_{bias} \rangle$ = -205 V) applied during the entire duration of the 10 s O_2 plasma exposure step. The presence of crystalline material (rutile) on planar surfaces and amorphous material on vertical sidewall surfaces are indicated.

to be amorphous. This can be explained by the directional or anisotropic nature of ions when they travel through a nearly collisionless plasma sheath[74] before impinging on a substrate. Using substrate biasing makes the directional ions impinge on the planar surface regions of the 3D trench nanostructures with much more energy than on its vertical sidewalls, thereby inducing differing film properties at different regions of the 3D substrate.

Hafnium oxide (HfOₓ): The cross-sectional TEM image of a HfO_x layer on 3D trench nanostructures is shown in Figure 17. The film was deposited at 150 °C using -204 V applied during the O_2 plasma exposure step. Film conformality of 71% and 80% was measured at the bottom-side and bottom regions of the trench, respectively, (see Figure A5.10 in Appendix 5) which is comparable with the results reported by Sharma *et al.*[47] for HfO_x deposited on such 3D trench nanostructures. Similar to the result for TiO_x discussed in the previous section, the role of energetic ion bombardment with substrate biasing during deposition is again observed in Figure 17 where the deposited HfO_x film has different morphologies on the planar and vertical surfaces of the 3D trench nanostructures. Earlier on, it was shown that PEALD of HfO_x on a planar substrate at 150 °C yielded an amorphous film when no $\langle V_{bias} \rangle$ was applied during plasma exposure (Figure 9a1 and a2). The use of -205 V during the O_2 plasma exposure step led to the
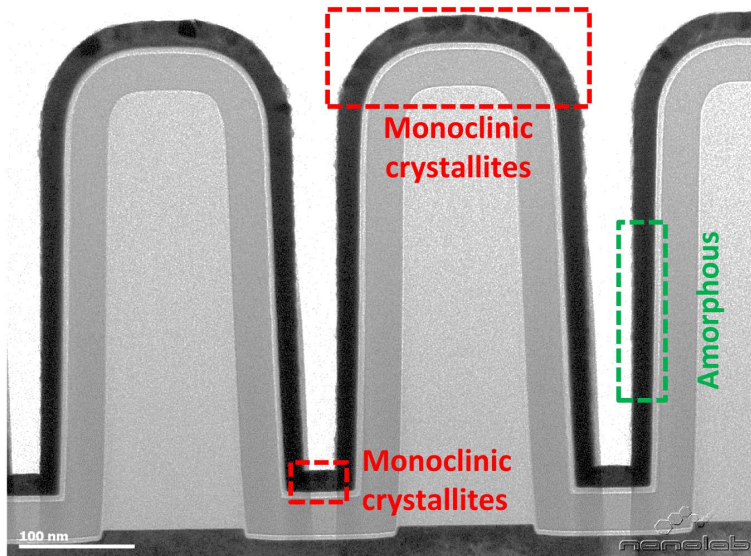
Figure 17. Cross-sectional TEM image of hafnium oxide film on 3D trench nanostructures (AR = 4.5 : 1) deposited at 150 °C with an average bias voltage ($\langle V_{bias} \rangle$ = -204 V) applied during the O_2 plasma exposure step. The presence of crystalline material (monoclinic) on planar surfaces and amorphous material on vertical sidewall surfaces are indicated.

growth of polycrystalline HfO_x (Figure 9b1 and b2) with a monoclinic crystal lattice structure (Figure 8). Consequently, the HfO_x film region at the planar top and bottom surfaces of the 3D trench nanostructures in Figure 17 can be expected to consist of polycrystalline monoclinic grains while the HfO_x film grown at the vertical sidewall surface regions can be assumed to be amorphous. This can again be attributed to the role of directional ions travelling through a nearly collisionless plasma sheath that bombard planar surface regions of the 3D trench nanostructures with more energy than the vertical sidewalls when implementing substrate biasing. The results obtained for HfO_x effectively reproduce the phenomenon seen earlier for TiO_x where enhancing the energy of directional oxygen ions during film deposition induced simultaneous growth of different phases (crystalline and amorphous) of the same material at different surfaces (planar and vertical) of a 3D substrate.

Silicon nitride (SiN$_x$): Cross-sectional TEM images of SiN_x layers on 3D trench nanostructures are shown in Figure 18. The images for as-deposited films grown at 500 °C without any substrate biasing and with -103 V during N_2 plasma exposure are shown in Figure 18A and B, respectively. Conformalities of 37% and 56% were obtained at the bottom-side and bottom of the trench structures, respectively, for the film deposited without any $\langle V_{bias} \rangle$ (Figure 18A), similar to the values reported by in our previous work[41]
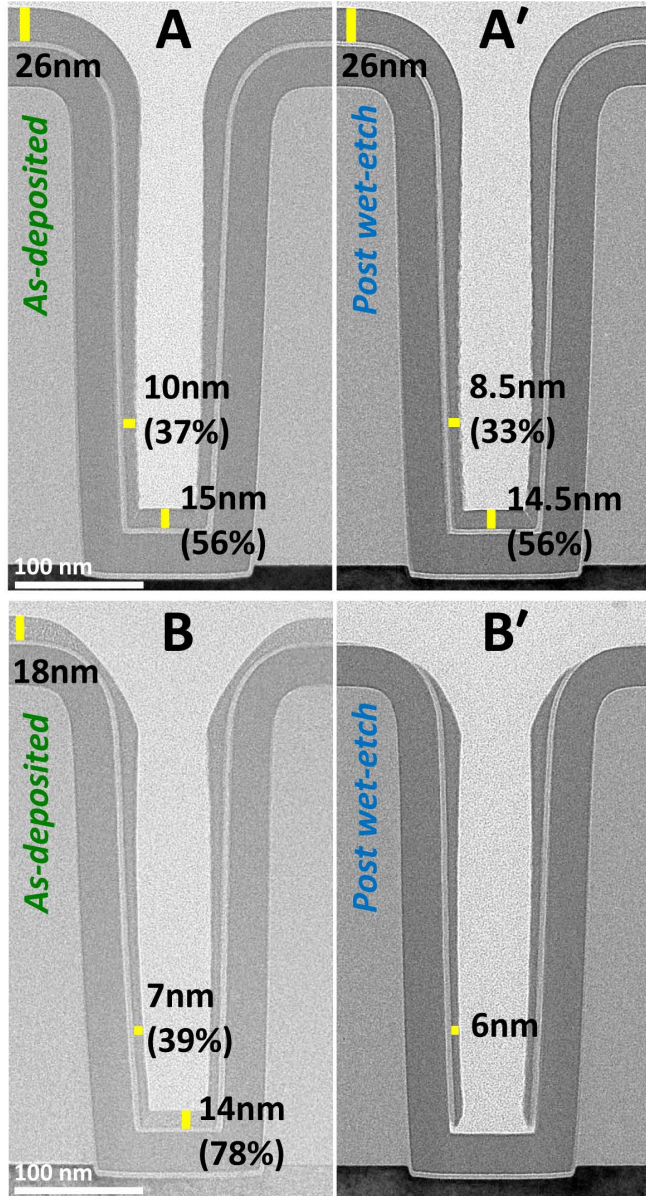
Figure 18. Cross-sectional TEM images of **(A)**, **(B)** as-deposited and **(A')**, **(B')** post wet-etch (in 30 s dilute HF) silicon nitride films grown on 3D trench nanostructures (AR = 4.5 : 1) at 500 °C. Images **(A)** and **(A')** are for films deposited without substrate biasing ($\langle V_{bias} \rangle$ = 0 V) while images **(B)** and **(B')** are for films deposited with substrate biasing ($\langle V_{bias} \rangle$ = -103 V). Film conformality at the bottom-side and bottom regions of the trench are indicated as a percentage of film thickness at the top of the trench.

Table 6. Wet-etch rates of silicon nitride on 3D trench nanostructures (AR = 4.5 : 1) for films deposited at 500 °C without ($\langle V_{bias} \rangle$ = 0 V) and with substrate biasing ($\langle V_{bias} \rangle$ = -103 V) applied during N_2 plasma exposure. The wet-etch rates are reported for silicon nitride films located at planar (*top*, *bottom*) and vertical (*bottom-side*) regions of the 3D substrate topographies after 30 s dip in an etchant solution of dilute hydrofluoric acid (HF : H_2O = 1 : 100). Typical uncertainties are given in the first row.

$\langle V_{bias} \rangle$ (V)	Wet-etch rate (nm/min)		
	Top	*Bottom-side*	*Bottom*
0	0 ± 1	3 ± 1	1 ± 1
-103	Completely etched	2 ± 1	Completely etched

for SiN$_x$ deposited on such 3D substrates. The bottom-side film conformality improved slightly to 39% while that at the bottom improved significantly to 78% for the film deposited using -103 V during N_2 plasma exposure (Figure 18B). Note that some significant corner tapering was observed for the SiN$_x$ film deposited with -103 V. The quality of these SiN$_x$ films was analyzed by measuring their etch resistance in dilute hydrofluoric acid solution (HF : H_2O = 1 : 100). The as-deposited films underwent a 30 s wet-etch treatment in dilute HF and cross-sectional TEM images of the films were measured after the etch treatment. Figure 18A′ and B′ show the post wet-etch TEM images of the films deposited without any substrate biasing and with -103 V applied during N_2 plasma exposure, respectively. The wet-etch rate (WER) values were determined by comparing the as-deposited and post wet-etch film thicknesses at three different regions (top, bottom-side, bottom) of the 3D trench nanostructures which are outlined in Table 6. The SiN$_x$ film deposited without biasing seemed to be highly etch resistant at the planar top and bottom regions of the trench as indicated by the small or insignificant WER values (≤1 ± 1 nm/min, Table 6) at those regions. These low WERs indicate the formation of high quality SiN$_x$ films on planar top and bottom surfaces of the 3D trench nanostructures for deposition without any substrate biasing. This is also in agreement with the high mass density, refractive index (Figure 15b, c) and low impurity content (Table 4) of SiN$_x$ deposited without biasing on a planar c-Si substrate, as discussed earlier. The WER observed at the bottom-side region of the trench (3 ± 1 nm/min, Table 6) is relatively higher than those at the two planar trench regions, indicating a reduced HF-etch resistance of SiN$_x$ at the vertical trench sidewalls. However, the value is small in absolute magnitude indicating an overall high HF-etch resistance at both planar and vertical trench surfaces for the film deposited without substrate biasing.

For the SiN$_x$ film deposited with -103 V during N$_2$ plasma exposure, the film regions located at the planar top and bottom surfaces of the trench exhibited very high WERs and were completely removed after the etch treatment (Figure 18B'). These high WERs indicate the degradation of SiN$_x$ films on planar top and bottom surfaces of the 3D trench nanostructures for deposition with substrate biasing. This is corroborated by the lower refractive index, mass density (Figure 15b, c) and higher impurity content (Table 4) observed earlier for SiN$_x$ deposited on planar substrates using -103 V during N$_2$ plasma exposure. However, SiN$_x$ film regions located at the vertical sidewalls of the trench nanostructures exhibited low WERs ($\sim$2 $\pm$ 1 nm/min, Table 6), similar to that for the film deposited without biasing, and remained selectively at the trench sidewalls after the wet-etch treatment (Figure 18B'). This can again be explained by the combined factors of high energy and directionality of the plasma ions travelling through a nearly collisionless plasma sheath when $\langle V_{bias} \rangle$ is applied to the substrate. These energetic ions collide with much more energy on the horizontal top and bottom surfaces of the 3D trenches than the vertical sidewalls. Consequently, the SiN$_x$ films growing at the top and bottom trench regions are selectively degraded in comparison to those growing at the sidewalls. As a result, the film regions obtained at those sidewalls for deposition with substrate biasing retain the high quality and HF-etch resistance inherent for films formed at the same vertical surfaces for deposition without any $\langle V_{bias} \rangle$.

5.6 Discussion

5.6.1 $\langle V_{bias} \rangle$ regimes during PEALD for tuning properties

The results obtained in this work demonstrate how substrate biasing during PEALD can have prominent effects on the growth and material properties of oxide and nitride thin-films. In the case of the four transition metal compounds, the trends in material properties as a function of $\langle V_{bias} \rangle$ mostly showed a two stage behavior composed of an initial buildup (or decrease) followed by a gradual fall (or increase) with increasing $\langle V_{bias} \rangle$. These trends observed for the large range of $\langle V_{bias} \rangle$ investigated in this work enabled identification of regimes for material property improvement (i.e., higher refractive index, conductivity and mass density) and degradation in PEALD processes. $\langle V_{bias} \rangle$ up to approximately -150 V during O$_2$ plasma exposure and -130 V during H$_2$ or Ar+H$_2$ plasma exposure improved material properties of the transition metal oxide and nitride films, respectively. Applying $\langle V_{bias} \rangle$ beyond these values showed material property degradation. For silicon oxide and silicon nitride, a one stage behavior was observed where material properties remained fairly unchanged for the former and instantly degraded for the latter as a function of substrate biasing. Besides varying $\langle V_{bias} \rangle$ magnitude, reducing the duration of substrate biasing during plasma exposure extended the $\langle V_{bias} \rangle$ regime for improving TiO$_x$ material properties to about -200 V.

These results indicate that regimes exist not only for the ion energy but also for the dose of higher energy ions. Consequently, both the magnitude of ⟨V_{bias}⟩ and the duration/duty cycle of the applied bias can be used as tuneable parameters for influencing ion-surface interactions by modifying the ion energy and dose/fluence of higher energy ions, respectively. It is interesting to note that even though an H_2 plasma generates lighter ions (e.g., H_3^+, H^+) than an $Ar+H_2$ plasma (e.g., ArH^+, Ar^+), similar trends in material properties were observed for the two transition metal nitrides when grown using these two plasmas with substrate biasing. This will be investigated in future work on the basis of growing a transition metal nitride using these plasmas with substrate biasing and measuring the corresponding ion characteristics (e.g., energy, flux, etc.) and material properties. Furthermore, the trends in material property variation reported for substrate biasing during conventional flux-controlled deposition processes (PECVD or PVD) are similar to those observed in the surface-controlled PEALD processes of this work for all films[62,75–78] except SiN_x. Enhancing ion energies during PEALD of SiN_x with relatively small ⟨V_{bias}⟩ (< -100 V) lowered mass density, refractive index and compressive stress while simultaneously increasing WER which are opposite to the trends reported for SiN_x PECVD or PVD processes with substrate biasing.[79,80] Even for substrate biasing during PEALD, the mass density of TiO_x as a function of ⟨V_{bias}⟩ increased for films in this work but decreased for films deposited in previous work reported by Profijt *et al.* who used different Ti precursors.[19,20] The unique trends in property variation with substrate biasing signify how the effects of controlling ion-surface interactions can be highly material and/or process specific. It therefore, necessitates further empirical investigation of other materials and process conditions for PEALD with substrate biasing.

As mentioned in the Introduction section, several inherent characteristics of the material deposited using varying ion energies and/or doses of higher energy ions can also influence the final film properties. It is beyond the scope of this work to provide a detailed account correlating all the characteristics with the observed results, so a brief discussion is made based on two factors. For instance, the bond energies are higher for oxides relative to nitrides for the six materials investigated in this work (see Table A5.1 in Appendix 5). This could play a role in the transition metal oxides showing a higher ⟨V_{bias}⟩ threshold than the corresponding nitrides before the onset of material degradation (i.e., reduction of mass density, increase in film void content and amorphization). Indeed, Si–O has the highest and Si–N the lowest bond energy among the six materials which could also be a factor behind SiO_x material properties remaining fairly unchanged even at large ⟨V_{bias}⟩ (> -200 V) while SiN_x films degraded at low ⟨V_{bias}⟩. Furthermore, the four transition metal compounds investigated in this work have been reported to form in a crystalline phase for PEALD processes between 100 and 250 °C (see Table A5.2 in Appendix 5). PEALD processes for SiO_x and SiN_x reported in the

literature so far have yielded only amorphous films since these materials require much higher temperatures for crystallization (> 900 °C, see Table A5.2 in Appendix 5) either during deposition or post-deposition annealing treatment. The high crystallization temperature could be a reason why the silicon compounds showed a one stage behavior compared to the two stage behavior of the transition metal compounds whose crystalline properties (phase, volume fraction) varied with enhanced ion energies.

5.6.2 Prospects for substrate biasing during PEALD

On the basis of the results obtained in this work, the implementation of substrate biasing during PEALD can provide several opportunities for enhancing the capabilities of atomic scale processing. Controlling the energy and/or dose of ions during the plasma exposure step can enable the tuning of a wide range of material properties for the same precursor/plasma reactants and deposition temperature. Furthermore, the crystalline phase of certain materials such as the transition metal compounds can be obtained using low temperatures at which PEALD without substrate biasing typically yields amorphous films. This also eliminates the requirement of specific substrate surfaces to deposit a high temperature crystalline phase material at a low temperature, for example, the need for a RuO_2 surface to deposit rutile phase TiO_2 at 250 °C.[81] This phase is known to have a high dielectric constant which is a desired property for semiconductor device applications.[81] Furthermore, mixed phase anatase + rutile TiO_2 is reported to have a higher photocatalytic activity[26] than the individual phases while films with small grains and/or a porous microstructure (i.e., high surface to volume ratio) have a higher sensitivity for gas sensing.[82]

During PEALD of TiN_x in this work, the Ti−N bonds in the deposited film originated from Ti−N bonds present in the TDMAT precursor. Substrate biasing during the subsequent reducing $Ar+H_2$ plasma step altered material composition by lowering [O] content that could have originated from background impurities in the vacuum environment. The chemical composition could also be modified at high $\langle V_{bias} \rangle$ by an increase in [C] content. While a low [O] and [C] content yielded more conductive TiN_x, an increase in [C] content could have an influence on the material work function.[83] The decrease in [O] content enabled by substrate biasing during a reducing plasma could in principle, be applicable for varying the composition of metal oxide films deposited with precursors containing metal−O bonds. Recently, it was shown that sub-stoichiometric TaO_x films could be obtained with PEALD using $Ta(OC_2H_5)_5$ as the precursor (that already contained Ta−O bonds) followed by a reducing $Ar+H_2$ plasma.[84] This process scheme led to the incorporation of oxygen vacancies in the deposited metal oxide. In this regard, it can be speculated that enhancing ion energies during the reductive plasma step could potentially confer *in-situ* control over the amount of generated oxygen vacancies. As a

result, PEALD with substrate biasing could be a method for growing sub-stoichiometric metal oxide layers with a tunable composition, relevant for emerging applications such as resistive nonvolatile memory devices e.g., RRAMs.[85]

Substrate biasing during PEALD has thus far been implemented in the second step of a two-step PEALD process, i.e., during the B step of an $(AB)_n$ process where n is the number of cycles. It could also be implemented in multistep PEALD processes, such as during the third C step of an $(ABC)_n$ cycle or an $[(AB)_xC]_n$ supercycle, where x is the number of AB cycles completed before the C step is performed and n is the number of supercycles (see Figure A5.1 and A5.2 in Appendix 5).[18] Furthermore, substrate biasing during PEALD has so far been carried out using reactive plasmas where enhancing ion energies result in combined physicochemical process during film growth. Using an inert plasma (e.g., Ar) in the C step of the aforementioned multistep cycles and applying a bias only at that step could in principle, lead to purely physical effects during energetic ion bombardment. Such purely physical processes could induce differences in the trends of material property variation as a function of substrate biasing.[86] Other variants of multistep PEALD supercycles are used to deposit layered film stacks (or nanolaminates[87]) that rely on the differences in properties of the individual layers. These differences are generally procured by growing at least two different materials alternately for the stacked layers. Since enhanced ion energies during PEALD can tailor the properties of a given material, stacked layers with different properties using the same material could in principle, be created by growing one layer without (Figure 1a) and the next layer with substrate biasing (Figure 1b or c). An example of such a stack is given in Figure A5.11 in Appendix 5. This technique could also be employed for growing films on sensitive substrates that cannot withstand the effects of enhanced ion energies. Deposition with biasing can be carried out only after initially performing some PEALD (or even thermal ALD) cycles without any biasing on such substrates. This could in principle, lead to energetic ion-surface interactions on the initial layer of the deposited film and not on the substrate, provided the initially grown layer is of a sufficient thickness (see Figure A5.11 in Appendix 5). For stacked layers comprised of different materials, substrate biasing during PEALD can enable better control over the properties of those layers, e.g., by reducing tensile stress of HfO_2 layers in HfO_2/Al_2O_3 bi-layers to prevent delamination.[23] Film growth with steadily increasing/decreasing bias voltages with each subsequent cycle could also enable tailoring of interface properties, e.g., formation of a gradually changing instead of an abrupt interface.

Furthermore, substrate biasing during plasma exposure can also be implemented as pre- or post-deposition treatment steps which, based on the reactants used and the treatment duration, can modify surface or sub-surface regions (i.e., a few monolayers below the surface). This can enable in-situ surface functionalization that can either

promote or inhibit film growth. For the case of substrate biasing applied in an interleaved manner in the plasma step (i.e., during a part of the plasma exposure time), another aspect that could potentially influence material properties is variation of the moment at which the bias is applied. For instance, a 50% bias duty cycle can be implemented in a 10 s plasma step by applying it for 5 s during either the first, middle or last half of the plasma exposure time. Simultaneous ignition of the plasma and the bias could lead to the cracking of bulky ligand species (e.g., amino, cyclopentadienyl, isopropoxide, etc.) remaining on the surface after precursor adsorption by the impact of high energy ions. This could lead to the incorporation of decomposed ligand species in the growing film and elevate film impurity content. Therefore, a means to prevent this could be to apply the bias near the end of the plasma exposure step as used in this work which should, in principle, lead to a cleaner or more ligand-free surface before the impingement of energetic ions.

Substrate biasing during PEALD of the two transition metal oxides on 3D trench nanostructures led to the simultaneous formation of different material phases at different surface orientations during growth of the same material in the same deposition run. This indicates how controlling the energy of directional ionic species in a collisionless plasma sheath allows for selective processing during PEALD on 3D substrates. A similar effect was also observed in case of SiN_x where enhanced ion energies during film growth induced selective degradation of material properties for the same material at different surface regions of a 3D substrate. Different categories of selectivity during film growth have been previously defined in terms of area-, phase-, microstructure- and/or chemical composition-selective deposition.[88] Recently, a new approach for carrying out selective deposition on 3D substrates was reported by Kim et al.[3] Selective surface treatment of planar regions in 3D trench nanostructures was performed using directional ions that enabled selective anisotropic deposition of Pt only on the vertical sidewalls of the trenches. This approach for growing films in an area-selective manner on 3D substrates having different geometries or topographical orientation was termed as topographically selective deposition. In this regard, the results obtained in this work demonstrate how ion energy control with substrate biasing during PEALD offers an alternative pathway for topographically selective deposition. Based on the aforementioned selective growth categories, substrate biasing during PEALD on 3D substrates can be considered to induce microstructure (or chemical composition) selective growth of SiN_x and phase selective growth of TiO_x and HfO_x at different surface regions of the 3D substrates. Implementing such variants of selective growth on 3D substrates therefore, enables different routes for conducting topographically selective deposition.

The selectivity attribute imparted by the directional impingement of high energy ions could in principle, be tuned (attenuated) by controlling (lowering) the directionality and/or energy of the ions. When substrate biasing is implemented in a collisional plasma sheath that can be obtained at high pressure conditions (e.g., > 100 mTorr), both the directionality and the energy of the ions are affected. At these conditions, the ion mean free path becomes smaller than the thickness of the plasma sheath causing the ions to experience collisions with gas-phase species while crossing the sheath. These collisions alter the vertical trajectory of the ions while transferring both charge and energy to neutral gas-phase species such as the reactive plasma radicals. As a result, the energy of ions impinging on planar substrate surfaces can become considerably lower than the voltage drop across the plasma sheath. The gas-phase collisions could also lead to the impingement of both ions and radicals on the vertical surfaces of a 3D structure. Depending on the pressure and magnitude of substrate bias applied during plasma exposure, the energy of the ions and radicals colliding with sidewalls could in principle, be higher than the energy of the same species interacting with the sidewalls in a nearly collisionless plasma sheath. This could have direct implications on the conformality and material properties of films deposited on 3D substrates. Therefore, substrate biasing during PEALD on 3D substrates with highly collisional plasma exposures offer new avenues for investigation.

5.7 Conclusions

The effects of modifying ion-surface interactions during PEALD on the growth and material properties of oxide (TiO_x, HfO_x, SiO_x) and nitride (TiN_x, HfN_x, SiN_x) thin-films have been investigated using a commercial 200 mm remote plasma ALD system equipped with RF substrate biasing. The magnitude of $\langle V_{bias} \rangle$ and the duration/duty cycle of the applied bias during plasma exposure were demonstrated as parameters for influencing ion-surface interactions by modifying the ion energy and dose/fluence of higher energy ions, respectively. Controlling these parameters had significant material and/or process specific effects that enabled tailoring of a wide range of properties during film growth. These include, but are not limited to, the mass density, optical refractive index, electrical resistivity, residual stress, crystalline properties (e.g., volume fraction, phase, grain size, etc.), void fraction, surface roughness, thickness uniformity (on large area planar substrates) and chemical composition, which are summarized in Figure 19.

As long as ion energies remained below the regimes for ion-induced degradation, enhancing ion energies by increasing $\langle V_{bias} \rangle$ led to an improvement in the mass density for all materials except SiN_x which degraded with substrate biasing. A higher mass

Figure 19. A schematic illustration representative of the material properties and process control enabled by substrate biasing during PEALD on planar and 3D substrate topographies.

density was generally accompanied by an increase in the optical refractive index of dielectric films. Growth of a denser material with biasing also indicated the presence of a compact film with a void free microstructure while the growth of underdense material generally led to an increase in the film void content. Enhancing ion energies with substrate biasing significantly reduced the electrical resistivity of the two transition metal nitrides. This was also accompanied by a significant reduction of the oxygen impurity content in TiN_x while implementing a high $\langle V_{bias} \rangle$ elevated the film carbon content. These serve to demonstrate how substrate biasing can be used for tuning the chemical composition of materials. The residual stress could be tailored from tensile under no bias conditions to compressive with substrate biasing for the transition metal compounds whereas that for the silicon compounds remained compressive as a function of $\langle V_{bias} \rangle$.

Substrate biasing during PEALD on 3D trench nanostructures effectively depicted the role of directional ion bombardment by inducing distinct film properties at different surface orientations (planar and vertical) of the 3D substrate. For TiO_x and HfO_x at low temperature, biasing led to phase selective growth of crystalline material on planar surfaces and amorphous material on vertical sidewalls of the trenches. For SiN_x, biasing led to microstructure selective degradation of film regions growing at planar surfaces of the trenches but not those growing at vertical sidewalls. These results demonstrate how substrate biasing during PEALD can enable topographically selective growth control on 3D substrates. The insights obtained in this work reveal numerous opportunities afforded by this technique for advancing the practical applications of atomic scale processing. The effects on other material systems, material properties and processing conditions will be reported in future investigations.

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Appendix *5*

Detailed outline of PEALD process conditions

For the deposition of titanium oxide (TiO_x), tetrakis(dimethylamido)titanium or TDMAT [$Ti(N(CH_3)_2)_4$, >99.99% purity from Sigma Aldrich] was used as the precursor while 100 sccm O_2 gas (>99.999% purity) was used for generating a plasma with 200 W RF-ICP power at a pressure of 9 mTorr. The precursor was held in a stainless steel bubbler that was heated to 60 °C at which TDMAT has a vapor pressure of 1 Torr.[1] For the precursor delivery to the deposition chamber, 100 sccm Ar (>99.999% purity) bubbling flow was employed. The precursor dose, purge, plasma exposure and purge times were set to 200 ms, 3 s, 10 s and 3 s, respectively. TDMAT was also used as the precursor for depositing TiN_x in which case a gas mixture of 10 sccm Ar and 40 sccm of H_2 (>99.999% purity) was used for generating a plasma with 100 W RF-ICP power at a pressure of 6 mTorr. For PEALD of TiN_x, the dose and purge times were 200 ms, 3 s, 10 s and 4 s, respectively.

Hafnium oxide (HfO_x) films were grown using tris(dimethylamino)cyclopentadienyl-hafnium or TDMACpH [$CpHf(N(CH_3)_2)_3$, >99.99% purity from Air Liquide] as the precursor while 100 sccm O_2 gas (>99.999% purity) was used for generating a plasma with 400 W RF-ICP power at a pressure of 15 mTorr. The precursor was held in a stainless steel bubbler that was heated to 60 °C at which TDMACpH has a vapor pressure of 100 mTorr.[2] The precursor was delivered to the deposition chamber using 100 sccm Ar (>99.999% purity) bubbling flow. The dose and purge times for PEALD of HfO_x were 200 ms, 3 s, 10 s and 4 s, respectively. TDMACpH was also used as the precursor for depositing HfN_x for which 100 sccm H_2 (>99.999% purity) gas was used for generating a plasma with 100 W RF-ICP power at a pressure of 30 mTorr. Lower pressures were not possible for stable ignition of an H_2 plasma. The dose and purge times for PEALD of HfN_x, were 400 ms, 2 s, 10 s and 4 s, respectively.

PEALD of silicon oxide (SiO_x) was performed using bis(diethylamino)silane or BDEAS [$SiH_2(N(C_2H_5)_2)_2$, >98% purity from Air Liquide] as the precursor while 100 sccm O_2 gas (>99.999% purity) was used for generating a plasma with 200 W RF-ICP power at a pressure of 15 mTorr. The precursor was held in a stainless steel bubbler that was heated to 50 °C at which BDEAS has a vapor pressure of ~10 Torr.[3] Owing to this high pressure, the precursor was vapor drawn into the deposition chamber with the butterfly valve completely closed. In order to maximize precursor utilization, a precursor hold or reaction step was employed immediately after precursor dosage keeping the butterfly valve closed. A continuous flow of 50 sccm Ar gas (purity 99.999%) through the alumina plasma tube was implemented during the precursor dose and reaction steps. This was done in order to reduce precursor adsorption on the inner surfaces of the plasma tube during these two steps. The precursor dose, reaction step, precursor purge, plasma exposure and purge times used for PEALD of SiO_x, were 175 ms, 1 s, 3 s, 5 s and 2 s,

respectively. PEALD of silicon nitride (SiN_x) was carried out using di(sec-butylamino)silane or DSBAS [($SiH_3N(^sBu)_2$), purity >99.3% from Versum Materials] as the precursor while 100 sccm N_2 gas (>99.999% purity) was used for generating a plasma with 600 W RF-ICP power at a pressure of 12 mTorr. The precursor was held in a stainless steel bubbler that was heated to 40 °C at which DSBAS has a vapor pressure of ~5 Torr.[4] Owing to this high pressure, the precursor was vapor drawn into the deposition chamber with the butterfly valve completely closed. A precursor hold or reaction step was again employed immediately after precursor dosage in order to maximize precursor utilization while a continuous flow of 50 sccm N_2 gas (purity 99.9999%) was passed through the alumina plasma tube during the precursor dose and reaction steps. This was again done to reduce precursor adsorption on the inner surfaces of the plasma tube during these two steps.

Substrate biasing during multistep PEALD processes

Step sequences of multistep PEALD processes without and with substrate biasing during plasma exposure are shown in Figure A5.1 and A5.2. In a three step *(ABC)n* process without substrate biasing (Figure A5.1a), a precursor dose step (*A*) is followed by two plasma exposure steps (*B* and *C*) using different co-reactants. These co-reactants can consist of inert, reactive or combined inert + reactive gas flows. When substrate biasing is implemented during plasma exposure, it can be applied either during both (Figure A5.1b) or just one (Figure A5.1c) plasma exposure step. The bias can also be applied in an interleaved manner in the plasma steps, i.e., during a part of the plasma exposure time (see Figure A5.1c of the manuscript). A three step PEALD process can also consist of an [*(AB)xC*]*n* supercycle (Figure A5.2) where *x* number of *AB* cycles are completed before the *C* step is performed and *n* is the number of supercycles. Again, substrate biasing can be applied either during all (Figure A5.2b) or just one (Figure A5.2c) plasma exposure step. The biasing could also be applied in an interleaved manner.
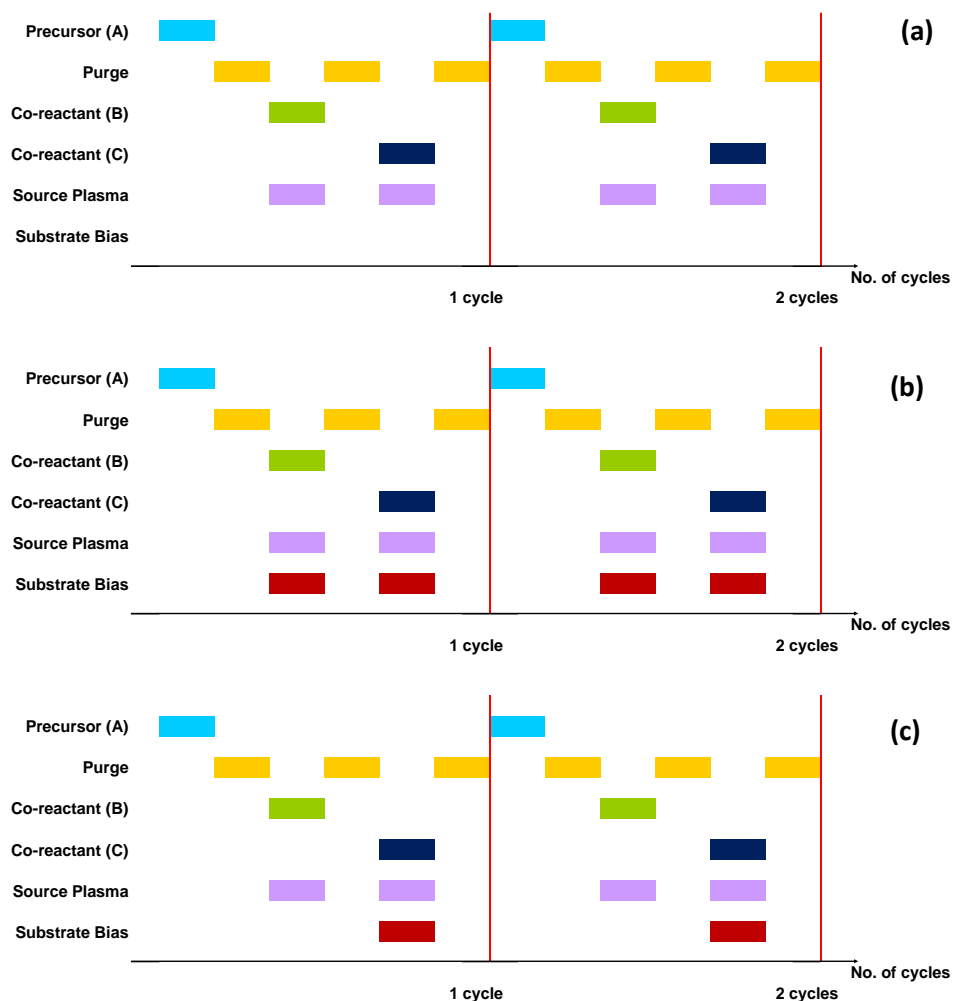
Figure A5.1. Step sequence for multistep *[ABC]ₙ* plasma ALD cycles **(a)** without any substrate bias during plasma exposure where the substrate table is grounded during both the *B* and *C* plasma exposure steps (Source Plasma "ON", Substrate Bias "OFF") **(b)** with substrate biasing during both the *B* and *C* plasma steps where the bias is applied for the full duration of the plasma exposure time (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%) and **(c)** with substrate biasing only during the *C* plasma exposure step where the bias is applied for the full duration of the plasma exposure time (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%). *A* refers to the precursor dose step, *B* the first co-reactant or plasma gas exposure step, *C* the second co-reactant or plasma gas exposure step and *n* is the number of ALD cycles.
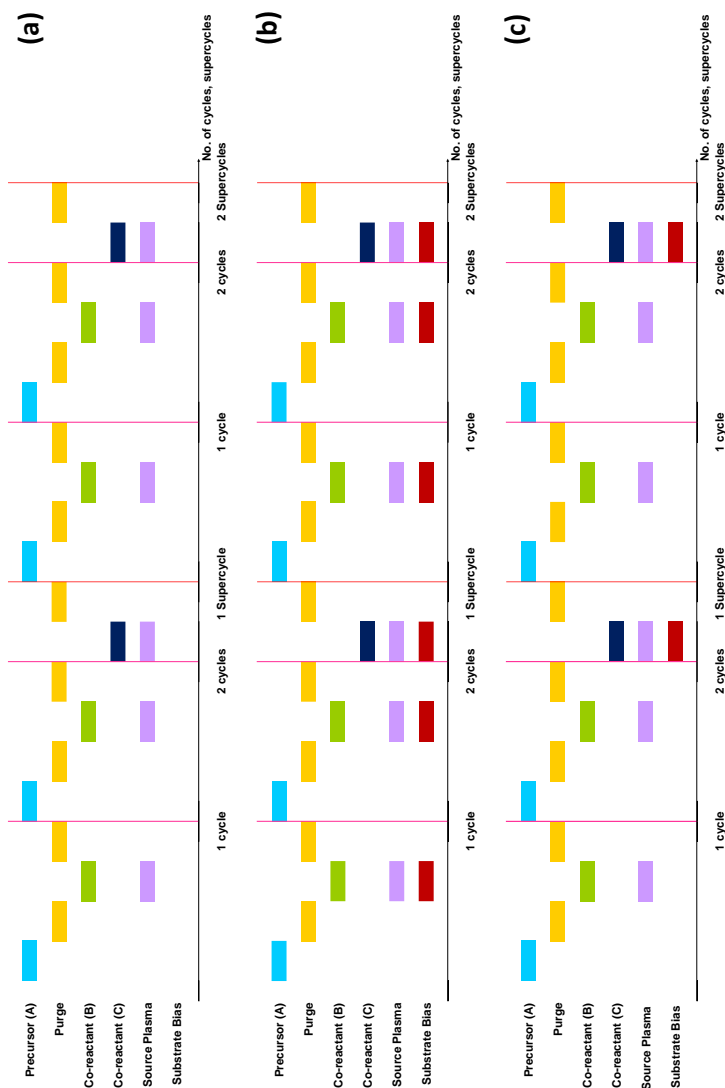
Figure A5.2. Step sequence for multistep $[(AB)_xC]_n$ plasma ALD supercycles **(a)** without any substrate bias during plasma exposure where the substrate table is grounded during both the B and C plasma exposure steps (Source Plasma "ON", Substrate Bias "ON", Substrate Bias "OFF") **(b)** with substrate biasing during both the B and C plasma steps where the bias is applied for the full duration of the plasma exposure time (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%) and **(c)** with substrate biasing only during the C plasma exposure step where the bias is applied for the full duration of the plasma exposure time (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%). A refers to the precursor dose step, B the first co-reactant or plasma gas exposure step, C the second co-reactant or plasma gas exposure step, x is the number of AB cycles completed before the C step is performed and n is the number of PEALD supercycles.
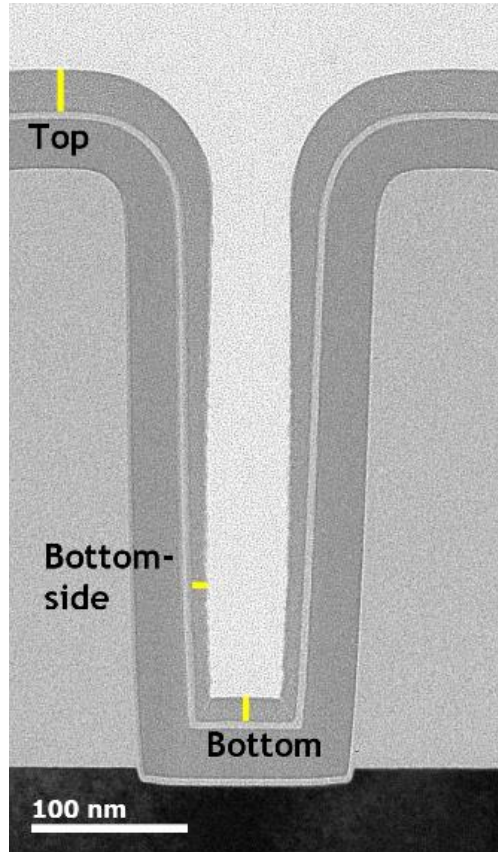
Thickness measurement regions in 3D trench nanostructures

Figure A5.3. Cross-sectional TEM image illustrating the three regions – Top, Bottom-side and Bottom – of a film deposited using PEALD on 3D trench nanostructures (width ∼100 nm, height ∼450 nm, AR = 4.5 : 1). The thickness of the deposited films were measured at these three regions in order to investigate film conformality and wet-etch rates.

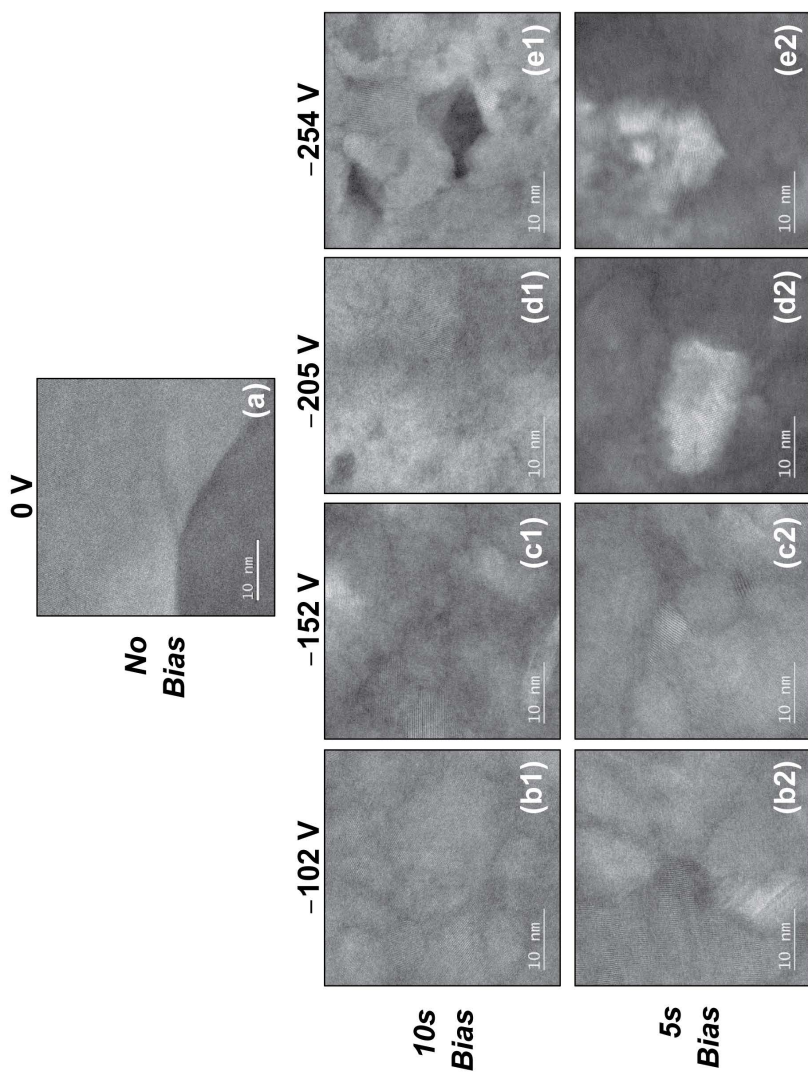## *PEALD of TiO$_x$ without and with biasing on planar substrates*

Figure A5.4. Magnified plan-view high angle annular dark-field (HAADF) STEM images for titanium oxide films deposited at 300 °C with (a) 0 V, (b1 and b2) -102 V, (c1 and c2) -152 V, (d1 and d2) -205 V and (e1 and e2) -254 V average bias voltages, $\langle V_{bias} \rangle$. Images (b1), (c1), (d1) and (e1) denote $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s O$_2$ plasma exposure step while images (b2), (c2), (d2) and (e2) represent $\langle V_{bias} \rangle$ applied for the last half (5 s) of the 10 s plasma exposure step.
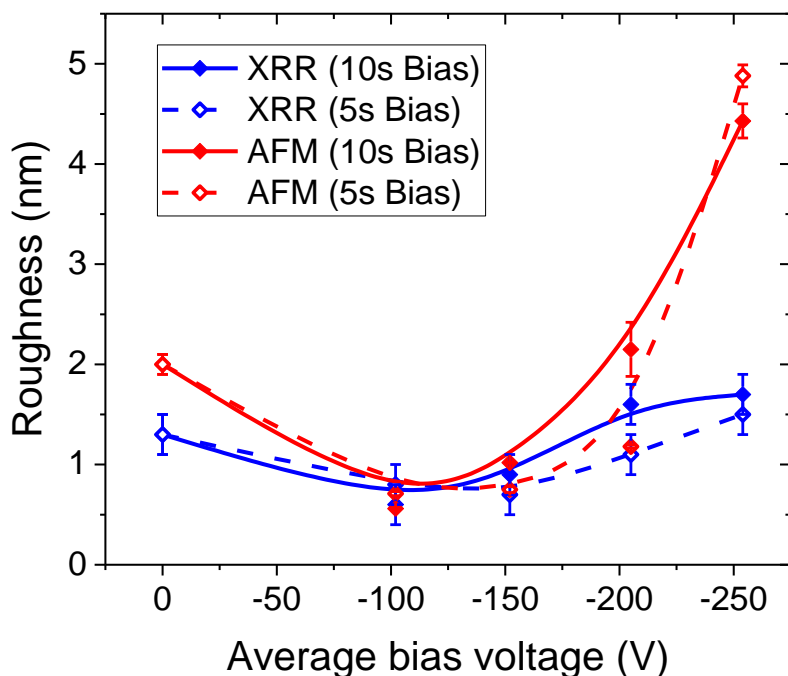
Figure A5.5. RMS surface roughness of titanium oxide films deposited at 300 °C expressed as a function of the average bias voltage, $\langle V_{bias} \rangle$, applied for the entire duration and last half (5 s) of the 10 s O$_2$ plasma exposure step. The data in blue are from x-ray reflectometry (XRR) measurements while those in red are from atomic for microscopy measurements.

Besides x-ray reflectometry (XRR) measurements, atomic force microscopy (AFM) was also used to determine the root-mean-squared (RMS) surface roughness of titanium oxide films. The results are plotted in Figure A5.5 for comparison. The AFM measurements were performed using a Bruker Dimension 3100 system and the RMS surface roughness values were calculated on the basis of 2 μm× 2 μm scans in tapping mode, shown in Figure A5.6. The values from both measurements are comparable to each other at all $\langle V_{bias} \rangle$ except -254 V, where the RMS roughness from AFM is significantly higher than that from XRR. The trends from both results show good correlation. Furthermore, a large lateral grain size was observed for the TiO$_x$ film deposited without biasing (Figure A5.6a) which decreased significantly upon growing TiO$_x$ films with substrate biasing (Figure A5.6b1 to A5.6e1 and Figure A5.6b2 to A5.6e2). This is in agreement with the trends observed for lateral grain dimensions in the HAADF-STEM images (Figure 5 in Chapter 5 and Figure A5.4 in Appendix 5).
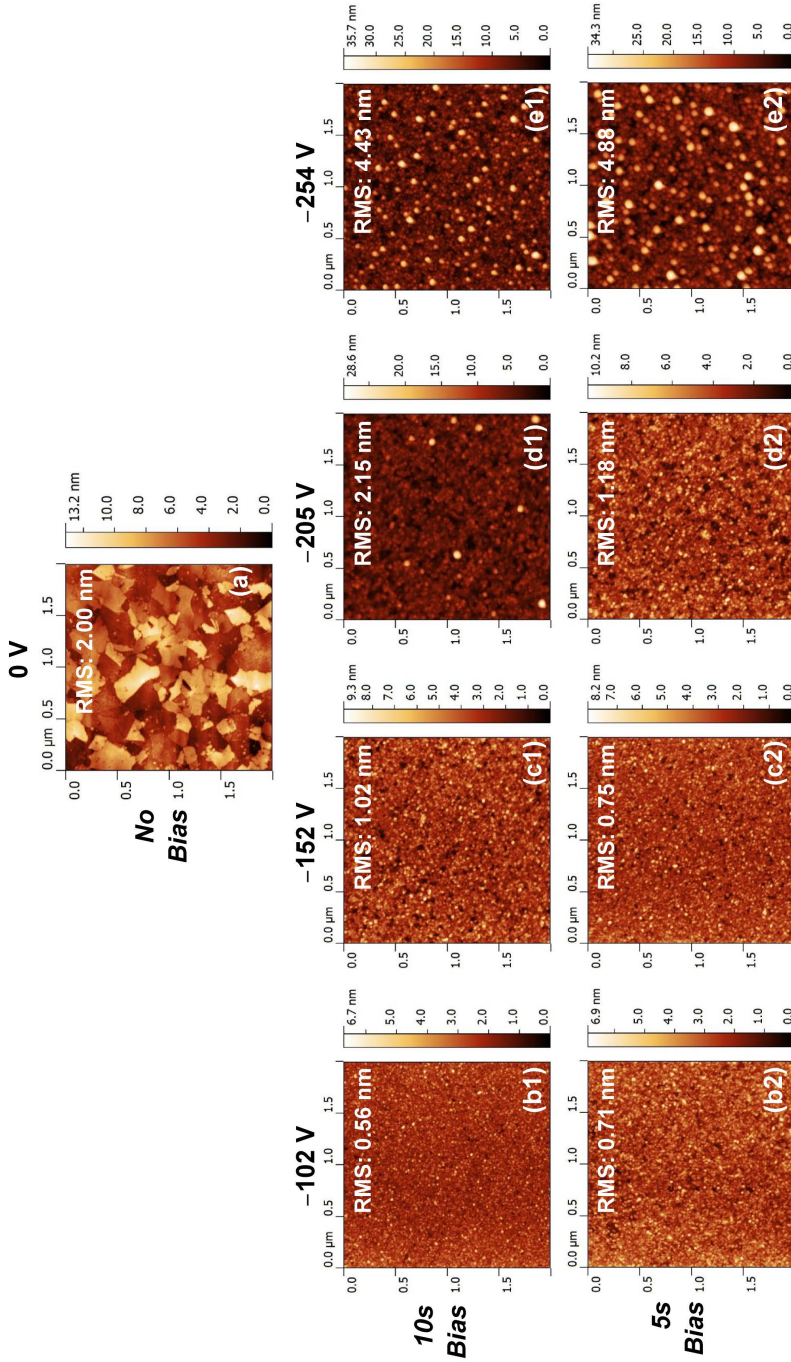
Figure A5.6. Plan-view atomic force microscopy (AFM) scans (2μm × 2μm) for titanium oxide films deposited at 300 °C with **(a)** 0 V, **(b1)**, **(b2)** -102 V, **(c1)**, **(c2)** -152 V, **(d1)**, **(d2)** -205 V and **(e1)**, **(e2)** -254 V average bias voltages, $\langle V_{bias} \rangle$. Images **(b1)**, **(c1)**, **(d1)** and **(e1)** denote $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s O_2 plasma exposure step while images **(b2)**, **(c2)**, **(d2)** and **(e2)** represent $\langle V_{bias} \rangle$ applied for the last half (5 s) of the 10s plasma exposure step. The RMS surface roughness values are indicated for each scan.
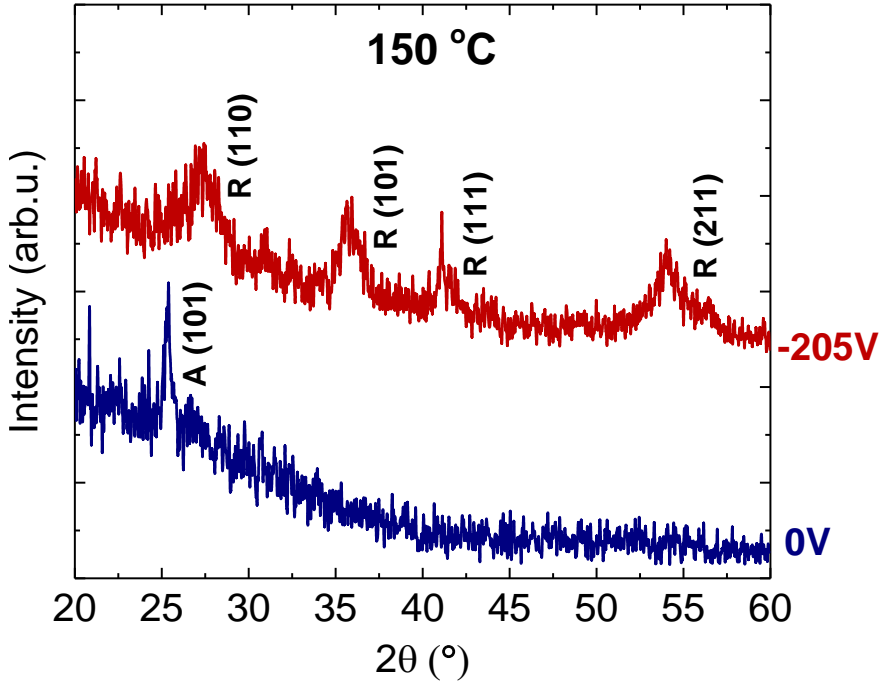
Figure A5.7. Grazing incidence X-ray diffractograms for titanium oxide films deposited at 150 °C with average bias voltages, $\langle V_{bias} \rangle$, ranging from 0 V to -205 V applied for the entire duration of the 10 s O_2 plasma exposure step. Peaks corresponding to the anatase and rutile phase are denoted with "A" and "R", respectively.

PEALD of TiN$_x$ without and with biasing on planar substrates
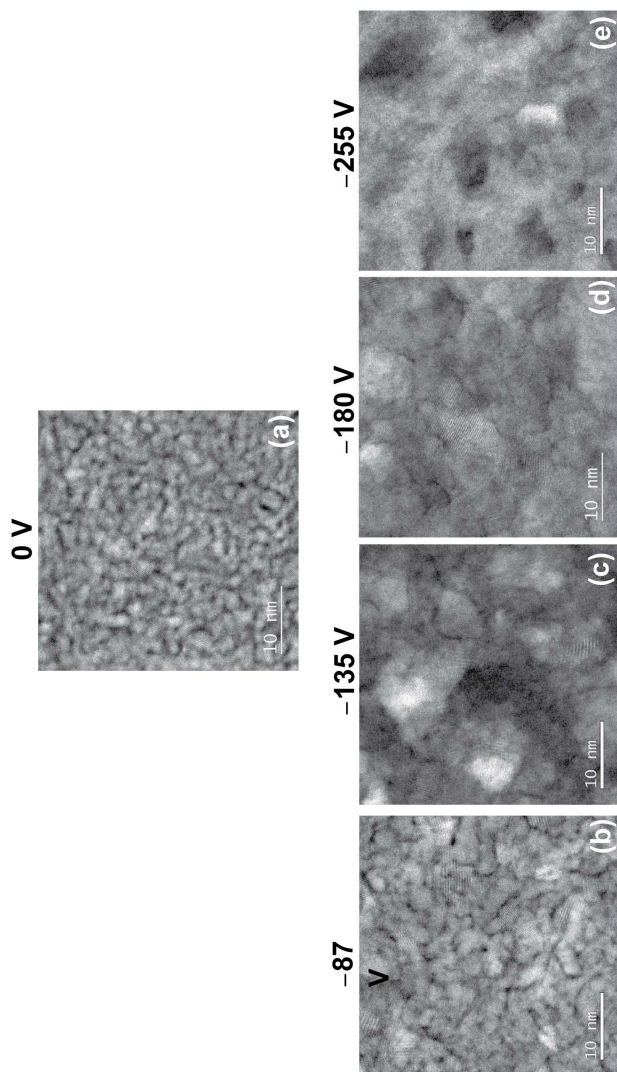
Figure A5.8. Magnified plan-view TEM high angle annular dark-field (HAADF) STEM images for titanium nitride films deposited at 200 °C with **(a)** 0 V, **(b)** -87 V, **(c)** -130 V, **(d)** -187 V and **(e)** -255 V average bias voltages, $\langle V_{bias} \rangle$, applied during the Ar+H$_2$ plasma exposure step.

PEALD of TiO$_x$ with biasing on 3D substrates
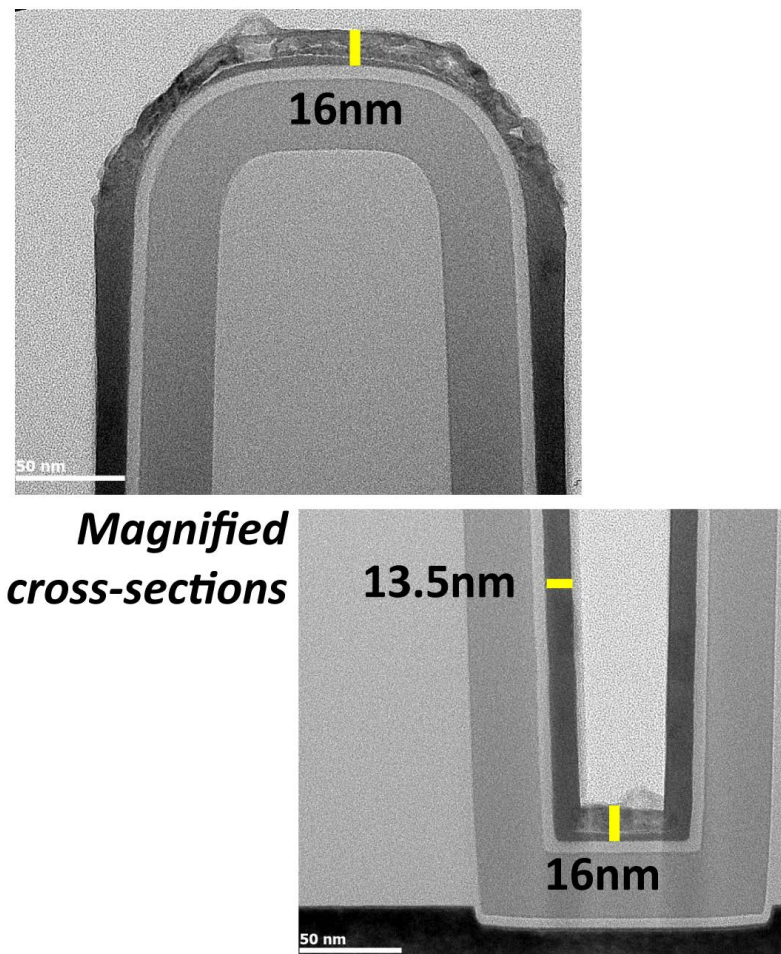
Figure A5.9. Magnified cross-sectional TEM images of titanium oxide film on 3D trench nanostructures (AR = 4.5 : 1) deposited at 150 °C with an average bias voltage ($\langle V_{bias} \rangle$, = -205 V) applied during the entire duration of the 10 s O$_2$ plasma exposure step. Film conformality at the bottom-side and bottom regions of the trench are indicated as a percentage of film thickness at the top.

PEALD of HfO$_x$ with biasing on 3D substrates

Figure A5.10. Magnified cross-sectional TEM images of hafnium oxide film on 3D trench nanostructures (AR = 4.5 : 1) deposited at 150 °C with an average bias voltage ($\langle V_{bias} \rangle$, = -204 V) applied during the O$_2$ plasma exposure step of PEALD. Film conformality at the bottom-side and bottom regions of the trench are indicated as a percentage of film thickness at the top.
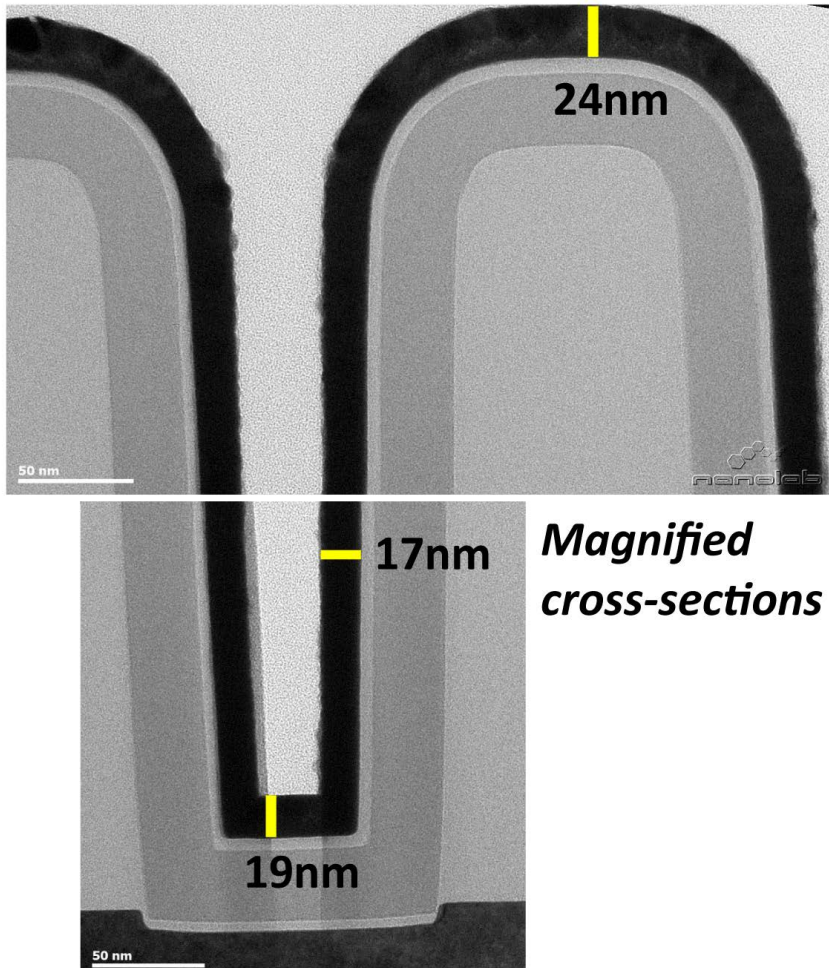
PEALD of SiN$_x$ without and with biasing on planar substrates

Stacked layers with different properties, known as nanolaminates,[14] can be obtained from the same material by growing one layer without and the next layer with substrate biasing, as shown in Figure A5.11a. The top SiN$_x$ layer grown with biasing has a lower contrast, and hence different properties, compared to the bottom SiN$_x$ layer grown while the same substrate was in a grounded configuration during N$_2$ plasma exposure. Comparing the thicknesses of each layer in Figure A5.11a with those of the single layers in Figure A5.11b and A5.11c grown without and with substrate biasing, respectively, reveal SiN$_x$ films of comparable thicknesses. Furthermore, the presence of a fairly sharp interface between the stacked layers is visible in Figure A5.11a. These factors together indicate that SiN$_x$ growth with $\langle V_{bias} \rangle$ of -103 V leads to an ion penetration depth below ~1 nm at the surface of the underlying SiN$_x$ layer grown without biasing. The results demonstrate that for film growth on sensitive substrates that cannot withstand the effects of enhanced ion energies, deposition with biasing can be carried out after initially growing a sufficiently thick layer (~1 nm) without any biasing on such substrates.
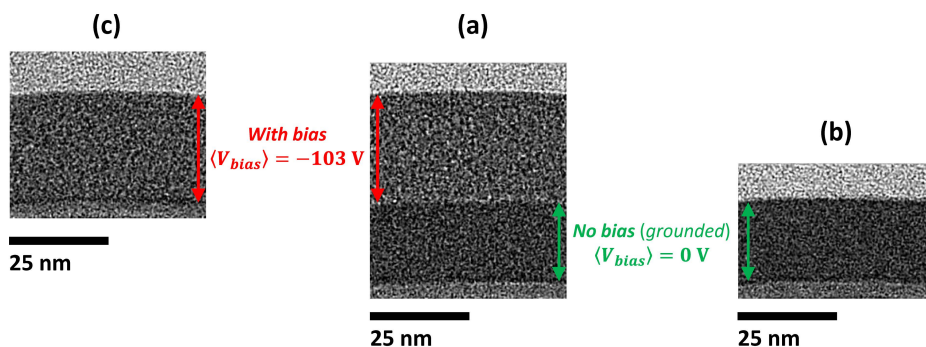
Figure A5.11 Cross-sectional TEM images of (a) stacked layers of silicon nitride films and (b), (c) single layer of silicon nitride film deposited at 500 °C. In image (a) the bottom film layer was first grown without biasing ($\langle V_{bias} \rangle$ = 0 V) after which the top film layer was grown with substrate biasing ($\langle V_{bias} \rangle$, = -103 V) during the N$_2$ plasma exposure step. In image (b) the film layer was grown without substrate biasing ($\langle V_{bias} \rangle$ = 0 V) while in image (c) the film layer was grown with substrate biasing ($\langle V_{bias} \rangle$, = -103 V) during the N$_2$ plasma exposure step.

Bond energies and crystallization temperatures

Table A5.1. Values of typical bond energies in the oxides and nitrides of Ti, Hf and Si.[5]

Bond type	Bond energy (eV)
Si–O	8.27
Hf–O	8.20
Ti–O	6.86
Hf–N	5.53
Ti–N	4.81
Si–N	4.54

Table A5.2. Temperature at which crystalline oxide and nitride films of Ti, Hf and Si have been deposited using PEALD. A "-" indicates no PEALD process has been reported so far yielding crystalline films, indicating the need for high temperature environments[6,7] either during deposition or post-deposition annealing treatments for crystallization.

PEALD film	Crystallization temperature (°C)
SiN_x	-
SiO_x	-
TiO_x	250[8]
HfO_x	250[8]
TiN_x	100[8,9]
HfN_x	250[8,10]

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Energetic Ions during Plasma-Enhanced Atomic Layer Deposition and their Role in Tailoring Material Properties
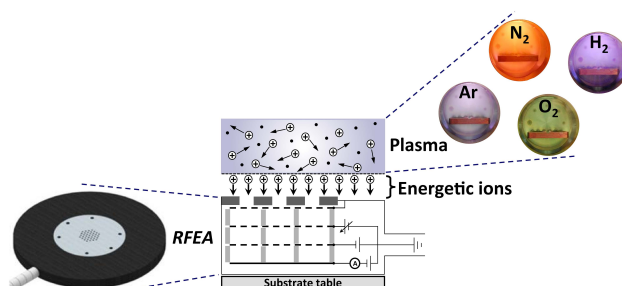
In this chapter, we report on the measurements of ion energy and flux characteristics on grounded and biased substrates during plasma exposure to investigate their role in plasma-enhanced atomic layer deposition (PEALD). Ion flux-energy distribution functions (IFEDFs) of reactive plasmas typically used for PEALD (O_2, H_2, N_2) were measured in a commercial 200-mm remote inductively coupled plasma (ICP) ALD system equipped with RF substrate biasing. IFEDFs were obtained using a gridded retarding field energy analyzer (RFEA, see image above) and the effect of varying ICP power, pressure and bias conditions on the ion energy and flux characteristics of the three reactive plasmas were investigated. The properties of three material examples – TiO_x, HfN_x and SiN_x – deposited using these plasmas were investigated on the basis of the energy and flux parameters derived from IFEDFs. Material properties were analyzed in terms of the total ion energy dose delivered to a growing film in every ALD cycle, which is a product of the mean ion energy, total ion flux and plasma exposure time. The properties responded differently to the ion energy dose depending on whether it was controlled with RF substrate biasing where ion energy was enhanced, or without any biasing where plasma exposure time was increased. This indicated that material properties were influenced by whether or not ion energies exceeded energy barriers related to physical atom displacement or activation of ion-induced chemical reactions during PEALD. Once ion energies were enhanced beyond these threshold barriers with RF substrate biasing, material properties became a function of both the enhanced ion energy and the duration for which the ion energy was enhanced during plasma exposure. These results serve to demonstrate how the measurement and control of ion energy and flux characteristics during PEALD can provide a platform for synthesizing nanoscale films with the desired material properties.

List of symbols

A_{eff}	effective ion sampling area at RFEA collector plate (mm^2)
A_{tot}	total ion sampling area at RFEA entrance orifices (mm^2)
e	elementary charge constant (C)
E_i	ion kinetic energy (eV)
$E_{i,max}$	maximum ion kinetic energy (eV)
$\langle E_i \rangle$	mean ion kinetic energy (eV)
$E_{i,flux}$	total ion kinetic energy flux (eV.nm^{-2}.s^{-1})
$E_{i,dose}$	total ion kinetic energy dose per unit substrate area per ALD cycle (eV.nm^{-2})
ΔE_{LP-HP}	low & high energy peak separation in multi-modal ion flux-energy distribution (eV)
$\mathbf{h}_\Gamma(E_i)$	ion flux-energy distribution function (cm^{-2}.s^{-1}.eV^{-1})
Γ_i	total ion flux (cm^{-2}.s^{-1})
I_C	ion current at RFEA collector plate (A)
J_C	ion current density at RFEA collector plate (A.m^{-2})
J_{CPP}	ion current density measured using a capacitive planar probe (A.m^{-2})
n_o	plasma density (cm^{-3})
$P_{RF,bias}$	RF bias power (W)
P_{ICP}	RF inductively coupled plasma power (W)
$\langle s \rangle$	time-averaged plasma sheath thickness (m)
t_p	duration of plasma exposure (s)
T_e	mean electron temperature (eV)
T_G	net transmission factor of RFEA grid stack
τ_i	ion transit time across a plasma sheath (s)
τ_{RF}	time period of RF bias signal (s)
V_{G2}	retarding voltage on ion discriminator grid of RFEA (V)
$\langle V_{bias} \rangle$	time-averaged substrate bias voltage (V)
V_p	plasma potential (V)
V_{sub}	substrate potential (V)
$\tilde{V}_{RF,bias}$	oscillation amplitude of time-varying RF bias signal (V)
$\tilde{V}_{sh}$	oscillation amplitude of time-varying sheath voltage (V)
ΔV_{sh}	potential across plasma sheath (V)

6.1 Introduction

Continuous downscaling of semiconductor technology nodes and emerging applications in nanotechnology exert rigorous demands on the techniques used in processing materials at the atomic level.[1,2] It has become vitally important to retain proper control over the growth of functional materials when they are deposited on substrates with nanoscale dimensions and three-dimensional (3D) geometries.[3–5] Atomic layer deposition (ALD) is a technique that has been widely adopted for synthesizing nanoscale films of a variety of materials.[6] It is a cyclic deposition process based on sequential and self-limiting precursor and co-reactant dose steps for growing films in a layer-by-layer fashion. These attributes confer excellent growth control that leads to uniform and conformal film deposition even on challenging substrate topographies. For materials that require low processing temperatures or for which thermally driven growth chemistries are not available, an energy-enhanced ALD method can be employed such as plasma-enhanced atomic layer deposition (PEALD).[7,8] In PEALD, a plasma is used during one of the reactant exposure steps of the cyclic deposition process. A plasma constitutes a mixture of highly reactive atomic and molecular neutrals (plasma radicals), photons, ions and electrons. The highly reactive species generated during plasma exposure can provide an alternate source of the energy required for film growth that is typically provided by substrate heating. While the contribution of highly reactive radicals towards film growth is a well-known feature of PEALD, the ions generated during plasma exposure can also play a significant role in the deposition process.

Ion-surface interactions are an inherent feature of plasma-enhanced processing techniques.[9,10] Additional energy can be delivered to a material surface by the kinetic energy of the charged ions impinging on the material. The extent to which ion-surface interactions can influence a material, during both deposition and etching, also depends on other factors such as the mass, reactivity, impingement rate (or flux) and dose (or net flux integrated over time) of ionic species incident on the film surface.[9,11–15] Furthermore, the concurrent arrival of energetic ions and reactive radicals at a surface has been reported in the literature to bring about synergistic ion-radical processes during both deposition and etching.[9,10,16] Although the effects of ion-surface interactions have been investigated in great detail for plasma-enhanced chemical and physical vapor deposition together with plasma-based dry etching processes, very limited studies have been conducted on the role of ions during PEALD. Building upon our previous work,[17,18] we recently demonstrated how the material properties of oxides and nitrides (of Ti, Hf and Si) grown using PEALD on planar and 3D substrates can be tailored by implementing RF substrate biasing in a remote plasma ALD system.[19,20] Specifically, an RF bias signal applied to the substrate table of the remote plasma system through a matching network (consisting of inductive and capacitive components)

induces a negative time-averaged bias voltage, $-\langle V_{bias} \rangle$, on the substrate. This increases the potential difference, and therefore, the electric field across the sheath region formed between the plasma and the substrate, which in turn accelerates ions toward the substrate in a direction perpendicular to its surface. As a result the energy brought to a growing film surface by the impinging ions can be controlled by means of RF substrate biasing. This technique was demonstrated to significantly enhance the versatility of PEALD processes by providing additional knobs – magnitude and duration of $\langle V_{bias} \rangle$ during plasma exposure – that enabled enhanced control over a wide range of material properties, relevant for numerous applications.[19] Based on these recent observations made in our previous work, it was concluded that controlling the magnitude of $\langle V_{bias} \rangle$ imparted ion energy control while varying the duration of $\langle V_{bias} \rangle$ during plasma exposure influenced the dose or fluence (i.e., particle flux integrated over time) of energetic ions impinging on a growing film.[19] While $\langle V_{bias} \rangle$ is an often known parameter given the relative ease with which it can be measured, the energy characteristic of ions also depends on the spatial and temporal variations of the electric field in the sheath region during RF substrate biasing. In order to better understand how any given PEALD process is influenced by ion-surface interactions, information on the energy and flux characteristics of ions impinging on a growing film surface under various plasma conditions is required. Such ion energy and flux characteristics are usually reported for plasma-based dry etching processes including the etch counterpart of PEALD, namely plasma-enhanced atomic layer etching (ALE) where so-called ALE windows have been identified for different materials as a function of the ion energy.[21–23]

In this work, we measured ion energy and flux characteristics of reactive plasmas typically used for PEALD (O_2, H_2, N_2) in order to investigate their role in tailoring material properties. An O_2 plasma is generally employed for depositing oxides, an H_2 plasma can typically act as the reducing agent for growing metallic elements or conductive compounds (e.g., transition metal nitrides and carbides) while an N_2 plasma can be used as the co-reactant for synthesizing nitrides.[8] Ion flux-energy distribution functions (IFEDFs) of these plasmas were measured in a commercial remote plasma ALD system equipped with RF substrate biasing that allows for processing large area (200 mm) substrates. The accuracy of the measured datasets were initially benchmarked for inert Ar plasma exposures without and with RF substrate biasing. The effect of varying operating conditions (source power, pressure) and substrate configurations (grounded or biased) on the ion energy and flux characteristics of the three reactive plasmas were also investigated. The properties of three materials having a dielectric or conductive nature – namely TiO_x, HfN_x and SiN_x – grown using the three reactive plasmas in this ALD system, without and with substrate biasing, were analyzed as a function of the ion energy and flux parameters derived from IFEDFs. The results obtained herein provide

experimental evidence for validating the conclusions made in our previous work (discussed above). The results of this work have also afforded a better understanding of the relation between energetic ion characteristics and the ensuing material properties, e.g., by providing energy maps of material properties in terms of the ion energy dose during PEALD. These findings can serve as practical guidelines for obtaining materials with the desired properties when growing nanoscale films using PEALD.

6.2 Experimental setup

A schematic of the experimental setup employing a remote plasma ALD system (Oxford Instruments FlexAL) is shown in Figure 1. The reactor consisted of a radio-frequency (RF) power supply (13.56 MHz, up to 600 W) connected to a water-cooled copper coil wrapped around a cylindrical alumina tube to generate an inductively coupled plasma (ICP). For the specific FlexAL configuration, an additional external RF power supply (13.56 MHz, up to 100 W) was connected to the reactor table that allowed for substrate biasing during plasma exposure. Both RF power sources were in phase with each other and connected to the system via automated matching units (AMUs) consisting of inductive and capacitive components. The FlexAL system provides a readout for $\langle V_{bias} \rangle$ when applying an RF bias signal during plasma exposure. Additionally, an oscilloscope was connected to the reactor table via a high-voltage probe, shown in Figure 1, from which sinusoidal RF bias voltage waveforms developing on the table could be measured. These oscilloscope measurements were used to independently verify $\langle V_{bias} \rangle$ readouts from the FlexAL system (within $\pm$ 5 V).). A base pressure in the reactor chamber of $\sim 10^{-6}$ Torr was obtained using a turbo pump. A butterfly valve in front of the turbo pump controlled the effective pumping speed and functioned as an automated pressure controller.

A commercial gridded retarding field energy analyzer (RFEA)[24–27] from Impedans Ltd. was placed on the reactor table for measuring IFEDFs during plasma exposures without and with substrate biasing. A schematic of the RFEA is shown in Figure 1. It consisted of a series of grids (G1, G2 and G3) located beneath an array of ion sampling orifices with total ion sampling area (A_{tot}) of about 19 mm^2 and terminated by a collector plate (Figure 1).[25,28,29] The ions entered the RFEA through the sampling orifices facing the plasma. The first grid, G1, was electrically connected to the body of the RFEA and therefore, floated at the potential of the reactor table. Grid G1 consisted of apertures with a diameter of about 25 μm which is less than the Debye length encountered in the plasma conditions of this work (> 100 μm),[26] thus preventing any plasma from extending inside the analyzer. The second grid, G2, was biased with a positive voltage sweep with respect to the potential at G1 to provide a retarding potential barrier, V_{G2}, for the incoming positive ions. V_{G2} was swept from the average potential of G1
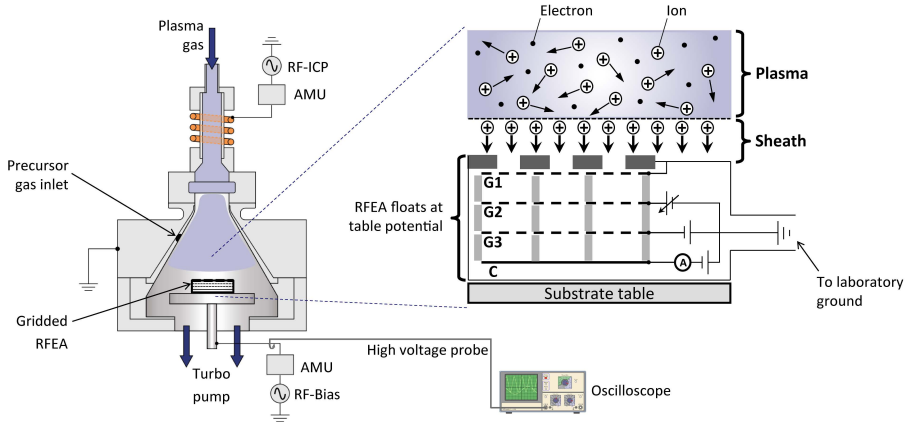
Figure 1. Schematic of an Oxford Instruments FlexAL system equipped with substrate biasing. A radio-frequency power supply (RF-ICP) acts as the remote inductively coupled plasma generator. A second RF power supply (RF-Bias) connected to the reactor table enables substrate biasing. Both RF power supplies are connected to the system via automated matching units (AMU) consisting of inductive and capacitive components. An oscilloscope connected to the reactor table via a high-voltage probe allowed measurement of voltage waveforms developing on the substrate and a gridded retarding field energy analyzer (RFEA) mounted on the substrate table allowed measurement of the flux-energy distribution function of ions (IFEDFs) impinging on the substrate. The magnified schematic on the right illustrates features of the plasma sheath formed between an electropositive plasma (consisting of positive ions and negative electrons as the charged species) and the substrate leading to a directional flux of accelerated positive ions on the RFEA. A cross-section of the RFEA illustrates three grids (G1, G2, G3) and a collector plate (C) on which fixed and varying potentials were applied to determine IFEDFs.

(corresponding to zero retarding potential) to about 50 V above plasma potential. At each step of the voltage sweep, only ions with energies greater than the energy barrier, eV_{G2}, formed at the discriminating grid G2 would be detected (e is the elementary charge constant). The third grid, G3, was biased about 60 V more negative than G1 to repel plasma electrons that may enter the RFEA and about 20 V more negative than the underlying collector plate. In other words, biasing the collector plate, C, 20 V more positive than G2 inhibits any secondary electrons that may be emitted from C. For each bias step applied to G2, the corresponding current at the collector plate, I_C, was recorded. This current arises from ions that initially pass through the sampling orifices before successively passing through the three layers of partially transmitting planar grids. Dividing I_C measured at the RFEA collector plate with an effective ion sampling area, A_{eff} (discussed below and in RFEA calibration section in Appendix 6), gives the ion current density at the collector, J_C, for each retarding voltage step applied to the discriminating grid G2 (i.e., $J_C = I_C/A_{eff}$). Taking the negative derivative of the J_C-V_{G2} characteristic measured using the RFEA results in the IFEDF. Note that RFEA measurements have been often reported in the literature using the term ion energy

distribution function (IEDF) although IFEDF is a more accurate representation of such measurements. Recently, several works have addressed this issue in nomenclature by using the term IFEDF instead of IEDF to represent RFEA measurements.[30–32] As such, this work also uses the term IFEDF to represent the measurements conducted using a RFEA (see section on Deriving IFEDF from J_C-V_{G2} measurements in Appendix 6).

The net transmission factor of the RFEA grid stack, T_G, is simply the proportion of incident ions at the entrance orifices that reach the collector plate after passing through all grids. The A_{eff} at the RFEA collector plate depends on the product of the aforementioned A_{tot} at the RFEA orifices and T_G (i.e., $A_{eff} = T_G.A_{tot}$ where $0 < T_G < 1$). Several methods have been reported in the literature to calibrate a RFEA in order to determine T_G and the associated A_{eff} at the underlying collector plate.[29,33–36] In this work, the RFEA was calibrated by comparing I_C measured at the RFEA collector with a reference ion current density, J_{CPP}, measured separately using a capacitive planar probe (CPP).[37] The calibration was performed for different plasmas at different operating conditions and yielded an A_{eff} of 0.39 ± 0.09 mm² at the RFEA collector plate (see Figure A6.1 and RFEA calibration section in Appendix 6). The relative measurement uncertainty of $\pm$ 23% arises from the calibration and includes the (non-systematic) measurement accuracy of the CPP. The A_{eff} at the collector expressed as a percentage of the A_{tot} at the entrance orifices yielded a T_G of about 2.1%. The aforementioned values for A_{eff}, its measurement uncertainty and T_G obtained from the calibration performed in this work were comparable to the corresponding values obtained from RFEA calibration reported in the literature (see RFEA calibration section in Appendix 6).[34] The values of J_C determined from the calibrated A_{eff} were used to derive parameters such as the ion flux, ion energy flux and kinetic energy dose of ions per unit substrate area per ALD cycle (discussed in the following section). The ion flux determined from the CPP calibrated J_C values obtained in our current work was comparable to the ion flux reported in our previous work measured in a similar FlexAL plasma ALD system under similar plasma conditions.[38] As a result, the uncertainty associated with the calibration technique implemented in this work was considered to be within acceptable limits. Furthermore, any systematic errors that were not included in the uncertainty but get incorporated in parameters derived using the calibrated J_C values were not expected to affect either the trends in material properties (as a function of the derived parameters), or the conclusions drawn on those trends.

When growing films in the FlexAL system using PEALD, the chamber wall temperature was set to 150 °C while the substrate table (or stage) temperature was set between 300 and 500 °C. All substrates underwent a thirty minute heating step prior to commencing deposition to ensure substrate temperature stabilization. The precursor

delivery lines were heated to 70 °C to prevent precursor condensation. TiO_x, HfN_x and SiN_x films were deposited using PEALD cycles composed of sequential precursor dose, precursor purge, plasma exposure (without or with substrate biasing) and plasma purge steps. The precursors, plasma gases and other PEALD process conditions for depositing the three materials are shown in Table 1, similar to that reported in our previous work.[19] Details regarding PEALD process conditions are further outlined in Appendix 6 and the step sequences implemented without and with substrate biasing are shown in Figure A6.2.

Table 1. PEALD process conditions for the materials deposited with and without substrate biasing during plasma exposure.

Material	TiO_x	HfN_x	SiN_x
Precursor	TDMAT[a]	TDMACpH[b]	DSBAS[c]
Bubbler temperature (°C)	60	60	40
Precursor delivery	Bubbled with 100 sccm Ar	Bubbled with 100 sccm Ar	Vapor drawn
Stage temperature (°C)	300	450	500
Precursor dose time (ms)	200	4000	500
Precursor reaction step (s)	-	-	3
Precursor purge time (s)	3	2	2
Plasma gas	O_2	H_2	N_2
Plasma gas flow (sccm)	100	100	100
Plasma pressure (mTorr)	9	30	11
RF-ICP power (W)	200	100	600
Plasma exposure time (s)	10	10	20
Plasma purge time (s)	3	4	3
$\langle V_{bias} \rangle$ or time-averaged substrate bias voltage (V)	0 to -254	0 to -210	0 to -103
Bias during plasma	All 10 s, Last 5 s	All 10 s	Last 10 s

[a] TDMAT – $Ti(NMe_2)_4$ [b] TDMACpH – $CpHf(NMe_2)_3$ [c] DSBAS – $SiH_3N(^sBu)_2$

6.3 Material property characterization

The substrates used for depositing films with and without substrate biasing were single side polished (SSP) c-Si (100) wafers having a thin native oxide layer (~1.5 nm) for dielectric materials and SSP c-Si (100) wafers having a thick thermal oxide layer (~450 nm) for conductive materials. Film thicknesses between ~20 and ~80 nm were

deposited for material characterization on these substrates. The optical properties and film thickness of the deposited layers on c-Si substrates were measured by means of spectroscopic ellipsometry (SE) using a J.A. Woollam M2000D rotating compensator ellipsometer (1.2 – 6.5 eV). For TiOx films deposited with and without substrate biasing, the optical model used consisted of a silicon substrate, ∼1.5 nm native oxide and the deposited layer parameterized using two Tauc-Lorentz oscillators.[18,39] For HfNx, different models were used for the films deposited with and without biasing, as reported previously by Karwal *et al*.[20,40] The optical model used for the films grown without biasing consisted of a silicon substrate, ∼450 nm thermal oxide and the deposited layer parameterized using one Drude, one Lorentz and one Tauc-Lorentz oscillator.[40] The HfNx films deposited with biasing were parameterized using one Drude and two Lorentz oscillators.[20] For SiNx films deposited with and without substrate biasing, the optical model used consisted of a silicon substrate, ∼1.5 nm native oxide and the deposited layer parameterized with a Cauchy dispersion relation.[41,42] The mass density of TiOx and SiNx films were analyzed using X-ray reflectometry (XRR) performed using a Bruker AXS D8 Advance system in the grazing incidence geometry with a Cu Kα x-ray source (radiation wavelength of 0.154 nm).[43] The residual stress of TiOx films were determined by means of wafer-curvature measurements at room temperature. A KLA-Tencor FLX 2320 system was used to determine the curvature of 3 inch double side polished (DSP) c-Si (100) wafers before and after deposition of the films. Based on the difference in curvature, the residual stress of the films deposited with and without substrate biasing was calculated using the Stoney equation.[18,43] A sign convention was used where positive values represented tensile and negative values represented compressive residual stress. The chemical composition and oxidation state of elements present in HfNx films were characterized using X-ray photoelectron spectroscopy (XPS). The XPS measurements were performed using a Thermoscientific K-Alpha KA1066 system equipped with a monochromatic Al Kα (hv = 1486.6 eV) source. The crystallinity of TiOx and HfNx films deposited on planar c-Si substrates was analyzed using grazing incidence x-ray diffraction (XRD). The measurements were performed in a PANalytical X'pert PRO MRD with a Cu Kα x-ray source (radiation wavelength of 0.154 nm) operated at an incidence angle of 0.5°. Electrical sheet resistance measurements of conductive HfNx films deposited on c-Si substrates with ∼450 nm thermal oxide were performed at room temperature using a Signatone four-point probe (FPP) in combination with a Keithley 2400 Source Measurement Unit (SMU) that acted as both current source and voltage meter. The electrical resistivity was obtained from the slope of the generated I-V curve and the film thickness deduced from the SE measurements. For investigating wet-etch rates of SiNx, the films were first deposited with and without substrate biasing during PEALD on coupons containing high aspect ratio trench nanostructures (width ∼100 nm, height ∼450 nm, AR = 4.5 : 1) and analyzed with cross-sectional transmission electron microscopy (TEM). Coupons containing these trench nanostructures were

prepared and provided by Lam Research.[42] A JEOL 2010F ultrahigh-resolution scanning TEM at 200 kV (Nanolab Technologies) was employed to obtain cross-sectional images of the deposited films. A detailed outline on sample preparation for TEM imaging has been outlined in our previous work.[19,42] The deposited film thickness was measured at planar and vertical regions of several trench nanostructures in the sample by counting pixels in the TEM image. To perform wet-etch treatments, coupons containing the trench nanostructures with the deposited films were dipped in a dilute hydrofluoric acid solution (HF : H_2O = 1 : 100) for 30 seconds. Two samples for TEM cross-sectional imaging were prepared from the same coupon, one before and one after the chemical wet-etch treatments. TEM measurements were conducted across several trench nanostructures of the same as-deposited and post wet-etch samples. The wet-etch rates were determined by comparing the as-deposited and post wet-etch film thicknesses on the trench nanostructures.

6.4 Results and discussion

6.4.1 Inert Ar plasma without & with RF substrate biasing

Figure 2a shows the IFEDF, $h_\Gamma(E_i)$, as a function of the ion kinetic energy, E_i, for an Ar plasma ignited at an ICP power, P_{ICP}, of 200 W and pressure of 9 mTorr for a grounded reactor table (i.e., without RF substrate biasing). The inset shows the J_C-V_{G2} characteristic from which the IFEDF was determined using

$$h_\Gamma(E_i) = -\frac{1}{e^2} \cdot \frac{\mathrm{d}J_C}{\mathrm{d}V_{G2}}$$

<div align="right">Eq. 1</div>

where e is the elementary charge constant. The E_i brought to a substrate by ions accelerated across a collisionless plasma sheath is determined by the sheath potential, ΔV_{sh}, which is the difference between the plasma potential, V_p, and the substrate potential, V_{sub}. These parameters are related by the following well-known expression

$$E_i = e\Delta V_{sh} = e(V_p - V_{sub})$$

<div align="right">Eq. 2</div>

The IFEDF consisted of a narrow mono-modal or single peaked feature which is a typical attribute of inductively coupled discharges exposed to a grounded substrate.[44–46] For a purely inductively coupled discharge over a grounded substrate, V_p is constant and V_{sub} = 0 V, resulting in the flux-energy distribution of ions impinging on the substrate to have a mono-modal feature around eV_p. For the practical inductive discharges over grounded substrates used in this work, the width of the mono-modal feature arises due to fluctuations in the plasma potential caused by parasitic capacitive coupling between the ICP coil and the discharge (in the absence of Faraday shielding), ion collisions in the
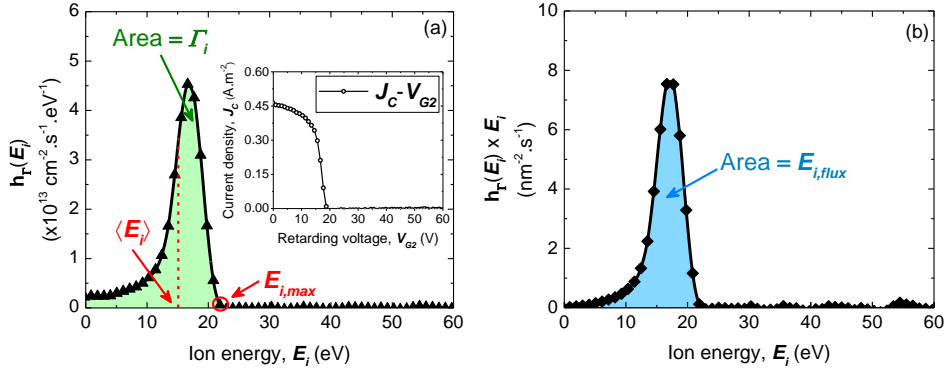
Figure 2. (a) Ion flux-energy distribution function (IFEDF), $\mathbf{h_\Gamma}(E_i)$, and **(b)** the product of the IFEDF and ion energy, $\mathbf{h_\Gamma}(E_i) \times E_i$, as a function of the ion kinetic energy, E_i, for an Ar plasma at an ICP power, P_{ICP}, of 200 W and pressure of 9 mTorr in case of a grounded substrate (i.e., without biasing). The inset in **(a)** shows the ion collector current density versus retarding grid voltage (J_C-V_{G2}) characteristic measured using the calibrated RFEA, the negative derivative of which yields $\mathbf{h_\Gamma}(E_i)$. The area under $\mathbf{h_\Gamma}(E_i)$ allows determination of the total ion flux, Γ_i, while the high energy peak edge corresponds to the maximum kinetic energy of ions, $E_{i,max}$, impinging on the grounded substrate. The area under $\mathbf{h_\Gamma}(E_i) \times E_i$ allows determination of the total ion energy flux, $E_{i,flux}$, while the ratio of $E_{i,flux}$ and Γ_i gives the mean ion energy, $\langle E_i \rangle$.

presheath and/or the energy resolution of the RFEA.[24,44–46] The low energy tail in the IFEDF in Figure 2a indicated that a relatively small number of Ar ions underwent collisions while traversing the plasma sheath. As such, the formation of a nearly collisionless sheath between the plasma and the grounded substrate can be assumed at the low pressure of 9 mTorr (discussed more below). The high energy edge of the IFEDF at about 20 eV corresponded to the maximum energy of ions, $E_{i,max}$, impinging on the grounded substrate (Figure 2a). The total flux of ions, Γ_i, impinging on the substrate is given by the area under the IFEDF[26,31,32] such that

$$\Gamma_i = \int_0^\infty \mathbf{h_\Gamma}(E_i)\, dE_i \qquad \text{Eq. 3}$$

which resulted in a Γ_i of about 3×10^{14} ions.cm^{-2}.s^{-1} for the grounded Ar plasma in Figure 2a. The mean energy of ions, $\langle E_i \rangle$ (Figure 2a), impinging on the grounded substrate can be determined from the ratio of the total ion kinetic energy flux, $E_{i,flux}$, and the Γ_i. The $E_{i,flux}$ can be obtained from a plot of the product of the IFEDF and the ion energy, i.e., $\mathbf{h_\Gamma}(E_i) \times E_i$, as a function of E_i shown in Figure 2b.[46] The area under $\mathbf{h_\Gamma}(E_i) \times E_i$ allows determination of the $E_{i,flux}$ such that[47,48]

$$E_{i,flux} = \int_0^\infty (\mathbf{h_\Gamma}(E_i) \times E_i)\, dE_i \qquad \text{Eq. 4}$$

For the inductive Ar plasma exposure on a grounded substrate shown in Figure 2, the $E_{i,flux}$ was about 44 eV.nm^{-2}.s^{-1}. Using Equation 3 and 4, the expression for $\langle E_i \rangle$ becomes[31,32,46]

$$\langle E_i \rangle = \frac{E_{i,flux}}{\Gamma_i} = \frac{\int_0^\infty (h_\Gamma(E_i) \times E_i)\, dE_i}{\int_0^\infty h_\Gamma(E_i)\, dE_i} \qquad \text{Eq. 5}$$

which yielded a $\langle E_i \rangle$ at around 15 eV in Figure 2a. The total ion kinetic energy dose imparted to the substrate by the impinging ions, $E_{i,dose}$, during plasma exposure can be obtained from the product of $E_{i,flux}$ and plasma exposure time, t_p, such that

$$E_{i,dose} = E_{i,flux} \times t_p \qquad \text{Eq. 6}$$

Therefore, a t_p of 10 s using an Ar plasma on a grounded substrate shown in Figure 2 yielded an $E_{i,dose}$ of about 440 eV.nm^{-2}.

When a sinusoidal RF voltage signal is applied to the substrate table through a matching network during plasma exposure, a negative average or DC offset voltage is induced on the substrate such that the net flux of ions and electrons impinging on it is zero over one RF cycle. The negative DC offset or time-averaged substrate bias voltage ($V_{sub} = -\langle V_{bias} \rangle$) can be increased by increasing the amplitude of the time-varying RF bias signal, $\tilde{V}_{RF,bias}$, applied to the substrate table. This can be visualized in Figure 3a which shows the RF bias voltage waveforms induced on the substrate in an Ar plasma as a function of time, measured using an oscilloscope (see also Figure A6.3 in Appendix 6). The oscillating waveforms were observed to have a time period, τ_{RF}, of about 74 ns, corresponding to the applied bias frequency of 13.56 MHz. $\langle V_{bias} \rangle$ can be controlled by varying the RF bias power, $P_{RF,bias}$, applied to the reactor table. This was observed in Figure 3b which shows $\langle V_{bias} \rangle$ as a function of $P_{RF,bias}$. The plot shows a deviation from an ideally linear trend suggesting that the applied $P_{RF,bias}$ was not dissipated entirely by accelerating ions across the plasma sheath. For remote ICP reactors employing RF substrate biasing, it has recently been reported that some of the bias power may be consumed in heating electrons near the substrate, which affects plasma density and consequently ion current.[49–52] This together with other effects such as power dissipation across resistive losses at the substrate or in the matching network can contribute to the non-linear trend in $\langle V_{bias} \rangle$ versus $P_{RF,bias}$.

A plot of Γ_i as a function of $P_{RF,bias}$ has also been shown in Figure 3b where a slight increase in Γ_i to 4.7×10^{14} ions.cm^{-2}.s^{-1} was observed on increasing $P_{RF,bias}$ to 20 W. Further increase in $P_{RF,bias}$ did not change Γ_i. The values of Γ_i have been determined using Equation 3 for IFEDFs obtained in the Ar plasma without and with RF substrate
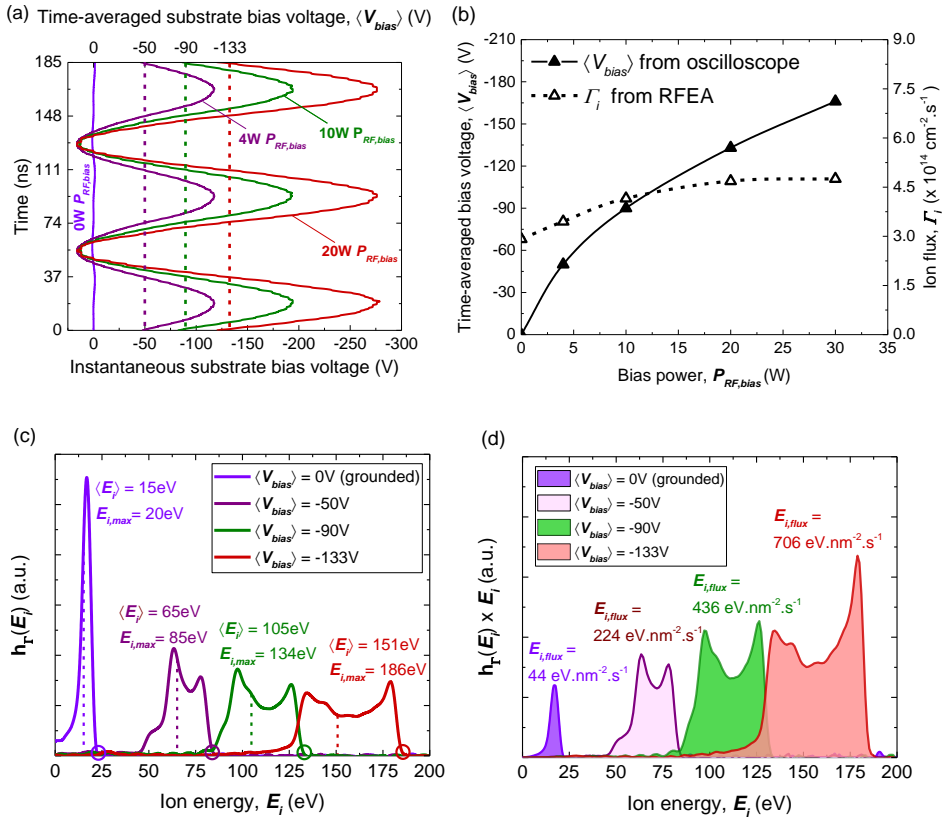
Figure 3. (a) Substrate voltage waveforms as a function of time measured using an oscilloscope in an Ar plasma at 200 W ICP power, P_{ICP}, and 9 mTorr pressure without (i.e., grounded) and with RF substrate biasing. It illustrates the development of instantaneous substrate bias voltages (bottom axis) and negative time-averaged substrate bias voltages, $\langle V_{bias} \rangle$, with respect to ground (top axis) for the corresponding RF bias powers, $P_{RF,bias}$. **(b)** $\langle V_{bias} \rangle$ and total ion flux, Γ_i, as a function of the applied $P_{RF,bias}$ where Γ_i was determined from measurements conducted using a calibrated retarding field energy analyzer (RFEA). **(c)** Ion flux-energy distribution function (IFEDF), $h_\Gamma(E_i)$, and **(d)** product of the IFEDF and ion energy, $h_\Gamma(E_i) \times E_i$, as a function of the ion kinetic energy, E_i, for the Ar plasma without and with RF substrate biasing measured using the calibrated RFEA. The mean ion energy, $\langle E_i \rangle$, maximum ion energy, $E_{i,max}$ and total ion energy flux, $E_{i,flux}$, for the corresponding $\langle V_{bias} \rangle$ are indicated.

biasing. Figure 3c shows the IFEDFs while Figure 3d shows the products of the IFEDFs and the corresponding ion energies for Ar plasma without and with RF substrate biasing. The narrow mono-modal distributions in the plots for a grounded substrate became broad bi-modal distributions with RF substrate biasing. They illustrate how $\langle E_i \rangle$, $E_{i,max}$ and $E_{i,flux}$ scale as a function of $\langle V_{bias} \rangle$ (see also Figure A6.4 in Appendix 6), which effectively demonstrates how E_i characteristics can be controlled by varying the

magnitude of $\langle V_{bias} \rangle$. The difference between $\langle E_i \rangle$ and $E_{i,max}$ was also observed to increase linearly with $\langle V_{bias} \rangle$. This was also observed for the case of reactive plasmas (discussed in following sections) which were studied to show how a growing film surface during PEALD with RF substrate biasing can get exposed to a range of ion energies that can significantly exceed $\langle E_i \rangle$. As a result, values for the $\langle E_i \rangle$ often calculated using Equation 2 with easily measurable values of $\langle V_{bias} \rangle$ may not be representative of the actual energies of ions impinging on a growing film surface. This serves to highlight the importance of measuring IFEDFs as they provide information beyond just the $\langle E_i \rangle$, which is essential for investigating the relation between energetic ion characteristics and the properties of materials grown with or without RF substrate biasing during PEALD (discussed in the following sections). The width of the bi-modal distributions in terms of the low and high energy peak separation, ΔE_{LP-HP}, is generally used in the literature as a means of quantifying the spread in the energy of ions impinging on the substrate. Various analytical models have been developed to measure ΔE_{LP-HP}. The model developed by Benoit-Cattin and Bernard[53] states that

$$\Delta E_{LP-HP} = \frac{4e\tilde{V}_{sh}}{\pi}\left(\frac{\tau_{RF}}{\tau_i}\right) \qquad \text{Eq. 7}$$

where $\tilde{V}_{sh}$ is the amplitude of the time-varying sheath voltage formed under RF biasing and is approximately given by $\tilde{V}_{RF,bias}$[25,26,54] (obtainable form oscilloscope measurements in Figure 3a), while τ_i is the ion transit time across the sheath.[55] Equation 7 states that the bi-modal IFEDFs become broader (i.e., ΔE_{LP-HP} increases) with increase in $\tilde{V}_{sh}$ and/or a decrease in τ_i. This was demonstrated in Figure 3c where ΔE_{LP-HP} can be inferred to scale with $\langle V_{bias} \rangle$, and hence with $\tilde{V}_{sh}$ (see also Figure A6.5 in Appendix 6), similar to the trend reported by Hayden et al.[25] Furthermore, no significant low energy tails were observed for the bi-modal IFEDFs in Figure 3c, which suggested that ions traversed the plasma sheaths formed with RF substrate biasing without undergoing significant ion-neutral charge-exchange collisions.[26,36] This was corroborated by calculating time-averaged sheath thicknesses, $\langle s \rangle$, for the investigated Ar plasmas using the expression for a collisionless Child-Langmuir sheath[55] where values of $\langle s \rangle$ up to 6 mm were obtained with RF substrate biasing (see Figure A6.6 and Equations A6.6 and A6.7 in Appendix 6). This indicated that the sheath thicknesses evolving as a function of $\langle V_{bias} \rangle$ were less than the ion mean free path ($\sim$8 mm for Ar plasma at $\sim$10 mTorr[26]), thereby confirming the formation of nearly collisionless plasma sheaths.

The values of ΔE_{LP-HP} measured in this work for an RF biased inductive Ar plasma were used to calculate τ_i using Equation 7. The magnitude of the calculated values of τ_i, ranging from $\sim$400 to $\sim$300 ns (see Figure A6.7 in Appendix 6), and the trend in those

values as a function of $\widetilde{V}_{sh}$ were comparable to those reported by Wen *et al.*[54] who used a Monte-Carlo model to calculate τ_i for an inductive Ar plasma at similar conditions. This indicated that the ion energy ($\langle E_i \rangle$, ΔE_{LP-HP}) and voltage ($\widetilde{V}_{sh}$, $\langle V_{bias} \rangle$) characteristics measured using the RFEA and oscilloscope, respectively, were of a reasonable accuracy.

6.4.2 Reactive plasmas for PEALD without & with RF substrate biasing

Materials synthesis with PEALD often makes use of gases such as O_2, H_2, N_2, etc. for generating reactive species in the plasma exposure step, which enable or contribute towards film growth. Although these gases are all diatomic molecules, the properties of the plasmas generated using these gases can be quite different owing to the difference in mass (32, 28 and 2 for O_2, N_2 and H_2 molecules), molecular dissociation energy (5.2, 9.8 and 4.5 eV for O=O, N≡N and H–H bonds),[56] ionization energy (12.1, 15.4 and 15.6 eV for creating O_2^+, N_2^+ and H_2^+ ions),[57] ion species composition, etc. For the pressures investigated in this work, diatomic O_2^+, N_2^+ and triatomic H_3^+ species have been reported to be the dominant ions in remote inductively coupled O_2, N_2 and H_2 plasmas, respectively.[36,58,59] The energy and flux of these ions generated in the respective plasmas will depend on all the aforementioned factors in a non-trivial manner, but are primarily determined by the plasma density, n_o, and the mean electron temperature, T_e. These two plasma properties are usually controlled by varying P_{ICP} and the discharge pressure. Therefore, the energy and flux characteristics of ions generated in remote inductively coupled O_2, H_2 and N_2 plasmas, without and with RF substrate biasing, have been investigated for different P_{ICP} and pressure conditions. Figure 4 and 5 show the IFEDFs obtained in O_2, H_2 and N_2 plasmas without and with RF substrate biasing during the respective plasma exposures. Figure 4 shows the effect of varying P_{ICP} (for a constant pressure) while Figure 5 illustrates the effect of a change in pressure (for the same P_{ICP}) as a function of $\langle V_{bias} \rangle$ induced on the substrate by the corresponding $P_{RF,bias}$ (a grounded substrate has been indicated by $\langle V_{bias} \rangle$ = 0 V for which $P_{RF,bias}$ = 0 W). Some common trends were observed for all three discharges without and with substrate biasing upon individually varying P_{ICP} and pressure which will first be presented. It will be followed by a discussion on trends that were more unique for the individual plasmas.

As observed previously for the case of Ar plasma, implementing substrate biasing during the three reactive plasmas led to the appearance of bi-modal features in the IFEDFs whose widths increased with $\langle V_{bias} \rangle$. At a constant pressure, the area under IFEDFs increased with increase in P_{ICP} (Figure 4). It is known that at higher P_{ICP}, more power is coupled into the plasma that increases the collision frequency between electrons and neutral plasma species resulting in a higher ionization rate.[38] This
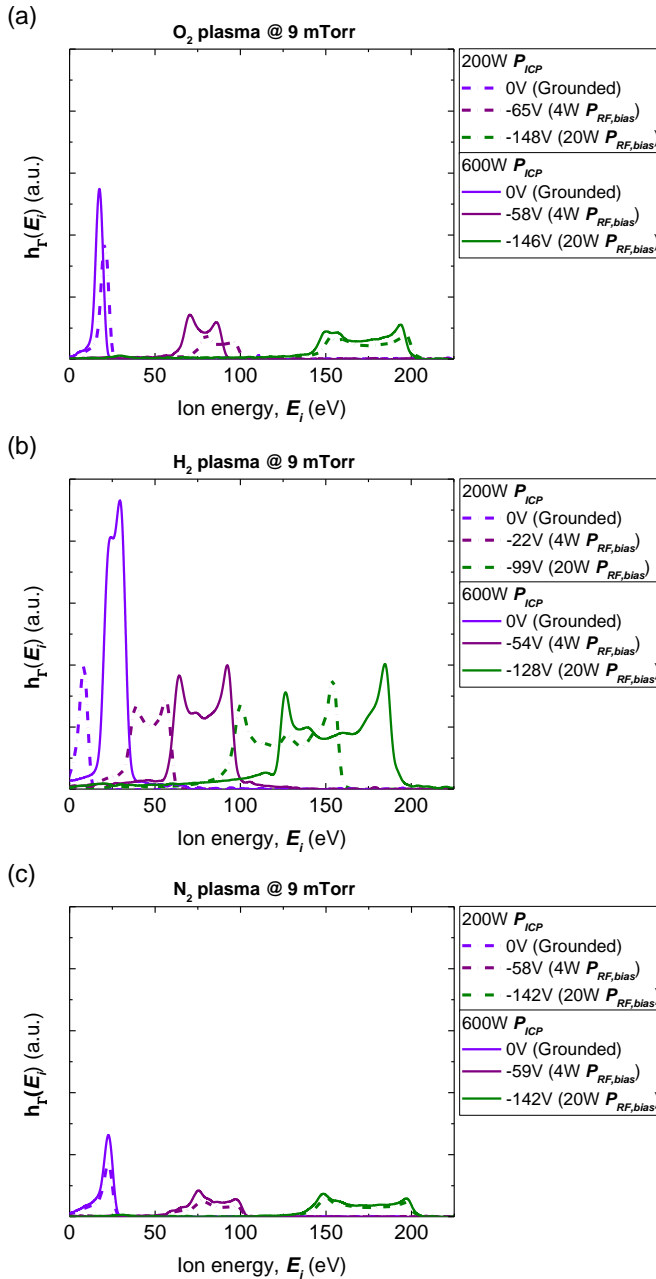
(a)

(b)

(c)

Figure 4. Effect of varying ICP power, P_{ICP}, on the ion flux-energy distribution functions, $\mathbf{h_\Gamma}(E_i)$, of **(a)** O_2, **(b)** H_2, and **(c)** N_2 plasmas with RF substrate biasing at a pressure of 9 mTorr. All plots have the same scale for the horizontal and vertical axes to facilitate comparison. The negative time-averaged substrate bias voltages formed by the applied RF bias powers are indicated in the legends.
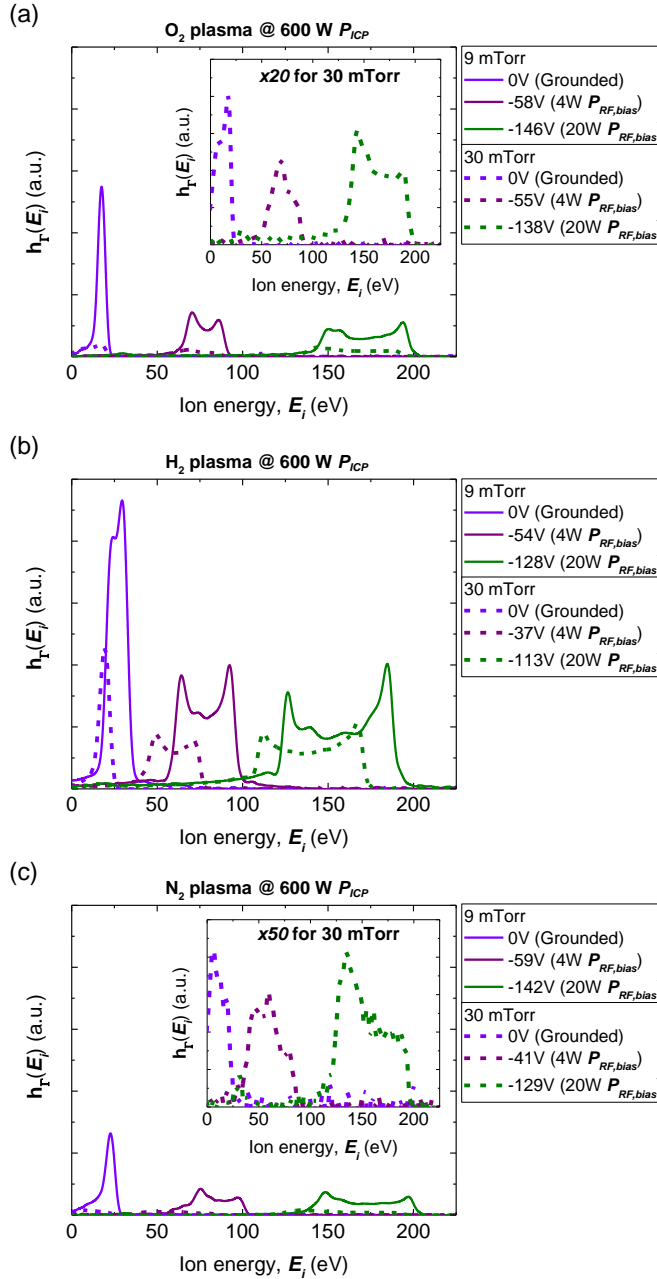
(a)

(b)

(c)

Figure 5. Effect of varying pressure on the ion flux-energy distribution functions, $\mathbf{h}_\Gamma(E_i)$, of **(a)** O_2, **(b)** H_2, and **(c)** N_2 plasmas with RF substrate biasing at an ICP power, P_{ICP}, of 600 W. All plots have the same scale for the horizontal and vertical axes to facilitate comparison. The insets in **(a)** and **(c)** depict $\mathbf{h}_\Gamma(E_i)$ for O_2 and N_2 plasma, respectively, at 30 mTorr with a scaled vertical axis for better illustration. The negative time-averaged substrate bias voltages formed by the applied RF bias powers are indicated in the legends.

increases n_o which leads to a higher Γ_i impinging on the substrate, thereby enhancing the area under IFEDFs (Equation 3 and Figure 4). Note that for H_2 plasmas, increasing P_{ICP} led to a much larger increase in the area under IFEDFs compared to O_2 or N_2 plasmas, which indicated significantly higher plasma densities at the higher P_{ICP} for H_2 plasmas. This could arise from the H_2 plasmas undergoing a transition from capacitive to inductive mode, also reported in the literature as the *E to H mode transition* which is a hallmark of ICP discharges.[60,61] A characteristic feature of this transition is the significant jump in n_o as P_{ICP} is increased from a low to a high value.[60,61] Furthermore, the IFEDFs of H_2 plasmas showed some other unique trends compared to O_2 or N_2 plasmas, which will be addressed at the end of this section. For a fixed P_{ICP}, increasing pressure led to a decrease in the area under IFEDFs, narrower IFEDF widths (i.e., lower ΔE_{LP-HP}), leftward shift of IFEDFs (i.e., lower $\langle E_i \rangle$, $E_{i,max}$) and a lower $\langle V_{bias} \rangle$ for the same $P_{RF,bias}$ (Figure 5). The n_o (and therefore Γ_i) has been reported to increase in a remote ICP system with a planar/spiral coil configuration when P_{ICP} is kept constant and the pressure is raised.[44,59] However, the spatial properties of plasma parameters in remote downstream ICP systems with an upper source chamber driven by a cylindrical coil configuration and a lower expansion chamber near the substrate can be quite complicated.[24,62–65] The substrate table, and hence the location at which RFEA measurements were conducted, lies at the end of the expansion chamber where n_o has been reported to decrease with pressure for a constant P_{ICP}.[38,62,63] This has been attributed to a reduced out-diffusion of charged particle species from the plasma source at elevated pressures that lowers Γ_i at the substrate,[38,62,63] which could explain the diminished areas under the IFEDFs. Furthermore, a reduced Γ_i induces a larger $\langle s \rangle$ which leads to a longer τ_i (see Equations A6.6, A6.7 and A6.8 in Appendix 6). The longer τ_i together with a lower $\widetilde{V}_{sh}$ (due to a lower $\langle V_{bias} \rangle$) could contribute towards the narrower widths (i.e., lower ΔE_{LP-HP}) observed for the IFEDFs. It is known that at higher pressures, the electron mean free path is reduced leading to more electron-neutral collisions and hence, a lower T_e.[29,66] As a result, ΔV_{sh} is lowered owing to the dependence of both V_p and $\langle V_{bias} \rangle$ on T_e[66] which can therefore, account for the shift in IFEDFs to lower $\langle E_i \rangle$ and $E_{i,max}$.

For O_2 plasma at a constant pressure, increasing P_{ICP} led to a slight shift of the IFEDFs to lower energies when the substrate was grounded or biased with a low $P_{RF,bias}$ of 4 W. This could be due to a lower T_e at the higher P_{ICP} condition as observed in previous work,[38] which could lead to a lower V_p.[8] However, the shift in IFEDF at the two P_{ICP} values decreased as the $P_{RF,bias}$ applied to the substrate was increased to 20 W. This suggested that the relatively small influence of P_{ICP} on V_p during O_2 plasmas diminished when the substrate was biased using high $P_{RF,bias}$, which may be speculated to arise from the previously mentioned electron heating effects in inductive discharges

with RF substrate biasing recently reported in the literature.[49–52] Further investigation is needed to better ascertain these effects which lies beyond the scope of this work. On the other hand, for H_2 plasma at a constant pressure, increasing P_{ICP} leads to wider IFEDFs together with a significant shift in IFEDFs to higher energies for both grounded and biased substrates compared to O_2 plasma. This could due to a combination of several possible factors discussed herein. The broader IFEDFs suggested an increase in $\widetilde{V}_{sh}$ and/or decrease in τ_i. As mentioned before, the IFEDF width in case of an inductively coupled plasma exposed to a grounded substrate can arise from parasitic capacitive coupling between the ICP coil and the discharge in the absence of electrostatic shielding.[36,58] Therefore, the plasma potential can have an oscillating RF component superimposed on it. The amplitude of this RF component can increase when the supplied power (i.e., P_{ICP}) was increased[58] from 200 to 600 W at a fixed pressure leading to an increase in $\widetilde{V}_{sh}$. Furthermore, for the pressures investigated in this work, H_2 plasmas are known to have an ion composition where H_3^+ has been reported to be the dominant ion.[36,58] The mass of H_3^+ is lower than that of ions generated in the other plasmas in this work. In addition, since the plasma densities in H_2 plasmas were observed to be significantly higher at 600 W P_{ICP}, thinner $\langle s \rangle$ could form over the substrate in H_2 plasmas compared to those formed in other plasmas. The combined effects of a thinner $\langle s \rangle$ and lower ion mass may therefore, lead to a comparatively lower τ_i (see Equation A6.8 in Appendix 6). The shift in IFEDFs to higher energies at a higher P_{ICP} suggested an increase in T_e, which is contrary to the trend for O_2 plasma as reported in our previous work.[38] Godyak *et al.*[67] have reported on the unusual increase in T_e with P_{ICP} at low pressure (1 and 10 mTorr) and attributed this to an increase in electron-electron collisions at the higher n_o obtained from increasing P_{ICP}. Similarly, the higher n_o of an H_2 plasma at 600 W P_{ICP} at the low pressure of 9 mTorr could allow for more electron-electron collisions resulting in the elevation of T_e with P_{ICP}. Another factor reported by different authors in the literature which could play a role at low pressure is gas heating by ion-neutral collisions during ion acceleration in the presheath by the plasma ambipolar potential.[67–72] This can lead to a lower gas density, which in turn can increase the electron mean free path and hence, T_e. Further investigation is required to verify these effects which lies beyond the scope of this work. In case of N_2 plasma at constant pressure, no comparable shifts in IFEDFs were observed with increase in P_{ICP}, which suggested that T_e was relatively unaffected by P_{ICP} in N_2 plasma.[73]

6.4.3 Role of ions on properties of materials grown without & with RF biasing

The effects of ion energy and flux characteristics on material properties of films deposited using PEALD without and with substrate biasing are discussed herein. Three

materials, namely TiO_x, HfN_x and SiN_x grown using reactive O_2, H_2 and N_2 plasmas, respectively, discussed in the previous section have been used as case studies.

i) Titanium oxide (TiO_x) grown with O_2 plasma: Table 2 compares the material properties of three TiO_x films deposited on planar substrates at 300 °C for two films grown without and one film grown with RF substrate biasing during the O_2 plasma exposure step of PEALD. An $\langle E_i \rangle$ of 19 eV was measured for both films deposited without biasing ($\langle V_{bias} \rangle$ = 0 V) and had a corresponding $E_{i,max}$ of 27 eV and $E_{i,flux}$ of 37 eV.nm^{-2}.s^{-1}. Keeping E_i constant at the grounded substrate configuration and increasing $E_{i,dose}$ from 380 to 4100 eV.nm^{-2} by increasing t_p from 10 to 108 s, respectively (as per Equation 6), led to a decrease in refractive index and mass density of TiO_x. Grazing incidence XRD patterns revealed that both films grown without any biasing had a crystalline composition consisting of predominantly anatase TiO_x (see Figure A6.8 in Appendix 6). This is similar to the observations reported by Schindler *et al.*[74] who obtained predominantly anatase TiO_x when the films were deposited with 60 and 180 s O_2 plasma exposure steps (without any biasing) in a remote PEALD system. However, when t_p was kept constant at 10 s and $E_{i,dose}$ was increased to 4290 eV.nm^{-2} by enhancing E_i with RF substrate biasing (-152 V $\langle V_{bias} \rangle$ applied for a bias duration of 10 s during the 10 s t_p) such that $\langle E_i \rangle$ reached 161 eV (Table 2), both refractive index and mass density increased in contrast to the trends discussed above. The XRD pattern for this biased condition revealed a mixed phase crystalline content consisting of anatase and rutile TiO_x (see also Figure A6.8 in Appendix 6). This is in agreement with the observations reported in our previous work for TiO_x deposited with substrate biasing where the higher refractive index and mass density were attributed to the presence of the denser rutile phase.[19] These results demonstrate how material properties of TiO_x respond differently to the $E_{i,dose}$ depending on whether it is controlled by enhancing E_i with RF substrate biasing, or increasing t_p without any biasing during O_2 plasma exposure. Similar effects have been reported in the literature where increasing E_i from 20 to 100 eV at a fixed incident flux ratio of ions to atoms had different effects on material properties compared to increasing the incident flux ratio of ions to atoms at a fixed E_i of 20 eV.[75,76]

    The results of this work indicated the presence of an E_i threshold at or above a lower limit of 27 eV given by $E_{i,max}$ measured for a grounded substrate in O_2 plasma, which the ions impinging on a growing TiO_x film must overcome to form the denser and more optically refractive rutile phase. This threshold generally refers to the energy barrier for displacing atoms from their equilibrium positions[66,77,78] and is proportional to the binding energy of the material, which is an average energy dependent on the specific position of material atoms (e.g., surface or bulk atom).[23] Typical values reported in the literature as thresholds for displacing surface atoms range from ~20 to ~50 eV.[66,77,78]

Table 2. Crystalline phase composition, refractive index and mass density of titanium oxide films deposited at a stage temperature of 300 °C without and with RF substrate biasing during O_2 plasma exposure ignited using 200 W ICP power and 9 mTorr. The time-averaged substrate bias voltage, $\langle V_{bias}\rangle$, plasma exposure time, t_p, bias duration during t_p, mean ion energy, $\langle E_i\rangle$, maximum ion energy, $E_{i,max}$, total ion energy flux, $E_{i,flux}$, and total ion energy dose per unit substrate area per ALD cycle, $E_{i,dose}$, for each film are indicated. Any associated measurement uncertainties are given in the first

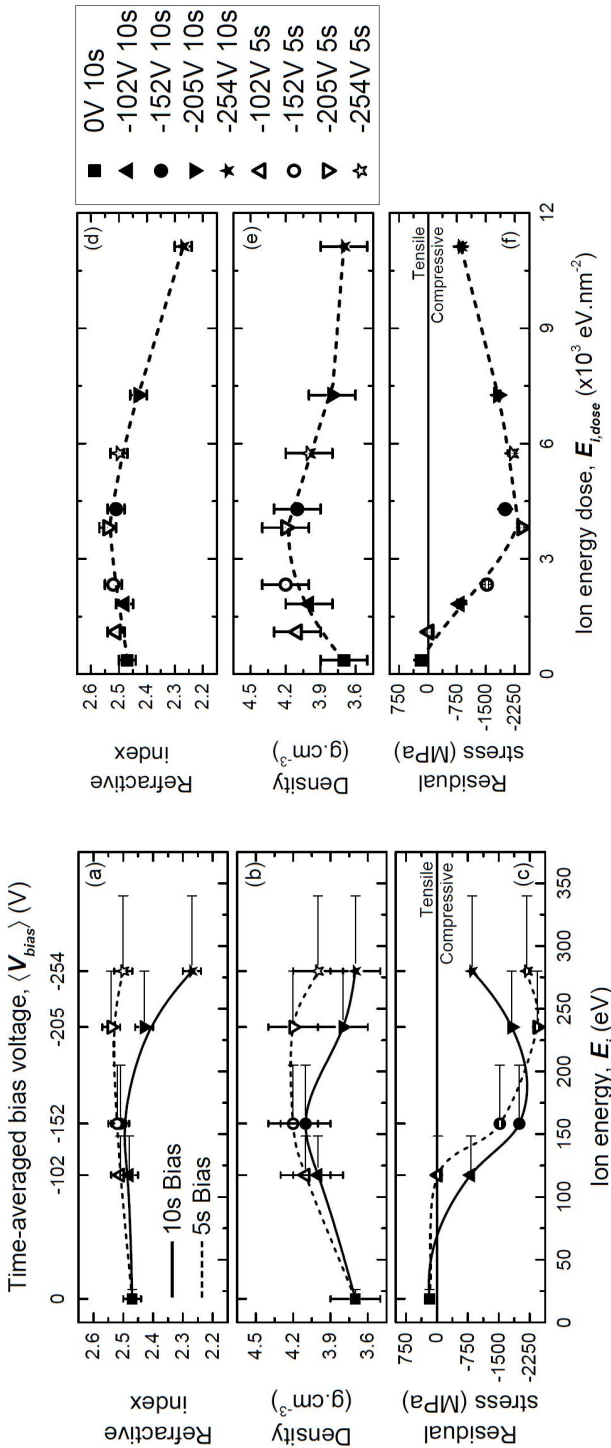| $\langle V_{bias}\rangle$ (V)	t_p (s)	Bias during t_p (s)	$\langle E_i\rangle$ (eV)	$E_{i,max}$ (eV)	$E_{i,flux}$ (eV.nm^{-2}.s^{-1})	$E_{i,dose}$ (eV.nm^{-2})	Crystal phase	Refractive index	Mass density (g.cm^{-3})
0	10	-	19	27	38	380	Anatase	2.47 ± 0.03	3.7 ± 0.2
0	108	-	19	27	38	4100	Anatase	2.39	3.3
-152	10	All 10	161	204	429	4290	Anatase + Rutile	2.51	4.1

Figure 6. (a) Refractive index, **(b)** mass density and **(c)** residual stress of titanium oxide films deposited at a stage temperature of 300 °C expressed as a function of the kinetic energy of ions, E_i, impinging on the substrate during O_2 plasma exposure using 200 W ICP power at a pressure of 9 mTorr. The solid square denotes film growth using an O_2 plasma exposure time, t_p, of 10 s without biasing while the rest of the symbols denote film growth with RF substrate bias spanning the entire duration (10 s, solid symbols) and last half (5 s, hollow symbols), respectively, of the t_p. Each non-square symbol denotes a particular mean ion kinetic energy, $\langle E_i \rangle$, for the corresponding negative time-averaged substrate bias voltage, $\langle V_{bias} \rangle$ during the O_2 plasma step. The horizontal bars represent the range of E_i between $\langle E_i \rangle$ and maximum ion energy, $E_{i,max}$, that a substrate is exposed to for the corresponding $\langle V_{bias} \rangle$. **(d)** Refractive index, **(e)** mass density and **(f)** residual stress of the same films expressed as a function of the total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, during O_2 plasma exposure without and with RF substrate biasing. The symbols represent the same parameters as before (indicated in the legend). All the lines serve as a guide to the eye.

The corresponding values typically reported for displacing sub-surface (or bulk) atoms lie between ~40 and ~100 eV since they have a comparatively higher coordination number and are therefore, more strongly bound than surface atoms.[77–79]

When E_i lies above atom displacement thresholds, ions impinging on a target material are known to transfer their energy by interacting with the nuclei and electrons of the material.[9,77,78] For E_i up to ~1 keV and comparable masses of incident ions and target material atoms, energy transfer has been reported to occur predominantly through elastic nuclear interactions.[9,15,77] Inelastic electronic interactions become significant for $E_i \gg 1$ keV and for a large mass difference between the impinging ions and target material atoms.[15,77,80] In this regard, for E_i up to a few hundred eV obtained for oxygen ions impinging on TiO$_x$ with substrate biasing, energy transfer could be considered to occur mainly through elastic nuclear interactions. Such interactions can initiate collision cascades through so-called recoil implantatation (i.e., forward sputtering of knock-on atoms generated by ion-surface interactions) and/or incident ion implantation,[77,81,82] which leads to atomic scale heating.[83] Therefore, the cascades represent a localized volume of material at a high temperature (i.e., *hot spot*)[82,84] where atoms are simultaneously in motion and undergo collisions that can break and reform bonds in the surface and sub-surface regions of the material undergoing ion bombardment.[66,77] The mobile atoms continue to undergo further collisions until their energy drops below the thresholds needed to displace other atoms from their equilibrium positions, at which point the remaining energy gets dissipated as thermal vibrations.[82,83] The anatase to rutile phase transformation of TiO$_x$ has been reported in the literature to be a reconstructive process involving the breaking and reforming of bonds, in contrast to other phase transformation processes where the original bonds are distorted but retained without being broken.[85] In this regard, the ions impinging on a growing TiO$_x$ film surface during O$_2$ plasma exposure could provide the energy needed to break and reform bonds as long as E_i lies above the thresholds for displacing atoms.

An alternative view could be that the local temperature spike induced by energetic ion-surface interactions enhance surface and bulk atom diffusion processes by mimicking high temperature deposition environments generally required to form rutile TiO$_x$.[77,82] Furthermore, it has been reported that when impinging ions originate from a reactive plasma (e.g., O$_2$ plasma), additional processes can occur simultaneously whereby reactive plasma radicals (e.g., O atoms) can diffuse to the surface and chemisorb at dangling bonds formed at the surface by the incident energetic ions.[16] The concurrent arrival of energetic ions and radical species at a surface during either material etching or deposition has been reported in the literature to lead to synergistic ion-radical processes.[9,10,16] Such processes typically consist of physical momentum transfer and chemical reaction components that yield unique characteristics, e.g.,

significantly enhanced etch rates during Si etching or the interplay between sp^2 and sp^3 bonds during a-C:H deposition.[9,10,16,86] In this regard, synergistic ion-radical processes during O_2 plasma exposure with substrate biasing could play a role in the anatase to rutile phase transformation of TiO_x obtained in this and previous work by PEALD.[17–19]

Figure 6a-c shows TiO_x material properties – refractive index, mass density and residual stress – as a function of E_i given in terms of $\langle E_i \rangle$ and $E_{i,max}$ obtained for the corresponding $\langle V_{bias} \rangle$ applied during plasma exposure. Although ΔE_{LP-HP} is generally used in the literature as an indicator for the spread in E_i delivered to a substrate by the impinging ions, Figure 6a illustrates how the spread can also be inferred from the difference between $E_{i,max}$ and $\langle E_i \rangle$. The horizontal bars in Figure 6a indicate that the substrate was exposed to a range of E_i between $\langle E_i \rangle$ and $E_{i,max}$ that widens with increase in the corresponding $\langle V_{bias} \rangle$, as discussed in the previous section. It highlights the importance of measuring IFEDFs that reveal how the actual E_i delivered to a growing material can be greater than the $\langle E_i \rangle$ and also allows determination of energy maps during deposition (see below). In our previous work, it was observed that the same $\langle V_{bias} \rangle$ applied for a different duration (or duty cycle) during t_p induced differences in the variation of material properties for TiO_x grown using PEALD with RF substrate biasing.[19] On the basis of these results, it was suggested that varying the duration of $\langle V_{bias} \rangle$ during plasma exposure can lead to a change in the dose or fluence (i.e., particle flux integrated over time) of energetic ions impinging on a growing film. This was concluded to provide an additional route for tailoring material properties besides varying the magnitude of $\langle V_{bias} \rangle$ to control the E_i delivered to a growing film.[19]

Figure 6a and b show that $\langle V_{bias} \rangle$ applied for the entire duration of the 10 s t_p causes the refractive index and mass density of TiO_x to demonstrate a two-stage behavior as a function of E_i: initial rise to a peak at $\langle E_i \rangle$ of 161 eV followed by a gradual fall with further increase in $\langle E_i \rangle$. When $\langle V_{bias} \rangle$ was applied for a duration of 5 s in the last half of the 10 s t_p, a similar behavior was observed for the refractive index and mass density but with peaks at a higher $\langle E_i \rangle$ of 230 eV. A parallel trend was observed for the residual stress of the films in Figure 6c. The stress changed from tensile to compressive on applying $\langle V_{bias} \rangle$ with a peak in compressive stress at $\langle E_i \rangle$ of 161 eV and 230 eV for bias durations of 10 s and 5 s, respectively, during the t_p of 10 s. The shift in peak positions suggested that when TiO_x was deposited with RF substrate biasing where E_i exceeded the atom displacement thresholds (i.e., $E_i >$ lower limit of 27 eV $E_{i,max}$ for a grounded substrate), the resulting material properties were influenced by several factors. These include the magnitude of E_i and the duration for which E_i was enhanced with RF substrate biasing during t_p. Figure 6d-f shows the three aforementioned TiO_x properties as a function of $E_{i,dose}$ during plasma exposure with $\langle V_{bias} \rangle$ spanning the

entire duration and last half (5 s) of the 10 s t_p. This plot also shows a similar two-stage behavior of the refractive index, mass density and compressive stress of TiO$_x$ films with a peak occurring at an $E_{i,dose}$ of ~3800 eV.nm^{-2}. It effectively demonstrates how the material properties of TiO$_x$ films become a function of both E_i and the bias duration during t_p when E_i is enhanced beyond the atom displacement thresholds (i.e., $E_i >$ at least 27 eV) with RF substrate biasing.

The results shown in Figure 6d-f validate the conclusions derived in our previous work where controlling the dose of energetic ions during PEALD with RF substrate biasing was suggested as an additional route (besides controlling ion energies) for tuning material properties.[19] A similar relation was reported recently for the etch counterpart of ALD employing energetic and directional ion bombardment, namely anisotropic ALE.[22,87] Berry *et al.*[22] reported that the rate of material removal during anisotropic plasma ALE becomes a function of both the ion energy and the duration of energetic ion exposure (hence, the ion energy dose) when the ion energy lies above the threshold for surface atom displacement. Note that Berry *et al.*[22] employed an inert Ar plasma with substrate biasing to remove target materials, where energetic inert ions created volatile etch products through purely physical momentum transfer. In contrast, this work utilized a reactive O$_2$ plasma with substrate biasing to deposit TiO$_x$, where energetic ions and reactive radicals created stable (or non-volatile) deposition products through both physical momentum transfer and chemical reaction components (discussed above). The results of this work signify that thresholds related to material atom displacement are parameters relevant not only for plasma ALE,[23,87] but also for plasma ALD carried out under the influence of energetic ions.

Figure 6d-f can also be interpreted as an energy map of TiO$_x$ properties in terms of the $E_{i,dose}$ during PEALD when E_i is enhanced beyond atom displacement thresholds (of at least 27 eV) with RF substrate biasing. An $E_{i,dose}$ of ~3800 eV.nm^{-2} obtained with RF substrate biasing serves as a transition point between regimes that yield different trends in material properties as a function of $E_{i,dose}$. The first $E_{i,dose}$ regime consisted of an increase in refractive index and mass density together with a change in crystalline composition from a predominantly anatase to a mixed anatase and rutile phase, which could be due to the formation of the denser rutile phase with substrate biasing as discussed above. This regime also showed a change in the residual stress from tensile to compressive. This was attributed to the formation of oxygen rich TiO$_x$ films (O/Ti ratio > 2) with substrate biasing in our previous work,[19] where the excess oxygen could be present as interstitial species that induce compressive stress.[81,88,89] The second $E_{i,dose}$ regime yielded a decrease in refractive index and mass density together with compressive stress relaxation. This was attributed to the incorporation of voids in the film microstructure and amorphization in our previous work,[19] together with the onset

of plastic deformation that could take place under highly energetic ion bombardment.[15,81,90] The results shown in Figure 6d-f (and in Figure 7a-c and Figure 8a-c in the next sections) illustrate how an energy map of material properties in terms of the $E_{i,dose}$ during PEALD can serve as a basis for growing nanoscale films with the desired material properties.

ii) Hafnium nitride (HfN$_x$) grown with H$_2$ plasma: Figure 7 shows an energy map of HfN$_x$ material properties,[20,40] that includes the resistivity, Hf^{3+} fraction and oxygen content, in terms of the $E_{i,dose}$ during PEALD at 450 °C without and with $\langle V_{bias} \rangle$ during H$_2$ plasma exposure. For the two films deposited without biasing ($\langle V_{bias} \rangle$ = 0 V), an $\langle E_i \rangle$ of 20 eV was measured together with a corresponding $E_{i,max}$ of 28 eV and $E_{i,flux}$ of 10 eV.nm^{-2}.s^{-1}. For a fixed E_i at the grounded substrate configuration, increasing $E_{i,dose}$ from ~600 to ~1800 eV.nm^{-2} by a three-fold increase in t_p from 10 to 30 s, respectively, led to a very small decrease in resistivity that essentially remained in the same order of magnitude. It was accompanied by a decrease in the Hf^{3+} fraction (by 0.06 $\pm$ 0.02) and an elevation in the film oxygen content (by about 5.0 $\pm$ 0.7 at. %). Grazing incidence XRD patterns for these films revealed peaks corresponding to cubic hafnium oxynitride, or Hf$_2$ON$_2$ (see Figure A6.9 in Appendix 6) confirming the presence of the high oxygen impurity content measured in these two films. This was attributed to the incorporation of oxygen in the film mainly during deposition due to background water present in the ~10^{-6} Torr vacuum environment of the PEALD system, as addressed in previous work conducted by Karwal *et al.*[40]

However, when t_p was kept constant at 10 s and $E_{i,dose}$ was increased to ~7400 eV.nm^{-2} by increasing E_i with RF substrate biasing (-95 V $\langle V_{bias} \rangle$ applied for a 10 s t_{bias}, during a 10 s H$_2$ t_p) such that $\langle E_i \rangle$ reached 109 eV, a drastic reduction of the film resistivity by about two orders of magnitude was observed (Figure 7a). This was accompanied by a significant increase in Hf^{3+} fraction (by about 0.20 $\pm$ 0.02, Figure 7b) and decrease in the film oxygen content (by about 8.0 $\pm$ 0.7 at. %, Figure 7c). Note that the change in the Hf^{3+} fraction and film oxygen content on increasing $E_{i,dose}$ through an increase in E_i with RF substrate biasing (at a constant t_p) was the exact opposite of the trends observed upon increasing $E_{i,dose}$ through an increase in t_p (at constant E_i for a grounded substrate). Increasing $E_{i,dose}$ by enhancing E_i with RF substrate biasing led to a two-stage behavior in resistivity and Hf^{3+} fraction, concurrent with the trends reported in previous work as a function of $\langle V_{bias} \rangle$.[20] The resistivity decreased to a minimum and Hf^{3+} fraction reached a peak at an $E_{i,dose}$ of ~12×10^3 eV.nm^{-2}. The film oxygen content, however, showed a monotonic decrease to levels below the instrument detection limit (< 2 at. %) as $E_{i,dose}$ was enhanced by means of RF substrate biasing. XRD patterns of the films deposited with biasing revealed peaks corresponding to face-centered-cubic
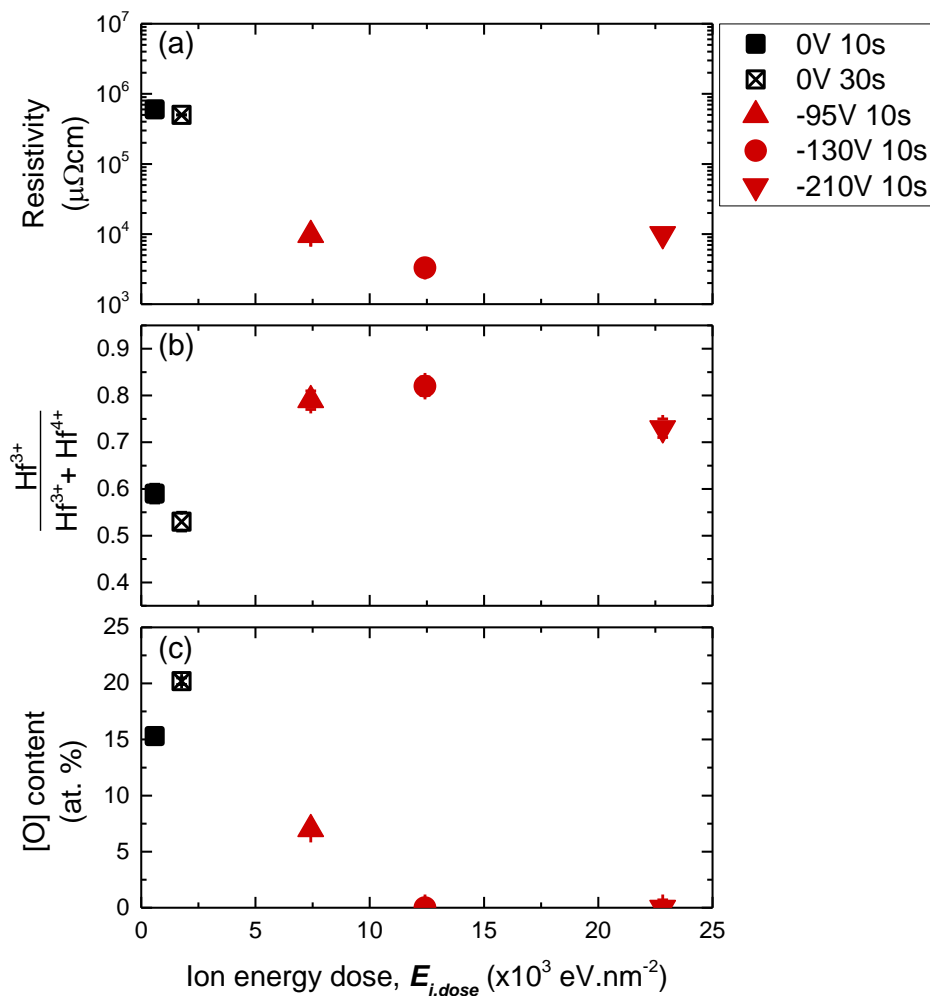
Figure 7. **(a)** Resistivity, **(b)** Hf^{3+} fraction, and **(c)** oxygen content of hafnium nitride films deposited at a stage temperature of 450 °C expressed as a function of the total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, during H_2 plasma exposure using 100 W ICP power at a pressure of 30 mTorr. The solid and crossed squares denote film growth using a plasma exposure time, t_p, of 10 s and 30 s, respectively, without any biasing while the rest of the symbols denote time-averaged substrate bias voltages, $\langle V_{bias} \rangle$, applied for the entire t_p of 10 s. Each non-square symbol denotes a particular $\langle V_{bias} \rangle$.

hafnium mononitride (see Figure A6.9 in Appendix 6).[20] As outlined in previous work reported by Karwal *et al.,*[20] the significant drop in resistivity and corresponding jump in Hf^{3+} fraction with RF substrate biasing could arise from the drastic reduction in film oxygen content. It could also contribute toward the formation of the more conductive face-centered-cubic hafnium mononitride films. Increasing $E_{i,dose}$ beyond $\sim 12 \times 10^3$ eV.nm^{-2} by enhancing E_i with RF substrate biasing led to a comparatively small increase in resistivity and a similar decline of the Hf^{3+} fraction. The was speculated to arise from an increase in film hydrogen content and associated Hf–H bonds for $\langle V_{bias} \rangle$ beyond -130 V, as explained in previous work reported by Karwal *et al.*[20]

Similar to the case of TiO$_x$, these results demonstrate how the material properties of HfN$_x$ deposited using an H$_2$ plasma respond differently to the $E_{i,dose}$ depending on whether it is controlled by enhancing E_i with RF substrate biasing, or increasing t_p without any biasing during plasma exposure. They again indicated the presence of an E_i threshold at or above a lower limit of 28 eV given by $E_{i,max}$ measured for a grounded substrate in H$_2$ plasma, which the ions impinging on a growing HfN$_x$ film surface must exceed to form highly conductive and oxygen impurity free hafnium mononitride. The results also allow identification of regimes characterized by different trends in material properties (resistivity and Hf^{3+} fraction) as a function of increasing $E_{i,dose}$ obtained by enhancing E_i beyond (at least) 28 eV with RF substrate biasing. The transition point between regimes could be considered to lie in the vicinity of the aforementioned $E_{i,dose}$ value of $\sim 12 \times 10^3$ eV.nm^{-2} (Figure 7). For the case of TiO$_x$, the thresholds were speculated to be related to synergistic oxygen based ion-radical processes involving both physical momentum transfer and chemical reaction components. The thresholds involving synergistic hydrogen based ion-radical processes are bound to be related primarily to the chemical reaction component and associated activation energy barrier involving removal of oxygen species from a hafnium oxynitride surface. This arises from the significantly lower mass of hydrogen plasma species that leads to a large mass difference between the incident hydrogen ions and target hafnium oxynitride atoms. As discussed previously, this renders physical momentum transfer processes through elastic nuclear interactions[15,78,80] highly unlikely. Based on recent experimental investigations reported in the literature,[91–93] the kinetic energy of the lighter hydrogen ions impinging on the significantly heavier hafnium oxynitride atoms is quite likely transferred through inelastic electronic interactions.[15,77,80] Energy transfer through such interactions do not contribute to physical displacement of hafnium oxynitride atoms but could play a role in facilitating chemical reactions between the oxygen species at the film surface and the concurrently arriving hydrogen plasma radicals. Chemical reactions activated by such ion-induced processes could remove oxygen species from the hafnium oxynitride surface, which eventually leads to the formation of hafnium mononitride. The

exact nature and mechanisms of these processes that induce changes in material composition and associated properties are currently being investigated on the basis of theoretical modelling and will be reported in a subsequent publication.[94]

iii) Silicon nitride (SiNₓ) grown with N₂ plasma: Figure 8 shows an energy map of SiN$_x$ material properties,[42] that includes the refractive index, mass density and wet-etch rate (WER), in terms of the $E_{i,dose}$ during PEALD at 500 °C without and with $\langle V_{bias} \rangle$ during N$_2$ plasma exposure. An $\langle E_i \rangle$ of 19 eV was measured for the two films deposited without any biasing ($\langle V_{bias} \rangle$ = 0 V) together with a corresponding $E_{i,max}$ of 29 eV and $E_{i,flux}$ of 35 eV.nm^{-2}.s^{-1}. For a fixed E_i at the grounded substrate configuration, increasing $E_{i,dose}$ from ~700 to ~2800 eV.nm^{-2} by a four-fold increase in t_p from 20 to 80 s did not cause any significant change in refractive index and WER while the mass density increased slightly by 0.1 g.cm^{-3}. The high refractive index and mass density of these two films confer excellent wet-etch resistance in dilute hydrofluoric acid. This accounts for the insignificant WER values of 0 ± 1 nm.min^{-1} measured at planar surface regions of films deposited on 3D trench nanostructures (see Figure A6.10 in Appendix 6).

However, when t_p was kept constant at 20 s and $E_{i,dose}$ was increased to ~2600 eV.nm^{-2} by increasing E_i with RF substrate biasing (-94 V $\langle V_{bias} \rangle$ applied for the last 10 s of a 20 s N$_2$ t_p) such that $\langle E_i \rangle$ reached 113 eV, a monotonic decrease was observed in refractive index and mass density. This was accompanied by a drastic increase in WER to about 36 ± 1 nm.min^{-1}. These results again indicated the presence of an E_i threshold at around 29 eV given by $E_{i,max}$ measured for a grounded substrate in N$_2$ plasma. The data suggests that ions impinging on a growing SiN$_x$ film during N$_2$ plasma exposure should not exceed this threshold if the aim is to form a dense and wet-etch resistant material. The monotonic trends in material properties of SiN$_x$ on increasing $E_{i,dose}$ by increasing E_i with RF substrate biasing were unlike the two-stage trends observed previously for TiO$_x$ and HfN$_x$. In those cases, material properties improved on increasing $E_{i,dose}$ up to a certain level with RF substrate biasing before being degraded, whereas SiN$_x$ degraded instantly on increasing $E_{i,dose}$ with biasing. Changes in other properties of SiN$_x$ due to energetic ion bombardment during N$_2$ plasma exposure reported in our previous work include formation of nitrogen rich films (N/Si ratio > 1.33) together with a significant increase in the film oxygen and carbon impurity content.[19] The excess nitrogen could be speculated to get incorporated as N–N bonds[95] in the material and/or N$_2$ gas bubbles,[15,96] as reported in the literature for films subjected to energetic ion bombardment. The film impurity content could be incorporated from species of dissociated ligand fragments and background impurities formed during plasma exposure. This was reported as the redeposition effect by Knoops *et al.*[97] for PEALD of SiN$_x$ using a Si precursor with two amino ligands (BTBAS). Although using DSBAS was
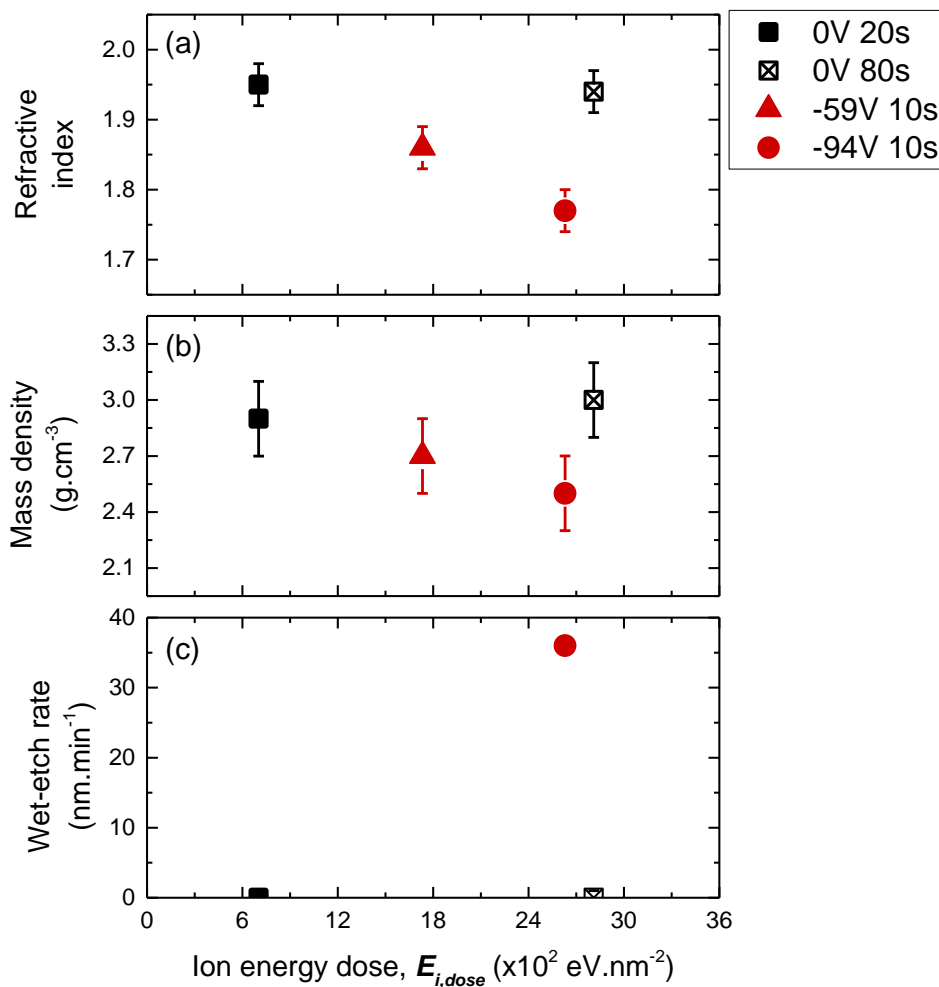
Figure 8. (a) Refractive index **(b)** mass density and **(c)** wet-etch rate of silicon nitride films deposited at a stage temperature of 500 °C expressed as a function of the total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, during N_2 plasma exposure using 600 W ICP power at a pressure of 12 mTorr. The solid and crossed squares denote film growth using a plasma exposure time, t_p, of 20 s and 80 s, respectively, without any biasing while the rest of the symbols denote time-averaged substrate bias voltages, $\langle V_{bias} \rangle$, applied for the last half (10 s) of the 20 s t_p. Each non-square symbol denotes a particular $\langle V_{bias} \rangle$.

shown to lower the redeposition effect in our previous work owing to it having one less amino ligand,[42] ionized species of dissociated ligand fragments formed in the plasma step can impinge on a growing film surface with a higher E_i when implementing RF substrate biasing. These factors could contribute towards degrading SiN_x by decreasing its refractive index, density and wet-etch resistance. An analogous decrease in etch resistance was recently reported for SiN_x films having a low density and high impurity content formed upon treatment with energetic helium and/or hydrogen ions.[95,98,99] Similar to the case of TiO_x and HfN_x, these results demonstrate how the properties of SiN_x films deposited using N_2 plasma behave differently as a function of the $E_{i,dose}$ depending on whether it is controlled by enhancing E_i with RF substrate biasing, or increasing t_p without any biasing during plasma exposure. They suggest that N_2 plasma exposure on a grounded substrate yields optimum SiN_x material properties as long as $E_{i,dose}$ is not enhanced with substrate biasing (i.e., $E_i < 29$ eV $E_{i,max}$ for a grounded substrate), which would otherwise induce degradation of those properties.

6.5 Conclusions

Ion flux-energy distributions functions (IFEDFs) of reactive O_2, H_2 and N_2 plasmas were measured using a gridded RFEA in a commercial 200-mm remote plasma ALD system without and with RF substrate biasing. These measurements were used to derive ion energy and flux characteristics to investigate their role in tuning the properties of films deposited by PEALD using the aforementioned plasmas. The properties of three materials having a dielectric or conductive nature – namely TiO_x, HfN_x and SiN_x – were analyzed as a function of the ion energy and flux parameters derived from IFEDFs measured for the reactive plasmas on grounded and RF biased substrates. Material properties were investigated in terms of the total ion kinetic energy dose imparted to a growing film in every plasma ALD cycle ($E_{i,dose}$), which was determined from the product of the mean ion kinetic energy, the total ion flux and the plasma exposure time. The properties were found to behave differently as a function of the $E_{i,dose}$ depending on whether it was controlled by enhancing the ion kinetic energy (E_i) with RF substrate biasing, or increasing the plasma exposure time (t_p) without any biasing. This showed that material properties during plasma ALD were influenced by whether E_i lied within or beyond certain energy thresholds. These are related to energy barriers involving physical displacement of material atoms or activation of an ion-induced chemical reaction component. A lower limit for these energy thresholds was obtained (at ~30 eV) from the maximum E_i measured in the IFEDFs for grounded substrates. When a grounded substrate was used in the plasma exposure step, E_i delivered to a growing film by the impinging ions was observed to lie below the aforementioned E_i thresholds. For this substrate configuration, increasing $E_{i,dose}$ by increasing t_p at a constant E_i

resulted in a) TiO$_x$ films remaining in the anatase phase with a comparatively low density and refractive index, b) HfN$_x$ films with higher oxygen impurity content and lower Hf^{3+} fraction while their resistivity remained comparatively unchanged, c) SiN$_x$ films retaining high refractive indices and mass densities with negligible wet-etch rates.

For RF biased substrates during plasma exposure, E_i can exceed the energy thresholds for physically relocating material atoms or for activating ion-induced chemical reactions. Increasing $E_{i,dose}$ by increasing E_i with RF biasing at constant t_p yielded a two-stage behavior in TiO$_x$ and HfN$_x$ material properties while those of SiN$_x$ showed a monotonic trend. The TiO$_x$ films gradually transformed from anatase to rutile while their refractive index and mass density initially increased followed by a gradual decline. For HfN$_x$, the films went from cubic hafnium oxynitride to face-centered-cubic hafnium mononitride while their conductivity and Hf^{3+} fraction initially increased significantly followed by a slight decline. SiN$_x$ films monotonically degraded to a lower mass density and refractive index while undergoing a significant increase in wet-etch rates. Additionally, material properties of TiO$_x$ grown with RF substrate biasing, where E_i was enhanced beyond the aforementioned thresholds, were found to become a function of both the enhanced E_i and the duration for which E_i was enhanced during t_p. These findings validated the conclusions made in our previous work where controlling the dose of energetic ions impinging on a growing film by varying the bias duration was suggested as an alternative route for tuning material properties. In addition, the results of this work shed light on the relation between the characteristics of energetic ions and the ensuing material properties, e.g., by providing energy maps of material properties in terms of the $E_{i,dose}$ during plasma ALD. They demonstrate how the quantification and control of ion energy and flux characteristics during plasma ALD serve as a means for obtaining nanoscale films with the required material properties. Finally, the results of this work signify how energy thresholds related to material atom displacement or activation of ion-induced chemical reactions are parameters relevant not only for plasma ALE,[23,87] but also for plasma ALD performed under the influence of energetic ions. Further investigation for better determination of such thresholds at $E_i <$ 100 eV can be carried out by implementing tailored bias voltage waveforms, which are known to provide mono-energetic ions (having narrow, mono-modal IFEDFs) during plasma exposure with substrate biasing.[100]

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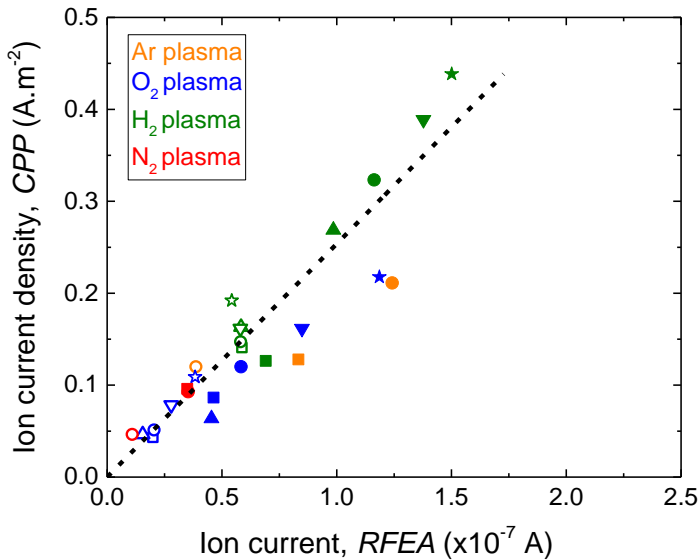
Appendix *6*

RFEA calibration

Figure A6.1. Scatter plot of ion current density, J_{CPP}, obtained from a capacitive planar probe (CPP)[1] as a function of ion current, I_C, obtained from the collector plate of the retarding field energy analyzer (RFEA) measured in Ar, O_2, H_2 and N_2 plasmas at different pressures and ICP powers for a grounded substrate. The dashed line through the origin is a linear fit of all the data points. The inverse of the slope of this line gives the effective ion sampling area, A_{eff}, of the RFEA collector plate, which can be used to derive the ion current density, J_C, from RFEA measurements. The solid symbols denote a plasma pressure of 7.5 mTorr while the hollow symbols denote 15 mTorr (except for H_2 plasma for which the hollow symbols represent 19 mTorr). ICP powers of 100, 200, 300, 400 and 500 W are denoted by the symbols with square, triangle, circle, inverted triangle and star shapes, respectively.

The RFEA used in this work consisted of a series of three grids sandwiched between sampling orifices and a collector plate. An array of 37 orifices, each with a diameter of 800 μm,[28,31,32] resulted in a total ion acceptance or sampling area (A_{tot}) of about 19 mm^2. Each grid and collector plate beneath the sampling orifice were situated in a plane perpendicular to the trajectory of the impinging ions. Low-pass filters with high input impedance at radio frequency were present between each grid and collector and the RFEA electronics. This allowed the RFEA and its components to float at the bias voltages developing on the substrate when AC bias powers at radio frequency were applied to the reactor table through the matching network. High-temperature cabling connected the RFEA to the data acquisition unit through a vacuum feed-through at the reactor wall.

The ion current, I_C, measured at the collector plate corresponds to ions that have entered the RFEA through the orifice and successively pass through the three layers of partially transmitting planar grids. As a result, the effective ion sampling area, A_{eff}, of the collector plate is lower than the A_{tot} of the RFEA orifices. A method with which the A_{eff} of the RFEA can be determined is by calibrating the I_C measured at the collector plate with the ion current density, J_{CPP}, measured using a capacitive planar probe (CPP) during plasma exposure. The technique of measuring J_{CPP} using a CPP (also known as an ion probe) has been thoroughly described in previous work conducted within our group by Petcu et al.[1] Figure A6.1 shows a scatter plot of J_{CPP} measured using a CPP versus I_C measured at the RFEA collector plate during plasma exposures on a grounded substrate stage in an Oxford Instruments FlexAL system. The measurements were performed in Ar, O_2, H_2 and N_2 plasmas at various operating pressures and ICP powers, covering the range of conditions reported in Chapter 6. The J_{CPP} measured using the CPP was observed to have a linear relationship with the I_C measured using the RFEA as indicated by the dashed line through the origin obtained from a linear fit of all data points. The inverse of the slope of this line gives the calibrated A_{eff} of the RFEA collector plate. It yielded a value of 0.39 $\pm$ 0.09 mm^2 where the uncertainty corresponds to the standard deviation of the 26 data points. Expressing the standard deviation as a percentage of the A_{eff} gives a relative measurement uncertainty within $\pm$ 23%, which gives an indicator for the spread in individual measurements around the fitted line. The A_{eff} at the collector expressed as a percentage of the total ion sampling area, A_{tot}, at the entrance orifices of the RFEA yielded a net grid transmission factor, T_G, of about 2.1%. Denieffe et al.[2] calibrated a similar three-grid RFEA (with A_{tot} of 21.5 mm^2) by comparing the ion currents at each grid with that at the collector plate. They reported a calibrated ion current density value of 0.5 A.m^{-2} (with an uncertainty up to 27%) for a collector current of 200 nA that can be used to calculate an A_{eff} of 0.40 mm^2 at the collector and a T_G of 1.9%.[2] These values were comparable to the corresponding values of the A_{eff} and T_G obtained in our work after CPP calibration. Although the differences in the plasma operating conditions and the type of plasma could play a role behind the $\pm$ 23% uncertainty in measurements, the accuracies of the measurement techniques themselves could also influence the uncertainty. Since it was not possible to discern between these factors limiting measurement uncertainty, an overall calibration was performed spanning all the data points shown in Figure A6.1. The I_C measured at the RFEA collector plate divided by the calibrated A_{eff} of 0.39 mm^2 allowed determination of the ion current density, J_C, at the RFEA collector plate (i.e., $J_C = I_C/A_{eff}$). The calibrated J_C was then used to derive parameters discussed in Chapter 6.

Deriving IFEDF from J_C-V_{G2} measurements

Assuming the formation of a collisionless plasma sheath above a RFEA exposed to a plasma, a directional flux of ions (with respect to the surface plane of the RFEA) can be considered to impinge on the RFEA with a homogeneous one-dimensional velocity distribution function, $f(v)$, and an energy distribution function, $g(E)$, corresponding to the one-dimensional velocity component.[3–6] Here v is the variable for velocity and E the variable for kinetic energy of the impinging ions that are related by the expression $E = (Mv^2)/2$ such that $dE = Mv\,dv$. By definition,[3,7]

$$f(v)\,dv = g(E)\,dE = dn \qquad \text{Eq. A6.1}$$

which states that the number of ions per unit volume, dn, in the velocity range v to $v + dv$ must equal the number of ions per unit volume in the corresponding energy range E to $E + dE$. The ion current density measured at the collector plate of the RFEA, J_C, can be expressed in terms of $f(v)$ and $g(E)$ as[3,4,6,7]

$$J_C = e \int_{v_i}^{\infty} v\,f(v)dv = e \int_{E_i}^{\infty} \sqrt{(2E)/M}\ g(E)dE \qquad \text{Eq. A6.2}$$

where e is the elementary charge constant, v_i is the minimum velocity and E_i the corresponding minimum kinetic energy of the ions impinging on the RFEA collector plate. Both v_i and E_i are functions of the retarding voltage, V_{G2}, applied to the discriminator grid G2 with respect to the voltage of the floating grid G1 of the RFEA (see Figure 1 in Chapter 6) and are given by the expressions $v_i = \sqrt{(2eV_{G2})/M}$, where M is the ion mass, and $E_i = eV_{G2}$. The maximum ion velocity and corresponding ion kinetic energy are independent of the retarding voltage. Differentiating under the integral expression for J_C in Equation A6.2 with respect to V_{G2} and rearranging gives expressions for $f(v_i)$ and $g(E_i)$ as[3,4,6,7]

$$f(v_i) = -M\,\frac{1}{e^2}\frac{dJ_C}{dV_{G2}} \qquad \text{Eq. A6.3}$$

$$g(E_i) = -\sqrt{\frac{M}{2E_i}}\,\frac{1}{e^2}\frac{dJ_C}{dV_{G2}} \qquad \text{Eq. A6.4}$$

Equation A6.3 is the expression depicting the ion velocity distribution function (IVDF) while Equation A6.4 gives the corresponding ion energy distribution function (IEDF) as reported in the literature.[3,4,6,7] For the molecular O_2, H_2 and N_2 plasmas investigated in this work, there can be several ion species present having different M. Consequently, it is not trivial to represent the exact IVDF and/or the exact IEDF of these plasmas by means of J_C-V_{G2} measurements conducted using a RFEA. A more accurate

representation of such RFEA measurements is given by the ion flux-energy distribution function (IFEDF),[5,8,9] $\mathbf{h_\Gamma}(E_i)$, which can be expressed as

$$\mathbf{h_\Gamma}(E_i) = \frac{1}{M}\, \mathbf{f}\left(\sqrt{\frac{2E_i}{M}}\right) = \sqrt{\frac{2E_i}{M}}\; \mathbf{g}(E_i) = -\frac{1}{e^2}\frac{\mathrm{d}J_C}{\mathrm{d}V_{G2}} \qquad \text{Eq. A6.5}$$

The term on the right hand side in Equation A6.5 is devoid of M and allows RFEA measurements to be represented using simply the negative derivative of the measured J_C with respect to V_{G2} (see Equation 1 of Chapter 6). It is conveniently plotted as a function of eV_{G2}, which basically denotes E_i as mentioned before.

Note that $\mathbf{h_\Gamma}(E_i)\,\mathbf{d}E_i$ gives the number of ions impinging on the surface per unit area per unit time in the energy range E_i to $E_i + \mathbf{d}E_i$. Therefore, the integral $\int_0^\infty \mathbf{h_\Gamma}(E_i)\,\mathbf{d}E_i$ yields the total ion flux, Γ_i, impinging on the surface (see Equation 3 of Chapter 6).[8–11] Moreover, the mean ion kinetic energy,[8,9,12] $\langle E_i \rangle$, is given by $\left[\int_0^\infty (\mathbf{h_\Gamma}(E_i) \times E_i)\,\mathbf{d}E_i\right]/\Gamma_i$ where the term on the numerator denotes the total kinetic energy flux delivered to the surface by the impinging ions,[13,14] $E_{i,flux}$ (see Equations 4 and 5 of Chapter 6).

Detailed outline of PEALD process conditions

For the deposition of titanium oxide (TiO$_x$), tetrakis(dimethylamido)titanium or TDMAT [Ti(N(CH$_3$)$_2$)$_4$, >99.99% purity from Sigma Aldrich] was used as the precursor while 100 sccm O$_2$ gas (>99.999% purity) was used for generating a plasma with 200 W RF-ICP power at a pressure of 9 mTorr. The precursor was held in a stainless steel bubbler that was heated to 60 °C at which TDMAT has a vapor pressure of 1 Torr.[15] For the precursor delivery to the deposition chamber, 100 sccm Ar (>99.999% purity) bubbling flow was employed. The precursor dose, purge, plasma exposure and purge times were set to 200 ms, 3 s, 10 s and 3 s, respectively.

Hafnium nitride (HfN$_x$) films were grown using tris(dimethylamino)cyclopentadienyl hafnium or TDMACpH [CpHf(N(CH$_3$)$_2$)$_3$, >99.99% purity from Air Liquide] as the precursor while 100 sccm H$_2$ (>99.999% purity) gas was used for generating a plasma with 100 W RF-ICP power at a pressure of 30 mTorr. Lower pressures were not possible for stable ignition of an H$_2$ plasma. The precursor was held in a stainless steel bubbler that was heated to 60 °C at which TDMACpH has a vapor pressure of 100 mTorr.[16] The precursor was delivered to the deposition chamber using 100 sccm Ar (>99.999% purity) bubbling flow. The dose and purge times for PEALD of HfN$_x$, were 400 ms, 2 s, 10 s and 4 s, respectively.

PEALD of silicon nitride (SiN$_x$) was carried out using di(*sec*-butylamino)silane or DSBAS [(SiH$_3$N(^{s}Bu)$_2$), purity >99.3% from Versum Materials] as the precursor while 100 sccm N$_2$ gas (>99.999% purity) was used for generating a plasma with 600 W RF-ICP power at a pressure of 12 mTorr. The precursor was held in a stainless steel bubbler that was heated to 40 °C at which DSBAS has a vapor pressure of ∼5 Torr.[17] Owing to this high pressure, the precursor was vapor drawn into the deposition chamber with the butterfly valve completely closed. A precursor hold or reaction step was employed immediately after precursor dosage in order to maximize precursor utilization while a continuous flow of 50 sccm N$_2$ gas (purity 99.9999%) was passed through the alumina plasma tube during the precursor dose and reaction steps. This was done in order to reduce precursor adsorption on the inner surfaces of the plasma tube during these two steps.

In order to perform PEALD with substrate biasing, the plasma exposure step was modified by applying a bias on the substrate table. The step sequences of the PEALD processes implemented without and with substrate biasing are shown in Figure A6.2. The substrate bias was applied either for the whole duration (bias duty cycle = 100%, Figure A6.2b) or a part of the duration (0% < bias duty cycle < 100%, Figure A6.2c) of the plasma exposure step. For example, during a plasma exposure step of 10 s, the bias was

active for all 10 s (Figure A6.2b) or half of this duration (5 s) by applying it in an interleaved manner at the end (Figure A6.2c) of the plasma exposure step.
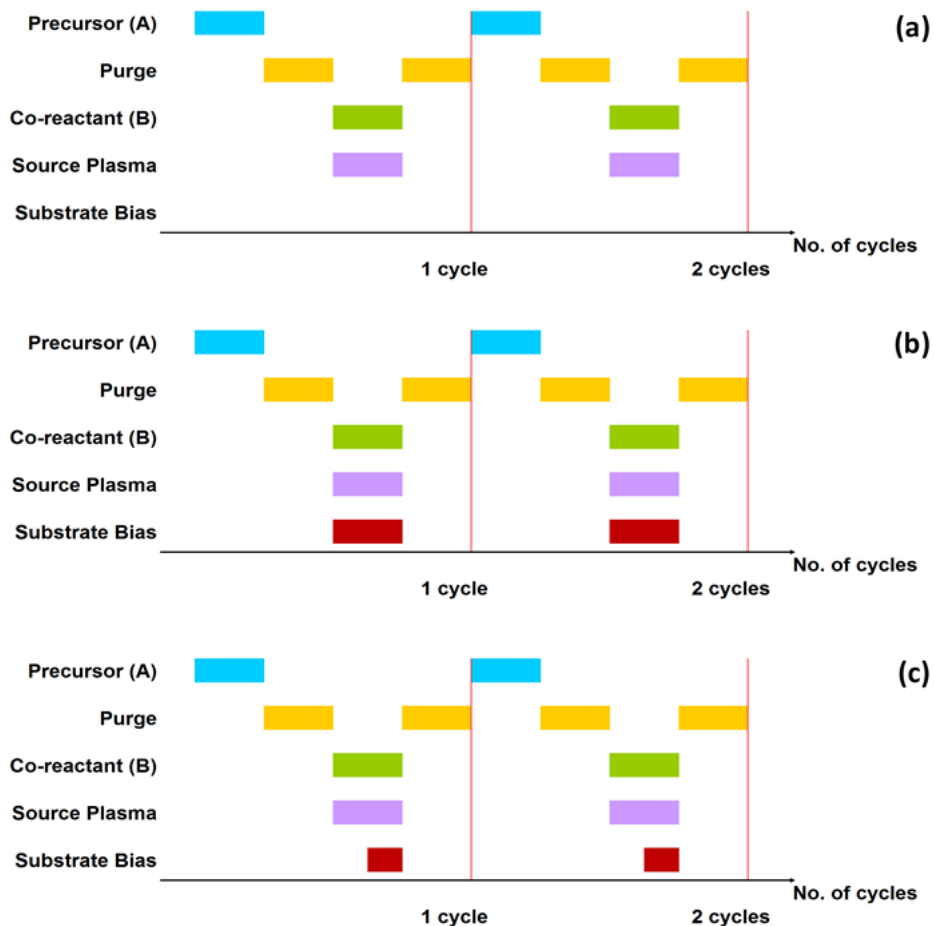

Figure A6.2. Step sequence for two-step *[AB]ₙ* plasma ALD cycles **(a)** without any substrate biasing during plasma exposure where the substrate table is grounded (Source Plasma "ON", Substrate Bias "OFF", bias duty cycle = 0%) **(b)** with substrate biasing during plasma exposure where the bias is applied for the full duration of the plasma exposure step (Source Plasma "ON", Substrate Bias "ON", bias duty cycle = 100%) and **(c)** with interleaved substrate biasing where the bias is applied for a fraction of the plasma exposure step (Source Plasma "ON", Substrate Bias "ON", 0% < bias duty cycle < 100%). *A* refers to the precursor dose step, *B* the co-reactant or plasma gas exposure step and *n* is the number of ALD cycles.

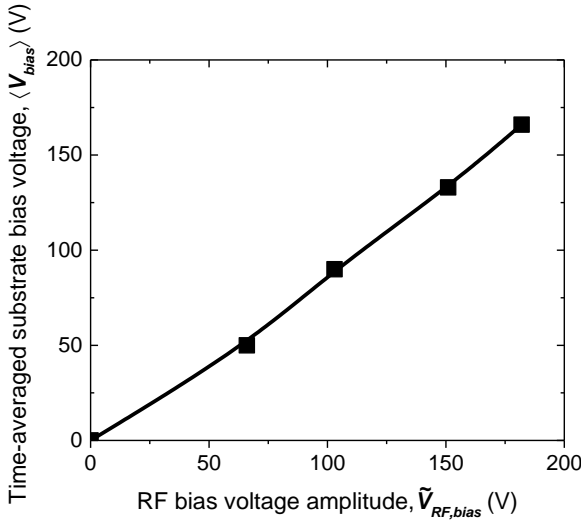## *Inert Ar plasma without and with RF substrate biasing*

Figure A6.3. Time-averaged substrate bias voltage, $\langle V_{bias} \rangle$, as a function of the RF bias voltage amplitude, $\tilde{V}_{RF,bias}$, measured using an oscilloscope connected to the reactor table via a high voltage probe in an Ar plasma at 200 W ICP power, P_{ICP}, and 9 mTorr pressure. It illustrates the linear dependence of $\langle V_{bias} \rangle$ on $\tilde{V}_{RF,bias}$.
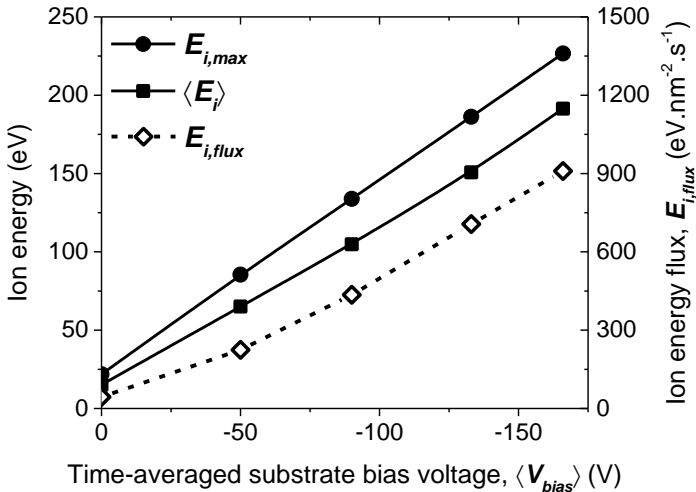

Figure A6.4. The mean ion kinetic energy, $\langle E_i \rangle$, maximum ion kinetic energy, $E_{i,max}$, and total ion kinetic energy flux, $E_{i,flux}$, as a function of the time-averaged substrate bias voltage, $\langle V_{bias} \rangle$, in an Ar plasma at 200 W ICP power, P_{ICP}, and 9 mTorr pressure.
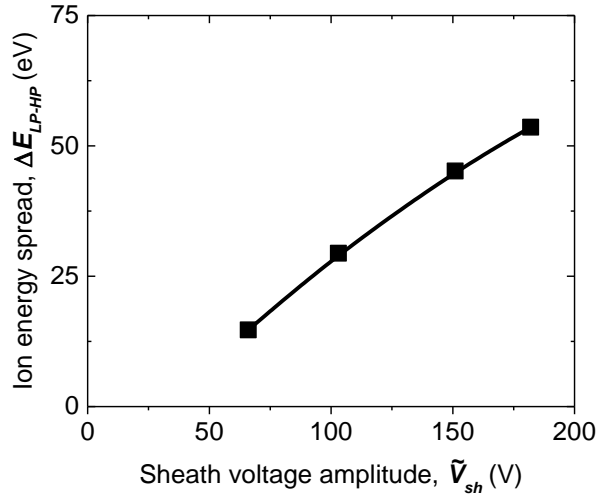
Figure A6.5. The spread in ion kinetic energy in terms of the low and high energy peak separation, ΔE_{LP-HP}, of bi-modal ion flux-energy distribution functions (IFEDFs) as a function of the oscillation amplitude of the sheath voltage, $\widetilde{V}_{sh}$, measured in an RF biased inductive Ar plasma at 200 W ICP power, P_{ICP}, and 9 mTorr pressure.

Figure A6.5 shows the experimentally measured values of ΔE_{LP-HP} as a function of the oscillation amplitude of the sheath voltage, $\widetilde{V}_{sh}$, for an Ar plasma ignited at 200 W ICP power and 9 mTorr pressure. $\widetilde{V}_{sh}$ is approximately given by the amplitude of the RF bias signal, $\widetilde{V}_{RF,bias}$,[10,18,19] applied to the substrate. Figure A6.5 shows ΔE_{LP-HP} scales with $\widetilde{V}_{RF,bias}$, which is in good agreement with the trend reported previously by Hayden *et al.*[18]
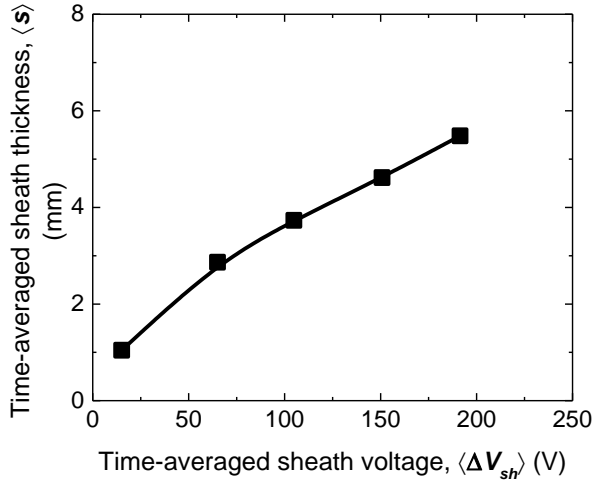
Figure A6.6. Time-averaged sheath thickness, $\langle s \rangle$, as a function of the time-averaged sheath voltage, $\langle \Delta V_{sh} \rangle$, for Ar plasma without and with RF substrate biasing at 200 W ICP power and 9 mTorr pressure.

For Ar plasmas without and with RF substrate biasing at 200 W ICP power and 9 mTorr pressure ignited in the remote ICP reactor used in this work, a collisionless Child-Langmuir sheath[20] has been assumed to calculate the time-averaged sheath thickness, $\langle s \rangle$, using

$$\langle s \rangle = \frac{4}{3} \left(\frac{\epsilon_o T_e}{0.61 e n_o} \right)^{1/2} \left(\frac{\langle \Delta V_{sh} \rangle}{2 T_e} \right)^{3/4}$$ Eq. A6.6

where ϵ_o is the permittivity of free space, T_e is the mean electron temperature, n_o is the plasma density and $\langle \Delta V_{sh} \rangle$ is the time-averaged sheath voltage, (determined using $\langle E_i \rangle$ from Figure 3c and Equation 2 of Chapter 6). T_e of approximately 3 eV[21] was assumed for the Ar plasma ignited at 200 W ICP and 9 mTorr. n_o was calculated using values of the total ion flux, Γ_i, determined from ion current densities measured using the calibrated RFEA (from Figure 3b of Chapter 6) and the expression for the Bohm velocity, u_B, such that[20]

$$n_o = \frac{\Gamma_i}{0.61 u_B} = \frac{\Gamma_i}{0.61} \left(\frac{eM}{T_e} \right)^{1/2}$$ Eq. A6.7

where M is the mass of an ion (Ar⁺). Figure A6.6 shows a plot of $\langle s \rangle$ versus $\langle \Delta V_{sh} \rangle$ for the aforementioned Ar plasmas without and with RF substrate biasing. The magnitude of the calculated values of $\langle s \rangle$ and the trend in those values as a function of $\langle \Delta V_{sh} \rangle$ are comparable to those reported recently by Wen *et al.*[19] for Ar plasmas ignited in a remote ICP reactor at similar pressures and ICP powers.

The ion transit time, τ_i, is related to time-averaged sheath thickness, $\langle s \rangle$, through the expression[22]

$$\tau_i = 3\langle s \rangle \left(\frac{M}{2e\langle \Delta V_{sh} \rangle} \right)^{1/2}$$ Eq. A6.8

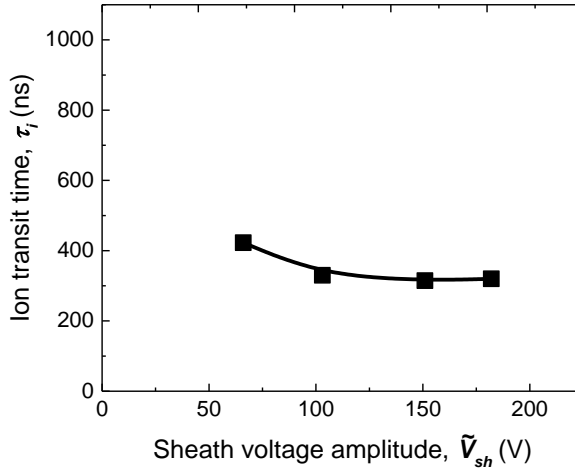**Figure A6.7.** Ion transit time, τ_i, as a function of the oscillation amplitude of the sheath voltage, $\widetilde{V}_{sh}$, for Ar plasma without and with RF substrate biasing at 200 W ICP power and 9 mTorr pressure.

The analytical model developed by Benoit-Cattan and Bernard[23] provides an expression for ΔE_{LP-HP} in terms of $\widetilde{V}_{sh}$, τ_i, and the time period of the applied bias signal, τ_{RF} (~74 ns for a radio-frequency bias). The values measured for ΔE_{LP-HP} using the RFEA in this work were used to determine τ_i using the aforementioned model, which is given by Equation 7 of Chapter 6. Figure A6.7 plots the τ_i dataset calculated in this work as a function of $\widetilde{V}_{sh}$. The magnitude of the calculated values of τ_i and the trend in those values as a function of $\widetilde{V}_{sh}$ were in good agreement with the corresponding parameters reported by Wen *et al.*[19] for Ar plasmas ignited in a remote ICP reactor at a similar pressure and ICP power.

Relationship between ion energy characteristics and properties of PEALD grown films

i) Titanium oxide (TiO$_x$) grown with O$_2$ plasma
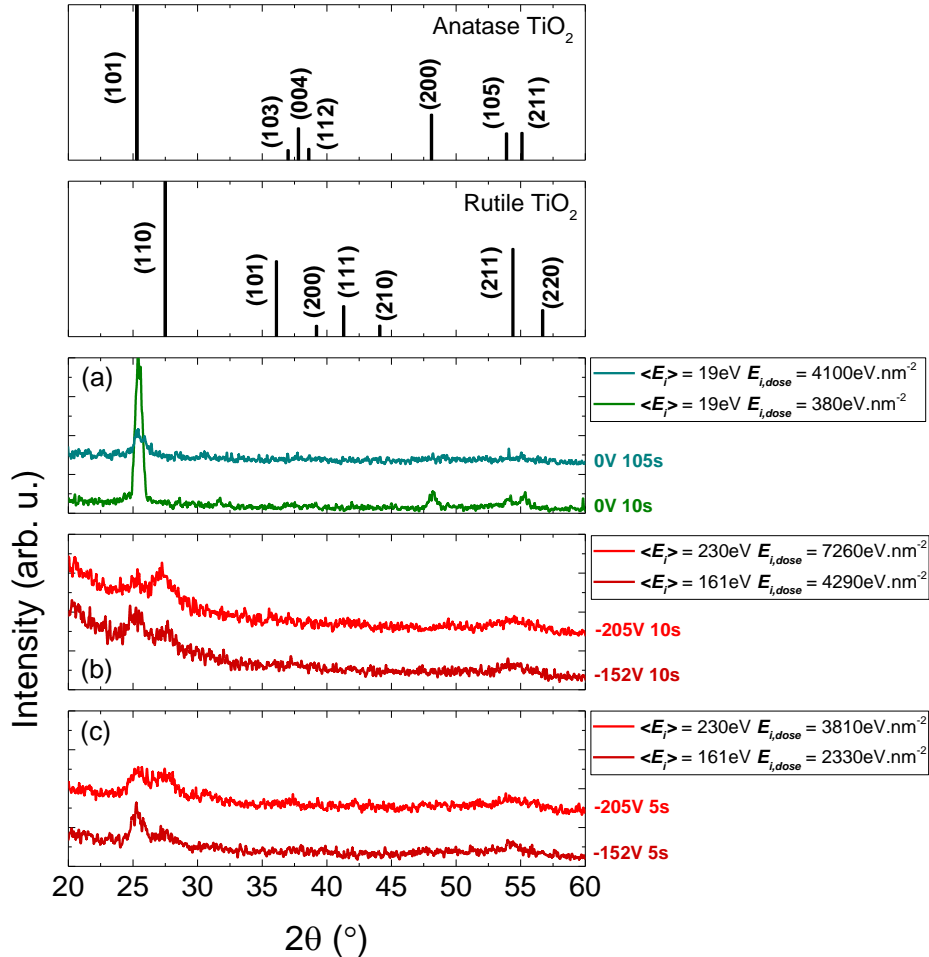

Figure A6.8. Grazing incidence X-ray diffractograms for titanium oxide films deposited at a stage temperature of 300 °C **(a)** without substrate biasing for 10 s and 108 s O$_2$ plasma steps, **(b)** with time-averaged substrate bias voltages, $\langle V_{bias} \rangle$, of -152 V and -205 V applied for all 10 s of O$_2$ plasma exposure and **(c)** $\langle V_{bias} \rangle$ of -152 V and -205 V applied for the last half (5 s) of the 10 s O$_2$ plasma step. Peaks corresponding to anatase and rutile phase of TiO$_2$ are shown in the reference patterns of powder samples. The mean ion kinetic energy, $\langle E_i \rangle$, total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, for the corresponding $\langle V_{bias} \rangle$ are indicated in the legends.

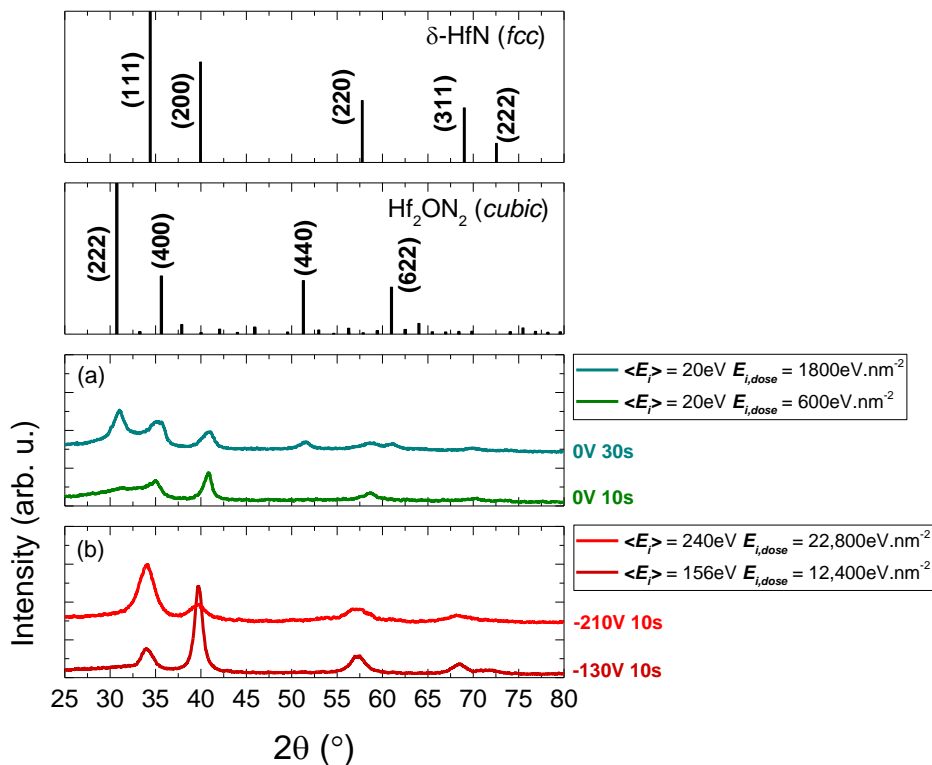## ii) Hafnium nitride (HfN$_x$) grown with H$_2$ plasma

Figure A6.9. Grazing incidence X-ray diffractograms for hafnium nitride films[24,25] deposited at a stage temperature of 450 °C **(a)** without substrate biasing for 10 s and 30 s H$_2$ plasma steps, **(b)** with time-averaged substrate bias voltages, $\langle V_{bias} \rangle$, of -130 V and -210 V applied for 10 s of H$_2$ plasma exposure Peaks corresponding to the fcc δ-HfN$_x$ and cubic Hf$_2$ON$_2$ are shown in the reference patterns of powder samples. The mean ion kinetic energy, $\langle E_i \rangle$, and total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, for the corresponding $\langle V_{bias} \rangle$ are indicated in the legends.
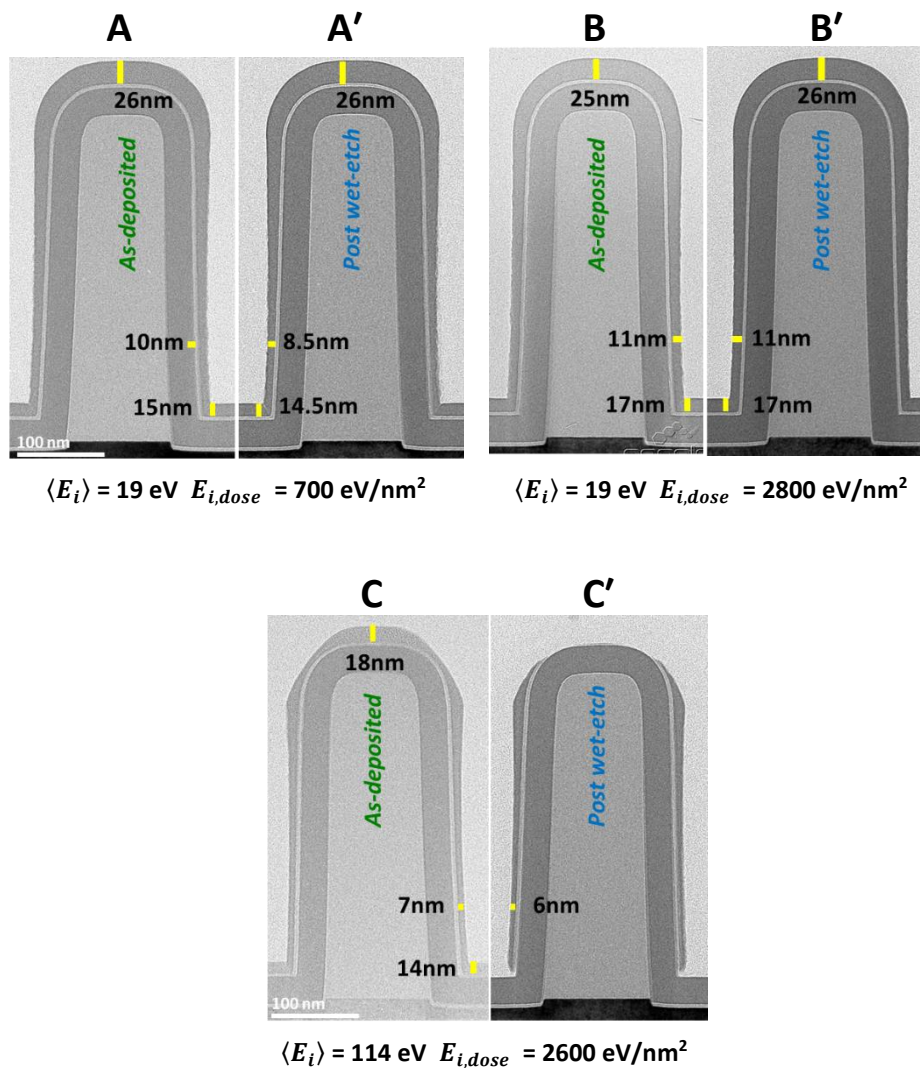
iii) Silicon nitride (SiN$_x$) grown with N$_2$ plasma

A **A'** **B** **B'**

26nm 26nm 25nm 26nm

As-deposited *Post wet-etch* *As-deposited* *Post wet-etch*

10nm 8.5nm 11nm 11nm

15nm 14.5nm 17nm 17nm

100 nm

$\langle E_i \rangle$ = 19 eV $E_{i,dose}$ = 700 eV/nm^2 $\langle E_i \rangle$ = 19 eV $E_{i,dose}$ = 2800 eV/nm^2

C **C'**

18nm

As-deposited *Post wet-etch*

7nm 6nm

14nm

100 nm

$\langle E_i \rangle$ = 114 eV $E_{i,dose}$ = 2600 eV/nm^2

Figure A6.10. Cross-sectional TEM images of **(A)**, **(B)**, **(C)** as-deposited and **(A')**, **(B')**, **(C')** post wet-etch (in 30 s dilute HF) silicon nitride films grown on 3D trench nanostructures (AR = 4.5:1) at a stage temperature of 500 °C. Images **(A)**, **(A')** and **(B)**, **(B')** are for films deposited using 10 s and 80 s N$_2$ plasma steps, respectively, without any biasing while images **(C)**, **(C')** are for films deposited with a time-averaged substrate bias voltage, $\langle V_{bias} \rangle$ = −94 V, during the last half (10 s) of a 20 s N$_2$ plasma exposure step. Film thicknesses at the top, bottom-side and bottom regions of the trench are shown using the yellow bars. The mean ion kinetic energy, $\langle E_i \rangle$, and total kinetic energy dose of ions per unit substrate area per ALD cycle, $E_{i,dose}$, for the corresponding $\langle V_{bias} \rangle$ are also indicated for each dataset.

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7

Atomic Layer Etching: What Can We Learn from Atomic Layer Deposition?

Anisotropic etching   **Isotropic etching**   **Selective etching**
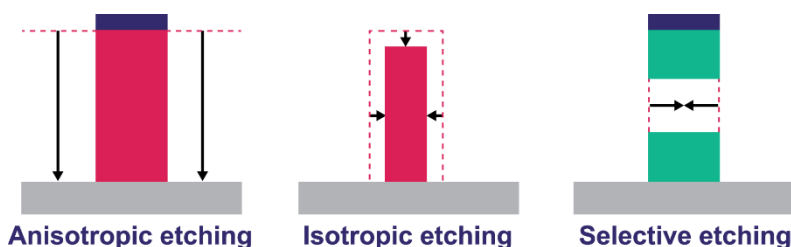
Current trends in semiconductor device manufacturing impose extremely stringent requirements on nanoscale processing techniques, both in terms of accurately controlling material properties and in terms of precisely controlling nanometer dimensions. To take nanostructuring by dry etching to the next level, there is a fast growing interest in so-called atomic layer etching processes, which are considered the etching counterpart of atomic layer deposition processes. In this chapter, past research efforts are reviewed and the key defining characteristics of atomic layer etching are identified, such as cyclic step-wise processing, self-limiting surface chemistry, and repeated removal of atomic layers (not necessarily a full monolayer) of the material. Subsequently, further parallels are drawn with the more mature and mainstream technology of atomic layer deposition from which lessons and concepts are extracted that can be beneficial for advancing the fields of anisotropic, isotropic and selective atomic layer etching (see images above).

7.1 Introduction

Since its inception in the late 1950s, the semiconductor industry has shown an unsurpassed and continuous potential to double the number of transistors on logic and memory dies typically every two years. This 2-year pace in scaling was recognized by Gordon Moore as early as in 1965[1] and has been referred to as Moore's Law. The driving business forces for scaling have been twofold: cost efficiency and device performance. Until the early 2000s, traditional optical lithography has enabled the continuous scaling of gate pitch and areal scaling of the planar CMOS units. New strategies were conceived in the International Technology Roadmap for Semiconductors (ITRS)[2] for the next, second era of scaling by using new materials such as strained silicon, gate stacks of high-*k* dielectrics and metals with optimum work function,[3,4] and high-mobility channels of Ge and III-V compound semiconductors.[5] However, these *materials-enabled* solutions also have a 2D scaling nature and are reaching fundamental limits. Consequently, for both logic and memory devices, the use of the third (vertical) dimension is now being explored, thus introducing the so-called third era of scaling. Here, 3D architectures and low power consumption designs are developed to further increase the areal transistor density, ranging from FinFETs with conducting channels on three sides of a vertical fin structure, to "gate-all-around" structures,[6,7] multiple transistor stacks in one die (e.g., 3D NAND[8]) and multiple die-stacks connected by through silicon vias (TSVs).[9]

The choice of materials and structures in semiconductor devices will greatly depend on the advancements in processing techniques and equipment. As devices approach single-digit nanometer critical dimensions (CDs), tolerances are required that are on the order of a few atoms. In addition, aspect ratios will become larger and topographies more complicated. The ability to precisely and selectively add and/or remove functional materials at an atomic scale has become imperative. The overall challenge in the processing of semiconductor devices lies therefore, in the accurate control of the material properties as well as in the control of the nanometer dimensions, hence in "materials control" and "dimensions control". This puts a heavy burden on processing techniques such as deposition and etch.

One technique that has been introduced in semiconductor device manufacturing in the past decade as a true enabling technology is atomic layer deposition (ALD).[10,11,12,13] ALD by itself is not a new technique – it was already developed by Suntola in 1977[14] – but it was not until the late 1990s that the semiconductor community started realizing that ALD could enable dedicated processes to meet the stringent demands on material quality, precise thickness and layer conformality control in future nanoscale device manufacturing.[15] Today, the technique has grown to be an essential technology in semiconductor device mass-manufacturing, especially of FinFET and other devices with

elevated 3D topology. Moreover, the processing at low temperatures (<150 °C) by ALD gained importance (e.g., in nanopatterning) which has led to the development of energy-enhanced ALD processes such as plasma-enhanced ALD.[16]

Initially, ALD served mainly as a method to replace the thermally-grown SiO_2 gate oxide in CMOS transistors by thin films of high-*k* oxide materials. Among the vapor-phase deposition methods, ALD is the preferred method of choice rather than physical or chemical vapor deposition (PVD and CVD). This is due to its layer-by-layer growth characteristic, its soft nature (no plasma or sputter damage), its conformality on 3D surface topologies, and its low thermal budget (ALD processes are typically limited to temperatures <500 °C). Furthermore, the fact that high quality films can be prepared with precise growth control is a key merit of the technique.

ALD is not a continuous process or a continuous process divided into steps (a pulsed process, see Figure 1). Instead, ALD is a cyclic process in which film growth takes place by a repetition of cycles with every cycle consisting of several steps. Typically, an ALD cycle consists of four basic steps: two reactant dosing steps that are separated by two purge steps. Thus each ALD cycle can be divided into two half-reactions, i.e., half-reaction A during the first reactant dosing step (for the first reactant the term "precursor" is often employed) and half-reaction B during the second reactant dosing step (for the second half reaction the term "co-reactant" is appropriate). In each half-reaction, chemical reactions take place at the surface of the film in such a way that the surface chemistry is self-limiting. Thus half-reactions A and B can contribute to film growth but add at most one atomic layer (defined here as a layer of atoms, not necessarily a full monolayer). Hence, after a full "AB cycle" with sufficiently long dosing times for the precursor and co-reactant species (i.e., under so-called "saturation conditions"), the film thickness is increased by a well-defined value representing at most one atomic layer of material independent of the exact dosing times. This well-defined thickness is very repeatable cycle-over-cycle such that the targeted film thickness can be reached very precisely upon careful selection of the required number of ALD cycles. Evidently, the self-limiting surface chemistry is also the reason for the excellent conformality and unparalleled uniformity that can be achieved by ALD.

Since the commercial onset of ALD, many dedicated ALD chemistries and processes have been developed for a growing set of materials. Other embodiments of ALD have also been developed but they all share the same defining characteristics where the processes take place cycle-wise with several steps per cycle and are based on self-limiting surface chemistry. Meanwhile, a large variety of ALD equipment has entered the market, including tools for single-wafer and batch processing, energy-enhanced and plasma-enhanced ALD tools, and more recently, even spatial ALD equipment.[17] These
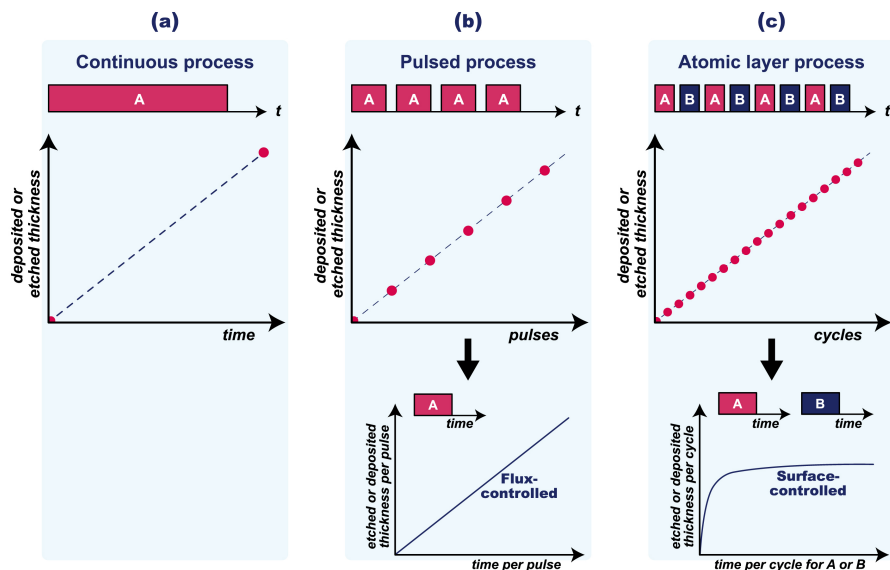
Figure 1. Several approaches can be adopted for thin film deposition and etching for vapor phase based techniques. **(a)** In a continuous process, the process A is started at *t* = 0 and stopped after the deposited or etched thickness has been reached. In this basic approach, the control of the deposited or etched thickness is limited as the deposited or etched thickness is "flux-controlled". Variations in the process conditions lead easily to variations in the flux of species and hence, in the final deposited or etched thickness, both over multiple deposition runs (i.e., wafer-to-wafer) or over the substrate area (i.e., within-wafer). **(b)** In a pulsed process, the continuous process is basically divided up into pulses and the pulses are repeated until the deposited or etched thickness has been reached. When the pulse length is well-defined, pulsing provides typically additional control over the continuous process but due to the flux-controlled nature similar drawbacks as in the continuous process hold. **(c)** Atomic layer processes are "surface-controlled" as they are based on self-limiting surface chemistries during, e.g., two half-reactions (A and B) that make up a full cycle. Every cycle yields a well-defined, fixed thickness that is deposited or etched when the time per cycle for the half-cycles is sufficiently long (i.e., when working in "saturated conditions"). This means that the thickness of the deposited or etched film can be controlled very accurately by choosing the right number of cycles. This holds when comparing one deposition run to another but it also leads to an excellent uniformity over the full substrate. Ideal atomic layer processes are very independent of variations in timings or process conditions.

developments have made ALD currently a mainstream technology for creating uniform and conformal nanomaterials and nanostructures with atomic scale accuracy.

Next-generation nanoscale devices will also require precise material removal or "etching". In the past 40 years Moore's Law could be continued by the numerous developments in plasma etching with continuously higher levels of dimensional control. Several of such developments have, for example, been enabled by approaches relying on pulsed operation, i.e., by time-modulation of the power, gas flows or bias voltages.[18]

Yet, every new technology node imposes new challenges in selectivity, plasma damage, aspect-ratio-dependent etching (ARDE) and line-edge roughness (LER).[18,19] These challenges related to current dry etching techniques provide a window of opportunity for being potentially tackled by an atomic-scale etching method analogous to ALD known as atomic layer etching (here abbreviated as "ALE", see also below). Although several efforts have been undertaken to develop layer-by-layer methods with precise etch control similar to its ALD counterpart, the development of ALE has comparatively lagged behind.

In this article, the efforts with respect to ALE will be first briefly reviewed (Section 2). Next, an attempt is made to identify the key aspects of ALE as well as its potential to become a novel technology option for producing single-digit nanometer critical dimensions (Section 3). This will be done by highlighting the cues it can take from the strengths and successes of its counterpart ALD process. Finally, the conclusions and a brief future outlook are presented (Section 4).

7.2 The early days of atomic layer etching

The concept of removing a single atomic layer from the surface of a solid was first claimed in a patent by Yoder in 1988 where he outlined a method for "atomic layer etching" of crystalline diamond.[20] In this patent, a cyclic process was described in which every cycle consisted of four steps (see Figure 2a): the diamond surface is flooded with NO_2 in the first step and with excited ions in step 3. Steps 2 and 4 are purge steps. Since then, a large set of publications has appeared in scientific literature and the method has come to be known by a variety of other names, namely digital etching,[21] layer-by-layer etching,[22] molecular-layer etching,[23] plasma atomic layer etching (PALE),[24] etc. Yet, the original name of "atomic layer etching" coined in the first patent has remained most popular. The acronym "ALE"[25] has often been used to distinguish the method from the abbreviation of atomic layer epitaxy (ALE),[10] the latter being used to identify atomic layer deposition processes before the term atomic layer deposition (with acronym "ALD") gained widespread adoption.[15]

Experimental efforts aimed at realizing ALE, commenced with the work of Maki *et al.* for GaAs[26] in 1989. They outlined a process, referred to as "atomic bilayer etching", where the exposure of a GaAs substrate to molecular chlorine led to a self-terminating spontaneous adsorption of the gas on the substrate surface producing a weakly bound surface chloride layer. A subsequent exposure of this chlorinated surface layer to a low-fluence 193 nm ArF excimer laser pulse induced desorption leading to the removal or etching of the halogenated surface layer. Meguro *et al.*[27] presented a "digital etching" process in which they used a Cl_2 gas pulse to passivate the surface of GaAs followed by
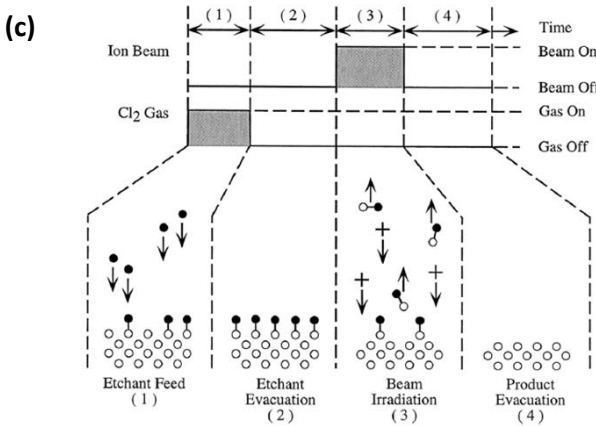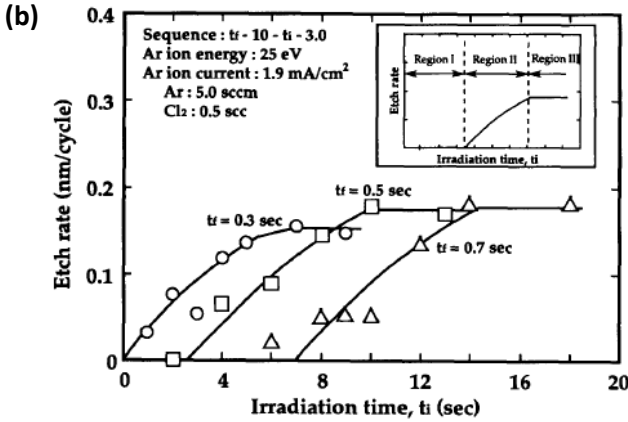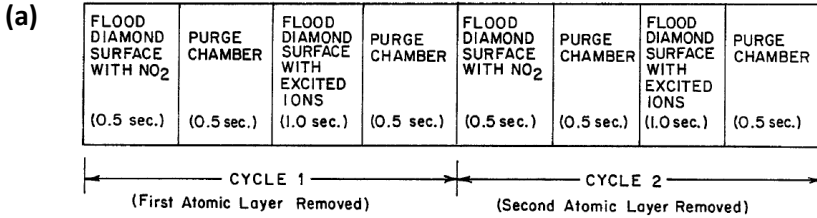
(a)

FLOOD DIAMOND SURFACE WITH NO$_2$	PURGE CHAMBER	FLOOD DIAMOND SURFACE WITH EXCITED IONS	PURGE CHAMBER	FLOOD DIAMOND SURFACE WITH NO$_2$	PURGE CHAMBER	FLOOD DIAMOND SURFACE WITH EXCITED IONS	PURGE CHAMBER
(0.5 sec.)	(0.5 sec.)	(I.0 sec.)	(0.5 sec.)	(0.5 sec.)	(0.5 sec.)	(I.0 sec.)	(0.5 sec.)

CYCLE 1
(First Atomic Layer Removed)

CYCLE 2
(Second Atomic Layer Removed)

(b)

Sequence : tf - 10 - ti - 3.0
Ar ion energy : 25 eV
Ar ion current : 1.9 mA/cm^2
Ar : 5.0 sccm
Cl$_2$: 0.5 scc

tf = 0.5 sec
tf = 0.3 sec
tf = 0.7 sec

Etch rate (nm/cycle)
Irradiation time, ti (sec)

Region I   Region II   Region III
Etch rate
Irradiation time, ti

(c)

(1)   (2)   (3)   (4)   Time
Ion Beam   Beam On
                                   Beam Off
Cl$_2$ Gas   Gas On
                                   Gas Off

Etchant Feed   Etchant Evacuation   Beam Irradiation   Product Evacuation
(1)   (2)   (3)   (4)

Figure 2. (a) Schematic from Yoder's early patent in 1988 showing the layout of the cycles for atomic layer etching crystalline diamond. The flooding of the diamond surface with NO$_2$ is alternated with flooding the surface with excited ions. Purging takes place in between these steps. Image from Ref. 20. **(b)** Saturation curves for atomic layer etching of GaAs by Cl$_2$ dosing and Ar$^+$ ion irradiation. Data is shown for various Cl$_2$ dosing or feed times. From Ref. 28. **(c)** Schematic of the atomic layer etching process of silicon by Cl$_2$ dosing and Ar$^+$ ion irradiation. The filled circles represent Cl atoms, the open circles represent Si atoms, and + represent Ar$^+$ ions. From Ref. 33. The processes shown in **(a)**-**(c)** are similar and form only one particular embodiment of atomic layer etching processes.

a purge cycle to remove residual Cl_2, a subsequent bombardment of the halogenated surface layer with 100 eV electrons followed by another purge of the etch products. Using this electron beam excited plasma process, an etch rate of 0.1 nm/cycle, i.e., ⅓ of a monolayer of GaAs was obtained, independent of the Cl_2 flow rate and the electron current density for the ranges investigated. The etch rate for GaAs was increased to 0.2 nm/cycle using a similar method[28] but using low energy 25 eV Ar^+ ions instead of electrons. In this work typical saturation curves were also provided showing zero etching at zero Ar^+ irradiation and a saturated etch rate for sufficiently long Ar^+ irradiation (see Figure 2b). For "layer-by-layer" etching, Ko et al.[29] used an electron cyclotron resonance (ECR) plasma source placed on top of a radio frequency (RF) powered electrode to generate reactive radicals with independent control over ion energy and ion flux. Bombardment of a surface-chlorinated GaAs layer with low energy but high-density Ar^+ ions at room temperature led to an etch rate of 0.5 nm/cycle, independent of the chlorine radical or Ar^+ ion exposure time. They also demonstrated ALE of other III-V semiconductors like GaInAs, AlInAs and InP. Ishii et al.[30] took an approach similar to that of Maki et al. by employing a 248 nm KrF excimer laser in place of a charged particle beam (ions, electrons) to irradiate a Cl_2 adsorbed GaAs surface. With their "digital etching" process, they obtained an etch rate of 0.2 nm/cycle, independent of excimer laser repetition rate and the amount of initially injected Cl_2.

In parallel to these investigations of atomic layer etching of III-V semiconductors, atomic layer etching of silicon was explored. Sakaue et al.[31] extrapolated the pioneering work of Horiike et al.[21] for "digital etching" of Si using molecular chlorine instead of fluorine as the adsorbate precursor. Removal of the surface-chlorine adsorbed species subsequently took place via desorption induced by Ar^+ ion irradiation. A saturated etch rate of about 0.4 Å/cycle was obtained as the Ar^+ ion irradiation time was increased. The value of 0.4 Å/cycle corresponds to about ⅓ of a monolayer of Si(100). Upon increasing substrate bias voltage, the etch rates increased rapidly with increased amounts of higher-order etch products ($SiCl_3$, $SiCl_4$). Matsuura et al.[22] and Suzue et al.[32] reported on "self-limited layer-by-layer etching" and "self-limited atomic layer etching" of Si, respectively, using ECR plasmas. The etch rate per cycle increased with the chlorine exposure time and saturated to a constant value of about ½ and ⅓ of a monolayer per cycle for Si(100) for Si(111), respectively, independent of the chlorine partial pressure. In their work, they also addressed the influence of the crystal orientation on the etch rate and the fact that only a fractional number of a monolayer is etched every cycle. On the basis of a molecular dynamics simulation study,[25] Athavale and Economou reported that ALE of a monolayer per cycle may be achieved with Cl_2 and Ar^+ ions (see Figure 2c). They presented experimental results in a follow up work in which they used a helicon plasma for generating the Ar^+ ions.[33] By applying and tuning a DC bias on the substrate, the Ar^+ ion bombardment energy could be adjusted to etch one monolayer off from

silicon in an a ~100 s cycle. The process was self-limiting with respect to both chlorine dose and the ion dose while the etch rate was found to be a strong function of the DC bias on the substrate, i.e., the ion bombardment energy.

ALE of silicon that makes use of energetic ions, albeit at low energy, may exclude any physical damage but may not be immune to any damage due to charging. To account for this charging damage, Park et al.[34,35] investigated ALE of silicon by using Cl_2 surface passivation followed by bombardment with energetic Ar neutrals. One monolayer per cycle of silicon (100) and (111) was etched in the process but with comparatively longer cycle durations of ~500 s and ~800 s, respectively, for the two orientations as the etch rates depended on the Cl_2 pressure and Ar neutral beam fluence. To overcome the drawback of such long cycle times, an ALE method incorporating pulsed plasmas has been proposed.[36,37] The concept relies on the formation of a self-limited halogenated surface layer in the presence of a plasma without initial substrate bias thus preventing ion bombardment induced etching. By using pulsed biasing, the halogenated surface layer is sputtered off faster than it can reform. Complete removal of this layer inhibits any further etching of the substrate provided the ion energy is below the sputtering threshold of the substrate. The bias is then switched off which again leads to the formation of a halogenated layer and the cycle can be repeated to obtain a fast ALE process.

Furthermore, attention was given to the ALE of oxides. Yeom and co-workers reported on ALE of HfO_2 using BCl_3 and an Ar neutral beam. They showed a considerable improvement in the electrical characteristics of the devices prepared by ALE when compared to results obtained for devices etched by conventional wet or dry etch techniques.[38,39] These improved results were attributed to a low edge damage of the gate oxide during ALE by maintaining the surface composition at the edge of the gate oxide together with exact control of the Si etch depth. Recently, Metzler et al.[40] also demonstrated ALE of SiO_2 using a steady-state Ar plasma, periodic injection of a defined amount of C_4F_8 gas and synchronized plasma-based Ar^+ ion bombardment. Injecting a predefined amount of C_4F_8 gas leads to the controlled deposition of a fluorocarbon (FC) layer in the one to several Ångstroms thickness range onto the SiO_2 surface. Applying low-energy Ar^+ ion bombardment induces etching of the FC layer together with reaction of carbon and fluorine with the underlying SiO_2 surface layer. The resulting modified SiO_2 surface layer is etched by the low-energy Ar^+ ion bombardment until the modified layer is removed at which point the SiO_2 etching terminates.

7.3 What can we learn from ALD?

As can be seen from the previous section, efforts for establishing an atomic-scale etching process analogous to ALD have been quite limited so far. They have been restricted to a few particular embodiments, material systems, and chemistries and the approaches developed till now have had limited success and/or a limited range of potential applicability. Yet, the efforts also demonstrate the potential opportunities provided by the ALE process concept, particularly in view of the current developments in the semiconductor industry. To significantly advance the applicability of ALE, it is worthwhile to look in more detail at the ins and outs of ALD. It can be meaningful to learn from the state-of-the-art features of this technology as well as from its historical developments and emerging trends. Identifying similarities and differences between ALE and its ALD counterpart can certainly contribute to expanding the toolbox of ALE processes with sufficient performance to tackle future challenges in semiconductor and other device manufacturing.

First, it is instructive to define atomic layer etching and to introduce a generalized ALE cycle. From the research efforts so far, it is clear that ALE is a layer-by-layer etching method with – similar to ALD – the following defining characteristics (see Figure 1): the process takes place cycle-wise with several steps per cycle, and is based on self-limiting surface chemistry. However, contrary to what is claimed or suggested in many previous reports (especially in the work related to silicon etching), it is not necessary or useful to restrict ALE to processes in which a full monolayer of material is etched. To achieve atomic layer etch precision in a very repeatable manner, the processes do not necessarily have to yield one monolayer per cycle. Removal of a submonolayer per cycle is adequate and, as a matter of fact, even better as the etch control can be even more precise. Note, that in virtually all ALD processes, the thickness increase per cycle is also limited to less than a monolayer (see Table 1) although there have been some cases reported in which the thickness increase is more than a monolayer.[41,42] Yet whether the decrease in thickness after one cycle of ALE is less or more than a monolayer, atomic scale precision in thickness and atomically smooth surfaces can still be obtained. In fact, it would be more sensible to add the criterion of (atomically) smooth surfaces to the definition of ALE. Furthermore, note that the limitation to processes that yield one monolayer per cycle is only well-defined when etching single-crystalline materials such as silicon. A monolayer is very ill-defined when etching amorphous or polycrystalline materials, for example high-k oxides such as HfO_2 in gate stacks.

A generalized ALE cycle can also be introduced by identifying parallels with ALD (see Figure 3). So far, the ALE technique has manifested itself mostly based on a chemically enhanced process in which passivation of the surface of the material to be

Table 1. The growth-per-cycle (GPC) for selected ALD processes. The GPC is given in metal atoms (M) per nm^2 and per cycle as well as equivalent monolayer (*eq. ML*) per cycle. For ALD, the GPC values can for example be ruled by the ionic radius of the metal center to be deposited,[64,65] the ligand sizes of the precursors,[64,66,67] or the density of adsorption sites on the surface.[68,69] For the calculation of the GPC as *eq. ML* the approximate distance between the metal atoms was used as derived from the atomic density of the bulk material neglecting the influence of crystal orientations, surface reconstructions, etc.

Material	Process details (substrate temperature)	GPC (Å)	GPC (M at. nm^{-2})	GPC (*Eq. ML*)	Reference
ZnO	$ZnEt_2 + H_2O$ (150 °C)	2.0	7.1	0.6	[70]
Al_2O_3	$AlMe_3 + H_2O$ (200 °C)	1.0	3.5	0.33	[71]
HfO_2	$HfCl_4 + H_2O$ (300 °C)	0.4	1.1	0.12	[72]
TiN	$TiCl_4 + NH_3$ (350 °C)	0.28	1.1	0.09	[73]
TaN_x	$Ta(NMe_2)_5 + H_2$ plasma (225 °C)	0.56	2.1	0.19	[59,74]
Pt	$MeCpPtMe_3 + O_2$ (300 °C)	0.45	3.0	0.2	[75]
Pd	$Pd(hfac)_2 + H_2$ plasma (100 °C)	0.17	0.9	0.05	[76]
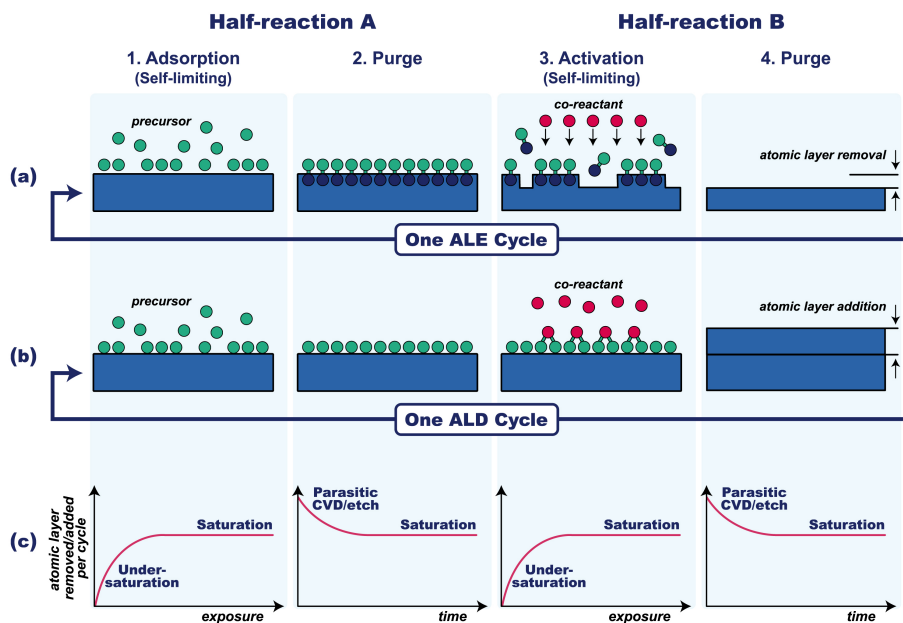
Figure 3. Schematic representation of one complete, generalized cycle of **(a)** atomic layer etching (ALE) and **(b)** atomic layer deposition (ALD). In **(c)** the so-called saturation curves for the various steps in the ALE and ALD processes are schematically illustrated. The depicted processes consist of two half-reactions A and B and the total cycle is divided into four process steps. Step 1 is the "adsorption step" and step 3 is the "activation step". In these steps the surface is exposed to reactants, here defined as "precursor" in step 1 and "co-reactant" in step 3. Step 2 and 4 are "purge steps". The cycles, and hence the process steps, are repeated multiple times when etching or depositing a film. Every cycle removes or adds an atomic layer from or to the film for ALE and ALD, respectively. The saturation curves show that exposure to the reactants in step 1 and 3 should be sufficiently long to reach saturation. The purging in between these steps should be sufficiently long to avoid parasitic CVD or parasitic etch reactions that compromise the ALE or ALD character of the processes.

etched with a layer of adsorbed precursor species decreases the activation energy required by energetic particle bombardment to remove that layer (see section 7.2). Limiting the discussion to a process with two half-reactions and four steps per cycle for simplicity reasons, it is more relevant and more comprehensive to identify an adsorption step and an activation step. In the adsorption step, the surface is exposed to a precursor gas which adsorbs onto the surface in a self-limiting way, i.e., preventing further multilayer adsorption. This adsorption of a precise amount of precursor is similar for ALE and ALD. This similarity also holds for the purge steps that separate the two half-reactions and which remove excess precursor species and reaction products from the reactor. However, the main differences lie in the third step. In ALE, the surface is activated by co-reactant species which remove volatile etch products from the surface

in a self-limiting way. After purging, this leads to the removal of one atomic layer from the surface (not necessarily a monolayer as discussed earlier). For ALD on the other hand, the activation step consists of exposing the surface to a co-reactant that completes the addition of an atomic layer of the material to be deposited on the surface, and, at the same time activates the surface for the next ALD cycle. The activation of the surface for the next cycle in the third step is a strict criterion for both ALD and ALE and this holds also for the self-limiting nature of the second half-cycle. For ALD, whether the elements of the co-reactant are added to the surface layer or not is insignificant from a conceptual point of view. Some co-reactants only activate the surface without contributing to growth, e.g., ALD of W from WF_6 and Si_2H_6 [43] and ALD of Pt from $(CH_3)_3Pt(CpCH_3)$ and O_2.[44,45]

The precursor in the adsorption step is typically well-defined. For ALD, it consists of an element to be deposited, e.g., the metal that defines the metal oxide, nitride, sulfide, etc. to be deposited. For ALE, it is typically a species which contains elements that can form volatile reaction products with the material to be etched. Fluorine- or chlorine-based precursors are typical examples used during ALE of silicon. The co-reactant during the activation step is less well-defined and is not limited to atoms or molecules. It can also consist of many other species such as ions, electrons, energetic neutrals from a neutral beam or photons. The activation step could even involve a substrate temperature ramp.[46] For ALE, such a multitude of possible co-reactants is apparent from the past research efforts reviewed in Section 2. However, for ALD, processes based on such co-reactants have been reported but have gained more attention fairly recently (see Ref. 47 and references therein).

Regarding the surface chemistry occurring during the two half-reactions in atomic layer processes, a large variety of surface reactions exists. For ALD, the surface chemistry can be based on reaction mechanisms such as ligand exchange, dissociation, association, combustion, abstraction, reduction, etc.[48] For ALE, in principle similar reaction mechanisms can take place although most studies so far relied on dissociation (e.g., dissociation of Cl_2 at active surface sites) in combination with desorption reactions, e.g., assisted by ions, electrons, or photons (see section 7.2). However, many processes relying on other chemistries can also be potentially developed as for example demonstrated in a recent article by Lee and George who developed a thermally driven "reverse ALD" process.[49]

For both ALE and ALD, the self-limiting behavior of the surface chemistry is key and should be verified by saturation curves. In case of ALD, one needs to verify whether or not an atomic layer of material has been added to the film independent of the dosing times as long as these are sufficiently long. The same holds for the removal of one

atomic layer in ALE. In both cases, this can be done by varying the dosing times for one step while keeping the dosing times for the other step(s) sufficiently long (see Figure 3c). One should also ensure that no atomic layer has been added or removed with zero dosing time for the precursor or co-reactant. If the latter does not hold true, the processes do not – strictly speaking – consist of two half-reactions and subsequently, the condition of an atomic layer deposition or etching process is not met. Another aspect is the purging after the two half-reactions. The purges should be long enough to ensure that excess precursor molecules and reaction products are completely removed from the reactor before the co-reactant is introduced, and vice versa. When the purging times are too short, precursor and co-reactant molecules can interact leading to parasitic CVD reactions occurring during ALD. Consequently, key features of ALD such as precise growth control, excellent conformality and unparalleled uniformity are compromised. For ALE, a similar phenomenon can occur, i.e., parasitic etch, which means that the etching is not restricted to one well-defined atomic layer. For example, in the processes reported for Si etching by Cl_2 adsorption and Ar^+ irradiation (see section 7.2), the Ar plasma used in the 2nd half-cycle to generate the Ar^+ might dissociate residual Cl_2 when the reactor has not been purged sufficiently. This will lead to uncontrolled etching of the silicon during the second half-reaction of the process.

Besides comparing ALE and ALD cycles and their process steps, it is also worthwhile to pay attention to the key (desired) features of the processes. From this perspective it is possible to identify some clear similarities and differences between ALE and ALD (see Figure 4). What both processes (should) have in common is that they should lead to a very good uniformity over a large substrate area, i.e. basically over the full wafer size when processing wafer-based semiconductor devices. For ideal ALE and ALD processes, this aspect is guaranteed by the fact that the processes are surface-controlled and self-limiting. This provides the opportunity to expose the wafer surface for a sufficiently long period to the precursor and co-reactant doses such that saturation of the surface chemistry can be reached over the full substrate area without multilayer removal or addition on highly-exposed surface regions. Obviously, another similarity lies in the control of the atomic layer processes: every cycle should lead to precise removal or addition of a well-defined atomic layer for ALE and ALD, respectively. However, major differences between ALE and ALD can be identified when considering the processing of 3D features at the substrate surface. The fact that ALD can yield very conformal films on demanding 3D topologies is a key asset of ALD intrinsic to the process. When depositing a film in, e.g., high aspect ratio trenches or holes, ALD processes will deposit a film with uniform thickness across the entire surface area of the substrate which includes the sidewalls and the bottom of the trenches or holes (see Figure 4b). Ideally, this is independent of the surface density of the features and their corresponding pitch. For the etching counterpart, the desired situation is however different. Dry etching is
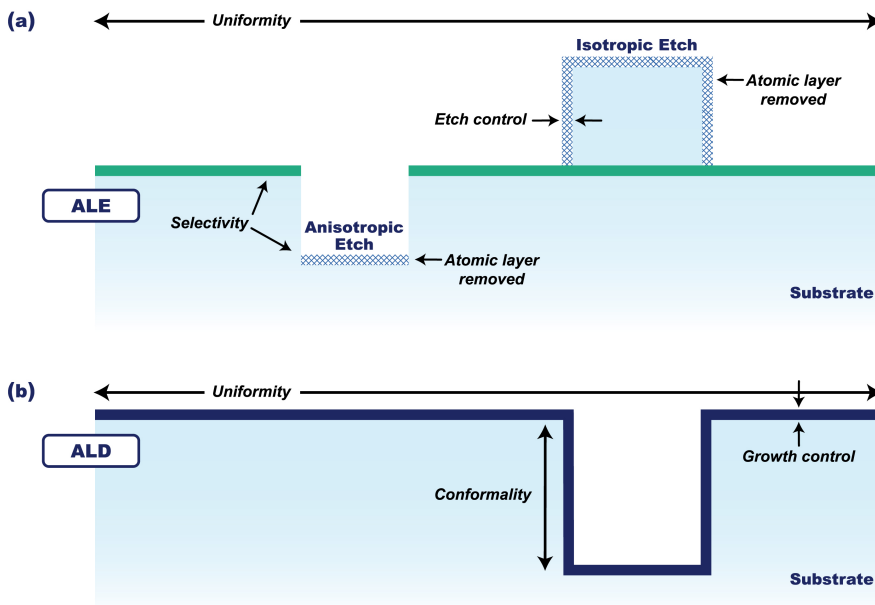
Figure 4. Schematic illustration of the key features for **(a)** atomic layer etching (ALE) and **(b)** atomic layer deposition (ALD). The processes yield a precise control of the thickness etched (etch control) or deposited (growth control) per cycle for ALE and ALD, respectively. The latter holds for the full substrate surface such that the uniformity is excellent. When processing a substrate with three-dimensional features, the situation for ALE and ALD is however different. For ALD, the coverage of three-dimensional features is similar throughout the features and comparable to the planar surface, hence the conformality of ALD-prepared films is excellent. For etching processes such as ALE, there is generally interest in etching vertical features which requires anisotropic processes in which only material is removed from the bottom of the vertical feature. In other cases, isotropic etching can be desired. In this case the material should be etched equally on all exposed surfaces, independent of the orientation of the local surface on the substrate. For ALE, also the selectivity of the etch process is key. Ideally only the to-be-etched material should be removed and not masking materials or materials underlying the to-be-etched material.

generally carried out to create vertical structures such as (high aspect ratio) trenches and holes within the surface region of the substrate and, therefore, anisotropic etch processes are generally employed. The anisotropy is typically achieved by directional processes such as physical sputtering by (plasma-generated) ion beams or by so-called reactive ion etching processes (in all kinds of plasma reactors) in which a physical component is added to a chemical etching process. In this case, the so-called ion-radical synergism[50] leads to significantly enhanced etch rates perpendicular to the substrate surface compared to those occurring parallel to the substrate surface. In this manner, the patterns to be etched can be effectively transferred to the substrate through the pre-defined openings in a hard mask covering the substrate material (see also discussion

about selectivity below). Thus, if the etching of vertical structures is intended, the ALE processes should be designed to have an anisotropic character. This is, e.g., the case for ALE processes in which the co-reactant consists of directional, energetic species such as ions, electrons or energetic atoms from a neutralized ion beam. In the research efforts reported so far (see section 7.2), this has often been the case. However, such anisotropic ("non-conformal") etching is only one possible manifestation of ALE. It can be envisioned that isotropic ("conformal") etching by ALE processes is also imperative for particular situations. This will however impose quite different requirements on the ALE process steps, in particular on the co-reactants used. For example, ALE processes that rely on a co-reactant consisting only of directional species are not an option for isotropic etching. A true "reverse ALD" process is probably more suited for isotropic etching, e.g., an ALE process which is purely thermally driven.[49]

Another aspect that is different for etch and deposition processes is that etch processes are characterized by an additional parameter which, by definition, does not have an equivalent for deposition processes. This parameter is the selectivity of the etch process, which is defined as the ratio between the rate of the layer being etched relative to that of a masking or underlying layer. Selectivity is critical for all etch processes including ALE and it also imposes constraints on the ALE cycles and its process steps. For example, it restricts the energy of ions when these are used as the co-reactant to activate the surface. Their energy should be sufficiently high to activate the to-be-etched surfaces but should be sufficiently low to leave the mask or underlying material intact.[24] This calls for precise ion-energy control under such conditions.

Having addressed the selectivity that needs to be achieved for etch processes based on ALE, it is also interesting to consider the currently increasing interest in area-selective ALD processes[51] and draw parallels here as well. Nanopatterning of films and structures by area-selective ALD in bottom-up processes is receiving growing attention as this could eliminate compatibility issues with top-down etch processes which are associated with the use of etchants, lift-off chemicals or resist films. Therefore, area-selective ALD processes relying on area-deactivation and area-activation (see Figure 5) are currently being explored.[51] However, for cases where incentives exist to restrict to top-down etching, it is interesting to explore area-selective ALE processes as well. Besides traditional masking of the substrate surface (i.e., "selective by surface deactivation"), the surface-controlled ALE processes can potentially also be designed such that one substrate material is etched while other substrate materials are not ("inherently selective"). Another possibility is area-activation ("selective by surface activation"), e.g., by carrying out the activation step during an ALE process (see Figure 3a) only locally by a spatially defined co-reactant exposure, e.g., an focused electron or ion beam. Examples of such processes are illustrated and discussed in Figure 5.
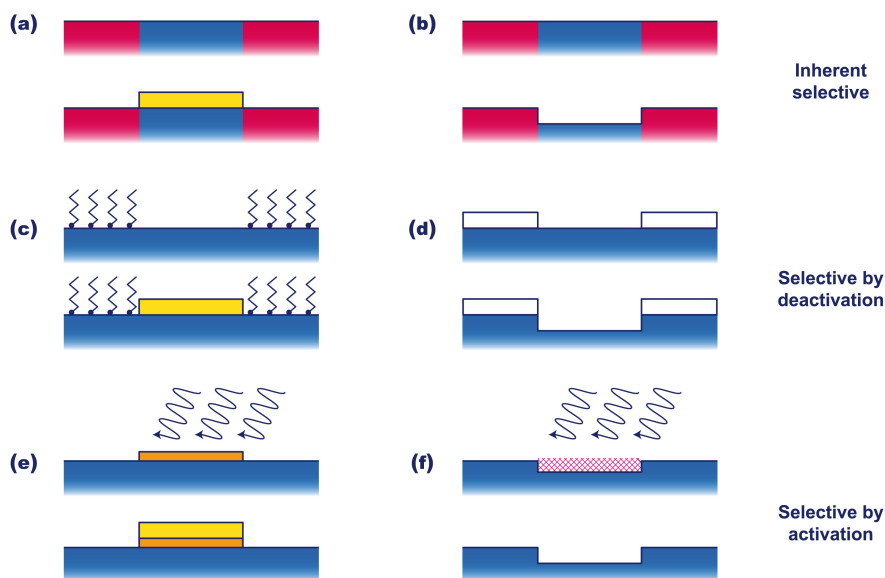
Figure 5. Approaches to realize area-selective ALD [**(a)**, **(c)** and **(e)**] and area-selective ALE [**(b)**, **(d)** and **(f)**]. **(a)** and **(b)** show an approach that can be labeled "inherently selective". The substrate is composed of several materials and on the surface of some of the materials, deposition or etching does (virtually) not occur for the ALD or ALE surface chemistry chosen. The selectivity is therefore, inherent to the specific ALD or ALE process. **(c)** and **(d)** show an approach that can be labeled as "selective by deactivation" since part of the substrate is deactivated by a layer of molecules or a film (mask). No etching or deposition takes place at the parts of the surface that are deactivated. This approach is standard for etching. It is not problematic if the mask material is somewhat etched as long as it etches much slower than the to-be-etched material. **(e)** and **(f)** show an approach that can be labeled "selective by activation". Film growth or etching only initiates on those parts of the surface that are activated, e.g., by a focused electron or ion beam that locally interacts with the surface. For ALD, processes exist in which this activation only needs to be done before the first cycle,[51] for ALE the local activation step needs to take place every cycle. In all the displayed cases for ALD [**(a)**, **(c)** and **(e)**], the area-selective ALD processes depend on an effect known as nucleation delay. The film material easily deposits on some surfaces whereas on other areas, the film hardly nucleates or it takes much longer for the film to nucleate. For area-selective ALE approaches **(b)** and **(d)**, selectivity has the same meaning as that typical for etch processes. The to-be-etched material should etch much faster than any other material used. In **(d)** the selectivity should preferably approach infinity. Furthermore, it is noted that the possibility exists for designing area-selective ALE approaches by combining ALE and ALD. For example, area-selective ALD films can serve as a local mask.

Several challenges for ALE have been discussed in this section. So far, these challenges were mainly process-related and a brief and probably incomplete overview is presented in Table 2. It is evident that it will not be a trivial task to overcome these challenges. At the same time, it has become clear that inspiration can be obtained from

ALD processing and the associated trends and developments within that field. This should also hold particularly for the surface chemistries that need to be developed. At this point it is important to stress that ALD or ALE processes are not necessarily limited to conventional AB-cycles (more precisely: $(AB)_n$ with n being the number of cycles). Also, multistep cycles such as $(ABC)_n$ or supercycles $((A1B1)_m(A2B2)_n)_x$ (with m and n being the number of A1B1 and A2B2 cycles, respectively and x being the total number of supercycles)[48] can be employed (see Figure 6). For ALD, such multistep cycles and supercycles have proven extremely powerful, e.g., in extending the temperature window of ALD processes (e.g., for Pt[52]), improving the properties of ALD-prepared materials (e.g., for Pd[76]), or depositing doped materials (e.g., Al-doped ZnO[53]) or complex oxides (e.g., $SrTiO_3$[54]).

Table 2 also lists some of the challenges for ALE which are equipment-related. Obviously, much like ALD, it is essential that dedicated ALE reactors will need to be developed. These reactors can be optimized for precursor and co-reactant dosing while

Table 2. Prominent challenges for atomic layer etching divided into process-related and equipment-related challenges

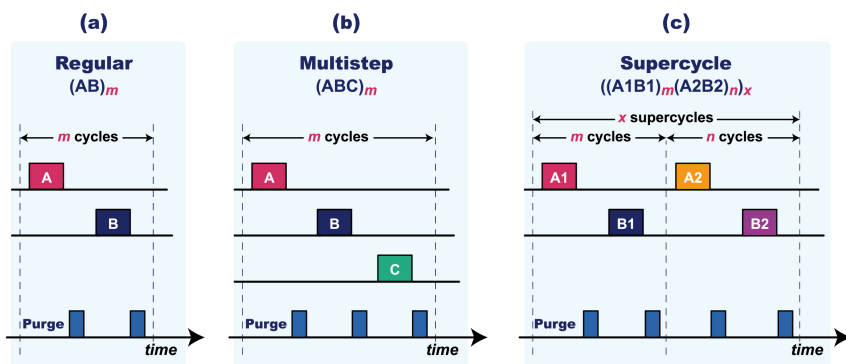| *Process-related* |
| --- |
| - **ALE processes for more material systems** |
| - **More diverse ALE surface chemistries** |
| - **Processes for isotropic and anisotropic ALE** |
| - **Selective-area ALE processes** |
| - **…** |
| *Equipment-related* |
| - **Dedicated ALE reactors** |
| - **Versatile, well-controlled co-reactant sources** |
| - **Process monitoring and control** |
| - **High-throughput methods and reactors** |
| - **…** |

Figure 6. A schematic representation of various types of cycles for ALD[48] that can also be employed for ALE: **(a)** a regular process, **(b)** a multistep process and **(c)** a supercycle process. In a multistep process, one or more additional steps are added to the cycle to form, for instance, an ABC process. In a supercycle, the steps of two regular processes are combined where m cycles of the first process are followed by n cycles of the second process. The variables m and n can be chosen so as to obtain the desired properties for the ALD or ALE process.

at the same time accounting for the design and implementation of versatile co-reactant sources. These co-reactants can be atoms, molecules, ions, electrons and photons, etc., and they can be delivered from the gas phase isotropically or directionally, e.g., using beams. ALE processes based on energetic ions will require accurate ion-energy control, e.g., by incorporating advanced substrate biasing schemes[55] yielding monodisperse ion energies which can be precisely controlled. Note that (advanced) substrate biasing[18] is already at the heart of the technology in plasma etching while it has just entered the field of plasma-enhanced ALD.[56,57] Furthermore, when working with plasma-based co-reactants, process and reactor design should take into account whether or not surface reaction products liberated from the surface during the co-reactant step can be dissociated in the plasma, e.g., by electron-impact. These dissociated reaction products can interact again with the surface and lead to additional etching or (re)deposition. Such effects have clearly been observed for plasma-enhanced ALD processes.[58,59] Next, also equipment-related challenges will exist that are economically driven. A particularly important challenge lies in reaching sufficiently high throughput numbers for the processes. So far, ALE processes suffer from long cycle times, even much more so than many ALD processes. However, at this point inspiration can also be derived from the developments and progresses made in ALD. Approaches such as operating under not-fully saturated conditions to reduce cycle times or resorting to spatial ALE concepts,[46,60,61] similar to spatial ALD processes,[62] can also provide pathways for increasing the throughput of ALE reactors, as illustrated in Figure 7. It goes without saying that eventually, it is the application that will determine the tolerance thresholds
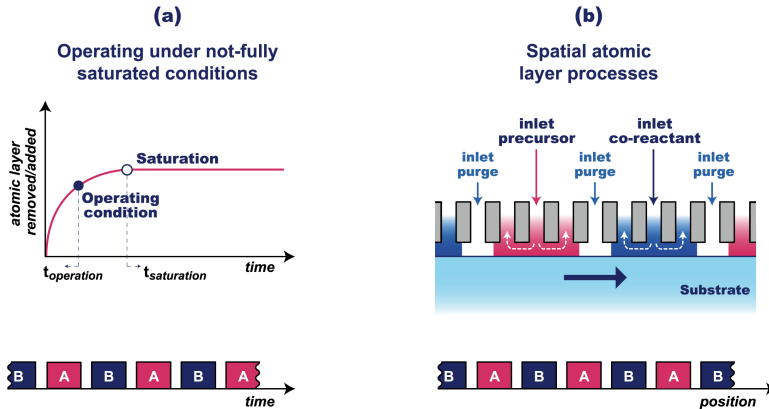
Figure 7. Approaches that are being used to increase the throughput of ALD reactors that in principle can also be adopted for ALE reactors. In **(a)** the approach is shown where the process is not operated under fully saturated conditions. When working with slightly shorter exposure times the cycle time can significantly be reduced (e.g., by a factor of two) while the thickness deposited or removed is only slightly reduced. For many processes and device architectures the level of growth or etch control remains acceptable. In **(b)** the so-called spatial atomic layer process is shown. The cycles are not carried out in the time domain but in the spatial domain. It is noted however, that developing appropriate processes for spatial ALD is not straightforward and this is probably even more so for spatial ALE.

for the processes involved and their parameters, not the fact of whether the processes themselves are strictly ALE or not.

7.4 Conclusions

Atomic layer etching (ALE) is an etch approach that can potentially tackle issues in semiconductor device manufacturing now that critical dimensions are nearing single-digit nanometer values. Being the etch counterpart of the commercially established method of atomic layer deposition (ALD), the aim of this article is to draw parallels between ALE and ALD in order to more precisely define atomic layer etching, to introduce a generalized ALE cycle and to identify similarities and differences between the processes. It is expected that this will be helpful in significantly advancing the field of ALE both through conceptual considerations as well as by practical guidelines and recommendations. ALE has been researched already for over 25 years now, with relatively limited endeavors and successes. However, this does not mean that the progress will remain slow. For ALD, it also took 25 years before the interest in this technology increased explosively owing to the fact that atomic layer precision in deposition became highly necessary. From that point onwards, many breakthroughs in both research and industrial applications were realized. A similar situation seems to

exist at the moment for ALE although the application range of ALE processes will be smaller than that for ALD (the latter having many applications both within and outside the semiconductor industry). Moreover, ALE seems to have process requirements that are less trivial and more demanding. Yet, research on ALE processes and equipment will certainly advance the field of etching even if ideal ALE processes remain unfeasible in the upcoming years. Research on ALE will certainly contribute to etching with more atomic layer precision.

Finally, it is noted that a recently appeared review article by Kanarik *et al.*[63] addresses some similar considerations as presented in this article.

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8

Conclusions & Outlook

The rise of the so-called data economy has led to the need for new logic and memory devices capable of delivering the performance and functionality gains required for data-intensive workloads spanning various applications. The emerging devices and novel device architectures are based on multi-material stacks having nanoscale dimensions and three-dimensional (3D) features. As a result, the fabrication of such devices calls for atomic scale processing techniques – such as plasma-enhanced atomic layer deposition (ALD) and atomic layer etching (ALE) – that can retain precise control over the thickness and properties of functional materials on both planar and 3D substrates. Furthermore, the increase in the quantity and type of materials involved together with the presence of 3D features have raised the complexity of manufacturing such devices. This has led to the need for expanding the current toolbox of materials deposition and etching techniques with novel approaches in selective processing.

This dissertation investigates plasma-enhanced atomic scale processing of functional materials (oxides and nitrides of Ti, Hf and Si) and the role of ions during these processes on both planar and 3D substrate topographies. The following conclusions can be drawn based on the results of this research:

❖ A new plasma ALD process for SiN_x was developed using a mono-aminosilane precursor, DSBAS [$SiH_3N(C_4H_9)_2$], and N_2 plasma. Material properties were analyzed over a wide stage temperature range (100 – 500 $^\circ$C) and compared with those obtained in previous work for SiN_x deposited using a bis-aminosilane precursor, BTBAS [$SiH_2(NH^tBu)_2$)], and N_2 plasma. High quality films were obtained on planar substrates using DSBAS and N_2 plasma, with the best films having a high density ($\sim$3.1 g/cm^3) approaching that of bulk Si_3N_4 and low carbon, oxygen and hydrogen impurity levels at low substrate temperature (<400 $^\circ$C). DSBAS, having one amino ligand and a silyl group, was hypothesized to leave a more amino ligand deficient surface after precursor adsorption compared to BTBAS that has two amino ligands and a silanediyl group. As a result, a lower redeposition effect during the subsequent N_2 plasma step was speculated to occur when using DSBAS as the precursor, which would account for the denser SiN_x films having lower impurity content compared to those obtained in previous work using BTBAS.

❖ SiN_x films were deposited on high aspect ratio (4.5 : 1) 3D trench-shaped nanostructures using DSBAS and N_2 plasma to investigate film conformality and wet-etch resistance (in dilute hydrofluoric acid, HF : H_2O = 1 : 100), relevant for both device fabrication and final device architectures. Film conformality was below the desired levels of >95% and has been attributed to the combined role played by nitrogen plasma soft saturation, radical species recombination and/or ion directionality during SiN_x deposition on 3D substrates. Yet, very low wet-etch rates

(WER ≤2 nm/min) were observed at all trench regions of the most conformal film deposited at low substrate temperature (<400 °C). It demonstrated that the process developed in this work is applicable for depositing high quality SiN_x films on both planar and 3D substrate topographies.

❖ The impact of energetic ions during plasma ALD was demonstrated on planar and 3D substrate topographies. A commercial remote plasma ALD system capable of processing of large-area substrates was equipped with RF substrate biasing for investigating the effects of energetic ions on the growth and material properties of films. The magnitude and the duration/duty cycle of the time-averaged bias voltage applied to the substrate during plasma exposure were demonstrated as parameters influencing ion-surface interactions. Controlling these parameters during film growth had significant material and/or process specific effects that enabled control over a wide range of film properties. An extensive characterization of the effects of substrate biasing was reported for several dielectric or conductive materials, namely oxide and nitride thin-films of Ti, Hf and Si that serve as functional layers for numerous applications. Below the regimes of ion-induced degradation, enhancing ion energies with substrate biasing during plasma ALD led to a significant improvement in the mass density for all materials except SiO_x and SiN_x. The density of SiO_x was slightly improved whereas that of SiN_x degraded as a function of the applied bias. A higher mass density was generally accompanied by an increase in the optical refractive index of dielectric films while a lower mass density showed the opposite trend. Growth of denser materials with biasing was also observed to yield compact films with a void-free microstructure while the growth of under-dense materials generally led to an increase in the void content.

❖ Plasma ALD of TiO_x and HfO_x on a grounded substrate at 150 °C yielded mainly amorphous films. However, implementing substrate biasing during deposition led to the formation of polycrystalline material corresponding to the rutile and monoclinic phases of TiO_x and HfO_x, respectively. These are crystalline phases that are normally obtained either by using high temperature deposition environments or by using special substrate materials that have crystal lattice parameters comparable to the deposited film. The results demonstrated that enhancing ion energies by substrate biasing during plasma ALD of such transition metal oxides enable crystalline film growth even at low temperatures and also without the need for any special substrates. Substrate biasing during plasma ALD drastically reduced the resistivity of conductive TiN_x and HfN_x films by one and two orders of magnitude, respectively. A high oxygen impurity content was generally observed in such transition metal nitride films when they were deposited without substrate biasing. The oxygen impurity content was significantly reduced ($\leq$ 4 atomic %) when

the films were grown with biasing during plasma exposure, which contributed in lowering the electrical resistivity. Furthermore, substrate biasing during plasma ALD enabled the residual stress of the four transition metal compounds to be altered from tensile to compressive. The compressive residual stress of SiO_x remained fairly unchanged with biasing while the compressive stress of SiN_x decreased as a function of the applied bias.

❖ Substrate biasing during plasma ALD of films on 3D trench-shaped nanostructures induced differing material properties simultaneously at different surface orientations (i.e., vertical sidewall, planar top and bottom surfaces) of the 3D substrate. This phenomenon was attributed to the directional nature of energetic ions during plasma exposure with substrate biasing. Directional ions impinge on the planar trench surfaces (aligned perpendicular to the ion flux) with much more energy than on the vertical trench sidewalls (aligned parallel to the ion flux) during deposition with substrate biasing. Consequently, films grow at the planar surfaces under the influence of highly energetic ions during substrate biasing, while the sidewall regions being devoid of energetic ion bombardment provide growth conditions resembling those on a grounded substrate. For TiO_x and HfO_x deposited at a low temperature of 150 °C, biasing led to phase-selective growth of crystalline material on planar surfaces and amorphous material on vertical sidewalls of the 3D trenches. For SiN_x, biasing led to microstructure-selective growth of low density films on planar surfaces and high density films on the vertical sidewalls of the 3D trench nanostructures. The low density SiN_x was subsequently removed in a selective manner from the planar regions after wet-etch treatment in dilute HF while the high density SiN_x at the vertical sidewalls remained intact. These results demonstrated how substrate biasing during plasma ALD on 3D substrates enables a new approach for topographically selective processing.

❖ Ion energy and flux characteristics were investigated for grounded and RF biased substrates during plasma exposure to investigate their role in tailoring material properties during plasma ALD. Ion flux-energy distribution functions (IFEDFs) of reactive plasmas (O_2, H_2, N_2) typically used for plasma ALD were measured in a commercial remote plasma ALD system equipped with RF substrate biasing. IFEDFs were obtained using a gridded retarding field energy analyzer (RFEA) and the effect of varying ICP power, pressure and bias conditions on the ion energy and flux characteristics of the three reactive plasmas were investigated. The properties of three materials – TiO_x, HfN_x and SiN_x – deposited using these three plasmas were investigated on the basis of the energy and flux parameters derived from IFEDFs. The material properties were analyzed in terms of the total ion energy dose delivered to a growing film in every ALD cycle, which is a product of the mean ion

energy, the total ion flux and the plasma exposure time. The properties responded differently to the ion energy dose depending on whether it was controlled with RF substrate biasing where ion energy was enhanced, or without any biasing where plasma exposure time was increased. This indicated that material properties were influenced by whether or not ion energies exceeded energy barriers related to physical atom displacement or activation of ion-induced chemical reactions during plasma ALD. Furthermore, once ion energies were enhanced beyond these threshold barriers with RF substrate biasing, material properties became a function of both the enhanced ion energy and the duration for which the ion energy was enhanced during plasma exposure. These results have led to a better insight into the relation between energetic ions and the ensuing material properties, e.g., by providing energy maps of material properties in terms of the ion energy dose during plasma ALD. Such analyses provide a new approach for investigating materials grown using plasma ALD and can serve as a platform for synthesizing nanoscale films with the desired material properties.

❖ Current trends in device manufacturing and the advent of 3D device architectures call for processing techniques that are able to add and/or remove functional materials precisely and selectively at the atomic level. As a result, there is a re-emerging and fast growing interest in atomic layer etching (ALE), which is the so-called etch counterpart of ALD. Past research efforts on ALE have been reviewed and the key defining characteristics of this technique have been identified in this dissertation. These include cyclic step-wise processing, self-limiting surface chemistry, repeated removal of atomic layers (not necessarily a full monolayer) of the material, and the presence or absence of directional species that lead to anisotropic or isotropic ALE processes, respectively. Furthermore, parallels were drawn between ALE and ALD in order to facilitate a better understanding of the precision and selectivity of ALE, introduce a generalized ALE cycle and identify similarities and differences between the two processes. It is expected that this will assist in significantly advancing the field of ALE, both through conceptual considerations as well as by highlighting practical guidelines and recommendations.

Based on the findings reported in this dissertation, some recommendations can be made for conducting further research in the following directions:

❖ When SiN_x was grown on 3D substrates with the ALD process developed in this work using an organosilane precursor, DSBAS, and N_2 plasma, the films were of a high quality (in terms of a high wet-etch resistance) but a low conformality. On the other hand, SiN_x ALD processes employing chlorosilane precursors and NH_3 gas or NH_3 plasma report films having high conformality but low film quality (i.e., low density

or wet-etch resistance).[1–3] In this regard, a SiN$_x$ ALD process that makes use of two co-reactant exposure steps where one supplies both nitrogen and hydrogen species while the other provides only nitrogen species could potentially yield films that are both conformal and wet-etch resistant on 3D substrates. This could be performed, for instance, in a three-step SiN$_x$ ALD process consisting of an organosilane precursor dose as the first step, followed by either an NH$_3$ gas, NH$_3$ plasma or mixed N$_2$/H$_2$ plasma exposure as the second step and an additional N$_2$ plasma exposure as the third step.

❖ Substrate biasing during plasma ALD has so far been implemented in the second step of a two-step ALD process cycle, i.e., during the *B* step of an (*AB*)$_n$ process where *n* is the number of cycles. It could very well be implemented in multistep plasma ALD processes, such as during the third *C* step of an (*ABC*)$_n$ cycle or an [(*AB*)$_x$*C*]$_n$ supercycle, where *x* is the number of *AB* cycles completed before the *C* step is performed and *n* is the number of supercycles. Furthermore, substrate biasing during plasma ALD has thus far been performed using reactive plasmas where enhancing ion energies result in combined physicochemical processes during film growth. Using an inert plasma (e.g., Ar) in the *C* step of the aforementioned multistep cycles and applying a bias only at that step could in principle, lead to purely physical effects during energetic ion bombardment. Such purely physical processes could induce differences in the trends of material property variation as a function of substrate biasing.

❖ Multistep plasma ALD supercycles have been used to deposit layered film stacks (or nanolaminates[4]) that rely on the differences in properties of the individual layers. These differences are generally procured by growing at least two different materials alternately for the stacked layers. Since enhanced ion energies during plasma ALD can tailor the properties of a given material, stacked layers with different properties using the same material could in principle, be created by growing one layer without and the next layer with substrate biasing. This technique could also be employed for growing films on sensitive substrates that cannot withstand the effects of enhanced ion energies. Deposition with biasing can be carried out only after initially performing some plasma ALD (or even thermal ALD) cycles without any biasing on such substrates. This could, in principle, lead to energetic ion-surface interactions on the initial layer of the deposited film and not on the substrate (provided the initially grown layer is of a sufficient thickness).

❖ Substrate biasing during plasma exposure can be implemented as pre- or post-deposition treatment steps which, based on the reactants used and the treatment duration, can modify surface or sub-surface regions (i.e., a few monolayers below

the surface). This can enable in-situ surface functionalization that can either promote or inhibit film growth, thereby having potential applications in area-selective deposition. For the case of substrate biasing applied in an interleaved manner in the plasma step (i.e., during a part of the plasma exposure time), another aspect that could potentially influence material properties is variation of the moment at which the bias is applied. For instance, a 50% bias duty cycle can be implemented in a 10 s plasma step by applying it for 5 s during either the first, middle or last half of the plasma exposure time. Simultaneous ignition of the plasma and the bias could lead to the cracking of bulky ligand species (e.g., amino, cyclopentadienyl, isopropoxide, etc.) remaining on the surface after precursor adsorption by the impact of high energy ions. This could lead to the incorporation of decomposed ligand species in the growing film and elevate film impurity content. Therefore, a means to prevent this could be to apply the bias near the end of the plasma exposure step as used in this work which should, in principle, lead to a cleaner or more ligand-free surface before the impingement of energetic ions.

❖ During plasma ALD of TiN_x in this work, the Ti−N bonds in the deposited film originated from Ti−N bonds present in the TDMAT precursor. Substrate biasing during the subsequent reducing $Ar+H_2$ plasma step influenced material composition by lowering oxygen content that could have originated from background impurities in the vacuum environment. The decrease in oxygen content enabled by substrate biasing during a reducing plasma could, in principle, be applicable for varying the composition of metal oxide films deposited with precursors containing metal−O bonds. It was recently reported that sub-stoichiometric TaO_x films could be obtained by plasma ALD using $Ta(OC_2H_5)_5$ as the precursor (that already contained Ta−O bonds) followed by a reducing $Ar+H_2$ plasma.[5] This process scheme led to the incorporation of oxygen vacancies in the metal oxide film during deposition. In this regard, it can be speculated that enhancing ion energies during the reductive plasma step could potentially lead to *in-situ* control over the amount of generated oxygen vacancies. Therefore, plasma ALD with substrate biasing could be a technique for growing sub-stoichiometric metal oxide layers with a tunable chemical composition.

❖ For SiN_x grown on 3D trench-shaped nanostructures using N_2 plasma with substrate biasing (at low pressure that formed a collisionless plasma sheath), the low density films formed only at the planar substrate regions were selectively removed by a wet-etch treatment in dilute HF performed after deposition. This led to the formation of SiN_x films only at vertical sidewalls. Another approach for obtaining SiN_x films selectively at the sidewalls without breaking vacuum could be achieved by the use of a dry-etch treatment step (e.g., using SF_6 plasma). This can be

implemented either after deposition or during the ALD process itself, e.g., in a three-step ALD process consisting of a precursor dose as the first step, followed by N_2 plasma with substrate biasing as the second step and an SF_6 plasma exposure (without biasing) as the third step.

❖ The ability to conduct topographically selective processing on 3D substrates could in principle, be altered (removed) by controlling (lowering) the directionality and/or energy of the ions. When substrate biasing is implemented in a collisional plasma sheath that can be obtained at higher pressure conditions (e.g., > 100 mTorr) than those of this work, both the directionality and the energy of the ions are affected. At these conditions, the ion mean free path becomes smaller than the thickness of the plasma sheath causing the ions to experience collisions with gas-phase species while crossing the sheath. As a result, the energy of ions impinging on planar substrate surfaces can become considerably lower than the voltage drop across the plasma sheath. The gas-phase collisions could also lead to the impingement of both ions and radicals on the vertical surfaces of a 3D structure. Depending on the pressure and magnitude of the applied bias during plasma exposure, the energy of the ions and radicals colliding with sidewalls could in principle, be higher than those colliding with the sidewalls in a nearly collisionless plasma sheath. This could have direct implications on the conformality and material properties of films deposited on 3D substrates and therefore, warrants further investigation.

❖ The results of this work signify how energy thresholds < 100 eV related to material atom displacement or activation of ion-induced chemical reactions are parameters relevant for both plasma ALD and ALE performed under the influence of energetic ions. Further investigation for better determination of such ion energy thresholds can be carried out by implementing tailored (or pulse-shaped) instead of sinusoidal RF bias voltage waveforms during plasma exposure. The tailored bias voltage waveforms are known to generate ions having narrow (or mono-modal) flux-energy distribution functions which would enable accurate measurement of ion energy thresholds.[6] Implementing such tailored bias voltage waveforms could also open new pathways for conducting selective plasma ALD and ALE.

❖ For most area-selective ALD approaches, it is extremely challenging to achieve a high selectivity. In reality, area-selective ALD will often need to be combined with a selective etching process as a correction step to increase the overall selectivity to the required level.[7] When incorporating selective etching, it is preferable to use an ALE process such that the merits of ALD (e.g., atomic scale control, high uniformity on large-area substrates, high conformality on 3D substrates, etc.) are retained. When using an ALE process, the self-limiting behavior of the ALE reactions ensures

that the same amount of material is etched uniformly on the growth area. A straightforward approach for combining area-selective ALD and ALE is to develop supercycle recipes, e.g., $[(AB)_x(CD)_y]_n$ where x number of AB cycles for area-selective ALD can be followed by y number of CD cycles for ALE to give n number of supercycles for the combined process. Since undesired etching of material on the growth area can also take place during such supercycles, ALE processes should preferably be developed yielding a higher etch rate for the material formed on the non-growth area (e.g., individual nuclei or islands) compared to that for the continuous layer formed on the growth area. Or in other words, from an ideal perspective, only etching of material on the non-growth area should occur. For this case, the implementation of an ALE correction step after every ALD cycle may very well lead to area-selective ALD.

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Summary

As we enter an era of atomic scale device dimensions, it has become imperative to utilize deposition and etching techniques that allow for processing materials at the atomic level. Furthermore, next-generation devices consist of various material layers across both planar and three-dimensional (3D) layouts which has led to an additional need for processing materials in a selective manner. As a result, it is now vitally important to retain proper control over the thickness and properties of materials grown or removed during fabrication of nanoscale devices with 3D geometries. Plasma-enhanced atomic layer deposition (ALD) has obtained a prominent position in synthesizing ultra-thin films of functional materials with atomic scale precision. Uniform and conformal film deposition even on challenging 3D substrate topographies can be attained by virtue of the sequential and self-limiting precursor and plasma exposure steps of plasma ALD. Highly reactive plasma radicals are generated during the plasma step and the contribution of these electrically neutral species toward film growth is a well-known feature of plasma ALD. However, the ions generated during plasma exposure can also play a significant role in the deposition process which has been relatively less explored. Furthermore, the challenges related to current plasma based dry-etching processes provide a window of opportunity for being potentially tackled by the etch counterpart of ALD, i.e., atomic layer etching (ALE). This dissertation investigates plasma-enhanced atomic scale processing of functional materials and the role of ions during these processes on planar and 3D substrate topographies, relevant for next-generation device technologies.

   In the first part of this work, a new ALD process for SiN_x was developed using a novel organosilane precursor (DSBAS) and N_2 plasma. Dense and wet-etch resistant SiN_x films that can be synthesized at low temperatures serve as spacers or encapsulation layers for protecting sensitive device components; e.g., gate stacks in 3D transistors or magnetic tunnel junctions in emerging magnetoresistive memories. SiN_x films with a high density and low impurity content were obtained at low substrate temperatures on planar substrates using the process developed in this work. Deposition were also performed on high aspect ratio 3D trench nanostructures to investigate SiN_x film conformality and wet-etch resistance. Sources limiting conformality on 3D substrates were attributed to factors occurring in the N_2 plasma step. Identification of factors associated with plasma processing conditions is a prerequisite for addressing the challenge of growing conformal SiN_x on 3D substrates. Yet, very low wet-etch rates were observed at different regions throughout the trenches, confirming high quality

SiN$_x$ could be grown at low substrate temperature on 3D substrates using the developed process.

Next, the effects substrate biasing during plasma ALD on the properties of materials (oxides and nitrides of Ti, Hf, and Si) grown on planar and 3D substrate topographies were investigated. A commercial 200-mm remote plasma ALD system equipped with RF substrate biasing was used to control the ion energy during the plasma exposure step. This technique was demonstrated to significantly enhance the versatility of plasma ALD processes by providing additional knobs for controlling a wide range of material properties, appropriate for numerous applications. Substrate biasing during plasma ALD increased the refractive index and mass density of TiO$_x$ and HfO$_x$ and enabled control over their crystalline properties. Plasma ALD of these oxides with substrate biasing formed crystalline films at a low temperature which would otherwise yield amorphous films without biasing. Substrate biasing drastically reduced the resistivity of conductive TiN$_x$ and HfN$_x$ films. Furthermore, biasing enabled the residual stress of these materials to be altered from tensile to compressive. The properties of SiO$_x$ were slightly improved whereas those of SiN$_x$ were degraded as a function of substrate biasing. Plasma ALD on 3D trench nanostructures with biasing induced differing film properties at different regions of the 3D substrate which demonstrated the potential of this technique in enabling new approaches for topographically selective deposition.

Ion energy characteristics on grounded and biased substrates during plasma exposure were also measured to investigate their role in tailoring material properties. Insights from such measurements are essential toward understanding how a given plasma ALD process at different operating conditions can be influenced by energetic ions. Ion flux-energy distribution functions (IFEDFs) were measured using a retarding field energy analyzer for reactive plasmas typically used in plasma ALD (O$_2$, H$_2$, N$_2$) without and with RF biasing. The properties of materials (TiO$_x$, HfN$_x$, SiN$_x$) grown using these plasmas were analyzed as a function of the ion energy and flux parameters derived from IFEDFs. These results have provided more insight on the relation between energetic ions and the ensuing material properties, e.g., by providing energy maps of material properties in terms of the ion energy dose during plasma ALD. They demonstrate how the measurement and control of ion energy characteristics during plasma ALD provide a platform for synthesizing ultra-thin films with the desired properties.

In the final part of this work, past research efforts on ALE were reviewed and the key defining characteristics of ALE identified. These include cyclic step-wise processing, self-limiting surface chemistry, repeated removal of atomic layers (not necessarily a full

monolayer) of the material, and the presence or absence of directional species that lead to anisotropic or isotropic ALE processes, respectively. Subsequently, further parallels were drawn with the more mature and mainstream technology of ALD from which lessons and concepts were extracted that can be beneficial for advancing the field of ALE.

To conclude, this dissertation elucidates important aspects associated with plasma-enhanced atomic scale processes that provide deeper insight on the fundamental and technological opportunities afforded by these techniques, relevant for future 3D device architectures. It serves to exemplify how the properties of functional materials can be tailored by accurate control and optimization of plasma based processing conditions.

Author contributions

The contents of this dissertation are the outcome of original work conducted by the author (T. Faraz). Nevertheless, this work was carried out in collaboration with individuals from academic and industrial institutions. Their contributions are stated below:

- M. van Drunen (TU/e) and the author (T. Faraz) contributed equally to the ALD process development of SiN_x in chapter 4.
- I. Buchanan (Air Products) and A. Mallikarjunan (Air Products) provided the DSBAS precursor for ALD of SiN_x.
- W.A. Bik (Acctec B.V.) contributed to the RBS measurements.
- M. Verheijen (Philips Innovation Services) contributed to the plan-view HAADF-STEM measurements.
- D.M. Hausmann (Lam Research) and J. Henri (Lam Research) provided the 3D trench-shaped nanostructures for cross-sectional TEM measurements conducted by Nanolab Technologies Inc.
- A. O'Mahony (Oxford Instruments) contributed to the SE measurements on large-area 200 mm wafers.
- C.A.A. van Helvoirt (TU/e) contributed to the XRD measurements
- S. Karwal (TU/e) contributed to the measurements of HfN_x datasets.
- A. Sharma (TU/e) contributed to the measurements of HfO_x datasets.
- V. Beladiya (Friedrich Schiller University Jena) contributed to the XRR and wafer curvature measurements conducted in the research group of A. Szeghalmi (Friedrich Schiller University Jena).

List of publications

Peer-reviewed articles

1) **T. Faraz**, K. Arts, S. Karwal, H.C.M. Knoops, W.M.M. Kessels, "Energetic Ions during Plasma-Enhanced Atomic Layer Deposition and their Role in Tailoring Material Properties" *Plasma Sources Science & Technology* 28, 024002 (2019)

2) **T. Faraz**, H.C.M. Knoops, M.A. Verheijen, C.A.A. van Helvoirt, S. Karwal, A. Sharma, V. Beladiya, A. Szeghalmi, D.M. Hausmann, J. Henri, M. Creatore, W.M.M. Kessels, "Tuning material properties of oxides and nitrides by substrate biasing during plasma-enhanced atomic layer deposition on planar and 3D substrate topographies" *ACS Applied Materials & Interfaces* 10, 13158–13180 (2018)

3) **T. Faraz**, M. van Drunen, H.C.M. Knoops, A. Mallikarjunan, I. Buchanan, D.M. Hausmann, J. Henri, W.M.M. Kessels, "Atomic layer deposition of wet-etch resistant silicon nitride using Di(sec-butylamino)silane and N_2 plasma on planar and 3D substrate topographies" *ACS Applied Materials & Interfaces* 9, 1858–1869 (2017)

4) **T. Faraz**, F. Roozeboom, H.C.M. Knoops, W.M.M. Kessels, "Atomic layer etching: what can we learn from atomic layer deposition?" *ECS Journal of Solid State Science & Technology* 4, N5023–N5032 (2015)

5) H.C.M. Knoops, **T. Faraz**, K. Arts, W.M.M. Kessels, "Status and prospects of plasma-assisted atomic layer deposition" *Journal of Vacuum Science & Technology A* 37, 030902 (2019)

6) S. Karwal, M.A. Verheijen, B.L. Williams, **T. Faraz**, W.M.M. Kessels, M. Creatore, "Low resistivity HfN_x grown by plasma-assisted ALD with external rf substrate biasing*" RSC Journal of Materials Chemistry C* 6, 3917–3926 (2018)

7) S. Karwal, M.A. Verheijen, K. Arts, **T. Faraz**, W.M.M. Kessels, M. Creatore, "Plasma-assisted ALD of highly conductive HfN_x: On the effect of energetic ions on film microstructure*" To be submitted*

8) V. Beladiya, **T. Faraz,** W.M.M. Kessels, A. Tünnermann, A. Szeghalmi , "Controlling mechanical, structural and optical properties of Al_2O_3 thin films deposited by plasma-enhanced atomic layer deposition with substrate biasing" *Proceedings of*

SPIE, Advances in Optical Thin Films VI (Volume 10691), Frankfurt, Germany, 14 – 17 May 2018

9) J. Palmans, **T. Faraz**, M.A. Verheijen, W.M.M. Kessels, M. Creatore, "Nucleation of microcrystalline silicon: on the effect of the substrate surface nature and nano-imprint topography" *Journal of Physics D: Applied Physics* 49, 055205 (2016)

Popular science articles

1) **T. Faraz**, H.C.M. Knoops, W.M.M. Kessels, "Ion energy control during plasma-enhanced atomic layer deposition: Enabling materials control and selective processing in the third dimension" *NEVAC Blad* 57, 6-10 (2019)

2) **T. Faraz**, "Topographically selective processing – Taking selectivity up a notch by processing in the 3rd dimension" *Atomic Limits Blog*, Feb 2019

List of conference presentations

1) *Invited oral presentation* at the upcoming 236th ECS Meeting, 13 – 17 Oct 2019, Atlanta, Georgia, U.S.A., titled "Expanding the Toolbox of Atomic Scale Processing: From Materials Control to Selective Processing By Plasma ALD"

2) *Oral presentation* at the 2019 NEVAC Day, 17 May 2019, Nijmegen, the Netherlands, titled "Ion energy control during plasma-enhanced atomic layer deposition: Enabling materials control and selective processing in the third dimension"

3) *Oral presentation* at the 65th AVS International Symposium, 21 – 26 Oct 2018, Long Beach, California, U.S.A., titled "Ion energy characteristics during plasma-enhanced atomic layer deposition and their role in tailoring material properties"

4) *Oral presentation* at the 18th International Conference on Atomic Layer Deposition, 29 July – 1 Aug 2018, Incheon, South Korea, titled "Energetic ions during plasma ALD and their role in tailoring material properties"

5) *Oral presentation* at the 64th AVS International Symposium, 29 Oct – 3 Nov 2017, Tampa, Florida, U.S.A., titled "Ion energy control during remote plasma-ALD for tuning material properties of transition metal nitrides"

6) *Oral presentation* at the 17th International Conference on Atomic Layer Deposition, 15 – 18 July 2017, Denver, Colorado, U.S.A., titled "Tuning material properties by ion energy control during remote plasma ALD on planar and 3D substrates"

7) *Oral presentation* at the 19th EU-Regional Workshop on the Exploration of Low Temperature Plasma Physics, 1 – 2 Dec 2016, Kerkrade, The Netherlands, titled "Substrate biasing during plasma-enhanced atomic layer deposition: On the role of ion energy control on planar and 3D substrates"

8) *Oral presentation* at the 63rd AVS International Symposium, 6 – 11 Nov 2016, Nashville, Tennessee, U.S.A., titled "Substrate Biasing during Remote Plasma-ALD on Planar and 3D Substrates"

9) ***Oral presentation*** at the 16th International Conference on Atomic Layer Deposition, 24 – 27 July 2016, Dublin, Ireland, titled "ALD of high quality SiN_x using DSBAS + N_2 plasma on planar and 3D substrates"

10) ***Poster presentation*** at the 15th International Conference on Atomic Layer Deposition, 28 June – 1 July 2015, Portland, Oregon, U.S.A., titled "Substrate biasing on a 200 mm remote plasma ALD system"

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"Well, here at last, dear friends, on the shores of the sea comes the end of our fellowship" – *Gandalf the Grey* at the end of *Lord of the Rings.*

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"For even the very wise cannot see all ends"

Tahsin Faraz
May 2019

About the author

Tahsin Faraz was born on 29 May 1987 in Dhaka, Bangladesh. In 2007, he enrolled at BRAC University in Bangladesh to pursue a B.Sc. in Physics + Electronics & Communication Engineering (double major). Tahsin graduated with honours (highest distinction) in 2011 and was awarded the Vice Chancellor's Gold Medal for obtaining the highest CGPA in physics. During the five years of his undergraduate studies, Tahsin was awarded a merit based full tuition fee waiver scholarship. He was also awarded an Erasmus Mundus scholarship to participate in a ten month study abroad programme during his undergraduate studies. This was carried out at the University of Nice Sophia Antipolis in France where Tahsin conducted research on his Bachelor's thesis in the field of optics and laser physics.

In 2012, Tahsin enrolled in a two year joint Master's programme in Environomical Pathways for Sustainable Energy Systems (SELECT). He spent the first year of his graduate studies at the Royal Institute of Technology (KTH) in Sweden and the second year at the Eindhoven University of Technology (TU/e) in the Netherlands. Tahsin conducted research on his Master's thesis in the department of Applied Physics at TU/e where he specialized on plasma-enhanced chemical vapour deposition for thin film solar cells. He was also awarded an Erasmus Mundus scholarship for the two years of his graduate studies.

After receiving his M.Sc. in 2014, Tahsin became a PhD candidate in the department of Applied Physics at TU/e in the same year. His doctoral research focused on plasma based atomic scale processing techniques (atomic layer deposition/etching) for next-generation nanoelectronic device technologies, the results of which are presented in this dissertation. In 2018, he received the John Coburn & Harold Winters award at the 65th AVS International Symposium (California, USA) for "*the best presentation and outstanding original research in plasma science*". In 2019, he was awarded the NEVAC Prize for "*the best research article related to vacuum technology*". In addition, Tahsin has been invited to give presentations on his research at the 2019 NEVAC Day (Nijmegen, the Netherlands) and at the 236th ECS Meeting (Georgia, USA). Since 2019, he is working as a post-doctoral researcher in the department of Applied Physics at TU/e.