Wireless receiver architectures towards 5G

Wireless Receiver Architectures Towards 5G: Where Are We?

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***Abstract*—With 5G posing different requirements to the mobile (handset) receiver than earlier generations, the receiver architecture needs to be carefully reconsidered. However, an up-to-date and complete overview is not yet available in literature. In this paper such a review of the currently available receiver architectures is provided, as well as an overview of current trends. For the first time, a framework is introduced that allows a systematic classification of architectures. An identification of unexplored possibilities and system-level trade-offs follows. A more flexible, low-power and high-performance receiver architecture than currently applied is needed for 5G, for which this framework becomes a useful tool.**

***Index Terms*—5G, Handset Receivers, Receiver Architectures, Review, Wireless Communication**

I. Introduction

THE choice of wireless receiver (Rx) architecture is a critical step in the mobile (handset) receiver design process. Among others, it sets the requirements for individual components such as duplexers, filters, Low Noise Amplifiers (LNAs), Mixers and Analog-to-Digital (A/D) Converters (ADCs) for a given overall system specification. These requirements lead indirectly to a certain level of integration, flexibility, power consumption and cost. With 5G imposing different requirements than earlier generations, an even more careful consideration is required. In the face of the desired flexibility in 5G the question arises whether the approaches currently taken in handset receivers remain viable or a new approach is needed.

In order to make a justified choice of architecture for a 5G handset, a clear overview of the main architectures that have so far been proposed is needed together with their advantages and disadvantages. While several papers [1]–[8] and books [9]–[14] provide a partial overview, to the best of the authors' knowledge no complete and up-to-date overview is available. In this paper, such an overview is presented, focusing on the sub 6-GHz frequency range, which contains over 50 bands for LTE [15] and WiFi [16], and will also be of relevance for 5G [17]–[19]. The particular challenges of receivers for the millimeter-wave bands (e.g. [20], [21]) are not included, since they would warrant a paper of their own. While similar concepts apply to transmitter architectures, this paper focuses on receivers in order to present a clear and insightful story, as different considerations apply to transmitters. Also for the first time, a systematic framework to classify the receiver architectures is proposed. It allows useful insights into the interrelations between different architectural approaches, and the architectural trade-offs that affect system-level performance. Using this overview and framework of architectures, current trends are illustrated and discussed in view of the expected requirements of 5G for handset receivers.

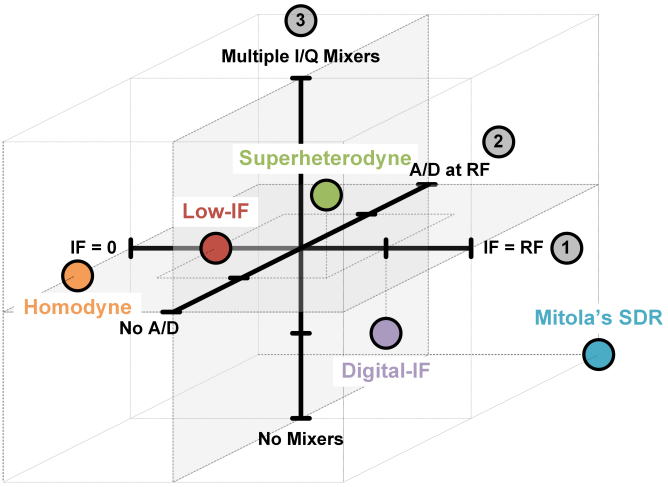


Fig. 1. Proposed framework, where the most commonly discussed receiver architectures are indicated. 2-Dimensional projections of this 3-Dimensional representation are given in Fig. 2.

This paper is organized as follows: the new framework is presented in Section II including the design trade-offs, and a short overview of the architectures in the framework is given. A more in-depth overview of each architecture, its (dis)advantages and developments follows in Section III. In Section IV trends in the development and use of architectures are identified, and discussed with respect to 5G. Finally, a conclusion is given in Section V.

II. Framework

While 5G will definitely bring changes to the physical layer when compared to 4G and earlier generations, and therefore impact the receiver requirements, there is no doubt that it will have to receive a high frequency signal and reconstruct the data that was transmitted. There will be an antenna at the input and data at the output, not changing the receiver functionality from a system level point of view. Therefore a framework can be based around the main functionalities that are currently needed for a receiver: downconversion and analog-to-digital conversion.

In Fig. 1 the proposed framework is shown. To the authors' best knowledge, this is the first time such a framework is attempted. In principle, it represents the design space of receiver architectures, i.e. it illustrates the degrees of freedom when defining a receiver architecture. It is constructed to allow a classification of the common receiver architectures, making

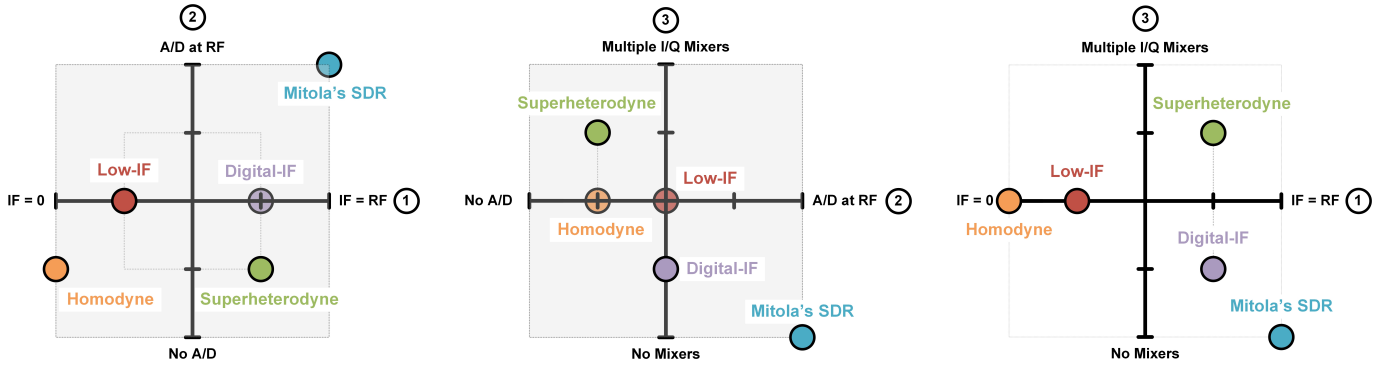


Fig. 2. 2-Dimensional projections of the proposed framework: (a) dimensions 1 and 2, (b) dimensions 2 and 3 and (c) dimensions 1 and 3. The 3-Dimensional view is given in Fig. 1.

their similarities and differences clear on an abstract level, and allowing one to display developments and trends in a graphical manner. Three dimensions (as indicated in Fig. 1) are considered. One key advantage of using this framework is that each dimension reflects an overall functionality and design freedom of a receiver:

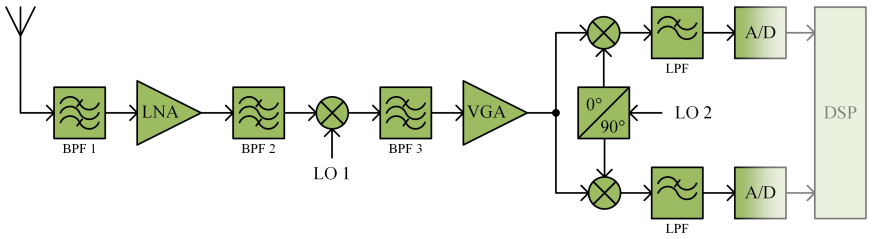
1) ***Intermediate Frequency (IF)***, ranging from IF = 0 to IF = RF. In most designs the signal is downconverted from its carrier frequency f_c to an intermediate frequency (IF, f_i) using (a) mixer(s). The IF to which the mixers translate the signal is an essential parameter, indicated in dimension 1.
2) ***Location of A/D Conversion***, ranging from no A/D (which implies analog decoding), through A/D at a low frequency, to A/D conversion at RF (e.g. directly after the antenna). In order to transfer the information to the digital domain, an ADC is always required. The location where the ADC is placed in the cascade, dimension 2 in the framework, defines the boundary between functionalities that have to be implemented in the analog domain and which can be implemented in the digital domain.
3) ***Mixing complexity***, ranging from no analog mixers to the use of multiple stages of analog I/Q mixing. The amount of cascaded mixers and whether I/Q mixing is used or not is indicated in dimension 3 in our framework.

Moving up in dimension 1 in the framework means an increase in the IF. Therefore the designer has more freedom in the design if a second down-conversion stage is applied, or the opportunity for increased bandwidth or additional digital signal processing if the ADC is placed at the first IF. Both options can increase performance, at the same time increasing cost and power consumption due to the added components and/or the need for a higher-performance ADC. In addition, a higher IF results in increased power consumption and circuit design challenges due to the increased frequency. An increase in dimension 2 corresponds to increasing the sampling frequency of the ADC and, thus, increases the flexibility in the digital domain since a larger bandwidth is digitized. This comes at the cost of increasing A/D conversion power consumption and cost, but relieves the filtering requirements in the analog domain. It also implies an increased bandwidth for the analog components, resulting in an increased linearity requirement since not all undesired signals can be filtered out. Moving up in dimension 3 means either an analog implementation of the in-phase and quadrature branches, or the use of multiple IF stages. Both possibilities increase the complexity and number of components in the analog domain, but provide more freedom in the frequency planning. Note that not all locations in the framework can be practically achieved, preventing some trade-offs from being made and some of the extremes from being reached. An example of this is Mitola's SDR.

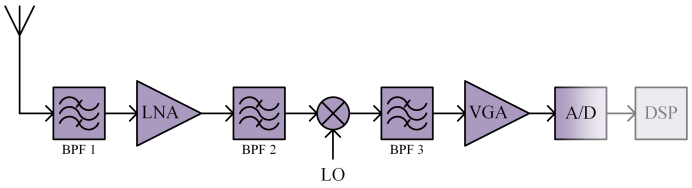
Together, the dimensions determine the frequency planning of the receiver. To further clarify the placement of the architectures in the 3-Dimensional framework, 2-Dimensional projections are given in Fig. 2. Looking at the first dimension, the IF, it can be observed that (from left to right in Fig. 2a and 2c) the Homodyne receiver has the lowest IF (IF = 0), followed by the low-IF (low IF), Superheterodyne/Digital-IF (medium/high IF) and finally Mitola's SDR (IF = RF). In the second dimension, A/D, no architectures lacking an A/D are presented in the framework. Thus, going from bottom to top in Fig. 2a or left to right in Fig. 2b the homodyne and superheterodyne are first encountered, having the A/D conversion after mixing to baseband, followed by the low-IF (at the low IF) and digital-IF (at a medium/high IF) architectures. Again Mitola's SDR is an extreme as it performs A/D conversion at RF. Finally in the third dimension, mixing complexity, going bottom to top in Fig. 2b and Fig. 2c, Mitola's SDR has no mixers at all, followed by the digital-IF (one mixer), low-IF and homodyne (two mixers), and finally superheterodyne (three mixers) architectures for increasing mixing complexity. Note that, while the dimensions are obviously related to each other, there is no one-to-one connection between them, as becomes clear from Fig. 2. Thus, all three dimensions are required to give a complete classification.

The properties of the common architectures will now be shortly introduced, with a more in-depth view presented in Section III.

The most traditionally used receiver is the superheterodyne



(a)



(b)

Fig. 3. Block diagram of (a) dual-conversion quadrature superheterodyne receiver (diagram based on [2], [7], [9], [10], [12], [13]) and (b) digital-IF receiver (diagram based on [1], [6], [10], [22]). Elements in the analog domain are outlined in black, while elements in the digital domain are outlined in grey.

receiver (Fig. 3a and Section III-A). By choosing the IF and filters properly excellent selectivity and sensitivity can be achieved using the superheterodyne receiver [1]–[3], [9], [10], and there are no DC-offset and leakage problems [2], [9], [10]. However, the (external) high-Q (surface acoustic wave (SAW), bulk acoustic wave (BAW) or film bulk acoustic resonator (FBAR)) filters that are required for image rejection and channel selection increase the cost, size and power consumption [2], [4], [9] and limit the flexibility, which becomes even more pressing in view of the required flexibility in 5G. The digital-IF receiver (Fig. 3b and Section III-A) is based on the superheterodyne receiver, performing A/D conversion after a single downconversion.

In contrast to the superheterodyne receiver, the homodyne receiver (Fig. 4 and Section III-B) directly converts to baseband. The homodyne receiver is the most common architecture used in low-power applications due to its simplicity and scalability [10], and can be fully integrated [9], [23]. However, it suffers from DC-offset [1]–[7], [9], [10], [24]–[26], flicker noise [1], [3]–[5], [8], [10]–[12] and even-order intermodulation [1], [5], [11]–[13] issues.

The low-IF receiver (Fig. 5 and Section III-C) combines some of the traits of the superheterodyne and homodyne receivers, using a low IF. It is particularly attractive for narrow-channel standards [12]. It does not suffer from the DC-offset problem found in homodyne receivers [4], [6], [7], [9], [27] or the 1/f noise problem [4], [27]. However, using the low-IF architecture, the mirror signal can be stronger than the wanted signal, resulting in more stringent mirror signal suppression requirements [6], [24].

Finally, Mitola's software-defined radio (SDR, Fig. 6 and Section III-D) consists of an ADC directly attached to the antenna, placing it far away from the more conventional architectures in our framework. This avoids the implementation of analog circuits and is very flexible as most of the functionality is defined in software, even enabling reception of every incident channel concurrently [28]. However, it poses very stringent requirements on the ADC which, even if they are achieved, would dissipate a very large amount of power [2], [28]–[30]. Nevertheless, the SDR concept has inspired some more realistic approaches, as discussed in Section III-D.

III. Architectures

The most important architectures and their derivatives are reviewed in this section. Each subsection corresponds to an architecture in the framework (Fig. 1 and Fig. 2), though some of the derived architectures might deviate from their indicated location.

A. Superheterodyne Receiver

Within the framework the superheterodyne receiver is indicated in green, appearing in the front-top-right octant in Fig. 1, as also illustrated in Fig. 2. If offers high performance, but has limited flexibility and relatively high cost and power consumption. Since Armstrong's publication in 1921 [31], the superheterodyne receiver has gained immense popularity, and is also known as the heterodyne or IF-receiver. The superheterodyne receiver usually uses one or two stages of down-conversion [11]. As an example, a block diagram of a double downconversion superheterodyne receiver is shown in Fig. 3a, while a single downconversion, also known as digital-IF, receiver is shown in Fig. 3b. In the latter case, the signal is digitized at the IF stage (hence the name digital-IF) and the quadrature downconversion is performed in the digital domain [6], [7], [10], placing it on the intersection of the two bottom-right octants of the framework, as shown in in Fig. 1 and 2.

In superheterodyne receivers, the signal coming from the antenna is downconverted to the (first) IF by the (first) mixer, as shown in Fig. 3. It can then be digitized at this IF (Fig. 3b) or further downconverted after filtering, by quadrature down-conversion if it is downconverted to DC (Fig. 3a). Its main disadvantage is that not only the wanted signal (situated at f_c) is downconverted to the IF, but also the mirror frequency (situated at $f_c - 2f_i$). Therefore, the mirror frequency has to be suppressed before mixing, which is performed by BPF 1

and BPF 2 in Fig. 3, known as the image-reject filtering [2], [6], [7], [12]. The requirements for these filters depend on the choice of IF: if the IF is high, then the wanted signal is far away from the mirror frequency [6], [7], [10], [12]. However, even when the IF is high, this results in stringent filtering requirements, so these filters cannot be integrated [6], [10]. This also means that it will be very hard to make flexible filtering to accommodate frequency flexibility for 5G. In addition to filtering, some amplification is performed before mixing by the LNA to decrease the noise figure (NF) and thereby increase the receiver's sensitivity. Therefore, BPF 1 also serves to remove out-of-band signal energy to avoid desensitization [7]. After downconversion to the IF, further filtering is applied by BPF 3 to separate the desired signal from other nearby signals, also known as the channel select filter [6], [7], [10], [12]. Since this operation is performed at IF, the choice of IF again affects the filter requirements: Choosing a high IF results in a higher required Q-factor than a lower IF if the channel separation remains the same. Again, integrating these IF filters is very hard [6]. Thus, the selection of IF becomes a trade-off between image rejection (before mixing) and channel selection (after mixing) [5], [7], [12]. BPF 3 is followed by a variable gain amplifier (VGA) to amplify the signal to the optimal range for the ADC. After the VGA, the signal can be further downconverted to a lower IF, or shifted to baseband [7]. In the case where the signal is downconverted to baseband, analog quadrature downconversion has to be performed (Fig. 3a) in order to separate the negative from the positive frequencies, similar to the homodyne receiver (Section III-B), also suffering from many of the same issues [12]. This approach is most common in modern heterodyne receivers [12]. Alternatively, the signal can be downconverted to a lower IF (adding more conversion steps is intended to alleviate the trade-off between image rejection and channel selection requirements [12]), or the signal can be sampled at IF (Fig. 3b). The latter is known as a digital-IF receiver [7] and has the advantage that there is no I/Q imbalance [7], [10], while it requires AD conversion at a higher frequency and thus a more expensive and power-hungry ADC [7].

A sliding-IF receiver is a dual-conversion superheterodyne receiver which employs only one oscillator, mainly because multiple oscillators on the same chip suffer from unwanted coupling [12]. Instead, the second local oscillator (LO) frequency is derived from the first by frequency division [12], [32].

To alleviate the filtering requirements, which would be especially useful in the face of 5G, image rejection techniques have been proposed, the most popular being the Hartley and Weaver architectures [11], [13]. These techniques are based on Weaver's single-sideband generator/receiver concept [1], [3], [5], [12], [33] and Hartley's image rejection receiver [1], [5], [34]. In both, a quadrature downconversion is applied to the RF signal, followed by low-pass filtering. In the Hartley architecture, the resulting signals are combined after one is shifted by $90°$, while in the Weaver architecture the phase shift is performed by a second pair of mixers [11]. Both the Hartley and Weaver architectures are sensitive to amplitude and/or phase imbalances, though the Weaver architecture suffers less

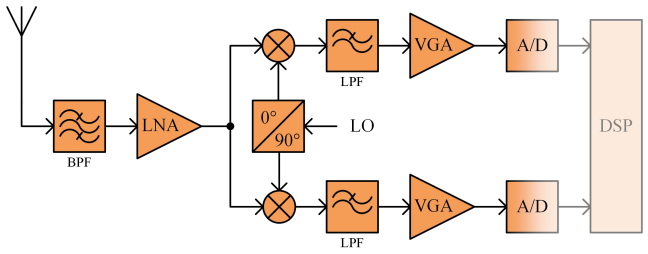


Fig. 4. Block diagram of zero-IF/direct-downconversion/homodyne receiver (diagram based on [1]–[3], [5], [7], [9]–[12], [37]). Elements in the analog domain are outlined in black, while elements in the digital domain are outlined in grey.

from amplitude mismatch due to the absence of a phase-shifter [1], [11], [12]. Calibration techniques can be used to improve the image rejection in both the Hartley and Weaver architectures [12]. In addition, an automatically tuned PLL-based filtering concept was proposed in order to obtain more attenuation of the image signal [35]. Alternatively, a tunable image-reject notch filtering approach was proposed [36].

In an attempt to achieve higher levels of integration, flexibility and performance, the wide-band IF double conversion receiver, often indicated simply as wideband-IF receiver, was introduced [2], [7], [9], [24], [25]. In this approach, like the conventional superheterodyne receiver, the frequency translation is distributed over multiple steps. However, in each conversion step, I/Q mixing is performed on all potential RF channels [7], and therefore all information to perform image rejection is available at baseband. This idea is very similar to the low-IF architecture with real filter (Section III-C and Fig. 5b), the main difference being that the A/D conversion is performed after the second downconversion, and therefore not treated in detail here.

B. Homodyne Receiver

The homodyne receiver, placed on the intersection of the two front-left octants in the framework (Fig. 1 and Fig. 2), also known as the direct-conversion or zero-IF receiver, was considered as early as 1924, though the concept lay dormant for a long time until it was revived in 1980 [3]. A block diagram of the homodyne receiver is shown in Fig. 4. The main difference with the superheterodyne receiver is that no IF is used or, in other words, the IF is chosen to be zero [3], [6], [7]. Therefore it trades off performance to lower cost and power consumption, since it is lower in dimension 1 than the superheterodyne receiver. The homodyne receiver is the most common architecture used in low-power applications due to its simplicity and scalability [10], and can be fully integrated on a chip [9], [23] since no high-performance BPF is needed. This also increases the feasibility to develop a tunable filter with sufficient performance for 5G.

In a homodyne receiver, the signal is directly downconverted to baseband, without using an IF. Thus, since $f_i = 0$, the mirror frequency is equal to the desired signal's frequency. Nevertheless, a problem with the mirror frequency still exists: the wanted signal is mirrored in the negative frequency range, resulting in the top end of the signal band from the positive

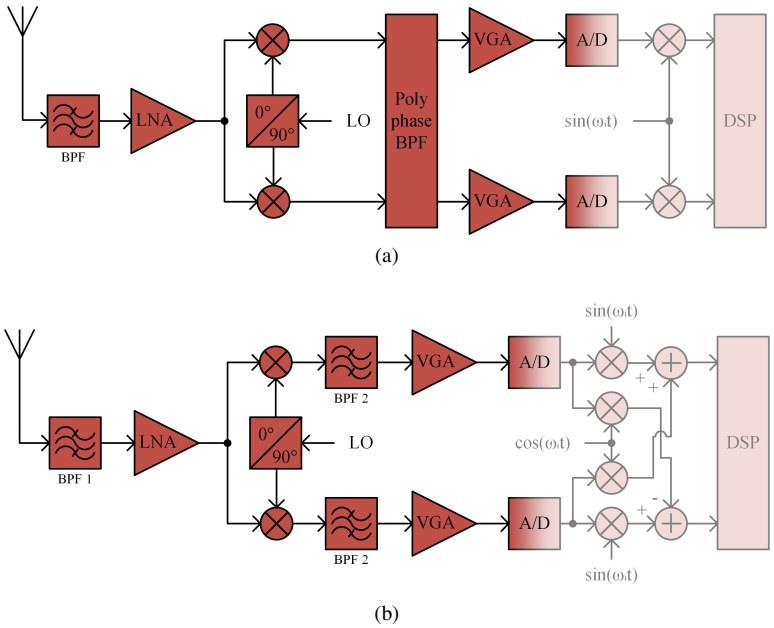


Fig. 5. Block diagram of (a) low-IF receiver which uses a complex BPF (diagram based on [6], [10], [13]) and (b) low-IF receiver which uses real filters (diagram based on [6], [7], [24], [27]). Elements in the analog domain are outlined in black, while elements in the digital domain are outlined in grey.

frequencies overlapping with the low end of the signal band from the negative frequencies after downconversion, and vice versa. Therefore, a quadrature downconversion is needed [3], as illustrated in Fig. 4. Since, in theory, quadrature downconversion is equivalent to complex mixing [6], [7], the desired signal can be obtained by the DSP. As shown in Fig. 4, in most homodyne receivers the signal from the antenna is filtered and amplified before mixing. The former serves to prevent desensitization due to blockers, while the latter serves to decrease the receiver's NF. After mixing, the desired signal is at baseband, and thus channel selection can be performed by low-pass filters (LPF). The signal is then brought in range of the ADC's by VGA's and converted to the digital domain where it is demodulated using a DSP.

Compared to the superheterodyne receiver, the main advantage of the homodyne receiver is the very high integration level that can be achieved, as in most designs no high-Q bandpass filters are required [6], [12]: the channel selection is performed by low-pass filters [12], and there is no need for an image rejection filter [7]. Instead, the suppression of the mirror signal depends on I/Q (mis)match [5], [6], which arises due to gain and phase errors: the complex LO output not only contains the negative frequency, but also a positive frequency component [7]. Both analog and digital I/Q imbalance compensation techniques have been proposed [38], including techniques non-data-aided ('blind') techniques [39]. In many high-performance systems this requires calibration [12]. However, since the mirror signal is the desired signal itself, the specifications on mirror suppression are less severe than in a heterodyne receiver, as the signal on the mirror frequency cannot be bigger than the desired signal [3], [6]. In addition to I/Q imbalance, flicker noise (also known as 1/f noise) is a drawback of the direct-conversion topology: as the signal is directly down-converted to baseband, flicker noise is an in-band phenomenon [1], [3]–[5], [8], [10]–[12]. The problem of flicker noise makes it difficult to use homodyne receivers for narrow-bandwidth standards [12]. Furthermore, homodyne receivers are (in addition to odd-order intermodulations) also vulnerable to even-order indermodulations [1], [5], [11]–[13], though several topologies have been proposed to combat this problem [11]. DC-offset is perhaps the worst problem in zero-IF receivers [1]–[7], [9], [10], [24]–[26], desensitizing the receiver by saturating the circuits. Due to finite isolation, the LO signal can leak to the other mixer input, or even the LNA input or through the antenna [1], [5], [7], [9]–[12], [25], mixing with itself and resulting in a DC component. The leakage to the antenna also creates an in-band interferer, since (part of) the power is radiated [1], [3], [7], [10], [12]. Another cause of self-mixing can be an in-band interferer (possibly the receiver's own radiated power) leaking to the LO port of the mixer [7], [9], [10]. Thus, the DC offset can also be time-varying [7]. Self-mixing is the problem that has kept the homodyne receiver from use in practical applications for a long time [6].

One approach to remove the DC offset is to use ac-coupling in the signal path, e.g. using a series capacitor. However, since currently used modulation schemes contain signal energy at DC, this would deteriorate the signal quality [7], [11], [12]. Other approaches include analog and/or digital offset estimation and cancellation [5], [7], [11].

C. Low-IF Receiver

In the framework (Fig. 1 and Fig. 2) the low-IF receiver is placed on the intersection of the four left octants and indicated in red. The goal of the low-IF receiver is to combine the advantages of the superheterodyne and zero-IF receivers [6], [7], and is particularly attractive for narrow-channel standards [12]. The low-IF receiver is roughly in between the superheterodyne

and the zero-IF receiver in the framework, illustrating that it balances the system-level trade-off between the two. It uses two downconversion paths like the homodyne receiver, but still uses an IF. This results in an image rejection topology similar to the Hartley and Weaver architectures [12]. In Fig. 5, two types of low-IF receiver are shown: one which uses a complex bandpass filter (also referred to as a polyphase bandpass filter, Fig. 5a), and one which uses a real bandpass filter (Fig. 5b).

In the low-IF receiver, the wanted and mirror signals are downconverted to the IF, but are not superimposed due to the use of I/Q mixing: the wanted signal is situated at negative frequencies, while the mirror image is situated at positive frequencies [6], as shown in Fig. 5. The IF can range from half to several times the channel bandwidth [7], [10], [13]. In the complex BPF approach the mirror signal is suppressed by the polyphase BPF, brought in range of the ADCs by the VGAs, converted to the digital domain, and then (digitally) downconverted to baseband by multiplication with a sine. Due to the low IF it is more feasible to sample the signal after the first mixer stage than in e.g. a superheterodyne receiver [7]. However, it requires a higher resolution than a wideband IF receiver since both the wanted and image signals are sampled while the image signal can be much larger than the desired signal [7]. In the approach using real filters, the BPFs separate both the desired and mirror signals from other nearby signals. The VGAs amplify the signals to bring them in range for the ADCs. Then, the final downconversion is performed in the digital domain, using a positive frequency equal to the IF [6].

Since the wanted signal is not situated around DC in this architecture, it does not suffer from the DC-offset problem found in homodyne receivers [4], [6], [7], [9], [27] or the 1/f noise problem [4], [27], and the signal path can be AC-coupled. Nevertheless, it features the same high degree of integration as a homodyne receiver [27] since the filtering after the LNA is done close to DC. Again, this also increases the possibility of developing a sufficiently performing filter to accommodate 5G's flexibility. Furthermore, part of the complex mixing is implemented in the digital domain, without I/Q mismatch. However, using the low-IF architecture, the mirror signal can be stronger than the wanted signal, resulting in more stringent mirror signal suppression requirements [6], [24]. Due to the I/Q mixing in the analog domain the major challenge in a low-IF receiver is the limited image rejection due to imbalances between the I- and Q-paths, typically limited to approximately 35dB without tuning or calibration [26].

D. SDR Receivers

For clarity, all architectures that were proposed with the ability to configure the receive path to different frequencies and/or bandwidths as the main goal are treated in this section. The ideal SDR receiver, as first envisioned by Mitola [40], is shown in Fig. 6, and placed on the far right corner in the framework, as illustrated in Fig. 1 and Fig. 2. Note that this extreme has not (yet) been reached in practice. Sometimes an LNA and anti-aliasing filter are shown in this architecture preceding the ADC [22], be these are then assumed to operate

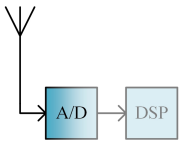


Fig. 6. Block diagram of the 'ideal' SDR receiver as envisioned by Mitola [40] (diagram based on [28], [30]). Elements in the analog domain are outlined in black, while elements in the digital domain are outlined in grey.

in all relevant bands and have sufficiently high linearity. The antenna is directly followed by the ADC, and thus all other functionalities are implemented in the digital domain. This avoids the implementation of analog circuits and is very flexible as most of the functionality is defined in software, even enabling reception of every incident channel concurrently [28]. Conceptually, this architecture could accommodate all standards as long as the ADC has sufficient sensitivity, dynamic range, sampling rate, etc., including 5G. However, it poses very stringent requirements on the ADC which, even if they are achieved, would dissipate an unacceptably large amount of power [2], [28]–[30] for mobile applications. To make matters worse, progress in ADCs is much slower than Moore's law [28], which mainly benefits the DSP, since the problem is more complex than scaling transistor sizes. More generally, SDR can be seen as the expansion of digital signal processing, and thus ADC, towards the antenna [22]. This expansion means that both the dynamic range and the input bandwidth of the ADC must improve, at the cost of increasing power consumption [1]. This also implies that the required linearity increases, since the increased bandwidth means that more signals (desired and undesired) have to be processed by the receiver, as opposed to being filtered out early in the receive chain.

An alternative approach to obtain flexibility for 5G is to use switching circuits instead of a mixer and/or using the switching to obtain a comb-filter-like functionality [41]–[48]. However, obtaining resilience to out-of-band blockers combined with a good noise figure and intermodulation performance over a wide frequency range remains challenging [48]. This approach shows much similarity to subsampling architectures. A similar concept employing bandpass sampling at RF is discussed in [2], [49] though the concept was not implemented, and there are several drawbacks such as very stringent requirements on the ADC, the need of tunable RF filters, noise aliasing, and degradation of the SNR due to clock jitter. Another interesting development is the introduction of the direct Delta-Sigma receiver [50]–[54]. This is also a direct RF to digital conversion approach, but combines the RF front-end with a feedback-type Delta-Sigma ADC [54]. Advantages include noise shaping at RF, full integration, and both tunable center frequency and bandwidth. Though this technique does not yet offer the performance of conventional receiver architectures, it is a promising candidate for a flexible receiver solution.

In order to avoid having to sample at RF, the IF-sampling (Fig. 3b and Section III-A) is a popular architecture in modern SDR receivers [10]. The idea is to digitize only the band that the particular SDR needs to cover [22]. When the sampling frequency is chosen much lower than the IF, the IF-sampling

receiver is referred to as an (IF-)subsampling receiver [2]. This technique intentionally aliases the incoming signal, and samples one of the resulting images, reducing the ADC requirements. Problems are noise aliasing and sensitivity to jitter [2].

On the other extreme from Mitola's SDR, zero-IF architectures have also been proposed for SDR [28], [37], [55], mainly because there is no need for image reject filters. A variation of the homodyne receiver is the subsampling receiver, where the mixer is replaced with a sampling circuit, which samples the RF signal at the Nyquist rate of the baseband signal [9]. While the availability of a high-speed switch is critical, the sampling frequency is much lower than the carrier frequency, making the oscillator simple to design and less power consuming [9]. Drawbacks are noise aliasing, magnification of jitter on the sampling clock, clock feedthrough, settling time of amplifiers, and the proportionality of the sampling frequency with the carrier frequency, resulting in high dynamic-range requirements and high sampling frequency of the ADC [9].

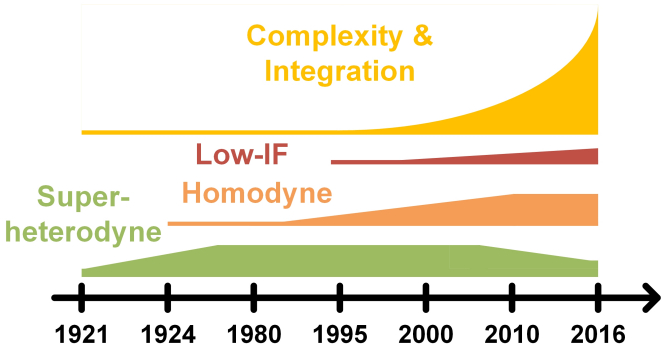


Fig. 7. Illustration of the popularity of receiver architectures and complexity/integration level over time. This figure is based on the trends observed in Section IV, and is intended to give an indication only (not drawn to scale).

IV. Trends

A. Architecture

In the 1990s and the early 2000s, the superheterodyne receiver was the most commonly used architecture for mobile communications [3], [4], [7], [25], [35], the direct conversion topology being limited to e.g. pager receivers [5]. Nevertheless, the zero-IF topology was gaining popularity, due to the need for better portability and lower cost [24], becoming an active research topic again [5]. They still had not been used for non-constant envelope modulation schemes in commercial products in 2000 [7] though. This is also illustrated in Fig. 7. The superheterodyne receiver was still the most popular around 2005, although a trend to a higher level of integration, lower cost and power levels was also observed [2] - and, logically, the appearance of low-IF and homodyne architectures for multiband solutions [8]. In 2011, Razavi noted that direct-conversion receivers had become popular in the last decade, when integration and signal processing made it a viable choice [12]. Now, the zero-IF and sliding-IF are the most commonly used low-power receiver architectures [56]. Within the framework (Fig. 1 and Fig. 2) this can be seen as a trends towards a lower IF in dimension 1, earlier A/D in dimension 2 and a decreasing number of mixers in dimension 2.

B. Integration

While in the 1990s the goal was to integrate one transceiver, current efforts aim for multiple transceivers, operating in different frequency bands for different wireless standards [12]. In modern smartphones, often GSM, W-CDMA, (TD-)LTE, WiFi, BT and GPS capabilities are combined, each in different bands and most of them requiring multiple bands. For example, LTE (release 13) defines 49 bands [15]. This results in an increase of both passive and active component count, which is also illustrated in Fig. 7 by the increase in complexity. Some manufacturers choose to build a phone that is compatible to nearly all popular standards in every country ('world phone'), while others build different models that can be used in particular regions ('local phone'). This results in different requirements, but their implementation is similar: the capabilities have not (yet) been integrated into a single module, and are implemented by duplicating RF paths, leading to component duplication [57]. In 2009, convergence of standards was achieved by assembling dedicated ICs on PCBs, though system-on-chip (SoC) solutions (integrating multiple RF front-ends and modems on the same chip) had also appeared [55]. Now, in popular modern smartphones, a SoC connected to PAs, SAW/BAW/FBAR duplexers or filters, LNAs and switches, often in modules (or 'banks') are observed. In order to save space, 3-dimensional packaging and filter banks have emerged [57]. This trend of increasing integration level is also illustrated in Fig. 7 with the 'Complexity and Integration' curve. While this leads to a reduced component count, it does not result in a reduction of parallel receive paths or a real change in architecture, and therefore does not decrease the complexity. As wireless standards evolved from 2G to 4G, the number of filters external to the receiver module increased from about 6 (2G) to 45 (4G), the number of RF ports of the transceiver increased from 10 to 60, and that the number of switch ports required for signal routing increased from 6 to 30 [58], altogether increasing the transceiver's complexity and cost drastically. Electronics remain affordable due to the integration on a single chip, thanks to scaling of VSLI processes (in particular, CMOS) and innovations in RF circuits and devices [12].

In research, a trend to use switching circuits instead of a mixer and/or using the switching to obtain a comb-filter-like functionality can be observed [41]–[48], sometimes completely omitting an LNA. Again, these topologies aim at higher integration and flexibility in operating frequency, targeting to replace the SAW/BAW/FBAR filters currently used. However, the harmonic responses and noise folding (noise folding back from the alias bands) present drawbacks. Nevertheless these topologies seem very promising for 5G since they can relieve the filter requirements.

C. 5G

It is expected that 5G will integrate current standards such as LTE-A and WiFi, as well as add a new '5G' air interface [17]–[19], e.g. cm-wave, mm-wave, and TV white-space spectrum, and/or new waveforms for increased spectral efficiency. In addition, a key goal of 5G is to increase the flexibility dramatically, making the SDR concept currently a hot research topic. Furthermore, even for current standards, the SDR concept has the potential to reduce the cost of the receiver dramatically by eliminating (or reducing the number of) parallel receive paths. For SDR receivers, moving the ADC closer to the antenna was already a trend in 2007 [49], providing more flexibility and the ability to receive several channels at different frequencies simultaneously. This comes at the cost of increased ADC requirements (dynamic range and input bandwidth) and increased linearity requirements of the receive chain. This becomes especially challenging for multi-mode operation and high data rates, which are expected for 5G. Nevertheless, the SDR concept provides very interesting possibilities.

In addition to higher flexibility, there is also a push for higher data rate ($>$ 10X on average and peak rates and $>$ 100X on cell edge) in 5G when compared to LTE release 12 [18], [19], as well as higher mobility ($>$ 1.5X), spectral efficiency and connection density ($>$ 100X) [18], [19]. Especially combined with the increased flexibility, this is a hard task from the handset receiver point of view. Therefore 5G asks for bold innovations on both component and architectural level.

V. Conclusion

An overview of the commonly used receiver architectures is given, each with their (dis)advantages and variations on them. The proposed framework allows a clear classification of architectures, as well as identification of unexplored possibilities. A trend towards integration and adding more standards and bands to the receiver has been observed. Currently this is done by introducing parallel RF paths, an unsustainable method in the face of 5G's expected flexibility requirement. While some more flexible receiver solutions have been proposed, modern smartphones still contain fixed filters, adding to their cost and limiting their flexibility. With 5G around the corner, a more flexible, low-power and high-performance solution is needed.

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