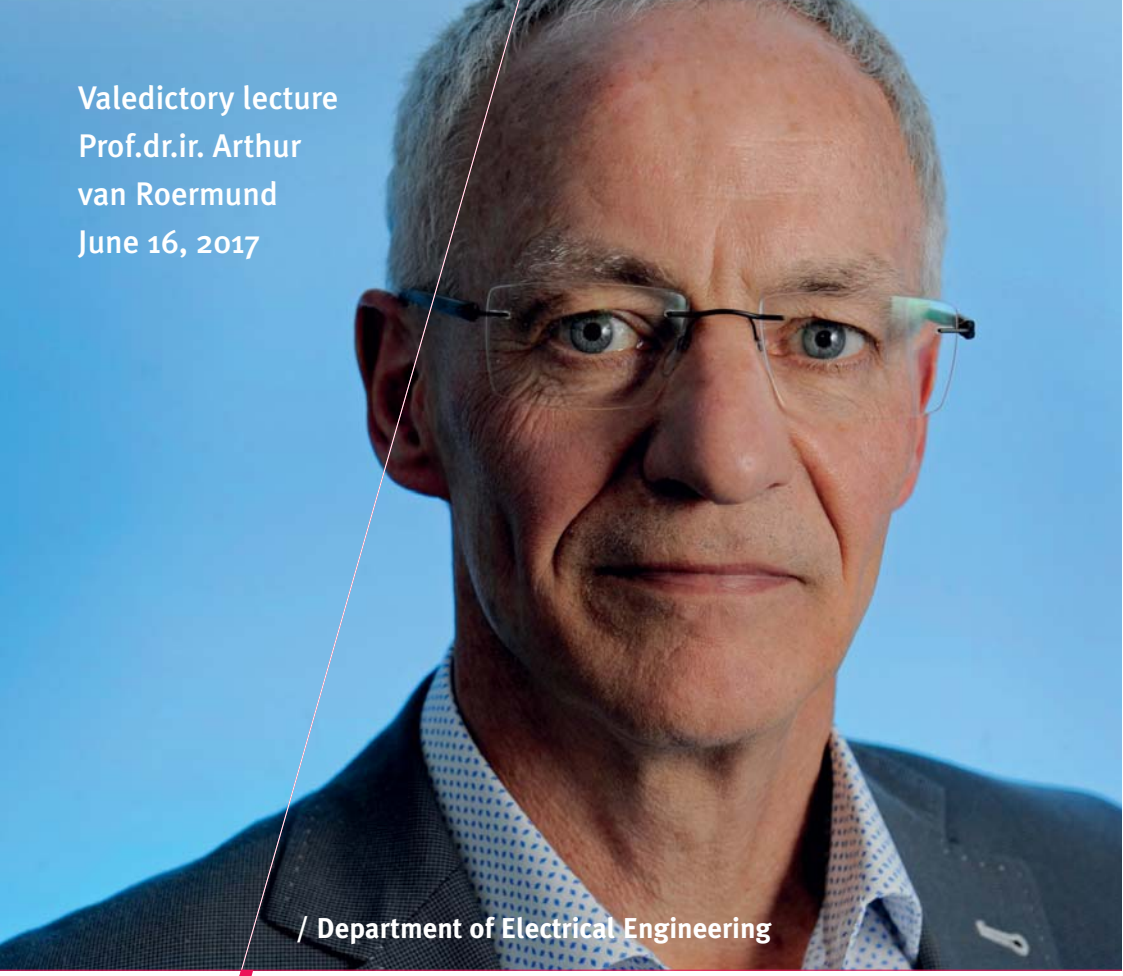
# Integration 2.0



Valedictory lecture
Prof.dr.ir. Arthur
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June 16, 2017

/ Department of Electrical Engineering

TU/e Technische Universiteit **Eindhoven** University of Technology

# Integration 2.0

**Where innovation starts**

Valedictory lecture Prof.dr.ir. Arthur van Roermund

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Presented on June 16, 2017
at Eindhoven University of Technology

# Introduction

Mijnheer de Rector Magnificus, geacht College van Bestuur, geachte collega-hoogleraren en andere collega's, studenten, promovendi, familie, vrienden en kennissen, dames en heren. Today, it is 42 years ago that I started my career in microelectronics, 25 years ago that I started as full professor at the university, and 18 years ago that I joined Eindhoven University of Technology.

In 1992, I gave my inaugural speech titled 'Over integratie gesproken' ('Speaking of integration'). Now, 25 years later, integration is even more a key word in microelectronics. In this valedictory lecture 'Integration 2.0', I will address various integration aspects, past and future, and, more specifically, the role of analog in it. I hope to make clear that analog plays an essential role in most electronic systems, despite the fact that the majority of these systems have become digital. I will also give my vision on future developments and explain why I think we are on the verge of a new microelectronics world. That is also why I called my speech 'Integration 2.0'.

# Integration technology, the microelectronics explosion

Most of you will be familiar with Moore's law. Gordon Moore, one of the founders of Intel, predicted in 1962 that the density of transistors would grow by a factor 2 every year. Later, in 1975, he adjusted that to a doubling every two years. Indeed, since then we have seen this enormous exponential growth. The performance grows even faster, by about a doubling every 1.5 years, as the speed of the transistors also increases every time we scale down the dimensions. This explosion has been enabled by a large-scale integration technology, based on ever larger silicon wafers with many small 'copy x, copy y' repeated integrated circuits (ICs, or 'chips') on it. This has led not only to a doubling in the number of transistors, but also to a reduction in cost per transistor, despite the increasing production costs per wafer due to both larger wafer sizes and smaller IC details. However, scaling becomes increasingly difficult, as we approach atomic scales. This manufacturing technology is normally the first association people have with the word 'integration'.

Another reason for the microelectronics explosion is the digitization. Manufacturing chips is one thing; designing them another. Indeed, the exponential growth in number of transistors led to an enormous growth in circuit and system design complexity. This could be controlled by the well-known digitization: the two-level electronic signals represent a logic 1 or 0 within a certain margin, such that physical errors can be corrected in time by every next logic gate. This signal redundancy enables a complete abstraction from the physics of the hardware. Consequently, various system layers can be decoupled, which strongly reduces design complexity; a design can be split into many independent subtasks; (re)programmability is possible; and so on. Digitization has been as crucial for the microelectronics explosion as the integration technology.

# All electronic hardware is analog, digital is an abstraction

All this might suggest that analog is out, but that conclusion is by no means correct. First, the electronics of the digital part of the chip, including the clock and data transport, is fundamentally analog, as the signal waveforms are analog by nature and should be accurate and robust enough to be *interpreted* flawlessly by every next gate as logic 0 or 1 (digital), see Figure 1. Designing robust 'digital' library blocks, therefore, remains an analog task at transistor level. The more we scale the technology and improve system specifications, the more the margins decrease, making the analog physical design of digital library blocks and their interconnections more and more complex.

Second, off-chip, digital information is often communicated via complex analog signals. Their translation to the bits for the digital part of the chip (and vice versa) is done by an on-chip analog part, again the red part in Figure 1, which is now a complete and complex analog 'frontend' instead of a simple logic gate. This is currently the dominant playing field for analog electronic designers.

Third, for future integration technologies, the situation may change considerably, as will the position of analog (and digital) in the electronics ball park. This will be explained later.

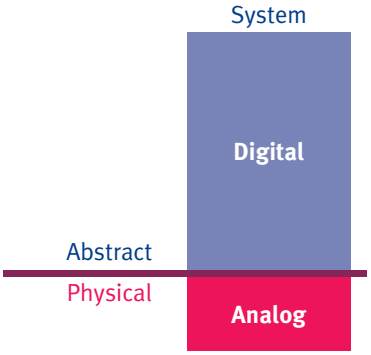


Figure 1

Analog is concerned with the physical hardware; digital is an abstraction.

# Mixed-signal integration, analog is mixed signal

Analog refers to continuous information, in contrast to digital that refers to discrete numbers. In hardware, information is represented by electronic waveforms: time-varying voltages or currents (or any other physical carrier). Both amplitude and time are continuous domains, so electronic hardware is analog by nature. However, depending on the way we package the information in our waveform, we distinguish *four signal domains* for the analog waveforms.

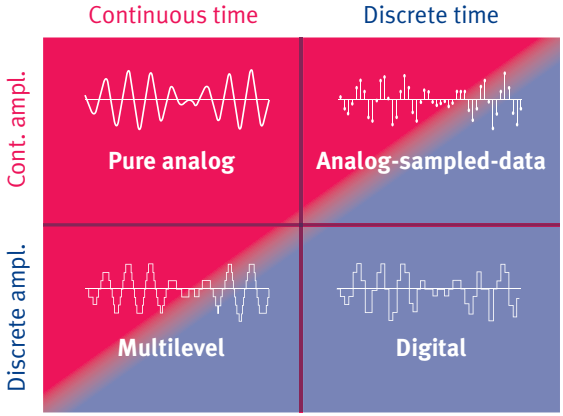


Figure 2

The four main sub-classes of analog waveforms, with discretization in one, two or both domains.

Pure analog, see Figure 2, refers to analog waveforms that carry information at any amplitude and at any moment. Analog-sampled-data (asd) refers to discrete information samples that can have any value (analog numbers), represented by analog waveforms that can have any amplitude, but only change once per clock moment. They are robust to timing errors, as the amplitude information is constant during a full clock period. Multilevel refers to waveforms that can change at any moment (asynchronous) but only to a limited set of discrete amplitude levels. The amplitude domain is then used only for discrete information values, but the time domain can cover analog (continuous) information. They are robust to amplitude errors. Digital waveforms carry only discrete numbers; the corresponding analog waveforms have discrete amplitudes (mostly two-level, for

1 bit) and are only interpreted (measured) at discrete clock transitions. Small physical variations, both in time and amplitude, can be restored by a next digital block to the original discrete value, thus fully preserving the information.

With discretization, in any or both domains, we make a tradeoff: we pay – as we give up part of the range of one or two physical domains – in exchange for robustness in that domain (allowing abstraction in that domain). Each of the four sub-domains has its own properties, and optimal mixed-signal analog design implies a proper mixed use of these domains.

# Integration of analog and digital, two complementary tasks

While the digitization of systems and chips did not rule out analog, it did force us to find the optimal combination of both, by formulating their different tasks more clearly. Optimal design means an optimal balance between functional performance (speed, accuracy, reprogrammability, etc.) on the one hand, and required resources (energy use, chip area, IC cost, design time, etc.) on the other hand. Together this is defined in the IC-design specifications, and derived from the application specifications, see Figure 3.

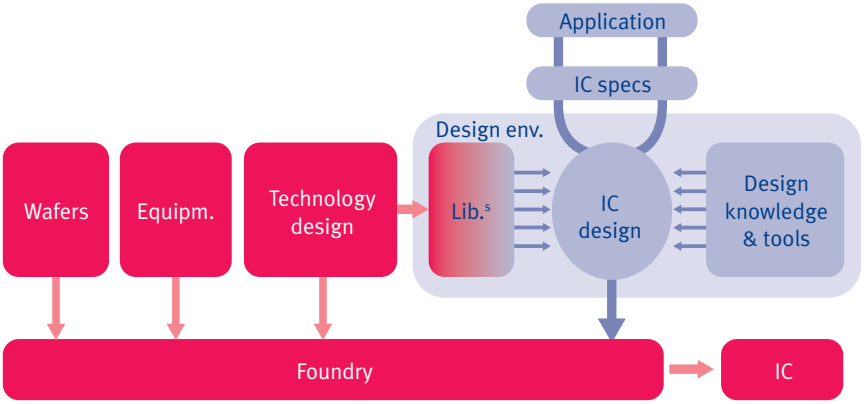


Figure 3
IC design environment with hardware-related parts in red.

As mentioned earlier, digital has its own strong properties, like accuracy, reliability, flexibility and programmability. The design complexity is strongly reduced by hiding all physical effects via the library models, so that a digital designer doesn't need to have knowledge on details of the technology used in the foundry (the IC factory), nor on the underlying physics, and can focus completely on the system complexity at the higher levels of design. System functionality is therefore preferably realized in the digital domain.

Analog, on the other hand, is fundamental in translating complex analog signals, like the modulation signals in communication channels, to digital and vice versa, and in providing robust and reliable discrete-level (analog) waveforms that can

subsequently be interpreted as abstract digital signals, see Figure 4. Abstraction costs hardware efficiency, but you can regain efficiency at the higher levels, e.g. by exploiting flexibility and (re)programmability.

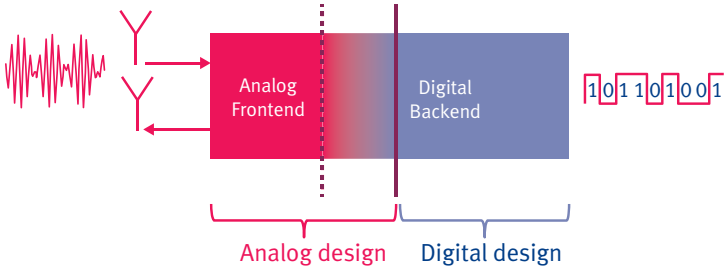


Figure 4

Two complementary functions for analog and digital on the IC.

So it is all about the best integral combination of analog and digital design, for an optimal design in terms of functionality versus resources: cutting-edge performance. Note that this is technology dependent: in an advanced technology a higher performance can be achieved than in a less advanced technology (like some emerging technologies discussed later); the tradeoffs will certainly be quite different, but the design challenge is similar.

An electronic designer needs to have good knowledge about the technology, and work with highly complex analog library models and simulation tools, see Figure 3, that incorporate many physical details of devices and interconnects, even e.g. 3-dimensional electromagnetic effects. The devil here lies in the physical details.

# Shannon-based integration, a fundamental view

The analog frontend, see Figure 4, can be seen as a physical bottleneck. The complexity of its design is very high, due to the amount of physical details and the large number of possible design choices to be made during the design process: definition of proper frontend specifications; optimal transition point(s) for amplitude/time discretization and final digitization (can be chosen anywhere in the chain); proper partitioning into sub-functions and sub-specifications; proper choice of signal domains (mixed signal) for each sub-function; translation to optimal transistor-level circuits; designing the layouts; etc. Moreover, digitization in not the only way to achieve robustness, as will become clear later. Therefore, a fundamental view on the problem makes sense, to get control of complexity and to achieve an out-of-the-box view for future developments, as discussed later. Three concepts play a crucial role in that: channel capacity, matching and redundancy.

### Channel capacity, matching, and redundancy

Already in 1948, Claude Shannon published a paper on the *channel capacity* of a communication channel, now well-known as the Shannon-Hartley theorem. It states the maximum amount of information that can be transmitted through a channel with a certain signal-to-noise ratio and bandwidth. It is widely applied for a free-space propagation channel between two antennas.

To fully exploit this channel capacity, the information (bits) should be encapsulated in a *matched* signal that fits this capacity exactly in all signal domains: time, frequency, amplitude and space. On the other hand, the capacity can be adapted by changing resources, in this case e.g. the transmitted signal energy or space used (e.g. antenna size/arrays). Efficiently exploiting a physical channel means an optimal interplay between expending resources and creating a correspondingly matched signal. For that reason, the communication signals used for wireless transmission are highly complex analog signals (see Figure 4). For wired transmission, e.g. cable distribution, different signals are used, but these too are complex analog signals.

An optimum match means expending minimum resources for the job, so no unused channel capacity or, in other words, no *redundancy*. In practice, interfering signals will be there and occupy part of the channel capacity, which means we need redundant[1] capacity to cover them. Moreover, propagation errors can be introduced. These, too, can be counteracted by redundancy, e.g. by redundant bits combined with redundant hardware for error correction.

### Extending the model to integrated circuits

The concept described above, used for free-space propagation, can be extended for transmission of signals within an IC [1]. The medium is now the silicon technology. Here, too, the capacity can be adapted by changing resources (in this case e.g. changing the technology, or expending more supply power or chip area) and by using a correspondingly matched signal waveform.

From the beginning the technology has been optimized completely for digital (two-level synchronous signals), enabling a very robust error correction at the lowest level, where every logic gate corrects all physical errors that occurred since the previous gate. The associated redundancy was very large, resulting in inefficient use of resources, but over the years, it has been reduced by lowering the supply voltages (lower power dissipation). The capacity has been improved by scaling, leading to ever higher transistor densities, and further by increasing the speed of the process (smaller dimensions). Clock speeds were increased up till the moment it was clear that it was more efficient to keep clock speeds constant and use more of the spatial domain: parallelization of the waveforms. This digital approach proved very successful and led to the microelectronics explosion mentioned earlier. However, other forms of redundancy and error correction have to be applied in the frontend, as the signal waveforms at its inputs (Figure 4) are analog and prescribed by the propagation channel. Moreover, with the advent of alternative (bio-inspired and nanoscale) technologies, with stronger emphasis on hardware efficiency, alternative approaches with redundancy and correction distributed over layers, might very well come up, as discussed later.

[1] Redundancy is defined here as superfluous with respect to the primary function.

# Integrated frontends

Let's first have a look at the frontend design issue, from a Shannon-point of view.

### Matching between propagation medium and digital backend

As stated, the communication signals outside the chip have been optimized using highly complex analog waveforms. At the same time, the silicon technology has been optimized to the digital waveforms for the digital backend, which are completely different. The function of the analog frontend in between the propagation medium and digital backend is basically to provide an optimal match between them: the transmitting part of the frontend has to create the communication signal from the bits, and the receiving part has to 'unpack' the signal to get the bit signals back such that they can be converted into the original digital words[2]. Figure 5 visualizes this matching process (for a simplified 2-dimensional situation).

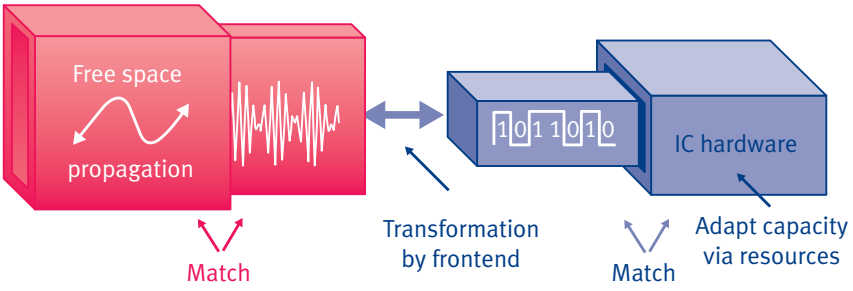


Figure 5

Visualization of frontend function: matching between propagation signal and hardware.

### Matching to the technology

Let's now look to the matching situation for the frontend itself. The signal waveforms *at its input and output* have been prescribed by the propagation medium and the digital technology respectively. Moreover, the frontend usually is

[2] A further part of the matching is done by the digital backend, via proper source and channel coding and decoding in the digital domain.

co-integrated with the digital backend, in the same CMOS technology[3], so it has to perform its function in a far from matched technology, with signals changing strongly from the complex purely analog modulation function, via all kinds of mixed-signal waveforms in between, up to the simple two-level digital waveforms (one or more in parallel, to match the speed). Still, we want to find the best possible match *also in the frontend itself*, so between the (varying) signals and the (silicon) medium, as visualized in Figure 6. This makes the design of a frontend a very tough job.

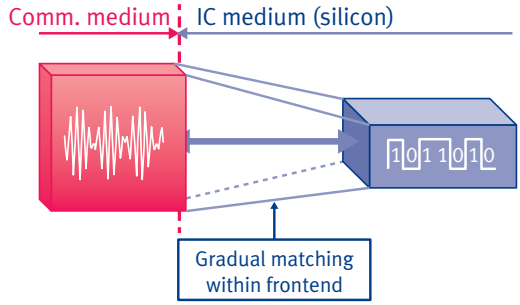


Figure 6

Gradual matching within the frontend.

The match can be achieved, on the one hand, via signal transformations that redistribute the signal information step by step over amplitude, time, frequency and space[4], and, on the other hand, by adapting, also step by step, the local capacity in the signal domains, via proper assignment of power and area, while keeping the boundary conditions of input and output signal waveforms in mind. Key is: *keep the hardware in its comfort zone, where its efficiency is highest*. By careful design, power dissipation and chip area can be kept very low, see e.g. [2].

### Integrated intelligence and redundancy, smart frontends

The design of a frontend (and any analog circuit in general) becomes significantly more complicated by unknown variations: all kinds of external en internal interfering signals, circuit and technology variations, ambient influences, crosstalk, user interaction, etc.

[3] If a separate IC is used, we can choose special technology options to get a better match, as discussed below.

[4] The basic transformation functions are gain and offset (amplitude); delay and phase shift (time); filtering and frequency shifting (frequency); modulation (time/frequency/amplitude); data conversion (translation to/from two-level waveforms); and (de)multiplexing of the two-level waveforms.

Enough redundant hardware capacity is needed *to cover* all variations, to prevent a lack of capacity for the desired signal and thus errors, but that requires extra resources, especially power[5] and chip area, so variations preferably should be *corrected* as soon as possible within the frontend. For the correction we need *information* about the variations. A *smart frontend* uses redundancy for both information acquisition and correction. Alternatively, information can be obtained further on in the chain, from the digital backend or higher system layers, to correct, via a feedback, errors in the frontend [1].

Redundancy can take different forms, e.g. redundant information (like deterministic or statistic information about desired signals, undesired signals, processing errors and ambient conditions); redundant signals (e.g. test signals); redundant operations (e.g. extra comparisons in an AD converter); redundancy in the signal domains (e.g. discrete-time or discrete-level operations); and redundant capacity.

*Embedded intelligence*, as usually present at the higher system levels, will increasingly be applied on-chip, to improve hardware efficiency. Ref. [3] shows, as an example, an extremely sensitive bio-sensor frontend with an efficient embeddable smart calibration.

[5] Power is a very serious constraint in frontends, both for battery and for cooling reasons.

# System integration, towards system-level optimization

ICs always are part of a larger system, ranging from big systems like baseband stations and autonomous cars, to extremely small identification tags and IoT sensors, see Figure 7. The analog frontend should be designed in relation to the digital backend, the propagation channel, the antenna (phased arrays), supply management, energy scavenging, protocols, security, etc. Reconfigurability for multi-mode, multi-user, wideband, multiband, multi-standard, etc., are also system-level choices.

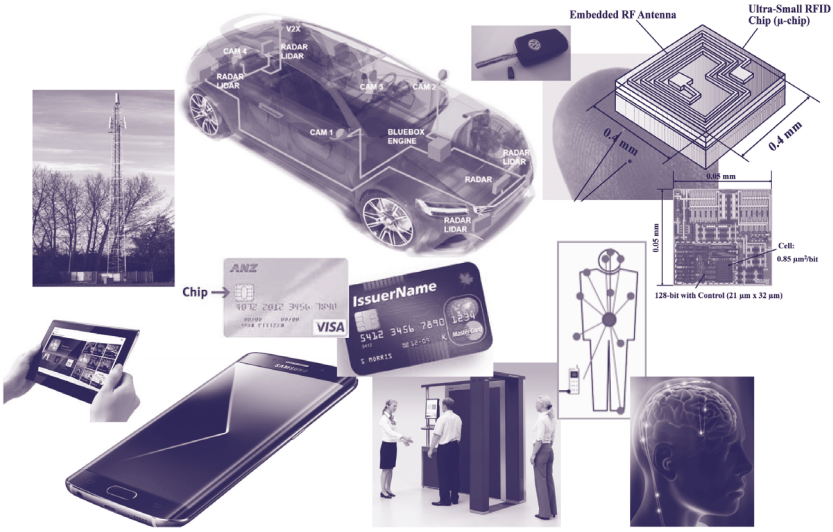


Figure 7

Electronics forms the basis for many applications in our society.

Three arbitrary examples from our group: Reference [4] shows an example of a frontend that can serve for both communication and radar application, and that includes the control and various outputs for a phased array antenna. Figure 8 shows the physical co-integration of antenna and frontend on one chip ('Antenna on Chip'), for an energy harvesting frontend[6] [5]. Reference [6] shows an example

[6] This frontend is (also) used to 'harvest' energy from the environment, to get completely rid of batteries.

of a circuit-level co-design for two sub-functions of a cellular base-station transmitter: mixing and digital to analog conversion; our integral approach enabled us to be the first to fulfill the high specs on a single chip.

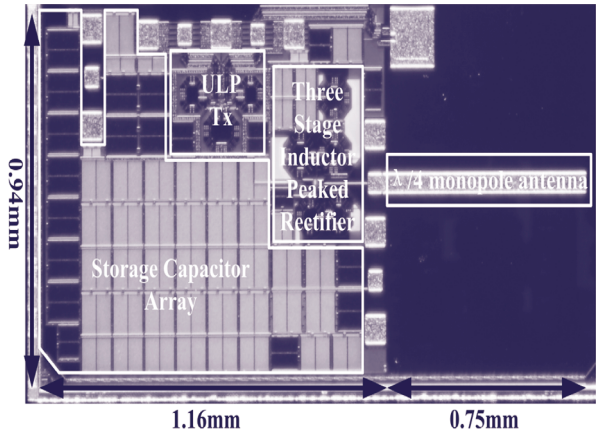


Figure 8

Millimeter-wave (60-GHz) energy-harvesting, with on-chip antenna and switch for ULP radios.

The overall system specs are indeed dependent on choices at all levels, and their mutual interactions. Moreover, information acquisition, redundancy and intelligence should be distributed over the various system levels in an optimal way. Consequently, system integration requires a strong multidisciplinary cooperation. The Mixed-signal Microelectronics group therefore participates, with other relevant groups and disciplines, in the Centre for Wireless Technology in Eindhoven (CWTe) and maintains a very strong cooperation with industry.

# More than Moore integration, the analog impact on technology

Above, we discussed the mainstream CMOS integration technology that has been following Moore's exponential law even up till now, although nanoscale effects increasingly influence its behavior. But for about 10 years already we see that the increase in transistor speed has no longer kept pace with the scaling. Moreover, the cost-per-IC reduction is declining, while interconnect bandwidth and power dissipation are becoming serious issues. Finally, atom sizes will become noticeable when we arrive at dimensions of only a few nanometers by around 2020, thereby changing the physical behavior significantly. Indeed, the ITRS roadmap [7] predicts that Moore's law will hit some walls around the next decennium, see 'Beyond CMOS' in Figure 9. The miniaturization line involves new materials, new transistor structures (like FinFet, Gate-All-Around, and tunnel transistors), and 3D integration (especially for memory devices). The focus is on miniaturization of digital (binary) basis functions, while analog has to take the technology for granted. However, the analog system, device and technology aspects have become increasingly important. That has led to a second technology development line in the ITRS roadmap, called the 'More than Moore' line.

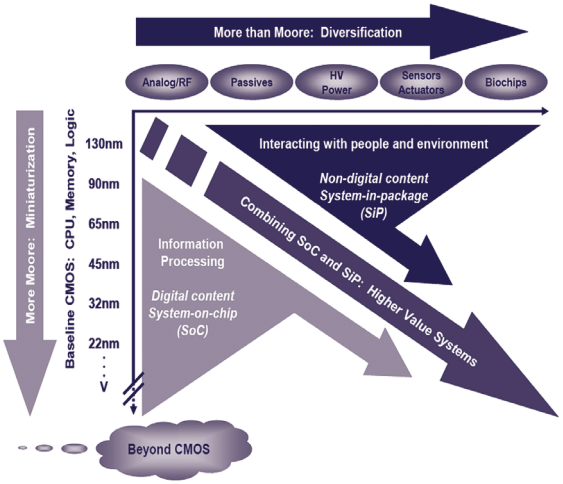


Figure 9

The two technology directions [7]: More Moore for miniaturization and More than Moore for diversification.

It focuses on diversification in technology, as it is recognized that the added value of extra technology options for analog purposes can be very high in contemporary systems.

For many years we have had CMOS technologies with electronic device options, like bipolar transistors (BiCMOS), CMOS transistors with different (low/high) thresholds, and optimized passive devices. Although these technologies lag behind for purely digital processing, they have undoubtedly added value for special (analog) applications. The More than Moore line goes further in this diversification. In the sequel I will focus on hybrid technologies and on flexible and printed electronics, and on their impact on analog.

# Hybrid integration, the best of two worlds

In hybrid technologies we combine different technologies to provide an optimal on-chip multidisciplinary integration. Analog electronics plays a crucial role here, both for interfacing with the external world, and for interfacing between the sub technologies.

Extremely small micro and nano-electromechanical systems (MEMS/NEMS) can be co-integrated in special IC technologies and perform electromechanical sensor or actuator functions, e.g. on-chip accelerometers for airbags or smartphone navigation apps. They can also be used for high-quality building blocks for analog signal processing, like resonators for filters or oscillators.

Extra chemical steps can be added in a technology to create on-chip chemical sensors, e.g. by adding a layer on top of the gate of a transistor, making it sensitive to gases, or by combining it with MEMS.

A very interesting merger is that of optics and electronics. Optoelectronics involves electronic devices for the conversion from electrons to light and vice versa, and for the control of the optic devices. Photonics is broader and involves the use of photons (the particles of light) for signal processing, transmission, generation and detection. Photronics is again one step further, combining a photonic chip with an

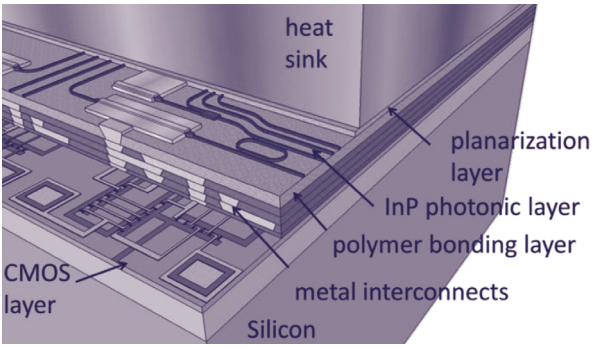


Figure 10

Photronics IC with electronic chip at the bottom and flip-chip die-bonded photonic chip on top.

electronic chip, see Figure 10. Our group cooperates in this field with the Photonic Integration group.

As a sample candidate for hybrid system integration, Figure 11 shows a terahertz (THz) set-up. THz frequencies are extremely high frequencies, in between the so-called millimeter-wave frequencies (the highest frequencies handled nowadays with electronics) and the frequencies of light, and are beyond the speeds of advanced CMOS technologies. Current THz set-ups comprise many dedicated, costly and bulky devices for THz sources, detectors, antennas, lenses, interfacing, control and millimeter-wave electronics. The addition of special high-frequency devices, as in the NXP Qubic process, together with hybrid technologies may pave the way to completely on-chip integration of THz applications, enabling a large amount of new, small and low-cost, professional and consumer applications, e.g. imaging systems for healthcare, detection systems for security, and extremely high data rate communication.

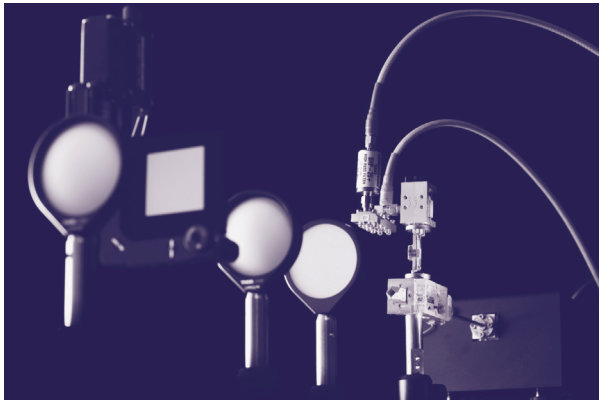

Figure 11

Hybrid THz system setup in the MsM group, subject to full on-chip integration.

# Flexible and printed integration, a different perspective

Most technologies are primarily driven by improving the electronics, but not all. In some applications, other specifications, like mechanical flexibility, large area and very low cost production, are the main drivers [8]. New and very interesting applications in this field include synthetic pressure-sensitive skins for prosthetic limbs, foldable screens, touchscreens, displays for tags, sensors in packaging, very low cost RFID, displays in tags, medical plasters, bio integrated electronics and brain interfaces. Flexible and printed technologies focus on these applications. Flexibility requires low-temperature processing, and low cost can be achieved by large-area and printing-based production. Organic semiconductors (based on molecules or compounds of molecules: oligomers, polymers) or metal-oxide semiconductors are good candidates, and are also investigated in the MsM group, see Figure 12. The focus is on realizing the best possible (cutting-edge) analog frontends, drivers and basic logic gates, by optimally matching analog electronics to the technology.

Figure 12

Flexible organic electronics in MsM.

Printing technology might even bring production of electronic hardware to the consumer home, and the strong development of 3D printers might even generate many new applications based on electronics co-printed in 3D objects.

# Nanoscale opportunities: mesoscopic and quantum integration

Having discussed the More Moore and the More than Moore lines, let's now come back to further miniaturization (Beyond Moore), and discuss which new opportunities arise if we approach atomic scales, and also link that to the analog design view.

All previous technology examples are based on macroscopic physics: they use properties of physical phenomena on a macro scale for bulk materials. In conventional electronics we use the charge property of electrons, but only for very large amounts of electrons that together create a current with a continuous range; we cannot distinguish between individual electrons. However, when we further scale down the dimensions (for lower power dissipation, higher frequencies, smaller form factor, higher processing capacity) we will approach the quantum scales, where quantum-mechanical effects (quantization, wave-particle duality, uncertainty) take place. Similar to many other disciplines, scaling provides us new quantum-mechanical options. Nanotechnology forms a broad scientific domain with all kinds of specialisms. In the context of this valedictory booklet, I will just give an impression of what future may bring for electronics (in particular analog).

### From macroscopic to mesoscopic and microscopic physics

Scaling further, the discrete number of electrons, dope atoms, etc. can no longer be ignored and, as such, the physical properties start showing a quantized character. Indeed, in current technology we already see aspects of it, like tunneling through the gate oxide (few nanometers thick), variability in doping, and mismatch problems between devices. As long as we still deal with (quantized) properties shared by a group of atoms, we talk about the mesoscopic scale, governed by the mesoscopic physics. Further scaling brings us in the regime of microscopic physics, where we deal with a relatively low number of atoms, with individual (but entangled) properties, making the quantum-mechanical effects even more dominant.

### Confinement, dimensionality

A further step in scaling can lead to confinement: the dimensions of the structure come into the same order as the (de Broglie) wavelength of the electron in its

wave model. Intuitively, you can see the electron as being confined in that dimension ('it feels imprisoned'). This comes with a lot of new properties. Confinement can be in one spatial dimension (a very thin layer, called 2-dimensional, or '2D'), in two (nanotubes or molecular strings; '1D'), or in all three (clusters of atoms, called super atoms, forming quantum dots; 'oD'). The more confinement, the more quantum-mechanical properties we see in the electrical (and other) properties.

**Coping with mesoscopic and microscopic effects**

One way of coping with mesoscopic technology-scaling effects is trying to stick with the conventional concepts (like a transistor) and trying to prevent or compensate the nanoscale effects by using 'better' materials, structures, etc. That is (more or less) what we see currently happen in the sustained downscaling in CMOS technology. However, that means fighting against physics; you force it to do what you want, because you have always done so, and of course for the very good reason that you don't want to de-invest the enormous amount of knowledge, manpower and money that has been built up in that powerful technology that you will still need for many applications. However, instead of fighting we can also try to use quantum-mechanical properties to improve the devices in our current processes, e.g. nanotube or graphene-based transistors. A lot is going on in that direction, but it falls outside the scope of this booklet. We can also go one step further, and leave the classical device functions: because of the higher resolution mesoscopic physics provides us, we can in principle acquire a far higher inherent processing power from the hardware. So, at least for the long term, it is better to 'match to the hardware' and try to use its inherent processing power optimally. In that new 'analog ball park', we can play with nanostructures (e.g. superatoms or molecules), and we will be free to choose the physical properties we like, to carry and process our information.

**2D layers, 1D tubes, metamaterials, molecular electronics, spintronics, plasmonics, photonics**

Many exotic structures with mesoscopic electron behavior (so impact on analog electronic behavior) are emerging. I will just give some examples here. *2D layers*, e.g. graphene or MoS2 [9], and *1D structures*, e.g. carbon nanotubes, are investigated for their extreme conductivity, among other things. *Metamaterials*, not present in nature, are composites created synthetically at nanoscale, with new properties, e.g. microscale transistors operating with free-space electrons like the old vacuum tubes, with extreme transconductivity [10]. In molecular nanotechnology, molecules are precisely fabricated at molecular level and used,

e.g., for mechanical applications (micro robots, micro cars), biochemical applications (chemical and biological agents, DNA tests), or electronic functions, in which case we talk about *molecular electronics*.[7] Currently the molecules mimic conventional electronic functions (molecular transistors, switches) but it might make sense to find functions that match better. In *spintronics*, the spin of the electron is used in addition to the charge property of the electron to carry, transfer, store and process our information. In current applications, the combined spins of a large amount of electrons manipulate the magnetic and electronic properties of a material. The magnetoresistive effect used in storage is a well known example. In *plasmonics*, the free electrons in a metal form a plasma that, when excited by an external EM field, can oscillate with respect to the fixed atomic grid (the ions). In quantum mechanics, these oscillations acquire a quantized character and plasmons are the quantized oscillations. These plasmonic phenomena can be used, aside for optical purposes, for electronics (antennas, modulators, etc.) and for our THz activities. *Photonics* is the quantum-mechanical part of optoelectronics; it uses the particle properties of light (photons) for signal-processing devices. For instance, strong light-material coupling in nanogrid cavities with specially designed materials can lead to 'exciton-polaritons' (half light, half matter) that improve optoelectronics [11].

**Quantum computing**

Quantum computing definitely appeals most to one's imagination, and is seen as a holy grail. A quantum-mechanical object has states that show quantized properties. A well-known example of a 'two-level' system is the spin of an electron or nucleus, that can have only two states *after measurement*: up or down. However, before the measurement, quantum mechanics describes the state as a (quantum) superposition of these two states: a linear (complex probabilistic) weighted combination of the two (final) states. This weighted combination is called a qubit, and can be seen as a vector with constant length (quantized) with *all possible angles* in a continuous 3D state space, so it can have any value on the surface of a sphere (Bloch sphere), which means a continuous, so analog, 2D domain. On top of that, atoms in each other neighborhood are 'entangled': their

[7] Chips using physical or chemical properties of molecular structures are also called bio chips, which is an ambiguous name as it can also be used for conventional electronic chips used for bio applications.

states influence each other [8]. For n atoms this means an arbitrary *superposition of all their analog quantum states*, which creates an incredibly larger processing power than digital (where n bits deliver only $2^n$ distinct states).

So, qubits differ strongly from digital bits; their superposition domain before measurement is continuous, so analog, and only after processing in the quantum computer is fulfilled, the answer is read out, causing a conversion to digital bits[9], as in a frontend at the transition from analog to digital. It is only after measurement, therefore, that the system becomes digital. So, fundamentally it acts as an analog computer[10], followed by a quantization step at detection that makes it 'robust' for further (electronic) processing. The measurements on quantum states are still very fragile and sensitive to errors and noise, which is a severe obstacle to efficient hardware integration. In several (bulky) physical test set-ups (excitation, detection, cooling, etc.), the principle of quantum computing has been shown on a few qubits (e.g. nuclear spins of a few atoms) and work is in progress to improve both robustness [12] and number of states [13].

8 Although nearby entanglement seems logical, quantum mechanics tells us that entanglement goes theoretically up to all distances, causing an enormous conflict with our intuitive feelings that are based on classical mechanics. However, current insight is that the quantum-mechanics view is right. Welcome to 'Alice in Wonderland'.

9 'Bit' in qubit confusingly refers to the (reduced) information after measurement: the bit.

10 Like early-day analog computers, but with physical carriers different from the electrons in electronics.

# Neuromorphic & cytomorphic integration, bio-inspiration

In my inaugural speech, 25 years ago, I already mentioned neural processing as a big inspiration for future processing. Now, we see some aspects of it taking off, like deep learning for translation, image processing, robots and self driving cars, among other things. In a broader sense, the morphology of all biological systems can inspire us to find more efficient structures for future integrated processing.

## Neuromorphic electronics

Current computers are digital, use 'von Neumann' architectures, and are reprogrammed for each new task. Our brains are different in almost all aspects[11]: they are not digital; use a generic 3D architecture with incredibly amounts of neurons with cell body, synapses and dendrites connected; learn continuously from each situation and for many different tasks sequentially, with the same neurons and without resetting the learned information from the past; do that based on so-called associative memory and processing; adapt continuously local properties (e.g. weights in the synapses); show diversification (clustering and mapping of types of functions to different parts of the brain); use inaccurate but massively parallel low-level neural processing; adapt and control accuracy according to the need[12] [14]; etc. The complexity, flexibility and efficiency are many orders of magnitude better than our best electronic systems, and current research shows we are still underestimating the amount of processing [15]. Fascinating, and inspiring to mimic: neuromorphic integration.

Deep learning, as researched nowadays, is just one step in that direction. Indeed, it uses a generic architecture that can learn, based on daily-life inputs and assessment of the outputs, and uses associative processing, and current research [16] sets a first step towards training without resetting the programming (catastrophic forgetting). The ideas have already been known for a long time; the enormous processing power of our computers now make it feasible, and for some

[11] The sequel is a oversimplified look on our central nervous system from a non-specialist, focusing just on the types of signal processing.

[12] In this book it is argued that our brains are continuously monitoring the probability of the outcome, and that in extreme cases, switch our thinking from the default, fast but inaccurately to slow and structured thinking that is more accurate.

highly complex functions this neural approach becomes favored over the conventional approach. However, the efficiency in terms of hardware and power is by no means comparable to the brain, and that is due to the difference in mapping to the hardware: the way the hardware is used, both in granularity (the scale) and signal processing. The details I leave to the specialists, but incoming analog signals are added, translated to the time domain via threshold functions to asynchronous spike series, with information in spatio-temporal and spatio-spectral domain, combined in an analog way in amplitude domain, translated back to time, added to spikes of other neurons in amplitude, etc., etc., and that by enormous amounts of neurons in parallel and in series.

What is important to note here is that there is mixed-signal analog processing at all levels, both continuous-time and asynchronous discrete-time, with a distributed form of redundancy (in the signal domain, and in the massively parallel/serial processing) that corrects for the variabilities and inaccuracies in the neurons and synapses and for the (local) information losses. Apparently, matching to hardware is optimized in favor of efficiency, while accuracy is achieved by proper use of redundancy at all levels in a massive strongly-connected 3D network, and by using all available and up-to-date information that enters the brain, in combination with continuous learning, which is in line with my approach discussed earlier, but applied at huge scale.

### Cytomorphic electronics

A similar discussion can be followed for all kinds of biological processes in our body: based on some form of analog processing, combined with distributed redundancy and with learning. From biologists we learn that even for a single molecule, the amount of processing is beyond our imagination. That has inspired electronic designers to learn from the morphology of cells ('cytomorphic'), to improve electronics, but also, mutually, to support biologists with analog cytomorphic simulators to speed up their research on cells.[13]

[13] Note that this is the inverse of the molecular electronics discussed earlier where electronic functions were mapped on molecules; in cytomorphic electronics, biological functions are mapped on analog electronics.

# Integrated autonomy, autonomous integration

In biology we see autonomous processes, in cells, molecules, organs, etc., combined with overall control. That makes sense: control of complexity requires distribution of control. On the chip I foresee a similar trend: we are already integrating intelligence to adapt to the environment. The next step will be autonomous chips, integrated with such an intelligence that they can operate autonomously. A further step will be autonomous integration: chips that can autonomously heal themselves, reassemble, compile, expand, reproduce, etc., as in the living world. We see already some aspects at the digital system levels, with e.g. robots; similar evolutions are possible at the lower analog electronics levels on chips, especially if we take into account combinations of previous trends (intelligence; hybrid integration with on-chip detectors and actuators; further nanoscaling; cytomorphic, neuromorphic and molecular electronics). Futuristic? Yes. But no fundamental boundaries.

# Scientific and societal integration

Electronics has penetrated into the veins of our society and nano-electronics will penetrate further, even into the veins of our body. Our future: intelligent robots and cars around us; intelligent and self-reproducing chips; molecular electronics; bionics: deep brain stimulation, brain-computer interfaces, neuroprosthetics; and so on. Even the sky is not the limit.

However, at this point, I would like to put the role of electronics into perspective. Many more scientific disciplines are contributing and many of them accelerating at a degree we haven't seen before, and all these disciplines are increasingly and mutually affecting each other. That raises a lot of challenges and questions. Are we at a crossroads? Can we technically maintain control, or will autonomous intelligence around us take over? And in a broader sense, can society control technical developments that go faster than society can follow? Science plays and should play a strong role but, unfortunately, its credibility is currently under debate. On the other hand, every scientist should see his knowledge in perspective, as fundamentally bounded by models, and be open to the mystery of life. As such, 'hard' science is, strictly seen, a misnomer, and a 'scientific' assessment of religions is fundamentally unscientific. It requires sense of perspective, mutual respect and a combined effort of alpha, beta and gamma disciplines, politics and the whole of society to tackle the growing bifurcations in terms of high/low educated, rich/poor people, open/closed societies, real/alternative facts, etc. Also there, it is all about integration...!

# Thanks

Looking back, I feel privileged that I have been able to share the exponential growth of electronics from almost the beginning to where we are now: at the verge of many new nano-based developments. I also feel it as a great privilege that I could contribute to the academic education of so many young people, from all over the world, not only to prepare them for their own technical career, but also for their broader task in our society.

I thank Philips, TUD and TU/e for the marvelous jobs. I thank all colleagues, relations, students, PDEngs and PhDs, for their cooperation over 42 years, in a field where you cannot do much on your own. You taught me a lot, in electronics, science and life, and it has been a great pleasure to work with you. I also thank STW, the industry and the EU for their financial support.

I want to thank explicitly all members of MsM: you were more than colleagues, you were and still are great friends. Thank you all for the great time, your trust in me, the fantastic atmosphere.

I'll miss this all, but I look forward to a new period, with more time for other aspects of life. More time with my family. And last but not least: thanks Marianne, for your support through all the years!

Ik heb gezegd.

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# Curriculum Vitae

**On October 1, 1999 Prof.dr.ir. Arthur van Roermund was appointed full professor in Mixed-signal Microelectronics in the department of Electrical Engineering at the Eindhoven University of Technology.**

After a 42-year career, the last 25 years of which have been as a full professor at the university, Arthur van Roermund is now approaching his retirement. In 1974 he joined Philips NatLab to fulfill his final project as a Master student of Electrical Engineering at Delft University. After his graduation in 1975, he stayed with Philips NatLab until 1992, when he exchanged the business world for the academic world. He became chairman of the Electronics group at Delft University, and switched to Eindhoven University in 1999, to chair the Mixed-signal Micro-electronics group. From 2002 to 2012 he was also member of the Electrical Engineering Departmental Board in Eindhoven. Professionally, he started in the analog electronics field, specializing in switched-capacitor circuits, a field in which he obtained his PhD degree from KU Leuven, Belgium. He then broadened his scope as a project leader within Philips to digital electronics, processor design and scheduling, video processing and system-level research before finally refocusing on analog and mixed-signal electronics during his last 25 years at the university.
In 2004 he gained the 'Simon Stevin Meester' award for his scientific and technological achievements. He has been a member of several national and international boards and advisory and assessment panels. He has (co)authored over 700 articles and 30 books, and is co-editor of another 11 books.

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