Ring resonator based integrated photonic circuits

Ring Resonator based Integrated Photonic Circuits

PROEFSCHRIFT

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“ If I have seen further, it is by standing on the shoulders of giants. ”

by Isaac Newton

Summary

Essay on Ring Resonator based Integrated Photonic Circuits

The research activities described herein are carried out as a part of the SmartLight project funded by The Dutch Technology Foundation (STW) which aims at developing the science and enhancing the technology for future generations of ultra-fast, low power and high connectivity photonic integrated circuit (PIC)s. Processing of ultra-fast signals and handling of big data for future systems is a major cause of concern and this spans across a variety of fields starting from medical science to internet networks. The internet backbone has the capability to process Tbps information but on a grander scale of things, computer processors which are limited to a few GHz, limit the system and lead to network congestion. Currently, the limited processing of signals has been dealt with by parallel processing but in regards to future demands, the energy and cost associated with the technique will limit the processing capabilities. In this regard, the goal of my PhD project has been to provide high scale optical switching matrices to provide data path control based on the switch element resonance. A path to low energy, high throughput and high data rate circuits has been identified which will overcome the aforementioned issues. The main topics of this thesis is the design, fabrication and characterization of sophisticated cross-point matrices, by using Micro-ring Resonator (MRR)s based switching elements. In the effort to realize large scale, low-loss and energy efficient photonic integrated circuits meant to cope with the incessant increase in bandwidth and energy efficiency demands of future networks, different material platforms have been explored. The main contributions of the work may be categorised as:

1. Large scale switch matrix based on fifth-order resonators have been

fabricated and demonstrated in Silicon-on-Insulator (SOI) platform. The design allows the circuit to cope with the dimensional errors induced during fabrication so that it can be fabricated using standard fabrication techniques. The connectivity achieved in the 8×4 switch matrix makes it the largest resonator based switch circuits demonstrated to date.

2. Sub-system level demonstrations of the fifth-order resonator based circuit include:

   (a) 10Gbps routing through the entire 8×4 switch matrix

   (b) 40Gbps routing through representative paths

   (c) Simultaneous dynamic routing from multiple inputs to multiple outputs

   (d) Simultaneous generation and routing of millimeter-wave (mm-wave) signals

   Higher speed data routing at low power penalties are very promising for such circuits. Moreover, the simultaneous multi-path routing involving as many as 8 different path combinations is a demonstration which is first of its kind.

3. Third-order resonators based on active-passive integrated InP platform allows the realization of faster switch matrices accompanied by lower energy consumption per switch element and potentially faster switching time of order of nanoseconds. The fabricated circuit and the 4 different paths tested across the prototype imply that this demonstration itself is also a first on its own. Switch element losses limit the scalability of this circuit and hence the origin of the losses are analysed and a low loss new design comprising of smaller resonator is proposed.

4. 3D integration of resonator based devices are simulated in order to provide a fabrication tolerant, wafer bonding free, dual-plane, high performance photonics platform. The performance is seen to be comparable with state-of-the-art devices and for this part, the resonance is explored as it is suitable for dense wavelength division multiplexing circuits.

Contents

Chapter 1

Introduction

1.1 Connected World

Optical communication has led to the establishment of communication links around the world using a mesh of networks. The exponential increase in the number of connected devices and the usage of the internet as a whole, particularly in terms of video streaming [1, 2], social networking [3, 4] and cloud computing [5], has burdened the existing infra-structure which is approaching the limits of its capacity [6, 7]. Increasingly, software and services are provided remotely from users leading to new networking bottlenecks. Moreover, to cope with this rise in traffic, complexity in networks is constantly increasing [8] leading to unsustainable energy consumption in them [9, 10]. In order to deal with these issues, network resources need to be dynamically reconfigured, allowing the use of network virtualisation along with improved schemes for network control and management. Optical switching can be used as a means to implement smart optical packet routing systems which can aid in this process. The possibility of achieving low latency, high bandwidth and controllable switch mechanism units has proved to be particularly challenging, especially at the optical link layer.

Fig. 1.1 is a schematic presented by Tarutani *et al.* [11] and an example of possible future networks using photonic switch matrices and wavelength selective components which can help in overcoming the bandwidth bottleneck issues and cope with future network demands. It shows a network configuration in data centres with the network being capable of operating in an energy-efficient way. In this configuration, the data centre, represented as server racks can be seen at the heart of the network and a migration from

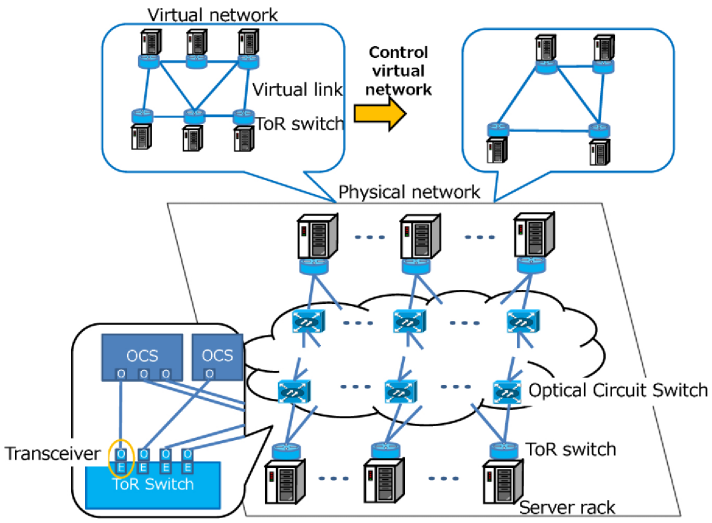


Figure 1.1: Network architecture [11].

previously established point to point and metro rings to peer to peer mesh networks and flattened hierarchy schemes is also visible with the link to the physical network made via a collection of optical switches. Moreover, all the network elements are placed at different spatial locations. This is possible because the optical medium involved allows the computing and storage units to be located at arbitrary sites leading to network virtualisation as utilised in this scheme and other similar architectures.

One of the major reasons for the increase in network congestion is the high amount of data that is required to be accessed and processed. Big data is a broad term related to this and it stands for data sets so large or complex that traditional data processing applications are inadequate to cope with it. The analysis of the data sets is increasing from its applications in combating financial fraud through to the spotting of business trends and combating crime [12] as well as in biomedical studies, all of which require unprecedented computational power.

Moreover, in and around the year 2000, a quarter of the world's stored information was digital and the rest was in the form of books and other analogue media - today, less than two percent of all the information in the world is non-digital. The data may vary from content related to medical sciences and astronomy to streamable videos and infotainment to contents related to social networking. No matter what the content, it is undeniable

that the collection of digital data is truly massive. While we access more and more of this data in our daily lives, increasingly using multiple mobile or nomadic devices, a very large demand is placed on existing networks to cope with the needs of today. Following this exponential increase in data usage, future networks are required which are capable of coping with the same.

The same challenges are present in the data centre and super computer environment and throughout the modern internet. Power consumptions of modern-day super computers are between 4-6MW - an electricity demand so high that it can be used to supply around 5000 homes. The latest super computer which is in the process of being built is called Blue Waters and it is being carried out as a result of the collaboration between researchers at the University of Illinois at Urbana-Champaigns National Centre for Supercomputing Applications, IBM, and the Great Lakes Consortium for Petascale Computation. By factoring in the power consumption of the cooling units, the operation of such a machine is expected to consume around 15MW or more in total [13].

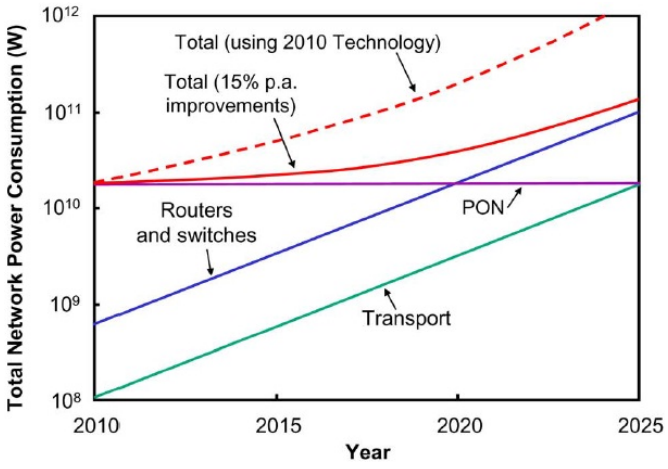


Figure 1.2: Total power consumption of the network, based on a top-down analysis assuming a 15% p.a. improvement in equipment energy efficiency, a 50% p.a. growth in access rate, a 10% p.a. growth in the number of users, and a user base of 1.8 billion in 2010. The average hop count in the network is 20 [14].

The energy required to shuffle data around between different chips or boards or racks is significantly larger than the energy required to perform

a mathematical operation. A 64 bit result is produced as a consequence of a typical floating-point operation between two 64 bit numbers. Thus, 200 bits of information are likely to be moved in this case, multiple times, in and out of some form of memory. Using conventional architecture and keeping all the additional overhead in mind, the best we could have achieved is a exaflop-class machine by 2015 which would consume around 1000-10000pJ per flop [13].

Fig. 1.2, based on the work done by Tucker [14] further illustrates the fact that low power consumption in components are especially required to keep the power consumption of the entire network in tact within thermal design limits. With a advancements in technology and considering a 15% per annum improvement, the power consumption between 2002 and 2025 is expected to increase to around 7% of the global electricity supply. Several devices have been investigated in the past to provide the required high performance at low energy cost and optical switches and wavelength selective elements are one of them.

1.2 Optical Switch Node

A crucial component in the schematic show in Fig. 1.1 is the optical switch node which helps to aggregate, disaggregate and route data in the optical domain. These switch nodes are electrically controlled and have different requirements based on where they are located. The number of switch nodes at the bottom levels of the schematic are greater than those in the backbone but the data rate requirements in the former are also lower as compared to the latter. An increase in the power dissipation in electronic switches beyond 40Gbps per channel data rates implies that they cannot adhere to the end-to-end bandwidth demands. However, optical switches can provide the required data rates as well as eliminate the need for optical to electrical connections at the switch interfaces which reduces network complexity as well as the cost associated with it. Hence, telecommunication systems [15], access networks [16], high performance computers [17] and optical interconnects [18] of the future demand the development of fast and reconfigurable Wavelength division multiplexing (WDM) optical switches. The commonly used methods of achieving such routing are as follows:

The first method deals with routers formed by a combination of N×N Arrayed Waveguide Grating (AWG)s as routers along with a tunable transceiver with fixed wavelength filters [15, 19]. In this method, tuning the wavelength

at any of the inputs allows the signal to be routed to one of the N outputs as desired which forms the basis of this approach. However, the requirement of electrically tuned lasers with tuning speeds in the order of a few nanoseconds limits the tunability that can be achieved. Placing tunable wavelength converters at each AWG input is an alternative [20, 21] but as far as single wavelength operation per port is concerned, the scaling of the bandwidth is limited. A broadcast and select architecture with an on-chip wavelength converter can also be used as different wavelengths in this scenario represent a distinct link. However the energy consumption greatly restricts the scalability of such a layout. An alternate approach to this can be achieved by heterogeneous integration of AWGs used for multiplexing and de-multiplexing wavelength channels in combination with semiconductor optical amplifier (SOA)s for gated control. Digital control of such circuits in a scalable manner and a relatively low number of SOA gates has been demonstrated [22–24] as well as circuits capable of establishing a few 100's of connections [25, 26]. A combination of gated SOAs and AWGs can also be used as reconfigurable optical switch elements. Fast and wideband routing using phase shifter aligned to the AWGs have been demonstrated [24, 27]. However their usage is hindered by issues such as the complexity in control and the increase in energy consumption for high port count circuits.

Multiplexers, optical switches and de-multiplexers can be used in series to form another route to achieve wavelength selective circuits.Various input channels are used to continuously fed an optical signal to a switch element which is either attenuated or routed individually to any one of the N output ports in a manner which is scalable and cost effective. They are programmable in terms of space and wavelength routing and allow multi-channel operations along with parallel processing and the ability to control every wavelength channel rendering the scope for optical bandwidth management [28]. Such optical switch matrices and wavelength selective switches have been shown to have a broad bandwidth while requiring low power for their operation. Current optical switches usually rely on slow, millisecond switching time, LCOS [29, 30] technology or MEMS [31, 32]. MEMS based technology has been used to demonstrate connectivity between hundreds to thousands of ports [33–36] while LCOS based switches are limited to a few tens of ports [29, 30]. The combination of wavelength selective elements and broadband photonic switches promise a route to achieve even larger scale switches with faster switching times but this comes

at the cost of increased design and layer control complexity.

The last method relies on using tunable filters such as either Fabry-Perot cavities [37], Bragg gratings [38, 39], phased array waveguides [22, 25], Mach-Zehnder interferometer (MZI)s [40–42] or ring resonators [43, 44]. Restrictions imposed by the fabrication tolerance in Fabry-Perot cavities and Bragg gratings limit their scalability and renders them undesirable for large scale circuits. Fast programming and wideband unicast routing of up to 16 output ports have been demonstrated using electro-optic phase shifters and arrayed waveguides [45]. However, the scalability and simplicity in control of MZIs and ring resonator based tunable filters make them more desirable compared to the others. MZI are sensitive to the power splitting ratio of its two couplers which greatly limit the signal extinction.

A possible route to achieve the required high performance while meeting the energy efficiency demands is envisaged by creating energy efficient optical routing devices using ring resonators. In Section 1.3.1, a few examples of such devices used for different functionalities have been shown in order to list the advantages and to assess the challenges presented by these devices.

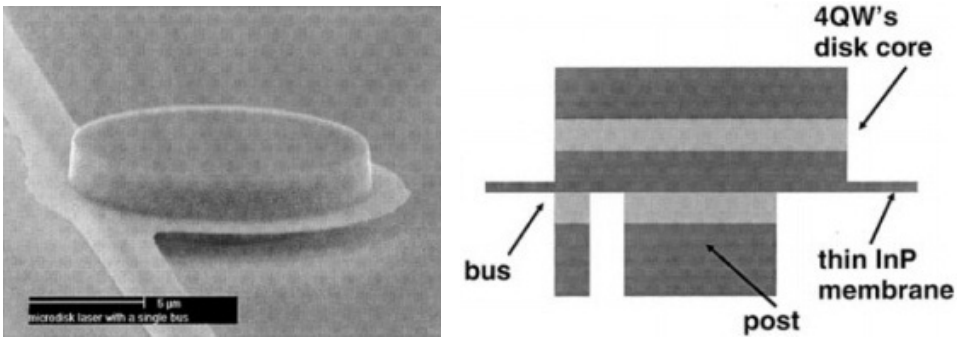
1.3 Resonant Photonics

Cavities are widely used to enhance electro-optic phenomena, but they can pose profound challenges in integrated circuit design. Researchers are devising increasingly elaborate techniques to facilitate reproducible coupling and reflection coefficients. The alignment of sharp spectral features is particularly problematic for the most efficient cavities. Nonetheless, there is considerable opportunity for enhanced energy efficiency.

1.3.1 State-of-the-art Micro-ring Resonator Devices

A lot of work has been done demonstrating energy efficient, high performance micro-ring resonator based optical devices. In this section, the micro-ring resonator based photonic devices have been classified based on their functionality and one key example has been used for each of these cases to analyse their performance, highlight the advances made and to pin point the need for improvement.

Micro-disc Lasers The work done on micro-disc lasers by Choi *et al.* [46] stands out as an example of lasers, demonstrating high performance with low power consumption. An image of the fabricated device is shown in Fig. 1.3a. This work relies on utilising a structure with two optically confining waveguide layers in the same cross-section - a bus waveguide located at the bottom optically confining plane which is evanescently coupled into a micro-disc located at the top optically confining plane as shown in Fig. 1.3b. The separation and hence the coupling between the two layers is governed by the spacer layer in between them which in turn is defined during the growth of the materials. Micro-disc lasers of different radii have been fabricated with the 8μm micro-disc quantified to have laser thresholds in the order of mA's while having a side mode suppression ratio greater than 30dB.



(a) (b)

Figure 1.3: (a) SEM image and (b) schematic cross-sectional view of the micro-disk vertically coupled to a bus waveguide [46].

The fact that the spacer layer and hence the separation between the two optically confining layers is defined during the growth process is supposed to make the device highly tolerant to fabrication variations. However, variations do occur due to the nominal variations in grown layer thickness and due to the misalignment between the bus waveguide and micro-disc which changes the spectral shape and emission wavelength of such devices.

Micro-ring Modulator The work done by Xu *et al.* [47] has been used as an example of micro-ring modulator performance. This work relies on lateral coupling where a bus waveguide couples into a micro-ring resonator as shown in Fig. 1.4 and the resultant spectra is tuned using injection based

electro-optic modulation. The inner part of the micro-ring, depicted in blue is p-doped and the outer part, depicted in yellow, is n-doped and allow for the fabrication of the two contacts required for current injection. The modulator is operated at a maximum of 104μW of power and experimental demonstrations at 12.5Gbps reveal an extinction ratio of 9dB or more.

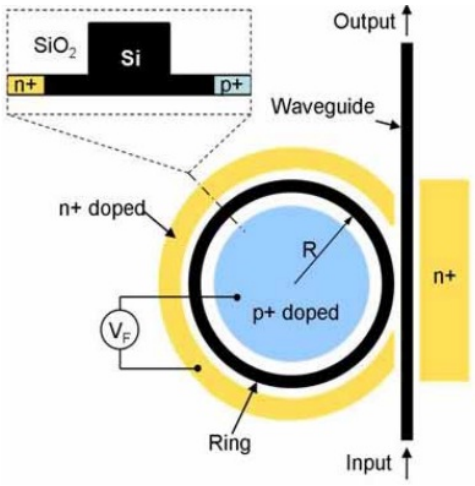
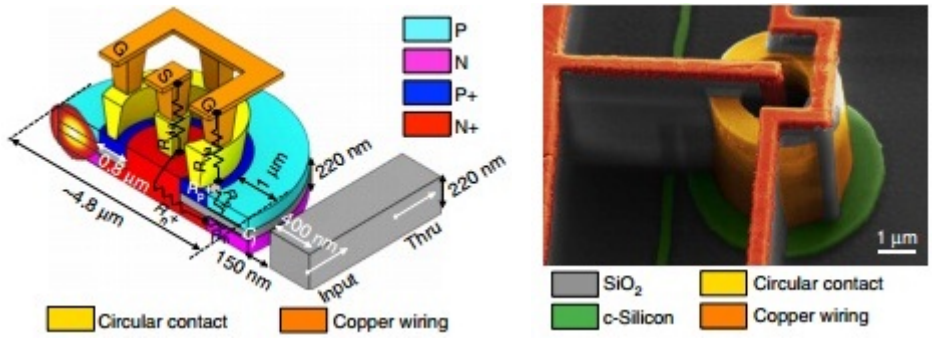


Figure 1.4: Schematic of the device structure [47].

The performance of this device is restricted because of two major factors - Firstly, such single order resonators are extremely prone to fabrication variations [48] which limit their utilisation in large scale PICs. Secondly, the extinction ratio of such devices is also limited as demonstrated by the 9dB extinction in this case. This limitation is owing to a trade-off between the device pass bandwidth and the extinction ratio observed in single-order resonators [48].

Athermalised Modulators Timurdogan *et al.* [49] have demonstrated an athermal silicon modulator based on lateral coupling and the device layout has been shown in Fig. 1.5. High speed modulation at 25Gbps has been shown in this with a low voltage of operation of 0.5V peak-to-peak leading to a nominal power consumption of 0.9fJ per bit. The key performance enhancement in this device is achieved by enhancing the electro-optic response which is enabled by using a vertical p-n junction and thus overlapping the p+ and n+ regions within the micro-disc centre which also results

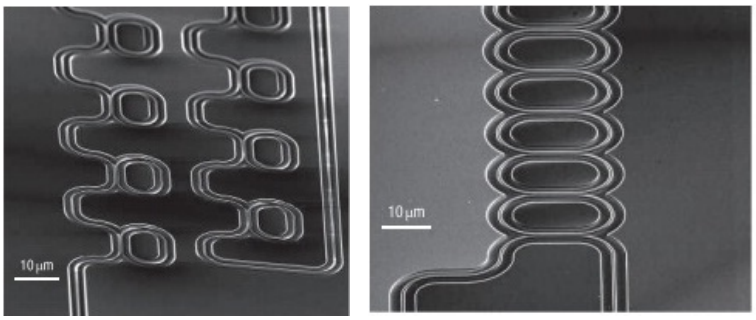
in minimising the device resistance. Thus, a highly efficient phase shift of 250pm/V is achieved. This high efficiency has then been further utilised to compensate for thermal drifts within a temperature range of 7.5°C. As PICs, especially majority of the demonstrated resonator based circuits are plagued by thermal drifts, athermal operation is key in achieving large scale circuits.



(a) (b)

Figure 1.5: (a) A three-dimensional sketch of the electro-optic silicon microdisk modulator. (b) A scanning electron microscopy image of the silicon microdisk modulator [49].

Optical Buffers Xia *et al.* [50] have used laterally coupled higher-order resonators as delay lines.



(a) (b)

Figure 1.6: (a) Delay line consisting of several ring resonators in an all pass filter configuration in a cascade. (b) Delay line composed of several resonators cascaded in a coupled resonator optical waveguide configuration. [50].

56 cascaded rings in an all pass filter configuration (Fig. 1.6a) and hundredth-order coupled optical waveguide configuration (Fig. 1.6b) have been used for this purpose. The device footprints achieved in both the demonstrations are significantly smaller than those of a 4cm bent photonics wire along with longer delays per unit area. However, these advances come at the cost of increased insertion loss and lower bandwidth as compared to a 4cm bent photonic wire. The demonstrated delay lines are capable of buffering over 1 Byte of information which is suitable for storing one ASCII character.

The size as related to the functionality achieved in such kind of devices still remains an issue. While the density achieved is 10 times smaller than that of conventional floppy disks, the device size is still significantly larger when compared to more current standards such as flash memory.

Optical Memory Hill *et al.* [51] use a waveguide laterally coupled into two micro-ring resonators. This work demonstrates optical memory based

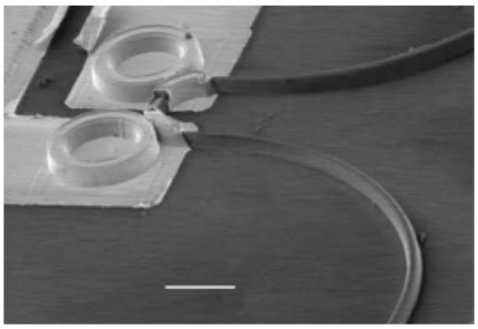


Figure 1.7: A memory element formed by two 16μm diameter micro-ring lasers coupled via a waveguide on a InP/InGaAsP photonic integrated circuit [51].

on micro-ring lasers using the clockwise and anti-clockwise lasing modes in such lasers. The device with a small footprint of $18\times40\mu m^2$, as shown in Fig. 1.7, is used fabricated this purpose. High speeds of 20ps have been shown in such devices along with a nominal energy consumption of 5.5fJ for optical switching.

Optical Switches In the work of Vlasov *et al.* [52], a fifth-order laterally coupled ring resonator is demonstrated as a route to achieve broadband fabrication tolerant switches. One input and one output bus is located on

either end of the resonator which consists of 5 racetrack sections coupled with six directional couplers, giving rise to the fifth-order switch element as shown in Fig. 1.8. The fifth-order of the resonator is used to maximise both the pass bandwidth and the on-off signal extinction with the demonstrated device having a bandwidth of 300GHz and extinction of 17dB. Moreover, the possibility of high bandwidth routing is also demonstrated by passing data at 40Gbps.

Although this device concept is attractive due to its improved performance, the fact remains that large scale PICs using higher-order resonators have, as of yet, to be demonstrated.

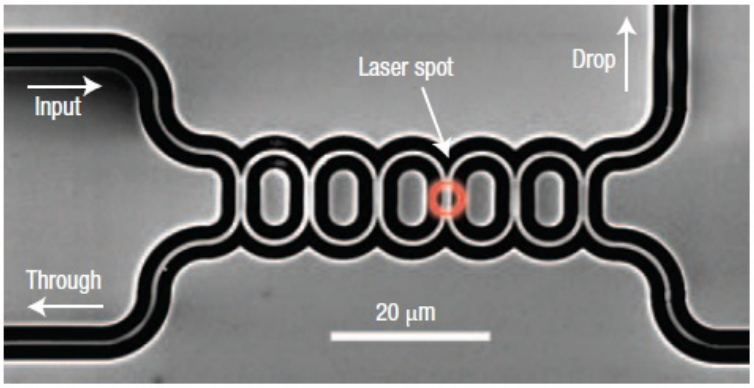


Figure 1.8: Top-down view of the fifth-order ring resonator switch [52].

Integration with Electronics Electrical to optical and optical to electrical conversion is an intense research topic as far as PICs are concerned. The demonstration by Assefa *et al.* [53] is one in which they fabricate and measure optical modulators and Ge photodetectors as a part of a transceiver circuit as shown in Fig. 1.9. This is achieved using 90nm CMOS-integrated technology and the yields have led to demonstration of low power consumption, multi-channel, WDM transceivers operating at 25Gbps.

The devices discussed in Section 1.3.1 have shown great promise as far as developing high performance, low power consumption devices are concerned. However, large scale circuit implementations using such micro-ring and micro-disc resonators have yet to be demonstrated and this is mostly limited by the high fabrication intolerance associated with resonant devices. In this thesis, fabrication tolerant resonators for PICs are explored in the

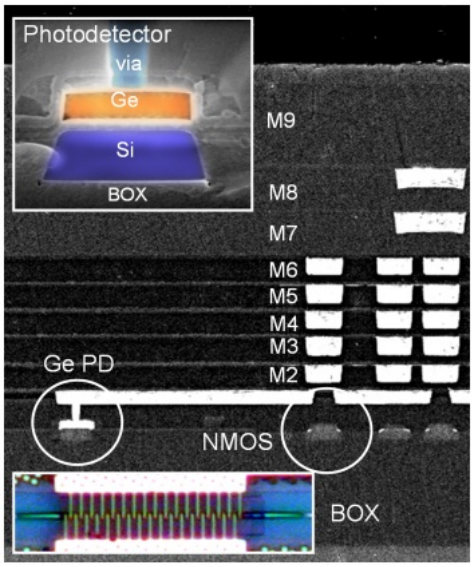


Figure 1.9: Cross-sectional SEM view of a 90nm CINP metal stack with Ge PD embedded into the front-end. Zoomed-in image of a photodetector is shown on top left. Optical microscope top-down image is shown on the low left [53].

form of higher order resonators in Chapter 2, Chapter 3 and Chapter 4 and a vertically coupled resonator in Chapter 5.

In the following sections, the principle of operation of micro-ring resonators is provided and then the challenges involved in developing such large scale PICs are addressed. This is followed by a description of the two different material platforms that were explored for the designs and fabrications presented in this thesis.

1.3.2 Micro-ring Resonators

As discussed in the previous section, a lot of theoretical and experimental studies have been done previously in order to better understand the principle of operation of resonant device [54–57]. Further to the previous section, a few key features related to this thesis have been highlighted in this section in order to put the content in the following chapters into perspective.

Fig. 1.10 shows a schematic of a typical single-order ring resonator. Multiple wavelengths are injected at the Input Port of such a device and partially coupled into the resonant ring and out of it through the Coupling

Region. Depending on the coupler design, as specified by Equation 1.1, certain wavelengths (λ_1) satisfy the resonant condition and are enhanced because of constructive interference in the closed loop system while the others (λ_2 and λ_3) are suppressed at the Drop Port.

$$n_{eff}L = m\lambda_1 \tag{1.1}$$

where, n_{eff} is the effective index of the waveguide and is dependant on the material platform, L is the circumference of the resonator and a design parameter and m is an integer.

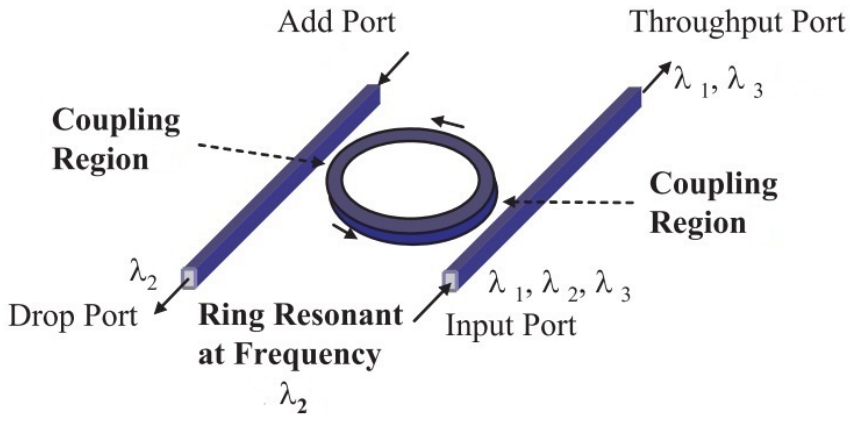


Figure 1.10: Schematic of a single-order ring resonator [58]

There are two key parameters for quantifying a ring resonator which are:

- Free Spectral Range (FSR): The FSR of a resonator is defined using Equation1.2 as follows:

$$FSR = \frac{{\lambda_1}^2}{n_g L} \tag{1.2}$$

  where, n_g is the group index of the waveguide and is dependant on the material platform, L is the circumference of the resonator and a design parameter and m is an integer.

  The FSR represents the periodicity of the output spectra of a resonator as shown in Fig. 1.11 and it is inversely proportional to the size of the resonator. In a material system with a fixed effective index,

the FSR can be varied by varying the circumference of the resonator. The percentage of light that evanescently couples from the waveguide into the resonator, termed as the coupling coefficient also determines the passband width of a resonator with a fixed FSR.

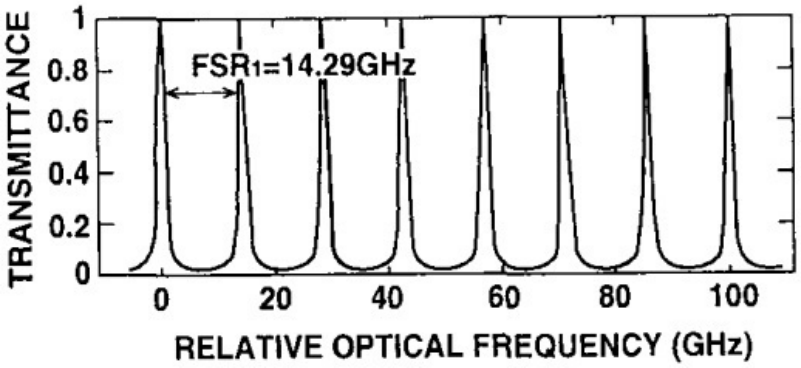


Figure 1.11: Schematic of a single-order ring resonator [59]

- Tuning of a resonator spectra is required to either tune the different phase-mismatched arms of a higher-order resonator with respect to each other or to tune the whole resonator with respect to the wavelength of operation so as to enable switch actuation or modulation. In particular, application of resonators in large scale circuits demands the presence of a tuning mechanism and its effectiveness plays a major role as well. The tuning efficiency itself is a fixed parameter for a given material system and a fixed tuning mechanism which can either be thermo-optic, electro-optic (only for InP materials) or electro-absorption or free-carrier injection based. However, the total tuning achieved in a resonator scales proportionally with the length over which it is tuned which implies that in order to achieve a minimum desired tuning range, the resonator has to be of a certain length. Hence, there is a trade-off between the FSR that can be achieved and the desired phase shift in each resonator and both these considerations have to be kept in play while fixing the resonator length and hence its circumference.

In a resonant micro-ring element, light coupled into the micro-ring, passes through the resonator multiple number of times. The multiple num-

ber of passes through the tuning or gain region lowers the pumping requirements for tuning or gain in such circuits as well as the heat dissipation and improves the device performance and power consumption.

Table 1.1: Comparison if state-of-the-art switches and modulators

Publication	Type	V_{pp} (in V)	Area (in μm^2)	Speed (in Gbps)	E.R. (in dB)	Electrical Energy (in fJ/bit)
Green *et al* [60]	MZM[a]	7.6	1000	10	6.0	5000
Liu *et al* [61]	EAM[c]	3.0	200	1.2	8.0	50
Yang *et al* [62]	MZM	-	-	-	15	16.3
Rohit *et al* [63]	SOA	-	22500	-	15	300
Dong *et al* [64]	Ring	1.0	1200	10.0	6.0	10
Watts *et al* [65]	Disk	1.0	10	12.5	3.2	3
Hofrichter *et al* [66]	Disk	1.6	50	10.0	4.5	43

E.R. = Extinction Ratio

a = Mach-Zehnder modulator

b = Electroabsorption modulator

The advantages of micro-ring resonators as compared to other commonly used devices is further illustrated using the example presented by Hofrichter *et al* in [66] along with other examples of state-of-the-art devices. The comparison is shown in Table 1.1 which lists Mach-Zehnder modulator, electro-absorption modulator, SOA and ring (and disk) resonators in relation to the performance achieved. The analysis is performed in terms of the voltage of operation, the area, the line-rate achieved, the extinction ratio and the energy consumption. It can be clearly seen from the comparison that although the line-rates and the extinction ratio achieved in most of the examples are quite similar, the ring resonator demonstrated by Watts *et al* easily outperform the others in terms of the peak-to-peak voltage required for operation and the energy consumed. This illustrates the claims of improved energy efficiency without comprising device performance achieved in ring resonator devices and motivates further the choice of micro-ring and micro-disks as a choice for low-power high performance devices which can be potentially applied in Dense wavelength division multiplexing (DWDM) systems.

1.4 Challenges

The aforementioned advantages have led to the fabrication of micro-ring resonators across a variety of platforms and demonstrating devices such as filters, switches, multiplexers, modulators and lasers [44, 47, 48, 51, 52, 66–115]. However, micro-ring resonators, especially single-order micro-rings, are extremely susceptible to variations in fabricated waveguide dimensions. The variations may be related to either feature size variations attributed to the fabrication process or to variations in the thickness of the grown layers. The sensitivity is so high that nanometre scale variations translate directly into similar shifts in the wavelength of operation of such devices [48, 71]. This has greatly limited the application of micro-ring resonators and poses a threat to the application of such devices as functional blocks in large scale circuits. In this thesis, new schemes for relaxing the tolerance of the device performance to fabrication variations have been explored. These are then used to provide a viable route for large scale circuits.

1.5 Material Platforms

There are several material platforms on offer for the fabrication of monolithically integrated photonic devices and circuits, key amongst them being SOI [116], InP-InGaAsP [117]. In this section, the relative advantages of each platform used has been provided.

1.5.1 Silicon Photonics

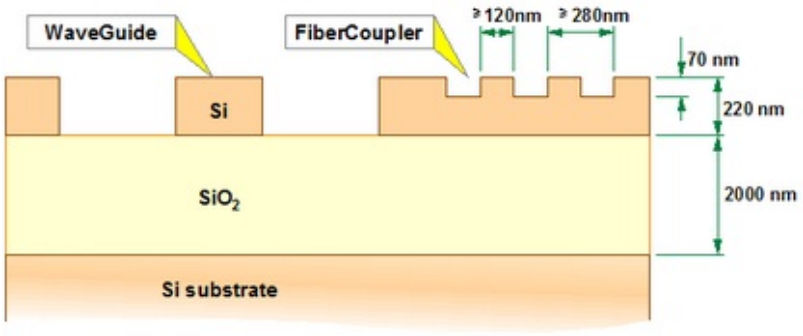


Figure 1.12: Schematic of a single-order ring resonator [116]

Fig. 1.12 shows the basic waveguide layout used in SOI based photonics, as provided by the ePIXfab foundry [116]. Silicon forms the high refractive index, optically confining layer and is placed on top of a buried SiO_2 cladding and the top cladding may be either air or SiO_2, as per design. The high index contrast afforded by a combination of silicon waveguides and the cladding used, allows for the realisation of extremely low bend radius waveguides with negligible micro-bend losses which is in the order of losses incurred by the straight waveguides [116]. Although lasers are not readily available on this platform, hybrid heterogeneous integration with III-V materials might be seen as a possible solution to that. Doped Si-Ge structures have also been useful for fabricating modulators and photodiodes, with the former having a V_π of 8.5V for 1.5mm long modulators [116]. Another approach in inducing phase shift in such structures is by using thermo-optic micro-heaters on top of the silicon waveguides. Coupling in and out of the PIC may be achieved by using either 1D surface grating couplers which are polarisation dependant but have lower fibre-to-chip coupling loss or by using 2D surface grating couplers which allow the possibility of incorporating polarisation diversity, at the cost of increased fibre-to-chip coupling loss. One of the major advantages of the platform itself is the fact that it exploits the mature CMOS foundry process in order to achieve a far greater line-width uniformity as compared ot other platforms.

1.5.2 InP Integrated Photonics

The InP platform offers multiple functionalities because of its ability to incorporate both purely passive and active waveguides within the same PIC. The ability to incorporate lasers, optical amplifiers, modulators and detectors allow for a higher degree of complexity to be achieved in such PICs. The possibility of two different etch depths further enhances its prospects. However, the relatively lower index contrast, as compared to SOI does lead to larger bend radii in waveguides. Fibre-to-chip coupling is achieved by using lensed fibres coupled onto cleaved waveguide facets. The challenges in packaging and the cost associated have been dealt with by foundry approaches such as JePPIX [117].

1.6 Preview of the Thesis

In this thesis, different in-plane and vertically coupled ring and disc based resonators designs are presented across both SOI and InP platform. The

design challenges are addressed and a possible means to achieve large scale PICs while keeping in mind the demands of future networks are explored. The following sections of the thesis have been classified into different chapters described as follows:

Chapter Two includes the design of a fifth-order resonator based switch matrix on SOI platform. The elements of the switch matrix are analysed in comparison with theoretical predictions and their tuning-efficiency is assessed. The switches are then studied quantitatively in terms of the voltage of operation, the switch spectra, the optical losses, the signal extinction and the thermal crosstalk between elements.

Chapter Three includes data routing across multiple-paths of the SOI switch matrix circuit, initially under static condition. A voltage driver control block is then developed for dynamic control of the circuit and the switch speeds are assessed. Simultaneous multi-path routing is then performed to test the data integrity under switched condition. Calibration of the gating window signifying the usable section of the switched data is then carried out through generation and routing of mm-wave signal and this part of the work is done in collaboration with Dr. Shihuan (Jim) Zou, a former member of the ECO Group, Technische Universiteit Eindhoven.

Chapter Four deals with the design of a third-order resonator based switch matrix on InP platform. Each switch element is analysed in terms of its spectra along with the phase modulation efficiency. The origins of the elemental losses are analysed and a new low-loss design is proposed. A proof-of-concept data routing experiment is then performed across two different path combinations

Chapter Five involves the design of a vertically coupled micro-ring resonator. The device concept is first presented. A combination of different simulation tools are then used to optimise the design and the possibility of achieving fabrication tolerance is assessed. The device performance is analysed with reference to state-of-the-art work in order to compare the performance in both cases.

Finally, Chapter Six presents the conclusion of this work. It explores the relative merits of each of the circuits and compares them in the context of the desired system level functionality. Topics of interest to further enhance the development of PICs in general are discussed and a final outlook is provided at the end.

Chapter 2

Fifth-order Resonator based Broadband 8×4 Switch Matrix

In this chapter, a switch circuit consisting of fifth-order ring resonator elements on SOI is presented as a route to achieve low loss, high connectivity and broadband switches. The work is placed in context of existent circuits in Section 2.1 and then the components and layout of the circuit are described in Section 2.2. The switch mechanism is actuated by use of thermo-optic heaters and their performance is scrutinized to determine their effectiveness in Section 2.3. The scalability is analysed in terms of the on-chip losses incurred, and devices are assessed using measured switch spectra in Section 2.4.

2.1 Introduction

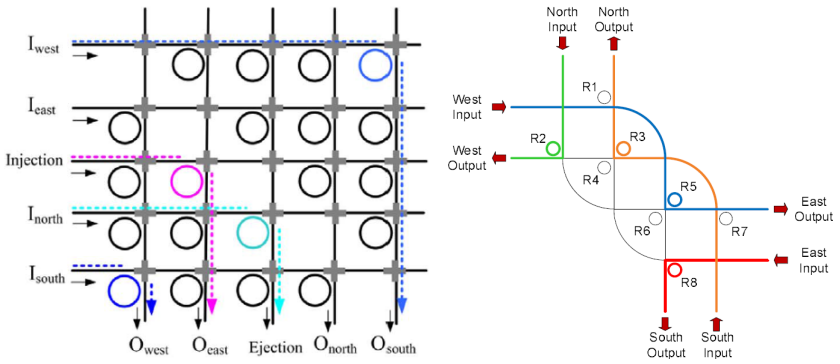
A lot of interest has been focused on ring resonators in the past decade or two, exploring their performance as modulators, filters and add-drop multiplexers [47, 48, 52, 67–86]. Ring resonators offer an interesting route to achieve high scalability switch matrix circuits and for this purpose single-order resonant devices have been in most instances been considered. However, single-order resonators exhibit a trade-off between the achievable pass bandwidth and the signal extinction rendering it impractical for high connectivity switches. Moreover, nanoscale feature size variations arising from fabrication and growth variability manifests themselves in the form of

nanoscale width and thickness variation in waveguides, leading to a equivalent shift in the resonant peak of such devices [48].

Higher-order resonators on the other hand help to decouple the aforementioned dependency and allow for the scope to optimise both the pass bandwidth and the on-off signal extinction individually. Moreover, the enhancement of the bandwidth achieved, leads to an improved fabrication tolerance, paving the way for higher connectivity switches. Using this principle, data routing at 40Gbps across a resonator with a bandwidth of 300GHz and an extinction ratio of 17dB has been recently demonstrated [52].

2.1.1 State of the Art

A comparative tabulation of the existent in-plane, ring resonator based circuits on SOI platform is presented in Table 2.1.1. Single order resonators as well as higher-order resonators have been studied for this purpose. The table has mainly been parametrised in terms of the number of input and output ports, the circuit architecture, the bandwidth along with the extinction ratio and performance while it is prioritised on the basis of the order of the rings and the number of paths tested. An n×m nomenclature has been used to signify the number of optical ports where n stands for the number of input ports and m stands for the number of output ports. Single and multiple elements have been separated in order to distinguish the level of complexity associated with each work. Most of the published work deals with single elements [52, 78, 81–83, 86]. In order to scale up to multiple input and output circuits, others use either a crossbar architecture [73, 75, 77, 80, 85] or a serpentine architecture [67, 76, 79]. As shown in Fig. 2.1a, a crossbar architecture consists of orthogonal waveguide crossing leading to a matrix circuit formation. A serpentine architecture, as demonstrated in Fig. 2.1b, places resonant components at suitable locations to minimise the number of components. This is achieved by using bend waveguides. A drawback is that data from the n^{th} input cannot be switched to the n^{th} output. Full connectivity between inputs and outputs have yet to be demonstrated but 4×4 [67, 76] and 5×5 [79] circuits are enough to be implemented into Torus type networks. The data routing experiments performed have been limited in terms of the number of paths tested. Higher-order rings [118] have also been explored but for mainly usage as delay lines.



(a) (b)

Figure 2.1: (a) Schematic of a 5×5 resonator based switch matrix demonstrated by A. W. Poon *et al.* in [80]. (b) Schematic of a 4×4 resonator based serpentine switch circuit demonstrated by N. Sherwood-Droz *et al.*. in [67].

Table 2.1: State-of-the-Art Circuits

Order	Ports	Circuit	Paths Tested	B.W. (in GHz)	E.R. (in dB)	Line Rate (in Gbps)	Power Penalty (in dB)	Group
1	4x4	Serpentine	2	39	20	c.w.	-	N. Sherwood-Droz *et al.*, 2008 [67]
1	4x4	Serpentine	3	39	8	3x10	1.3	A. Biberman *et al.*, 2010 [76]
1	2x2	One element	2	13	8	6x10	1.2	B.G. Lee *et al.*, 2009 [78]

Continued on next page

Table 2.1 – continued...

Order	Ports	Circuit	Paths Tested	B.W. (in GHz)	E.R. (in dB)	Line Rate (in Gbps)	Power Penalty (in dB)	Group
1	5x5	Serpentine	8	38	16	12.5	-1.7	R. Ji *et al.*, 2008 [79]
1	1x2	One element	1	13	14	10	2.2	A. Melloni *et al.*, 2004 [81]
2	1x2	One element	1	7 [a]	14.5	10	1.3	A. Melloni *et al.*, 2004 [81]
3	1x2	One element	1	88 [a]	8	c.w.	-	T. Barwicz *et al.*, 2004 [83]
3	1x3	Series coupled	3	40	30	c.w	-	M.A. Popovic *et al.*, 2006 [84]
5	1x2	One element	1	300	17	40	0.3	Y. Vlasov *et al.*, 2008 [52]
6	1x2	One element	1	102	50	c.w.	-	A. Canciamilla *et al.*, 2010 [86]

B.W.: Bandwidth ER: Extinction Ratio CW: Continuous Wave

Comparing different state of the art circuits presented in Table 2.1.1, it can be seen that the single-order rings are optimised to maximise either the

bandwidth or the extinction ratio but not both, leading to compromised performance. The coupling of the bandwidth and the extinction ratio in such devices leads to a Gaussian passband with a narrow width which limits their application. Furthermore, in circuits involving multiple such switch elements, bandwidth narrowing effects are prominent as a consequence of the feed-through approach which hinders the scalability of such circuits. A 100GHz bandwidth has been demonstrated by B.E. Little *et al.*, but no switching was actuated hence the on-off state signal extinction cannot be estimated [75]. The sixth-order microring with 102GHz bandwidth and 60dB signal extinction demonstrated by A. Canciamilla *et al.*, [86] by far denotes the best performance achieved in a single element but each of the six arms of a single element have been optimised individually to achieve this performance and no switch actuation has been demonstrated. In other recent examples, the bandwidth has been comparable, but the extinction ratio has been lower. In the case of the optically switched fifth order element [52], only one part of the switch element is tuned. Tuning all of the resonant elements together may be expected to lead to considerably higher extinction ratios [48, 72]. The broad box-like Lorentzian passband thus achieved in higher-order resonators is expected to increase the tolerance to fabrication variation which makes them an alluring prospect for large scale switch matrices [48].

2.2 Design

The design aspect of the switch matrix is discussed in this chapter. The individual switch elements are described in Section 2.2.1. An overview of the optical circuitry is provided in Section 2.2.2. The thermo-optically activated switch mechanism in each switch element and the electrical wiring of the whole circuit are described in Section 2.2.3 and Section 2.2.4 respectively.

2.2.1 Photonics layout

A SOI wafer is used to fabricate the photonic layout by the ePIXfab foundry. The platform was chosen as the very high fabrication tolerances afforded by CMOS technology and the possibility of creating high confinement SOI waveguides with modest loss in combination with the relaxed tolerance afforded in higher-order resonators, are expected to give rise to a resilient

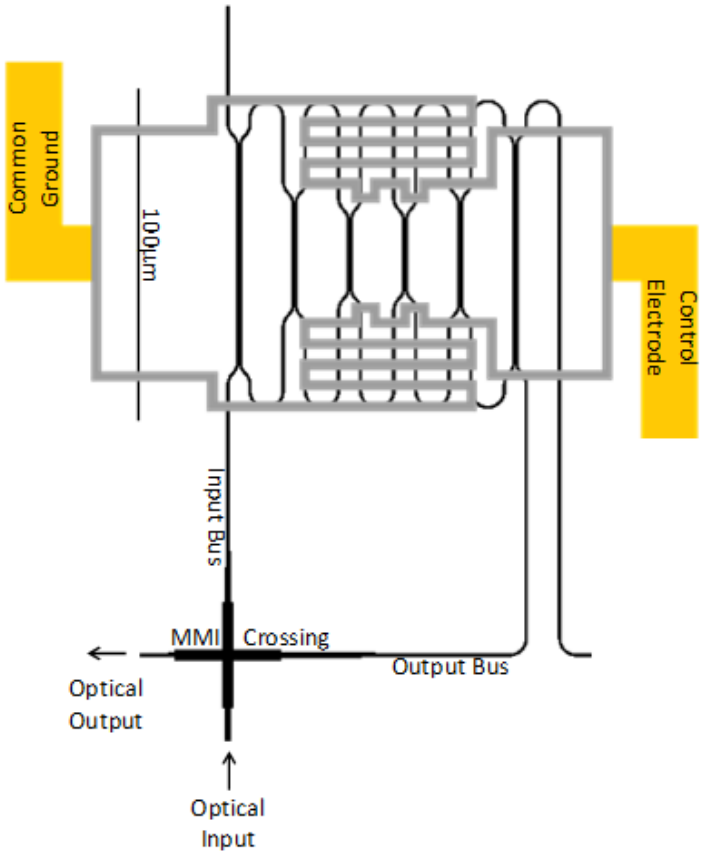


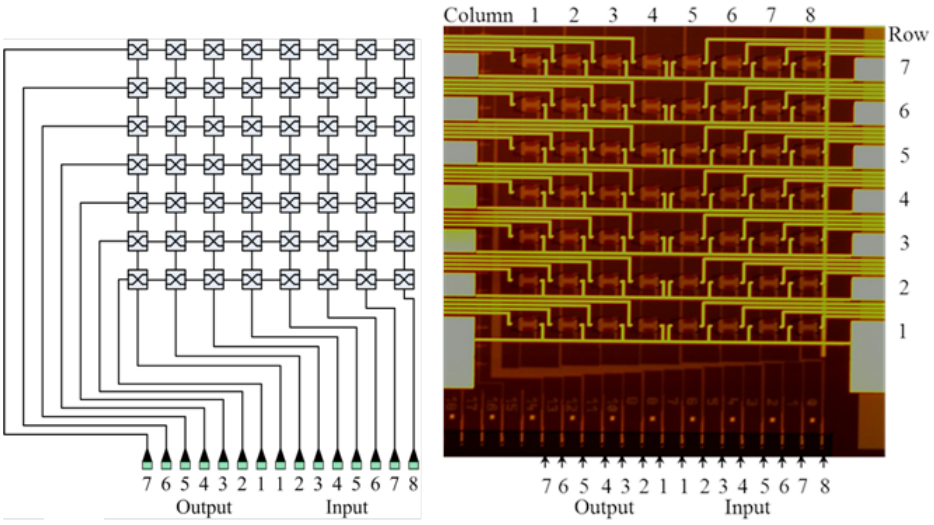
Figure 2.2: Mask details for one switch element. The optical waveguides are shown in black. The narrow Ti/Pt micro-heater features are shown in grey, and the wider gold on-chip wiring is shown in orange.

and scalable switch matrix design. $220\times500\mu m^2$ Si layer forms the optical waveguides and is covered by 1.2μm and 2.0μm top and bottom silica cladding respectively. Each switch element is a fifth-order resonator in which each arm comprises of a racetrack with 5μm bend radii. Fig. 2.2 shows the mask layer of a single switch element in which the layer in black depicts the optical part. Each arm is evanescently coupled to the next arm by using directional couplers which are at a constant spacing of 280nm from each other and this waveguide separation is specified by the foundry and is defined by the tools used in fabrication. The constant spacing is maintained in order to ensure a consistent feature reproduction across the fabricated

chip and the coupling coefficient is optimised individually by varying the length of the directional couplers. Directional couplers of length 72.1μm, 29μm and 21.2μm from outside to inwards, are used in order to achieve the desired coupling coefficients. The coupling coefficient is maximised as discussed in Table 2.2 in order to allow for greater fabrication tolerance in accordance with prior simulations [48]. The coupling length is computed for each desired coupling coefficient using optical propagation simulation tool, FimmPROP [119]. A long circumference is needed to ensure that the desired minimum π phase shift is achieved. The designed length of the rings provides a good compromise between the phase shift achieved and the device circumference enabling the switch to be compact enough so that a designed FSR of 350GHz for each switch element is attained. The input and output waveguides are densely packed using optical buses as shown in Fig. 2.3. Orthogonal waveguides run across the chip with a pitch of 300μm in the vertical direction and 250μm in the horizontal direction. Each switch element is located at the intersection of the buses to give rise to the matrix. $32\times3\mu m^2$ MMIs are used as waveguide crossing for the buses in the matrix. Each device ends up with a footprint of $110\times115\mu m^2$.

2.2.2 Circuit Concept

Fig. 2.3a depicts the scheme of the switch matrix circuit and Fig. 2.3b is a microscope image of the fabricated circuit. Orthogonal intersection of eight rows and seven columns make up the 8×7 switch matrix. Several switch matrices were fabricated on the same tile and based on the dimensions of the tile, the size of the switch matrix was fixed. A combination of eight inputs to four outputs leading to a 8×4 switch circuit was characterised during the measurements. Bus waveguides depicted in the schematic in Fig. 2.3a appear below the metallised sections as blurred and hazy lines running across the tile in Fig. 2.3b as they are out of the depth of focus that was set on the microscope. Optical connections are established by using 1D tapers and 1D surface grating couplers located at the edge of the chip as shown in Fig. 2.3. The surface grating couplers are polarisation selective and are optimised for TE polarisation. The gold metal tracks and bond pads are visible as yellow lines across the chip.



(a) (b)

Figure 2.3: (a)Schematic layout for the 8×7 matrix switch. (b) Photograph of the full switch matrix with seven rows of eight resonant switches in a crossbar configuration. The inputs and outputs are made via the surface grating couplers at the bottom of the image.

2.2.3 Micro-heater

Two parallel micro-heaters are used as switch actuators for each circuit element. The 1.2μm silica cladding on top of each resonant switch is used to separate the waveguide from the deposited metal. A multi-step metallisation process is used to deposit 100nm Ti, 20nm Pt and 300nm Au layers and is patterned to give rise to the 18.5μm metal tracks, the bond pads and the 3μm micro-heaters. The Au is selectively etched away from the 3μm wide heaters to increase the resistance of each micro-heater element to 400Ω. The metallised micro-heaters with the Au etched away is visible as orange lines in Fig.2.4 whereas the metal tracks with the Au on top are visible as thicker gold lines. Finally polyimide is deposited all over the circuit, in particular the micro-heaters so as to prevent them from degrading. However, the Au bond pads and the surface grating couplers are left open in order to facilitate external electrical and optical access to the circuit. Local heating induced by the micro-heaters is then used to tune or de-tune each switch element with respect to a particular wavelength and hence form the switch mechanism.

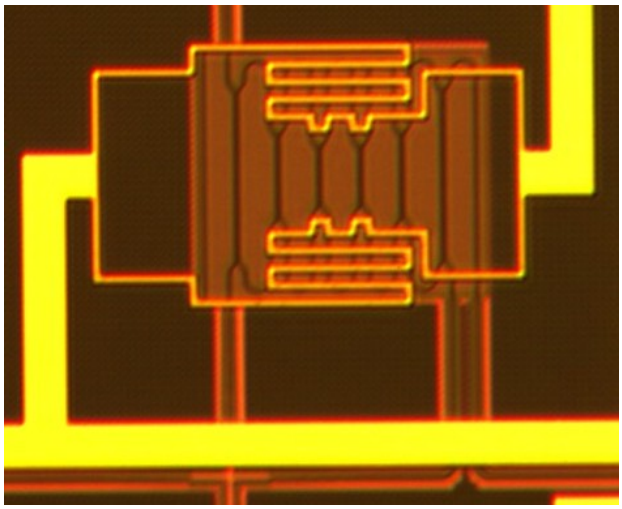


Figure 2.4: Photograph of a single fifth-order switch element.

2.2.4 Electrical Addressing

Figure 2.5: Photograph of assembled circuit. Wire bonds leading to the left and right of the image are control lines. Wire bonds leading to the bottom edge are the common ground lines.

Each switch element has two electrodes one is for the control line signal and the other is a common ground. The two parallel micro-heaters used per element help in reducing the density of bond pads used as well as aid in

reducing the switch actuation voltage by half. For the entire 8×4 under test, a total of 32 control electrodes are in use. A common ground is present for each row and the common ground pads for each row are bonded together as they are vertically lead off and connected to the heatsink as seen in Fig. 2.5. The control lines run horizontally across the chip and terminate at the bond pads which are located at the right and left extremities of the chip. The bond pads are wire bonded onto a PCB enabling external electrical connections to the chip to be made as seen in Fig. 2.5. The chip itself is epoxy bonded onto a water cooled mount which is maintained at a constant temperature of 22℃.

2.3 Switch Element Actuation

The switch element lying at the intersection of input 1 to output 1 does not utilise the off-state of any other element and hence it represents the most unambiguous transfer function attainable in the circuit. Therefore, the tuning data of this particular element is used for initial study and evaluation of the switch. An already established transfer matrix model [48] is used to calculate the transfer function as well as the thermal tuning. Section 2.3.1 outlines the parameters used, and the methodology for curve fitting. Section 2.3.3 shows comparative measured and calculated data for the tuning response of the switch element. Section 2.3.4 analyses the measured data in order to predict the temperature rise in the circuit.

2.3.1 Transfer Matrix Model

The frequency domain model is implemented by discretising in the periodic z-domain. The transfer function is described as product of the optical field transfer functions for individual resonators [48, 120].

$$\begin{bmatrix} T_N \\ R_N \end{bmatrix} = \prod_{n=0}^{N} j(S_n^2 \gamma_n z^{-1})^{-\frac{1}{2}} \begin{bmatrix} 1 & -c_n \\ c_n \gamma_n Z^{-1} & -\gamma_n z^{-1} \end{bmatrix} \cdot \begin{bmatrix} T_0 \\ R_0 \end{bmatrix} \tag{2.1}$$

$$c_n = \sqrt{1 - \kappa_n} \tag{2.2}$$

$$s_n = \sqrt{\kappa_n} \tag{2.3}$$

$$\gamma = \exp^{(\alpha L + j\delta\theta_n)} \tag{2.4}$$

The analysis is used to describe a higher-order resonant element in terms of a complex propagation coefficient γ_n and field coupling coefficients c_n and s_n. The field coupling coefficients are defined directly by the power coupling coefficient κ_n. The optical transfer function from the input to the ring coupled drop port output may be performed for the transmission of a normalised broadband signal from input T_0 to the output of the fifth ring at T_5. The five arms of the ring are assumed to have equal length L but different coupling and propagation coefficients. The coupling coefficients are estimated through reverse engineering, by curve fitting to the measured inherent transfer function with no switch actuation, implying no electrical heating with a simulation of the said device based on a Transfer Matrix Model. The dimensions for the ring resonator are taken from the designed mask layout, and parameters used in the calculations are summarised in Table 2.2.

Table 2.2: Parameters used for Transfer Matrix Calculations

Symbol	Quantity	Value
λ	Optical wavelength	1550nm
FSR	Free spectral range	2.84nm
κ_n	Coupling coefficient	{ 0.90, 0.60, 0.35 } [a]
L	Ring circumference	200μm
α_{fibre}	Total fibre to chip coupling loss [b]	12dB
α_{chip}	On-state chip component loss [c]	2dB
α	Optical waveguide loss	2.6dBcm^{-1}

[a] Coupling coefficients are symmetric about the third ring and computed in Section 2.3.2

[b] Including tapers and grating couplers

[c] Component losses as measured in Section 2.4.3

2.3.2 Coupling coefficients

A single transfer spectrum of the fifth-order resonant switch traversed from input 1 to output 1 is measured under unbiased condition, normalised and plotted in Fig. 2.6. A theoretical fit is applied to the measured spectra based on the Transfer Matrix Model described in Section 2.3.1, where the coupling coefficients are used as the fitting parameter while assuming zero

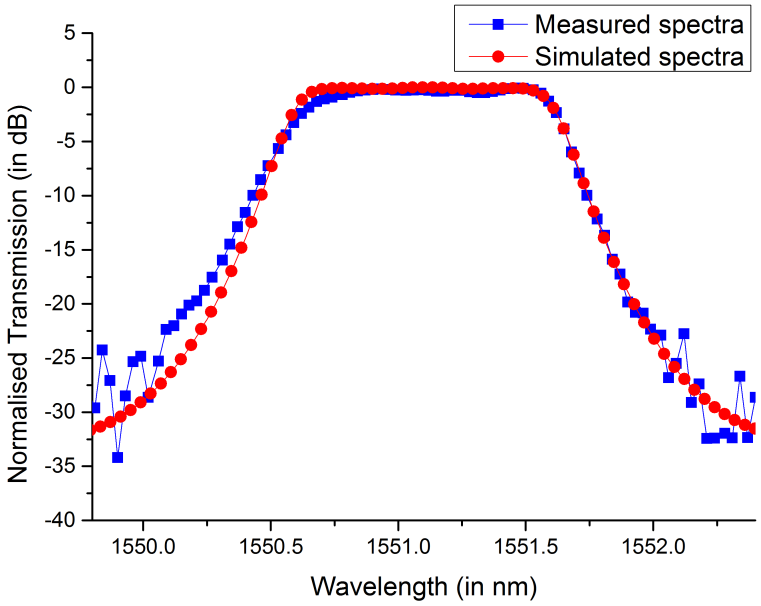


Figure 2.6: Transmission through a single fifth-order resonant switch. Measured spectra has been used to compute the achieved coupling coefficients by fitting to a simulation

waveguide losses. A best fit is observed for coupling coefficients of 0.90, 0.60 and 0.35. It should be remembered at this instance that two consecutive waveguides forming the directional couplers are separated by a layer of silica as opposed to being separated by an air gap and this factor was not taken into account in the initial design. Removal of the silica layer will lead to lower coupling coefficients, leading to another design parameter which might be utilised in future designs.

2.3.3 Thermo-optic Tuning

The thermo-optic tuning mechanism for switch actuation is studied by scanning the voltage applied to the higher-order switch element located at the intersection of input 1 and output 1 and by recording the transfer function at each instance. The voltage is scanned within a range of 0.0V to 8.0V with steps of 100mV. Fig. 2.7 is a colour map, representing the measured 81 spectra covering a span of 10nm i.e. spanning across more than three free spectral ranges of the switch element and it emphasises the shift of the passband peak wavelength with applied power. The vertical axis repre-

Table 2.3: Parameters used for Temperature Estimations

Symbol	Quantity	Value
P	Input heater power for π-shift	120mW
k	Thermal conductivity of Silica	$0.014 \mathrm{W} cm^{-1} K^{-1}$
	Thermal conductivity of Silicon	$1.4 \mathrm{W} cm^{-1} K^{-1}$
A_{heater}	Micro-heater metallisation area	$2{\times}10^{-5}\mathrm{cm}^2$
A_{switch}	Optical switch element area	$1.15{\times}10^{-5}\mathrm{cm}^2$
S_1	Silica upper cladding thickness	1.2μm
S_2	Silicon waveguide core thickness	0.22μm
S_3	Silica lower cladding thickness	2.0μm
S_4	Silicon substrate thickness	725μm

sents the input electrical power which is scanned and a constant resistance of 400Ω is assumed throughout the range of voltages that are scanned. The tuning is found to be non-linear with voltage applied and linear with the power. A tuning efficiency of 11.8pm/mW is obtained with an increase in applied voltage from 0.0V to 6.9V (120mW) leading to a π phase-shift in the fifth-order resonator spectra. The orange passband with fibre-to-chip-to-fibre loss in the order of 17dB signifies the minimum loss section. The passband is seen to be uniform at low voltages but ripples start to appear at the higher applied voltages. Furthermore, as voltage increases, passband narrowing can be observed as well as the introduction of an asymmetry in the transfer function. The asymmetry is evident as a light blue-green shoulder around -30dB to the shorter wavelength side of the stop-band. The stop-bands are depicted in blue with losses in the range of -40dB to -50dB. Some speckled features are observed in the low power blue sections of the measurements and they originate from the measurement noise floor.

Calculations are performed using the transfer matrix model to establish the cause of the bandwidth narrowing and transfer function asymmetry under higher bias conditions. An excess loss of 14dB is included in this process to match the experimental data with the calculated one and this 14dB value is consistent with the expected losses in circuit, a fact which is also confirmed by the measurements, as shown in Section 2.4.3. The phase tuning is carried out independently for each arm of a single fifth-order switch element and a linear approximation is used in order to correlate

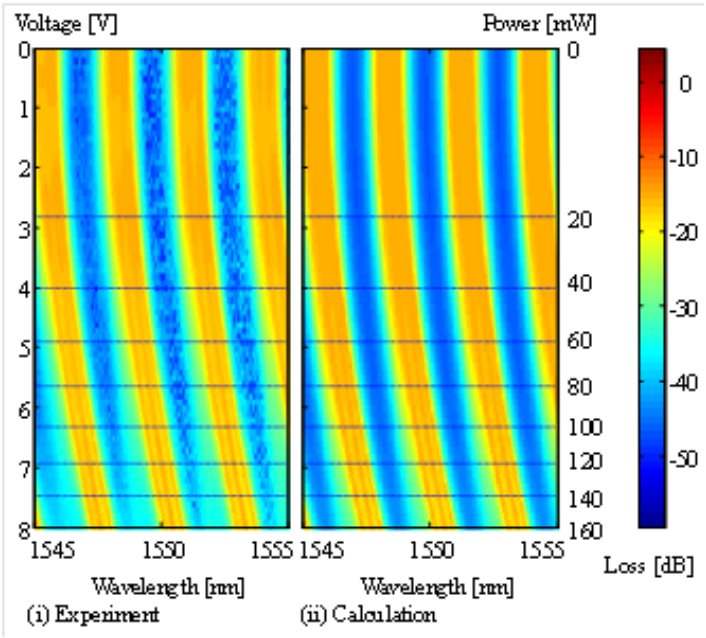


Figure 2.7: Thermal tuning of the switch element connecting input 1 to output 1. Experimentally measured optical transfer functions (left) and calculated transfer functions using the transfer matrix model (right).

the phase shift to the power applied to the heater. The simulated results and the experimental measurements seem to be in good agreement leading to new insight into the transfer function and the cause of the bandwidth narrowing and the asymmetry in spectra at higher biases. An efficiency of 7.4pm/mW and 13.3pm/mW is thus computed for the outer two and inner three arms of the switch element respectively. The small deviation from the ideal box-like transfer function, evident in the light blue-green shorter wavelength shoulders can be avoided with equal tuning efficiencies for each of the five rings. This indicates that the passband distortion is a result of high biases applied to the unoptimised heaters implemented and thus, it is not an artefact of the optical circuitry and can be rectified by modifying the design of the micro-heaters such that the outer arms have a greater overlap with the heater than the inner arms.

2.3.4 Thermal Analysis

The performance of the micro-heater is benchmarked against the idealised case of a one-dimensional heat flux, f_n. Power, P flows through area f_n and leads to a temperature drop $T_n - T_{n+1}$ at layer, n:

$$f_n = \frac{P}{A_n} = k_n \frac{T_n - T_{n+1}}{S_n} \tag{2.5}$$

The area is defined as the micro-heater metallisation area for layer 1, and as the optical switch footprint area elsewhere. Equation 2.5 is generalised to multiple layers with a bidiagonal thermal transfer matrix, H such that f=HT. Interface temperatures, T are then calculated using the parameters in Table 2.3, and they predict a rise in temperature of 122K and 69K at the micro-heater and waveguide core respectively. Notably, the temperature drop is almost halved at the waveguide core for the 1D heatflow model and this is directly attributable to the two orders of magnitude difference in the thermal conductance for the upper Silica cladding layer relative to the Silicon waveguide core. Ambient temperature tuning measurements [73], done by varying the temperature at the substrate via the water cooler system used, show an even lower 20K temperature rise for a π phase shift. The discrepancy with the ideal 1D heatflow model is attributable to the geometry of the micro-heaters [121]. Significant efficiency enhancements are therefore anticipated by placing the micro-heaters directly on the higher thermal-conductivity Silicon as demonstrated by subsequent work in [121–123].

2.4 8×4 Matrix

The transfer function of each switch element is studied and qualified in terms of its on-state and off-state spectra. The phase errors within the arms of a single switch element appear to be nominal such that the transfer function of each ring can be tuned using a single control electrode. However, phase errors between different switch elements imply that by applying a bias, the switch elements need to be spectrally aligned to each other. As a prologue to a systematic analysis of the crosspoint matrix paths, each resonant switch element is tuned to determine the voltages required to align the pass-band (on-state) and stop-band (off-state) to a common signal wavelength in Section 2.4.1. Once these values are identified, the matrix is analysed for each path in turn with one on-state switch and the remaining

switches for the path in the off-state. Representative transfer functions are presented for the on-state and off-state switch conditions in Section 2.4.2. A comprehensive comparison of path dependent loss, operational bandwidth and switch extinction is subsequently presented for all paths in Section 2.4.3 and Section 2.4.4. Thermo-optic tuning of switch elements imply the risk of undesirable thermal leakage and hence crosstalk between neighbouring elements and this aspect has been investigated in Section 2.4.5.

2.4.1 Switch State Calibration

An operation wavelength of 1551.35nm is fixed and the on-state and off-state bias for each switch element is determined. The on-state bias implies the condition at which the element pass bandwidth is centred around the wavelength of operation. The on-state bandwidth is achieved keeping this in consideration and tuning the ring transfer function so as to obtain a bandwidth of 100GHz. The off-state is achieved by tuning to the condition where the highest extinction is obtained across the entire 100GHz pass bandwidth. In order to carry out these calibrations, an Erbium-doped Fibre Amplifier (EDFA) is used as a broadband noise source and the spectra at the output is monitored using an Optical Spectrum Analyser (OSA). Two markers situated at either side of the operation wavelength and centred around it help to depict the required pass-band during optimisations.

The on-state and off-state biases as a function of each switch element are plotted in Fig. 2.8. Four of the paths i.e. from input 8 to output 3 and from inputs 6, 7 and 8 to output 4 are untested due to open-circuits. Although a sizeable spread is seen across the entire range of biases applied, some similarities might be seen for those used in neighbouring elements. The standard deviation of the bias for each measured on and off state is 1.3V and 0.7V respectively. Previous work on the shift in resonant wavelength associated with fabrication induced errors in feature dimensions confirm this fact [73, 124].

In order to make or break a connection, the element in use has to be tuned on while the other elements acting as optical vias and leading up to the element in question, are tuned to their off-states. A low thermal cross-talk is exhibited by the fact that the voltage combination used for the on and off states is fixed separately for each element and is in most cases independent of the path used - a further exploration of the thermal crosstalk in the switch matrix has been presented in Section 2.4.5. In case of a limited number of paths, a change in the off-state bias limited to 1.5V

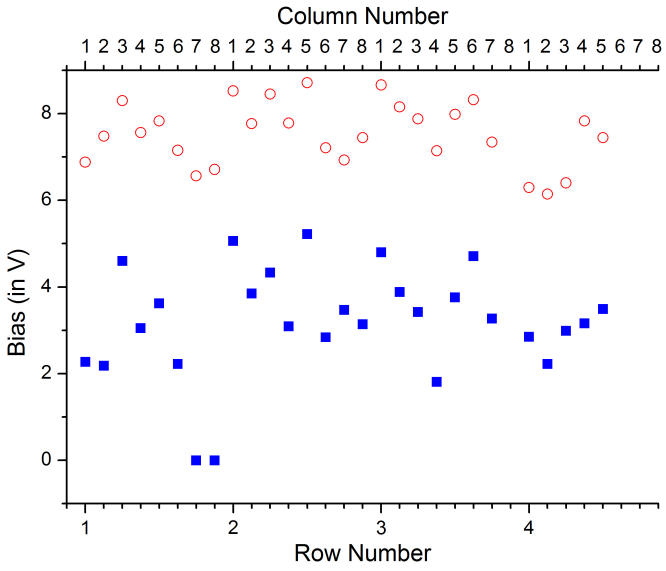


Figure 2.8: On state (■) and off-state (○) voltages for an input signal centred at a wavelength of 1551.35 nm for each switch element.

is applied to further improve the transfer function.

2.4.2 Transfer Function

The input of the chip is fed by an EDFA which is used as a broadband noise source and the output is recorded using and OSA with a resolution of 0.1nm. The recorded spectra is then normalised with respect to the EDFA noise spectra to obtain the transfer function. However, these transfer functions do not take into account the 6dB loss while coupling using a surface grating coupler as specified by the ePIXfab foundry [124, 125] and hence, a total of 12dB fibre-to-chip-to-fibre coupling loss is also present in these measurements. Fig. 2.9 shows the transfer functions obtained for a combination of multiple representative paths along input 1 to output 1 and three of the longest paths of the circuit along input 8 to output 1 and output 2 as well as input 5 to output 4. In Fig. 2.9, a 100GHz bandwidth has been demarcated to signify the passband and a minimum extinction of 19dB is achieved across its entirety. The spectra are in most cases flat but a certain degree of reduction of the flatness for some longer paths is observed and this is attributed to phase errors leading to spectral misalignment observed

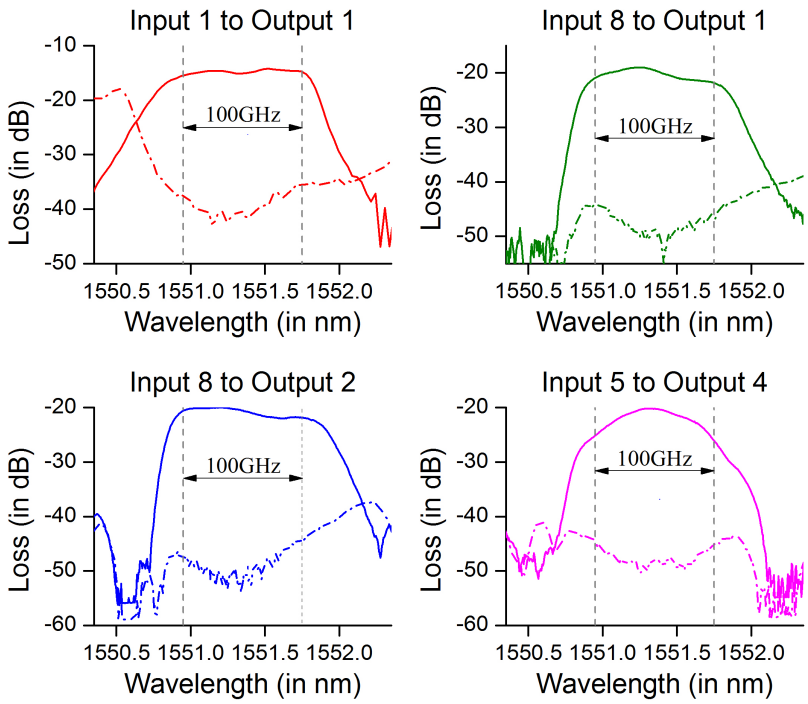


Figure 2.9: On-state loss (solid) and off-state loss (dashed). The vertical dashed lines show a bandwidth of 100GHz. A range of representative paths are presented: Shortest path from input 1 to output 1 (Red), Long path from input 8 to output 1 (Green), One of the longest measured paths from input 8 to output 2 (Blue) and Worst case passband from input 5 to output 4 (Magenta) are shown.

within different switch elements within the circuit. This spectral mismatch is cumulative and hence it is most visible in some of the longer paths, the most notable of them being in the case of the path from input 5 to output 4. A slope is also observed within the passbands for some paths, and there is some asymmetry. The slope within the passband is below 3dB for 27 of the measured paths. Only in the case from input 5 to output 4, the slope is extended to 6dB which reduces its 3dB bandwidth to 75GHz. However, no specific correlation with path length is observed.

2.4.3 Optical Path Loss

The on-chip losses incurred for each path are studied by measuring the fibre-to-fibre losses at 1551.35nm for each measured path and then plotting

them as a function of off-state ring traversed i.e. path length as shown in Fig. 2.10.

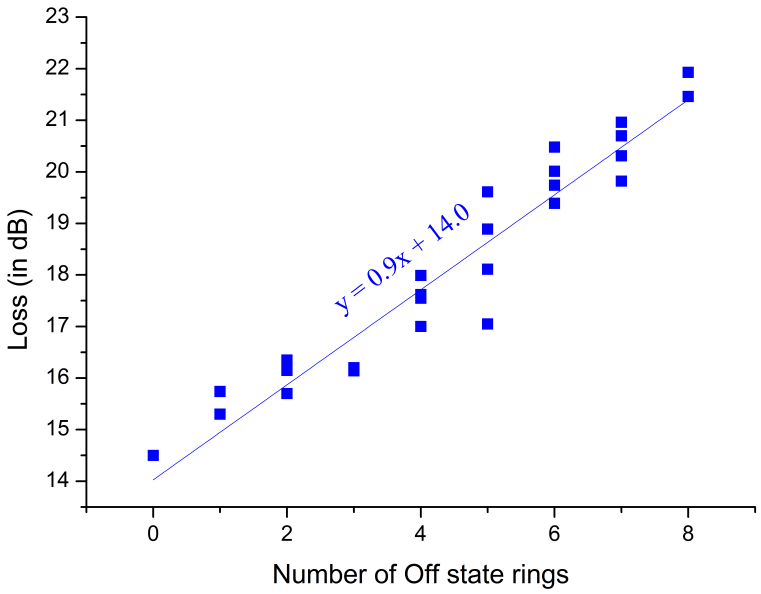


Figure 2.10: Fibre coupled losses for paths through the optical switch matrix.

The lowest losses are observed for the path from input 1 to output 1 as that path represents the fewest number of traversed rings one on-state ring and zero off-state rings. In case of the two longest measured paths i.e. from input 8 to output 2 and from input 7 to output 3, the number of rings traversed increases to 1 on state ring and 8 off state rings. This variation in the number of off-state switch elements allows the loss data to be used to separate common losses such as on-state switch loss and fibre chip coupling losses, from path dependent losses which include the number of crossings and off-state resonator. The plotted losses also include waveguide propagation loss of 2.6dB/cm and the loss at each MMI crossing which is estimated in the order of 0.1dB [73]. An error margin of up to 1dB is expected as the paths are scanned manually using two single fibres and moving them across and aligning them manually to a combination of inputs and outputs. Least means square method is used to form a linear fit to the data points and they reveal that a loss of 0.9dB is incurred per off-state element traversed. Fibre to chip losses of 26.0dB [124, 125] is also

included as a part of the losses and so, the 14.0dB loss at the intersect implies an on state ring loss of 2.0dB.

2.4.4 Extinction Ratio

In order to achieve high scalability in switches, a high on-off signal extinction is required. Leaking off-state paths and scattering from any waveguide crossings lead to a path dependent crosstalk which is critical for desirable switch performance. The crosstalk arising solely due to the switch cannot be isolated independently and hence the signal extinction across the entire pass bandwidth is measured. A variation in on-off signal extinction is observed across the entire pass bandwidth of different switch elements. In order to quantify this, the difference in signal extinction is quantified across the entire 100GHz bandwidth while the transfer function is centred at the wavelength of operation and presented in Table 2.4 as the minimum achievable extinction per path across the entire pass bandwidth. The minimum and maximum values for the lowest achievable signal extinction is 19.5dB and 23.4dB respectively.

Table 2.4: Extinction Ratio across 100GHz Bandwidth

Input port	Output port (in dB)			
	1	2	3	4
1	-20.7	-20.9	-22.0	-21.4
2	-21.3	-20.7	-21.4	-21.7
3	-21.5	-21.3	-21.3	-20.2
4	-22.8	-22.7	-19.5	-23.0
5	-20.8	-21.1	-22.7	-19.5
6	-22.0	-22.5	-19.7	n.c.
7	-23.4	-20.3	-23.2	n.c.
8	-23.4	-22.3	n.c.	n.c.

n.c.: not connected

2.4.5 Thermal Crosstalk

The adjacent element thermal crosstalk is studied for one of the most central of the switch elements between input 2 and output 2 in Fig. 2.3 tuned to operate at 1543nm. The optical transfer functions are then measured

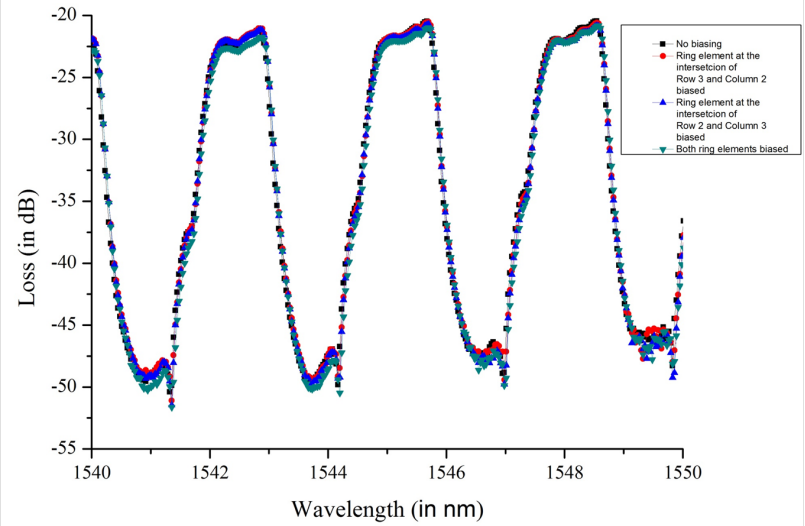


Figure 2.11: Transfer function for the (2×2) switching element with unbiased (black solid line) and biased (red, blue and green) adjacent elements. Loss is quoted comparing powers in fibre.

for the case where adjacent elements are actuated. The element to the top (connecting input 2 to output 3) and the element to the right (connecting input 3 to output 2) are actuated together, independently, and then switched off. The switch element under test is biased in the on-state with a 5V bias voltage. The transfer functions are overlaid in Fig. 2.11. Negligible differences are observed for (i) no adjacent element actuation, (ii) only the adjacent element in the top row (2×3), (iii) only the adjacent element in the right side column (3×2), and (iv) both adjacent elements (2×3) and (3×2) leading to the conclusion that the thermal cross-talk between the adjacent heaters is small.

2.5 Conclusions

Fifth order resonator-based optical elements are used as switches in a fabricated 8×7 switch matrix. Analysis of fabricated switch matrix is restricted to a 8×4 segment in which all the paths are tested barring four paths which are found to be electrically disconnected due to open circuits. Phase matching within the arms of a single resonant switch is good enough to achieve a flat passband without individually tuning each arm within a single ele-

ment. However, phase errors between different resonant switch elements under unbiased condition do exist which needs to be compensated for by tuning the spectra. Each switch is actuated and phase matched with respect to each other by thermo-optic micro-heaters and on comparing with theoretical data, an heater efficiency of 11.8pm/mW is expected. Silica, acting as an insulator, negates the possibility of any thermal crosstalk in the switch matrix but it is achieved at the cost of switch actuation efficiency. Further improvements in heater design can be envisaged following the concepts demonstrated in [121–123]. A signal extinction of 20dB across a 100GHz bandwidth has also been demonstrated for 25 of the 28 measured paths making it the largest resonant switch circuit demonstrated to date. Losses of 0.9dB per off state ring and 2.0dB per on state ring are observed in the fabricated switch matrix which is promising from the aspect of circuit scalability. Initial analysis of the individual switch elements and the matrix as a whole seem to be promising enough to prompt further experiments involving data routing under different conditions in the switch matrix as discussed in Chapter 3.

Chapter 3

Multi-path Switch Performance

In this chapter, the switch elements as described in Chapter 2 are used to form a 8×4 switch matrix and the performance of the switch circuit has been studied. Sub-system level demonstrations have been performed in order to analyse the circuit performance. The first means of gradation is done by passing data at different line-rates through the circuit. A control plane for the switch matrix is developed in order to achieve a high level of electrical connectivity as discussed in Section 3.3.1. The switch performance is then evaluated in terms of the switching time achieved in the circuit and switching from two inputs to one output is used as a precursor to multi-path analysis to justify the need for power equalisation at the output. Simultaneous multi-path, dynamic routing between eight paths is then studied in the fifth-order resonant based 8×4 switch matrix . Device performance is analysed in terms of time-gated Bit Error Rate (BER)s and quantified in terms of the power penalty. A new scheme for generation and routing of mm-wave signal is also used for a set of proof-of-concept experiments.

3.1 State of the Art

High bit-rates have been demonstrated recently using resonators as switched circuit elements with Vlasov *et al.* [52] demonstrating line rates of 40Gbps. A range of power penalties have been observed in each case. A flat top switch spectra has been observed to lead to lower power penalties. However, in case of larger circuits, bandwidth narrowing arising from spectral

misalignments between consecutive switch elements have lead to an increase in power penalty. This has limited the large scale switch applications using resonators with the 8 paths tested by R. Ji *et al.* [79] being the largest.

Dynamic routing has been demonstrated as well with B.G. Lee *et al.* [78] achieving a power penalty of 1.2dB for a line rate of 10Gbps under static condition. A modest degradation of the penalty, up to 3.5dB is observed while routing dynamically from one input to two outputs.

The purpose of this study is to utilise the fabrication resilience obtained as a consequence of the enhanced bandwidth and on-off signal extinction of the fifth-order resonator to achieve switching across multiple paths of the circuits.

3.2 Data Routing

Analysis of the switch matrix done in Chapter 2 seems promising for further studies. This has led to various measurements involving data routing across the said circuit being performed. In this section, only the static routing experiments are discussed. In an effort to test the data integrity along with the scalable limit of the said circuit, the performance for all the possible physical connections in the circuit are experimentally assessed using line rates of 10Gbps in Section 3.2.1 while in Section 3.2.2 proof-of-concept studies for high bit rate data at 40Gbps are presented.

3.2.1 Static Routing

BERs are measured for all the connected paths using the setup shown in Fig. 3.1. A tunable laser tuned to 1551.35nm is used as input to a Mach-Zehnder modulator which is modulated at 10Gbps using a 2^{31}-1 Pseudo-random Bit Sequence (PRBS). The modulated pattern is then passed into the chip and the output from the chip is analysed using an XFP Avalanche Photodiode (APD) receiver and a BER tester. No EDFAs are used in this experiment with discrete bench top power supply units being used to provide the required bias of each switch. For each set of through the chip measurements performed, a relevant back to back measurement is performed by replacing the PIC with a variable optical attenuator (VOA) in which the attenuation has been adjusted in order to match the total on-chip loss.

A plot of the BERs of elements in every even column is shown in Fig. 3.2. A very nominal power penalty is observed for each of them. The power

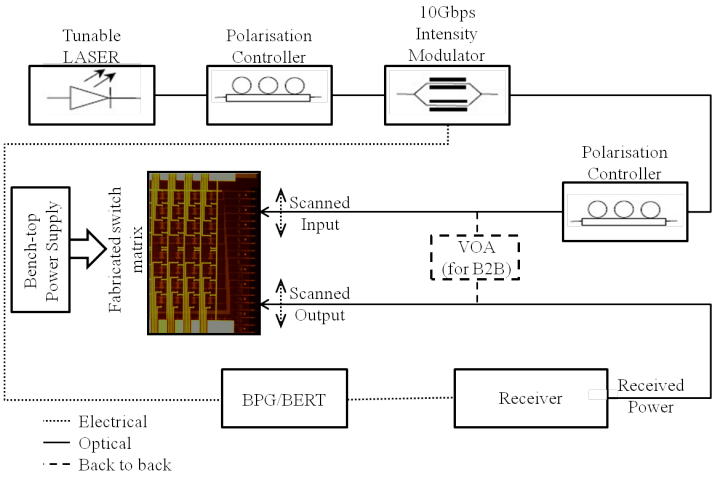


Figure 3.1: Schematic of the experimental setup used for 10Gb/s data routing.

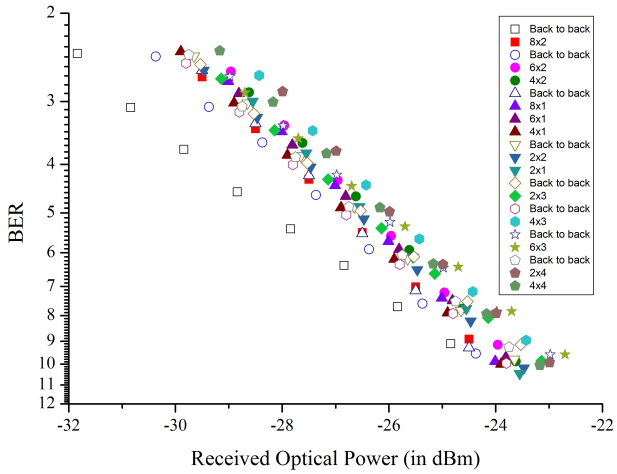


Figure 3.2: Bit error rate as a function of received optical power for the even inputs to all the outputs. A 10Gb/s 2^{31}-1 PRBS sequence is used. The solid and open symbols represent the routed and back to back measurements.

penalty for all electrically connected and measured paths is listed in Table 3.1. No particular path dependence of the power penalty is obvious from this. However, the shape of the passband does play a crucial role in this. The highest power penalty of 1.0dB is presented by the path from

Table 3.1: Power Penalty at 10Gbps

Input port	Output port (in dB)			
	1	2	3	4
1	0.0	0.0	0.1	0.4
2	0.2	0.0	0.0	0.5
3	0.2	0.4	0.4	0.5
4	0.2	0.6	0.8	0.2
5	0.1	0.7	0.6	1.0
6	0.5	0.6	0.3	n.c.
7	0.4	0.5	0.2	n.c.
8	0.3	0.3	n.c.	n.c.

n.c.: not connected

input 5 to output 4, and this is attributed to the fact that in this path, the highest slope in the passband is observed.

3.2.2 High Line Rate Data Routing

Data routing at 40Gb/s is subsequently studied to evaluate the circuit performance at high capacity. A setup similar to the previous one, shown in Fig. 3.3 is used. A laser source tuned at 1543.0 nm is used as an optical source and a 2^{31}-1 PRBS pattern is applied to a subsequent on-off-keyed Mach-Zehnder modulator. The modulated optical pattern is then fed to the chip element under test and the output is connected to a SHF 41210B, pin photodiode detector and onto a BER tester to evaluate the performance. As shown in Fig. 3.3, an EDFA in combination with a 0.9nm Full-width at half-maximum (FWHM) Band-pass Filtre (BPF) is used to amplify the chip output before the pin detector. For the relevant back to back measurements, a VOA is used in place of the chip to account for the on-chip losses which in effect ensures that the same amount of power is going into the amplifier, thus maintaining a constant optical signal-to-noise ratio (OSNR) of 30dB/0.1nm at the receiver side for each set of BER measurement. Received power is specified after the filter, i.e. the power going into the pin detector.

Fig. 3.4 shows the measured BERs which are performed for the first three switch elements on the leading diagonal as shown in Fig. 3.4 inset, chosen as three representative paths of the circuit for this proof-of-concept demonstration. Measurement consistency is ensured by carrying out sep-

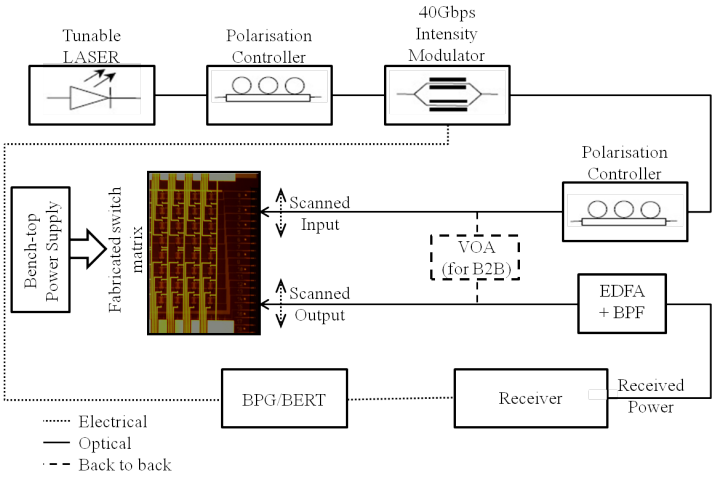


Figure 3.3: Schematic of the experimental setup used for 40Gbps data routing.

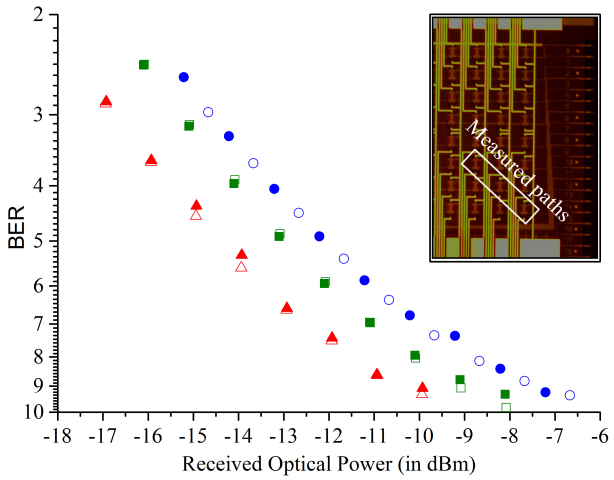


Figure 3.4: Bit-Error Rate curves of the measured paths at 40Gb/s using a 231-1 PRBS sequence. The solid and open symbols represent the routed and back to back measurements for path 1 to 1 (□), 2 to 2 (△) and 3 to 3 (○) respectively. The measured paths have been highlighted in the inset.

arate back to back measurements for each through the chip measurement. Minimal power penalty comparable to the ones obtained at 10Gbps is observed for each path and is limited to a maximum of 0.2dB. The power

penalty observed for 10Gbps and 40Gbps are similar and the slight difference observed is within the range of experimental error associated with it. Moreover, a curved tail depicting a noise floor is seen in all of the measured plots. This curved tail is also present in the back to back measurements confirming that this artefact does not originate from the switch elements but is a part of the measurement setup employed.

3.3 Dynamic Switching

3.3.1 Switch Control Plane

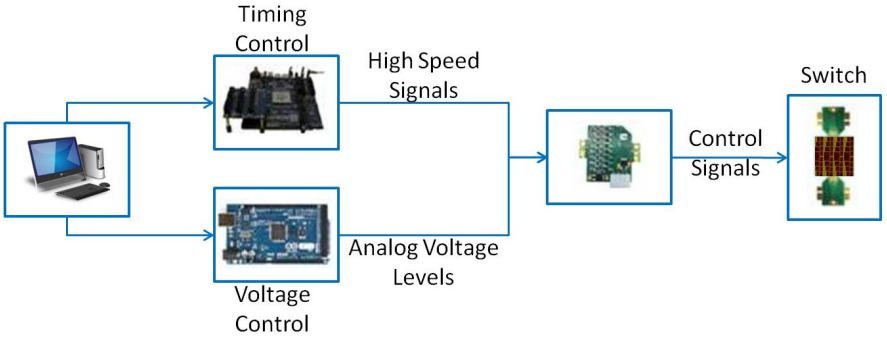


Figure 3.5: The control plane developed and required for the dynamic experimental setup

Fig. 3.5 shows the schematic of the control plane implemented in order to enable multi-path routing across the switch matrix. An Altera Stratix III FPGA is used to implement an automated scheduler marked as the "Timing Control" in the figure. Digital signals from the FPGA are used to set the timing of the switch states for each of the thirty-two, 2×2 elements present in the 8×4 matrix via a voltage driver array. The on-state and off-states are programmed in the voltage driver through the "Voltage Control" by using an ATmega microcontroller in combination with arrays of 8-bit digital to analogue converter arrays. All the components are mounted onto two separate 19" racks - one housing the "Timing Control" and the other dealing with the "Voltage Control". Bench top power supply units provide the required bias for the drivers where as the DAC supplies are drawn from the microcontroller. The scheduler and level controller are configured in a C++ programming environment and are controlled using two separate

excel spreadsheets.

3.3.2 Switching Speed

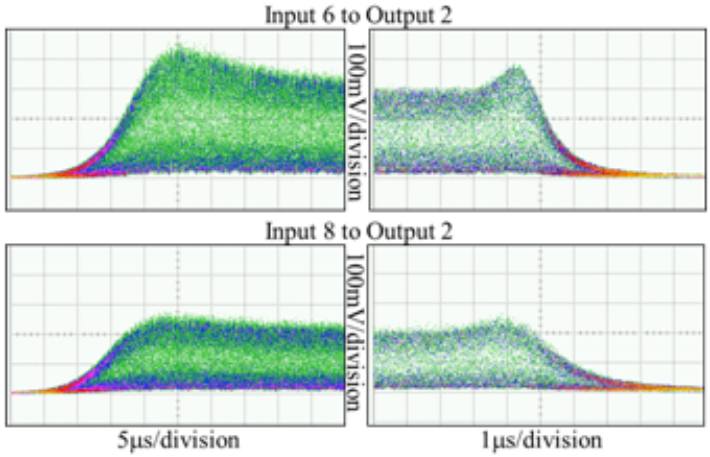


Figure 3.6: Rise and fall transitions for routed 10Gbps data for the switch elements from input 6 to output 2 (top) and input 8 to output 2 (bottom).

Simultaneous, dynamic routing experiments using two input ports and one output port are performed as a precursor to routing using a combination of a higher number of paths. This is done to assess the switching times associated with the switch elements as well as to understand the effect, if any, of the path dependant losses on multi-path routing schemes. The transmitter setup schematic is shown in Fig. 3.8. A three, single fibre system was used to connect to two input optical ports and one output optical port. The modulated pattern was split into two with a fibre coupler and connected to two different inputs of the chip. Both the inputs were switched through the circuit to the same output port which was then visualized using a sampling oscilloscope. The trigger from the pattern generator was used to trigger the pulse generators which actuated the micro-heaters. Only one element is in the on-state at any particular instant of time. Input 8 and input 6 in combination with output 2 were used for the measurements and the relevant rise and fall time are plotted in Fig. 3.6. The rise time is seen to be in the order of 17μs while the fall time is in the order of 4μs.

The length of the entire pattern is 800μs and 35μs long guard bands are

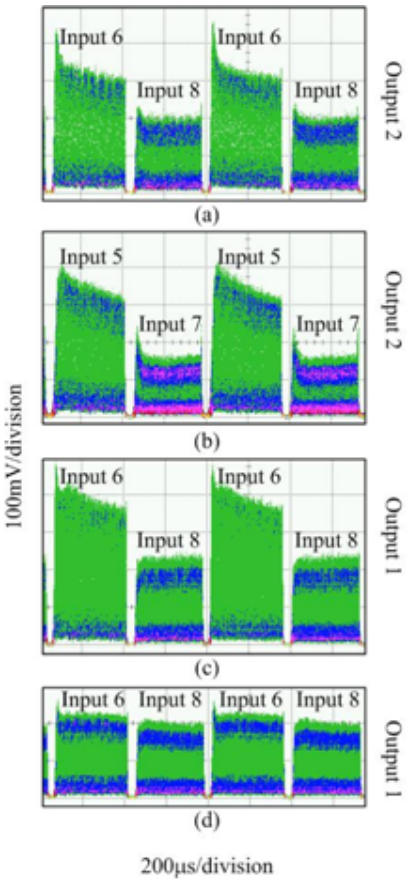


Figure 3.7: Dynamic multipath routing for 10Gb/s data a) Inputs 6 and 8 to output 2 b) Inputs 5 and 7 to output 2 c) Inputs 6 and 8 to output 1 d) Inputs 6 and 8 to output 1 with power equalised

used in between each switch stage. An overshoot in the rise and fall time measurements is observed and it is deemed to originate from the carrier lifetime in the EDFA used. To study this effect better, simultaneous routing from a combination sets of input 6 and 8 and input 5 and 7 to output 2 and output 1 is studied by measuring the time traces. The overshoot is seen to be minimised when signals with equalised power are routed to the output, which confirms the origin of these overshoots as shown in Fig. 3.7. The output sequence for the case without any overshoot involves consecutive routing from path input 6 to output 1 and input 8 to output 1 where

the input signal at port 6 is deliberately attenuated to give levelled output signals. The recorded time-traces indicate a minimised overshoot. In future designs, incorporation of on-chip gain elements at the output of each switched paths can be used to provide the necessary power equalisation. This negates the need for VOA to provide the necessary power equalisation thus reducing the complexity of the experimental setup.

3.3.3 Multiple Input to Multiple Output Switching

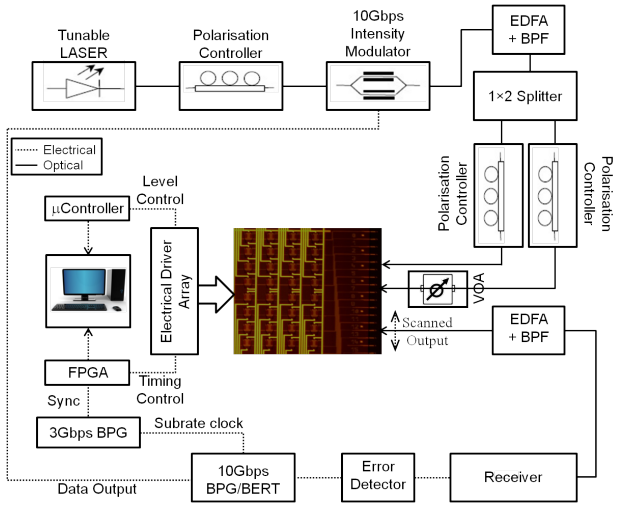


Figure 3.8: The control plane and three fibre setup used for simultaneous multi-path routing.

To demonstrate high-signal-integrity, multi-path routing, the complete switch fabric is implemented using the control plane described in Section 3.3.1. Two optical input connections are made using a common 10Gb/s transmitter, similar to the previously described schematic in Fig. 3.5. The wavelength of operation is 1551.35nm and a 2^{15}-1 pseudo-random binary sequence (PRBS) is used. It is expected that the crosstalk incurred in the switch will be enhanced as the same coherent source with an optical splitter for two different inputs is used. A DC-coupled lightwave converter (HP11982A) is used as a receiver and EDFAs are used at the input and output side of the circuit for amplification. These help to compensate the 12dB loss arising from the surface grating couplers and the poor detector

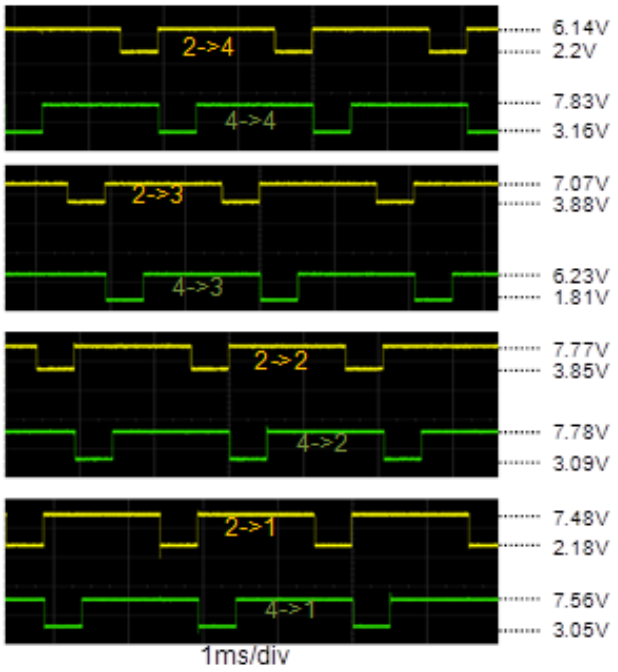


Figure 3.9: Voltage waveforms from the micro-heater drivers. The full span for the timebase is 10ms.

sensitivity of -10dBm. Polarization control is also used on the transmitter side.

Optical signals are connected to inputs 2 and 4. An attenuator is placed before input 2 to compensate the additional on-chip loss of 1.8 dB from two additional off-state 2×2 switch elements and hence to equalise the output power. Losses from the on-state 2×2 switch element are measured to be typically 2.0 dB. This is then required to synchronize the switch fabric controller to the 10Gbps data clock. This is done by means of an intermediate pulse pattern generator. The 10Gbps pattern generator sends a sub-rate clock at a quarter of the clock value which is used to phase lock a 3Gbps intermediate pattern generator. The latter, in turn generates a square waveform used as an external clock input into the FPGA, and also provides the synchronization trigger to the timing control logic.

The measured bias values in Section 2.4.1 are populated in a switch fabric look-up table. The selection of states is programmed by a time schedule to give the periodic voltage waveforms shown in Fig 3.9. Paths

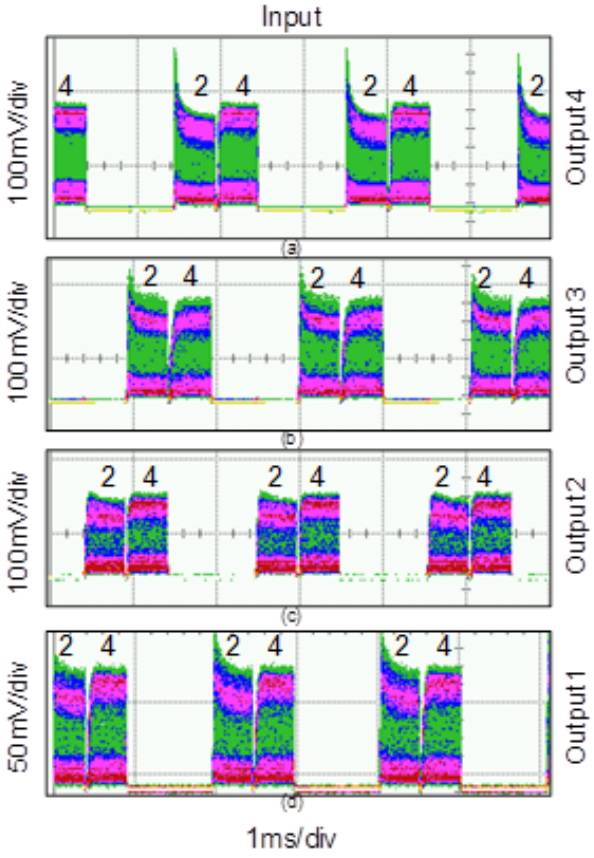


Figure 3.10: Dynamic multipath routing for 10Gb/s data with equalised output power a) Inputs 4 and 2 to output 4 b) Inputs 2 and 4 to output 3 c) Inputs 4 and 2 to output 2 d) Inputs 2 and 4 to output 1

from inputs 2 and 4 are connected to outputs 1, 2, 3 and 4 as the output fibre is scanned. The time traces appear inverted as the on-state voltage is lower than the off-state voltage. Each connection is made for a 500μs time-slot, and then broken for three 500μs time-slots. 16μs guard bands are also introduced between each time-slot. The period for the control waveforms is therefore 2064μs with each path on for around a quarter of this period. A time-gate signal is also generated by the FPGA to control the error detector. A time window of 350μs is used for gating the error detector, allowing 70% of the transmitted bits to be assessed for every time-slot.

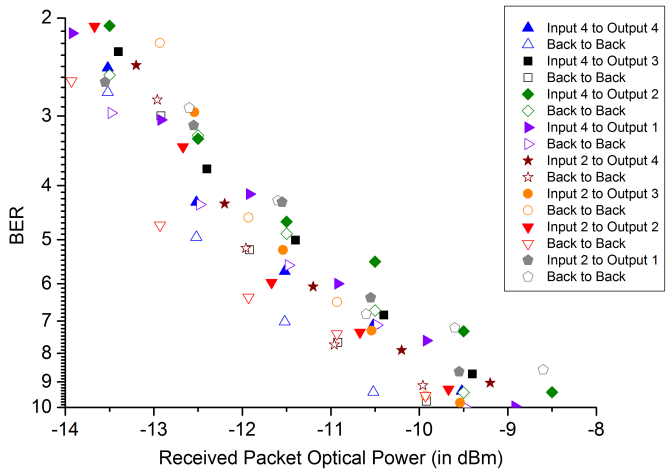


Figure 3.11: Bit error rate performance for dynamic switch performance. Open and solid symbols of the same type and colour represent consecutive back-to-back and routed data.

The optical data routed through the scheduled switch fabric is shown in Fig 3.10. The same time-base is used allowing the clear alignment of the time-slotted data to the control signals in Fig. 3.9. Some overshoot is evident in the connections from input 2 to outputs 1 and 4 but this is more suppressed for the routing from input 4 and to outputs 2 and 3. The overshoots are present due to non-optimal equalisation of the output power for different paths. This is consistent with improved path uniformity between consecutive time slots as seen in Section 3.3.2 and may be attributable to the use of Erbium amplifiers in the measurement path. The colour-graded time traces do however show clean rise and fall transitions, and distinct ones and zeros levels for the on-off keyed data.

Performance is quantified in terms of time-gated bit error rate. The relevant BER curves are plotted in Fig 3.11. The time-gating window is chosen so that at least 70% of the transmitted bits can be assessed for every time-slot and a majority of the overshoot is also avoided. However, the gating window has not been precisely optimised and scanning it across the time traces to select each of the routed time-slots is expected to improve it. A fibre is also scanned across the four different outputs to characterize the output signals in turn. Back-to-back measurements are also performed during their relevant time-gated operation individually for each set of through the chip measurement. Under this multiple-path, dynamically-scheduled

mode of operation, power penalties are measured in the range 0.4dB to 1.1dB which are comparable to those reported for the static data routing scenario as shown in Table 3.2. The most prominent difference in power penalty is seen noted for the path from input 4 to output 4. During the static measurements, bench top power supplies with voltage control accurate up to 10mV were used whereas in case of the dynamics, the control plane setup used was limited by the 8-bit DACs allowing for a voltage control of up to 39mV. Thus the bias set to the switch elements in both cases were not exactly the same leading to a nominal increase in power penalty in case of the dynamic measurement.

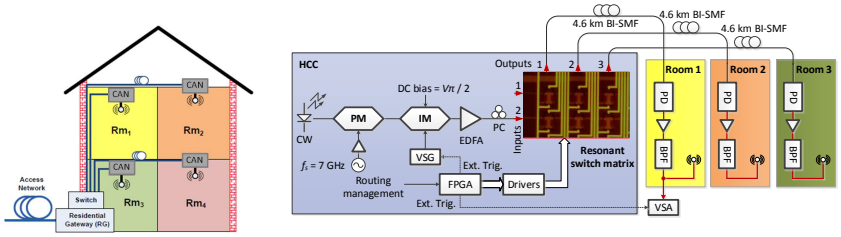
Table 3.2: Power penalty under static and dynamic condition

Input port	Output port (in dB)							
	1		2		3		4	
	Static	Dynamic	Static	Dynamic	Static	Dynamic	Static	Dynamic
2	0.2	0.5	0.0	0.4	0.0	0.6	0.5	0.7
4	0.2	0.4	0.6	0.8	0.8	0.8	0.2	0.8

3.4 Millimetre-Wave Signal Generation and Routing

A concept for a mm-wave signal generation and routing scheme as described by Zou *et. al*, in [126] is used to optimise the time gated performance of the switch elements and the schematic is shown in Fig. 3.12. The box-like filter response of the fifth-order resonant elements allows the phase modulation to intensity modulation conversion required in optical frequency multiplying (OFM) schemes to generate the mm-wave signal as integral multiples of the sweep signal used [126]. Furthermore, the switch matrix provides routing functionality by dropping a particular wavelength at the desired output. The radio frequency (RF) data is eventually up-converted as a double sideband signal at each RF harmonic after direct detection. In the final step, electrical BPFs are used to extort the mm-wave signal from air radiation.

A scheme to up-convert the intermediate frequency (IF) signal and route it to the cell access node (CAN) simultaneously is used as a proof-of-concept demonstration. In Section 3.4.1 this concept is extended to dynamic routing



(a) (b)

Figure 3.12: (a) In-building star architecture. (b) Resonant switch matrix utilised in routing and mm-wave generation.

between mm-wave pico-cells for in-building networks by using the resonant switch matrix and the time gating window per switched time slot is analysed in the process.

3.4.1 Dynamic Routing and Generation

The experimental setup is the same as shown in Fig. 3.12. A 64-quadrature amplitude modulation (QAM)/128-QAM format with a 25MSym/s is used in the following experiments. The paths from input 2 to output 1 and input 2 to output 3 are used for simultaneous data routing and they exhibit 3.74 dB and 4.2 dB on-chip losses respectively. A scheduling scheme was implemented using the control plane described in Section 3.3.1 and 400μs periodic signals with a 50% duty cycle is used for the experiments.

Fig. 3.13 shows the EVM value of the received 175Mb/s, 128-QAM signal at 37.5GHz as measured at CAN 1 and CAN 3. The constellation diagrams at an EVM of 2.2% shows clear and distinct points without any visible distortion. The performance at different powers for both the CANs are comparable leading to negligible power penalty. The best case EVM obtained is 2.2% for either CANs and it is used as the reference for the subsequent analysis of dynamic multi-path switching.

Fig. 3.14 shows the times traces of the received mm-wave signals at CAN 1 and CAN 3. The lowermost trace is of an FPGA generated time trace representing the periodicity and the duty cycle of the signal used to activate the path leading up to CAN 1. The vector signal generator (VSG) generates a packet signal with a symbol length equal to the on-period of the switched path and the transmission is activated by the rising edge of the switched signal from the FPGA. An internal delay of 3.5μs exists in the

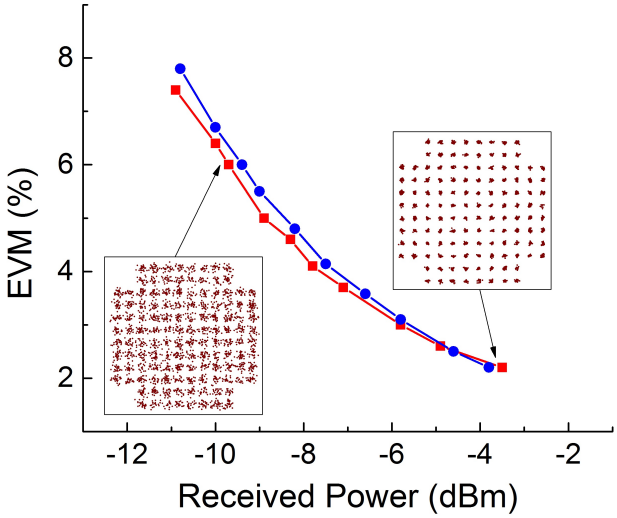


Figure 3.13: EVM performance for two routings from HCC to picocells with CAN 1 as (□) and CAN 3 as (○).

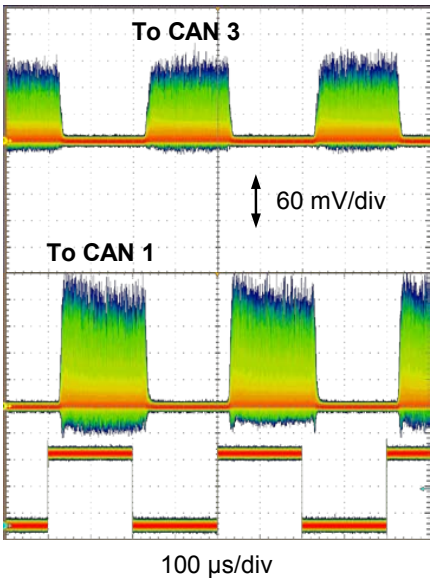
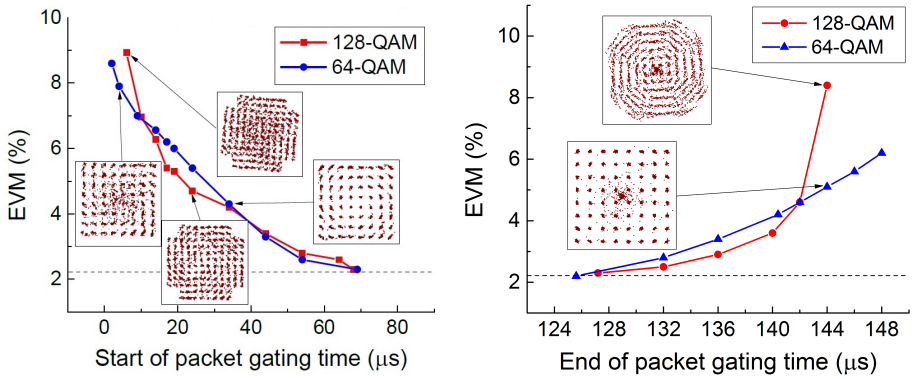


Figure 3.14: Time trace of received mm-wave at 37.5 GHz at CAN 1 and CAN 3.

VSG when it is actuated by an external trigger. Demodulation in the vector signal analyser (VSA) at the CAN side is triggered by a similar external trigger, with a 26μs delay being added to it so as to compensate for the propagation time of the optical signal through the whole system and the trigger delay observed at the VSG. Equal number of symbols are recorded in the VSA as in the VSG in order to ensure that the mm-wave signal is transmitted and analysed only during the on-period of each switched path.



(a) (b)

Figure 3.15: (a) EVM trends of received mm-wave signal impacted by the rising and (b) falling edges of switching window.

Reconfiguration time of the dynamic routing system is studied in terms of the performance achieved for varying gating times as a function of a fixed switched time slot. The routing to CAN 3 from residential gateway (RG) is highlighted for this purpose and the study is performed by qualifying the quality at the rising and falling edges of the control signals i.e. at the off-on and on-off transitions. Signals from the FPGA are used to provide the timing for each switch. An additional terminal of the FPGA is used to form a waveform which is a replication of the timing features of the control signal used at the switch under test and this waveform is used to trigger the VSG so as to maintain synchrony. On being triggered, the VSG generates a 64-QAM/128-QAM packet of length 2000 symbols which is equal to an 80μs time duration. An additional delay with a varied offset is then applied to both the transmitter and the receiver to scan the gated measurement window relative to the start of the off-on transition i.e. actuation of the concerned switched path. Fig. 3.15a shows the generated plot revealing that for measurements in which the gating period is offset by less than

68μs from the initiation of the off-on transition, the EVM is degraded. The constellation for both 64-QAM and 128-QAM as shown in inset, are distorted in this region of operation owing to the fact that the demodulator does not receive sufficient power to track the phase of the received mm-wave signal. However, when the offset is set to 68μs or higher, the EVM is measured to be 2.3% which is comparable to the values obtained in the static case using the same path. Hence, maximum utilisation of the bits at each switched time window is observed when the gating period starts 68μs after the off-on transition of the switch control signal. Fig. 3.15b shows a similar plot but for the analysis of the on-off transition and its effects on the performance. In this case, gating signal extending up to 128μs before the on-off transition exhibit intransigent performance. Considering the fact that after 148μs the control signal transition from on-off, it is concluded that in order to maximise the utilisation of bits in each time window, the gating time has to end 20μs before the switch control signal. Similar measurements were done for the signal routed to CAN 1 revealing comparable performance.

3.5 Conclusions

BER measurements at line rates of 10Gbps are carried out across the 8×4 matrix making it the largest Silicon based resonant switch matrix to date. High data rate routing of 40Gbps data across representative paths yield comparable performance to the 10Gbps routing. As a precursor to simultaneous multi-path circuit analysis in the case of switched paths, an easy-to-use control plane, in which the scheduling is managed via a single desktop run C++ interface is first implemented to govern the duration of each switched path. Further analysis of the switch matrix is then performed to reveal switching speeds in the order of a few μs. The switching speed is limited by the thermo-optic switch actuation process used. A cumulative loss arising from the feed-through approach of the matrix architecture implies that power equalisation at the output is essential. The first demonstration of simultaneous, multi-path dynamic routing measurements have also been shown in an optical switch matrix composed of higher order resonator elements. Power penalties between 0.4 to 0.8dB are observed during time gated power penalty measurements for the combination of eight paths tested, indicating low levels of crosstalk and signal degradation. The gate time is chosen so that at least 70% of the bits in each switched sequence

are accounted for in each BER measurement but further optimisation of the said gating is still required. Hence, a study of the gated time period is carried out using scheme which performs orthogonal frequency-division multiplexing (OFDM) generation and routing and as a result, it is observed that the most optimised gating window is obtained when it is 68μs after the off-on transition and 20μs before the on-off transition of control signal of the switch element under test.

Chapter 4

Active-passive integrated InP based Ring Resonator Switches

In this chapter, a third-order resonator based switch matrix is designed in an active-passive integrated InP platform. The possibility to incorporate high efficiency phase modulators for fast switch actuation and on-chip gain for loss compensation makes active-passive integrated InP platform very attractive for implementation of such resonant switches. Tools currently in use for InP circuit fabrication, provide critical dimensional control in the order of ±500nm. Therefore, a study is performed into the achievable dimensional control and its potential impact on the fabricated chip performance. In order for the fabrication and realisation of the circuit, the critical dimensions of the foundry process are first determined based on which the matrix circuit is designed to give rise to the first InP based switch matrix using higher-order resonant elements. The switch elements are then qualitatively analysed in terms of their spectral characteristics, the switch extinction and the tuning mechanism employed. The on-chip losses are then probed to understand their origins and to pave the path for a lower loss design. Finally, the circuit is characterised by passing 10Gbps data through two different paths of the circuit.

4.1 Introduction

An active-passive integrated III-V photonic ICs provides some additional features as compared to monolithic heterogeneous integrated SOI ICs which are as follows:

- A gain medium can be added to the circuit which will not only help to compensate for fibre to chip coupling losses but will also aid in power equalisation at the output.
- Phase modulators of a given length have a comparable low V_π for both material platforms. However, a relatively simpler layout of the phase modulators eases the involved design aspect and allows the incorporation of phase modulator sections in the directional coupler segments as explained in Section 4.2.1.

The above factors have motivated the implementation of a new higher-order resonant switch matrix design on III-V substrate.

4.1.1 State of the Art

Most of the work done on resonators on III-V material system relates to using them as filters, switches, logic gates, modulators and lasers [51, 87–105]. All the demonstrations listed use only a single switch element. Majority of the work is based on single-order ring with the work by Ibrahim *et al.* [94], standing out. The single ring to bus waveguide coupling section used, are fused together as shown in Fig. 4.1a. This is done in order to achieve a higher coupling coefficient for a short coupler length and device circumference. A demonstrated bandwidth of 97.5GHz, and an out-of-band extinction of 30dB makes this work distinct because of the performance achieved. Data routing at line-rates up to 30Gbps have also been demonstrated using this device. However, precise control of the coupling coefficients in such structures is difficult and it is plausible that this issue might prohibit the application of such devices in a large scale switch circuit.

Higher-order resonators have also been demonstrated [89–92, 97–99, 101, 103, 104]. Guzzon *et. al.* [100] have integrated SOAs into the arms of a third-order element as shown in Fig. 4.1b. The gain sections are used to demonstrate a loss less filter while the tunable couplers are used to set the desired coupling coefficient between each arms of the same third-order resonator. Phase modulators located in the waveguide bends are used for

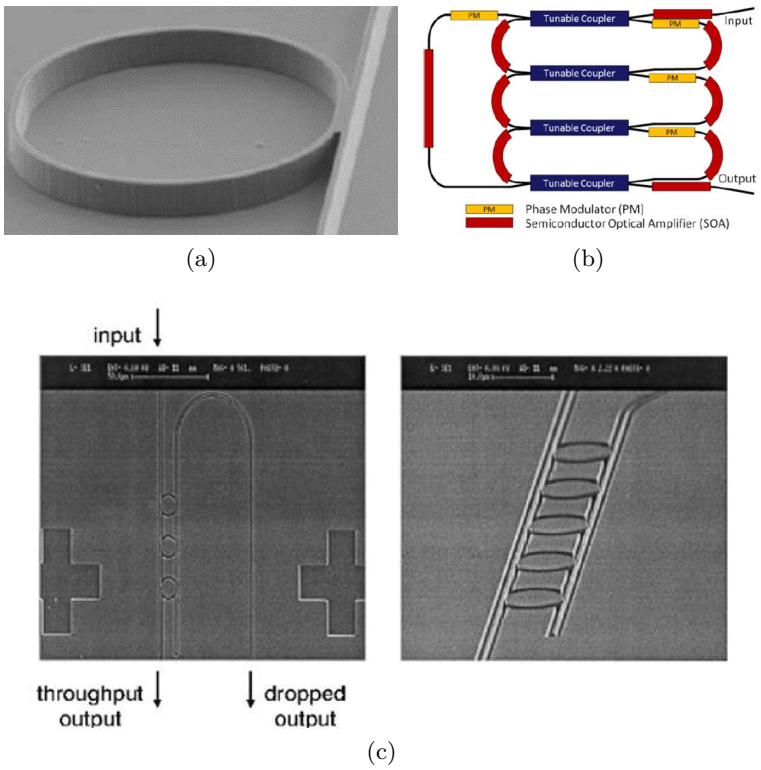


Figure 4.1: (a) Fused bus and resonator coupler fabricated by Ibrahim *et al.* [94] (b) Schematic of the third-order resonator with gain medium with the resonator arms as used by Guzzon *et al.*. [100] (b) Cascaded multi-ring arrangement as fabricated by Ma *et. al.* [103].

individual phase matching between the different arms as well. This device has been used to demonstrate an out-of-band extinction of 30dB but a limited bandwidth of at most 7GHz. Furthermore, use of MZI based couplers have also allowed for 2π tuning to be achieved while applying 6.25mA in forward bias. Fig. 4.1c shows the three and five cascaded resonators fabricated by Ma *et. al.* [103]. The five resonators cascaded element has been used as filters with 437.5GHz along with an out-of-band extinction of 12.5dB. All the demonstrations involving tuning have also relied on individual electrodes for tuning each arm of a single resonator which helps to compensate the phase mismatch arising from fabrication variations. Thus, in a circuit consisting of n^{th}-order resonators, the number of electrodes multiplies by a factor of at least (n+1). An increase in the number of electrodes by such

a factor limits the scalability of such circuits. Moreover, all the demonstrations are limited to a single device so large scale circuit demonstrations using laterally coupled resonators fabricated on monolithic III-V platform is unexplored.

4.2 Design

The designed switch matrix is based on third-order resonant elements, fabricated on active-passive integrated InP platform by SMARTPhotonics. Two different etch depths are used for processing of the wafers, viz.- a Shallow Etch which etches into the confinement layer while the Deep Etch entails etching all the way past the thin confinement layer.

4.2.1 Optical Switch Element

There are three different kind on waveguide layers used in the design of the switch matrix as highlighted in Table. 4.1. The active section has a confinement layer consisting of gain material in the form of multiple quantum wells. Both the active and phase modulator layers have a topmost p+ layer in order to enable the formation of ohmic contacts. The phase modulator and passive layers are both comprised of bulk quaternary films in its confinement layer with the p+ doped top contact layer being etched away in the case of the passives. This is done to give lower waveguide losses in this section and also to allow metal wiring run over the purely passive sections.

Table 4.1: Types of waveguide layers used in 4×4 switch matrix design

Waveguide type	**Confinement layer**	**p+ doped top contact**
Active	Multiple quantum wells	Kept intact
Phase modulator	Bulk quaternary thin film	Kept intact
Passive	Bulk quaternary thin film	Etched away

Third-order resonators are the preferred choice of switch elements to be fabricated on active-passive integrated InP platform. The target of this design was to fabricate a 4× matrix so the choice of the order is mainly based on a combination of the device footprint and the foundry defined die size. Fig. 4.2 is a mask image of a single, third-order resonant switch element and

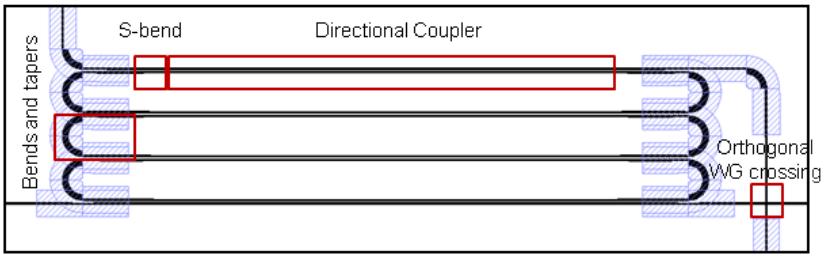


Figure 4.2: Mask image highlighting the optical layout of a single switch element. The black lines represent all the fabricated waveguides while the blue hashed section highlight the deep etched sections.

Fig. 4.3 which highlights the different components used. Each third-order switch is 133μm×635μm resulting in a device footprint of 0.08mm^2. The different sections of each device can be categorised as follows:

- Directional Couplers: Shallow etched passive waveguides are used to form the couplers. 450μm long couplers are designed by placing 2.0μm wide waveguides next to each other. A constant coupler length is maintained and the coupling coefficient is optimised for each individual arm by varying the separation of the directional couplers. The waveguides in between the outer two arms and the input-out buses are maintained at a spacing of 1.1μm (45% coupling) and 1.56μm (9% coupling) between the outer arm-to-bus and outer-to-inner arms respectively. The choice of the minimum waveguide spacing was determined by the test structure analysis done in Section 4.3.1 while the coupler length required to meet the desired coupling coefficients was determined using optical propagation simulation tool, FimmPROP [119].

- Phase modulators: The entire length of the directional couplers are also defined as phase modulators which serve two purposes viz.-

  - ☐ They aid in optimising the phase of different arms of each switch in order to achieve the required phase matching condition within each third-order resonator.
  - ☐ They are also used for switch actuation.

- S-bends: Shallow etched S-bends are used at either ends of the directional couplers in each arm in order to increase the separation

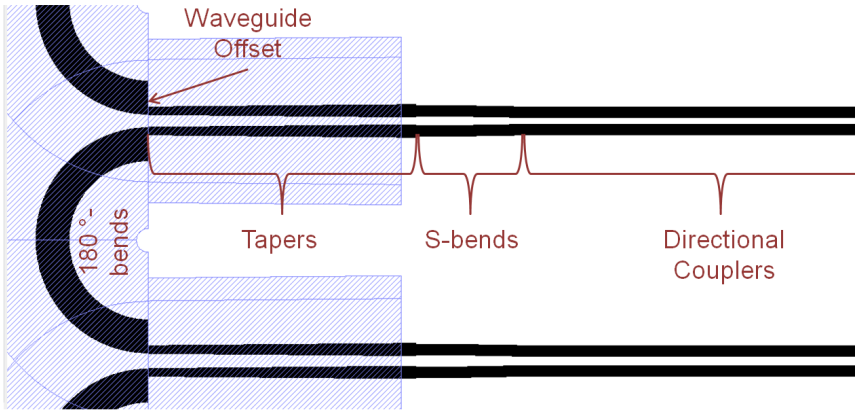


Figure 4.3: Mask image highlighting the different components of a single arm of the third-order resonator.. The black lines represent all the fabricated waveguides while the blue hashed section highlight the deep etched sections.

between two consecutive coupled waveguides. This allows the scope to add lateral tapers after the S-bend while maintaining a spacing greater than 1.1μm between the wider end of two consecutive tapers. The S-bends used have a length of 25μm and a height of 0.25μm.

- Tapers: Lateral tapers are used at the end of each S-bend as transition from shallow to deep waveguides. Each taper is 45μm long, 2.3μm at the shallow-etched wider end and 1.5μm at the deep-etched narrower end. Simulation using optical propagation simulation tool, FimmPROP reveal that a loss of 0.2dB can be expected per taper.

- 180°-bends: Deep etched bends operating in the whispering gallery regime are used to complete each resonant arm. The bends are 6μm wide and have a radius of 20μm and are designed to have an offset of 0.089μm with the straight waveguides. Each 180°bend is expected to have a loss of 0.2dB [127].

Fig. 4.4 shows the theoretical spectral response expected for each designed resonant element. A round-trip length i.e. the length of each arm of the third-order switch element of 1305μm results in the device having a FSR of 0.5nm or 62.5GHz with the relevant theoretical computations suggesting a pass bandwidth of 0.08nm or 10GHz. However, no losses were considered during this theoretical computation which renders this spectral response as ideal.

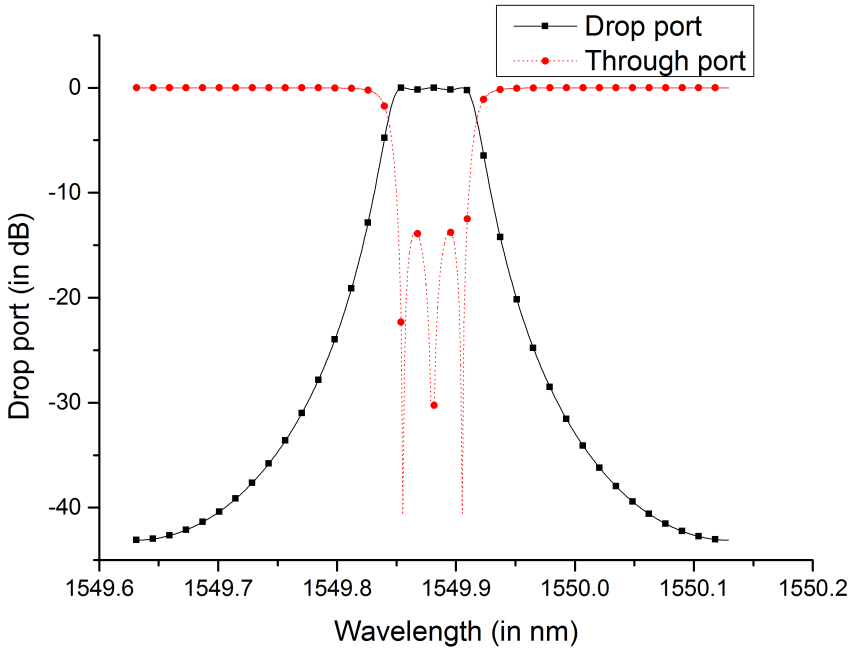


Figure 4.4: Theoretical spectral response of each third-order resonant switch element.

4.2.2 Directional Couplers

Based on the analysis presented in Section 4.3.1, two different waveguide separations of 1.1μm and 1.56μm are used in the implemented directional couplers. This difference in waveguide separation leading to a difference in the etch area is expected to give rise to different etch depths in different couplers. The waveguides with 1.1μm separation are expected to have a lower etch depth in between them as compared to the waveguides with 1.56μm separation. To understand the effects of this variation of etch depth on the coupling coefficient, directional couplers with a fixed coupler length of 450μm and a varying etch depth for the two sets of waveguide separation used are simulated and the results are plotted in Fig. 4.5. For the purpose of this simulation, the outer side-walls of the waveguides are assumed to be etched all the way into the quaternary layer and the etch-depth in the inner side-walls, separating the two is varied. It can be seen from the figure that for deeper etch depths, above 150nm, the coupling coefficient is almost unchanged with variations in etch depth but as the etch depth is reduced, the coupling increases non-linearly. In the plot depicting a

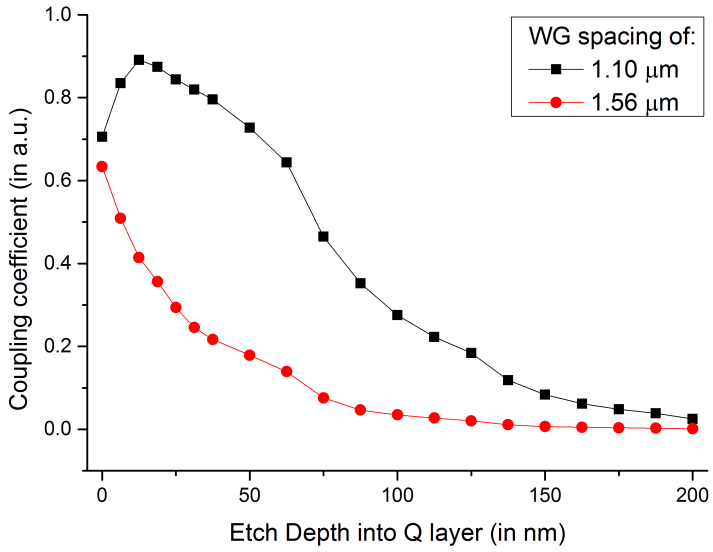


Figure 4.5: Coupling coefficient as a function of etch depth for two different waveguide spacings.

waveguide spacing of 1.1μm, for etch depths lower than 50nm, the two waveguides are found to be very strongly coupled as the modes in the two almost tend to behave as a single mode leading to an erratic nature of the plot in the region below 50nm etch depth.

4.2.3 Electrical Layout of Switch Element

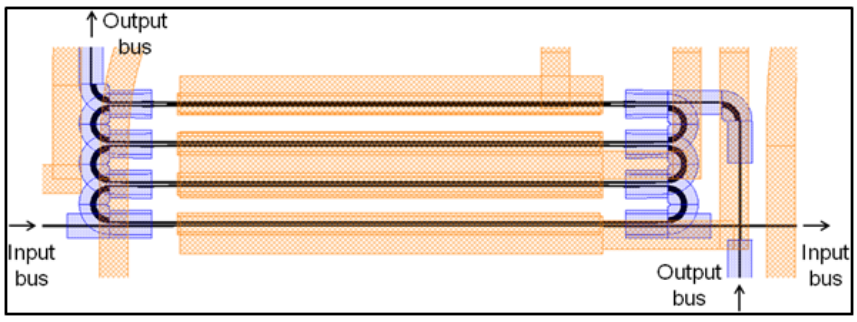


Figure 4.6: Mask image highlighting the optical and electrical layout of a single switch element.

Each third-order switch element consists of three control electrodes in the form of phase modulators acting on quaternary waveguide layers visible as orange blocks in Fig. 4.2.3 and one common ground on the backplane. The three control electrodes are made by designing two metallised pads placed over each of the outer arms of the switch element with a common metal pad over the two arms at the centre of the third-order resonator. Using three individual pads, provides a higher degree of freedom as they can be used to individually phase match the different arms of the switch element in order to overcome any fabrication induced variations in dimensions. Hence for the entire fabricated 4×4 switch matrix under test, we end up with 48 control electrodes and a common ground.

4.2.4 Circuit Concept

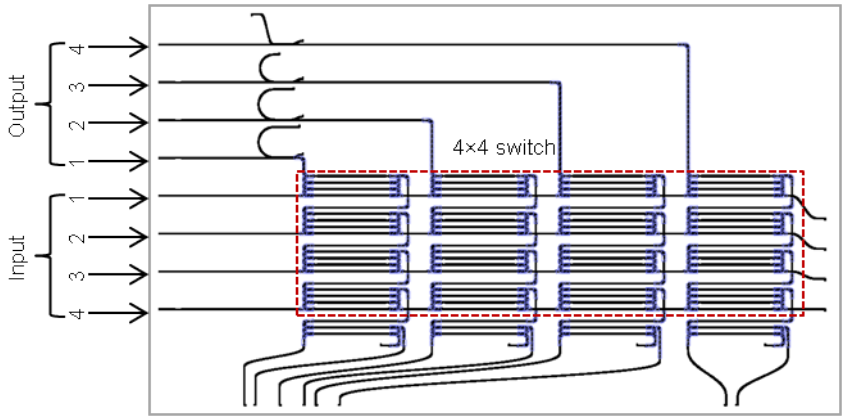


Figure 4.7: Mask image of the designed 4×4 switch matrix on active-passive integrated InP platform. The red lines represent the optical layout while the grey lines and boxes depict metallised sections.

Fig. 4.7 is a mask image of the designed circuit with the switch matrix highlighted. Each optical switch element is placed on a grid with a horizontal pitch of 850μm and a vertical pitch of 250μm. The layout consists of four horizontal input buses and four vertical output buses with shallow etched waveguides crossing each other at 90° forming orthogonal crossings. The input and output buses are led off the left edge of the chip to and a pitch of 250μm is maintained between each consecutive input-output facet. Thus, a 4×4 matrix circuit is designed. 500μm long SOAs are placed after

each input-output port. The SOAs are meant to compensate the fibre-chip coupling and on-chip losses while the SOAs at the output bus are also meant for power equalisation at the output. A fifth row of single-order rings is placed below the fourth and final row of third-order switches and is connected to a row on-chip photodiodes, to be used as on-chip feedback elements. Each input bus ends in a column of photodiodes situated at the right edge of the chip providing through port monitoring. A final set of photodiodes are also placed at each output to enable monitoring of the output.

4.3 Fabrication

4.3.1 Calibration

Resonator based switch circuits are made as compact as possible to achieve the following advantages:

- A device with smaller footprint gives rise to the possibility of denser circuits.
- Light in resonant devices passes through the resonator sections multiple number of times. Thus, the overall loss in the coupled path is a function of the lumped losses per round trip and the length of each round trip. Hence, for fixed waveguide and component losses, a diminished device size leads to a reduction in the loss incurred at the resonator-coupled output.

However, there are certain trade-offs which restrict the size of the resonant device:

- A minimum resolvable feature size can be attained during fabrication. This is process dependant and a constraint determined by the fabrication tools used by the foundry.
- A resonant switch used in a matrix circuit would require a tuning mechanism which is at least able to induce a π phase shift. For phase shifters with a fixed length, a tuning efficiency of V_π i.e. the minimum required phase shift can only be ensured by using a certain length of phase modulators making it a parameter which needs to be optimised during design.

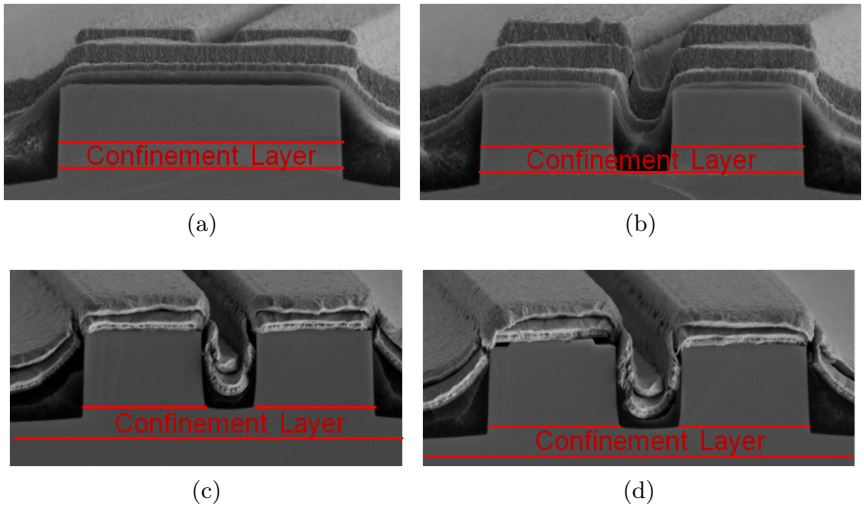


Figure 4.8: SEM images designed to have a varying waveguide separation of: (a) 0.75μm and (b) 1.22μm in deep-etched waveguides. (c) 1.05μm and (d) 1.52μm in shallow-etched waveguides

Table 4.2: Comparison of designed and measured waveguide features

Wafer	Etch type	Waveguide width		Waveguide separation		Etch depth[a]
		Designed	Measured	Designed	Measured	
Test wafer	Deep	2.30	Fused	0.75	Unresolved	-
	Deep	2.30	2.61	1.22	1.00	1.64
	Shallow	2.00	2.24	1.05	0.85	1.40
	Shallow	2.00	2.32	1.52	1.08	1.51

[a] Measured using Scanning Electron Microscope (SEM) images shown in Fig. 4.8

In order to understand better the resolvable feature size offered by SMARTPhotonics, a test run is performed using different etch depths and different feature sizes. Fig. 4.8 shows the SEM images of the test waveguides. Sets of shallow etched 2.0μm wide waveguides and deep etched 2.3μm wide waveguides are placed at varying separations. Various sets of waveguide width and separations are used to obtain a better understanding of the minimum achievable and resolvable feature size. Table 4.3.1 summarises the results obtained by using the SEM images in terms of the

resultant fabricated waveguides as compared to the designed specifications and are categorised in terms of the waveguide width and the waveguide separation. For designs with waveguide separations of 0.75μm, the features are not resolved and the two waveguides merge into a single fused section. However, immaterial of the etch depth used, for waveguide separations designed to be 1.05μmm and above, the features do resolve and we end up with two distinct waveguides. In terms of the waveguide geometry, the results in Table 4.2 suggest an increase in width by 0.2μm to 0.3μm of the fabricated waveguides which lead to a 0.2μm to 0.4μm decrease in the waveguide separation as compared to the designed values which is why a critical dimension parameter of 0.1μm is used while designing 4×4 resonator based circuit discussed in Section 4.4, 4.5.1 and 4.6. Furthermore, a key finding in terms of the etch-depth achieved in said structures is that for shallow-etched waveguides, the etch depth varies by a maximum of 100nm for the different separations used.

The most crucial finding of Table 4.2 is that a minimum waveguide separation of 1.05μm is achievable and because of this insight, a minimum waveguide separation of 1.1μm is used in the following circuit design. In order to achieve the maximum required desired coupling coefficient, the directional couplers have to be 450μm long for a waveguide separation of 1.1μm. This allows us to have coupler cum phase modulators which are long enough to ensure the desired phase shift implying both the critical parameters of the design are being met.

4.3.2 I-line design

Fig. 4.9 is an image of the fabricated circuit, with the lightly visible white undulations on the surface being the optical layout and the metallised sections visible as golden lines and rectangles. The external optical connections to the chip are made via the input and output ports placed along the left edge of the chip and two single mode lensed fibres have been used for this purpose.

The placement of two rows of bond pads on the top and bottom edge of the chip and a single column on the right edge imply that the electrodes are scattered throughout the chip and poses a challenge as far as wire bonding the chip is concerned. Hence, a larger SOI tile is metallised and used as a fan-out tile. Fig. 4.10 is a mask image of the said tile with the orange layer highlighting the metallised sections.

The tile design is such that it has a broad single metal block in the

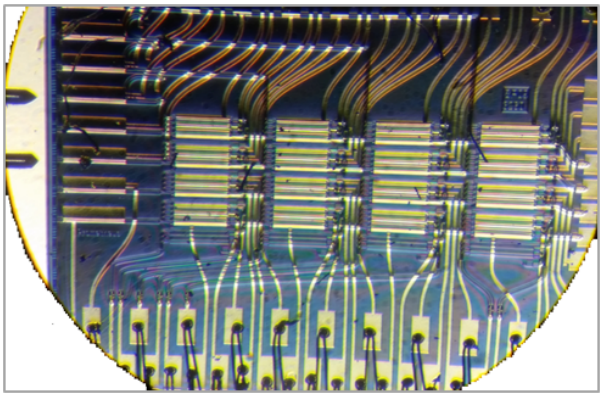


Figure 4.9: Image of the fabricated and wire bonded switch matrix.

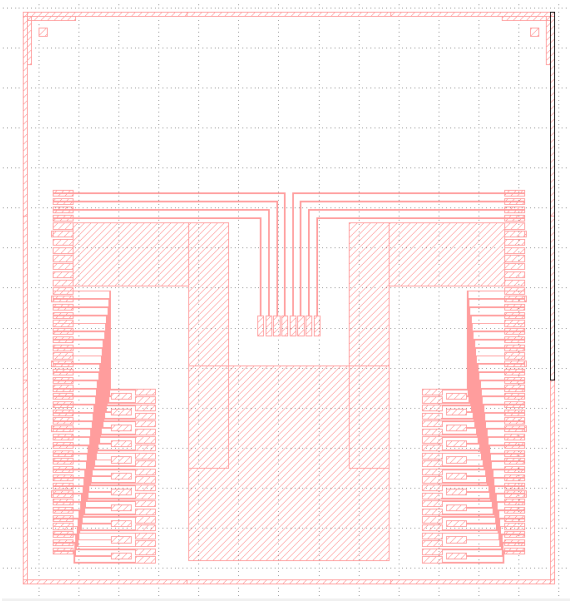


Figure 4.10: Mask image of the fan-out tile used as an intermittent layer leading onto a PCB used for external electrical connectivity.

middle which will enable the substrate of the InP chip to be fixed onto it while maintaining connectivity to the common ground backplane. The inner columns of bond pads in the fan-out chip is a mirror image of the bond pads of the circuit under test while the outer section is such that it

perfectly matches the Printed Circuit Board (PCB) pitch. The InP circuit is then bonded on top of large metal plate at the centre using conductive epoxy. Wire bonding is carried out by first bonding the bond pads in the fan-out tile to a PCB and then from the InP chip to the fan-out tile which enables the opportunity to establish external electrical connections. The chip itself is epoxy bonded onto a water cooled mount where the chiller is maintained at a constant temperature of 22℃.

4.3.3 Deep-UV design

Third-order ring resonator based switch matrix fabricated on active-passive integrated InP platform has been presented. Phase modulators are used to compensate for phase errors between different arms of a single switch element as well as to actuate switching. The on-chip losses associated with each switch element arising as a direct consequence of the different components used limit the scalability of this circuits. The losses can be reduced by:

- Reducing the length of the device which requires the length of the directional couplers to be reduced. Since the coupling length varies as a square of the waveguide separation, by using smaller features, as possible by using scanner lithography, the losses can be reduced further.

- A large portion of the losses arise due to waveguide transition tapers and due to the bends. Moving to higher confinement platforms, for example membrane based InP material platform, such losses can be significantly minimised.

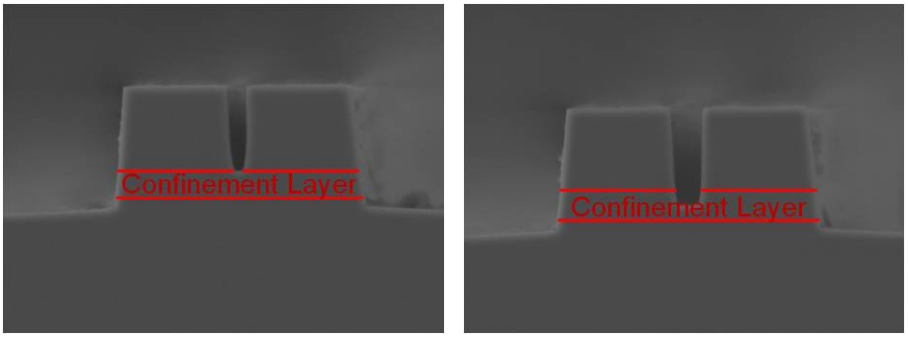
Table 4.3: Component losses

Condition	WG loss (in dB/cm)	Total WG loss[A] (in dB)	Loss per taper (in dB)	Total taper loss[B] (in dB)	Loss per 180°-bend (in dB)	Total bending loss[C] (in dB)	Total round trip loss (in dB)
1	6	0.096	0.2	0.8	0.2	0.4	1.296

A - For two 80μm long waveguides per arm (loss in directional coupler)

B - For four tapers at deep to shallow-etched waveguide transitions

C - For two 180°-bends



(a) (b)

Figure 4.11: SEM images designed to have a varying waveguide separation of: (a) 0.25μm and (b) 0.5μm in shallow-etched waveguides.

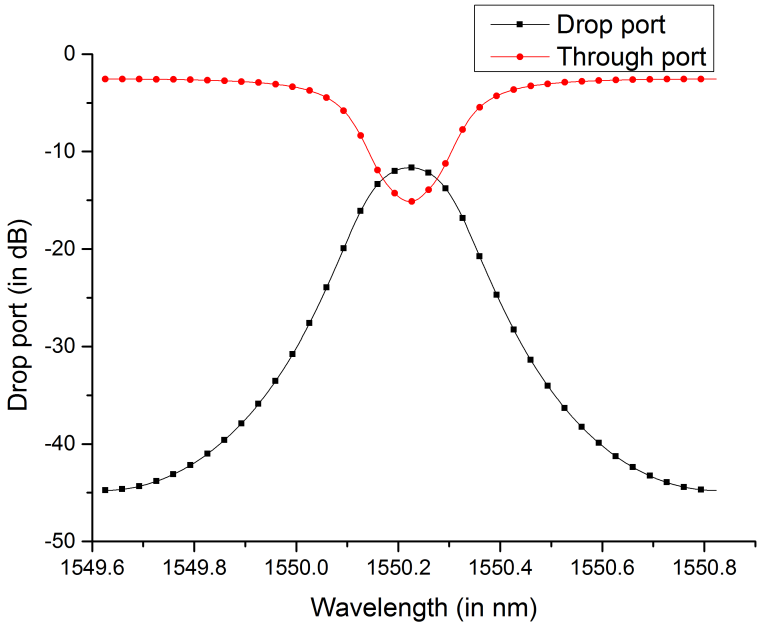


Figure 4.12: Expected spectral response of each third-order resonant switch element as designed for the scanner run.

Fig. 4.11 shows the SEM images using deep-UV lithography for a waveguide separation of 0.25μm and 0.5μm respectively. In both cases, the waveguides can be seen to be clearly resolved and separate. Although the SEM

images are from a test run which is used to determine the achievable feature size using this process, the results are very promising for miniaturisation and hence reducing the losses in resonator circuits in InP platform. Moreover, it provides the possibility of achieving the spectra presented in Fig. 4.12 purely by miniaturising the device circumference.

4.4 Device Perfromance

The performance of individual switch elements of a 4×4 matrix circuit is studied in this section. The phase modulators of each switch element are used to compensate for any phase mismatch between different arms of a single element. Current injection into the phase modulators imply a spectral shift towards the shorter wavelength region while a reverse bias applied to the phase modulators induce a shift towards the longer wavelength region. This adds a new degree of freedom to the tuning mechanism as this grants us the ability to tune in either direction with respect to the spectrum of the device under unbiased condition.

4.4.1 Switch Calibration

Table 4.4: Extinction Ratio at 1549.875nm

Input port	Output port (in dB)	
	1	2
1	16.6	16.1
2	15.2	15.5

The on-state spectra is optimised by tuning each ring such that the peak power is maximised - in order to achieve this, a tunable laser is fixed at a wavelength of 1549.875nm and is fed into the circuit via a polarisation controller. The output of the chip is then monitored on an OSA whilst the peak power at the operation wavelength is noted. The phase modulators are then tuned and a combination of both current injection and reverse bias operation is used. A maximum of 20mA of current is injected while a maximum reverse bias of 10.5V is used. The off-state of each switch element is then determined so that the on-off signal extinction is maximised. In order to measure the on-off signal extinction, the same setup is used. The peak power at the operating wavelength of 1549.875nm is noted using an

OSA during both the on and off state of each element under test. Table 4.4 lists the extinction ratios of all the measured resonant elements with a minimum switch extinction of 15.2dB is measured for the path running from input 2 to output 1.

4.4.2 Spectral Response

The transfer function is recorded by using a tunable laser source which is fed through a polarisation controller onto the input of the circuit. The output from the chip is then fed into a photodiode to monitor the power. The laser is then set to scan using steps of 5pm from a wavelength of 1549.65nm to 1550.25 so as to cover a full FSR which spans across 62.5GHz (0.6nm) of each device while the power is recorded at each instance in order to obtain the spectra.

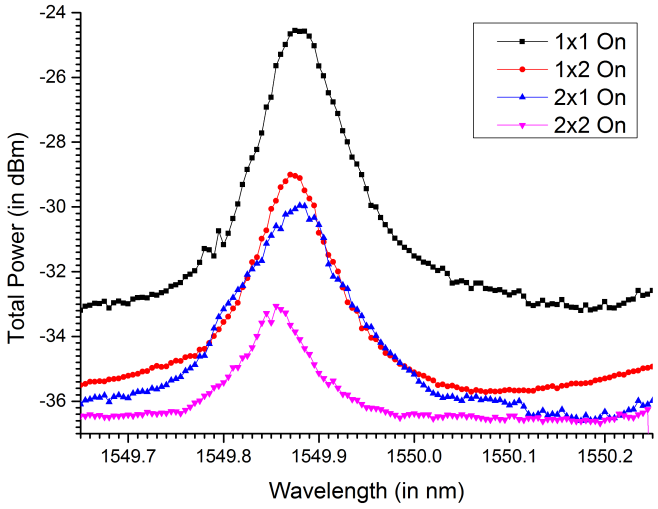


Figure 4.13: Spectral response of all the paths of the 2×2 switch matrix with the fibre to chip to fibre coupling losses subtracted. The passband data is uncorrupted while the stop band is limited by the noise arising from the SOA.

Fig. 4.13 shows the optical spectra of the measured four elements as a part of the 4×4 matrix with the 12dB (2×6dB) fibre to chip to fibre coupling loss already subtracted from the plots. The stop-band part of the spectra is limited by the SOA noise and hence it does not represent the entire spectra along the full FSR of the switch element. However, the passband data is

uncorrupted and can be used to initially qualify the elements. Fig. 4.13 clearly demonstrates a minimum passband width of 11.25GHz (0.09nm) for each of the switch elements.

A clear increase in losses with an increase in path length can be seen in Fig. 4.13 which arises from the matrix architecture itself. The losses for all the paths have been summarised in Table 4.5. The device with the most intrinsic spectra i.e. the device for which the transfer function is independent of others is the switch element between input 1 to output 1. An on-chip, on-state loss of 24.6dB is obtained for this path which excludes the fibre to chip to fibre coupling loss of 12dB. For the other paths, an increase in losses is observed but there are not enough measured paths to accurately determine the exact off-state losses involved. However, the three measured paths with one or more off-state ring suggests that the off-state losses are around 5dB.

Table 4.5: On-chip losses at 1549.875nm

Input port	Output port (in dB)	
	1	2
1	24.55	29.04
2	30.06	33.95

4.4.3 Phase Modulation

Fig. 4.14 presents a study of the phase modulators used in reverse bias. The study is limited to the device from input 1 to output 1 as it represents the most intrinsic transfer function achievable. For the purpose of the study, the two outer phase modulators were tuned together between a range of 0V to -4V with steps of -1V while the inner one is unbiased. The spectra is recorded for each step and the fibre to chip to coupling losses are subtracted from it and plotted as colour map. A shift to the longer wavelength with an increase in reverse bias is noted. A maximum shift of 0.1nm ($\frac{1}{5}^{th}$ of the FSR) is achieved on the application of the -4V bias. However, in order to achieve the required phase shift, during the spectral alignment of each resonant switch with respect to each other, biases up to -10V were used.

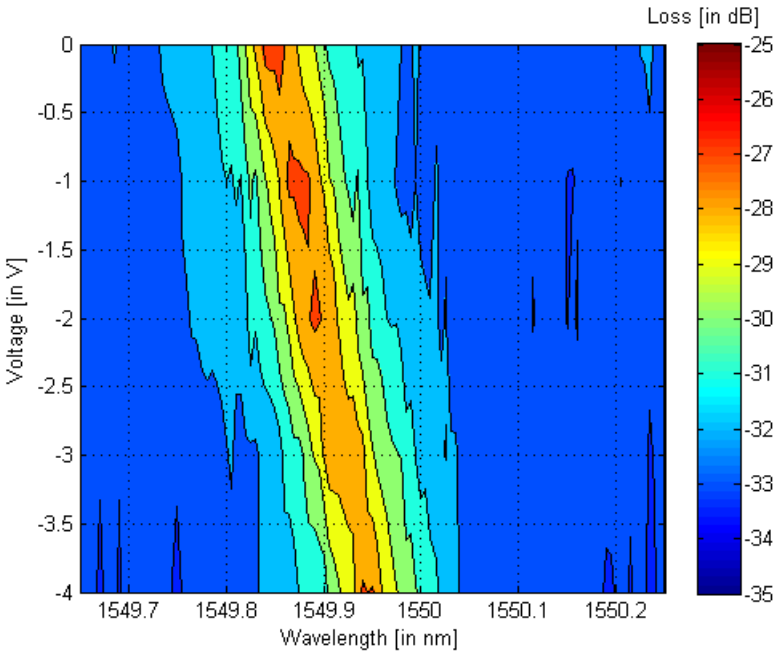


Figure 4.14: Tuning of the switch element connecting input 1 to output 1.

4.5 Circuit Optimisation

4.5.1 Loss analysis

The analysis of each third-order resonant switch element is done in this section in terms of the on-chip losses as a function of the component losses. The on chip losses incurred in the fabricated matrix greatly limit the scalability of the switch matrix and hence an understanding of the origin of these losses is essential for future designs.

Table 4.6 summarises the different component losses which were taken into account. The individual component losses have been added together as lumped losses, summarised as the total round trip loss in each arm of the third-order resonant element. The waveguide losses depicted in the table are related to the losses in each of the 450μm long phase modulators, represented as a variable parameter so different values ranging from 3 to 9 dB/cm have been used. The taper and 180°-bend losses have been determined by simulation using FimmProp. Fig. 4.15 shows the measured spectral characteristics of a single switch element along with several sim-

Table 4.6: Component losses

Condition	WG loss[A] (in dB/cm)	Total WG loss[B] (in dB)	Loss per taper (in dB)	Total taper loss[C] (in dB)	Loss per 180°-bend (in dB)	Total bending loss[D] (in dB)	Total round trip loss (in dB)
1	3	0.27	0.2	0.8	0.2	0.4	1.47
2	4	0.36	0.2	0.8	0.2	0.4	1.56
3	6	0.54	0.2	0.8	0.2	0.4	1.74
4	8	0.72	0.2	0.8	0.2	0.4	1.92
5	9	0.81	0.2	0.8	0.2	0.4	2.01

A - Unknown parameter

B - For two 450μm long waveguides per arm (loss in directional coupler)

C - For four tapers at deep to shallow-etched waveguide transitions

D - For two 180°-bends

ulation fits applied to it. The solid black line without symbols represents the measured spectra for the path from input 1 to output 1. This path is chosen as it also represents the most uncorrupted spectra since it involves only one on-state switch element and none in off-state. The different arms of the resonant element were optimised in order to achieve phase matching between them. The conditions of varying losses as mentioned in Table 4.6 are simulated and the resulting SOA noise is also added to the theoretical spectra. The coupling coefficient is then used to fit the theoretical spectra with the measured one. The different combination of coupling coefficients used are mentioned in Table 4.7. The variations in coupling coefficients are then related to the expected variation in etch depths, which varied within a range of 40nm.

Table 4.7: Simulated coupling coefficients

Condition	Waveguide spacing of 1.1μm		Waveguide spacing of 1.56μm	
	Coupling coefficient	Etch Depth into Q layer (in nm)	Coupling coefficient	Etch Depth into Q layer (in nm)
1	0.47	75	0.10	69
2	0.55	69	0.11	67
3	0.68	56	0.12	65
4	0.78	40	0.15	60
5	0.80	36	0.19	45

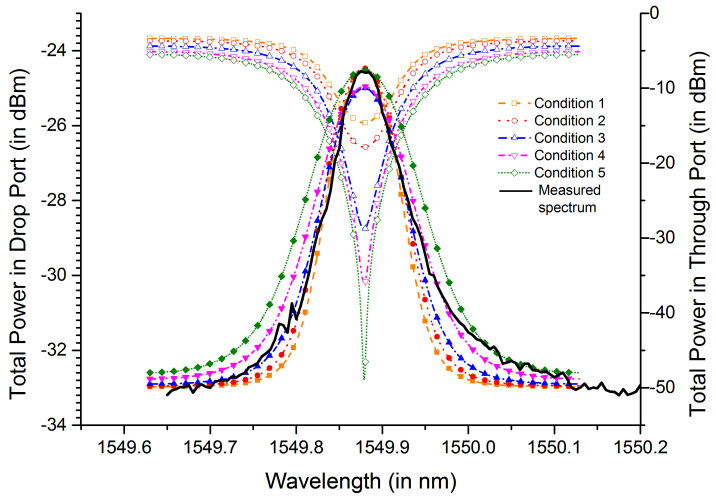


Figure 4.15: Spectral characteristics of a single switch element. Solid black lines represent the measured spectra for the path from input 1 to output 1 with the arms of the resonator phase matched by biasing the phase modulators. The different symbol and line styles used correspond to the simulations using the parameters described as "Condition" in Table 4.6 and Table 4.7 with the open and solid symbols representing the through port and the drop port respectively. The black line represents the measured spectrum.

4.5.2 Loss Minimisation

An understanding of the tolerance to losses for each third-order switch element is important for the implementation of a higher degree of scalability in future designs. In Fig. 4.16, the theoretically computed expected spectra for a third-order element with the same size and FSR as the scanner design has been plotted. Different values of loss, specified as the round trip loss per arm of each third-order element have been specified showing the evolution of the spectra from a box-like Lorentzian shape starting from the 0dB loss condition to an almost Gaussian shape as the loss increase to 1.131dB. In order to maintain the desired spectral shape, round trip losses less than 0.566dB seem to be ideal. The on-state losses in that case are expected to be less than 5dB which is a remarkable improvement from the current design and would greatly aid the prospects of scaling similar circuits.

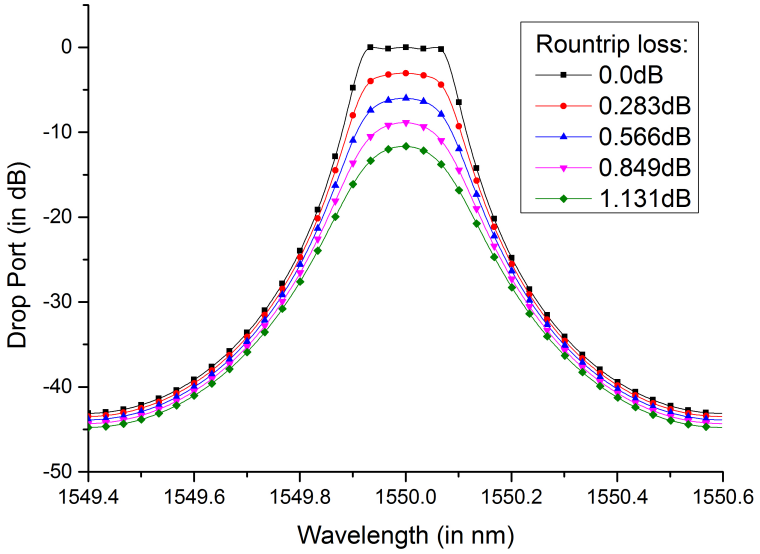


Figure 4.16: Expected spectral response of each third-order resonant switch element as designed for the scanner run. Different round trip losses have been used to highlight the evolution of the transfer function.

4.6 Data Routing

Quantification of the matrix switch circuit performance is performed in terms of the power penalty incurred by carrying out BER measurements across two representative paths of the circuit.

4.6.1 Static Routing

BER are measured for the two representative paths using the setup shown in Fig. 4.17. A tunable laser tuned to 1549.875nm is used as input to a MZI based modulator which is modulated at 10Gbps using a 2^{31}-1 PRBS and amplified using an EDFA. The modulated pattern is then passed through the chip and its output paseed through a 0.9nm FWHM BPF and onto a combination of an EDFA and a BPF with a FWHM of 1.52nm is fed to a XFP APD receiver and onto a BER tester. The resultant BER curves are plotted in fig. 4.18 as a function of the received optical power for the switch elements at the intersection of input 1 and output 1 and input 1 and output 2. Back to back measurement are done by replacing the chip with an optical attenuator which is used to replicate the on-chip losses. To

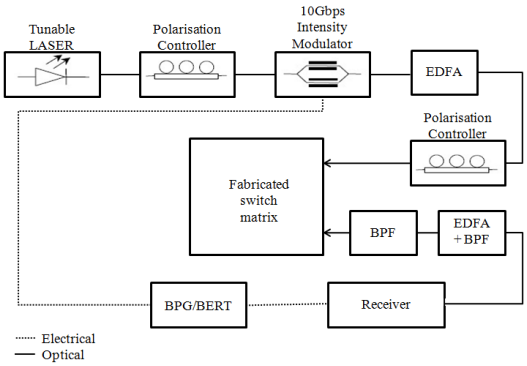


Figure 4.17: Schematic showing the experimental setup used for BER measurements.

maintain a high level of consistency, each through the chip measurement is followed by its corresponding back to back measurement.The path from input 1 to output 1 has a power penalty fo 2.5dB while the paths from input 1 to output 2 incurs a penalty of 2.2dB. A curved tail at the end of each measured BER plot is observed and it is attributed to the on-chip SOA noise.

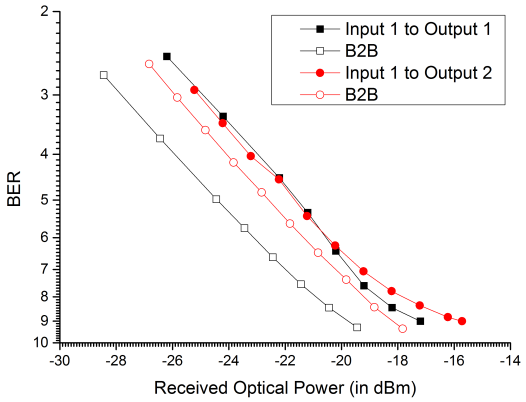


Figure 4.18: Bit error rate as a function of received optical power for the measured representative paths. A 10Gbps, 2^{31}-1 PRBS sequence is used. The solid and open symbols represent the routed and back to back measurements.

4.7 Conclusion

The first 4×4 third-order resonator based switch matrix has been fabricated on InP material platform. A study has been performed to identify the fabrication limits that can be achieved, based on which the design and subsequent fabrication is performed. Each switch element is demonstrated to have a bandwidth in excess of 11.25GHz along with a minimum switch extinction of 15.2dB with a maximum power penalty of 2.5dB measured in tested paths. However, the on-chip losses of 24.6dB limit the scalability of such circuits which has prompted a study exploring its cause. Tolerable losses in terms of the round trip loss per arm of the resonator have been analysed, based on which, a new design utilising the improved feature size provided by deep UV lithography has been used as a route to reduced losses in such devices.

Chapter 5

Vertically-coupled Micro-ring Resonator

In this chapter, three dimensional integration of resonator based devices are studied. Vertical integration leads to a step change in miniaturisation while maintaining improved critical dimensional control provided by the epitaxially grown layers. New techniques and designs are developed leading to a novel resonator device layout. Simulations in order to provide a fabrication tolerant, wafer bonding free, single side processed, dual-plane, high density photonics platform is explored, and the resonance is exploited as a suitable route for DWDM circuits.

5.1 Introduction

3D electrical wiring in electronic ICs enable the extension of CMOS performance by providing a higher functionality per chip. Similarly, 3D optical wiring using multiple confinement layers in a vertical plane, leads to the possibility of a higher density in the functionality achieved per chip. Optoelectronic devices exploiting this phenomenon, using two optically confining waveguide layers in one vertical plane have been studied previously across a variety of material platforms, demonstrating their implementation in waveguide crossings [128], filters [108, 110–112], switches [107, 129–135], multiplexers/demultiplexers [44, 109, 114], modulators [66, 106, 136] and lasers [113, 115].

A large section of such demonstrations are based on vertical directional couplers [128–136] where the evanescent coupling between two parallelly

running waveguides are utilised. The key advantage in these demonstrations rest upon the fact that other than the demonstration done by B. Liu *et al.*, in [134], all the others are fabricated using standard fabrication techniques and without any wafer bonding. Low power switching has been demonstrated by F. Dollinger *et al.*, [133] in which, 85μm vertically coupled devices are switched on the application of 5V reverse bias with a nominal switch extinction of 10dB. R. Varrazza *et al.*, [135], fabricated a lossless 4×4 crossbar switch matrix using active-gain material and vertical directional couplers in combination with TIR mirrors. Dense optical wiring requirements in a circuit necessitates the need for waveguide crossing. 3D optical circuits as well are no exception and waveguide crossing in such structures have been shown by D. D. John *et al.*, [128]. Multimode waveguide crossing have been shown to be favourable in this case with a nominal loss of 0.25dB per crossing being demonstrated. While the switch and waveguide crossing ideas are useful for implementation in DWDM circuits, a suitable design of modulators using such structures is lacking which has prompted a study of resonator structures vertically coupled to a bus waveguide located on a different confinement layer in the same vertical plane as discussed in Section 5.1.1.

5.1.1 Vertically-coupled Resonant Devices

Vertically coupled micro-ring resonators are another form of devices which have been intensively studied using 3D optical wiring schemes. The advantage of improved density in circuits have been previously discussed in Section 5.1 but in case of micro-ring resonators, vertically coupled structures provide one more key advantage as compared to laterally coupled structures - the separation between the resonator and the bus waveguide is a critical parameter and for laterally coupled resonators, its dependence on fabrication induced variations is higher than the levels that can be achieved using state-of-the art fabrication techniques [48] leading to spectral shifts in fabricated laterally coupled resonant structures. However, in vertically coupled resonators, the separation is determined during the growth process leading to a greater control over it. This concept has been used to demonstrate a multitude of vertically coupled resonator based devices as tabulated in Table 5.1 and Table 5.2.

Based on the material system employed, previously demonstrated vertically coupled micro-ring resonators can be classified as follows:

- All III-V material system based demonstrations rely on wafer bonding processes in order to realise the desired device as shown in the examples listed in Table 5.1 and involve either dual wafer processing on two separate wafers, or using the same material (homogeneous) or of two different materials (heterogeneous) and bonding them together or double sided processing on a single wafer.

- In the examples listed in Table 5.2, Ta_2O_5-SiO_2 compounds are used for vertically coupled resonators, employing RF sputtering for deposition of materials, thus avoiding the wafer bonding process.

Both the tables are arranged chronologically with the spectral characteristics of the resonators and their features being highlighted. Table 5.1 is sub-divided further into three different classifications based on the processing involved.

Table 5.1: Vertically Coupled MRR using wafer bonding

Dual wafer processing		
BW	**Features**	**Group**
0.22	12μm ring radius	K. Djordjev *et al.*, 2002 [137]
Heterogeneous integration		
BW	**Features**	**Group**
-	8μm ring radius	J. Hofrichter *et al.*, 2001 [66]
Double-sided processing		
BW	**Features**	**Group**
0.6	5μm ring radius	R. Grover *et al.*, 2001 [110]
0.6	10μm ring radius	
0.5	10μm ring radius single-order resonator	P. P. Absil *et al.*, 2001 [109]
0.9	10μm ring radius second-order resonator	

Continued on next page

Table 5.1 – continued...

BW (in nm)	**Features**	**Group**
0.4	9.55μm ring radius single-order resonator	R. Grover *et al.*, 2002 [111]
1.5	Three parallely cascaded rings with radius of 9.55μm	
-	1. 20μm ring radius 2. Thermo-optic tuning with a 2π shift on application of 17mW	I. Christiaens *et al.*, 2004 [138]
-	40μm ring radius lasers	A. Bennecer *et al.*, 2008 [44]
-	50 to 80μm ring radius	A. Kapsalis *et al.*, 2011 [113]

Table 5.2: Monolithically Integrated Vertically Coupled MRR

BW	**Features**	**Group**
5.2	6μm ring radius	B. E. Little *et al.*, 1999 [108]
0.51	22.78μm ring radius for two rings and 6μm ring radius for the third	Y. Yanagase *et al.*[a], 2002 [112]
0.61	28.5μm ring radius for two rings and 39.3μm ring radius for the third	
-	38.1μm ring radius for two rings and 59.1μm ring radius for the third	
a: Third-order resonator		

The majority of the demonstrations utilise single-order rings [108, 109, 113, 137–139] with some of the key works being discussed in greater detail. J. Hofrichter *et al.* [66] have fabricated 8μm microdisks modulators in a InP-InGaAsP confinement layer heterogeneously integrated on top of a SOI bus waveguide as shown in Fig. 5.1a with the energy consumption estimated to be 43fJ/bit at a line rate of 10Gbps. The modulator performance has been studied using multiple line rates and compared to the performance of a commercial modulator. Power penalties of about 3.1dB were obtained for line rates of 2.5Gbps and 5Gbps but was further increased to 7.0dB for line rates of 10Gbps. The high penalty is associated with the low extinction ratio obtained and this effect is more pronounced at higher data rates as the extinction ratio decreases with an increase in the data rate. A. Bennecer*et al.*, in [44] have used double sided processing as shown in Fig. 5.1b in order to fabricate a resonator based optical add multiplexer using a 40μm radius microring laser. Single channel and WDM schemes have been studied with a maximum power penalty of 2.4dB observed for transmission of 2.5Gbps data. A. Kapsalis *et al.*, in [113] have also demonstrated vertically couples ring resonators with fabricated devices [115] of different radii as shown in Fig. 5.1c with the devices having a radii between 50μm to 80μm demonstrated to have a threshold current in the order of 10$'$s of mAs.

Higher-order resonators as well as cascaded resonators have been studied using vertically coupled resonators as well. P. P. Absil *et al.*, [109] have used second-order rings placed in different vertical confinement layers to fabricate a 1×4 multiplexer/demultiplexer and achieve a channel to channel crosstalk of < -10dB. Y. Yanagase *et al.*, [112] have used vertically coupled third-order resonator as filters with flat-topped transfer function. Fig. 5.1d shows the schematic with two rings in one confinement plane and one ring and a bus fabricated in another vertical plane. Parallelly cascaded resonant filters have also been demonstrated using a combination of three rings by R. Grover *et al.*, [111]. Higher-order resonators do considerably enhance the bandwidth achieved in such device and lead to a passband with a pronounced Lorentzian box-like shape. However, an additional alignment factor comes into play in these structures which renders the alignment advantages of vertically coupled resonators, mute.

Monolithically integrated demonstrations use RF sputtered Ta_2O_5 and SiO_2, both of which are high dielectric materials and hence not suitable as a material system in which non-thermal phase modulation techniques can

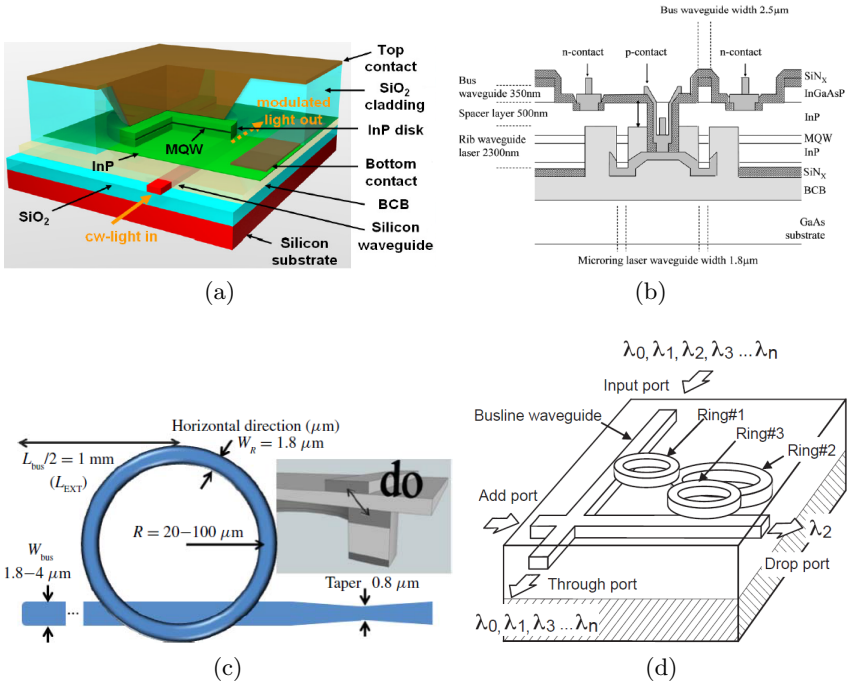


Figure 5.1: (a) Schematic view of an InP micro-disk modulator heterogeneously integrated on a SOI waveguide [66]. (b) Cross-sectional view of the vertically coupled micro-ring structure [114]. (c) Cross section of the vertically coupled micro-ring laser [113]. (d) Perspective view of triple series-coupled micro-ring resonator filter with stacked configuration [113].

be employed. Other techniques demonstrated rely on processing involving wafer bonding in some form which makes the fabrication and realisation of the circuit complex whether it be different wafer processed on a single side and bonded together or a double sided process. Moreover, it also adds a critical alignment step to the process which has been analysed by C. W. Tee *et al.*, [139].

The purpose of the study of this design is to overcome the aforementioned limitations and come up with a monolithically integrated, single side processed design which can be fabricated using standard techniques [140] without compromising the performance of the device. For this purpose, the fabrication tolerance of the design is studied in 5.3 and compared to the existing work in [139]. Moreover, the chosen layers are based on previous demonstrations of active devices, giving rise to the possibility of utilising

electro-optic interactions in the device, facilitating its use as a modulator and laser in DWDM circuits.

5.2 Device Layout

5.2.1 Device Concept

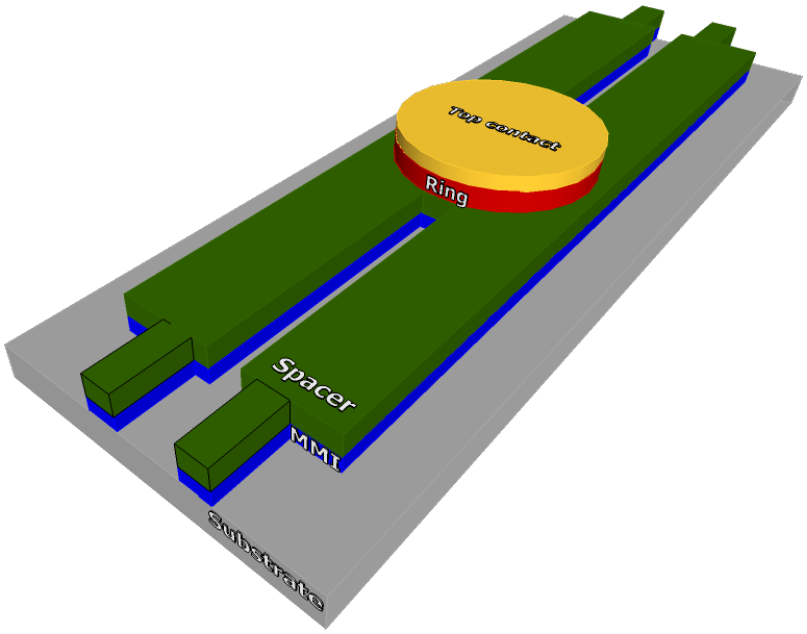


Figure 5.2: Schematic of the proposed vertically coupled micro-ring resonator.

Fig. 5.2 shows a schematic of the proposed 3D device. The device design consists of a two optically confining layers separated by an InP spacer layer. C. W. Tee *et al.*, [139] have demonstrated a relaxed alignment tolerance by using multi-mode bus waveguides. In this design, 1×1 MMI is designed for the same purpose, on the lower confinement layer, depicted in blue in Fig. 5.2. The length of the MMI is chosen to be twice the imaging length and the single mode, input and output waveguides of the MMI are placed at an offset. This is done so that the image within the MMI is shifted towards one of its edges and a stub is placed, centrally along its length and on the opposite edge of the image of the MMI. The stub is a mechanically rigid

platform on which a resonator can be fabricated in the upper confinement layer. It is conceivable that with the usage of this stub, the entire device can be fabricated using single sided processing making the fabrication process a lot simpler than the previously demonstrated concepts discussed in Section 5.1.1. The resonator is fabricated on the upper confining layer depicted in red in Fig. 5.2 and is separated by the MMI using a spacer layer shown in green.

All the components on the bottom waveguide are specified to be deep-etched structures i.e. they are etched all the way past the bottom waveguide layer into the substrate. Similarly, all the components in the top waveguide layer are designed to be deep-etched as well i.e. they are etched all the way past the top waveguide layer and stop at its interface with the spacer layer.

5.2.2 Layer Profile

	LAYERSTACK		
	MATERIAL/LAYER	**THICKNESS (in μm)**	**Refractive index**
	Top contact	0.5	3.165
	InP (Micro-ring Cladding)	1.0	3.165
Upper Waveguide Layer	Q1.25 (Confinement)	0.5	3.3636
	MQW Q1.3(barrier)-Q1.6(QW) (Micro-ring)		
	Q1.25 (Confinement)		
	InP (Spacer)	0.75	3.165
Lower Waveguide Layer	Bulk Q1.25	0.5	3.3636
	InP (Waveguide Cladding)	0.5	3.165
	InP (Buffer)	0.5	3.165
	InP (Substrate)	4.0	3.165

Figure 5.3: Layer profile proposed for the vertically coupler micro-ring resonator.

The proposed layer profile is depicted in Fig. 5.3 with the relevant refractive indices used highlighted. The layer profile is consists of InP-InGaAsP layers [140] and in the proposed scenario, instead of a single confinement

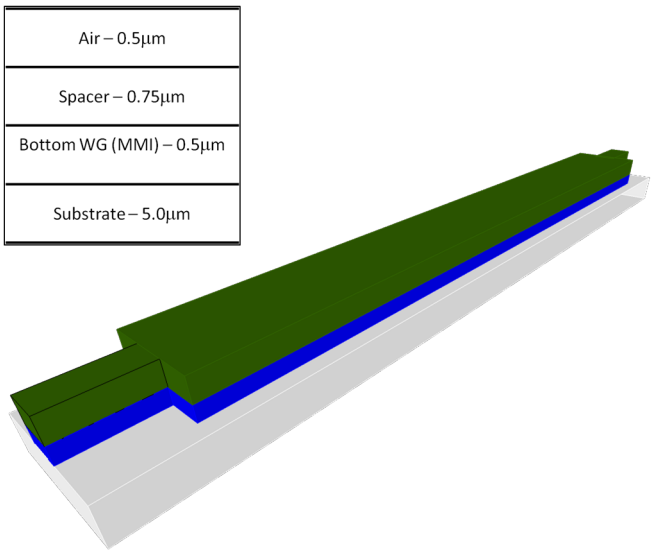
layer, two confinement layers vertically separated by an InP spacer layer are present. The coupling between the two layers is governed by the thickness of the spacer layer and since it is defined during the grown process, the variation in the actually grown layer as opposed to the designed one is expected to be less than ±2.5% which is significantly better than the variation expected in laterally coupled structures explored in Chapter 2, 3 and 4 where the coupling is defined by etching during fabrication. For the purpose of all the simulations, the bottom 3 InP layers including the waveguide cladding, the buffer and the substrate were considered to be a single layer. Similarly for the top layer, the top contact and micro-ring cladding layers were considered to be a single InP layer. This was done to improve the computational time associated with each simulation.

5.3 Tolerance Study

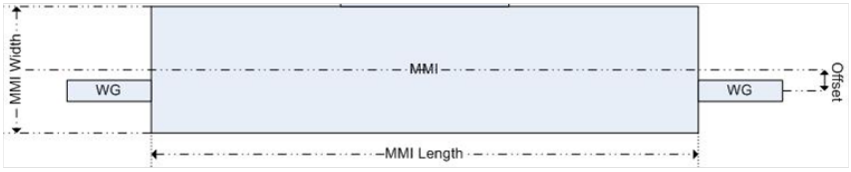
5.3.1 Restrictive Imaging in MMI

As discussed in Section 5.1.1, C. W. Tee *et al.*, [139] have shown that vertically coupling a multi-mode bus to a ring resonator improves the alignment tolerance of such devices. Keeping this in mind, an MMI is chosen as the component which is vertically coupled to the resonator. Furthermore, an MMI, as shown in Fig. 5.4a exhibiting what is coined as restrictive imaging is chosen. In such an MMI, the single mode input and output waveguides are offset by the same amount with respect to its centre as shown in the top view of the schematic in Fig. 5.4b. This is done in order to shift the point of imaging of the MMI to the opposite side with respect to the input-output waveguide offset and more towards one of its edges. By restricting the imaging point of the MMI to one of its edges, a dark region is formed on the other edge. This phenomenon allows the addition of a stub which is a mechanical platform on top of which the resonator is placed and this is utilised in the structures simulated in Section 5.3.2.

Fig. 5.4a shows a schematic of the MMI used in the simulations with the, substrate in grey, bottom confinement layer in blue, the spacer layer, acting as a top cladding of the MMI in this case in green and their thickness's listed in inset. All the 2D simulations were performed using optical propagation simulation tool, FimmPROP [119]. Fig. 5.4b highlights the different parameters characterising the MMI. The width of the MMI was fixed at 6μm with the offset of the input and output waveguides the main variable. The length of the MMI was fixed based on the offset used.



(a)

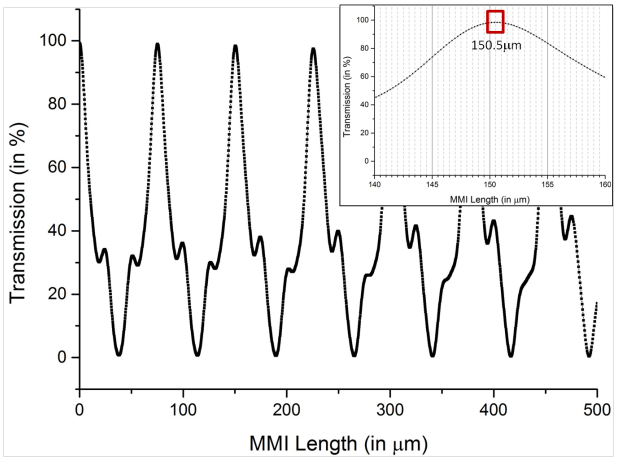


(b)

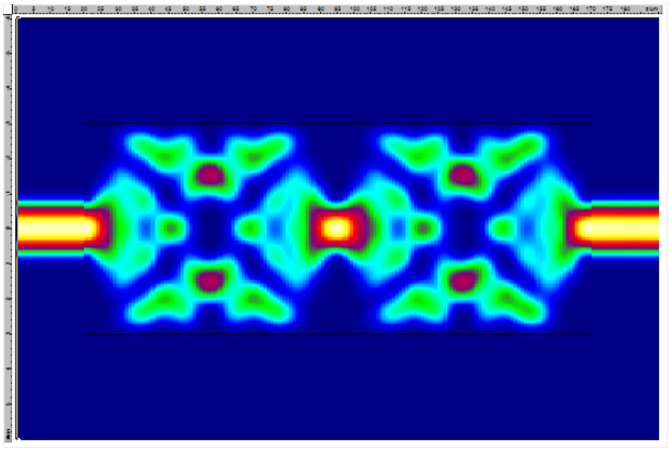
Figure 5.4: (a) 3D schematic of the MMI with the etch depth and layers simulated shown in inset. (b) Top view of the MMI.

The length of the MMI is scanned first while the input and output waveguides are set at zero offset. Fig. 5.5a shows a plot of the transmission from the input to the output as a function of the MMI length. The length was chosen to be double the minimum imaging length so as to ensure that the MMI images once at its centre and once at the output. Fig. 5.5b shows the field profile of the MMI, rotated clockwise by 90°, with the length optimised to be 150·5μm with a transmission of 98.42% power or a loss of 0.07dB.

In order to achieve restrictive imaging, the input and output waveguides have to be set at an offset with respect to the MMI. Fig. 5.6a, Fig. 5.6b, Fig. 5.6c and Fig. 5.6d show the initial results, where the length was scanned for a combination of offsets used and set at intervals of 0.5μm. Initial results seemed to suggest that the highest transmission is obtained for an offset



(a)



(b)

Figure 5.5: (a) Simulation showing the results of scanning the length of a 1×1 MMI. (b) Field profile of the MMI with the length optimised to cover two imaging points.

of 1.0μm and 3.0μm from the edge of the MMI or an offset of 1.0μm from the centre of the waveguide to the centre of the MMI, in either direction. Further simulations shown in Fig 5.6e using offsets set at smaller intervals of 0.1μm confirm that the aforementioned offset is the most suitable value to work with. Fig. 5.6f shows a field plot of the 1×1 MMI with optimised offset of the input and output waveguide. The length was optimised to be 201μm with a transmission of 97·61% power or a loss of 0.1dB. It can clearly be seen in the field plot that the MMI images towards one edge

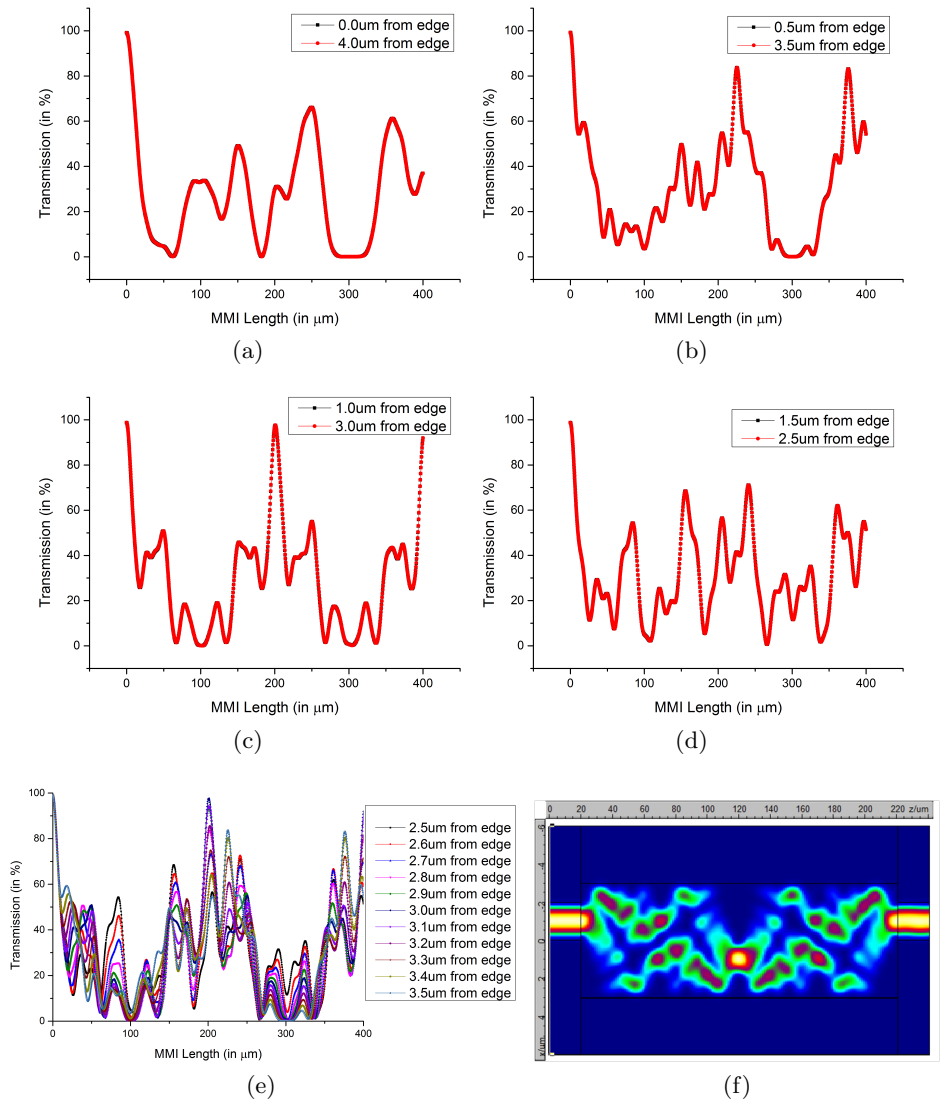


Figure 5.6: Simulation showing the results of scanning the length of a 1×1 MMI for different offset values of:(a) 0.0μm and 4.0μm from the edge (b) 0.5μm and 3.5μm from the edge (c) 1.0μm and 3.0μm from the edge (d) 1.5μm and 2.5μm from the edge (e) Simulation showing the results of scan with the offset set to smaller steps of 0.1μm. (f) Field profile of the MMI demonstrating a restrictive interference.

while a dark region is formed on the other edge. This is a direct artefact of the restrictive imaging induced in the MMI and is exploited in the single

side process concept.

5.3.2 Fabrication Tolerance

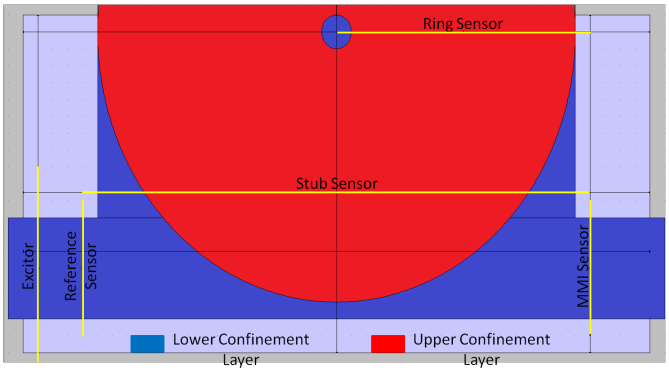


Figure 5.7: Schematic of the structure used for 3D FDTD simulations.

Fig. 5.7 shows a schematic of the top view of the structure used in the FDTD simulation. In order to limit the computational time of the simulation while maintaining a high degree of accuracy of the results, as compared to Fig. 5.2, only half of the structure is simulated. 3D FDTD simulations were carried out for this part of the analysis using OmniSim [141]. A part of the filed profile is exported from FimmProp and imported into OmniSim at the "Excitor"in Fig. 5.7. The main parameter that is noted here is the amount of light coupling into the ring at the "Ring Sensor" with reference to the "Reference Sensor" shown in Fig. 5.7. It is important to note here that during the fabrication of the actual device, the stub will be fabricated along with the MMI and hence, by fixing the width of the stub to be the same as the diameter of the ring, it can be ensured that the misalignment between the ring and the MMI, along its length is nominal. The power transmitted into the MMI is noted using the "MMI Sensor" while any leakage into the stub is monitored at the "Stub Sensor".

The ring resonator designed on the top waveguide is meant to operate in the whispering gallery regime. For this purpose, an initial study is done in Fig. 5.8 in which the width of a 16μm radius ring resonator is plotted as a function of the coupling coefficient. A variation in the coupling coefficient from 2.7% for a ring width of 5.3μm to 2.76% for a ring width of 16μm is observed.

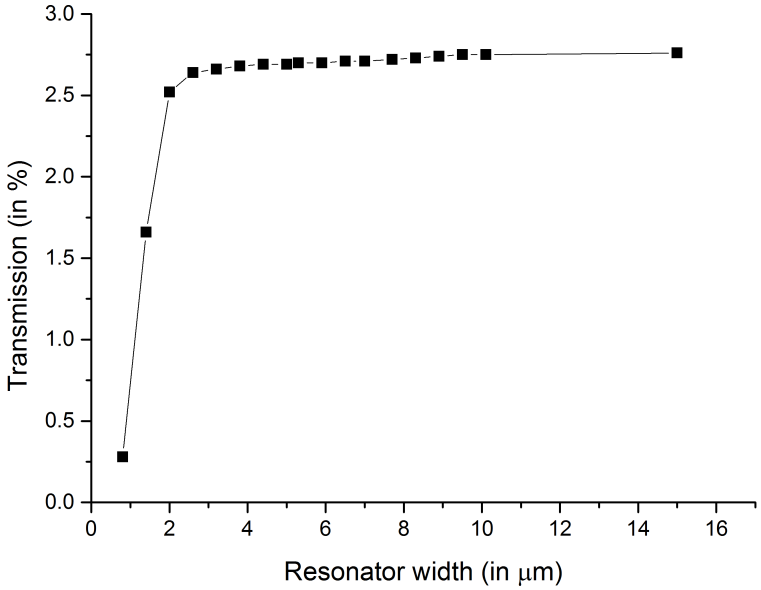


Figure 5.8: Simulation of the width of the ring resonator as a function of coupling coefficient.

For the purpose of the misalignment study, two ring resonators of 16μm and 8μm radius are studied separately. Since two 6μm MMIs are used and designed to have a minimum separation of 4μm between them, a minimum resonator diameter of 16μm is required which prompts the simulation of a minimum resonator radius of 8μm. Several conditions related to the misalignment of the ring with respect to the MMI across the width of the latter is simulated and the results are plotted in Fig. 5.9. The solid and open symbols are for the 16μm and 8μm radius ring resonators respectively with the square, circular and triangular symbols representing the transmitted power in the MMI, ring resonator and the stub respectively.

In a region between 0.4μm to 0.6μm, the coupling coefficient is varied by around 7%. This corresponds to a deviation of the coupling coefficient from the designed value is less than 7% for a $\pm$0.1μm lateral misalignment. Moreover, within this range, the power coupled into the stub is nominal and restricted to less than half of the power coupled into the ring resonator. Fig. 5.10 compares the results that we have for the 8μm design to the demonstrations by C. W. Tee *et al.*, by estimating the data points shown in [139]. The vertical axis in both cases has been normalised to

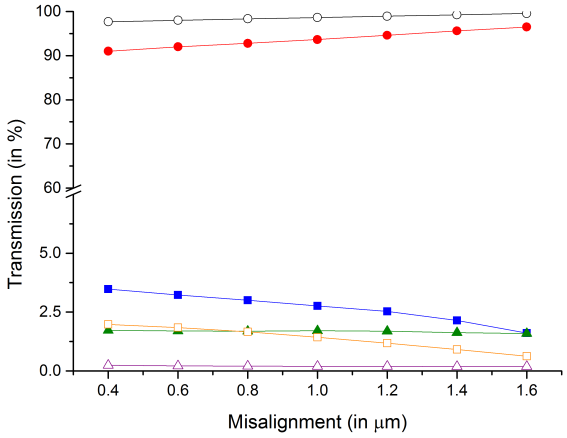


Figure 5.9: Effects on misalignment in the vertically coupled micro-ring structure. Solid and open symbols signify 16μm and 8μm radius ring resonators respectively while the square (□), circle (◯) and triangle (△) symbol represents the transmission in the ring, MMI and the stub respectively.

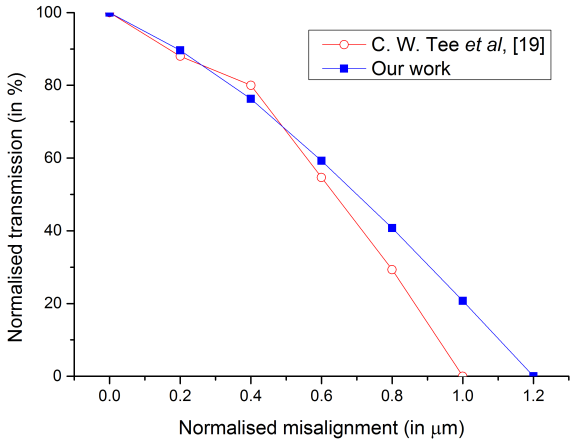


Figure 5.10: Simulation of the effects of misalignment along the width of the MMI as a function of the coupling coefficient. The solid blue symbols represent the work done in the context of the thesis and the red hollow symbols represent the work done previously by C. W. Tee *et al.*, in [139].

level the comparison between both so that their performance in terms of the change in coupling coefficient can be visualised. Similar performance is noted in either case implying that the proposed single wafer, side processed

design does not compromise the performance in anyway meaning the structure proposed here does not require any sort of wafer bonding and can be fabricated using standard techniques involving an easier processing [140].

5.3.3 Resilience to Growth Variations

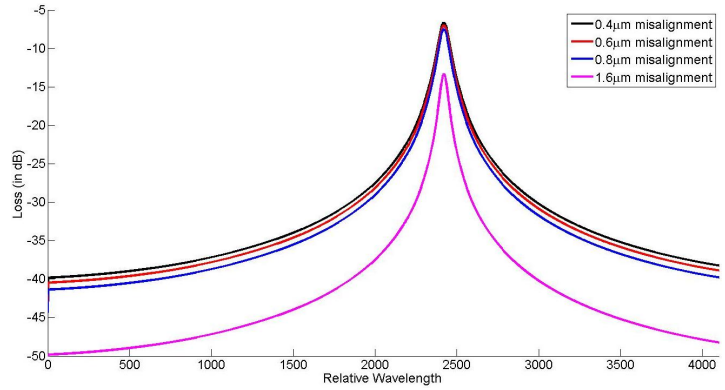
The definition of the separation of the waveguide and the ring resonator by the spacer layer implies that there is a greater control over the coupling coefficient. However, the grown layers are expected have a variation in thickness limited to ±2.5%. Hence, a study is performed in which each of the lower confinement, spacer and upper confinement layers are individually varied by ±2.5% and the change in coupling coefficient is noted. In Table 5.3, we list this variation in coupling coefficient. The coupling coefficient is found to be less sensitive to variations in the upper confinement or resonator layer and the lower confinement or MMI layer. However the variation is found to be most significant for deviation in spacer layer thickness. Nonetheless, the maximum variation in coupling coefficient is still restricted to 6.08%.

Table 5.3: Resilience to Grown Layer Thickness

Layer	Percentage variation in coupling coefficient (in %)
Upper Confinement (Resonator)	2.72
Spacer	6.08
Lower Confinement (MMI)	4.11

5.3.4 Device Spectra

Fig. 5.11 shows simulated plots for the vertically coupled ring resonator using the coupling coefficients under certain misalignment conditions which are obtained within the fabrication tolerant regime in Section 5.3.2. The simulations are based on Coupled Mode Theory and carried out using VPI-componenetmaker to get the spectral response of the device based on the coupling coefficient and the device dimensions. The effective index of the waveguides is kept as a constant. This is a valid assumption because in the situation where there is a lateral misalignment between the resonator and the MMI, the coupling coefficient changes nominally but the effective



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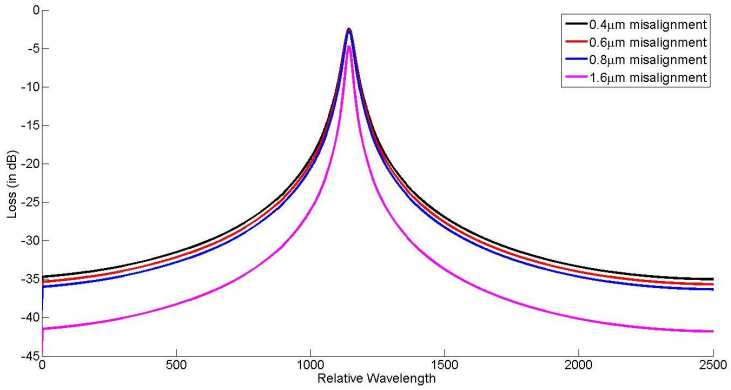

(b)

Figure 5.11: Simulated device spectra for the different values of coupling coefficients in the case of 0.4μm, 0.6μm, 0.8μm and 1.6μm misalignment using (a) 8μm resonator radius with a round-trip loss of 0.2dB and (b) 16μm resonator radius with a round trip loss of 0.1dB. The round-trip losses were based on the work done in [127].

index still remains the same. Round-trip losses of 0.1db and 0.2dB were added for the 16μm and 8μm resonators respectively and these loss values are based on the bending loss computed by Stabile *et al.* in [127]. The spectra for misalignments of 0.4μm and 0.6μm are seen to have a similar shape in terms of the roll-of of the passband and it is the primary feature which sets out the device design. For the sake of comparison, the spectra for 0.8μm and the extreme case of 1.6μm misalignment are also plotted in the same graph. In these regions however, the resonator is no longer in the tolerant regime and hence changes in the shape and finesse can be seen. A loss of 2.6dB and 7.0dB are observed for the 16μm and 8μm rings and

these originate from the round-trip loss that was used in the simulations. This leads to a more conclusive demonstration which further emphasises the fabrication tolerance which is achieved in this resonance based device design.

5.4 Summary

In this chapter, a fabrication tolerant vertically coupled micro-ring resonator design is proposed. The design relies on inducing restrictive imaging in an MMI located in a bottom waveguide layer coupled to a ring resonator operating in the whispering gallery regime, located in the top waveguide layer. Tolerance studies based on possible lateral misalignments suggest that for a $\pm$100nm misalignment, the coupling coefficient varies by $\leq$7%. Possible variation in thickness of grown layers are also taken into account and reveal that for expected deviations in grown layer thickness, the coupling coefficient is still restricted to a maximum of 6% of the designed value. Thus, a single sided monolithic approach to fabricated a vertically coupled micro-ring resonator is proposed and the performance of the device is not compromised in any way. The layer profile is based on previous active device demonstrations discussed in Section 5.1.1 which allows the prospect of these devices to be used as modulators in DWDM circuits.

Chapter 6

Conclusions

Summary: In this thesis, the possibility of using resonator based devices for large scale circuit applications has been explored. In the context of future network architectures such as the Corona [18], the study has been focused on the utilisation of these resonator based devices as broadband switch and modulators elements.

A part of the work has focused on using higher-order resonators to decouple the trade-off between pass bandwidth and on-off switch extinction as exhibited by single order resonators. This in turn is used as a mechanism to achieve large scale switch matrices. The SOI work has focused on using fifth-order resonators as switch elements in a crossbar matrix. The relaxed tolerance afforded by the broadband fifth-order design nullifies the effects of feature size variations within a single fabricated resonant element. The different arms of a single switch element are phase matched because of the implemented design tolerance, allowing a single parallel micro-heater to be used as a phase shifter for each switch element actuation. The function of the phase shifters in this case is to spectrally match the transfer of different switch elements with respect to each other and also to provide a mean for switch actuation. In the 8×4 circuit, 28 out of a possible 32 path combinations have been studied because the remaining 4 paths were found to be electrically disconnected. However, this is still the largest resonator based SOI switch circuit to date. Thermal crosstalk has also been studied and reveals no significant effects in the fabricated circuit. High line-rate experiments are carried out in accordance with the need of future networks. 10Gbps routing through each of the measured paths reveals a nominal power penalty with a maximum of 1.0dB for the path between input 5

and output 4 while 40Gbps routing through representative paths incurs comparable penalties as well. The micro-heater design limits the switching speed of these devices as the rise and fall times are found to be in the order of 17μs and 4μs respectively. However, recent demonstrations in which the micro-heaters are fabricated directly on top of the silicon layer [121–123] have shown a great deal of promise and can be utilised to achieve greater tuning efficiency as well as faster switching speeds. Simultaneous multi-path routing across combinations of two inputs to four outputs i.e. a total of eight paths have also been performed making it the largest scale demonstration of its kind.

The InP in-plane rings have focused on using third-order resonators on an active-passive platform, allowing the realisation of a higher complexity circuit as far as the functional components are concerned. The minimum possible waveguide separation that can be achieved using I-line lithography limits the bandwidth of this device. Phase errors within the different arms of a single third-order element, induced by feature size variations in the fabricated chip require the utilisation of individual phase shifters in each arm of a single resonant switch element. The phase shifters in turn are made by placing phase modulators on top of the directional couplers present in each arm of a resonant element. 4 paths of the fabricated 4×4 matrix circuit have been spectrally characterised making it the largest InP based matrix switch demonstrated to date. A proof-of concept routing at 10Gbps across two different paths reveal a maximum power penalty of 2.5dB.

Outlook: A comparison is drawn for both the InP and SOI based in-plane resonator circuits based on the experimental observations so as to evaluate their performance. Initial assessment is provided in Table 6.1 with further discussion done in terms of certain critical parameters which are key for their utilisation in future optical networks.

Table 6.1: Comparison of switch matrices fabricated in SOI and InP platform

Platform	Low loss	Large scale circuits	High bandwidth routing	Low power consumption	High component density	Phase tuning
SOI	✓	✓	✓	×	×	✓
InP	×	×	✓	✓	✓	✓

Loss and Scalability - The loss in a PIC is a crucial parameter which ultimately defines the scalability of the circuit. In this section the origins of the loss in both the circuits and the possibility of reducing them in the future in order to make higher port count PICs are discussed. The origin of the losses have been broadly classified into two categories viz.- fibre-to-chip coupling loss and on-chip loss.

Fibre-to-chip Coupling Loss - The fibre-to-chip coupling loss is mainly dependant on the coupling mechanism involved. The 1D surface grating couplers used in the SOI circuit have a coupling efficiency of about 30% [116] leading to a fibre-to-chip coupling loss of about 5-6dB. However, recent progress in surface grating coupler design has shown a considerable increase in the coupling efficiency resulting in lower coupling losses [142–144].

Fibre-to-chip coupling in the InP based third order resonator is achieved by using end facets obtained by cleaving waveguides with lensed fibres and it results in a coupling loss of 6dB per coupler. Majority of this loss arises from the mismatch in the spot-size of the light in the fibre and that in the waveguides. Spot-size converters have been used to enlarge the spot size at the end facets of the waveguides leading to a better match in the two and hence a considerable reduction in the coupling loss [145, 146].

Improvement of the fibre-to-chip coupling efficiency leading to a reduction of the coupling loss and hence the total loss in both cases provides the scope for scaling up such PICs.

On-chip Loss - In the SOI fifth-order resonator based switch matrix, on-chip losses of 2.0dB per on-state switch element and 0.9dB per off-state switch element are noted. The measured losses are quite low and have played a major role in enabling the measurement of the 28 paths across the 8×4 matrix. These losses partly arise from the 2.6dB/cm [116] waveguide losses which are a consequence of the material platform and the fabrication tools employed by the Foundry. A less significant part of the loss arises from the orthogonal waveguide crossings which are expected to be in the order of 0.1dB. Another factor influencing the on-chip losses is the size of each switch element. In a resonant device, output spectra is formed as a consequence of constructive interference between the light wave travelling through the resonator multiple number of times. As the circumference and hence the physical size of each resonator is reduced, the light wave

propagates through a shorter distance inside the waveguide and hence for a fixed value of waveguide loss, a lower on-state loss is achieved. However, a reduction in the the resonator circumference leads to an increase in the device FSR as well as a reduction in the phase modulator length and the latter has to be long enough to provide the required phase shift in each switch element.

An on-state loss of 24dB and an off-state loss 5dB limit the large scale application of the InP third-order resonator based switch matrix. A majority of the loss arises from components such as the 180°-bends and the tapers located at the deep to shallow etched waveguide interfaces and the rest arises from the inherent losses in the waveguides. A marked reduction of the losses incurred is expected for the Deep-UV (DUV) design and it is achieved as a direct consequence of fabricating smaller resonators. However, reducing these component losses is vital for improving the scalability of circuits using such switch elements as these losses are fixed irrespective of the size of the resonator and hence in this case, the on-chip losses do not scale linearly with a reduction in resonator circumference. The possible means of doing so are as follows:

- Designing a device consisting of only deep etched structures and thus negating the need for lossy waveguide tapers. The losses arising from the bends still remain in this case and the efficiency of the phase modulators in deep-etched waveguides is also a cause for concern.
- Designing new low loss components which fit the requirements as governed by the theoretical spectra.
- Designing and fabricating the circuit on high confinement waveguides in a membrane based iMOS platform.

Bandwidth and Extinction Ratio - The SOI work has revealed an extinction of 20dB across a 100GHz bandwidth across the fabricated circuit. The 100GHz bandwidth cannot be fully utilised using on-off keyed signals and a part of the bandwidth can be sacrificed in order to achieve an even higher extinction ratio as predicted in [48]. This can be achieved by etching away the SiO_2 layer between two neighbouring waveguides in a directional coupler in order to reduce the coupling coefficient to the actual designed values.

The 4 paths in the InP third-order resonator circuit have a bandwidth of 12.5GHz. This FSR and hence the bandwidth can be increased by making

more compact directional couplers and hence reducing the circumference of the couplers. A shift to DUV lithography is expected to aid this process. The minimum on-off signal extinction as measured at the output of the chip is found to be 15dB. This value however is limited by the noise of the output SOA and simulation suggests that it is in the order of 40dB for just a resonator switch element. A reduction in on-chip losses will further improve this overall extinction in the PIC as observed after the output SOA.

New components: Other than large scale switch matrices, next generation networks like the Corona architecture [18], require new component designs, principle among them being modulators and lasers. Apossible route to achieve this is proposed through the use of 3D vertically coupled MRR. This work has dealt with the design of a dual-plane resonator structure which can be fabricated using standard foundry processes (for example, using the JePPIX foundry) and is tolerant to feature size variations expected in a fabricated device. The schematic of the device has been shown in Fig. 5.2 in Chapter 5. The design rests on using an MMI as a part of the input bus waveguide located in the lower confinement layer. An offset is applied to the input and output waveguides of the MMI so as to shift the MMI image towards one of its sidewalls and a stub is placed on the opposite sidewall. The purpose of the stub is to aid in single side processing and providing a mechanical platform, resting on which, a ring resonator can be fabricated on the upper confinement layer. The light in the resonator is then coupled into the output bus via another MMI which is a mirror image of the first one. The design has been shown to be tolerant to fabrication variations in the order of $\pm$100nm as well as to thickness variations in the order of $\pm$2.5% from the designed value with the variation in the coupling coefficient limited to $\leq$ 7%. The discussed design concept of the 3D MRR and the related simulations were done for a purely passive structure in which the optical propagation was modelled. However, the layer profile used for the design in similar to previously demonstrated active 3D integrated structures such as modulators [66, 106, 136] and lasers [113, 115]. Hence, the scope to incorporate active elements in the proposed structure in order to give rise to modulators and lasers is conceivable.

Material platform and tooling: The major advantage of SOI is that the fabrication process is more mature and the waveguides are strongly

confined owing to the high effective index. Hence, more reproducible feature sizes can be fabricated and the high index contrast allows for smaller structures such as low bending radius waveguides and rings. Moreover, recent demonstrations have also lead to addition of phase modulators in SOI foundry [116] with the modulation efficiency being comparable to InP [117, 140]. However, direct band gap structures using InP quaternary layers allow for the incorporation of active medium in InP leading to on-chip lasers and gain medium in the form of SOAs [140]. Other than the choice of material platform, fabrication tools are of importance in realising PICs. High density, low loss structures are required to be ultra-compact in VLSI photonics. In order to achieve this, state-of-the-art DUV lithography is preferable as this allows the scope for reduced feature sizes which result in devices with low footprint with a higher degree of reproducibility.

Future of PICs: In this thesis, different resonator based PICs have been carried out based on device simulations and designs of the said circuits. Performance evaluation has been performed in terms of device spectral characteristics and routing high bandwidth data across multiple paths of the circuit which has shown promise for application as high bandwidth PICs for future networks.

However, certain advancements in the technology are still required for full scale implementations. PICs demand the use of multiple electrodes on a single chip leading to the possibility of multi-level wiring schemes and high density connectivity in such circuits. Use of CMOS-compatible processes such as through-silicon-vias make the possibility of such wiring schemes much easier in SOI than in InP. Moreover, a plausible route to achieve this in both platforms is through the use of flip-chip bonding. However, these issues have to be explored in a far greater detail in order to cope with the demands of PICs.

Temperature Independent Operation and Self-Calibration - The current circuits are wavelength dependant and hence, require their spectra to be manually aligned with respect to each other which is a tedious process and not suited for large scale network applications. Moreover, the very significant dependence of the device performance on temperature is another detrimental factor. Athermal and self-aligned circuits have been explored recently [147, 148] and further utilisation of similar schemes on larger scales is very essential to ensure uninterrupted performance of res-

onator circuits.

Polarisation Independence - High data rate routing schemes have been performed in this thesis at line rates of 10Gbps and 40Gbps. However, further increase in line rates may be performed by using advanced modulation formats. One such scheme involves doubling the effective line rate using polarisation multiplexing which requires a polarisation independent circuit design. A viable way of achieving this can be done by using polarisation divergent circuits using, for example, 2D surface grating couplers. An added advantage of polarisation diversity is that the same waveguide and component designs, as presented in this thesis can be used in the circuit in order to transmit data at twice the line rate. The disadvantage is that the circuit will cover double the area as the same circuit has to be replicated twice. Another possible way to achieve this is by using polarisation converters [149–151] which enables the usage of the same circuit design to achieve polarisation independent operation.

Discussion: In this thesis, PICs using resonators as key functional elements have been discussed. The fabricated switch matrix on SOI platform has provided a route for broad bandwidth and high signal extinction switches and the low losses achieved in these devices make it very suitable for large scale circuits. A combination of these factors have allowed for this demonstration to span across 28 of the possible 32 paths in the 8×4 switch matrix making it the largest resonator based switch circuit to date. However, the switching times are limited by the micro-heater phase shifters used and has led to the exploration of other material platforms. 4×4 switch matrix on InP has provided the opportunity for on-chip gain and potentially faster switching times. In the proof-of-concept demonstrations, multiple paths of the matrix have been tested making it the first of its kind. However, the high component losses limit the scalability of this circuit and hence the losses are analysed in terms of the components used.

A new design is then proposed using a combination of the conclusions of this analysis and the device circumference miniaturisation afforded by deep-UV lithography. A design for a vertically coupled resonator, capable of being fabricated using standard photo-lithographic means has also been explored. The simulations prove that a desirable degree of fabrication tolerance is achieved in this design without compromising its performance and these devices can potentially be used as modulators in future DWDM

circuits.

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Acronyms

Abbreviation	Description
APD	Avalanche Photodiode
AWG	Arrayed Waveguide Grating
BW	Bandwidth
BER	Bit Error Rate
BPF	Band-pass Filtre
CAN	cell access node
CW	Continuous wave input signal
DUV	Deep-UV
DWDM	Dense wavelength division multiplexing
EDFA	Erbium-doped Fibre Amplifier
ER	Extinction Ratio
ESA	Electrical Spectrum Analyser
EVM	error vector magnitude
FSR	Free Spectral Range
FWHM	Full-width at half-maximum
HCC	home communication controller
IF	intermediate frequency

IM	intensity modulator
MMI	Multi-mode Interferometers
mm-wave	millimeter-wave
MRR	Micro-ring Resonator
MZI	Mach-Zehnder interferometer
OFDM	orthogonal frequency-division multiplexing
OFM	optical frequency multiplying
OSA	Optical Spectrum Analyser
OSNR	optical signal-to-noise ratio
PC	polarization controller
PCB	Printed Circuit Board
PD	photo-detector
PIC	photonic integrated circuit
PRBS	Pseudo-random Bit Sequence
QAM	quadrature amplitude modulation
RF	radio frequency
RG	residential gateway
RoF	radio-over-fiber
SEM	Scanning Electron Microscope
SNR	signal-to-noise ratio
SOA	semiconductor optical amplifier
SOI	Silicon-on-Insulator
SSB	single-sideband
VOA	variable optical attenuator

VSA	vector signal analyser
VSG	vector signal generator
WDM	Wavelength division multiplexing

List of publications

Journals

1. P. DasMahapatra, R. Stabile, A. Rohit and K. A. Williams, "Optical crosspoint matrix using broadband resonant switches," *J. Sel. Topics Quantum Electron.*, vol. 20, no. 4, pp. 1-10, July-Aug. 2014.

2. P. DasMahapatra, R. Stabile, A. Rohit and K. A. Williams, "40Gb/s data routing through a scalable 2D matrix of higher order ring resonator switches," *Electron. Lett.*, vol. 49, no. 24, pp. 1545-1547, Nov. 2013.

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6. P. DasMahapatra, R. Stabile and K. A. Williams, "Third-order ring resonator based InP switch matrix," in *Proc. International Confer-*

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7. S. Zou, P. DasMahapatra, R. Stabile, K. A. Williams, E. Tangdiongga, and A. M. J. Koonen, "Dynamic routing of millimeter-wave signal for in-building networks using integrated resonant switch matrix," in *Proc. Optical Fiber Communications Conference and Exhibition (OFC)*, California, USA, Mar. 2014, Th1D.5.

8. P. DasMahapatra, R. Stabile and K. A. Williams, "Simultaneous Multi-path Routing in an 8x4 Optical Switch Matrix," in *Proc. International Conference on Fiber Optics and Photonics*, Kharagpur, India, Dec. 2014, M2C.4.

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Curriculum Vitae

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In November 2011, he started working towards the Ph.D degree under the supervision of Prof. Kevin A. Williams in the Electro-Optical Communications group (ECO) of COBRA research institute at Eindhoven University of Technology (TU/e), The Netherlands, where he conducted research work in the area of ring resonator based photonic integrated circuits. His PhD work has been performed as a part of the SmartLight project funded by The Dutch Technology Foundation (STW) which aims at developing the science and enhancing the technology for future generations of ultra-fast, low power and high connectivity photonics integrated circuits.