Physical-based analytical model of flexible a-IGZO TFTs accounting for both charge injection and transport

Physical-based Analytical Model of Flexible a-IGZO TFTs Accounting for Both Charge Injection and Transport

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Abstract

Here we show a new physical-based analytical model of a-IGZO TFTs. TFTs scaling from L=200 μm to L=15 μm and fabricated on plastic foil are accurately reproduced with a unique set of parameters. The model is used to design a zero-VGS inverter. It is a valuable tool for circuit design and technology characterization.

Introduction

Amorphous Indium-Gallium-Zinc-Oxide thin-film transistors (a-IGZO TFTs) are promising candidates for the next generation of flexible and large area electronics [1-3]. A-IGZO TFTs show high electron mobility (μ~10cm^2/Vs), simple, low-cost and room-temperature fabrication processes, optical transparency, good uniformity, satisfactory device lifetime, and large-area integration even on flexible substrates [1]. The technology development and the design of displays and circuits urgently demand accurate physical-based analytical models. State-of-art physical-based [4-7] and compact [8] models merely describe the channel transport and are only suitable for long channel a-IGZO TFTs. In high mobility and/or short channel a-IGZO TFTs the charge injection severely affects the transistor performance [9,10] and it must be taken into account.

Here we show a new physical-based analytical model of the drain current in a-IGZO TFTs. The model takes into account both the charge transport in the channel and the charge injection at the source contact. It accurately reproduces, with a unique set of parameters, the measurements of high-performance a-IGZO TFTs with channel lengths scaling from L=200 μm to L=15 μm fabricated in our flexible technology. The physical-based analytical model combined with the good stability and uniformity of the fabrication process allow us to disentangle and quantify the channel and contact contributions. The model provides a comprehensive physical picture of the a-IGZO TFTs, and it is a valuable tool for the technology characterization. The model has been eventually implemented in a circuit simulator and it has been used to simulate analog and digital a-IGZO circuits.

a-IGZO TFTs fabrication

Fig. 1 shows cross-section and the top-view optical image of the fabricated a-IGZO TFTs with staggered architecture.

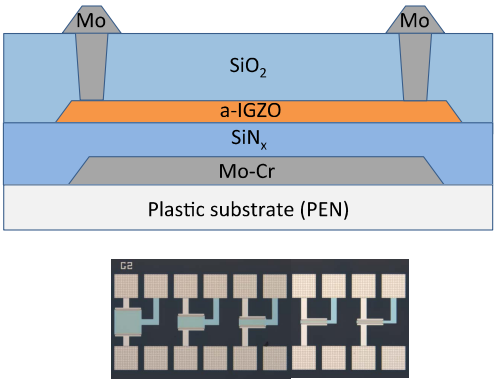

Fig. 1 – Top panel: Cross-section of the a-IGZO TFTs. Bottom panel: Optical image of the a-IGZO TFTs, W = 200 μm, L = [200, 100, 60, 20, 15] μm.

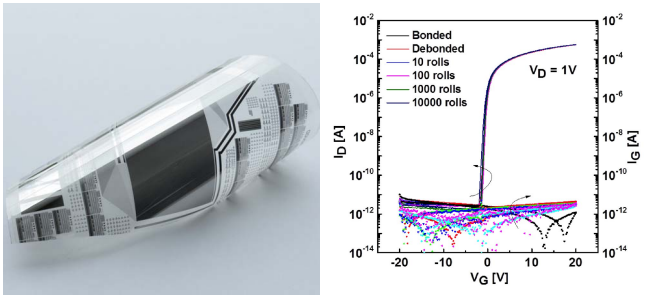

Fig. 2 – Left panel: Optical image of the a-IGZO TFTs and circuits fabricated on PEN foil. Right panel: Transfer characteristic of a-IGZO TFTs before and after deboding from the rigid carrier substrate, and as a function of rolls. Up to 10^5 rolls do not affect the a-IGZO TFTs.

A thin-film moisture barrier is deposited on top of the PEN film and a Mo-Cr gate metal is sputtered and patterned using photolithography. A 200 nm thick SiNx gate dielectric is formed by a 180 °C PECVD process. The 12 nm thick IGZO layer is deposited using direct-current sputtering. IGZO film thickness and O_2 flow in the sputter chamber were optimized in order to achieve good TFT performance at low temperature. A 100 nm thick SiO_2 ESL layer is grown using PECVD at 200 °C on top of the patterned semiconductor and it is patterned by dry etching process. The metal lines thickness is 100 nm and they are patterned using standard photolithography techniques. After TFT fabrication a post-anneal step under N_2 was performed in order to improve TFT stability and a 2 μm thick layer of a hard-baked photoresist was deposited as an interlayer on top of the semiconductor.

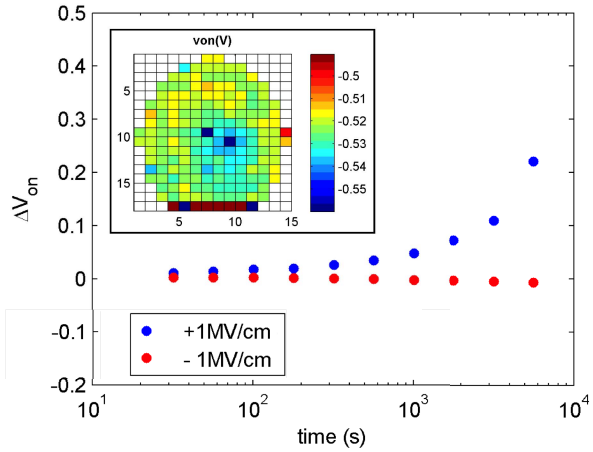

Fig. 3 – Device stability and uniformity. Main Panel. A constant gate bias stress of +1 MV/cm (-1 MV/cm) is applied for 10^4 s. The maximum ON voltage shift is +0.3 V (-0.03 V). Inset. Color map of the measured 216 a-IGZO TFTs.

The transistors and circuits fabricated in this large-area flexible technology are shown in Fig. 2, left. The plastic foil is glued to a rigid substrate and detached after the fabrication with no impact on the a-IGZO TFTs characteristics (Fig. 2, right). The fabricated TFTs show stable characteristics also if rolled up to 10^5 times.

a-IGZO TFTs uniformity and stability

The breakdown electric-field of the gate insulator is larger than 6 MV/cm and the leakage current is lower than 10^{-8} A/cm^2 at V_{GS} = 20 V. The measured gate capacitance per unit area is 22 nF/cm^2. Bias stress stability is very important for stable operation of flexible displays and circuits. A constant gate bias stress of +1 MV/cm (-1 MV/cm) is applied for 10^4 s. Fig. 3 shows that the maximum ON voltage shift (ΔV_{ON}) is lower than +0.3 V (-0.03 V), and the on-voltage variation across the wafer is below 5% (216 a-IGZO TFTs were measured).

a-IGZO TFTs analytical model

In a-IGZO the spherical symmetry of the bonds between the *s* orbital of metal cations reflects in a reduced density of localized (trap) states. Therefore, in a-IGZO TFTs the carrier concentration, and hence the drain current, depends on the interplay of trapped and free charges. In addition, the low density of trapped charges enables to easily push the Fermi energy level above the conduction band edge and at large V_G the degenerate conduction is reached. The a-IGZO conductivity is described by the multiple trapping and release transport theory combined with the band-percolation [4-7].

The drift-diffusion drain current integral [11,12] accounting for the charge transport in the a-IGZO reads

$$I_{DS} = \frac{W}{L}\int_{V_S}^{V_D}\int_0^{\varphi_s}\frac{q\mu_b n_b(\varphi,V_{ch})}{\sqrt{F_{xt}^2(\varphi,V_{ch})+F_{xb}^2(\varphi,V_{ch})}}d\varphi dV_{ch} \quad (1)$$

where W is the channel width, L is the channel length, V_S and V_D are the source and the drain voltages, respectively, V_{ch} is the channel potential (viz. pseudo Fermi potential), φ is the electrostatic potential, φ_s is the surface potential at the insulator-semiconductor interface, n_b is the free charge carrier concentration, $\mu_b = \mu_0 \exp\left[\frac{\phi_{b0}}{k_BT} + \frac{\sigma_b^2}{2k_B^2T^2}\right]$ is the band mobility μ_0 modulated by the percolation term [7], F_{xt} and F_{xb}, are the electric fields calculated accounting for the trapped and the free charges, respectively. The electric field depends on the charge concentration and it is expressed as

$$F_{xo} = \sqrt{\frac{2q}{\epsilon_s}\int_{V_{ch}}^{\varphi} n_o(\varphi', V_{ch})d\varphi'} \quad (2)$$

where $o \in \{b, t\}$, n_o is the charge concentration and ϵ_s is the a-IGZO permittivity. The free and the trapped charge carrier concentrations, respectively, read [13]:

$$n_b = N_b 2\sqrt{2} W_0\left[\exp\frac{\left(\frac{E_F-E_C}{k_BT}\right)}{2\sqrt{2}}\right] \quad (3)$$

$$n_t = N_t\theta_t\left(2\sqrt{2}\right)^{\frac{T}{T_t}} W_0\left[\exp\frac{\left(\frac{E_F-E_C}{k_BT}\right)}{2\sqrt{2}}\right]^{\frac{T}{T_t}} \quad (4)$$

where W_0 is the principal branch of the Lambert W function [7], N_b is the total number of delocalized (band) states, N_t is the total number of localized (trapped) states and T_t is the characteristic temperature of the localized states. It is worth noting that Eqs. (3) and (4) are valid for both the non-degenerate and degenerate conduction regime and hold for Fermi energy levels up to 0.15 eV above the conduction band edge. Eq. (1), accounting for Eqs. (2)-(4), can be solved only with numerical methods, because the denominator is given by the sum of Lambert functions. The overall charge carrier concentration $n_T = n_b + n_t$ can be approximated by the trapped charge concentration n_t when $E_F < E_c + 2k_BT$ and F_{xb} can be neglected in Eq. (1), while in the case $E_F > E_c + 2k_BT$ results $n_T \simeq n_b$ and F_{xt} can be neglected in Eq. (1). Since in a TFT the position of the Fermi energy depends on V_G, the drain current is dominated by the trapped charge when the transistor operates in the subthreshold and weak accumulation regions while I_D is dominated by the free charge when the transistor operates in the strong accumulation region.

These two limiting regimes as well as the transition between them can be described by means of the Matthiessen's model and the overall drain current can be written as

$$I_{DS} = \frac{I_{DS|F_{xb}=0} \times I_{DS|F_{xt}=0}}{I_{DS|F_{xb}=0} + I_{DS|F_{xt}=0}} \quad (5)$$

where $I_{DS|F_{xb}=0}$ is the drain current given by Eq. (1) with $F_{xb} = 0$ and $I_{DS|F_{xt}=0}$ is the drain current given by Eq. (1) with $F_{xt} = 0$.

Solving Eq. (5) and accounting for the leakage current flowing from the source to the drain contact when the transistor is in the off-state, the drain current results

$$I_{DS} = \frac{W}{L}\frac{\Gamma_t\Psi_t \times \Gamma_b\Psi_b}{\Gamma_t\Psi_{t+}\Gamma_b\Psi_b} + \frac{V_{DS}}{R_{OFF}} \quad (6)$$

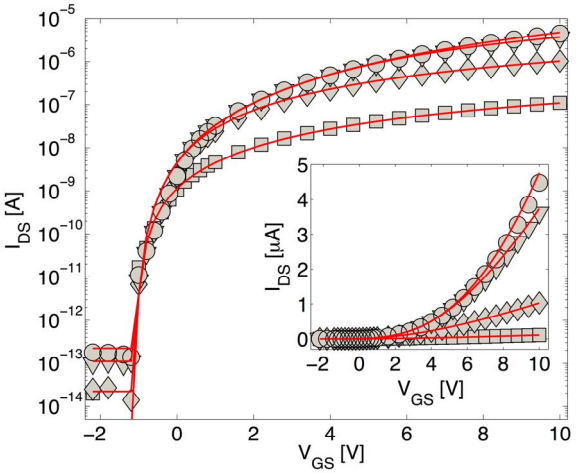

Fig. 4 – Measured (symbols) and modeled [Eq. (6), lines] transfer characteristics of L=200 μm a-IGZO TFT. The drain voltages are: 0.1 V (squares), 1 V (diamonds), 5 V (triangles), and 10 V (circles).

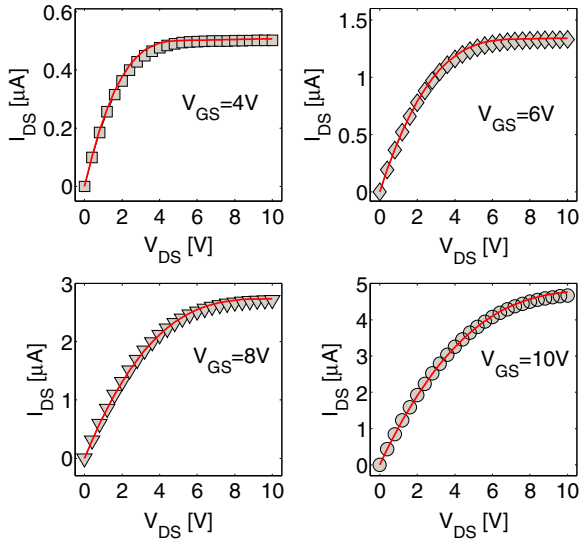

Fig. 5 – Measured (symbols) and modeled [Eq. (6), lines] output characteristics of L=200 μm a-IGZO TFT.

$$\Gamma_t = \frac{\epsilon_s \mu_b N_b}{C_i} k_B T \frac{T}{2T_t - T} \left[\frac{C_i^2}{2\epsilon_s N_t \theta_t k_B T_t}\right]^{\frac{T_t}{T}} \quad (7)$$

$$\Gamma_b = \frac{\mu_b C_i}{2} \quad (8)$$

$$\Psi_t = \left[\phi_{GS}^{\frac{2T_t}{T}} - \phi_{GD}^{\frac{2T_t}{T}}\right] \quad (9)$$

$$\Psi_b = [\phi_{GS}^2 - \phi_{GD}^2] \quad (10)$$

$$\phi_{GX} = V_G - V_{fb} - \varphi_{sX} \quad (11)$$

where V_G and V_{fb} are the gate and the flatband voltage, respectively, C_i is the gate capacitance per unit area, φ_{sX}, with $X \in \{S, D\}$ is the surface potential at the source or drain contact, calculated as in [7], and R_{OFF} is the source drain leakage resistance when the transistor is in the off-state.

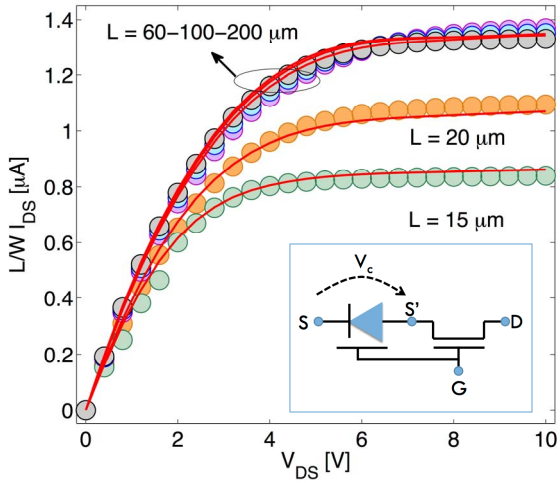

Fig. 6 – Main panel: Measured (symbols) and modeled [Eqs. (6), (12), lines] L/W normalized output characteristics of a-IGZO TFTs with various channel lengths. Inset. Schematic device model.

In Fig. 4 and Fig. 5 the channel model [Eq. (6)] is validated on the transfer and output characteristics of long channel (L=200 μm) a-IGZO TFTs, respectively. In both cases the model shows negligible error in a wide range of biasing conditions. Fig. 6 (symbols) shows the L/W normalized output characteristics varying the a-IGZO TFTs channel length. The normalized current is lower for short channel devices and this can be explained by the limited charge injection at the source contact [9,10]. The stability and uniformity of our a-IGZO TFTs together with the analytical channel model allowed us to accurately calculate the contact characteristics. The I_D-V_C of the shortest channel (L=15 μm) a-IGZO TFT is obtained by splitting the channel into a small contact region [14], where there is a voltage drop V_C, and the main channel, where the voltage drop is V_{DS} - V_C (Fig. 6, inset). Fig. 7 (symbols) shows the I_D-V_C for several gate voltages. We model the contact as a reverse biased Schottky-gated diode as proposed for staggered organic TFTs [15,16]. The contact model reads:

$$I_c = W \times I_0 \times \exp\left(\sqrt[4]{\frac{V_c}{V_0}}\right) \times \left[\exp\left(-\frac{qV_c}{\eta k_B T}\right) - 1\right] \quad (12)$$

$$I_0 = I_{00} \times \left\{\log\left[1 + \exp\left(\frac{V_G - V_{fb}}{V_{00}}\right)\right]\right\}^{\gamma} \quad (13)$$

where V_0 accounts for the Schottky barrier lowering effect, is the quality factor, and I_{00} is the reverse current prefactor. V_{00} = 1V and it is introduced to keep the dimensionality of the pre-factor I_{00}, and γ is a fitting parameter.

In Fig. 6 (full lines) the model (viz. channel and contact model), enables to describe the drain current of a-IGZO TFTs with L ranging from 15 μm to 200 μm. It is worth to note that the model describes a-IGZO TFTs with different channel lengths with the single set of parameters reported in Tab. 1. The model [Eqs. (6), (12)] has been implemented in a circuit simulator and used to design a unipolar zero-V_{GS} inverter, that is the basic building block of any analogue and digital circuits.

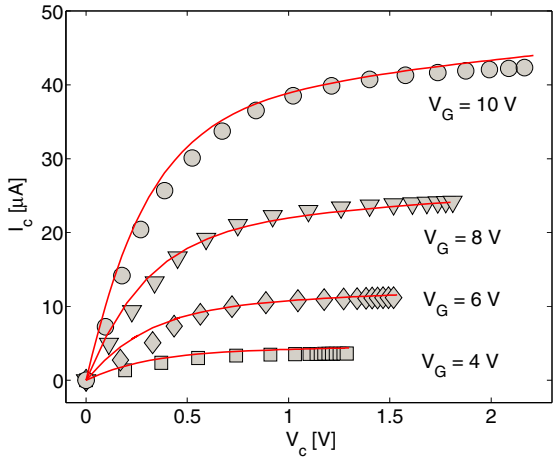

Fig. 7 - Measured (symbols) and modeled [Eq. (12), lines] contact characteristics of a-IGZO TFTs.

N_b [cm^{-3}]	5 x 10^{18}		R_{OFF} [Ω]	90 x 10^{12}
N_t [cm^{-3}]	1.5 x 10^{18}		I_{oo} [A/cm]	1.2 x 10^{-6}
T_t [K]	470		γ [.]	2.88
μ_b [cm^2/Vs]	9.8		V_0 [V]	20
V_{fb} [V]	-1.18		η [.]	10

Tab. 1 - Physical parameters of the model [Eqs. (6), (12)].

The comparison between the designed and measured inverter transfer characteristic is shown in Fig. 8. A good agreement between the simulation and the measurements is obtained thanks to the model accuracy and the process stability.

Conclusion

A physical-based analytical model of the drain current and charge concentrations in a-IGZO TFTs is proposed. The model is validated with the measurements of a-IGZO TFTs fabricated on flexible plastic substrate. We show that the a-IGZO TFTs scaling from L=200 μm to L=15 μm can be accurately reproduced with a single set of parameters. Both the charge transport in the channel and the charge injection at the source contact must be taken into account when L≤20 μm. The model is implemented in a circuit simulator and a zero-V_{GS} unipolar inverter is designed. The agreement between the simulations and measurements show that the model can be used for the design of flexible displays and circuits.

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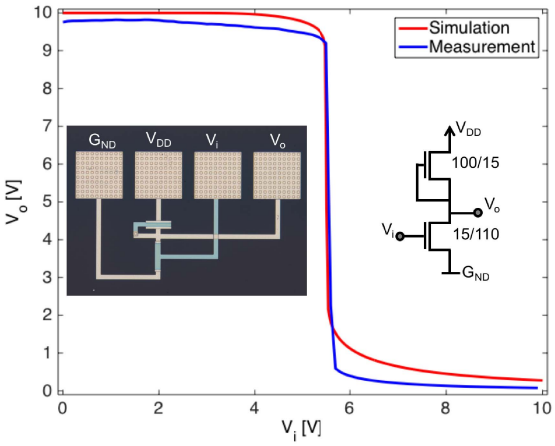

Fig. 8 - Comparison between the measured and simulated zero-VGS inverter characteristic. The a-IGZO TFT model is given by Eqs. (6), (12). The optical image is the fabricated and measured inverter.

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