Plasma-enhanced chemical vapor deposition of thick silicon nitride films with low stress on InP

Citation for published version (APA):
Shi, L., Steenbergen, C. A. M., Vreede, De, A. H., Smit, M. K., Scholtes, T. L. M., Groen, F. H., & Pedersen, J. W. (1996). Plasma-enhanced chemical vapor deposition of thick silicon nitride films with low stress on InP. *Journal of Vacuum Science and Technology A*, *14*(2), 471-473.

Document status and date:
Published: 01/01/1996

Document Version:
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

Link to publication

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy
If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

Download date: 08. Feb. 2024

This section is reserved for short submissions which contain important new results and are intended for accelerated publication.

Plasma-enhanced chemical vapor deposition of thick silicon nitride films with low stress on InP

L. Shi, C. A. M. Steenbergen, A. H. de Vreede, and M. K. Smit
Faculty of Electrical Engineering, Laboratory of Telecommunication and Remote Sensing Technology, Delft University of Technology, P.O. Box 5031, 2600GA Delft, The Netherlands

T. L. M. Scholtes and F. H. Groen
Department of Applied Physics, Optics Research Group, Delft University of Technology, P.O. Box 5046, 2600GA Delft, The Netherlands

J. W. Pedersen
Royal PTT Nederland N.V. PTT Research, P.O. Box 421, 2260AK Leidschendam, The Netherlands

(Received 24 April 1995; accepted 2 December 1995)

We have developed a low-temperature plasma-enhanced chemical vapor deposition process that facilitates the deposition of silicon nitride films with controlled stress by using periodically alternating high- and low-frequency power sources. Very thick films of 3 μm with low stress were deposited on InP substrates. Suitable sidewall profiles for metallization are obtained at 250 °C deposition temperature. A 3-μm-thick low-stress nitride film was successfully applied to reduce the capacitance of bond pad for an array of four InP based photodetectors, that were integrated with a four channel phased-array wavelength demultiplexer. The capacitance of the detectors was below 0.5 pF at −5 V bias. *© 1996 American Vacuum Society.*

I. INTRODUCTION

Plasma-enhanced chemical vapor deposition (PECVD) is a versatile thin film deposition technique for III–V semiconductor based devices.[1] Silicon nitride thin films deposited by this technique with a thickness up to a few hundred nanometers can be used for interlayer insulation, device passivation,[2] and as a masking layer for reactive ion etching (RIE).[3] For devices such as high-speed photodetectors on n^+ substrates, a thick dielectric layer with a suitable sidewall profile for metallization is needed between the substrate and bond pads in order to keep parasitic capacitances sufficiently low.

In this communication we describe a PECVD process operating at 250 °C, which facilitates the deposition of a silicon nitride film with controlled stress and a thickness up to 3 μm on InP. Low stress is a necessity for thick films, because a thick film with high stress is easily damaged during subsequent processing steps due to, e.g., adhesion failure. We have achieved substantial stress reduction by using periodically alternating high- and low-frequency power sources, which produce a tensile and a compressive film stress, respectively. Compared to the low-stress technique based on film annealing,[4] our low-stress technique avoids the necessity to anneal the film at a high temperature, which can damage the InP chip. The wet chemical etching behavior of the low-stress film, which is important for the sidewall profile, is shown as a function of the deposition temperature.

II. EXPERIMENT

The PECVD apparatus used for this work is a capacitively coupled planar parallel electrode system (Surface Technology Systems, Ltd.). The electrode diameter was 24 cm. The system was equipped with a mixed frequency upgrade consisting of two power sources of 13.65 MHz [low frequency

TABLE I. Deposition conditions and film properties of single-frequency deposited films.

Power source (W)	Substrate temperature (°C)	Pressure (mTorr)	Gas flow (sccm)	Refractive index	Deposition rate (nm/min)	Etching rate in BHF (nm/min)	Film stress (GPa)
LF 380 kHz (400)	250	750	SiH_4 73 NH_3 122 N_2 1000	1.985	250	40–60	0.45, compress.
HF 13.65 MHz (17)	250	900	SiH_4 30 NH_3 50 N_2 1960	1.980	12	40–60	0.36, tensile

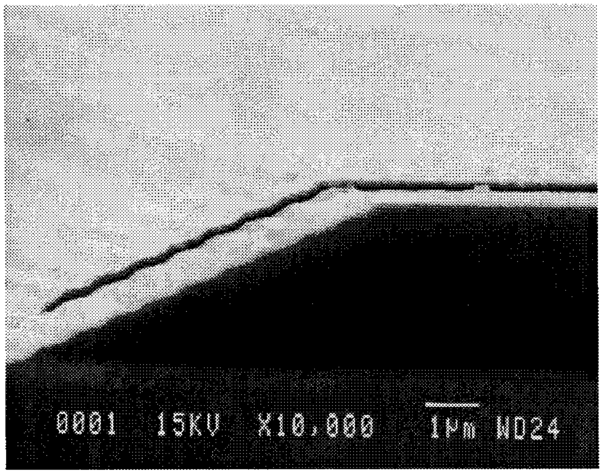

FIG. 1. Wet chemically etched sidewall profile (cleaved cross section) of a 3-μm-thick low-stress Si–N film deposited at 250 °C covered with a 200-nm-thin metal layer.

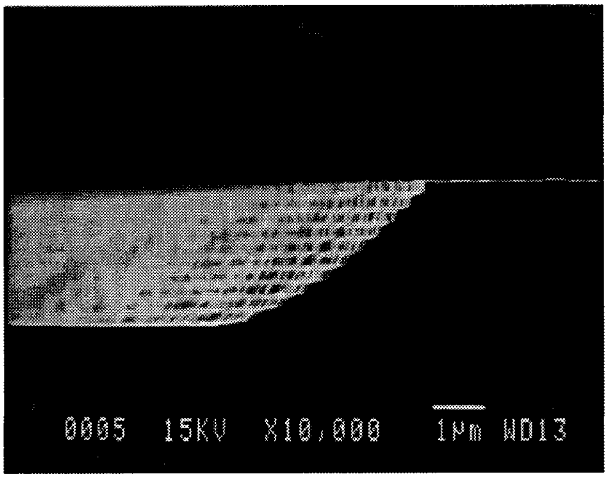

FIG. 3. Wet chemically etched sidewall profile of a 3-μm-thick low-stress Si–N film deposited at 200 °C.

(LF)] and 380 kHz [high frequency (HF)] respectively. This option enables periodic switching between the HF and the LF power sources. The time durations that the HF or LF power source is "on" can be adjusted separately through the process control computer. The film stress was measured by depositing onto a 95-μm-thick silicon substrate and determining the change in substrate curvature. The refractive index and the thickness of the film were measured with an ellipsometer operating at 633 nm. The thickness was also measured using an alpha-step profiler. The films were etched using BHF (ammonium fluoride, AF, 87.5–12.5) at room temperature. The deposition conditions and film properties of single-frequency deposited films are summarized in Table I.

It should be noted that the films deposited using the LF and HF processes have stress values with opposite signs. This suggests that nitride films with a low residual stress can be deposited by periodically alternating LF and HF depositions with an optimized layer thickness ratio.

A series of films were deposited, each consisting of a stack of LF/HF deposited layers with different LF/HF time ratios. The residual stress values of the films were measured. It was found that the residual film stress approaches zero when the LF/HF film thickness ratio is 0.8. This corresponds with the stress values listed in Table I.

III. RESULTS AND DISCUSSION

Using this time ratio and the process parameters given in Table I, films of several micrometers thick were deposited on InP substrates. A typical thick film of about 3 μm consists of ten LF/HF sequences of 135 nm/170 nm (32 s/15 min) each. The residual stress was measured to be about 0.015 GPa, which is a reduction by a factor of 30 compared with a single-frequency deposited layer. The total deposition time was about 200 min, including the time needed to reach the specified gas flows during each switching between the LF and HF processes.

Figure 1 is a scanning electron microscope (SEM) image showing the sidewall profile of a nitride film deposited

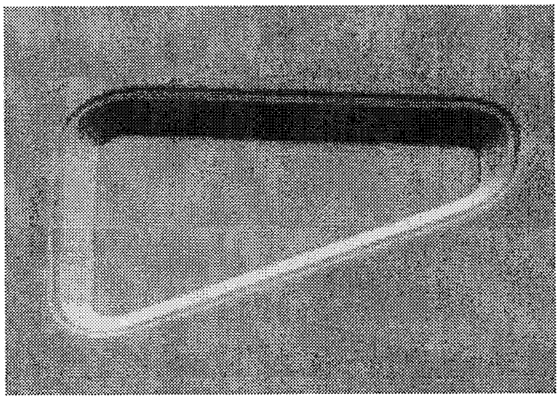

FIG. 2. A via hole wet chemically etched in the film shown in Fig. 1.

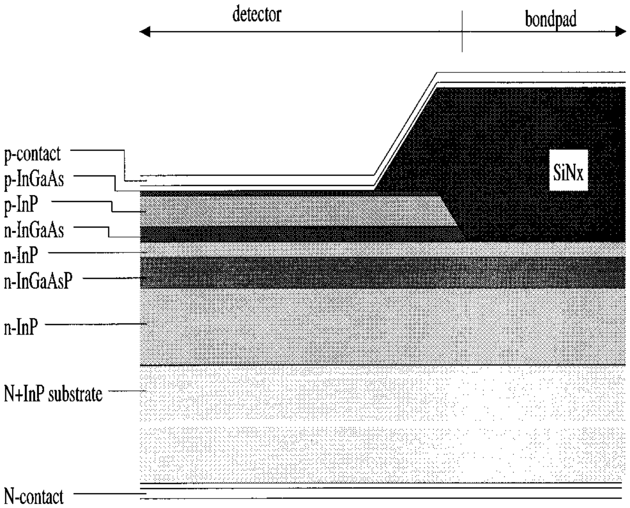

FIG. 4. Configuration of the photodetectors in which a 3-μm-thick low-stress Si–N film was used as a dielectric layer between the p metal contact bond pad and the n^+ substrate.

at 250 °C. The structure was obtained by photoresist masking and wet chemical etching (BHF). The etching time was 90 min. The wall has a slope of about 30° relative to the substrate. Figure 1 also shows the coverage of the wall by a thin metal layer of 200 nm (Ti/Au), which was deposited by means of high-vacuum electron-gun evaporation and partly etched wet chemically. Figure 2 shows a via hole structure etched in such a film. Figure 3 displays the sidewall profile of low-stress nitride film deposited at 200 °C. The corresponding etching time was 40 min. The sidewall profile shows a clear steplike structure. This is probably caused by a large difference in etching rates of the LF and HF layers deposited at this low temperature. The obtained slope is about 40°.

High-speed integrated photodetectors as shown in Fig. 4 were successfully fabricated. A low-stress 3 μm nitride film deposited at 250 °C was used as a dielectric insulation layer between the n^+ substrate and the bonding pads. The detectors, with a capacitance below 0.5 pF at -5 V bias, were integrated with a four channel phased-array wavelength demultiplexer with flat responses. The details of this device are published elsewhere.[5]

IV. CONCLUSIONS

Low-stress PECVD silicon nitride films with a thickness of several micrometers were fabricated and successfully applied as a dielectric layer for high-speed InP based photodetectors with a capacitance below 0.5 pF at -5 V bias.

ACKNOWLEDGMENTS

J. W. M. van Uffelen is acknowledged for his contributions. This work was partly supported by PTT Research and the I.O.P. (Innovative Research Program) of Nederlandse Ministrie van Economische Zaken.

[1] A. Piccirillo and A. L. Gobbi, J. Electrochem. Soc. **137**, 3910 (1990).
[2] R.-T. Huang and D. Renner, IEEE Photon. Technol. Lett. **3**, 934 (1991).
[3] G. H. B. Thompson *et al.*, in Proceedings of the European Conference on Integrated Optics, edited by P. Roth, Neuchâtel, Switzerland, April 1993 (unpublished), pp. 2–12.
[4] P. Ambrée *et al.*, J. Vac. Sci. Technol. B **11**, 614 (1993).
[5] C. A. M. Steenbergen *et al.*, in Proceedings of the 7th European Conference on Integrated Optics, edited by L. Shi *et al.*, Delft, The Netherlands, 3–6 April 1995 (unpublished), pp. 271–274.