

## InP-based photonic ICs

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# InP-based Photonic ICs

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#### Abstract.

Generic InP-based foundry processes lead to a large reduction in entry costs and bring photonic ICs within reach for many SMEs and larger companies.

#### INTRODUCTION

The generic foundry approach will cause a revolution in micro and nanophotonics, just as it did in microelectronics thirty years ago. Generic integration causes a dramatic reduction in the entry costs for applying Photonic ICs in novel or improved products and brings them within reach for many SMEs and larger companies. So far, most applications have been in the field of telecommunications and datacommunications, but presently they are becoming much broader: examples are fibre sensor readout units, gas sensors, medical diagnostics and metrology.

#### GENERIC FOUNDRY APPROACH

In Europe, three integration technology platforms are active in introducing the generic foundry concept for the major integration technologies in Photonics: JePPIX for InP-based monolithic integration, ePIXfab for silicon photonics, and TriPleX for low-loss dielectric waveguide technology.

In the JePPIX platform Europe's key players in the field of InP-based photonic integration technology are cooperating on the development of a generic foundry model using generic integration processes: highly standardized integration processes that can be used for a broad range of different applications. Presently a number of large R&D projects are running, developing both the generic foundry technologies, and the infrastructure to make them accessible at low cost for a broad range of companies: design tools, component libraries, generic packaging technology and generic test equipment. This model will reduce the entry costs for companies that want to apply Photonic ICs in their products by more than an order of magnitude.

#### MULTI-PROJECT WAFER RUNS

Multi-Project Wafer Runs are a key concept in the generic foundry model. In an MPW run a number of different designs are combined on a single wafer, so that the costs of the wafer run can be shared by a number of different designs. This becomes possible once different chips can be fabricated in the same standardized integration process. Through Multi-Project Wafer Runs the entry costs for developing a Photonic ICs are strongly reduced because a chip designer can use a well developed high performance process, which he does not have to develop himself, and for his designs he can buy some wafer area in an MPW run, which will provide him with a number of his chips without having to pay for the whole run. Further, he can use a dedicated design kit, including component libraries which will bring him a better design in a strongly reduced design time. Altogether, this will bring the costs of an experimental chip set down from hundreds of thousand Euros to something in the order of magnitude. It will bring Photonic ICs (PICs) within reach for many SMEs and larger companies for which the entry costs of today's technology are too high.

#### STATUS AND PROSPECTS

In 2012 the first experimental industrial foundry runs in InP-based technology were executed, with more than 30 chip designs for a variety of applications. The figure on the next page illustrates a few of the Application-Specific Photonic ICs (ASPICs) that have been designed and fabricated. Interest in participation is large. For 2013 we expect the first beta-runs with semi-commercial access for the technology that has been trialled in the EU-FP7 project EuroPIC, these are runs with small scale commercial access to processes that are not yet completely qualified. Dependent on the results, general commercial access can be expected in 2014 or 2015.

In the presentation the present status and prospects of InP-based Photonic foundry technology will be reviewed.

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Examples of Application-Specific Photonic ICs (ASPICs) fabricated in InP-based generic foundry runs