A class of robust switched-mode power amplifiers with highly linear transfer characteristics : on the elimination of zero-crossing distortion in switching converters

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On the elimination of zero-crossing distortion in switching converters

PROEFSCHRIFT

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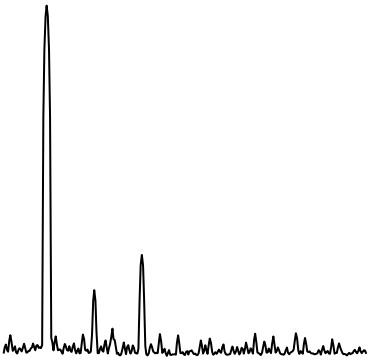

Jan Schellekens

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Summary

A class of robust switched-mode power amplifiers with highly linear transfer characteristics

On the elimination of zero-crossing distortion in switching converters

When looking at the trends of the technology road map in the semiconductor industry, it can be recognized that the high-power switching amplifiers used in lithographic equipment are rapidly becoming a limiting factor. In order to satisfy the requirements for the next decade, the generated noise and other disturbances are required to decrease by at least one order of magnitude. A further complicating factor is that due to the increasing complexity the number of amplifiers in such systems is growing. As a result, the reliability of power amplifier systems should also improve. Similar trends are visible in medical imaging, where improved accuracy is needed for higher resolution images, and in high-power studio-quality audio amplification, where high efficiency switched-mode power amplifiers have to compete with less efficient linear amplifiers that do not suffer from distortion due to switched-mode operation.

Switched-mode amplifiers process electrical power efficiently by controlling the energy flow between intermediate storage components. Modern switched-mode amplifiers are mostly based on the conventional switching leg, which, in turn, consists of two stacked semiconductor switches that are operated complementarily. Several sources of distortion can be attributed to the pulse-width-modulated switching leg, the most significant being blanking time. This blanking time, also referred to as dead time, is essential to avoid fatal cross conduction and results in a current-dependent voltage error, typically several percent of the input power supply voltage.

Extensive studies can be found in the literature on blanking time in pulse-width-modulated (PWM) converters, aiming at elimination, minimization, and compensation of its effects. The proposed techniques achieve mitigation of the problem but are not capable of completely eliminating it. Alternative topologies have been proposed that do not suffer from blanking-time effects. However, the proposed solutions have either a nonlinear relation between input and output, or are not robust for shoot-through currents.

The conventional switching leg can be transformed to a topology that does not suffer from distortion due to blanking time, is robust for shoot-through current, and has a linear relation between input and output. This topology is based on parallel-complementary unidirectional switching legs, and is known as the dual-buck (DB) converter. The DB exhibits a linear relation between input and output only for continuous inductor currents, which is accomplished with a bias current.

Compared to a conventional switching leg the DB requires additional inductive components, potentially resulting in a larger volume. The combination of interleaved voltages and coupled inductors is investigated, aiming to integrate the functionality of the filter and bias current inductor in a single magnetic device, with reduced total volume. It is shown that using coupled inductors with non-interleaved voltages results in a significant reduction of the inductor volume. However, the power density of the DB remains slightly lower than that of its conventional equivalent.

The DB topology does not suffer from blanking-time-related effects. However, other sources of distortion also affect switched-mode amplifiers. The impact of semiconductor switch and diode parameters on the output quality of the DB is investigated. It is shown that the forward voltages of the diodes and switches have no effect on the output quality.

The switching nature of power amplifiers comes with a substantial amount of distortion and electromagnetic interference. The effect of the modulation strategy on the output voltage quality under open-loop conditions, including the effect of the bias voltage, is investigated. It is shown that by selecting the appropriate interleaving strategy it is possible to achieve 3-level switching waveforms with doubled output ripple frequency, and a constant common-mode voltage at the output of the converter. This reduces distortion and results in reduced electromagnetic interference.

A linear state-space model is deduced which accurately captures the switching-cycle averaged dynamic behavior of the DB converter. Two different output current feedback control strategies are proposed. The first strategy applies decoupled single-input single-output control of output and bias current. The second

approach is based on full state-feedback with dynamics chosen such that a constant group delay is obtained over a wide frequency range.

A prototype of the selected topology with its proposed control has been realized in order to validate the methods described in this thesis. The effectiveness of the converter system is verified by experiments. Compared to conventional switching amplifiers, more than 40 dB improvement of the open-loop spurious-free dynamic range has been demonstrated. The experiments identify the DB topology as a valuable candidate for the next generation of power-amplifiers for applications that require high-quality output.

Contents

Chapter 1

Introduction

"A whole is that which has beginning, middle, and end."

(Aristotle)

An electronic amplifier is a device for increasing the amplitude of electrical signals. However, the term amplifier appears also in many other disciplines, such as optical amplifiers to amplify laser light, or torque amplifiers to amplify the torque of a rotating shaft without affecting its rotational speed. All amplifiers share the fact that the output is generated by modulating an external source of energy. In case of an optical amplifier the external source of energy can be a pump laser, in case of a torque amplifier an internal combustion engine. For electronic amplifiers the external power source is commonly a DC power supply.

The information-carrying quantities of electronic amplifiers can be voltage, current, or power. However, the same quantities can also be dependent quantities. That is, for a given load circuit, when the output quantity of the amplifier is voltage, the current and power depend on the load circuit, and are, thus, dependent quantities. Figure 1.1 shows a schematic representation of an amplifier circuit where the amplifier is indicated with a triangle. The external source, designated supply, is indicated with a circle.

In analog circuit theory the type of an amplifier is defined by its transmittance A, which is its input-to-output relation. Nine types of transmittance can be classified for the output quantities, i.e. voltage, current, and power [75, page 4]. The most commonly used are voltage gain ($u_{\text{out}}/u_{\text{in}}$), current gain ($i_{\text{out}}/i_{\text{in}}$), transimpedance ($u_{\text{out}}/i_{\text{in}}$), and transadmittance ($i_{\text{out}}/u_{\text{in}}$). Power can also be used as an input or output quantity but is considered a dependent quantity in the remainder of this section.

Other important design aspects are input impedance ($u_{\text{in}}/i_{\text{in}}$), output impedance ($u_{\text{out}}/i_{\text{out}}$), linearity, gain- and phase-error as a function of frequency, bandwidth, offset, spurious signals, and noise. The loading of the driving circuit is determined by the input impedance of the amplifier. This can cause undesired distortion of the input quantity that propagates to the output. Similarly, the output impedance determines the effect of the loading of the amplifier on its output, and can also be a source of distortion. An electronic amplifier ideally has a linear relation between input and output. Any nonlinear behavior causes undesired harmonics at the output[1]. Gain error, phase error, and offset result in deviation from the intended output but do not cause harmonic distortion. The combination of spurious signals and noise, which is often random in nature, is the remaining unwanted power that is transferred to the load.

The term power amplifier is often associated with the last circuit in a signal chain (the end-stage). This stage transfers the actual power to the load, thus making

[1]Some amplifier types are made deliberately nonlinear, such as frequency multipliers which amplify a specific harmonic of the input quantity.

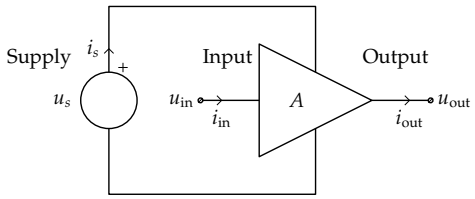


Figure 1.1: Schematic diagram of an amplifier with transmittance A and its external energy source (Supply). The electrical quantities are indicated, where u represents voltage and i represents current.

losses and efficiency, especially for this stage, important additional design requirements [75, chapter 1].

Power amplifiers have found their way in many daily applications, to drive loudspeakers in audio systems, to drive the electric machines in electrically propelled vehicles, and in electric power-steering systems. But they are also used in industrial servo systems, radio transmitters, medical imaging systems, and many other applications.

1.1 A brief history of power amplification

Power amplifiers can be grouped into two distinct kinds: linear power amplifiers, and switched-mode power amplifiers (SMPAs). Figure 1.2a depicts a schematic diagram of a linear power amplifier with a symmetrical voltage source as external power supply, and a push-pull configuration as output stage. The output quantity is generated by modulating the variable resistances (T_1 & T_2) based on the input quantity. There are many realizations of this basic concept. The most common are known as amplifier classes A, B, AB, and C, and are detailed in many works [99].

Switched mode power amplifiers generate the output quantity by switching between two or more voltage or current levels. Figure 1.2b depicts a schematic diagram of an SMPA which switches between the two voltage levels of the symmetrical external power supply. The switching, or gating, signals are generated by the modulator (M) based on the input quantity. A low-pass demodulation filter is required to recover the desired output quantity from the modulated supply. There are many kinds of SMPAs, most of which are based on a switching leg, i.e. two complementary operated switches, as depicted in Figure 1.2b.

In both linear and switched-mode amplifiers, the devices that are used to mod-

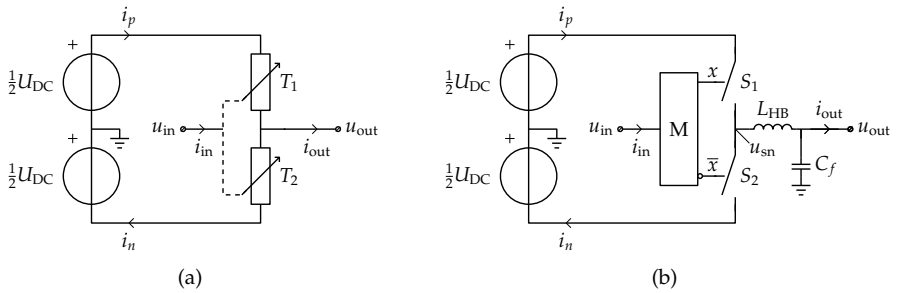


Figure 1.2: Schematic diagram of (a) a voltage-source linear power amplifier, and (b) a voltage-source switched-mode power amplifier with output filter.

ulate the external power supply changed over time from vacuum tubes to modern semiconductor transistors such as bipolar junction transistors, metal-oxide semiconductor field-effect transistors, and insulated-gate bipolar-transistors. Depending on how they are used these devices basically behave as controlled current sources, resistances, or switches.

Figure 1.3 shows the waveforms of the linear and switched-mode amplifier depicted in Figure 1.2, for $U_{DC} = 100\,V$, a resistive load of $8\,\Omega$, and the output modulated to 80 % of the maximum voltage range. In the linear case, as shown in Figures 1.2a and 1.3a, the positive half of the output current waveform is supplied through controlled resistance T_1, and the bottom half is supplied through T_2. This is commonly referred to as a push-pull amplifier stage. In this example, an additional current is flowing through both T_1 and T_2, as can be seen from the current waveforms in the bottom graph of Figure 1.3a. This constant current is commonly referred to as bias current, and is sometimes added to improve the zero-crossing behavior in linear push-pull amplifier stages.

The push-pull configuration, as depicted in Figure 1.2a, is often used in linear power amplifiers, and is referred to as class B, or class AB when used without or with bias current, respectively. The instantaneous power dissipation of linear amplifiers is determined by the current flowing through the controlled resistances times the voltage across them. In case of a class B amplifier the efficiency can reach a theoretical maximum of $\pi/4$ (78.5 %), for a resistive load, and sinusoidal output voltage with maximum amplitude. However, the efficiency becomes even less for smaller output voltages and when a bias current is flowing.

Figure 1.3b depicts the voltage and current waveforms of the SMPA from Figure 1.2b. The switches (S_1 & S_2) are conducting complementarily at a constant frequency, and the output voltage is determined by the relative on-time of the switches. The switch-node voltage u_{sn} is thus pulse-width-modulated (PWM).

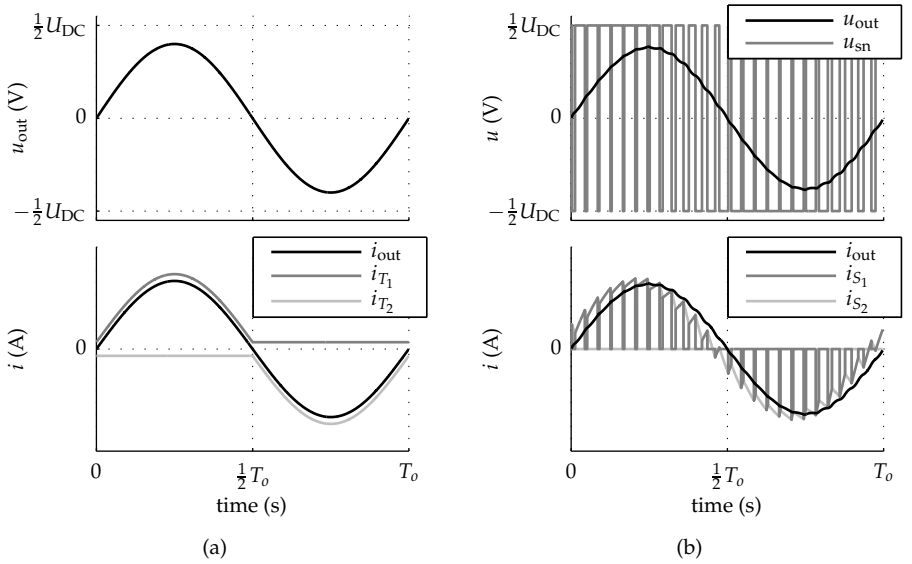


Figure 1.3: Voltage and current waveforms of (a) a voltage-source linear power amplifier, and (b) a voltage-source SMPA, as illustrated in Figure 1.2.

Many other fixed and variable frequency modulation techniques exist for SMPAs, all of which share the characteristic that the output is generated by switching between different voltage or current levels. In all cases filtering is required to recover the output quantity from the switched voltage or current. However, the undesired switching harmonics are not removed completely by the filter and appear attenuated at the output. This is a disadvantage of SMPAs compared to their linear counterparts. After filtering the distortion due to switching is usually small and is barely visible on u_{out} and i_{out} in Figure 1.3b.

A switched-mode power amplifier theoretically has 100 % efficiency when considering lossless switches and lossless passive components. The advances in semiconductor switches achieved over the past decades have resulted in significantly better efficiencies and power densities of SMPAs. Recently, in renewable energy applications, switched-mode converter efficiencies up to 98 %, and higher, have been reported in literature [51, 124]. As a result of this trend high-power amplifiers are almost always switched mode. One reason is that the cost of ownership of linear amplifiers, for the same power rating, is higher than for SMPAs. Linear amplifiers are less efficient, resulting in higher energy costs, and requiring bulkier, more expensive cooling systems. Nowadays, environmental legislation starts to force manufacturers to consider energy efficiency in new products, and as a result switched-mode amplifiers are used in a growing range of applications.

1.2 Trends in SMPCs for high-precision applications

The increasing availability of low-cost processing power, driven by Moore's law[2], has led to almost full digitization of information processing and transport in both industrial and consumer applications. More recently, this trend has also spread to power amplifiers, which are nowadays often implemented fully digital, i.e. with both digital control and modulation. As a result, the term "amplifier" might not be appropriate anymore. The term "converter" more accurately describes modern SMPAs. Therefore, a better name for a modern SMPA is switched-mode power converter (SMPC), or power digital-to-analog converter.

The photo-lithographic equipment used in the IC production process relies on SMPCs in combination with linear or planar actuators to position the wafers on which the circuits are printed with significantly higher accuracy than the feature size[3] [14, 86]. As a result, the accuracy of SMPCs in lithography is required to increase with the same trend as the decrease of the smallest feature size. From Moore's law it can be deduced that the feature size in lithography shrinks by a factor of four every two years.

Simultaneously the throughput of lithographic equipment, i.e. the number of wafers processed per unit time, is increasing over time. As a result the power requirements of the SMPCs increase over time too[4]. Furthermore, due to the increasing complexity and cost of ownership of lithographic machines the reliability of high-power SMPCs starts to become a serious issue. Especially the effects of single-event burn-out (SEB) [33, 121], and thermal cycling [70] pose significant problems. Similar trends can be observed in medical imaging, e.g. magnetic resonance imaging (MRI) and computer tomography (CT), where the resolution and frame rates increase over time, thus requiring increased accuracy and dynamic range of the SMPCs.

The accuracy and dynamic range of an SMPC with its control and modulation is limited by the noise and distortion added by the measurements required for feedback. However, it also depends on the distortion and noise added by the end stage, on the modulation technique, and on the distortion and noise added by the external power supply of the converter. The power capability is limited by the losses of the converter, which in turn depend on the chosen topology, modulation,

[2] In 1970, Gordon Moore, co-founder of Intel Corporation, predicted that the number of transistors on integrated-circuits (ICs) will double every two years. This has become known as Moore's law, which has been used in semiconductor industry to set research and development targets.

[3] The feature size is the smallest feature that can be printed on a wafer.

[4] The required peak mechanical power in wafer scanners increases with the third power of the throughput.

semiconductors, and passive components. The reliability is mainly determined by the used components, the topology, and the modulation.

1.3 Research objectives and thesis outline

Conventional switched-mode converters suffer from disturbances caused by the modulation, end stage, and external power supply. The most commonly applied remedy is to reject such disturbances using feedback control. Although, the use of control algorithms reduces the effect of disturbances by a certain amount, they cannot be eliminated completely. A better first step is to eliminate the sources of distortion as much as possible, before trying to mask them using advanced control.

This thesis focuses on the elimination of zero-crossing distortion caused by the end stage. The effects of the measurements, control algorithms, and external power supply on the output quality are not detailed in this thesis.

The first part of this thesis treats SMPC modeling techniques and sources of distortion in state-of-the-art SMPCs. In the second part a new class of switched-mode power amplifiers with high-quality output is proposed. The proposed topology and modulation completely eliminate the zero-crossing distortion that is normally present in SMPCs. Moreover, the proposed topology is robust for shoot-through current, i.e. short circuiting caused by accidental turn-on of semiconductor switches, thereby improving the reliability of the converter. The theory developed in the second part is verified by measurements performed on a prototype converter. In the final part conclusions are drawn, recommendations are given, and the thesis contributions are summarized.

Towards high-quality power amplification

In Chapter 2, modeling of switched-mode converters using state-space averaging is treated. Furthermore, a method is proposed to remove superfluous states from circuits with state dependencies.

Chapter 3 treats various sources of distortion in SMPCs and identifies switching blanking time as the main source of disturbances in PWM converters. Lastly, in Section 3.6, existing methods to suppress the effects of blanking time in PWM converters are discussed. Furthermore, existing alternative topologies are highlighted that do not suffer from blanking-time-related distortion and/or are ro-

bust for shoot-through currents. The dual-buck (DB) topology is identified to not suffer from blanking-time-related distortion and to be robust for shoot-through currents.

A robust power converter with high signal-quality

The second part contains the main contributions of this thesis. First, in Chapter 4 a class of converters based on the DB end stage is treated. Linear operation of a converter is essential for low output distortion. Therefore, boundaries are given for the linear operation of the DB converter. It is shown that to ensure linear behavior a bias current has to be imposed. Furthermore, the variable transformations are given that are used in the remainder of Part II.

The bias current that is required for linear operation results in increased losses and volume with respect to conventional PWM converters. In Chapter 5 it is shown that the volumetric footprint of the DB can be reduced by employing coupling of the inductive components in combination with a proper modulation strategy. Different combinations of coupling and modulation strategies are verified with measurements on prototype converters.

The DB topology does not suffer from blanking-time-related distortion. In Chapter 6 it is shown that the DB also does not suffer from distortion caused by the forward voltage drops across the semiconductor devices. Using a detailed analytical model it is shown that the input-output relation of the DB is perfectly linear when the end-stage components are properly selected. The harmonic distortion under various conditions is investigated through a simulation study that includes the switching transients.

In Chapter 7 different modulation strategies are compared for the full-bridge equivalent of the DB using simulation and measurement results.

Chapter 8 proposes two feedback control schemes for the DB converter. One relies on industrial standard single-input single-output (SISO) controllers to separately control the output and bias current by applying decoupling. The second is a full-state feedback control, where the closed-loop poles are placed according to a Bessel prototype system. As a result, the output of the DB becomes a delayed version of the reference signal without overshoot.

Chapter 9 contains experimental results obtained from a prototype DB converter. The measured harmonic performance is compared to the analytical and simulation results of Chapter 6, and to measurements obtained from a prototype of the conventional counterpart of the DB.

Chapter 10 summarizes the conclusions. The thesis contributions are listed, and recommendations for future research are given.

Part I

Towards high-quality power amplification

Chapter 2

Modeling of power electronic converters

"Understanding is, after all, what science is all about – and science is a great deal more than mindless computation."

(Roger Penrose)

Abstract — Most techniques for frequency response analysis and control system design rely on the existence of linear models for the system under test or control. Cyclically switched converters are nonlinear but can be considered piecewise linear when assuming that switching between the linear circuits occurs instantaneously. Several methods exist to obtain linear approximate models for piecewise linear systems. However, in some cases it can be difficult to obtain linear models without constraints. This chapter introduces a systematic approach based on state-space averaging to obtain linear time-invariant state-space models without constraints from cyclically switched electrical circuits. Next, an efficient method is given to eliminate superfluous states from a state-space description with constraints.

2.1 Introduction

Switched-mode power converters are nonlinear due to the intrinsic switching nature. Power processing occurs by routing the energy flow between intermediate storage components, usually by periodically changing the circuit between a finite number of configurations. Switching converters can be considered piecewise linear when assuming that the switching transient between configurations occurs instantaneously, and that the electrical components used in each configuration are linear.

Frequency response analysis is a well-established method to characterize the behavior of power converters, servo systems, audio amplifiers, power supplies, and many other applications. Both frequency response analysis and controller design rely mostly on the existence of linear time-invariant (LTI) models for the system under test or control.

Two well-established methods to obtain LTI models for switched-mode power converters (SMPCs) are state-space averaging [65] and sampled-data modeling [26, 43]. Both methods result in operating-point dependent LTI models. The sampled-data modeling method results in discrete models with a very high accuracy at the chosen sample instances, and unlike the state-space averaging method it can be used for all classes of converters. However, the resulting discrete models are not as insightful as the analytical continuous-time models that can be obtained by state-space averaging. Even though bold assumptions are made when applying state-space averaging, in many cases sufficiently accurate models can be obtained.

2.2 State-space averaging applied to piecewise linear models

Piecewise linear systems can be described using a state-space representation by selecting the matrices and inputs from a finite set $K \subset \mathbb{N}$, as given by

$$\dot{\mathbf{x}}(t) = \mathbf{F}_k \mathbf{x}(t) + \mathbf{g}_k \tag{2.1a}$$

$$\mathbf{y}(t) = \mathbf{M}_k \mathbf{x}(t) + \mathbf{n}_k \tag{2.1b}$$

where $\mathbf{F}$ is the state-matrix, $\mathbf{g}$ is the input vector, $\mathbf{M}$ is the output matrix, $\mathbf{n}$ is the direct feed-through vector. The index $k \in K$, indicates which matrices and/or vectors are active from set K. In (2.1) it is assumed that the input vectors $\mathbf{g}_k$, and

$\mathbf{n}_k$ are only dependent on k and are consequently assumed constant in each linear interval.

In the case of switching converters, k represents the switching state, and therefore it changes cyclically over time. It should be noted that the sequence of switching states that are covered during a cycle might depend on the operating point of the converter. State-space averaging requires a fixed sequence, therefore, care should be taken when averaging models that have no fixed sequence.

2.2.1 Determining the moving-average of the model

State-space averaging results in approximately linear models that are not dependent on k. The procedure involves two steps: determining the moving-average model, and linearization in an operating point. The moving average is given by

$$\langle \mathbf{\Lambda} \rangle (t) = \frac{1}{T_{\text{sw}}} \int_{t}^{t+T_{\text{sw}}} \mathbf{\Lambda}(\tau) \mathrm{d}\tau \tag{2.2}$$

where $\mathbf{\Lambda}$ is a matrix or vector that depends on time (t). For the special case that $\mathbf{\Lambda}$ is only dependent on the switching state k, (2.2) simplifies to

$$\langle \mathbf{\Lambda} \rangle = \frac{1}{T_{\text{sw}}} \sum_{k \in K} \mathbf{\Lambda}_k T_k, \text{ with} \tag{2.3a}$$

$$T_{\text{sw}} = \sum_{k \in K} T_k \tag{2.3b}$$

where in turn, $\mathbf{\Lambda}_k$ is a matrix or vector that is cyclically switched, T_{sw} is the switching cycle time of the converter, and T_k is the time that each switching state is active. For clarity, from here on the time dependency (t) will be omitted from the notation.

For pulse-width-modulated (PWM) converters most, and in some cases even all, of the time intervals (T_k) can be expressed in terms of the desired inputs ($\mathbf{u}$) of the system, e.g. duty-cycles or modulation indices. In that case, by using (2.2) and (2.3a) on (2.1), the following average model can be obtained:

$$\langle \dot{\mathbf{x}} \rangle = \langle \mathbf{F}(\mathbf{u}) \mathbf{x} \rangle + \langle \mathbf{g}(\mathbf{u}) \rangle \tag{2.4a}$$

$$\langle \mathbf{y} \rangle = \langle \mathbf{M}(\mathbf{u}) \mathbf{x} \rangle + \langle \mathbf{n}(\mathbf{u}) \rangle \tag{2.4b}$$

where $\mathbf{u}$ is a vector with desired inputs, which typically contains duty ratios (δ) that are relative conduction times of semiconductors, modulation indices (m), and

desired voltages, but might also include additional disturbance inputs.

When assuming

$$\langle \mathbf{F}(\mathbf{u})\mathbf{x} \rangle \approx \langle \mathbf{F}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle, \text{ and} \tag{2.5a}$$

$$\langle \mathbf{M}(\mathbf{u})\mathbf{x} \rangle \approx \langle \mathbf{M}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle \tag{2.5b}$$

equation (2.4) can be approximated by

$$\langle \dot{\mathbf{x}} \rangle \approx \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u}) = \langle \mathbf{F}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle + \langle \mathbf{g}(\mathbf{u}) \rangle \tag{2.6a}$$

$$\langle \mathbf{y} \rangle \approx \mathbf{g}(\langle \mathbf{x} \rangle, \mathbf{u}) = \langle \mathbf{M}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle + \langle \mathbf{n}(\mathbf{u}) \rangle \tag{2.6b}$$

where $\mathbf{f}$, and $\mathbf{g}$ depend on the moving average of the state vector ($\langle \mathbf{x} \rangle$) and the input vector ($\mathbf{u}$).

There are many works on the accuracy of the state-space averaging procedure, starting with [64] and more recent [7]. However, only the assumption given in (2.5) leads to an error from the moving-average behavior of (2.1), as briefly explained in [43, page 307]. In other words, (2.6) becomes an equality when $\mathbf{x}$ is constant over one switching cycle, or when $\mathbf{F}$ and $\mathbf{M}$ do not depend on the switching state of the converter; that is, when $\mathbf{x}$ or $\mathbf{F}$ and $\mathbf{M}$ are time-invariant.

When $\langle \mathbf{y} \rangle$ is a linear combination of $\langle \mathbf{x} \rangle$, which is mostly the case, the output matrix $\mathbf{M}$ is time-invariant. However, that is not generally true for the state matrix $\mathbf{F}$ due to the switching nature of a converter. The state vector $\mathbf{x}$ is in practice never constant, since it would imply a zero time derivative of the state vector ($\dot{\mathbf{x}} = 0$). Still, the state-space averaging procedure can be a very powerful tool, since in many cases time-invariant state matrices can be obtained. Moreover, even when it is not possible to obtain time-invariant state matrices the error introduced by (2.5) is in many cases small enough to obtain reasonably accurate small-signal models.

2.2.2 Linearization in an operating point

The state-space average model, given by (2.6), is nonlinear since its matrices and vectors depend on the operating point of the converter. A linear model can be obtained by linearizion in an operating point using the Taylor expansion of (2.6)

and truncating the result beyond the first order terms, resulting in

$$\langle \dot{\mathbf{x}} \rangle \approx \mathbf{f}(\mathbf{x}_o, \mathbf{u}_o) + \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{x} \rangle}\right|_{\mathbf{u}_o} (\langle \mathbf{x} \rangle - \mathbf{x}_o) + \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{(\mathbf{x}_o, \mathbf{u}_o)} (\mathbf{u} - \mathbf{u}_o) \quad (2.7a)$$

$$\langle \mathbf{y} \rangle \approx \mathbf{g}(\mathbf{x}_o, \mathbf{u}_o) + \left.\frac{\partial \mathbf{g}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{y} \rangle}\right|_{\mathbf{u}_o} (\langle \mathbf{x} \rangle - \mathbf{x}_o) + \left.\frac{\partial \mathbf{g}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{(\mathbf{x}_o \mathbf{u}_o)} (\mathbf{u} - \mathbf{u}_o) \quad (2.7b)$$

where in turn $\mathbf{x}_o$ and $\mathbf{u}_o$ represent the steady-state operating-point for which the switched-mode converter is linearized.

When expressing perturbations from steady state as $\tilde{\mathbf{x}} = \langle \mathbf{x} \rangle - \mathbf{x}_o$, $\tilde{\mathbf{u}} = \langle \mathbf{u} \rangle - \mathbf{u}_o$, and acknowledging that in the steady-state $\dot{\mathbf{x}}_\mathbf{o} = 0$, (2.7) simplifies to

$$\dot{\tilde{\mathbf{x}}} \approx \mathbf{A}(\mathbf{u}_o)\tilde{\mathbf{x}} + \mathbf{B}(\mathbf{x}_o, \mathbf{u}_o)\tilde{\mathbf{u}} + \mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) \quad (2.8a)$$

$$\tilde{\mathbf{y}} \approx \mathbf{C}(\mathbf{u}_o)\tilde{\mathbf{x}} + \mathbf{D}(\mathbf{x}_o, \mathbf{u}_o)\tilde{\mathbf{u}} + \mathbf{v}_o(\mathbf{x}_o, \mathbf{u}_o) \quad (2.8b)$$

where the state and input matrices equal

$$\mathbf{A}(\mathbf{u}_o) = \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{x} \rangle}\right|_{\mathbf{u}_o} \quad (2.8c)$$

$$\mathbf{B}(\mathbf{x}_o, \mathbf{u}_o) = \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{(\mathbf{x}_o, \mathbf{u}_o)} \quad (2.8d)$$

the output and direct feed-through matrices become

$$\mathbf{C}(\mathbf{u}_o) = \left.\frac{\partial \mathbf{g}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{x} \rangle}\right|_{\mathbf{u}_o} \quad (2.8e)$$

$$\mathbf{D}(\mathbf{x}_o, \mathbf{u}_o) = \left.\frac{\partial \mathbf{g}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{(\mathbf{x}_o, \mathbf{u}_o)} \quad (2.8f)$$

and the operating-point-dependent disturbance terms are given by

$$\mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) = \mathbf{f}(\mathbf{x}_o, \mathbf{u}_o) \quad (2.8g)$$

$$\mathbf{v}_o(\mathbf{x}_o, \mathbf{u}_o) = \mathbf{g}(\mathbf{x}_o, \mathbf{u}_o). \quad (2.8h)$$

The state-space averaging method as explained in this section assumes that the moving averages of the state variables approximate the circuit's dynamical behavior. This is not generally true. In many resonant converter topologies dynamics are captured in the switching frequency component, or harmonics of the switching frequency, instead of the moving average of the state variables. In that case one can use the generalized average, instead of the moving average, as pro-

posed in [88]. The so-called Floquet theory is in fact the underlying averaging principle applied [106]. Of course, methods based on sampled data, as presented in [26,43], also result in very accurate models in the sample points and can, therefore, be used for all classes of converters.

2.3 Removing superfluous states

The previous section describes the state-space averaging procedure that is used to determine an operating-point-dependent linear approximate model of a piecewise linear system, as given in (2.1). For the averaging procedure the state-space matrices and vectors of all switching states, $k \in K$, should be known.

Determining state-space matrices for switching states is in many cases straightforward. It is sufficient to choose the state vector to include all the inductor currents and capacitor voltages and to determine the corresponding state equations. However, when state dependencies are present, difficulties occur. Determining a state-space model without constraints can be a labor-intensive task. In such cases it is often easier to add algebraic constraints, resulting in a so-called semi-explicit differential algebraic equations (DAEs) or ordinary differential equations (ODEs) with algebraic constraints. However, such constraints might not be allowed for the methods that need to be applied to the model.

Electronic circuit simulation software typically relies on methods as proposed by Gear [31] or Runge and Kutta [127] for solving DAEs. There are also many works on index reduction of DAEs [32, 60, 110], where the strangeness index is a measure for the distance of a DAE to its related ODE. However, most approaches rely on differentiation, adding dummy variables, substitution, or a combination of those, and often add complexity to the model. In [35, chapter 3] a method to remove superfluous states based on the generic system matrix is introduced. The proposed method is especially suited for automatic generation of state-space models from net lists. The result of the procedure still contains the superfluous state equations. However, the corresponding outputs and the superfluous state equations are correctly expressed in terms of the *real* states of the circuit.

The remainder of this section presents an alternative approach to remove superfluous states from a circuit with state dependencies. The method effectively transforms a semi-explicit DAE or ODE with Kirchhoff's voltage and current law constraints to an ODE without constraints. The resulting state-space representation has the lowest possible order, while fully describing all the dynamics of the system. A disadvantage of the proposed procedure is that it only can be used in

combination with state-space averaging when the state-space matrices are time-invariant.

2.3.1 The procedure

A system with superfluous states can be written in the state-space form as

$$\dot{\mathbf{x}}_d = \mathbf{A}_d\mathbf{x}_d + \mathbf{B}_d\mathbf{u}_d \tag{2.9a}$$
$$\mathbf{0} = \mathbf{K}\mathbf{x}_d \tag{2.9b}$$
$$\mathbf{y} = \mathbf{C}_d\mathbf{x}_d + \mathbf{D}_d\mathbf{u}_d \tag{2.9c}$$

with

$$\mathbf{x}_d = \begin{pmatrix} \mathbf{x}_s \\ \mathbf{x}_r \end{pmatrix} \tag{2.9d}$$
$$\mathbf{u}_d = \begin{pmatrix} \mathbf{u}_s \\ \mathbf{u} \end{pmatrix} \tag{2.9e}$$

and

$$\mathbf{B}_d = \begin{pmatrix} \mathbf{B}_s & \mathbf{B}_r \end{pmatrix} \tag{2.9f}$$
$$\mathbf{D}_d = \begin{pmatrix} \mathbf{D}_s & \mathbf{D}_r \end{pmatrix} \tag{2.9g}$$

where $\mathbf{x}_s \in \mathbb{R}^n$ refers to the states of the superfluous storage elements that need to be removed from $\mathbf{x}_d \in \mathbb{R}^m$, and where $\mathbf{u}_s \in \mathbb{R}^n$ refers to the artificial inputs/sources, which are added to the system nodes and meshes with state dependencies. The matrix $\mathbf{K} \in \mathbb{R}^{n\times m}$ contains the Kirchhoff voltage- and current-law equations that apply to the dependent states.

For such a system an ODE exists, given by

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{2.10}$$
$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{2.11}$$

with $\mathbf{x} \in \mathbb{R}^{m-n}$ and where the system matrices of (2.10) can be expressed in terms

of the matrices of (2.9) as

$$\mathbf{A} = \mathbf{T}\mathbf{A}_d\mathbf{G} \tag{2.12}$$
$$\mathbf{B} = \mathbf{T}\mathbf{B}_r \tag{2.13}$$
$$\mathbf{C} = \left(\mathbf{C}_d - \mathbf{D}_s\mathbf{S}\mathbf{A}_d\right)\mathbf{G} \tag{2.14}$$
$$\mathbf{D} = \mathbf{D}_r - \mathbf{D}_s\mathbf{S}\mathbf{B}_r \tag{2.15}$$

with

$$\mathbf{S} = \left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K} \tag{2.16}$$
$$\mathbf{T} = \mathbf{G}^{+}\left(\mathbf{I}_m - \mathbf{B}_s\mathbf{S}\right) \tag{2.17}$$

and where $\mathbf{G}^{+}$ is the Moore-Penrose pseudo inverse of $\mathbf{G}$ for linearly independent columns, that is,

$$\mathbf{G}^{+} = \left(\mathbf{G}^{\intercal}\mathbf{G}\right)^{-1}\mathbf{G}^{\intercal}. \tag{2.18}$$

The obtained state vector $\mathbf{x}$ is related to $\mathbf{x}_d$ by

$$\mathbf{x}_d = \mathbf{G}\mathbf{x} \tag{2.19}$$

where $\mathbf{G}$ is a matrix whose columns are a basis of the null space of $\mathbf{K}$,

$$\mathbf{G} = \operatorname{null}\left(\mathbf{K}\right). \tag{2.20}$$

Any basis of the null space can be used, however, the rational basis obtained through Gaussian elimination preserves $\mathbf{x}_r$ of the DAE, that is $\mathbf{x} = \mathbf{x}_r$.

2.3.2 Proof

The above results can be proven by first combining (2.19) with (2.9), which results in

$$\mathbf{G}\dot{\mathbf{x}} = \mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{B}_s\mathbf{u}_s + \mathbf{B}_r\mathbf{u} \tag{2.21a}$$
$$\mathbf{y} = \mathbf{C}_d\mathbf{G}\mathbf{x} + \mathbf{D}_s\mathbf{u}_s + \mathbf{D}_r\mathbf{u} \tag{2.21b}$$

where $\mathbf{B}_d$, $\mathbf{D}_d$, and $\mathbf{u}_d$ are expanded as in (2.9e) to (2.9g).

Multiplying (2.21a) with $\mathbf{K}$, yields

$$\mathbf{0} = \mathbf{K}\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{K}\mathbf{B}_s\mathbf{u}_s + \mathbf{K}\mathbf{B}_r\mathbf{u} \tag{2.22}$$

since $\mathbf{K}\mathbf{G}\dot{\mathbf{x}} = \mathbf{0}$. Furthermore, because $\mathbf{x} \in \mathbb{R}^{m-n}$, the matrix multiplication $\mathbf{K}\mathbf{G}$ should equal an $m \times (m-n)$ zero matrix, and consequently the columns of $\mathbf{G}$ are zero vectors of $\mathbf{K}$. Moreover, the columns of $\mathbf{G}$ are linearly independent, making $\mathbf{G}$ a basis for the null-space of $\mathbf{K}$, and the number of columns in $\mathbf{G}$ the nullity of $\mathbf{K}$.

Using (2.22) the artificial input vector ($\mathbf{u}_s$) can be expressed in terms of $\mathbf{x}$ and $\mathbf{u}$ as

$$\mathbf{u}_s = -\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\left(\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{B}_r\mathbf{u}\right) \tag{2.23}$$

where $\mathbf{K}\mathbf{B}_s$ is square and invertible.

When assuming that the columns of $\mathbf{G}$ are linearly independent, that is $\mathbf{G}^+\mathbf{G} = \mathbf{I}_{m-n}$, and substituting $\mathbf{u}_s$ with (2.23), (2.21) can be rewritten to

$$\dot{\mathbf{x}} = \mathbf{G}^+\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{G}^+\mathbf{B}_r\mathbf{u} - \mathbf{G}^+\mathbf{B}_s\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\left(\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{B}_r\mathbf{u}\right) \tag{2.24a}$$

$$\mathbf{y} = \mathbf{C}_d\mathbf{G}\mathbf{x} + \mathbf{D}_r\mathbf{u} - \mathbf{D}_s\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\left(\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{B}_r\mathbf{u}\right). \tag{2.24b}$$

Finally, the result of (2.24) can be simplified to

$$\dot{\mathbf{x}} = \mathbf{G}^+\left(\mathbf{I}_m - \mathbf{B}_s\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\right)\left(\mathbf{A}_d\mathbf{G}\mathbf{x} + \mathbf{B}_r\mathbf{u}\right) \tag{2.25a}$$

$$\mathbf{y} = \left(\mathbf{C}_d - \mathbf{D}_s\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\mathbf{A}_d\right)\mathbf{G}\mathbf{x} + \left(\mathbf{D}_r - \mathbf{D}_s\left(\mathbf{K}\mathbf{B}_s\right)^{-1}\mathbf{K}\mathbf{B}_r\right)\mathbf{u} \tag{2.25b}$$

which is equal to (2.10).

Two practical examples of the proposed method are given in Appendix B.

2.4 Discretization

Models obtained through state-space averaging are time-continuous and might need discretization when applying discrete control. When assuming zero-order holds for the inputs, that is the inputs remain constant over a sampling time in-

terval, the resulting discrete system may be denoted as

$$\mathbf{x}[k+1] = \mathbf{\Phi}\mathbf{x}[k] + \mathbf{\Gamma}\mathbf{u}[k] \tag{2.26a}$$

$$\mathbf{y}[k] = \mathbf{C}\mathbf{x}[k] \tag{2.26b}$$

where the matrices $\mathbf{\Phi}$, and $\mathbf{\Gamma}$ are obtained from the time-continuous model [120, chapter 4] by

$$\mathbf{\Phi} = e^{\mathbf{A}T_s} \tag{2.27a}$$

$$\mathbf{\Gamma} = \left(\int_0^{T_s} e^{\mathbf{A}\tau} \mathrm{d}\tau \right) \mathbf{B} = \mathbf{A}^{-1} \left(\mathbf{\Phi} - \mathbf{I} \right) \mathbf{B} \tag{2.27b}$$

where in turn $\mathbf{I}$ is an identity matrix of the same size as $\mathbf{\Phi}$ and T_s is the sampling time of the discrete model. It should be noted that the last equality of (2.27b) is only valid for non-singular $\mathbf{A}$. For singular $\mathbf{A}$ Van Loan's method [120, 122] can be used. First construct matrix $\mathbf{M}$ as

$$\mathbf{M} = \begin{pmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{0} & \mathbf{0} \end{pmatrix} \tag{2.28}$$

where the zero matrices are chosen such that $\mathbf{M}$ is square. Then the $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ can be determined as

$$e^{\mathbf{M}T_s} = \begin{pmatrix} \mathbf{\Phi} & \mathbf{\Gamma} \\ \mathbf{0} & \mathbf{I} \end{pmatrix}. \tag{2.29}$$

For PWM converters the sampling time, T_s, and switching time, $T_{\mathrm{sw}} = 1/f_{\mathrm{sw}}$, are often integer multiples of each other. Moreover, to prevent offsets between the discrete model and sampled data of the real system, the measured variables need to be sampled at their periodic average value. This is explained in more detail in Chapter 8.

2.5 Summary

This chapter treats state-space averaging together with a procedure to remove superfluous states from a circuit. The effectiveness of both approaches is illustrated with examples in appendices B and C. Both methods are used later in this thesis to obtain linear time-invariant state-space models without constraints.

Chapter 3

Sources of distortion in PWM converters

"All progress is precarious, and the solution of one problem brings us face to face with another problem."

(Martin Luther King Jr.)

Abstract — Switched-mode converters process electrical energy efficiently by switching power flows between sources and outputs through intermediate storage elements, i.e. inductors and capacitors. Switched-mode converters generally have higher efficiencies than linear amplifiers but at the cost of switching harmonics. However, harmonics due to switching are not the only source of output waveform distortion. This chapter focuses on PWM switching legs with output filter. The impact of different sources of distortion is explored. The blanking time, required to prevent short-circuit during switching transitions, is identified as the most significant contribution. Different methods and topologies that eliminate blanking-time effects are explored and the dual buck topology is identified as a robust converter with high output quality.

3.1 Introduction

Most switched-mode converters with bidirectional power flow rely on conventional switching legs. They can be operated with a current or voltage source as an external power-supply, and with or without demodulation or output filters. Figure 3.1 depicts such a bidirectional switching leg, including its output filter (L_{HB} & C_f), and a voltage-source external supply. By modulating the switches, the power of the external supply is processed to the desired output quantity (u_{out} or i_{out}). This configuration is often referred to as the half-bridge (HB) converter.

Although this type of converter is bidirectional, the external power supply (U_{DC}) is often called the input. This is different from linear amplifiers, as discussed in Chapter 1, where the input is the signal that controls the modulation. The input that controls the modulator in SMPCs is often called reference or set point. The outputs of the modulator control the states of the switches, and are called gating signals.

To prevent short circuiting, the switches (S_1 & S_2) should be operated complementary. Since in practice a switch needs a finite time to make a transition, antiparallel diodes (D_1 & D_2) are added to create a free-wheeling path when both switches are off, i.e. not conducting. Depending on the applied semiconductor switch, these diodes have to be added explicitly when they are not intrinsically present in the device.

This chapter highlights the main sources of distortion in PWM converters. These origin from the modulator, the external supply, and the switching leg. Next, the importance of the various types of distortion is determined. Finally, methods and topologies are explored that eliminate blanking-time-related distortion.

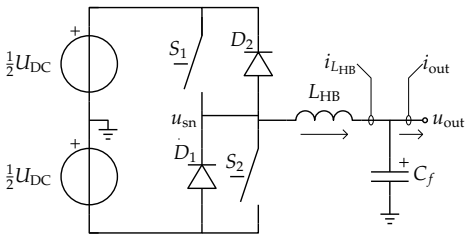


Figure 3.1: Conventional half-bridge converter, with voltage-source input and output filter.

3.2 The modulator

Many fixed- and variable-frequency modulation techniques can be found in the literature [38, 67]. Fixed-frequency PWM is one of the most widely used schemes. PWM can be implemented using analog circuits, or in a digital way using programmable logic or dedicated integrated-circuits (ICs). Digitally implemented PWM is often referred to as digital pulse-width modulation (DPWM). In both the analog and digital methods the reference, i.e. duty cycle (δ) or modulation index (m), is compared to a triangular (double edge), or sawtooth (single edge) waveform.

The best baseband signal quality can be obtained applying either double-edge natural-sampled PWM, or asymmetrical regular-sampled PWM, as explained in [38, chapter 3]. Figure 3.2a depicts double-edge natural-sampled PWM. Both the carrier and the modulation index (m) are time-continuous. Ideally this type of modulation generates no baseband harmonics [38, chapter 3], i.e. harmonics of the reference waveform. The signal quality is, therefore, only determined by the carrier side-band harmonics (switching harmonics) that enter the baseband frequency range. As a consequence, the output quality can be set arbitrarily high by choosing the ratio between the switching and the reference frequency f_{sw}/f_o, and by proper selection of the cut-off frequency of the output filter.

In practice the carrier ratio is often chosen as $f_{sw}/\hat{f}_o > 20$ [13, chapter 3], where $\hat{f}_o$ is the maximum reference frequency that needs to be generated. However, depending on the application higher carrier ratios might be required, or lower ratios can be allowed.

Natural-sampled PWM relies on analog circuits. The quality of the carrier is essential as any deviation from an ideal triangular waveform introduces harmonic distortion into the output [111]. Also the analog comparator used for the reference carrier comparison has to be selected carefully, as explained in [74, chapter 4].

Figure 3.2b depicts digitally generated double-edge-carrier asymmetrical regular-sampled modulation. The carrier is time-discretized with frequency f_{clk} and the modulation index (m) is sampled two times per switching cycle (T_{sw}). Figure 3.3a depicts the resulting spectrum for $f_{\text{clk}} \gg f_{\text{sw}}$. The regular sampling process causes baseband harmonics [38, chapter 3], as can be seen from Figure 3.3a. These baseband harmonics can be made arbitrarily small by increasing the ratio between the switching and reference frequency (f_{sw}/f_o). Given that the clock is sufficiently stable, carrier waveform distortion is not an issue when PWM is generated digitally [126]. The carrier signal is indeed represented with exact (digital)

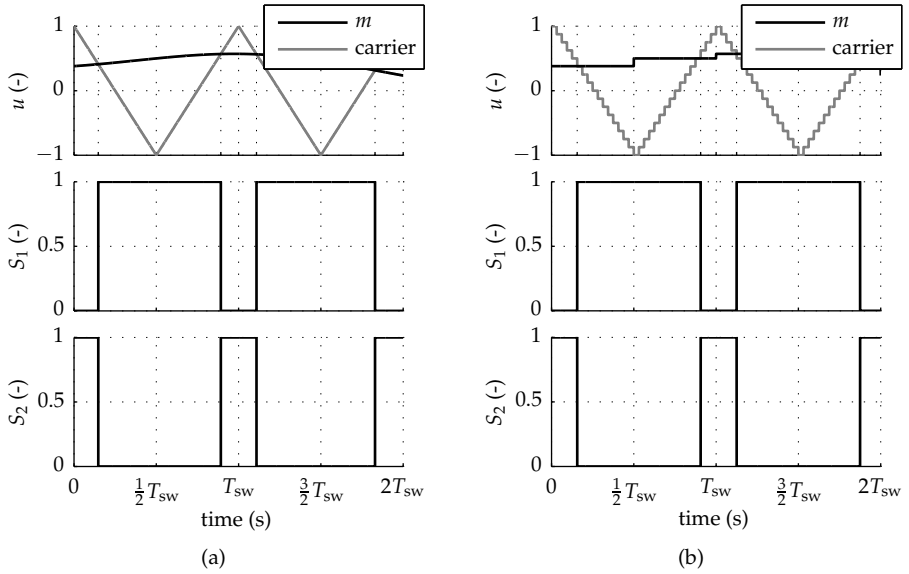


Figure 3.2: Double-edge (triangular) carrier PWM generation, (a) natural sampled with time-continuous carrier, and (b) asymmetrical regular-sampled with time-discrete carrier and 4 bits resolution.

integer values. However, the time discretization of the carrier has the same effect as amplitude quantization of the modulation index. The resulting quantization noise depends on the ratio between the clock frequency of the discrete carrier (f_{clk}) and f_{sw} [13, chapter 3]. Quantization noise is in practice the most dominant source of baseband distortion.

Figure 3.3b depicts the spectrum of discrete double-edge-carrier asymmetrical-sampled modulation with 8 bits resolution, i.e. $f_{\text{clk}} = 512 f_{\text{sw}}$. The total harmonic distortion (THD) indicated in the graphs only includes (baseband) harmonics up to harmonic number $N = 20$ and is determined as

$$\text{THD}_N = \frac{\sqrt{\sum_{n=2}^{N} \left(U_{\text{sn}}(nf_o)\right)^2}}{U_{\text{sn}}(f_o)} \tag{3.1}$$

where U_{sn} is the (root mean square (RMS)) magnitude spectrum of u_{sn}, and n the harmonic number.

Quantization noise can be reduced by increasing the resolution of the modulator. This can be done in various ways. The most straightforward method is to increase the clock frequency. However, this is not as simple as it might seem. Take for

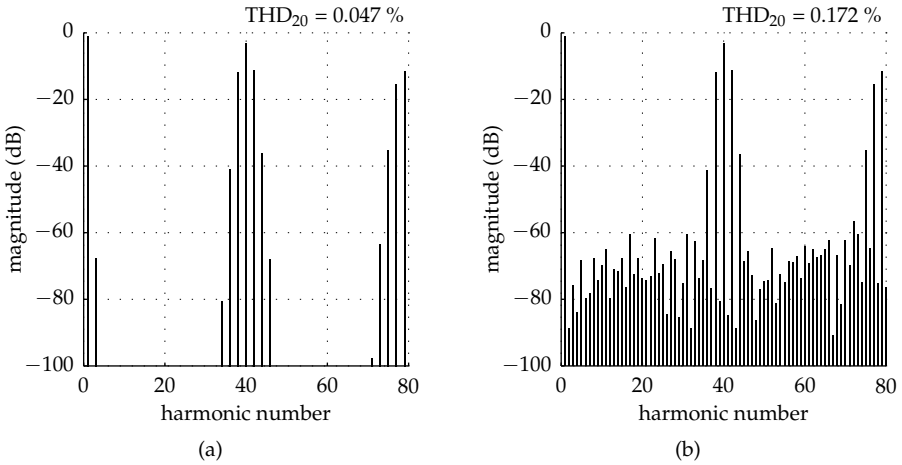


Figure 3.3: Magnitude spectrum of u_{sn} for double-edge regular-sampled modulation, with $f_{\mathrm{sw}}/f_o = 40$, and $\hat{m} = 0.9$. Plot (a) shows a time-continuous carrier (infinite precision), (b) illustrates a time-discrete carrier with 8 bits resolution ($f_{\mathrm{clk}} = 512 f_{\mathrm{sw}}$).

instance digital class-D audio amplifiers. These are normally operated using a double-edge carrier with frequencies close to 400 kHz. A typical signal-to-noise ratio (SNR) of 80 dB requires about 13 bits resolution, and consequently a carrier clock frequency of $f_{\mathrm{clk}} = 2^{13+1} f_{\mathrm{sw}} \approx 6.5\,\mathrm{GHz}$. At the time of writing this thesis this is not possible with commercially available hardware.

Other methods to improve DPWM resolution include use of multiple phase-shifted clocks, multiple counters and/or programmable delay lines [36,69,73,115]. Some of these techniques achieve picosecond resolution on currently existing hardware. Feedback control, and/or noise shaping are commonly applied to improve the output signal quality of SMPCs, as detailed in [74,76,89]. Still another approach to improve the baseband signal quality of DPWM is to emulate naturally sampled PWM digitally using interpolation or extrapolation [62].

3.2.1 Blanking time

Semiconductor switches have finite switching transition times[1] that depend on the operating point. Usually a blanking time T_{bt} is added to the gating signals of the switches in a leg (S_1 & S_2) to prevent short-circuit of the DC bus during

[1]The gate drive circuit and other electrical circuits that are involved in the switching process also contribute to the response time of the switch.

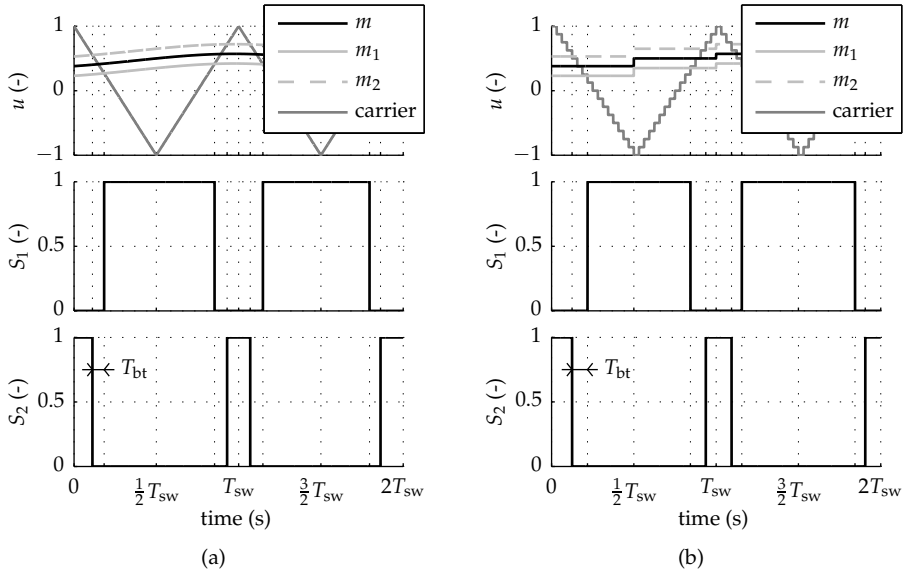


Figure 3.4: Double-edge (triangular) carrier PWM generation with blanking time (T_{bt}) for, (a) time-continuous natural sampled, and (b) discrete-time asymmetrical regular-sampled modulation.

switching. During the blanking time both switches of a switching leg are in the off state. This blanking time can be generated in various ways. Probably the most common method is to turn off a switch immediately, and delay the turn on of the complementary switch, as explained in [67, chapter 8] and [96]. Another, less common, method is to offset the modulation index (m) with a fixed negative and positive value for S_1 and S_2, respectively. This is depicted in Figure 3.4 for both natural and time-discrete asymmetrical regular-sampled PWM.

The blanking-time generation method depicted in Figure 3.4 results in a switch-node voltage (u_{sn}) that is center-aligned with the PWM signals for distinct positive or negative inductor current ($i_{L_{\text{HB}}}$), i.e., when $i_{L_{\text{HB}}}$ does not cross zero during a switching cycle. However, when zero crossings of $i_{L_{\text{HB}}}$ occur during a switching cycle, u_{sn} will be time shifted by $-\frac{1}{2}T_{\text{bt}}$, as illustrated in Figure 3.5.

For the first method, as treated in [67, chapter 8], no time shift occurs when $i_{L_{\text{HB}}}$ crosses zero within a switching cycle and a time shift of $\frac{1}{2}T_{\text{bt}}$ occurs for either a continuous positive or negative current. Which method is best depends on the application, and will not be detailed further in this thesis. Both methods, however, result in the same voltage error, as explained later in this chapter.

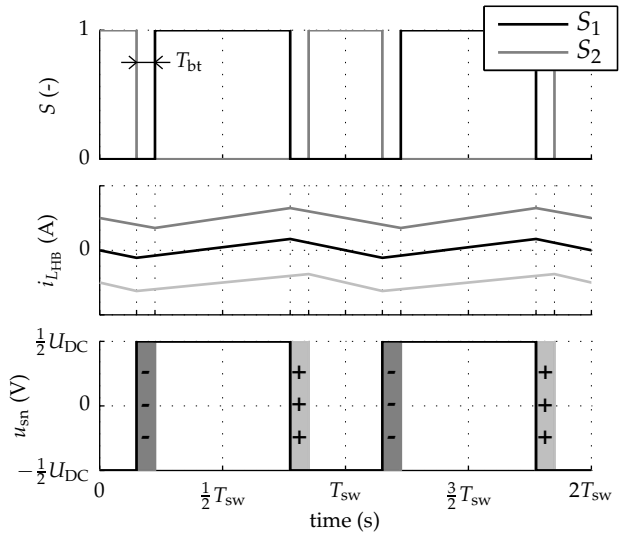


Figure 3.5: Switch-node voltage (u_{sn}) for double-edge (triangular)-carrier PWM generation with blanking time (T_{bt}), in case of distinct positive, zero average, and distinct negative inductor current.

3.3 The external power supply

SMPCs generate output quantities by switching between voltage levels. As a result, the output quality depends on the stability of the external power supplies. When assuming ideal switches and power supply, without blanking time, as illustrated in Figure 3.1, it is straightforward to show that the moving-average switch-node voltage ($\langle u_{sn} \rangle$) of a switching leg is given by

$$\langle u_{sn} \rangle = \tfrac{1}{2} U_{DC} m \tag{3.2}$$

where U_{DC} is the constant supply voltage, and m the modulation index.

From (3.2) it can be seen that there is a linear relation between modulation index (m) and $\langle u_{sn} \rangle$. In case of a perturbed supply voltage, as shown in Figure 3.6 with $R_w = 0$, the moving-average switch-node voltage becomes

$$\langle u_{sn} \rangle = \tfrac{1}{2} \left(U_{DC} + \tilde{u}_{DC} \right) m = \tfrac{1}{2} U_{DC} m + \tfrac{1}{2} \tilde{u}_{DC} m \tag{3.3}$$

where $\tilde{u}_{DC}$ represents the perturbation present on the supply voltage.

From (3.3) it can be seen that the power-supply perturbation results in an additive error term. In case of sinusoidal modulation and sinusoidal perturbation of the

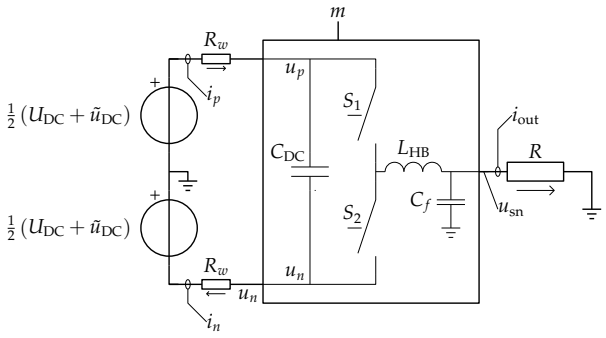


Figure 3.6: Schematic diagram of a switching leg with resistive load and symmetrical power supply with output resistance R_w.

power supply, that is, with

$$m = \hat{m} \sin(2\pi f_o t + \phi_o) \tag{3.4}$$

and

$$\tilde{u}_{DC} = \hat{u}_{DC} \sin(2\pi f_d t + \phi_d) \tag{3.5}$$

the resulting distortion present on $\langle u_{sn} \rangle$ in (3.3) becomes

$$\langle \tilde{u}_{sn} \rangle = \tfrac{1}{2} \hat{u}_{DC} \hat{m} \cos(2\pi (f_d \pm f_o) t + \phi_d \pm \phi_o) \tag{3.6}$$

where f_o is the frequency of the reference waveform, and f_d is the frequency of the power-supply perturbation. The corresponding phase shifts are given by ϕ_o and ϕ_d, respectively. The amplitudes of the reference and power supply perturbation are given by $\hat{m}$ and $\hat{u}_{DC}$, respectively.

From (3.6) it can be seen that intermodulation products will appear for every sinusoidal disturbance component present on the DC power supply.

Another source of distortion is due to the output impedance of a power supply. For steady-state, and assuming a resistive load and power supply output impedance, as depicted in Figure 3.6 with $\tilde{u}_{DC} = 0$, the distorted moving-average switch-node voltage becomes [84]

$$\langle u_{sn} \rangle = \frac{R}{R + \frac{1}{2} R_w (1 + m^2)} \tfrac{1}{2} U_{DC} m \tag{3.7}$$

where R_w represents the power supply output resistance and wire resistance.

From (3.7) it can be seen that R_w results in a multiplicative error term, which

becomes unity when R_w equals zero. The error due to R_w is a function of the squared modulation-index, and can be made arbitrarily small by increasing the ratio R/R_w. The resistance in the return path is not considered because it is in series with the load resistance R and does not add to the harmonic distortion. It should be noted that (3.7) is only valid under the assumption that u_p and u_n, in Figure 3.6, are constant over one switching cycle. The capacitance C_{DC} and inductor L_{HB} in Figure 3.6 should, therefore, be sufficiently large. When C_{DC} is omitted, the effect of R_w becomes equivalent to the on-resistance of the switches, which is treated later in this chapter.

Figure 3.7a illustrates the magnitude spectrum of u_{sn} for a power supply perturbed with sinusoidal $\tilde{u}_{\mathrm{DC}}$ signal with $\hat{u}_{\mathrm{DC}} = 0.1U_{\mathrm{DC}}$, $f_d = 10f_o$, $R_w = 0\,\Omega$, and $\hat{m} = 0.9$, as given in (3.5). Intermodulation products appear at $f_d \pm f_o$ with amplitude $\frac{1}{2}\hat{u}_{\mathrm{DC}}\hat{m}$, as given in (3.6), and the first harmonic (f_o) is not affected by the perturbed power supply. Power-supply perturbation also leads to additional sideband harmonics of the switching frequency (f_{sw}), as can be seen from Figure 3.7a. Natural-sampled PWM with $f_{\mathrm{sw}} = 40f_o$ has been used for these results. As a consequence no other baseband harmonics appear in Figure 3.7a.

The influence of the output resistance of the power supply on the magnitude spectrum of u_{sn} is illustrated in Figure 3.7b, for $R_w = 0.1R$, and $\hat{u}_{\mathrm{DC}} = 0\,\mathrm{V}$. The distortion appears as an amplitude error of the first harmonic (f_o) that in practice can be regarded as an increased output resistance of the end stage. The higher harmonics due to R_w fall off very fast. In practice only the first two or three (odd) harmonics are significant. It should once more be noted that (3.7) is only valid for steady-state, therefore, the effects of the reactive components are neglected for harmonics of the reference waveform.

Figure 3.8 depicts the moving-average output current ($\langle i_{\mathrm{out}} \rangle$) and power-supply currents ($\langle i_p \rangle$ & $\langle i_n \rangle$) for a symmetrical power supply, as depicted in Figure 3.6, which are, when assuming steady-state, given by

$$\langle i_p \rangle = \frac{1}{4} U_{\mathrm{DC}} R^{-1} (1 + m)\, m \tag{3.8}$$

$$\langle i_n \rangle = -\frac{1}{4} U_{\mathrm{DC}} R^{-1} (1 - m)\, m \tag{3.9}$$

and

$$\langle i_{\mathrm{out}} \rangle = \langle i_p \rangle - \langle i_n \rangle. \tag{3.10}$$

From Figure 3.8 it can be seen that for both positive and negative output current one of the supplies needs to sink power/current. This effect might cause considerable perturbation of the power supply voltage U_{DC} and is commonly referred

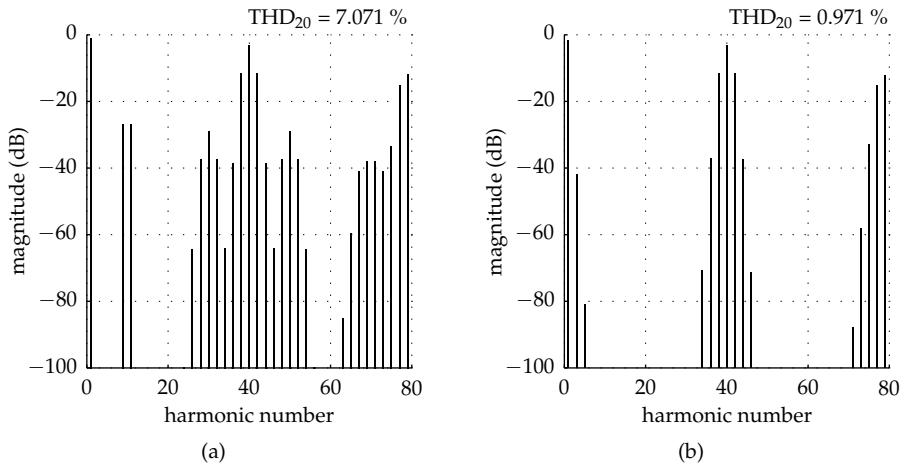


Figure 3.7: Magnitude spectrum of u_{sn} for double-edge natural-sampled modulation, with $f_{\text{sw}}/f_o = 40$, and $\hat{m} = 0.9$. Plot (a) shows the effect of a perturbed power-supply, as given in (3.3), for $\hat{u}_{\text{DC}} = 0.1U_{\text{DC}}$, and $f_d = 10f_o$. Plot (b) illustrates the effect of power-supply output resistance, as shown in Figure 3.6, for $R_w = 0.1R$.

to as power supply pumping. Supply pumping is a common cause of distortion in HB converters with symmetrical power supplies and output filters or inductive loads. Supply pumping can be eliminated by applying a full-bridge (FB) configuration with single supply [39]. This configuration is also used for the experimental results in this thesis. For generality, however, most theory in this thesis is based on a single switching leg with symmetrical supplies. Note that, due to the steady-state assumption the effects of the reactive components are again neglected for harmonics of the reference waveform.

3.3.1 Modulator gain compensation

It has been shown in Section 3.3 that both perturbation of the power supply and finite output resistance result in significant distortion of the output of an SMPC. It can be shown relatively easily that power-supply-related distortion is eliminated by compensation of the modulation index with

$$m = \frac{2}{\mathring{u}_{\text{DC}}} u^*_{\text{sn}} \tag{3.11}$$

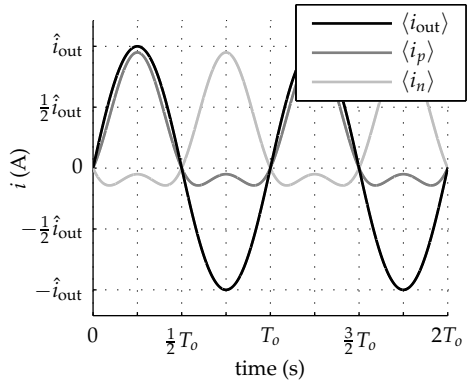


Figure 3.8: Moving-average output current ($\langle i_{\text{out}} \rangle$), and power-supply currents ($\langle i_p \rangle$ & $\langle i_n \rangle$), for a symmetrical power supply, as depicted in Figure 3.6.

where u^*_{sn} is the desired average switch-node voltage, and $\mathring{u}_{\text{DC}}$ is the estimated or measured power supply voltage. Substituting (3.11) into (3.3) results in

$$\langle u_{\text{sn}} \rangle = \frac{U_{\text{DC}} + \tilde{u}_{\text{DC}}}{\mathring{u}_{\text{DC}}} u^*_{\text{sn}}. \tag{3.12}$$

From (3.12) it can be seen that $\langle u_{\text{sn}} \rangle$ becomes equal to its desired value (u^*_{sn}) when $\mathring{u}_{\text{DC}}$ equals the perturbed power supply voltage ($U_{\text{DC}} + \tilde{u}_{\text{DC}}$).

The same also applies for the distortion caused by the output resistance of the power supply, as given in (3.7). By combining (3.7) with (3.11) using $\mathring{u}_{\text{DC}} = \langle u_p \rangle - \langle u_n \rangle$, of which in turn $\langle u_p \rangle$ and $\langle u_n \rangle$ can be expressed in terms of $\mathring{u}_{\text{DC}}$, it can be shown that the moving-average switch-node voltage after compensation of the modulation index is given by

$$\langle u_{\text{sn}} \rangle = \frac{R}{R + \frac{1}{2}R_w} u^*_{\text{sn}}. \tag{3.13}$$

From equation (3.13) it can be seen that the nonlinearity that is present in (3.7) is eliminated by the compensation, leaving only an increased output resistance of the power stage.

Ideally the baseband harmonics due to the perturbed power supply can be eliminated using the correction given in (3.11). However, in practice it is not possible to fully eliminate the distortion due to the power-supply nonlinearities. Figure 3.9a and Figure 3.9b depict the same cases as Figure 3.7 but with correction of the modulator gain, as described in Figure 3.10. The compensation is updated only twice per switching cycle (T_{sw}), which is usual practice in DPWM converters.

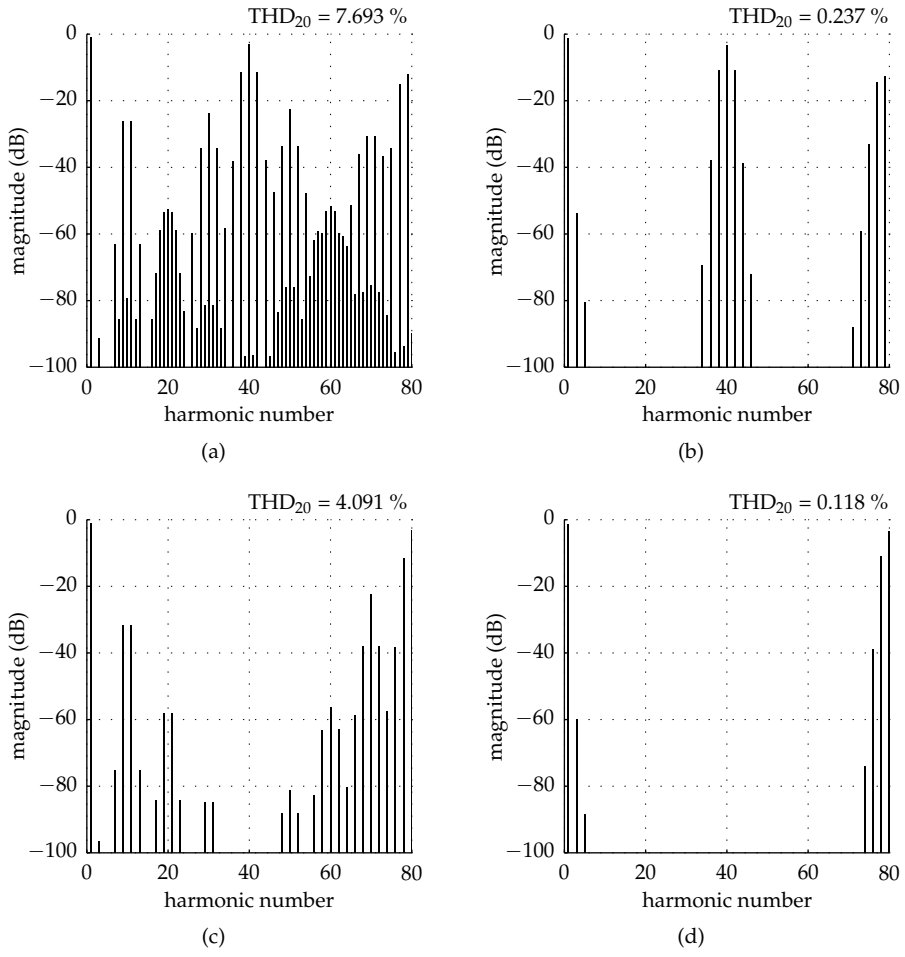


Figure 3.9: Magnitude spectrum of u_{sn} for double-edge natural-sampled modulation, as depicted in Figure 3.7, but with correction of the modulator gain, as depicted in Figure 3.10, to compensate for power supply perturbation. Plot (a) shows the effect of a perturbed power-supply, for $\hat{u}_{\text{DC}} = 0.1U_{\text{DC}}$, and $f_d = 10f_o$, after compensation, and (b) illustrates the effect of power-supply output resistance, for $R_w = 0.1R$, after compensation. Note that the THD in (a) is higher than in Figure 3.7a. Plots (c) and (d) depict the spectra under the same conditions as in (a) and (b) respectively. However, here f_{sw} and consequently the update frequency of the compensation is doubled.

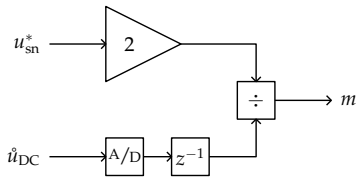


Figure 3.10: Schematic diagram of the modulator gain compensation used to correct for perturbation of the power supply voltage.

When comparing Figure 3.9a with Figure 3.7a it can be seen that the modulator gain correction results in more distortion. This is not the case for the effect of the power supply resistance. Figure 3.9b and Figure 3.7b show the effect of R_w with and without gain compensation, respectively. The first spurious spectral component is reduced by 12 dB compared to the uncompensated case. The imperfections of the compensation, and the increased distortion in the first case, are caused by the delay between measurement and compensation action due to the sampling process. The ratio between the cycle time of the disturbances ($1/f_d$) and the delay in the gain compensation ($\frac{1}{2}T_{sw}$) should, therefore, be chosen sufficiently large to keep the error of the gain compensation within desired bounds.

Figure 3.9c and Figure 3.9d depict the same results with gain compensation, however, now with two times higher switching frequency, and consequently two times lower T_{sw}. The dominant spurious harmonic components are approximately 6 dB lower compared to the results in Figure 3.9a and Figure 3.9b. Moreover, when comparing Figure 3.9d with Figure 3.7b it can be seen that even the effects of the power supply perturbation are reduced due to the gain compensation.

Other methods exist to compensate for the power supply intermodulation effects, e.g. in [117] the analog-generated carrier is augmented using the supply voltage. This method is especially suited for low-voltage amplifiers with analog carrier generation.

The effectiveness of modulator gain compensation highly depends on the accuracy of the measurements and delay between measurement and compensation action. Therefore, compensation of the power supply is rarely implemented in practice for the purpose of distortion reduction.

3.4 The end stage

The end stage consists of the semiconductor switches and diodes in the switching legs, the associated gate driver circuits, and the input and output filters. All components in the end-stage effect the output quality of an SMPC. Nonlinearity of the passive components in the filters leads to harmonic distortion, as pointed out in [84], and further detailed in [46]. Jitter of the gating signals leads to noise and distortion. Furthermore, in order to prevent aliasing effects, clocked digital gate-drivers should be synchronized with the PWM carrier clock, and the PWM clock should be synchronized to the clock of the incoming reference signal.

The effects of nonlinearities of the filter components, distortion due to the gate drivers, and switching delay is not further investigated in this section. This section only treats the distortion effects caused by blanking time and the forward voltages and on resistances of the semiconductor devices, excluding the effects of the switching transients[2].

3.4.1 Blanking time

For a switching leg with ideal switches, as depicted in Figure 3.1, seven operating modes can be identified. These operating modes are discussed in detail in [6]. The seven operating modes can be classified as:

1. strictly positive inductor current
2. positive average discontinuous inductor current, with commutation to D_1
3. positive average discontinuous inductor current, with commutation to D_2
4. zero-voltage-switching region
5. negative average discontinuous inductor current, with commutation to D_1
6. negative average discontinuous inductor current, with commutation to D_2
7. strictly negative inductor current

This section draws on the analysis presented in [6], but uses the notation applied in this thesis. The following analysis of the seven operating modes is only valid for steady-state and $T_{bt}/T_{sw} < 0.25$.

[2]For reference, an analysis of the first-order effects of switching transients is presented in [109].

Continuous inductor current

Figure 3.11a depicts the gating signals, inductor current ($i_{L_{\mathrm{HB}}}$), and switch-node voltage (u_{sn}) for strictly positive inductor current, that is

$$\langle i_{L_{\mathrm{HB}}} \rangle > \Delta i_{L_{\mathrm{HB}_1}} \tag{3.14}$$

where $\Delta i_{L_{\mathrm{HB}_1}}$ represents the inductor current ripple amplitude for strictly positive current, as given from

$$\Delta i_{L_{\mathrm{HB}_1}} = \hat{\Delta} i_{L_{\mathrm{HB}}} \left(1 - \left(m - \frac{2T_{\mathrm{bt}}}{T_{\mathrm{sw}}} \right)^2 \right) \tag{3.15}$$

with

$$\hat{\Delta} i_{L_{\mathrm{HB}}} = \frac{U_{\mathrm{DC}}}{8 L_{\mathrm{HB}} f_{\mathrm{sw}}} \tag{3.16}$$

which represents the maximum inductor current ripple amplitude.

From Figure 3.11a it can be seen that the inductor current commutates to the low-side diode (D_1) during the blanking times. As a result, the moving-average output voltage ($\langle u_{\mathrm{out}} \rangle$) is lower than expected from the set modulation index, and is calculated to be

$$\langle u_{\mathrm{out}_1} \rangle = \tfrac{1}{2} U_{\mathrm{DC}} \left(m - \frac{2T_{\mathrm{bt}}}{T_{\mathrm{sw}}} \right) \tag{3.17}$$

being a factor $T_{\mathrm{bt}} U_{\mathrm{DC}} / T_{\mathrm{sw}}$ lower than expected when the effect of blanking time is neglected.

The switching waveforms for strictly negative inductor current are depicted in Figure 3.11b. Strictly negative inductor current occurs when

$$\langle i_{L_{\mathrm{HB}}} \rangle < -\Delta i_{L_{\mathrm{HB}_7}} \tag{3.18}$$

where $\Delta i_{L_{\mathrm{HB}_7}}$ is the inductor current ripple amplitude for strictly negative current, which in turn is given by

$$\Delta i_{L_{\mathrm{HB}_7}} = \hat{\Delta} i_{L_{\mathrm{HB}}} \left(1 - \left(m + \frac{2T_{\mathrm{bt}}}{T_{\mathrm{sw}}} \right)^2 \right). \tag{3.19}$$

For strictly negative inductor current, commutation to the high-side diode (D_2) occurs during the blanking times. As a result, the moving-average output voltage

is determined by

$$\langle u_{\text{out}_7} \rangle = \tfrac{1}{2} U_{\text{DC}} \left(m + \frac{2T_{\text{bt}}}{T_{\text{sw}}} \right) \tag{3.20}$$

being $T_{\text{bt}}/T_{\text{sw}} U_{\text{DC}}$ higher than expected.

Figure 3.11c depicts the case when $i_{L_{\text{HB}}}$ is positive when switch S_1 is turned off, and negative when S_2 is turned off. As a result, during the blanking times, the current commutates to the diode in parallel with the switch that is going to be turned on. This leads to zero voltage across a switch when it is turned on under the condition that the diode remains conducting during the blanking time. This mode of operation is called zero-voltage switching (ZVS).

Since the inductor current always commutates to the diode in parallel to the switch that is going to be turned on, no voltage is lost or gained, resulting in the following expression for the moving-average output voltage

$$\langle u_{\text{out}_4} \rangle = \tfrac{1}{2} U_{\text{DC}} m. \tag{3.21}$$

This operating mode requires the moving-average inductor current to be within the interval

$$-a + 2b\,(1+m) < \langle i_{L_{\text{HB}}} \rangle < a - 2b\,(1-m) \tag{3.22}$$

with

$$a = \hat{\Delta} i_{L_{\text{HB}}} \left(1 - m^2 \right)$$
$$b = \hat{\Delta} i_{L_{\text{HB}}} \frac{2T_{\text{bt}}}{T_{\text{sw}}}.$$

Discontinuous inductor current

Figure 3.12 depicts the operating modes with discontinuous inductor currents, which occur during the transitions between the three operating modes with continuous inductor currents. From Figure 3.12 it can be seen that the switch-node voltage is equal to the periodic average output voltage ($\langle u_{\text{out}} \rangle$) when $i_{L_{\text{HB}}}$ clamps to zero.

Figure 3.12a depicts the switching waveforms for operating mode 2. In mode 2 S_2 is turned off when $i_{L_{\text{HB}}} > 0$, and as a result the inductor current commutates to D_1 before discontinuous conduction mode (DCM) occurs. For this operating

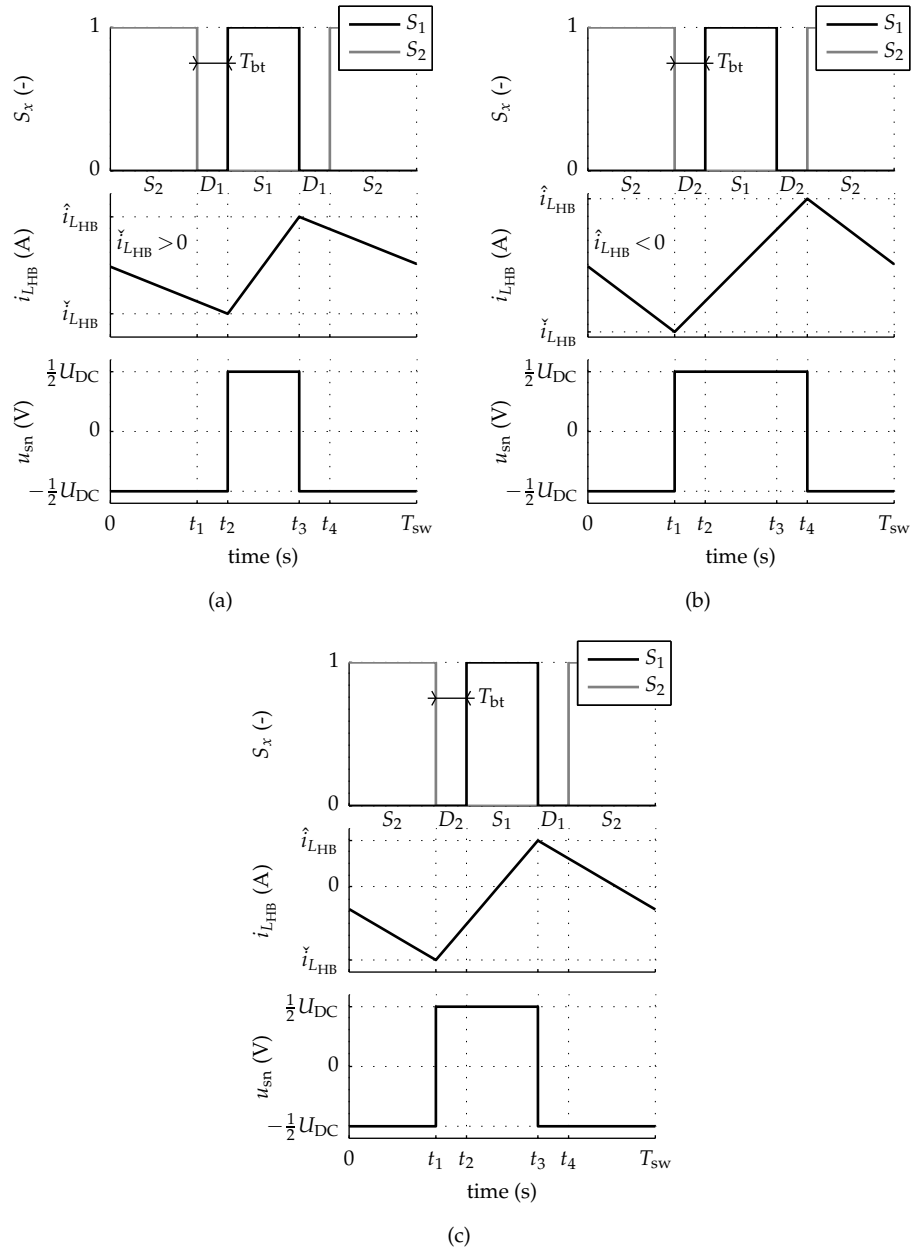


Figure 3.11: Switching waveforms for the conventional HB converter, as illustrated in Figure 3.1, operated with blanking time. Plots (a) and (b) are for strictly positive and negative current, respectively, and (c) is for ZVS, involving natural commutation to a diode after turn-off of a switch.

mode the moving-average inductor current is within

$$a - b\,(1-m) < \langle i_{L_{\mathrm{HB}}} \rangle \leq \Delta i_{L_{\mathrm{HB}_1}} \tag{3.23}$$

and the moving-average output voltage for this operating mode is given by

$$\langle u_{\mathrm{out}_2} \rangle = \tfrac{1}{2} U_{\mathrm{DC}} \frac{\left(m - \frac{2T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\right)^2 + 2m - \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}} + 1 - \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}{\left(m - \frac{2T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\right)^2 + 2m - \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}} + 1 + \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}. \tag{3.24}$$

The switching waveforms for operating mode 3 are shown in Figure 3.12b. At the moment that S_2 is turned off, $i_{L_{\mathrm{HB}}}$ is smaller than zero. As a result the current commutates to D_2, whereafter DCM occurs. The moving-average inductor current for this operating mode is within

$$a - 2b\,(1-m) \leq \langle i_{L_{\mathrm{HB}}} \rangle \leq a - b\,(1-m) \tag{3.25}$$

and the moving-average output voltage for this operating mode is given by

$$\langle u_{\mathrm{out}_3} \rangle = \tfrac{1}{2} U_{\mathrm{DC}} \frac{3m^2 - 2m - 1 + \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\,(1-m) + \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}{m^2 + 2m - 3 + \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\,(1-m) + \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}. \tag{3.26}$$

Figure 3.12c and Figure 3.12d illustrate the DCM operating modes for negative $\langle i_{L_{\mathrm{HB}}} \rangle$. Operating mode 5 occurs when the inductor current is within the interval

$$-a + b\,(1+m) \leq \langle i_{L_{\mathrm{HB}}} \rangle \leq -a + 2b\,(1+m) \tag{3.27}$$

and the moving-average output voltage for operating mode 5 is given by

$$\langle u_{\mathrm{out}_5} \rangle = -\tfrac{1}{2} U_{\mathrm{DC}} \frac{3m^2 + 2m - 1 + \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\,(1+m) - \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}{m^2 - 2m - 3 + \frac{4T_{\mathrm{bt}}}{T_{\mathrm{sw}}}\,(1+m) - \frac{\langle i_{L_{\mathrm{HB}}} \rangle}{\hat{\Delta} i_{L_{\mathrm{HB}}}}}. \tag{3.28}$$

Operating mode 6 occurs when $\langle i_{L_{\mathrm{HB}}} \rangle$ is within

$$\Delta i_{L_{\mathrm{HB}_7}} \leq \langle i_{L_{\mathrm{HB}}} \rangle < -a + b\,(1+m) \tag{3.29}$$

and the corresponding moving-average output voltage is given by

$$\langle u_{\text{out}_6} \rangle = -\tfrac{1}{2} U_{\text{DC}} \frac{\left(m + \frac{2T_{\text{bt}}}{T_{\text{sw}}}\right)^2 - 2m - \frac{4T_{\text{bt}}}{T_{\text{sw}}} + 1 + \frac{\langle i_{L_{\text{HB}}} \rangle}{\tilde{\Delta} i_{L_{\text{HB}}}}}{\left(m + \frac{2T_{\text{bt}}}{T_{\text{sw}}}\right)^2 - 2m - \frac{4T_{\text{bt}}}{T_{\text{sw}}} + 1 - \frac{\langle i_{L_{\text{HB}}} \rangle}{\tilde{\Delta} i_{L_{\text{HB}}}}}. \tag{3.30}$$

The effect of blanking time on the output voltage quality

Figure 3.13a depicts the normalized output voltage as function of the normalized current for different modulation indices, and illustrates the voltage loss and gain that occurs during the transitions between the operating modes for 8 % blanking time. The moving-average output voltage for the transitions between the operating modes with continuous inductor current, as given by equations (3.24), (3.26), (3.28), and (3.30) depends nonlinearly on the modulation index. The output voltage does not depend on the inductor current for the operating modes with continuous current, i.e. modes 1, 4, and 7. The maximum and minimum modulation indices are limited by the points where the current required to transit from operating mode 4 to 3 equals the current required to go from mode 4 to 5, and are calculated to be

$$\hat{m} = \sqrt{1 - \frac{4T_{\text{bt}}}{T_{\text{sw}}}} \tag{3.31a}$$

$$\check{m} = -\sqrt{1 - \frac{4T_{\text{bt}}}{T_{\text{sw}}}} \tag{3.31b}$$

where $\hat{m}$ and $\check{m}$ respectively represent the maximum and minimum modulation index.

Figure 3.13b depicts the normalized voltage error due to blanking time as function of the normalized current, for multiple modulation indices. The transitions between the operating modes are indicated by thin black lines. From Figure 3.13b, and equations (3.17) and (3.20), it can be seen that the moving-average output voltage differs $\mp U_{\text{DC}} T_{\text{bt}} / T_{\text{sw}}$ from the expected value for strictly positive and negative current, respectively. For ZVS no voltage error occurs, as can also be seen from Figure 3.13b, and (3.21). The moving-average voltage error due to blanking

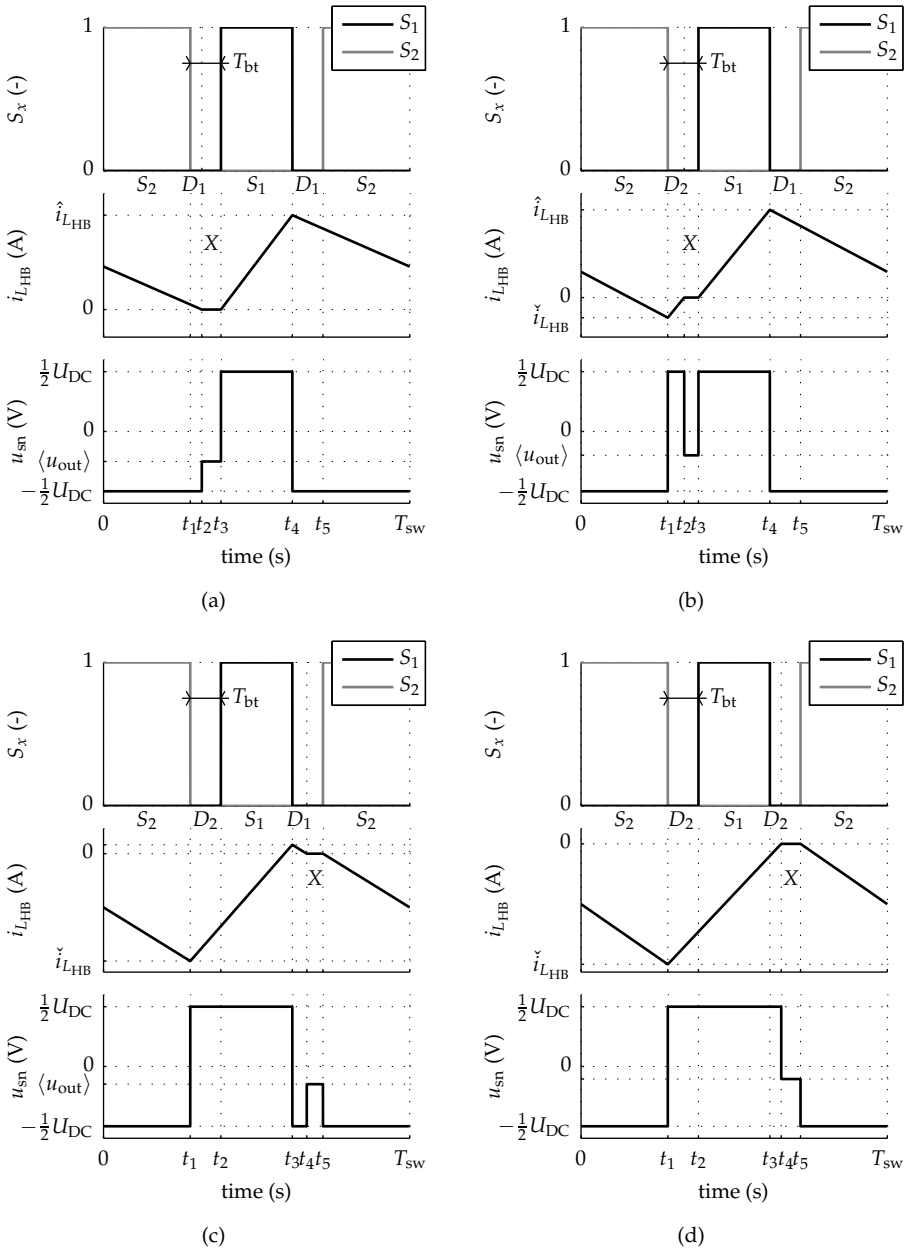


Figure 3.12: Switching waveforms for the conventional HB with blanking time. This figure illustrates the different cases of DCM that can occur during (a & b) the transition from strictly positive current to the ZVS region and vice versa, and (c & d) strictly negative current to the ZVS region and vice versa.

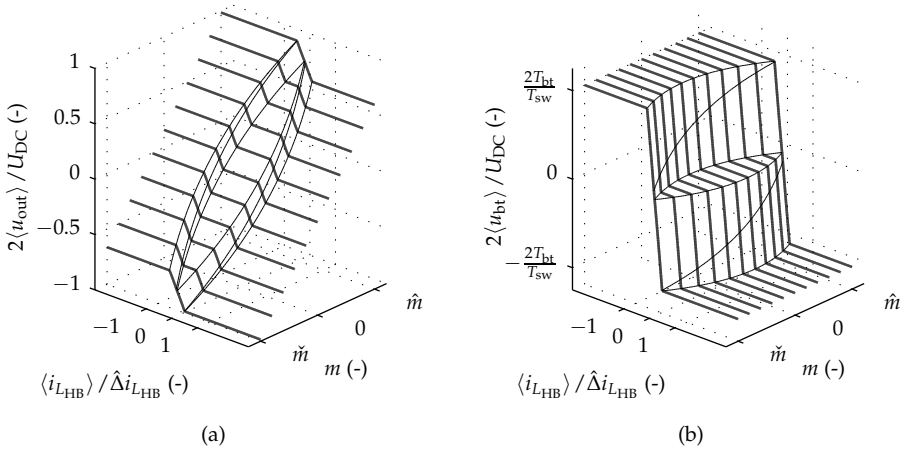


Figure 3.13: The normalized moving-average output voltage ($\langle u_{\text{out}}\rangle / \frac{1}{2} U_{\text{DC}}$) (a), and voltage error due to blanking time (b), as function of the normalized moving-average filter inductor current ($\langle i_{L_{\text{HB}}}\rangle / \hat{\Delta} i_{L_{\text{HB}}}$) for varying modulation index (m) with 8 % blanking time. The transitions between the operating modes are indicated with thin lines.

time for the operating modes with continuous inductor current is given by

$$\langle u_{\text{bt}}\rangle = \begin{cases} -\frac{T_{\text{bt}}}{T_{\text{sw}}} U_{\text{DC}}, & \text{for (3.14)} \\ 0, & \text{for (3.22)} \\ \frac{T_{\text{bt}}}{T_{\text{sw}}} U_{\text{DC}}, & \text{for (3.18)} \end{cases} \tag{3.32}$$

where u_{bt} is the voltage error due to blanking time.

The voltage error as function of the inductor current for the discontinuous operating modes, as given in equations (3.24), (3.26), (3.28), and (3.30), appears almost linear instead of second order. Therefore, when assuming instantaneous switching, the voltage error due to blanking time can be approximated piecewise linearly with relatively small errors. This was also shown in [90], in which a piecewise linear feed forward compensation was suggested to compensate the voltage error due to blanking time.

3.4.2 Semiconductor device parameters

The previous analysis of voltage error due to blanking time does not include the effect of the forward voltages and on resistances of the switches and diodes. Figure 3.14 depicts the model used to analyze the impact of forward voltages (V_{on} & V_f) and on resistances (R_{on} & R_f) of the switches and diodes, respectively. Nonlinear effects and the parasitic switch-node capacitances are neglected. As indicated with the arrowheads in the switch symbols, the model is only valid for unipolar current switches. Examples are insulated-gate bipolar-transistors (IGBTs) or metal-oxide semiconductor field-effect transistors (MOSFETs) from which the integrated antiparallel diodes are blocked and bypassed with additional discrete diodes[3].

Figure 3.15 depicts the switching waveforms for strictly positive and negative inductor current, including the effects of the voltages and resistances indicated in Figure 3.14. The resulting voltage error, for strictly positive and negative current, is given by

$$\begin{aligned}\langle u_{\text{err}} \rangle = {} & V_b m - \left(R_{L_{\text{HB}}} + R_a\right) \langle i_{L_{\text{HB}}} \rangle - \frac{2T_{\text{bt}}}{T_{\text{sw}}} R_b \langle i_{L_{\text{HB}}} \rangle + \dots \\ & \begin{cases} -V_a + R_b \langle i_{L_{\text{HB}}} \rangle m - \frac{T_{\text{bt}}}{T_{\text{sw}}} \left(U_{\text{DC}} + 2V_b\right), & \text{for strictly positive } i_{L_{\text{HB}}} \\ V_a - R_b \langle i_{L_{\text{HB}}} \rangle m + \frac{T_{\text{bt}}}{T_{\text{sw}}} \left(U_{\text{DC}} + 2V_b\right), & \text{for strictly negative } i_{L_{\text{HB}}} \end{cases}\end{aligned} \tag{3.33}$$

with

$$\begin{aligned} V_a &= \tfrac{1}{2}\left(V_f + V_{\text{on}}\right) \\ V_b &= \tfrac{1}{2}\left(V_f - V_{\text{on}}\right) \\ R_a &= \tfrac{1}{2}\left(R_f + R_{\text{on}}\right) \\ R_b &= \tfrac{1}{2}\left(R_f - R_{\text{on}}\right) \end{aligned}$$

and where $R_{L_{\text{HB}}}$ represents the series resistance of the filter inductor L_{HB}.

From (3.33) it can be seen that only the last two terms, which depend on the sign of the current, are nonlinear and lead to harmonic distortion. The voltage error due to the sum of the forward voltages of the switches and diodes (V_a) has the same effect as the error due to blanking time. The voltage error of the other

[3]This configuration is commonly applied in high-power MOSFET converters to reduce diode reverse recovery losses [29, page 68].

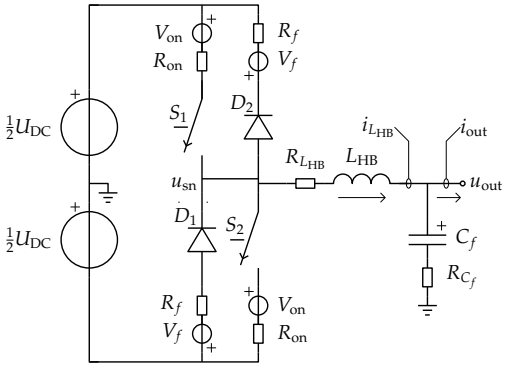


Figure 3.14: Schematic diagram of a conventional switching leg with unipolar current switches with forward voltage and on resistance (V_{on} & R_{on}), diodes with forward voltage and on resistance (V_f & R_f), and series resistances of the filter inductor and capacitor ($R_{L_{HB}}$ & R_{C_f}).

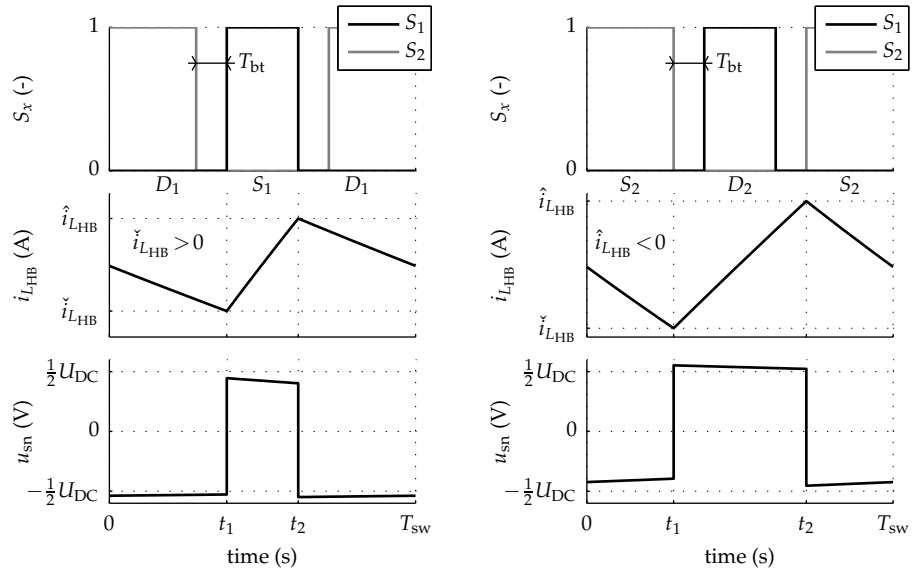


Figure 3.15: Switching waveforms for the conventional HB with blanking time for strictly positive (a) and strictly negative current (b), respectively.

operating modes cannot be expressed analytically.

Figure 3.16a depicts simulated waveforms of the filter inductor current ($i_{L_{\mathrm{HB}}}$), output current (i_{out}), and the output voltage (u_{out}) for a conventional switching leg, as depicted in Figure 3.14. The output is modulated sinusoidally to 75 % of the output voltage range with frequency $f_{\mathrm{sw}}/1000$, without feedback. The forward voltages of the switches and diodes are set to 1.5 V. Because V_f and V_{on} are assumed to have the same values, the combined effect is identical to the distortion introduced by blanking time. The blanking time is set such that the combined voltage error is 3 % of U_{DC}, which is typical in high-power converters.

The transitions between the modes with continuous $i_{L_{\mathrm{HB}}}$ result in small time intervals with relatively stable i_{out} during the zero crossings of $i_{L_{\mathrm{HB}}}$. This effect is known as zero-current clamping and is described extensively in the literature [19, 118, 119]. Basically the filter inductor current clamps to zero until the modulation index is increased to compensate for the voltage loss which occurs due to the nonlinear term of (3.33).

Figure 3.16b depicts the resulting magnitude spectrum of the switch-node voltage (u_{sn}). From Figure 3.16b it can be seen that the combination of blanking time and forward voltage results in significant distortion. The spectrum contains only odd harmonics and the resulting THD is in the range of several percent. The THD is defined as in (3.1).

In practice the blanking time is several percent of T_{sw}, and can in some applications reach up to 5 % [67, chapter 8]. The simulation results depicted in Figure 3.16, with 1.5 % blanking time, illustrate what can be expected when using conventional PWM switching legs.

The output spectrum in Figure 3.16b is obtained by means of simulation. There are many literature references on analytical expressions for the output spectrum or THD due to blanking time. Most of these techniques rely on Fourier analysis, and do not include the effects of the inductor current ripple amplitude, nor the resulting zero-current clamping effect [47, 68, 129]. In [74, chapter 4] and [71] a method is proposed to analytically determine the THD due to blanking time, including the effect of the inductor current ripple amplitude. However, these methods are only valid for resistive loads. Analytical expressions for the distortion due to blanking time are not treated further in this thesis.

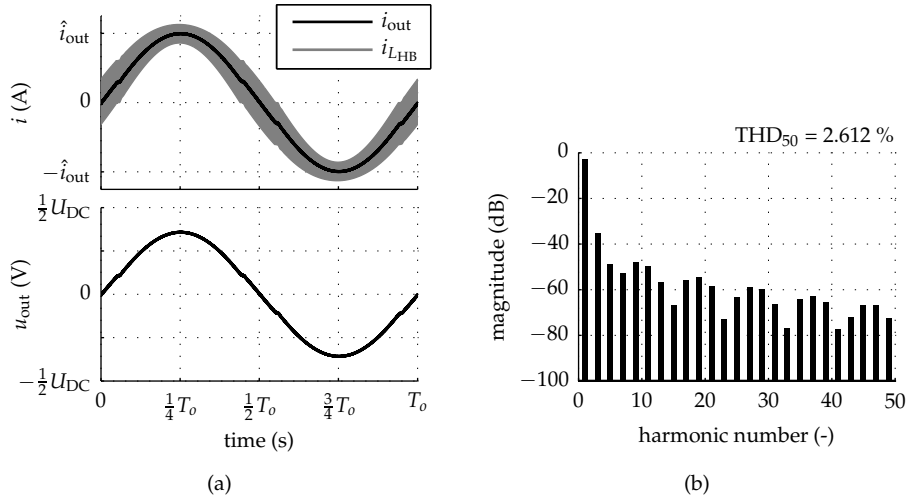


Figure 3.16: Output waveforms for the conventional HB with 1.5 % blanking time and 1.5 V forward voltage for the semiconductor switch and diode (a) and the corresponding magnitude spectrum of u_{sn} (b).

3.5 Ranking of the various error contributions

The previous sections highlighted the most dominant sources of voltage errors in PWM converters. These originate from the modulation strategy, external power supply, and the switching leg itself.

In Section 3.2 it was explained that the error due to PWM modulation can be made arbitrarily small by increasing the ratio between the switching and output frequency (f_{sw}/f_o), and the ratio between the PWM clock and switching frequency ($f_{\text{clk}}/f_{\text{sw}}$). At the cost of more high-frequency noise, noise shaping can be used to improve the baseband performance of the PWM modulator [89]. In practice more than 8 bits resolution can be obtained relatively easily, resulting in less than 0.5 % error.

The external power supply is one of the most dominant sources of distortion in PWM converters. However, this kind of distortion is also present in linear amplifiers. The impact on the output voltage quality is dependent on the power supply and its output impedance. In Section 3.3 it is shown that the voltage error due to the power supply can be compensated using the measured supply voltage when the measurement delay is significantly smaller than the output cycle time (T_o).

Several sources of distortion that originate in the switching leg have been high-

lighted in Section 3.4. Blanking time is, in practice, the most dominant source of switching-leg induced distortion, typically producing voltage errors in the order of several percent of the output voltage range. Furthermore, in case of unipolar-current switches, as given in (3.33), the forward voltages and on resistances of the switches and diodes also cause significant distortion. However, this effect is usually smaller than the distortion due to blanking time, and typically less than one percent.

Blanking time is identified as the most dominant source of output signal distortion in SMPCs, followed by PWM resolution, and, in case of unipolar current switches, the forward voltages of the semiconductor devices. Distortion due to the power supply is not PWM-converter specific, and not detailed further in this thesis. The remainder of this thesis focuses on the elimination of zero-crossing distortion due to blanking time and forward voltages.

3.6 Eliminating blanking-time-related distortion

Blanking time is one of the most dominant sources of output voltage distortion for PWM amplifiers. Especially, high-precision applications, which require accurate input current, like short-stroke linear mechanical actuators for wafer steppers, gradient coils for magnetic resonance imaging (MRI) systems, and studio-quality audio suffer from the blanking-time effect.

Feedback is normally applied in SMPCs to reject disturbances. The impact of blanking time can indeed be reduced by feedback. However, due to the extremely fast change of the output voltage as a function of current and modulation index, it is not practical to eliminate the distortion due to blanking time with feedback only.

Extensive studies have been done on the elimination [133], minimization [3], and compensation [40, 49, 56, 78, 90, 118, 119, 130] of blanking time in PWM converters. Most of these techniques rely on the detection of the polarity of the sampled inductor current of the converter. This can be done by:

- Directly measuring the current
- Reconstruction of the current, using an observer
- Feedforward of the setpoint current
- External circuits to detect switch-node commutation

Most methods assume instantaneous switching and neglect the switching transients. A more complete model including switch-node commutation is treated

in [118], however, the method is designed for 3-phase machines and requires significant computation time. The inductor current ripple is often neglected in the compensation. Especially for converters with relatively large inductor current ripple, it is essential to include this ripple in the compensation scheme.

In [90] a compensation scheme was suggested that includes the inductor current ripple, and in [56] a more advanced model of the switch-node commutation is added. All techniques mentioned above achieve a reduction of the distortion. However, due to errors in the detection of current polarity and DCM during zero crossings, they are not capable of completely removing it.

Different modulation techniques have been suggested which do not suffer from blanking time effects [3, 18, 49, 133], however, these methods also rely on the polarity of the current and do not completely remove all the effects of blanking time. In [5, 55, 85, 134] the amount of blanking time is reduced (adaptively or actively) to the absolute minimum at the cost of increased losses.

In [57] hysteresis current control is proposed as a solution for all types of distortion in switching converters. However, hysteresis current control does not completely eliminate blanking-time-related distortion, unless the hysteresis levels are chosen such that the high-side switch is turned off when the inductor current is positive, and the low-side switch is turned off when the inductor current is negative. This hysteresis current control scheme is known as the resonant-pole inverter (RPI) and has been the subject of many papers, which include [17, 22, 24].

The RPI features ZVS, i.e. a switch is turned on and off when the voltage across the device is nearly zero, and therefore does not suffer from blanking-time-related distortion. However, to achieve ZVS the RPI requires considerable circulating current. In [80] the modulation method of the RPI was adapted to reduce the amount of circulating current, and, consequently, the conduction losses. Later in [95], a method was proposed to ensure ZVS when the output clamps to the supply voltage.

To achieve zero-voltage turn-off in RPIs the slew rate of the switch-node voltage is limited by adding capacitance in parallel with the switches[4]. The resulting lower slew rate during commutation leads to reduced electromagnetic interference (EMI). The result is that a well designed RPI does not require additional EMI filtering, as is normally required in conventional PWM converters. The slew rate of the switching transients, however, is strongly dependent on the operating point of the converter and adds significant distortion.

[4]Practical switching devices have parasitic capacitance. However, in many practical implementations the parasitic capacitance of the switches is not sufficient to ensure zero-voltage turn-off. Therefore, additional discrete capacitors are used.

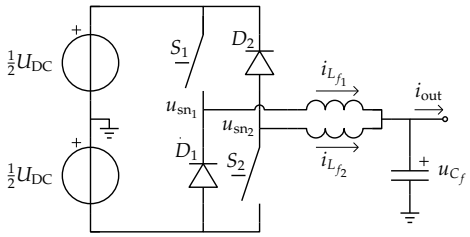


Figure 3.17: Practical implementation of a dual-buck switching leg.

In practice, the output-voltage quality of RPIs is better than that of conventional PWM converters, but not sufficient for many high-precision applications. Furthermore, the hysteresis control scheme of an RPI results in variable switching frequency and is hard to implement digitally. The RPI is, therefore, rarely used in industry.

The RPI is based on a conventional switching leg with two stacked switches, and even though it does not suffer from blanking-time-related distortion, it still requires blanking time to prevent short-circuits of the DC bus when switching. As a result the RPI is not robust for shoot-through current, i.e. accidental turn-on of a switch, and does not solve the reliability issue in high-precision equipment that is highlighted in Chapter 1.

Topologies like the current-source inverter (CSI) are robust for shoot-through but fail when a switch accidentally opens. Circuits like the Z-source converter [79], the switched boost converter [66], the series-resonant buck-boost inverter [125], and the Ćuk converter [64] are robust for shoot-through, but have a nonlinear relation between input and output. This in turn leads to harmonic distortion in the output stage.

In [137] a circuit consisting of two parallel-connected down converters, one for positive current and one for negative current, is presented as a high-performance converter that is robust for shoot-through, does not suffer from blanking-time-related distortion, and has a linear relation between input and output. The remainder of this thesis will focus on this so-called dual-buck (DB) topology, as shown in Figure 3.17.

Part II

A robust power converter with high signal-quality

Chapter 4

Robust topologies

"In all things success depends on previous preparation, and without such previous preparation there is sure to be failure."

(Confucius)

Abstract — In Part I it is shown that blanking time is one of the most significant sources of distortion in pulse-width-modulated switched-mode power amplifiers. Over time different topologies have been proposed that do not suffer from this effect. However, all have either a nonlinear relation between input and output, or are not robust for shoot-through current. This chapter starts with the basic canonical cell and extends it to a topology that does not suffer from distortion due to blanking time, is robust for shoot-through current, and has a linear relation between input and output.

Contributions of this chapter are published in:

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Elimination of zero-crossing distortion for high-precision amplifiers," in *Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2011, pp. 3370–3375.
- J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. A. Lomonova, "High precision switched-mode amplifier with an auxiliary bias circuit," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.
- E. Lemmen, J. M. Schellekens, C. G. E. Wijnands, and J. L. Duarte, "The extra L opposed current converter," in *Proceedings of the 29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 1304–1311.

4.1 Introduction

The conventional switching leg or canonical cell [48], as depicted in Figure 4.1a is the basic building block of many converter topologies. When only one canonical cell is considered, four unique configurations exist, where it should be noted that the Ćuk and buck-boost converter, and the boost and buck converter are dual forms of each other [20]. These converters, when built from the canonical cell, share the fact that they support bidirectional power flow. It can be shown that the canonical cell is self-dual and is, therefore, invariant to the duality transform in terms of its behavior [20].

Many converters only allow unidirectional power flow as they are not built from the canonical cell pur sang. In [45], two alternative basic switching cells are proposed, both based on a combination of an active switch and a diode. These cells, which are depicted in Figure 4.1b and Figure 4.1c, are known as the P-cell and N-cell. Both cells share the fact that they allow only unidirectional power flow and that they are each other's dual form. The presented cells result in eight unique unidirectional converters [45].

Nowadays when implementing a canonical cell, semiconductor switches, such as MOSFETs and IGBTs are preferred. These switching devices have a finite turn-on and turn-off time, requiring a blanking time between the gating signals to prevent short circuit when switching. In practice, antiparallel diodes are present, as depicted in Figure 4.1d, to offer a so-called freewheeling path for the inductor current during the blanking time. This works satisfactory under normal operating conditions. However, accidental turn-on of a switch can result in a short circuit. When a voltage source is present at the input of the cell, a large "shoot-through" current occurs, which results in increased losses and/or device failure.

In Part I it is shown that the blanking time is one of the dominant sources of distortion for PWM SMPCs. Different topologies and modulation strategies that solve the blanking time issue were identified [17,22,24]. Some of the presented topologies were shown to be robust for shoot-through current [64,66,79,125]. However, none of the converters share the four features required for a high-efficiency, high-precision, robust power amplifier:

- no distortion due to blanking time,
- robust for accidental turn-on of switching devices,
- a linear relation between input and output,
- bidirectional power flow capability.

There are two candidates in Figure 4.1 that satisfy three of these features, being

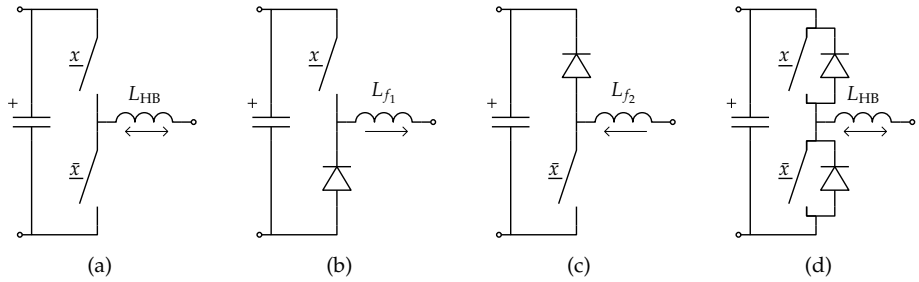


Figure 4.1: Basic switching cells with, (a) canonical cell, (b) P-cell, (c) N-cell, and (d) practical canonical cell.

the P-cell, and the N-cell. These both do not require blanking time due to the fact that there is always a blocking diode in the possible shoot-through path, being therefore also robust for accidental switch turn-on. Furthermore, they share a linear relation between switch duty ratio and output voltage when operating in continuous conduction mode, as will be shown later in this chapter. However, the topologies allow only unidirectional power flow, i.e. positive power flow for the P-cell, and negative power flow for the N-cell. Combining two unidirectional complementary switching legs (i.e. the P-cell and the N-cell) by means of parallel connection, as depicted in Figure 4.2a, results in a topology with bidirectional power flow capability [116].

The resulting cell in Figure 4.2a is basically a split version of the fundamental canonical cell as it is depicted in Figure 4.1d. Due to the diode in each leg, only positive current can flow through inductor L_{f_1}, and only negative current through L_{f_2}.

Usually, in parallel-connected switching cells the output current i_{out} is equally distributed over the inductors in order to evenly distribute losses [10]. This is of course not possible in case of the parallel-connected P-cell and N-cell, since each leg will only be able to process current of one polarity.

The most basic use of the circuit shown in Figure 4.2a would be to use the P-leg for positive current and the N-leg for negative current. However, severe distortion is produced at near-zero current levels, because each leg will eventually operate in DCM.

In order to avoid discontinuous-current operation, and consequently distortion, a bias current should be added to each leg as depicted in Figure 4.2b. This bias current should be chosen such that the currents supplied by the P-cell and the N-cell do not become discontinuous. The resulting topology has two independent auxiliary bias current sources.

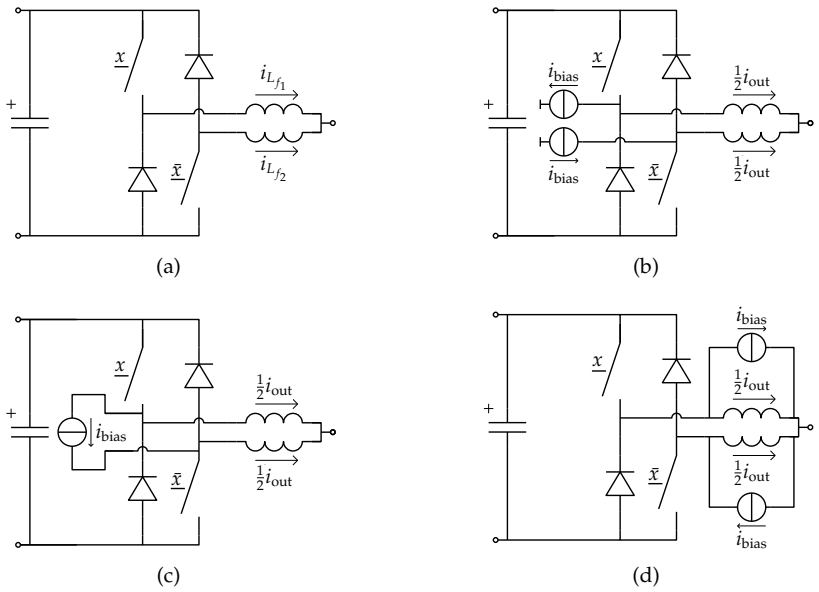


Figure 4.2: Parallel connection of a P-cell and an N-cell (a), with independent auxiliary bias (b), with differential bias (c), and with integrated bias (d).

By applying the dual form of the Blakesley transformation, as presented in [8] and [23, chapter 10], the two auxiliary current sources, depicted in Figure 4.2b, can be connected in series and combined, as depicted in Figure 4.2c. The resulting circuit has a differentially connected bias source.

Alternatively, the dual form of the Blakesley transformation can also be applied to Figure 4.2b by connecting the common node of the current sources to the output terminal of the parallel connected P- and N-cell, as depicted in Figure 4.2d. Now the parallel-connected P- and N-cell are integrated with the bias sources, which is basically the same as the circuit shown in Figure 4.2a, with

$$i_{L_{f_1}} = \tfrac{1}{2} i_{\text{out}} + i_{\text{bias}} \tag{4.1a}$$

$$i_{L_{f_2}} = \tfrac{1}{2} i_{\text{out}} - i_{\text{bias}} \tag{4.1b}$$

where i_{out} is output current of the converter, and i_{bias} is the circulating current required to prevent DCM.

The current sources in Figure 4.2 can be realized using inductors, as depicted in Figure 4.3. Figure 4.3c has two parallel current paths that cannot be regulated independently. It is, therefore, not possible to concentrate the bias current to one of these parallel paths. The distribution of the current over the parallel paths can

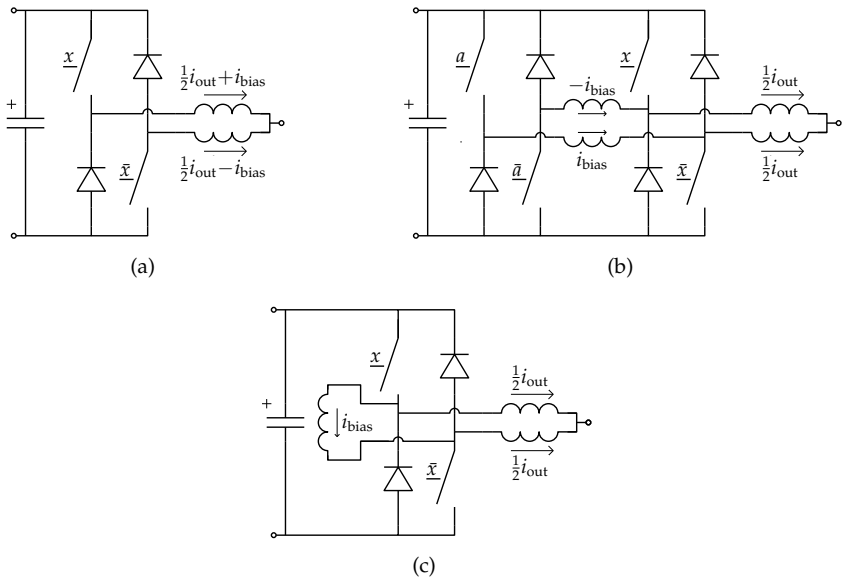


Figure 4.3: Practical realizations of the parallel-connected P- and N-cell, with integrated bias inductors (a), auxiliary bias inductors (b), and differentially connected bias inductor (c).

be set by proper selection of the inductance values of the three inductors as shown in [50]. Of course it is possible to eliminate the parallel paths by application of the Δ-Y transform to the three inductors, resulting in an additional node voltage. However, both the Δ- and Y-connected options are functionally equivalent to the circuit of Figure 4.2a with coupled inductors. This will be treated in more detail in Chapter 5.

The normalized waveforms for the split-leg topologies, when assuming infinite switching frequency, are shown in Figure 4.4, where $\hat{i}_{out}$ represents the peak value of the output current, and where T_o is the cycle time of the sinusoidal reference. The bias current i_{bias} is given by

$$i_{bias} = \tfrac{1}{2}\,|i_{out}| + i_{th} \tag{4.2}$$

where i_{th} is a non-negative offset current. Figure 4.4 illustrates the relation between the inductor currents, i_{bias}, and i_{out}, where i_{bias} is required to guarantee continuous conduction mode (CCM) for each leg.

The configuration with a parallel-connected P- and N-cell has some advantages over the conventional switching cell. Firstly, the diodes and switches can be optimized separately. This can result in reduced losses and even in a decreased

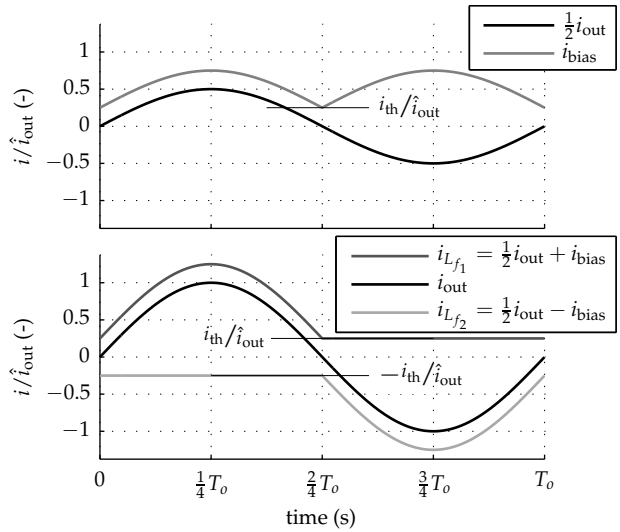


Figure 4.4: Normalized ideal waveforms with minimal losses for the DB topology.

number of discrete diodes compared to a conventional switching leg since no extra diode is required to block a low-performance MOSFET body diode. Secondly, it has an additional degree of freedom with respect to its switching waveforms compared to the canonical cell because the gating signals do not need to be complementary. On the other hand, it requires at least one additional inductor.

The filter inductors make the split-leg attractive for applications that require filtering of the PWM waveforms, in combination with the necessity of eliminating blanking-time-related distortion. These applications include

(a) high-performance positioning systems with strict electromagnetic interference requirements, where the use of stiff shielded-cables to the moving actuator is precluded due to the resulting mechanical disturbance forces, the original trigger of this work,

(b) high-precision magnetic fields, as in MRI and scanning-electron-microscope (SEM) imaging, where there are strict requirements on the variations of the generated fields due to switching,

(c) studio-quality audio amplifiers, which require filtering of the PWM voltage to suppress audible inter-modulation products due to the switching [105],

(d) grid-connected applications with high voltage- or current-quality requirements [108].

It should be noted the DB switching leg is a standard building block that can be used to replace a conventional switching leg in many topologies, as in parallel- and series-connected half- and full-bridge converters [105, 108], and other multi-level topologies, like the flying-capacitor and neutral-point-clamped converter [30, 53, 107, 112, 113].

4.2 Integrated bias

The circuit featuring parallel-connected P- and N-cells was first suggested in [136], and later in [137], as a high-performance current-regulated DC to AC converter with no shoot-through paths. It was shown that with proper control, low distortion can be achieved, even when non-linear loads are connected. Later in [105] the circuit was introduced as a buck-converter-derived PWM power stage with reduced shoot-through current, allowing zero blanking-time operation, and was baptized opposed-current converter (OCC). Operation of multiple parallel OCC stages was proposed, and it was shown that the topology is suitable for studio-quality audio reproduction and high-precision positioning systems. In [52] hysteresis current control was proposed for the OCC, and it was renamed to dual-buck (DB) converter. Later the same topology started to appear as split-phase dual-buck [139], and split-phase inverter [34]. More recently the DB got renewed attention for grid-connected renewable-energy applications [108,132,138]. In the remainder of this thesis the parallel-connected P- and N-cell will be referred to as DB.

Figure 4.5 depicts a practical implementation of the DB switching leg with filtering of the PWM voltage waveforms. The P-cell components are indicated with subscript 1, and the N-cell components with subscript 2. Furthermore, the filter inductors have equal values, L_f, and all voltages are referenced to the center terminal of the symmetrical DC supply.

Both legs are effectively operated in parallel and can be analyzed separately when assuming u_{C_f} constant over one switching cycle (T_{sw}). This is approximately valid because in practice the series resistance of C_f can be neglected, and C_f is chosen large enough that the output voltage is smooth. Figures 4.6a and 4.6b show the CCM waveforms. Under CCM operation, the steady-state inductor cur-

rent ripple amplitude (Δi_{L_f}) becomes

$$\Delta i_{L_{fx}} = \hat{\Delta} i_{L_f} \left(1 - {m_x}^2\right), \text{ with} \tag{4.3a}$$

$$\hat{\Delta} i_{L_f} = \frac{U_{\text{DC}}}{8 L_f} T_{\text{sw}} \tag{4.3b}$$

where the subscripts x indicate the corresponding switching leg, m_x is the modulation index, which is limited to the interval $[-1 \ldots 1]$, U_{DC} is the DC supply voltage of the DB switching leg, T_{sw} is the switching cycle time of the PWM, and L_f is the filter inductance. The amplitude of the inductor current ripple is given by

$$\begin{aligned} \Delta i_{L_f} &= \hat{i}_{L_f} - \langle i_{L_f} \rangle \\ &= \langle i_{L_f} \rangle - \check{i}_{L_f} \end{aligned}$$

where $\hat{i}_{L_f}$, $\check{i}_{L_f}$, and $\langle i_{L_f} \rangle$ represent the steady-state maximum, minimum and average inductor current, respectively.

The modulation index (m_x) is related to the duty-ratio (δ_x) of the switching leg as

$$\delta_x = \tfrac{1}{2} \left(1 + m_x\right) \tag{4.4}$$

with the duty ratio defined as

$$\delta_x = \frac{T_x^p}{T_{\text{sw}}} \tag{4.5}$$

where $T_{\text{sw}} = {f_{\text{sw}}}^{-1}$ is the switching cycle time, and T_x^p is the time interval that a switch node is connected to the positive DC supply.

The periodic average switch-node voltage $\langle u_{\text{sn}_x} \rangle$ can be determined by applying the state-space averaging method as presented in Chapter 2 and [65]. When disregarding losses and assuming CCM operation it becomes

$$\langle u_{\text{sn}_x} \rangle = \tfrac{1}{2} U_{\text{DC}} m_x. \tag{4.6}$$

4.2.1 Bounds for linear behavior

For CCM there is, ideally, a linear relation between m and $\langle u_{\text{sn}} \rangle$ for both the P- and N-cells. However, this is not the case for DCM, in which the node voltage does

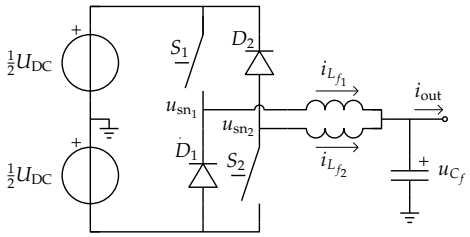


Figure 4.5: Practical implementation of a DB switching leg with integrated bias inductors.

not clamp to the DC rails during the whole switching cycle time. Figures 4.6c and 4.6d depict the voltage and current waveforms of the P- and N-cell during DCM. It is shown that the switch-node voltage u_{sn} ideally[1] becomes equal to u_{C_f} when the diode stops conducting, during $(t' \dots t_1)$ for the P-cell and during $(t' \dots t_2)$ for the N-cell. As a result, for DCM the steady-state switch-node voltages are found to be

$$\langle u_{sn_1} \rangle = \frac{(m_1+1)^2 - \langle i_{L_{f_1}} \rangle / \hat{\Delta} i_{L_{f_1}}}{(m_1+1)^2 + \langle i_{L_{f_1}} \rangle / \hat{\Delta} i_{L_{f_1}}} \frac{1}{2} U_{DC} \tag{4.7}$$

$$\langle u_{sn_2} \rangle = -\frac{(m_2-1)^2 + \langle i_{L_{f_2}} \rangle / \hat{\Delta} i_{L_{f_2}}}{(m_2-1)^2 - \langle i_{L_{f_2}} \rangle / \hat{\Delta} i_{L_{f_2}}} \frac{1}{2} U_{DC} \tag{4.8}$$

where m_1 and m_2 are the modulation indices of the P- and N-cell, respectively. The inductor currents of the P- and N-cell are represented by $i_{L_{f_1}}$ and $i_{L_{f_2}}$, and the corresponding maximum inductor current ripple amplitudes are given by $\hat{\Delta} i_{L_{f_1}}$ and $\hat{\Delta} i_{L_{f_2}}$.

From (4.7) and (4.8) it can be deduced that, for DCM, the switch-node voltages have a quadratic relation with respect to the modulation index, and are additionally dependent on the ratio between the average inductor current and the maximum inductor current ripple amplitude. As a result, a nonlinear distortion is introduced in the output voltage.

Figure 4.7 shows the resulting normalized average switch-node voltage as function of the normalized average inductor current ($\langle i_{L_f} \rangle$), where $\hat{\Delta} i_{L_f}$ denotes the maximum inductor current ripple amplitude. Figure 4.7 illustrates the nonlinear relation between m and the average switch-node voltage in case of DCM.

[1] In practice, high-frequency oscillations will occur, which might result in considerable electromagnetic interference.

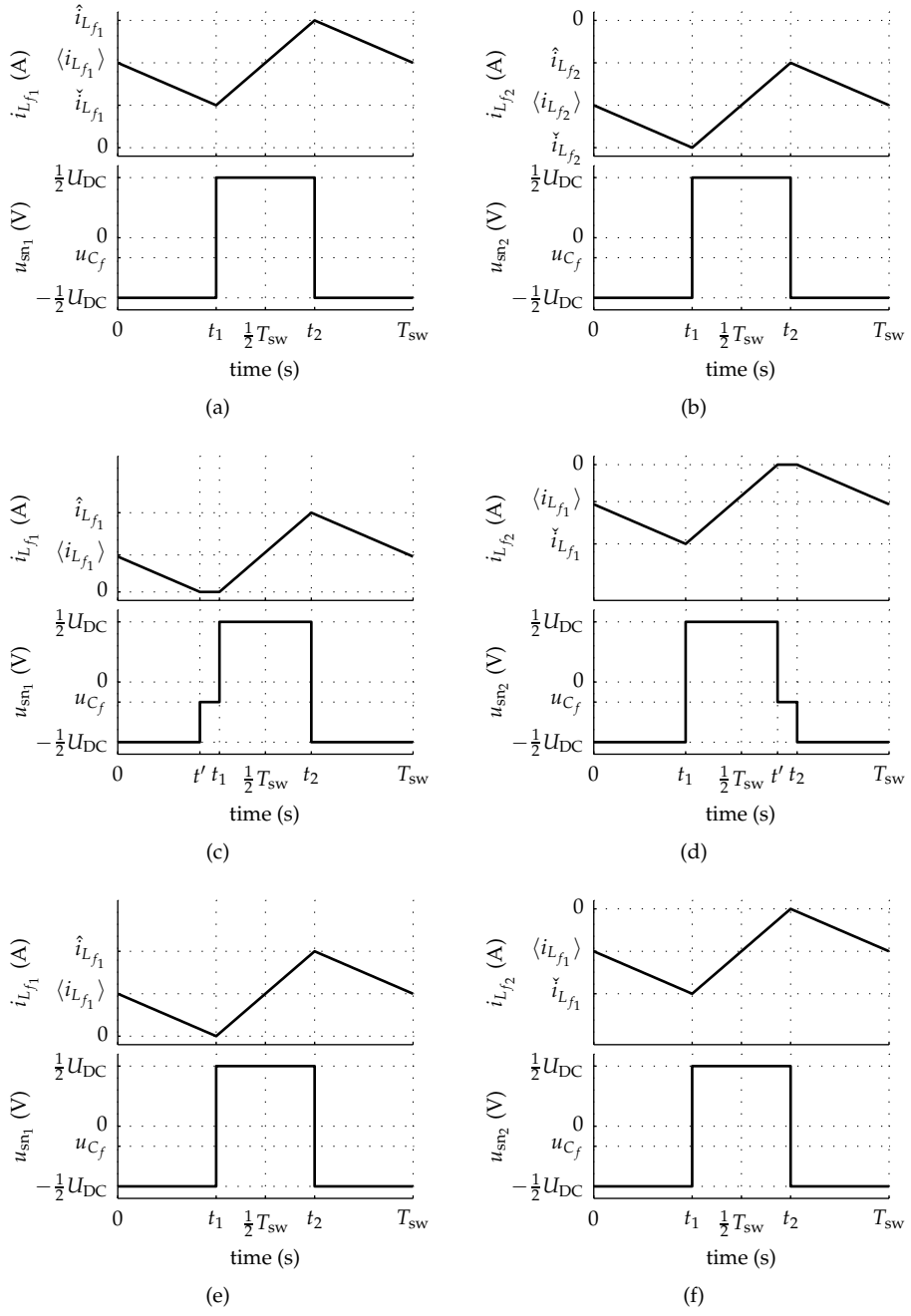


Figure 4.6: Normalized voltage and current waveforms for the P-cell (left), and the N-cell (right). From top to bottom the graphs represent: CCM, DCM, and BCM.

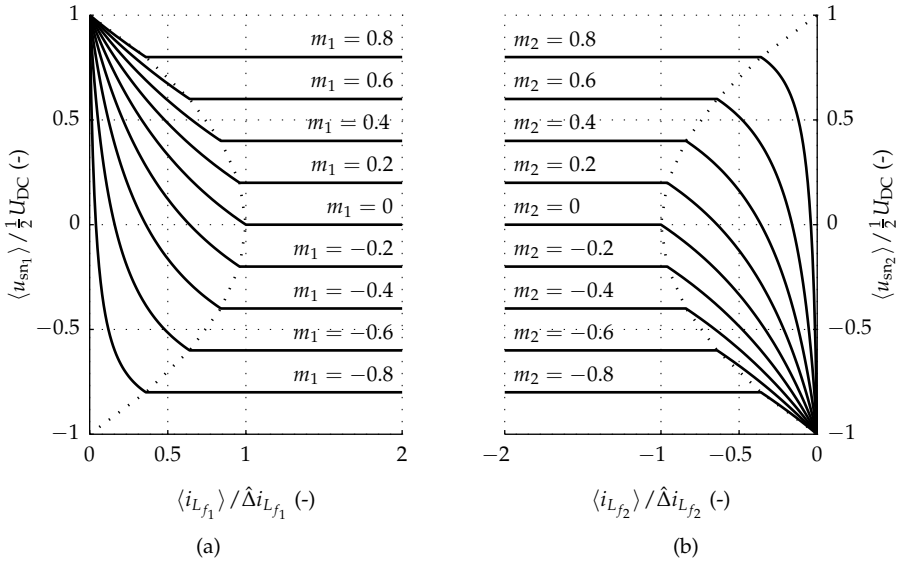


Figure 4.7: Normalized steady-state moving-average switch-node voltage as function of the normalized steady-state moving-average inductor current, for the P-cell (a), and the N-cell (b).

The transition between CCM and DCM, often referred to as boundary conduction mode (BCM) or critical conduction mode, is indicated by a dotted line and is determined by $^{\Delta i_{L_f}}/_{\hat{\Delta} i_{L_f}}$.

When examining Figure 4.7 more closely it can be deduced that, when no losses are present, the resulting switch-node voltage as imposed by a cell in DCM will force its current to enter BCM. However, in practice some losses are present preventing convergence to BCM, thus resulting in distorted output power. In that case a bias voltage can be applied to overcome these losses. Also an offset can exist between switch-node voltages which, when $\langle u_{sn_1} \rangle > \langle u_{sn_2} \rangle$, results in additional circulating current that is only limited by the losses in the circuit. Since efficiencies are generally high in SMPCs, a small offset voltage can lead to significantly more bias current than strictly required and, consequently, more losses. This again can be compensated by applying a negative bias voltage.

4.2.2 Decoupling through variable transformation

It is convenient to separate the bias voltage and current from the voltage and current that drive the output. Doing so leads to decoupled control of the output

power and the current necessary to maintain CCM. The following transformation can be used for that purpose:

$$u_{\text{avg}} = \tfrac{1}{2}\left(u_{\text{sn}_1} + u_{\text{sn}_2}\right) \tag{4.9a}$$

$$u_{\text{bias}} = u_{\text{sn}_1} - u_{\text{sn}_2} \tag{4.9b}$$

where u_{avg} is the average switch-node voltage of the P- and N-cell, and u_{bias} is the difference between the switch-node voltages which drives the bias current. A similar transformation for the currents is given by

$$i_{\text{sum}} = i_{L_{f_1}} + i_{L_{f_2}} \tag{4.10a}$$

$$i_{\text{bias}} = \tfrac{1}{2}\left(i_{L_{f_1}} - i_{L_{f_2}}\right) \tag{4.10b}$$

where i_{sum} is the combined current of the output filter inductors, and i_{bias} is the current required to prevent DCM.

When high-quality open-loop output power is required, a nonlinear relation between the control inputs (m_1 & m_2) and the corresponding outputs (u_{sn_1} & u_{sn_2}) should be avoided. It is thus essential that CCM is maintained under all input and output conditions. This can be achieved by ensuring that the moving average inductor currents are larger than the corresponding inductor current ripple amplitudes, $\langle i_{L_{f_1}} \rangle \geq \Delta i_{L_{f_1}}$ and $\langle i_{L_{f_2}} \rangle \leq \Delta i_{L_{f_2}}$, basically meaning that

$$\langle i_{\text{bias}} \rangle \geq \tfrac{1}{2}\left|\langle i_{\text{sum}} \rangle\right| + i_{\text{th}} \tag{4.11}$$

with

$$i_{\text{th}} \geq \begin{cases} \Delta i_{L_{f_2}}, & \langle i_{\text{sum}} \rangle \geq 0 \\ \Delta i_{L_{f_1}}, & \langle i_{\text{sum}} \rangle < 0. \end{cases} \tag{4.12}$$

In practice, the periodic average reactive filter capacitor current ($\langle i_{C_f} \rangle$) is often small compared to i_{out} and can therefore be disregarded in many cases. As a consequence, $\langle i_{\text{sum}} \rangle$ can be assumed equal to $\langle i_{\text{out}} \rangle$, making (4.11) virtually equal to (4.2).

A similar transformation can be used for the controlling inputs, leading to

$$m_{\text{avg}} = \tfrac{1}{2}\left(m_1 + m_2\right) \tag{4.13a}$$

$$m_{\text{bias}} = m_1 - m_2 \tag{4.13b}$$

where m_{avg} is the controlling modulation index for $\langle u_{\text{avg}} \rangle$, and m_{bias} for $\langle u_{\text{bias}} \rangle$.

Finally, by again combining (4.6) and (4.13) it follows that

$$\langle u_{\text{avg}} \rangle = \tfrac{1}{2} U_{\text{DC}} m_{\text{avg}} \tag{4.14a}$$
$$\langle u_{\text{bias}} \rangle = \tfrac{1}{2} U_{\text{DC}} m_{\text{bias}} \tag{4.14b}$$

which is valid when assuming no losses and CCM conditions.

It should be noted that the output voltage range of the DB converter is limited by the amount of bias voltage that is required, since the absolute value of the modulation indices (m_x) cannot exceed one, which leads to the following bound on the modulation indexes

$$|m_{\text{avg}}| + \tfrac{1}{2} m_{\text{bias}} \leq 1. \tag{4.15}$$

The inductances (L_f) can also be expressed in terms of L_{sum} and L_{bias}, which for uncoupled inductors simplifies to

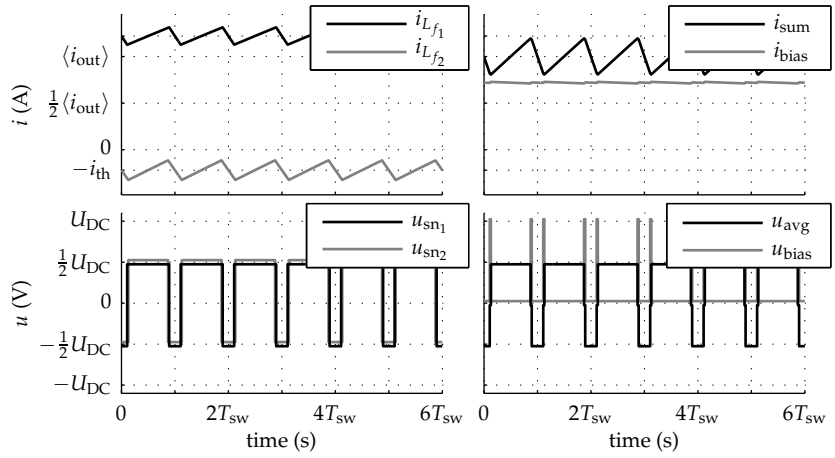
$$L_{\text{sum}} = \tfrac{1}{2} L_f \tag{4.16a}$$
$$L_{\text{bias}} = 2 L_f. \tag{4.16b}$$

The variable transformation presented in this section decouples the bias and output related voltages and currents and will be applied to the DB converter from hereon.

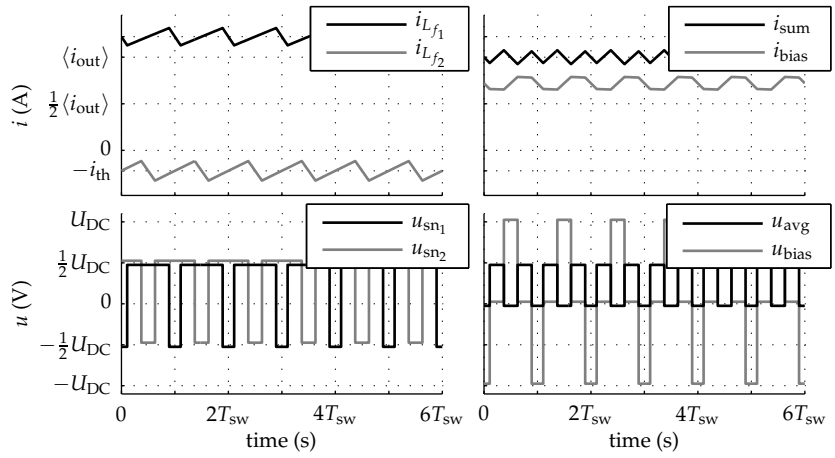
4.2.3 PWM generation

Because the rate of current change is limited by the inductors that couple the switching-leg voltages, the gating signals for a DB switching leg do not need to be complementary and may even overlap. This adds an additional degree of freedom to the PWM patterns of the DB switching leg. In the ideal case only two possible PWM methods make sense; to switch both legs either simultaneously (non-interleaved) or time shifted by $\frac{1}{2} T_{\text{sw}}$ (interleaved).

Figure 4.8 depicts the switching waveforms for the DB switching leg with integrated bias inductors for both non-interleaved and interleaved ($\frac{1}{2} T_{\text{sw}}$ shifted) switch-node voltage (u_{sn}) with and without variable transformation. A small shift has been added to the voltage traces to make the waveforms clearer. Furthermore, losses are included. This results in $u_{\text{bias}} = 0.04 U_{\text{DC}}$, which is realistic in a practical set-up. The bias voltage is especially visible in Figure 4.8a where it



(a)



(b)

Figure 4.8: Switching waveforms of the DB switching leg, for (a) non-interleaved u_{sn}, and (b) interleaved u_{sn}.

appears in the form of narrow voltage peaks. In Figure 4.8b the bias voltage appears as slightly wider positive u_{bias} pulses compared to the negative u_{bias} pulses.

The inductor current ripples of the DB switching leg with integrated bias inductors can be expressed in terms of the current ripple amplitudes of i_{sum} and i_{bias} when neglecting u_{bias}, which has only a small effect in practice. This results in

$$\Delta i_{L_{f_1}} = \Delta i_{L_{f_2}} = \tfrac{1}{2}\Delta i_{\text{sum}} + \Delta i_{\text{bias}} \tag{4.17}$$

where, Δi_{sum} and Δi_{bias} are given by

$$\Delta i_{\text{sum}} = \begin{cases} \frac{U_{\text{DC}}}{8L_{\text{sum}}} T_{\text{sw}} \left(1 - m_{\text{avg}}^2\right), & \text{non-interleaved } u_{\text{sn}} \\ \frac{U_{\text{DC}}}{8L_{\text{sum}}} T_{\text{sw}} \left(\left|m_{\text{avg}}\right| - m_{\text{avg}}^2\right), & \text{interleaved } u_{\text{sn}} \end{cases} \tag{4.18}$$

$$\Delta i_{\text{bias}} = \begin{cases} 0, & \text{non-interleaved } u_{\text{sn}} \\ \frac{U_{\text{DC}}}{4L_{\text{bias}}} T_{\text{sw}} \left(1 - \left|m_{\text{avg}}\right|\right), & \text{interleaved } u_{\text{sn}}. \end{cases} \tag{4.19}$$

When $\langle u_{\text{bias}} \rangle = 0$, in case of non-interleaved voltages, as depicted in Figure 4.8a, i_{bias} and u_{bias} have no ripple, and i_{sum} and u_{avg} have ripple with frequency equal to the switching frequency. For interleaved voltages, as in Figure 4.8b, the frequency of the ripples of i_{sum} and u_{avg} doubles and the ripple amplitudes halve. However, a non-zero ripple with fundamental frequency equal to the switching frequency appears on i_{bias} and u_{bias}. Consequently, there is a trade-off between the effective frequency and the amplitude of the ripple of u_{avg} and i_{sum} on one hand, and the ripple of u_{bias} and i_{bias} on the other hand.

4.2.4 Losses

Ideally, the DB switching leg with integrated bias inductors, as depicted in Figure 4.5, is lossless. In practice this is not the case. When evaluating losses of a converter, it is important to know the conditions for which the losses are determined. This is especially true for the DB since it requires a bias current that can be chosen with arbitrary value as long as it satisfies (4.11).

Two different methods for bias current generation are considered from hereon. The first method concerns constant bias current, for which

$$\langle i_{\text{bias}} \rangle = \tfrac{1}{2}\hat{i}_{\text{sum}} + i_{\text{th}}. \tag{4.20}$$

The second method is related to modulated bias current, and is given by

$$\langle i_{\text{bias}} \rangle = \tfrac{1}{2} \left| i_{\text{sum}} \right| + i_{\text{th}} \tag{4.21}$$

where $\hat{i}_{\text{sum}}$ represents the maximum expected i_{sum}. When $\langle i_{C_f} \rangle$ is small compared to i_{out}, which is often true in practice, i_{sum} can be assumed equal to i_{out}. When the variation of Δi_{L_f} is small compared to $\hat{i}_{L_f}$, i_{th} can be chosen equal to

$$i_{\text{th}} = \lambda_{\text{th}} \hat{\Delta} i_{L_f} \tag{4.22}$$

without adding significant losses, where λ_{th} is a constant greater than or equal to one resulting in an additional offset current to prevent DCM during transients.

The two modulation methods, together with the possibility of non-interleaved and interleaved voltages, lead to four methods to drive the DB converter. Figures 4.9 and 4.10 depict the DB waveforms for non-interleaved and interleaved switch-node voltages with both constant and modulated bias current for sinusoidal excitation with cycle time (T_o). The maximum modulation index ($\hat{m}_x$) is 0.75 and the level of the offset current is indicated by i_{th}. The switching frequency is chosen high compared to the excitation frequency, resulting in very dense switching waveforms, which appear as bands in the figure. The dependency of $\Delta i_{L_{fx}}$ on the modulation index can be clearly seen in the figure. The bias voltage is chosen 4 % of U_{DC}, which is realistic, and is multiplied by a factor five in the graph to make it more clear. Also notice that the output voltage (u_{C_f}) and output current (i_{out}) show no visible distortion as it would be the case with a practical switching cell with blanking time.

For non-modulated bias, as shown in Figures 4.9a and 4.10a, the level of the bias current depends on $\hat{i}_{\text{sum}}$ and can potentially result in high losses for arbitrary waveforms. However, for arbitrary waveforms, where maximum expected current is known a-priori, it is possible to limit losses by adapting the level of the bias current to particular situations. For instance, in audio applications the bias current can be made dependent on the selected volume, or for MRI the level of i_{bias} can be set according to the signal that is going to be applied to the gradient coil at that moment[2]. Non-modulated bias current requires only very low bandwidth control because the bias voltage is constant for a given i_{bias}.

For modulated bias, as illustrated in Figures 4.9b and 4.10b, the level of i_{bias} is dependent on the absolute value of i_{sum}. Therefore, the modulation results in bias voltage steps at the zero crossings of i_{out}. These steps require more demanding control, possibly in combination with feed-forward. However, it leads to less bias

[2]Such prior knowledge is, in principle, available in an MRI system.

current and, consequently, less losses.

Both Figures 4.9 and 4.10 show the difference between the non-interleaved and interleaved switch-node voltages. Both inductor currents have equal envelopes, but are phase shifted for the interleaved case, as depicted in Figure 4.8b. Interleaved switch-node voltages, however, lead to a factor two reduction of $\hat{\Delta} i_{\text{sum}}$, at the cost of a significant increase of the bias current ripple.

Both the P-cell and the N-cell of the DB switching-leg support only unidirectional current. Consequently, the (parasitic) antiparallel diodes of the switches never conduct current. For this reason it is possible to describe the conduction losses for uni- and bidirectional current semiconductor devices, such as IGBTs and MOSFETs, in a single model.

Figure 4.11 depicts the model used to determine the conduction losses. The ideal diodes and switches are extended with a forward voltage (V_f & V_{on}) and an on-resistance (R_f & R_{on}), which is a linear approximation of underlying exponential behavior. However, for power diodes and IGBTs the voltage drop due to the on-resistance is dominant, which masks the exponential behavior [67, page 525]. As a consequence the voltage/resistor representation is in practice a good model for power diodes and IGBTs. Power MOSFETs behave resistive when conducting, as a consequence $V_{\text{on}} = 0$ for MOSFET switches. It should be noted that semiconductor parameters vary significantly as function of temperature. The effects of temperature are neglected in this thesis.

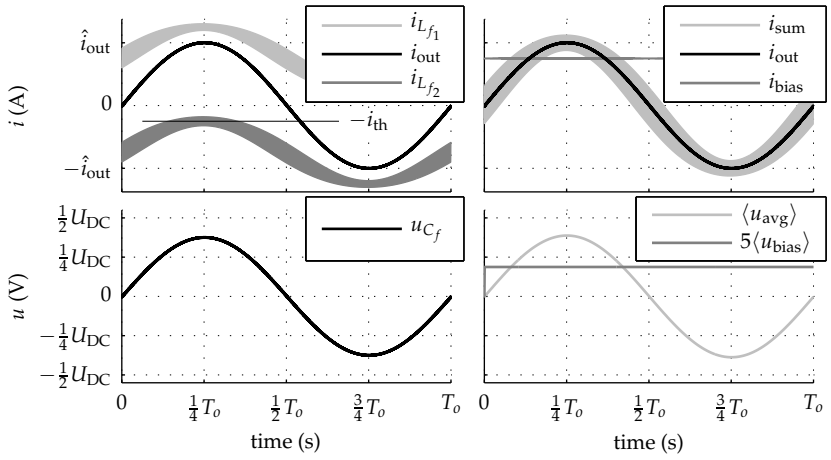
The conduction losses of the passive components are taken into account by series resistances. For determining losses, the switching currents are assumed ideal triangular shaped, and any amplitude, frequency or temperature dependencies are neglected. Furthermore, it is assumed that the DB converter is operating in CCM.

Losses in passive components

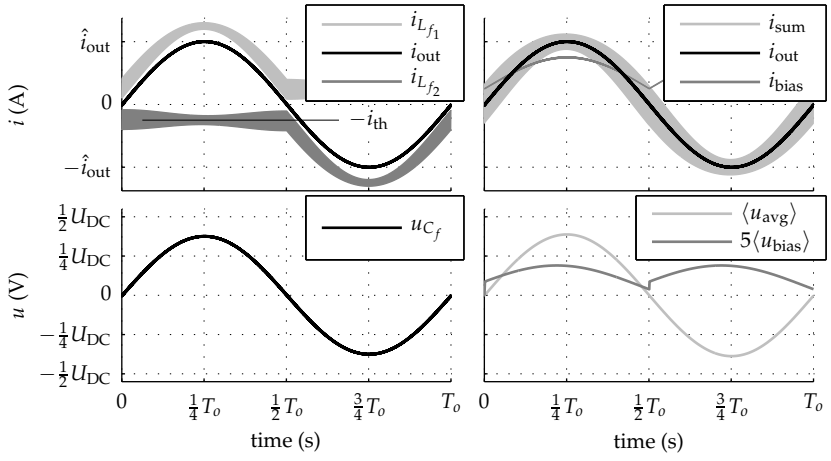
The losses of the output filter can be expressed as follows:

$$P_{R_{L_f}} = R_{L_f} \frac{1}{T} \left[\int_T \left(i_{L_{f_1}}(t) \right)^2 \mathrm{d}t + \int_T \left(i_{L_{f_2}}(t) \right)^2 \mathrm{d}t \right]. \tag{4.23}$$

It is illustrative to compare these losses to the situation in conventional switching cells. This can be achieved by expressing $i_{L_{f_x}}$ in (4.23) in terms of i_{sum} and i_{bias},



(a)



(b)

Figure 4.9: Simulated waveforms of the DB converter, (a) without, and (b) with modulated bias voltage for non-interleaved switch-node voltages.

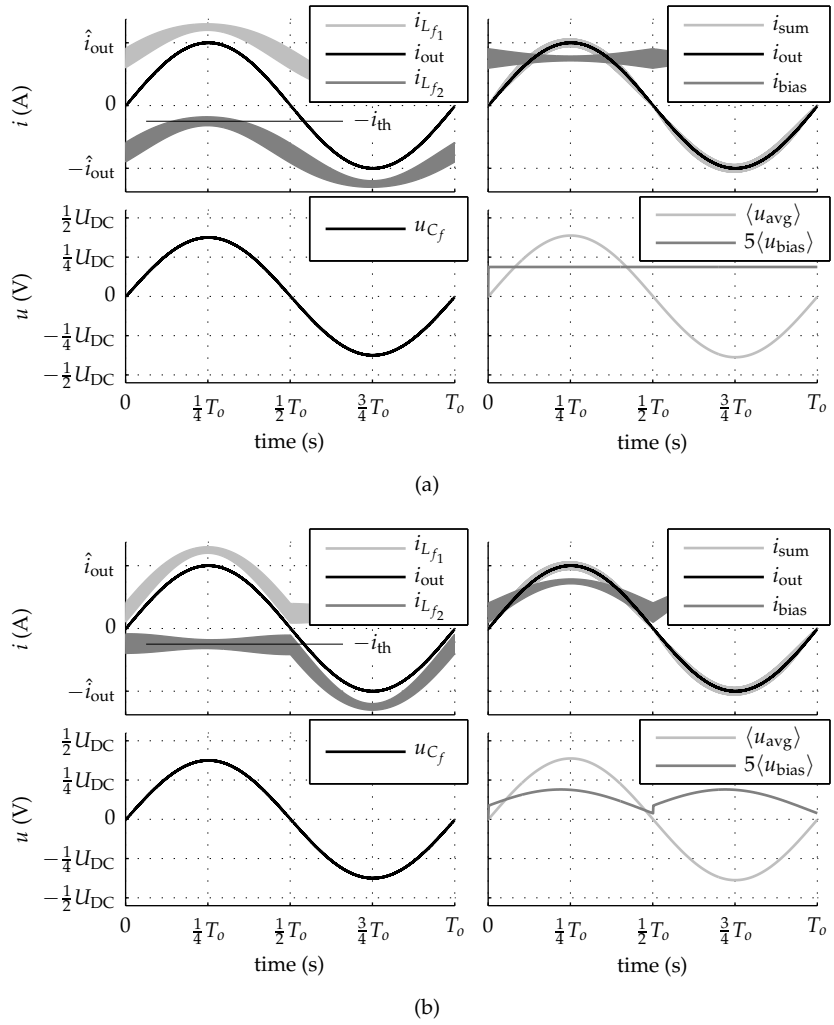


Figure 4.10: Simulated waveforms of the DB converter, (a) without, and (b) with modulated bias voltage for interleaved switch-node voltages.

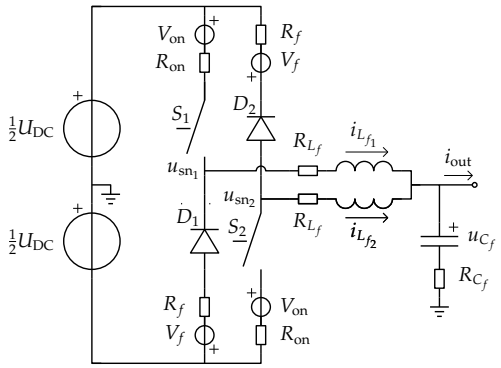


Figure 4.11: Split-leg with integrated bias and lossy components.

as in (4.10), which leads to

$$P_{R_{L_f}} = R_{L_f} \frac{1}{T_o} \int_{T_o} \left(\tfrac{1}{2} i_{\text{sum}}(t) \pm i_{\text{bias}}(t) \right)^2 \mathrm{d}t \tag{4.24}$$

where in turn equation (4.24) can be rewritten to

$$P_{R_{L_f}} = R_{L_f} \frac{2}{T_o} \int_{T_o} \left(\tfrac{1}{4} \left(i_{\text{sum}}(t) \right)^2 + \left(i_{\text{bias}}(t) \right)^2 \right) \mathrm{d}t. \tag{4.25}$$

Analogous with (4.16), R_{L_f} can be expressed in terms of $R_{L_{\text{sum}}}$ and $R_{L_{\text{bias}}}$, with

$$R_{L_{\text{sum}}} = \tfrac{1}{2} R_{L_f} \tag{4.26a}$$

$$R_{L_{\text{bias}}} = 2 R_{L_f}. \tag{4.26b}$$

By combining (4.26) and (4.25) the expression for the losses in the inductors for the DB switching leg becomes

$$P_{R_{L_f}} = R_{L_{\text{sum}}} I_{\text{sum}}^2 + R_{L_{\text{bias}}} I_{\text{bias}}^2 \tag{4.27}$$

where RMS values are represented by capitals. Equation (4.27) shows that the proposed variable transformations are invariant for loss power. When comparing the losses in the filter inductors of teh DB to its equivalent conventional switching cell, that is when $R_{L_{\text{sum}}}$ is equal to the filter inductor resistance of the conventional cell, it can be seen that the inductive losses increase with the square of the RMS bias current times $R_{L_{\text{bias}}}$. It is, therefore, essential to keep the bias current as small as possible.

When assuming sinusoidal output current and neglecting the effect of the switching current ripple the ratio $P_{R_{L_f}}/P_{R_{L_{\text{HB}}}}$ between the losses of the DB and its conventional equivalent HB can be approximated by

$$\frac{P_{R_{L_f}}}{P_{R_{L_{\text{HB}}}}} \approx \begin{cases} 3 + 8\frac{i_{\text{th}}}{\hat{i}_{\text{out}}}, & \text{constant bias} \\ 2 + \frac{16}{\pi}\frac{i_{\text{th}}}{\hat{i}_{\text{out}}}, & \text{modulated bias} \end{cases} \tag{4.28}$$

which is definitely significant. In practice, when assuming $i_{\text{th}}/\hat{i}_{\text{out}} = 0.2$, the conduction losses in the inductive components will increase with a factor 4.6 for constant bias and approximately with a factor three for modulated bias, compared to a conventional switching leg. From (4.28) it can also be seen that the inductive losses for modulated bias current improve by at factor $2/3$ to $2/\pi$ compared to the losses for constant bias current. It should be noted that (4.28) assumes that the filter inductor of the equivalent HB is assumed equal to L_{sum}, thus the individual DB inductors are valued two times larger than the filter inductor of its equivalent HB.

The conduction losses of the filter capacitor of the DB are equal to its conventional switching, and can be expressed as

$$P_{R_{C_f}} = R_{C_f} \frac{1}{T_o} \int_{T_o} \left(i_{C_f}(t) \right)^2 \mathrm{d}t \tag{4.29}$$

where $i_{C_f} = i_{\text{sum}} - i_{\text{out}}$, and R_{C_f} is the parasitic equivalent series resistance of the filter capacitor (C_f). For constant (DC) $\langle u_{C_f} \rangle$, (4.29) simplifies to

$$P_{R_{C_f}} = R_{C_f} \tfrac{1}{3} \left(\Delta i_{\text{sum}} \right)^2 . \tag{4.30}$$

For the non-interleaved case, the DB is equivalent to the conventional switching leg with filter inductor resistance and current equal to $R_{L_{\text{sum}}}$ and i_{sum}, respectively. The additional inductor conduction losses of the DB with respect to the conventional switching leg can therefore be simply expressed as $R_{L_{\text{bias}}} I_{\text{bias}}^2$. It should be noted that, when scaled to the conventional switching leg, $R_{L_{\text{bias}}}$ is four times bigger than the corresponding resistance in the conventional switching cell, resulting in at least twice as much losses. It is therefore important to keep I_{bias} as small as possible, and the DB should be properly designed to minimize conduction losses.

Losses in switching devices

A similar analysis can be done for the switching devices. The steady-state conduction losses of the switching devices (P_S^{con}) and diodes (P_D^{con}) for one switching cycle are given by

$$P_S^{\text{con}} = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} \left(V_{\text{on}} \left(i_{S_1}(t) + i_{S_2}(t) \right) + R_{\text{on}} \left(\left(i_{S_1}(t) \right)^2 + \left(i_{S_2}(t) \right)^2 \right) \right) \mathrm{d}t \quad (4.31a)$$

$$P_D^{\text{con}} = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} \left(V_f \left(i_{D_1}(t) + i_{D_2}(t) \right) + R_f \left(\left(i_{D_1}(t) \right)^2 + \left(i_{D_2}(t) \right)^2 \right) \right) \mathrm{d}t \quad (4.31b)$$

where i_{S_x} and i_{D_x} are the currents flowing through the corresponding switches and diodes, and V_{on} and R_{on}, and V_f and R_f are the forward voltage and on-resistance of the switches and diodes, respectively.

Equation (4.31b) can be rewritten in terms of the inductor currents by changing the integration interval, because the current flowing through the switching devices is zero when they are not conducting

$$P_S^{\text{con}} = \frac{1}{T_{\text{sw}}} \int_{T_1^p} \left(R_{\text{on}} \left(i_{L_{f_1}}(t) \right)^2 + V_{\text{on}} i_{L_{f_1}}(t) \right) \mathrm{d}t + \frac{1}{T_{\text{sw}}} \int_{T_2^n} \left(R_{\text{on}} \left(i_{L_{f_2}}(t) \right)^2 - V_{\text{on}} i_{L_{f_2}}(t) \right) \mathrm{d}t \quad (4.32a)$$

$$P_D^{\text{con}} = \frac{1}{T_{\text{sw}}} \int_{T_1^n} \left(R_f \left(i_{L_{f_1}}(t) \right)^2 + V_f i_{L_{f_1}}(t) \right) \mathrm{d}t + \frac{1}{T_{\text{sw}}} \int_{T_2^p} \left(R_f \left(i_{L_{f_2}}(t) \right)^2 - V_f i_{L_{f_2}}(t) \right) \mathrm{d}t \quad (4.32b)$$

where T_x^p and T_x^n are the time intervals that the corresponding switch node is connected to the positive or negative DC supply, as represented by the time intervals $(t_1 \ldots t_2)$ and $(t_2 \ldots t_1)$, respectively in Figures 4.6a and 4.6b.

When assuming ideal triangular switching currents and applying the proposed variable transformations, the total steady-state instantaneous conduction losses

of the switching leg become

$$P^{\text{con}} = \left(V_{\text{on}} + V_f\right)\langle i_{\text{bias}}\rangle + \tfrac{1}{2}\left(V_{\text{on}} - V_f\right)\left(\langle i_{\text{sum}}\rangle\, m_{\text{avg}} + \langle i_{\text{bias}}\rangle\, m_{\text{bias}}\right) + \left(R_{\text{on}} + R_f\right)\left(\tfrac{1}{4}I_{\text{sum}}^2 + I_{\text{bias}}^2\right) + \tfrac{1}{2}\left(R_{\text{on}} - R_f\right)\left(\tfrac{1}{4}I_{\text{sum}}^2 + I_{\text{bias}}^2\right) m_{\text{bias}} + \left(R_{\text{on}} - R_f\right)\langle i_{\text{bias}}\rangle\langle i_{\text{sum}}\rangle\, m_{\text{avg}} \quad (4.33)$$

where, in turn, the switching time intervals are expressed in terms of m_{avg} and m_{bias}, $\langle\cdot\rangle$ represents a periodic average value, and the capitalized currents represent cycle RMS values, respectively. From (4.33) it can be seen that the losses of a DB switching leg become independent of the modulation index when $V_{\text{on}} = V_f$ and $R_{\text{on}} = R_f$. Furthermore, when $V_{\text{on}} = V_f$ the losses due to forward voltage only depend on the average bias current and not on $\langle i_{\text{sum}}\rangle$. The effects of the forward voltage and resistive losses on output quality are treated in detail in Chapter 6.

The conduction losses in a conventional switching leg can be calculated similarly as for the DB. When neglecting blanking time and assuming unipolar current devices, i.e. IGBTs and ideal triangular switching currents, the steady state conduction losses are given by

$$P_{\text{HB}}^{\text{con}} = \begin{cases} \tfrac{1}{2}\left(V_{\text{on}} + V_f\right)\langle i_{L_{\text{HB}}}\rangle + \tfrac{1}{2}\left(R_{\text{on}} + R_f\right) I_{L_{\text{HB}}}^2 + \\ \quad \tfrac{1}{2}\left(V_{\text{on}} - V_f\right)\langle i_{L_{\text{HB}}}\rangle m + \tfrac{1}{2}\left(R_{\text{on}} - R_f\right) I_{L_{\text{HB}}}^2 m, \quad \check{i}_{L_{\text{HB}}} > 0 \\ -\tfrac{1}{2}\left(V_{\text{on}} + V_f\right)\langle i_{L_{\text{HB}}}\rangle + \tfrac{1}{2}\left(R_{\text{on}} + R_f\right) I_{L_{\text{HB}}}^2 + \\ \quad \tfrac{1}{2}\left(V_{\text{on}} - V_f\right)\langle i_{L_{\text{HB}}}\rangle m - \tfrac{1}{2}\left(R_{\text{on}} - R_f\right) I_{L_{\text{HB}}}^2 m, \quad \hat{i}_{L_{\text{HB}}} < 0 \end{cases} \quad (4.34)$$

where $\langle i_{L_{\text{HB}}}\rangle$ and $I_{L_{\text{HB}}}$ are the periodic average and cycle RMS inductor currents of the equivalent conventional HB, and m represents the modulation index of the HB. It should be noted that (4.34) is only valid for distinct positive or negative steady-state inductor current.

When assuming $m = m_{\text{avg}} = m_{\text{bias}} = 0$, i.e. the losses are equally distributed over the switching devices, and neglecting the effects of the switching current ripple, the instantaneous losses due to V_{on} and V_f, and R_{on} and R_f of the DB increase approximately by a factor $1 + {}^{2i_{\text{th}}}/_{\hat{i}_{\text{out}}}$ and $2.5 + {}^{4i_{\text{th}}}/_{\hat{i}_{\text{out}}}$, respectively, compared to the conventional HB. In practice, when again assuming ${}^{i_{\text{th}}}/_{\hat{i}_{\text{out}}} = 0.2$, the conduction losses due to V_{on} and V_f, and R_{on} and R_f of the DB, increase by factor 1.4 and 3.3, respectively.

The switching losses of the DB are not detailed in this thesis. However, the DB has the same number of switching devices as the HB, two switches and two diodes, and therefore both legs of the DB suffer from diode reverse-recovery losses when the corresponding semiconductor switch is turned on, which is not the case for the conventional HB. The HB has only one occurrence of diode reverse-recovery losses per switching cycle.

When a semiconductor switch is turned off, soft commutation to the corresponding discrete diode occurs in a DB leg, and, consequently, the inherit antiparallel diodes of the semiconductor switches do not conduct during normal operation. Power MOSFETs have an integrated parasitic bipolar junction transistor (BJT), which can turn-on unintendedly when too-fast transients of the drain-source voltage (u_{DS}) occur due to reverse recovery of the internal antiparallel diode of the MOSFET [67, page 590]. Therefore, in case that MOSFETs are used in a DB, this accidental turn-on cannot occur. Moreover, the mostly poor integrated antiparallel diodes of the semiconductor switches do not need to be blocked and bypassed, as might be required for convention switching legs [67, page 592].

It should be noted that it is possible to optimize the diode and switch separately for the DB, since the antiparallel diodes of the switches are never conducting. Therefore, less concessions have to be made when selecting the semiconductor devices. Losses can be reduced by selecting diodes with low reverse-recovery charge and switches with very low on-state voltage. The loss analysis made in this section assumed use of the same switches and diodes in the DB and the HB, which most likely does not result in the lowest possible losses.

Both the losses in the inductors and switching devices increase significantly compared to the conventional PWM switching leg, this is the price to pay for signal quality.

4.3 Auxiliary bias

Figure 4.12 shows the DB with the auxiliary bias circuit. Since the polarity of $i_{L_{ax}}$ is always the same, only unipolar current capability is required for the auxiliary switching legs. Therefore, additional P- and N-cells with auxiliary bias inductors are incorporated in the DB converter, resulting in a topology that is still robust for shoot-through current and will be referred to as auxiliary-bias dual-buck (ABDB) converter from here on.

The moving average inductor currents required to guarantee CCM are found to be

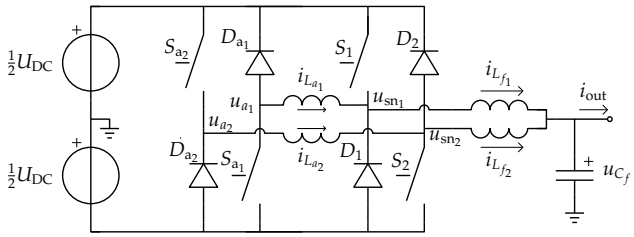


Figure 4.12: Practical implementation of a dual-buck with auxiliary bias inductors.

$$\langle i_{L_{f_1}} \rangle = \tfrac{1}{2} \langle i_{\text{sum}} \rangle \tag{4.35a}$$

$$\langle i_{L_{f_2}} \rangle = \tfrac{1}{2} \langle i_{\text{sum}} \rangle \tag{4.35b}$$

$$\langle i_{L_{a_1}} \rangle = -\tfrac{1}{2} \left| \langle i_{\text{sum}} \rangle \right| - i'_{\text{th}} \tag{4.35c}$$

$$\langle i_{L_{a_2}} \rangle = \tfrac{1}{2} \left| \langle i_{\text{sum}} \rangle \right| + i'_{\text{th}} \tag{4.35d}$$

with, for positive power flow (active power flowing from the source to the load),

$$i'_{\text{th}} \geq \begin{cases} \Delta i_{L_{f_2}} + \Delta i_{L_{a_2}}, & \langle i_{\text{sum}} \rangle \geq 0 \wedge m_{\text{avg}} \geq 0 \\ \Delta i_{L_{f_1}} + \Delta i_{L_{a_1}}, & \langle i_{\text{sum}} \rangle < 0 \wedge m_{\text{avg}} < 0 \end{cases} \tag{4.36}$$

where $\Delta i_{L_{fx}}$ and $\Delta i_{L_{ax}}$ are the current ripple amplitudes of the corresponding inductors. For negative power flow, i'_{th} as given in (4.36) is slightly conservative.

The inductor current ripple amplitudes $\Delta i_{L_{f_1}}$ and $\Delta i_{L_{f_2}}$ are ideally equal, and given by

$$\Delta i_{L_f} = \hat{\Delta} i_{L_f} \left(1 - m_{\text{avg}}^2 \right), \text{ with} \tag{4.37a}$$

$$\Delta \hat{i}_{L_f} = \frac{U_{\text{DC}}}{8 L_f} T_{\text{sw}} \tag{4.37b}$$

where T_{sw} is the PWM switching cycle time, and m_{avg} represents the modulation index that corresponds to the output voltage. The modulation index m_{avg} is confined to the interval $[-1 \ldots 1]$ and is, as for the DB, given by

$$m_{\text{avg}} = \frac{2}{U_{\text{DC}}} \left\langle u_{\text{avg}} \right\rangle . \tag{4.38}$$

For $m_{\text{bias}_1} \leq 0$, and $m_{\text{bias}_2} \geq 0$, the inductor current ripple of the auxiliary induc-

tors can be determined from

$$\Delta i_{L_{a_1}} = \hat{\Delta} i_{L_{a_1}} \cdot \max\left(\tfrac{1}{2}\left(1 + m_{\text{avg}}\right) + m_{\text{bias}_1},\ \tfrac{1}{2}\left(1 - m_{\text{avg}}\right)\right) \tag{4.39a}$$

$$\Delta i_{L_{a_2}} = \hat{\Delta} i_{L_{a_2}} \cdot \max\left(\tfrac{1}{2}\left(1 - m_{\text{avg}}\right) - m_{\text{bias}_2},\ \tfrac{1}{2}\left(1 + m_{\text{avg}}\right)\right) \tag{4.39b}$$

$$\hat{\Delta} i_{L_{a_x}} = \frac{U_{\text{DC}}}{2L_a} T_{\text{sw}} \left| m_{\text{bias}_x} \right| \tag{4.39c}$$

where $\max(\cdot,\cdot)$ represents the maximum of both elements. The modulation indices for the bias voltages of the corresponding switching legs are given by m_{bias_1} and m_{bias_2}, which are also limited within the interval $[-1 \ldots 1]$, and are given by

$$m_{\text{bias}_x} = \frac{1}{U_{\text{DC}}} \left\langle u_{\text{bias}_x} \right\rangle, \text{ with} \tag{4.40a}$$

$$u_{\text{bias}_x} = u_{a_x} - u_{\text{sn}_x}. \tag{4.40b}$$

For completeness, the offset current i'_{th} for negative power is determined from

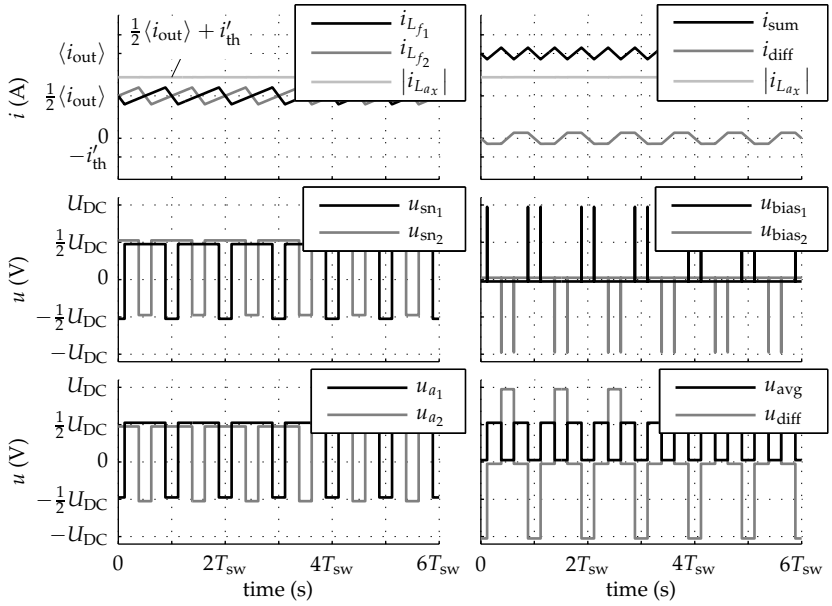
$$i'_{\text{th}} \geq \begin{cases} \Delta i_{L_{f_2}} + \hat{\Delta} i_{L_{a_2}} \cdot \min\left(\tfrac{1}{2}\left(1 - m_{\text{avg}}\right) - m_{\text{bias}_2},\ \tfrac{1}{2}\left(1 + m_{\text{avg}}\right)\right), \\ \qquad\qquad \left\langle i_{\text{sum}} \right\rangle \geq 0 \wedge m_{\text{avg}} < 0 \\ \Delta i_{L_{f_1}} + \hat{\Delta} i_{L_{a_1}} \cdot \min\left(\tfrac{1}{2}\left(1 + m_{\text{avg}}\right) + m_{\text{bias}_1},\ \tfrac{1}{2}\left(1 - m_{\text{avg}}\right)\right), \\ \qquad\qquad \left\langle i_{\text{sum}} \right\rangle < 0 \wedge m_{\text{avg}} \geq 0 \end{cases} \tag{4.41}$$

which is equal to (4.36) for $m_{\text{bias}_x} = 0$, and where $\min(\cdot,\cdot)$ represents the minimum of both elements.

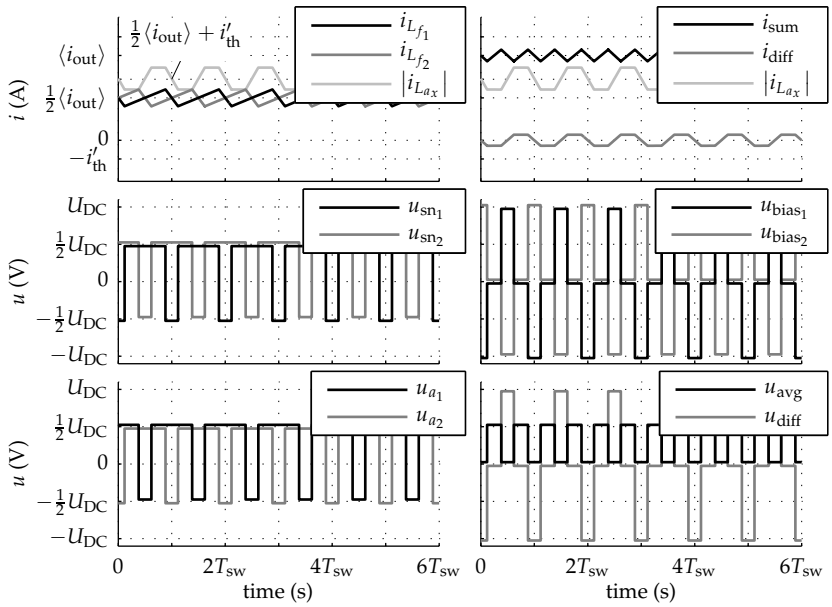
As with interleaved converters, the phase shift between the individual switch-node voltages (u_{sn_x}) should be chosen $\phi = {}^{360°}/_{N}$, with $N = 2$, or according to [15] when component variation needs to be included. To minimize the auxiliary inductor current ripple $\Delta i_{L_{a_x}}$, the phase shifts of u_{a_x} should be chosen equal to the corresponding u_{sn_x}, as suggested with the left-hand waveforms in Figure 4.13a.

Figure 4.13b shows the ABDB waveforms with phase-shifted u_{a_x}, a scheme which results in significant $\Delta i_{L_{a_x}}$ ripple. Applying a different switching frequency for the auxiliary legs is in most cases not beneficial for either losses or auxiliary inductor (L_a) volume. This is due to the small u_{bias_x} that is normally required for the ABDB.

The amount of circulating current through the filter inductors (L_f) should be minimized to keep the losses as low as possible. At the same time, DCM has to be prevented to ensure a high-quality output voltage. Therefore, $i_{L_{a_1}}$ and $i_{L_{a_2}}$ need to



(a)



(b)

Figure 4.13: Simulated voltage and current waveforms for the ABDB, with equal phase shift u_{sn_x} and u_{a_x} (a), and with 180° phase shift (b).

be set according to (4.35). A convenient transformation for the output quantities is

$$i_{\text{sum}} = i_{L_{f_1}} + i_{L_{f_2}} \tag{4.42a}$$

$$i_{\text{diff}} = \tfrac{1}{2}\left(i_{L_{f_1}} - i_{L_{f_2}}\right) \tag{4.42b}$$

where i_{sum} is the combined output filter current, and i_{diff} is the unwanted circulating current in the filter inductors. The corresponding transformation for the input quantities is given by

$$u_{\text{avg}} = \tfrac{1}{2}\left(u_{\text{sn}_1} + u_{\text{sn}_2}\right) \tag{4.43a}$$

$$u_{\text{diff}} = u_{\text{sn}_1} - u_{\text{sn}_2} \tag{4.43b}$$

$$u_{\text{bias}_1} = u_{a_1} - u_{\text{sn}_1} \tag{4.43c}$$

$$u_{\text{bias}_2} = u_{a_2} - u_{\text{sn}_2}. \tag{4.43d}$$

The waveforms after variable transformation are shown in the right-hand graphs of Figure 4.13. From Figure 4.13a, it can be seen that a low current ripple of i_{L_a} is obtained when applying the proposed modulation on the ABDB converter. Both inductors L_{f_x} carry approximately half the current compared to the conventional DB with interleaved voltages, see Figure 4.8b. Furthermore, the inductors L_{a_x} can be designed much smaller than the filter inductors L_{f_x}. This is because the proposed PWM scheme in combination with the small bias voltage that is required to overcome the losses in the switches, diodes and auxiliary inductors, results in a very small volt-second product. Both , a three-level u_{avg} with double frequency.

The value of L_a that produces the smallest total inductor volume may not be immediately clear, since decreasing of L_{a_x} results in a higher $\Delta i_{L_{a_x}}$, which in turn needs to be compensated by increasing i'_{th} as will be shown in Chapter 5.

4.4 Summary

This chapter introduces the DB and two derived topologies, and shows their relation to the conventional canonical cell. Furthermore, the notation and variable transformations that will be used in the remainder of this thesis are given. The DB and its derivatives do not suffer from distortion due to the blanking time that is normally needed for converters based on conventional switching legs. Furthermore, the DB is robust for shoot-through, making it more reliable. Both the DB and ABDB are treated in detail in this chapter.

It is shown that high output quality requires that the DB switching legs operate in CCM by allowing a bias current, and that the DB legs allow overlapping gating signals, resulting in additional degrees of freedom for PWM generation. Moreover, different PWM and bias current modulation strategies are proposed.

The DB converter has more losses than its conventional equivalent switching leg. However, since the integrated antiparallel diodes of the switches are not used, the DB allows separate optimization of the discrete diodes and switches, which is, in case of MOSFET switches, not possible in the conventional switching leg.

It should again be noted the DB switching leg is a standard building block that can be used to replace a conventional switching leg in many topologies, as in parallel- and series-connected half- and full-bridge converters, and other multi-level topologies like the flying-capacitor or neutral-point-clamped converter.

Chapter 5

Volume reduction of the inductive components

"Beauty depends on size as well as symmetry."

(Aristotle)

Abstract — This chapter focuses on the selection of the inductive components. The combination of interleaved voltages and coupled inductors is investigated, with the aim to integrate the functionality of both the filter and bias-current inductors in a single coupled device, while reducing the total volume of the inductive components. It is shown that combining coupled inductors with non-interleaved voltages results in a significant reduction of the inductor volume. However, the power density of the DB converter remains lower than its conventional equivalent HB. The total inductor volume of the ABDB is investigated as well, showing that the total inductor volume for this circuit is similar to that of the DB.

Contributions of this chapter are published in:

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Volume reduction of opposed current converters through coupling of inductors and interleaved switching," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 852–857.
- J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. A. Lomonova, "High precision switched-mode amplifier with an auxiliary bias circuit," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

5.1 Introduction

In Chapter 4 two topologies were introduced that do not suffer from the effects of blanking time, and which are robust for shoot-through current. These converters consist of parallel-connected sets of P- and N-cells [116]. Each cell consists of one diode and switch and allows, therefore, only unidirectional power flow. The combination of a P- and N-cell, which became known as OCC, and DB in [105] and [52] respectively, supports bi-directional power flow. Each DB leg has the same number of diodes and switches as a conventional half-bridge leg (HB), as shown in Figure 4.1d, however, it requires one additional inductor resulting in a possibly increased volume.

Attempts have already been made to reduce the volume of the DB by means of coupling of inductors. In [16, 87] and [131] tight coupling is suggested to reduce the volume of the passive components of the DB switching leg. In [82] the full-bridge equivalent DB is considered, and crosswise coupling between two DB legs is suggested by means of common-mode chokes. Both proposed methods consider only the inductance required to prevent shoot-through currents and, therefore, require an additional filter inductor to achieve a high-quality, smooth, output voltage.

It should be mentioned that the method proposed in [82] is limited to full-bridge equivalent circuits DB, due to the crosswise coupling between DB legs. In this chapter only a single DB leg is considered, therefore, the method discussed in [82] will not be investigated further.

In this chapter, the selection of the inductive components based on the area-product method is treated. The combination of interleaved voltages and coupled DB filter inductors is explored with the aim to reduce the volume of the passive components while integrating the inductance required to prevent shoot-through current and filtering in a single device. Furthermore, the total inductor volume of the ABDB is determined and compared to that of the DB.

5.2 Selecting the passive components

Selection of the passive component values in power converters is all but straightforward. Different design approaches exist, such as methods based on load step behavior for power supplies [9, chapter 1], power bandwidth, losses, and volume. Most approaches focus on the inductive components, which can be categorized in two groups; namely, methods that include optimization processes, as in [72], and

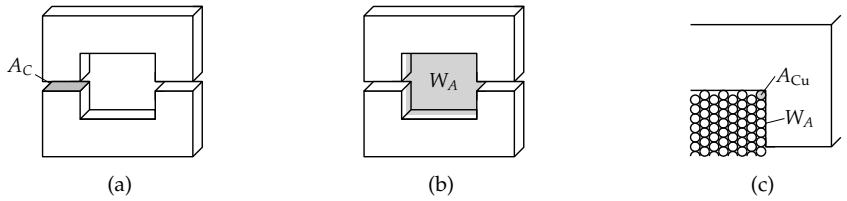


Figure 5.1: Area product geometric parameters.

methods that rely on closed-form equations like the power-bandwidth approach as in [123].

In this section the area-product method is used to determine the volume of the filter inductors. The area product (A_P) treated in [21] and [61] results in a closed-form expression that can be used to analyze the inductor volume. The A_P is the product of the effective core area (A_C) and the winding area (W_A), as illustrated in Figures 5.1a and 5.1b, and is given by

$$A_P = \frac{L}{\hat{B} J K_{\mathrm{u}}} \hat{\imath} I \tag{5.1}$$

where L is the inductance, $\hat{B}$ is the peak magnetic flux density, J is the RMS current density in the wire of the inductor, and K_{u} is the window utilization, which is the ratio of the winding area and the number of windings times the wire cross-sectional area A_{Cu}, as indicated in Figure 5.1c. The peak and RMS current are represented by $\hat{\imath}$ and I, respectively. The inductor volume can be estimated from the A_P by

$$V_L \approx K_{\mathrm{vol}} A_P^{3/4} \tag{5.2}$$

where K_{vol} represents the core's geometric constant.

As can be seen from (5.1), the area product takes only the peak flux density and copper losses into account. Core losses, eddy-current losses, skin effect, proximity effect and leakage flux are neglected in the area product pur sang. Moreover, a homogeneous magnetic flux distribution in the core is assumed. Still the area product can be a useful tool to compare inductor volumes or to make an initial design that can be further optimized [63, page 146 to 157]. A derivation of the area product is included in Appendix D.1.

5.3 Integrated-bias dual-buck converter

To determine the area product of the filter inductors (L_f) of the conventional DB, as depicted in Figure 4.5, first, the peak and RMS currents need to be expressed in terms of a-priori known design parameters. The inductor current of switching converters can typically be expressed in a sum of the periodic average $\langle i_{L_f} \rangle$ and a high-frequency ripple ($\tilde{i}$) due to switching.

To simplify the analysis, from here on i_{out} is assumed sinusoidal, and the inductor current ripples are assumed triangular. Furthermore, the inductor current ripple is assumed to be eliminated completely from i_{out} by the output filter (L_{f_x}, C_f). With these assumptions the maximum filter inductor current can be approximated by

$$\hat{i}_{L_f} \approx \hat{i}_{\text{out}} + (1 + \lambda_{\text{th}})\, \hat{\Delta} i_{L_f} \tag{5.3}$$

where $\hat{i}_{\text{out}}$ is the maximum expected output, $\hat{\Delta} i_{L_f}$ the maximum inductor current ripple amplitude, and $\lambda_{\text{th}} = {}^{i_{\text{th}}}/_{\hat{\Delta} i_{L_f}}$. The parameter λ_{th} adds the offset current necessary to prevent DCM, as explained in Section 4.2, and is equal to or greater than one. It should be noted that it is assumed here that the peak output current coincides with the peak inductor current ripple, which is worst-case and only valid for purely inductive loads. Therefore, a higher penalty than absolutely necessary is applied to the inductor current ripple in case of resistive loading.

Using the same notation as in (5.3), the RMS inductor current becomes

$$I_{L_f} \approx \begin{cases} \sqrt{\frac{3}{8}\hat{i}_{\text{out}}^2 + \left(\frac{1}{3} + \lambda_{\text{th}}^2\right)\left(\hat{\Delta} i_{L_f}\right)^2 + \hat{i}_{\text{out}} \lambda_{\text{th}} \hat{\Delta} i_{L_f}}, & \text{constant bias} \\ \sqrt{\frac{1}{4}\hat{i}_{\text{out}}^2 + \left(\frac{1}{3} + \lambda_{\text{th}}^2\right)\left(\hat{\Delta} i_{L_f}\right)^2 + \frac{2}{\pi}\hat{i}_{\text{out}} \lambda_{\text{th}} \hat{\Delta} i_{L_f}}, & \text{modulated bias} \end{cases} \tag{5.4}$$

where it is supposed that the inductor current ripple amplitude is at its maximum.

In practice, the inductor current ripple amplitude varies as function of the operating point. Therefore, also in the RMS term a higher penalty on inductor current ripple is applied. The conservativeness of the A_P for large $\hat{\Delta} i_{L_f}$ partly compensates for the frequency-dependent losses that are neglected in the area product. The derivation of the peak and RMS currents is included in Appendix D.2.

In view of (4.3b) L_f can be expressed in terms of $\hat{\Delta} i_{L_f}$, which in turn can be written

in terms of $\hat{i}_{\text{out}}$ as

$$\hat{\Delta} i_{L_f} = \lambda_{L_f} \hat{i}_{\text{out}}. \tag{5.5}$$

Finally, by combining the results of (5.1), (5.3), (5.4), and (5.5) the area product of the DB filter inductor becomes

$$A_{P_{\text{const}}} = \frac{U_{\text{DC}} \hat{i}_{\text{out}} T_{\text{sw}}}{8 \hat{B} J K_{\text{u}}} \left(\lambda_{L_f}^{-1} + \lambda_{\text{th}} + 1 \right) \sqrt{\tfrac{3}{8} + \lambda_{\text{th}}^2 \lambda_{L_f}^2 + R_R \tfrac{1}{3} \lambda_{L_f}^2 + \lambda_{\text{th}} \lambda_{L_f}} \tag{5.6}$$

for a constant bias current, and

$$A_{P_{\text{mod}}} = \frac{U_{\text{DC}} \hat{i}_{\text{out}} T_{\text{sw}}}{8 \hat{B} J K_{\text{u}}} \left(\lambda_{L_f}^{-1} + \lambda_{\text{th}} + 1 \right) \sqrt{\tfrac{1}{4} + \lambda_{\text{th}}^2 \lambda_{L_f}^2 + R_R \tfrac{1}{3} \lambda_{L_f}^2 + \tfrac{2}{\pi} \lambda_{\text{th}} \lambda_{L_f}} \tag{5.7}$$

for modulated bias current. Similarly, without further details, the area product for the filter inductor of a conventional HB [63, page 146] can be determined to be

$$A_{P_{\text{HB}}} = \frac{U_{\text{DC}} \hat{i}_{\text{out}} T_{\text{sw}}}{8 \hat{B} J K_{\text{u}}} \left(\lambda_{L_{\text{HB}}}^{-1} + 1 \right) \sqrt{\tfrac{1}{2} + R_R \tfrac{1}{3} \lambda_{L_{\text{HB}}}^2} \tag{5.8}$$

where $\lambda_{L_{\text{HB}}}$ is the inductor ripple ratio of the HB filter inductor, which in turn is given by $\lambda_{L_{\text{HB}}} = \hat{\Delta} i_{L_{\text{HB}}} / \hat{i}_{\text{out}}$.

A resistance ratio $R_R = R_{\text{AC}} / R_{\text{DC}}$ is added to the area products given in (5.6), (5.7), and (5.8) to incorporate the skin and proximity effects as proposed in [63, page 149]. Inclusion of the core losses is challenging since the loss models heavily depend on the material used, and is, therefore, omitted. The area products presented above are, therefore, only valid for saturation-limited designs.

The area products given in (5.6) to (5.8) can be minimized as function of λ_{L_f} or $\lambda_{L_{\text{HB}}}$. The other parameters are constants that depend on the converter specifications and on the magnetic core, bobbin, and wire used, and can be assumed constant when comparing the area products given in (5.6) to (5.8).

The optimal inductor current ripple ratio, that is the λ_{L_x} that minimizes the area product, can be determined by solving

$$0 = \frac{\mathrm{d} A_{P_x}(\lambda_{L_x})}{\mathrm{d} \lambda_{L_x}} \tag{5.9}$$

which, for the HB, leads to $\lambda_{L_{\text{HB}}} = \sqrt[3]{3 R_{\text{DC}} / 2 R_{\text{AC}}}$. For the DB, however, the corresponding results are lengthy, not insightful, and, therefore, not included in this thesis. Instead the results are visualized in Figure 5.2, which depicts the relative

core volumes as a function of λ_{L_f}, for both $R_R = 2$ and $R_R = 10$ and $\lambda_{\text{th}} = 1.5$, which are practical values. The volumes are determined using (5.2), assuming equal magnetic core geometric constants. Furthermore, for the DB, inductor volumes are multiplied by a factor of two and all inductor volumes are normalized to the volume for the conventional HB, as illustrated in Figure 4.1d without filter capacitor, with $\lambda_{L_{\text{HB}}} = 0.25$, which is again a practical value.

From Figure 5.2 it can be seen that the minimum magnetic volume for the HB occurs at $\lambda_{L_{\text{HB}}} = 0.91$ with $R_R = 2$, which is almost in the ZVS region [95], and $\lambda_{L_{\text{HB}}} = 0.53$ with $R_R = 10$. Furthermore, the core volume changes only slightly over a broad range of $\lambda_{L_{\text{HB}}}$.

The previous results are valid for saturation-limited magnetic designs. Designs that are limited by core losses require a larger penalty on high current ripple, and consequently magnetic flux ripple. In [63, page 150] an example is given how to include core losses in the area product. However, also in designs limited by saturation it is beneficial to prevent large inductor current ripple because of the associated increased losses in the semiconductor switches and filter capacitors. Therefore, λ_{L_x} should be chosen to minimize the volume of the complete converter, and not only to minimize the inductor volume.

From (5.6) to (5.8) it can be seen that λ_{L_x} impacts the RMS current, which in turn determines the conduction losses in various other components in a converter. In case of the HB, when $\lambda_{L_{\text{HB}}} > 1$, i.e. operation at ZVS, the RMS contribution of the switching ripple becomes larger than the RMS contribution of the output current if $R_R < 3/2$. However, it results in nearly zero switching losses. On the other hand, if $\lambda_{L_{\text{HB}}} < 1$ switching losses occur, and any additional inductor current ripple will add to the losses in the semiconductor switches, diodes and other passive components. For hard-switched converters $\lambda_{L_{\text{HB}}}$ should be chosen such that the overall volume is minimized. In practice, for hard-switched converters, $\lambda_{L_{\text{HB}}}$ is chosen between 0.1 and 0.3.

The DB has a smaller range over which λ_{L_f} can be varied without significantly changing the total inductor volume. This is due to the offset current (i_{th}) that is required to guarantee CCM. From Figure 5.2 it can be seen that a DB requires approximately 3 times more inductor volume than its equivalent conventional HB. The relative core volumes for the DB depicted in Figure 5.2 are valid for both non-interleaved and interleaved operation since the area products are determined based on the current in one DB filter inductor.

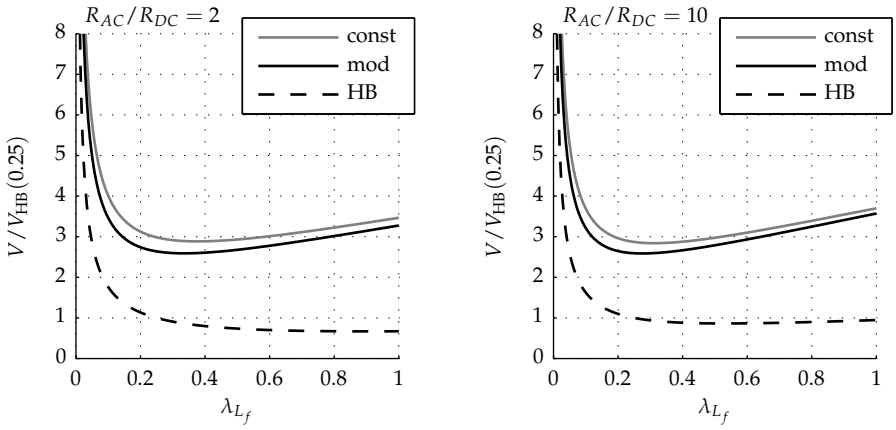


Figure 5.2: Relative inductor volume of a DB as a function of λ_{L_f} with $\lambda_{\mathrm{th}} = 1.5$, and for (a) $R_R = 2$ and (b) $R_R = 10$.

Figure 5.3: Coupled DB filter inductor with (a) positive coupling, and (b) negative coupling.

5.3.1 Coupled inductors

Coupled inductors are often used in parallel-connected converters with interleaved switching patterns in order to reduce the volume of the inductive components, to reduce losses, and improve dynamic behavior [9, 16, 82, 87, 140]. In [16] and [87] tight magnetic coupling is applied to the DB leg to reduce the total volume of inductive components. In [82] coupling is applied between inductors $L_{f_{1p}}$ and $L_{f_{2n}}$, and $L_{f_{2p}}$ and $L_{f_{1n}}$, where p and n denote the positive and negative side of a full-bridge equivalent DB. Both proposed methods only consider the inductance required to prevent shoot-through currents and, therefore, still require an additional filter inductor (L_f) when high-quality smooth output voltage is required. In this section weak magnetic coupling is exploited to achieve filtering and limitation of the shoot-through current in a single integrated inductive component. This can be realized by applying partly coupled DB filter inductors, as depicted in Figure 5.3.

The relation between the voltages and currents of the coupled inductor shown in Figure 5.3 are given by

$$\begin{pmatrix} u_{\mathrm{sn}_1} - u_{C_f} \\ u_{\mathrm{sn}_2} - u_{C_f} \end{pmatrix} = \begin{pmatrix} L & \pm M \\ \pm M & L \end{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_{L_{f_1}} \\ i_{L_{f_2}} \end{pmatrix} \tag{5.10}$$

where equal number of turns is assumed, L and M represent the inductance and mutual inductance, and the polarities $\pm$ indicate positive or negative coupling, respectively. The mutual inductance (M) equals $k_f L$ where k_f is the coupling coefficient, which lies in the range $0 \leq k_f \leq 1$.

When applying the variable transformations given in (4.9) and (4.10), (5.10) becomes

$$\begin{pmatrix} u_{\mathrm{avg}} - u_{C_f} \\ u_{\mathrm{bias}} \end{pmatrix} = \begin{pmatrix} L_{\mathrm{sum}} & 0 \\ 0 & L_{\mathrm{bias}} \end{pmatrix} \frac{\mathrm{d}}{\mathrm{d}t} \begin{pmatrix} i_{\mathrm{sum}} \\ i_{\mathrm{bias}} \end{pmatrix} \tag{5.11}$$

with

$$L_{\mathrm{sum}} = \tfrac{1}{2} \left(1 + \kappa_f\right) L \tag{5.12}$$

$$L_{\mathrm{bias}} = 2 \left(1 - \kappa_f\right) L \tag{5.13}$$

and where κ_f represents the coupling coefficient including the sign of the coupling ($\kappa_f = \pm k_f$).

From the diagonal matrix form in (5.11) it can be seen that the suggested coupled inductors have no effect on the proposed decoupling given in (4.9) and (4.10). Moreover, by adjusting the coupling coefficient (κ_f), the ratio between L_{sum} and L_{bias} can be set arbitrarily.

5.3.2 Area product for coupled inductors

In this section the required volume of the inductive component for a DB switching leg using a single coupled inductor with variable coupling coefficient (κ_f) is compared to the volume of the inductive component required for a HB. Figure 5.4 depicts such a coupled inductor and its corresponding reluctance model. Due to the gap in all three legs, the coupling coefficient can be set arbitrarily by varying the gap lengths in the outer legs with respect to the gap length in the center leg, and the sign of the coupling is set by the changing the direction of the turns in one of the inductors. Notice that $\kappa_f = 0$ and $|\kappa_f| = 1$, are not possible in practice

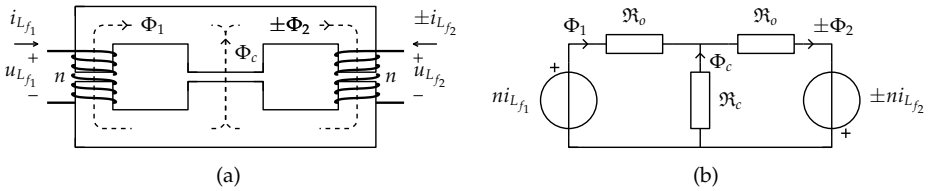


Figure 5.4: DB coupled inductor (a) and corresponding reluctance model (b), n is the number of windings.

due to the finite permeability of the core material.

When assuming a homogeneous magnetic field distribution the fluxes in the outer legs of the coupled inductor are given by

$$\begin{pmatrix}\Phi_1\\ \Phi_2\end{pmatrix} = \frac{n}{\Re_o\left(\Re_o+2\Re_c\right)}\begin{pmatrix}\Re_c+\Re_o & \pm\Re_c\\ \pm\Re_c & \Re_c+\Re_o\end{pmatrix}\begin{pmatrix}i_{L_{f_1}}\\ i_{L_{f_2}}\end{pmatrix} \tag{5.14}$$

where Φ_x are the magnetic fluxes and $\Re_x$ are the corresponding magnetic core reluctances as depicted in Figure 5.4b. The flux in the center leg equals $\Phi_C = -\Phi_1 \pm \Phi_2$. Equation (5.14) can be expressed in terms of L and M as

$$\begin{pmatrix}\Phi_1\\ \Phi_2\end{pmatrix} = \frac{1}{n}\begin{pmatrix}L & \pm M\\ \pm M & L\end{pmatrix}\begin{pmatrix}i_{L_{f_1}}\\ i_{L_{f_2}}\end{pmatrix} \tag{5.15}$$

and in turn by applying the proposed variable transformation (5.15) becomes

$$\begin{pmatrix}\Phi_1\\ \Phi_2\end{pmatrix} = \frac{1}{n}\begin{pmatrix}L_{\text{sum}} & \frac{1}{2}L_{\text{bias}}\\ L_{\text{sum}} & -\frac{1}{2}L_{\text{bias}}\end{pmatrix}\begin{pmatrix}i_{\text{sum}}\\ i_{\text{bias}}\end{pmatrix}. \tag{5.16}$$

The maximum fluxes in both of the outer core legs are equal when assuming sinusoidal excitation, thus only one outer leg needs to be considered. By using (5.12), (5.13), and

$$\Phi = BA_C \tag{5.17}$$

equation (5.16) can be rewritten in terms of L, κ_f, $\hat{B}$, and A_C, resulting in the following expression for the effective core area

$$A_C = \frac{L}{\hat{B}n}\max_t\left(\tfrac{1}{2}\left(1+\kappa_f\right)i_{\text{sum}}(t) + \left(1-\kappa_f\right)i_{\text{bias}}(t)\right). \tag{5.18}$$

The winding area for one of the inductors is determined by

$$K_{\mathrm{u}} W_A = n A_{\mathrm{Cu}} \tag{5.19}$$

where A_{Cu} is the wire cross-sectional area. When assuming again a sinusoidal output waveform the RMS currents in both inductors become equal and (5.19) can be rewritten as

$$W_A = \frac{n}{J K_{\mathrm{u}}} I_{L_f} \tag{5.20}$$

which, in turn, can be expressed in terms of i_{sum} and i_{bias} as

$$W_A = \frac{n}{J K_{\mathrm{u}}} \sqrt{\frac{1}{T} \int_{t}^{t+T} \left(\tfrac{1}{2} i_{\mathrm{sum}}(\tau) + i_{\mathrm{bias}}(\tau) \right)^2 \mathrm{d}\tau} \tag{5.21}$$

by again applying the proposed variable transformation.

Finally, by using (5.12) the area product becomes

$$A_{P_{\mathrm{DB}}} = \frac{2 L_{\mathrm{sum}}}{\hat{B} J K_{\mathrm{u}}} \frac{1}{1+\kappa} \max_t \left(\left(1+\kappa_f\right) \frac{1}{2} i_{\mathrm{sum}}(t) + \left(1-\kappa_f\right) i_{\mathrm{bias}}(t) \right) \times \sqrt{\frac{1}{T} \int_{t}^{t+T} \left(\tfrac{1}{2} i_{\mathrm{sum}}(\tau) + i_{\mathrm{bias}}(\tau) \right)^2 \mathrm{d}\tau}. \tag{5.22}$$

The parts representing the peak and RMS currents in (5.22) can be expressed in terms of time-independent variables, as detailed in Appendix D.3, resulting in

$$A_{P_{\mathrm{DB}}} = \frac{U_{\mathrm{DC}} \hat{i}_{\mathrm{out}} T_{\mathrm{sw}}}{8 \hat{B} J K_{\mathrm{u}}} \frac{1}{1+\kappa} \hat{i}_{\mathrm{DB}} I_{\mathrm{DB}} \tag{5.23}$$

where the normalized peak and RMS currents ($\hat{i}_{\mathrm{DB}}$ & I_{DB}) are given by

$$\hat{i}_{\mathrm{DB}} = 2 \lambda_{\mathrm{sum}}^{-1} + \left(1-\kappa_f\right) \lambda_{\mathrm{th}} + \left(1+\kappa_f\right) \tag{5.24}$$

and

$$I_{\mathrm{DB}} = \begin{cases} \sqrt{\frac{3}{8} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)\frac{1}{4}\lambda_{\mathrm{sum}}^2 + \frac{1}{2}\lambda_{\mathrm{th}}\lambda_{\mathrm{sum}}}, & \text{constant bias} \\ \sqrt{\frac{1}{4} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)\frac{1}{4}\lambda_{\mathrm{sum}}^2 + \frac{1}{\pi}\lambda_{\mathrm{th}}\lambda_{\mathrm{sum}}}, & \text{modulated bias} \end{cases} \tag{5.25}$$

for non-interleaved switch-node voltages u_{sn}, and

$$\hat{i}_{\mathrm{DB}} = \tfrac{1}{2}\lambda_{\mathrm{sum}}^{-1} + \left(1-\kappa_f\right)\max_{m_{\mathrm{avg}}}\left(\left(\frac{1+\kappa_f}{1-\kappa_f} + \lambda_{\mathrm{th}}\right)\left(|m_{\mathrm{avg}}| - m_{\mathrm{avg}}^2\right) + \ldots \right.$$
$$\left. \left(1+\lambda_{\mathrm{th}}\right)\frac{1+\kappa_f}{1-\kappa_f}\left(1-|m_{\mathrm{avg}}|\right)\right) \tag{5.26}$$

and

$$I_{\mathrm{DB}} = \begin{cases} \sqrt{\frac{3}{8} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)4\lambda_{\Delta}^2\lambda_{\mathrm{sum}}^2 + 2\lambda_{\mathrm{th}}\lambda_{\Delta}\lambda_{\mathrm{sum}}}, & \text{constant bias} \\ \sqrt{\frac{1}{4} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)4\lambda_{\Delta}^2\lambda_{\mathrm{sum}}^2 + \frac{4}{\pi}\lambda_{\mathrm{th}}\lambda_{\Delta}\lambda_{\mathrm{sum}}}, & \text{modulated bias} \end{cases} \tag{5.27}$$

for interleaved switch-node voltages u_{sn}. The ratio between λ_{sum} is given by

$$\lambda_{\mathrm{sum}} = \frac{\hat{\Delta}i_{\mathrm{sum}}}{\hat{i}_{\mathrm{out}}} \tag{5.28}$$

and λ_{Δ} for interleaved u_{sn} equals

$$\lambda_{\Delta} = \max_{m_{\mathrm{avg}}}\left(\frac{1+\kappa_f}{1-\kappa_f} - \frac{2\kappa_f}{1-\kappa_f}|m_{\mathrm{avg}}| - m_{\mathrm{avg}}^2\right). \tag{5.29}$$

Finally, it should again be noted that $\hat{i}_{\mathrm{DB}}$ and I_{DB} are normalized to $\hat{i}_{\mathrm{out}}$, being thus dimensionless.

Using (5.23) the total inductor volume of the DB with coupled inductors becomes

$$V_{\mathrm{DB}} = 2K_{\mathrm{vol}}\left(A_{P_{\mathrm{DB}}}(\lambda_{\mathrm{sum}}, \kappa_f)\right)^{3/4}. \tag{5.30}$$

Figure 5.5 illustrates the inductor volume ratio between the DB with modulated bias current and a conventional HB when assuming equal core volumetric constants, $\lambda_{\mathrm{th}} = 1.5$, $R_R = 6$, and again it is assumed that $\lambda_{L_{\mathrm{HB}}} = 0.25$. The values

of λ_{th} and R_R are the same as in the experimental setup used to verify the results later in this section.

For non-interleaved switch-node voltages, as depicted in Figure 5.5a, κ_f should be chosen close to 1. Negative coupling results in a larger volume because L_{sum} decreases for smaller κ_f, which, in turn, results in larger $\hat{\Delta}i_{\text{sum}}$, which, in turn, has to be compensated by increasing i_{th}. Furthermore, it should be noted that κ_f should always be smaller than one, to ensure sufficient L_{bias} to prevent discontinuous current.

For interleaved switch-node voltages, as depicted in Figure 5.5b, the minimum relative inductor volume occurs for κ_f close to zero, thus for almost separate inductors. The inductor volume becomes infinite for both $\kappa_f = \pm 1$.

Figure 5.6a depicts the relative inductor volume for the value of λ_{sum} that minimizes the inductor volume. For non-interleaved switch-node voltages and modulated bias current, the relative inductor volume approaches 1.5 for κ_f just under 1. The minimum inductor volume for interleaved switch-node voltages occurs for $\kappa_f \approx -0.25$.

Chapelsy *et al.* compared the total weight of the inductive components for a DB switching leg with interleaved switching to the weight of the filter inductor of a conventional HB in [16]. For the case studied there the weights were comparable. Figure 5.6a also depicts the relative volume that can be obtained by using a coupled inductor with κ_f close to minus one for the bias inductance in combination with a separate filter inductor for the ripple component of i_{sum}, as proposed in [16]. Those results are calculated using the area-product method as detailed in Appendix D.4. The method proposed in [16] results in approximately 30 % less inductor volume for interleaved switch-node voltages and approximately 10 % less volume for non-interleaved switch-node voltages and is, therefore, definitely the best method to reduce the volume of the inductive components in a DB. However, contrary to the claims of [16], volume and, therefore, also the weight of the inductive components will increase compared to the HB.

It should be noted that the circuit proposed in [16] requires two components instead of one, as in the coupled case for non-interleaved switch-node voltages described in this chapter. Even though the total volume for [16] is slightly smaller, the required board area for two discrete components might be larger than one component.

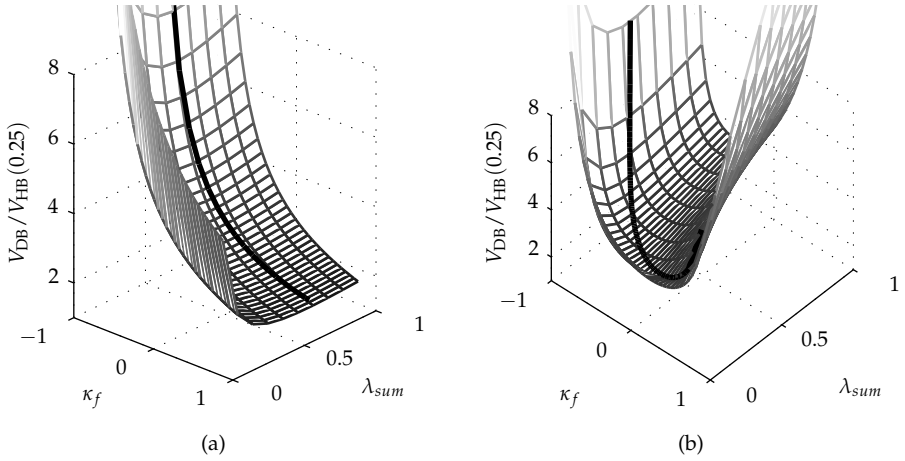


Figure 5.5: Relative coupled inductor volume for a DB with modulated bias current as function of κ_f and λ_{sum} with $\lambda_{\text{th}} = 1.5$ and $R_R = 6$, for (a) non-interleaved, and (b) interleaved u_{sn}. The black lines indicate the λ_{sum} that minimizes the relative inductor volume for a given κ_f.

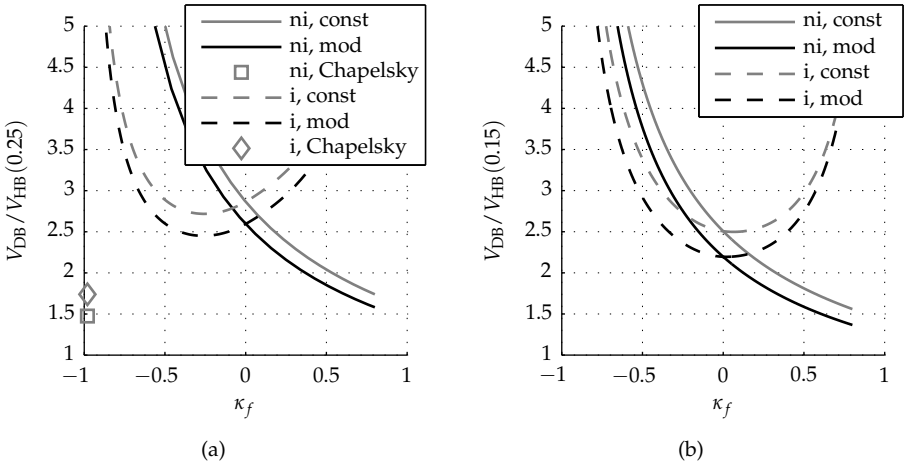


Figure 5.6: Relative coupled inductor volume for a DB as function of κ_f for $\lambda_{\text{th}} = 1.5$ and $R_R = 6$, with (a) the λ_{sum} that minimizes the inductor volume, where Chapelsky refers to the results of Chapelsky *et al.* presented in [16], and (b) with $\lambda_{\text{sum}} = 0.3$ for non-interleaved u_{sn} and $\lambda_{\text{sum}} = 0.075$ for interleaved u_{sn}. In the legend 'ni' and 'i' represent non-interleaved and interleaved u_{sn}, respectively, and 'const' and 'mod' denote constant and modulated bias current, respectively.

Table 5.1: Magnetic core material specifications.

Manufacturer	Magnetics, Inc.
Type	0078737A7
Material	XFlux
Relative permeability	60
Effective cross section	497 mm^2
Effective length	184 mm
Nominal inductance	204 nH/Turns^2

5.3.3 Results

A prototype DB was built using available power components with control and PWM generation implemented on a dSPACE prototyping system. The control hardware consists of a processor board and an analog capture board for the measurement and control, and a field-programmable gate array (FPGA) module for PWM generation. Two sets of inductors were constructed to compare the resulting inductor volume in case of non-interleaved switch-node voltages with coupled filter inductors and interleaved switch-node voltages with separate inductors. For the interleaved case separate inductors were chosen because no significant decrease of volume is expected when coupled inductors are used. Details about the experimental DB setup are described in Appendix A.4.

The inductors were designed for a maximum current of 40 A and $\lambda_{L_f} = 0.15$ for each inductor. This translates to $\lambda_{\text{sum}} = 0.3$ for non-interleaved switch-node voltages and $\lambda_{\text{sum}} = 0.075$ for interleaved switch-node voltages, respectively. The inductor volume ratios for that case are depicted in Figure 5.6b. It shows that the volume ratio between the coupled and separate inductors is 0.64. Notice that the DB inductor volumes are shown normalized to a HB with $\lambda_{L_{\text{HB}}} = 0.15$.

Both inductors are based on the same toroidal core with distributed air gap, wound with litz wire with 0.28 mm diameter and 100 strands. The separate and coupled inductors have 32 and 23 turns, respectively, resulting in $L_{\text{sum}} = 104\,\mu\text{H}$ for separate inductors, and $L_{\text{sum}} = 108\,\mu\text{H}$ and $\kappa_f = 0.75$ for coupled inductors. The coupling coefficient was set by partial winding of the toroidal core, as can be seen in Figure 5.7. Details about the used magnetic core are given in Table 5.1, and Table 5.2 contains a summary of the calculated and obtained parameters.

Figure 5.7 depicts the inductors which were used for the experimental verification. The inductor shown on the right-hand side is the coupled filter inductor, and the inductors depicted on the left-hand side are the separate inductors. The

Table 5.2: Calculated and (measured) inductor parameters.

	Turns	κ_f	L_{f_1} (µH)	L_{sum} (µH)	L_{bias} (µH)
Separate	32	-	208 (206)	104 (103)	416 (412)
Coupled	23	0.76 (0.71)	123 (129)	108 (111)	59 (74)

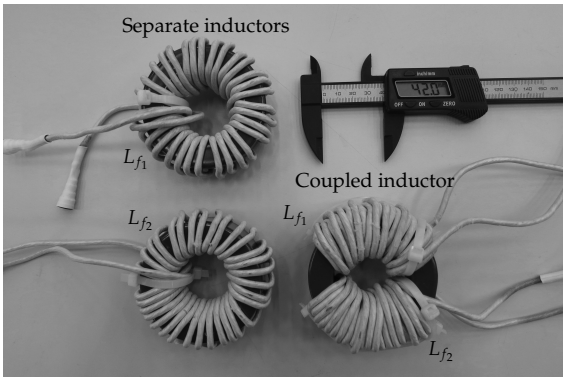


Figure 5.7: Coupled inductors with $\kappa_f = 0.75$, $L_{\text{sum}} = 108\,\mu\text{H}$, and $L_{\text{bias}} = 62\,\mu\text{H}$ designed for non-interleaved u_{sn}, and separate inductors with $L_f = 208\,\mu\text{H}$ designed for interleaved u_{sn}.

volume ratio of the coupled and separate inductors after correcting for $\hat{B}$ is 0.57, which is 11 % smaller than the 0.64 that can be read from Figure 5.6b. The mismatch between the calculated and realized volume can be attributed to the difference in core volumetric constant, which in turn is caused by the different winding method of the inductors. The separate inductors have one layer of turns distributed over the entire core and the coupled inductors have multiple layers of windings distributed over part of the core to set κ_f.

Simulation results were compared to measurements obtained from an experimental DB setup based on IGBT switches, as described in Appendix A.4. Figure 5.8 shows simulation results for both coupled inductors with non-interleaved switch-node voltages and separate inductors with interleaved switch-node voltages, using the inductors described in Table 5.2, with $U_{\text{DC}} = 100\,\text{V}$, 10 kHz switching frequency, and 10 A output current. Figure 5.8 shows the relations between voltages and currents before and after application of the variable transformations given in (4.9) and (4.10).

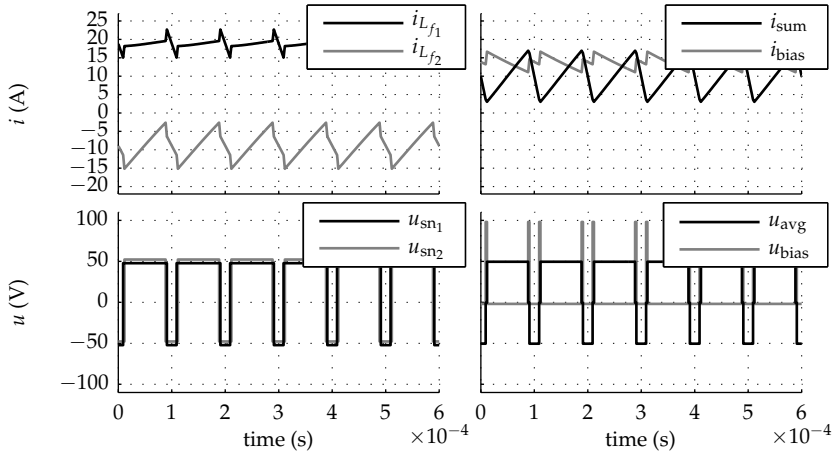
The simulated voltages and currents for non-interleaved switch-node voltages are depicted in Figure 5.8a. It can be seen that there is a considerable current rip-

ple present on i_{bias}. The presence of this ripple component on i_{bias} is due to the required bias voltage that was assumed zero when determining the area products. In this case the bias voltage was 5 % of U_{DC}, which is relatively high, and κ_f was 0.75. The bias current ripple leads to more losses than included in the area product and should be small compared to the current ripple of i_{sum} for a fair comparison of the inductor volume using the method presented in this chapter. Therefore, when κ_f is chosen close to one, care should be taken about the bias voltage that is required to maintain CCM. In practice, κ_f should be chosen smaller than 0.8.

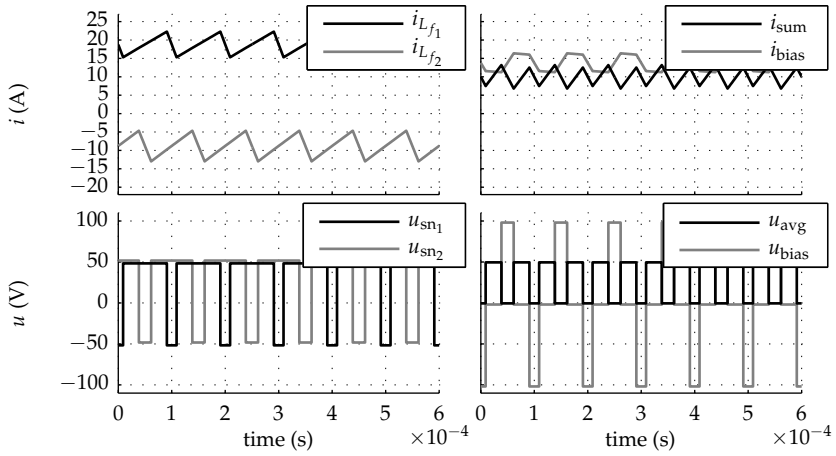
The results of the interleaved case, depicted in Figure 5.8b, are similar to the results depicted in Figure 4.8b and illustrate that interleaved switching results in unipolar u_{avg} with double effective switching frequency. Because of the interleaved currents the ripple amplitude of i_{sum} is half that of the individual filter inductor currents. Since the switch-node voltages are interleaved, the bias voltage is bipolar, resulting in considerable bias current ripple.

For separate inductors there is no significant interaction between the P-cell and N-cell of the DB. For coupled inductors, as depicted in Figure 5.8a, there is significant interaction between both cells. Figure 5.8a shows that the bias current ripple adds to the ripple component of $i_{L_{f_1}}$ and subtracts from $i_{L_{f_2}}$ for $m_{\text{avg}} > 0$. The opposite occurs for $m_{\text{avg}} < 0$. The offset current (i_{th}) should be adjusted for the bias current ripple such that CCM is guaranteed under all output conditions. Furthermore, there is a trade-off between the voltage ripple of u_{bias} and u_{avg}. Non-interleaved switch-node voltages result in a bipolar u_{avg} and unipolar u_{bias}, and interleaved switch-node voltages result in unipolar u_{avg} and bipolar u_{bias}. The effects of this trade-off on the output voltage spectrum will be treated in Chapter 7.

Figure 5.9 depicts the corresponding measurement results obtained using the experimental DB setup described in Appendix A.4. The voltage and currents after variable transformation, illustrated right, were calculated from the measured voltages and currents that are depicted left. From the voltage waveforms it can be seen that the switching legs have higher resistive losses than expected from the device specifications. This might be due to the connections, which were not taken into account. Also spikes are present on the measured voltages and currents, which are induced by the edges of switching voltages, and sampling of the analog-to-digital converters (ADCs) in the setup. Other than that the measured waveforms agree very well with the simulation results depicted in Figure 5.8.

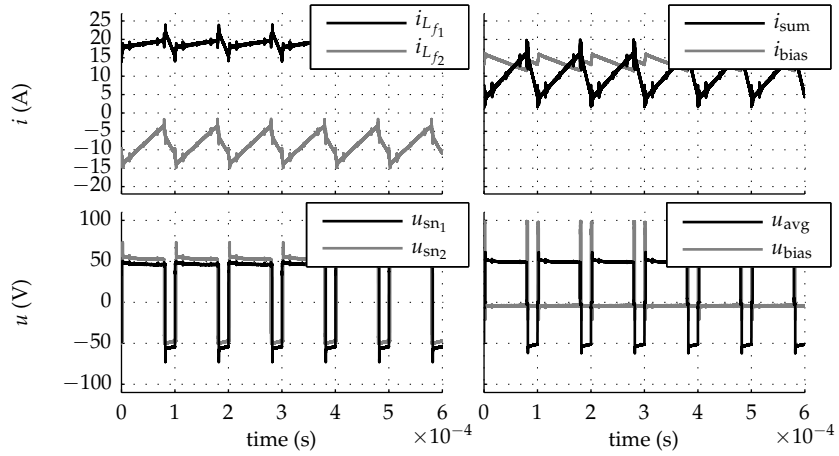


(a)

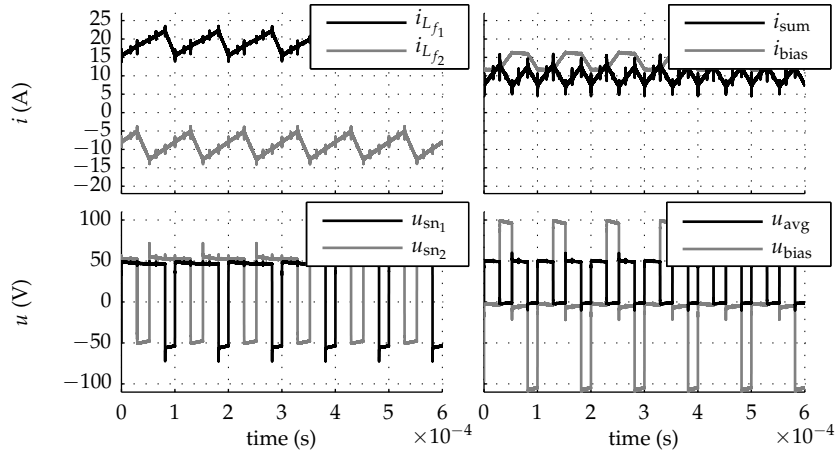


(b)

Figure 5.8: Simulated voltage and current waveforms for the DB, for (a) non-interleaved u_{sn} with $\kappa_f = 0.7$ and L_f, and (b) interleaved u_{sn} with $\kappa_f = 0$.



(a)



(b)

Figure 5.9: Measured voltage and current waveforms for the DB, for (a) non-interleaved u_{sn} with $\kappa_f = 0.7$ and L_f, and (b) interleaved u_{sn} with $\kappa_f = 0$.

5.4 Auxiliary-bias dual-buck converter

The filter inductors (L_{f_1} & L_{f_2}) of the ABDB ideally have equally shared interleaved currents as explained in Chapter 4. Moreover, the number of semiconductor switches and diodes are also the same as in two parallel-connected conventional HBs. Therefore, the increase in volume of the inductive components, in an ABDB, with respect to a conventional two-leg interleaved converter, can be determined from the ratio of the volumes of L_a and L_f, depicted in Figure 4.12. As in the previous section, the volume of both inductors will be determined using the area-product method.

5.4.1 Area products for the auxiliary bias DB inductors

When assuming steady-state operation and that the maximum output current coincides with the maximum current ripple, the peak currents of both L_{f_1} and L_{f_2}, and L_{a_x} can be written as

$$\hat{i}_{L_f} = \tfrac{1}{2}\hat{i}_{\text{out}} + \hat{\Delta}i_{L_f} \tag{5.31}$$

$$\hat{i}_{L_{a_2}} = \tfrac{1}{2}\hat{i}_{\text{out}} + (1+\lambda_{\text{th}})\hat{\Delta}i_{L_a} + \lambda_{\text{th}}\hat{\Delta}i_{L_f} \tag{5.32}$$

where $\check{i}_{L_{a_1}} = -\hat{i}_{L_{a_2}}$.

Furthermore, assuming sinusoidal output current and that the switching cycle time (T_{sw}) is much smaller than the cycle time of the sinusoidal reference, the RMS current becomes

$$I_{L_f} = \sqrt{\tfrac{1}{8}\hat{i}^2_{\text{out}} + \tfrac{1}{3}(\hat{\Delta}i_{L_f})^2} \tag{5.33}$$

$$I_{L_a} = \sqrt{\tfrac{1}{8}\hat{i}^2_{\text{out}} + \tfrac{1}{3}(\hat{\Delta}i_{L_a})^2 + \lambda^2_{\text{th}}(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f})^2 + \tfrac{2}{\pi}\hat{i}_{\text{out}}\lambda_{\text{th}}(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f})} \tag{5.34}$$

as explained in detail in Appendix D.5.

As in the previous section the current ripple amplitudes can be expressed in terms of maximum output current as

$$\hat{\Delta}i_{L_f} = \lambda_{L_f}\hat{i}_{\text{out}} \tag{5.35}$$

$$\hat{\Delta}i_{L_a} = \lambda_{L_a}\hat{i}_{\text{out}}. \tag{5.36}$$

Also the inductances L_a and L_f can be expressed in terms of supply voltage, T_{sw}, and maximum current ripple amplitude by using (4.37b), (4.39c), (5.35), and

(5.36). As a result the area products for both inductors become

$$A_{PL_f} = \frac{U_{\mathrm{DC}} T_{\mathrm{sw}} \hat{i}_{\mathrm{out}}}{8 \hat{B} J K_{\mathrm{u}}} \left(1 + \tfrac{1}{2}\lambda_{L_f}^{-1}\right) \sqrt{\tfrac{1}{8} + R_R \tfrac{1}{3}\lambda_{L_f}^2} \tag{5.37}$$

$$A_{PL_a} = \hat{m}_{\mathrm{bias}} \frac{U_{\mathrm{DC}} T_{\mathrm{sw}} \hat{i}_{\mathrm{out}}}{2 \hat{B} J K_{\mathrm{u}}} \left(1 + \tfrac{1}{2}\lambda_{L_a}^{-1} + \lambda_{\mathrm{th}}(1 + \lambda_{L_f}{\lambda_{L_a}}^{-1})\right) \times \ldots \sqrt{\tfrac{1}{8} + R_R \tfrac{1}{3}\lambda_{L_a}^2 + \lambda_{\mathrm{th}}^2(\lambda_{L_a} + \lambda_{L_f})^2 + \tfrac{2}{\pi}\lambda_{\mathrm{th}}(\lambda_{L_a} + \lambda_{L_f})} \tag{5.38}$$

where the resistance ratio R_R has been added to incorporate the skin and proximity effects to the area-product, as proposed in [63, page 149]. The core losses are not included, therefore, the area-products given in (5.37) and (5.38) are only valid for saturation-limited designs.

From (5.38) it can be seen that, when no bias voltage is needed, the volume of L_a can be made arbitrary small. This is because the modulation is chosen such that the voltage across the auxiliary inductor (L_a) becomes zero when no bias voltage is present. As a result, L_a can be chosen arbitrarily small when $\hat{m}_{\mathrm{bias}} = 0$. However, in practice bias voltages in the order of several percent of U_{DC} can be expected.

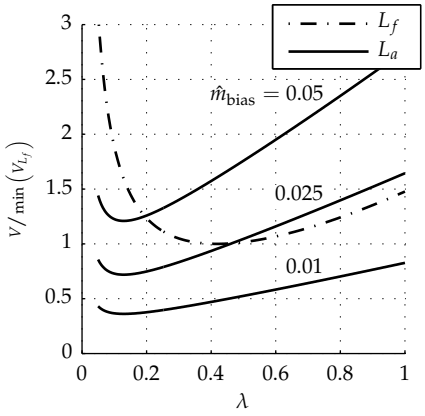
After some manipulation a compact analytical expression can be found for the value of λ_{L_f} that minimizes (5.37), which is given by

$$\lambda_{L_{f_{\mathrm{opt}}}} = \sqrt[3]{\frac{3}{16}\frac{R_{\mathrm{DC}}}{R_{\mathrm{AC}}}}. \tag{5.39}$$

The analytical result for the ripple ratio, λ_{L_a}, that minimizes A_{PL_a} is straightforward but lengthy and not detailed further here. More illustrating is Figure 5.10a, which depicts the resulting normalized volume of both L_f and L_a when assuming the same core geometric constant (K_{vol}) for both cores, and by choosing $\lambda_{\mathrm{th}} = 1.5$ together with $R_R = 2$, which matches the parameters of the experimental ABDB setup described Appendix A.4. From Figure 5.10a it can be seen that the auxiliary bias inductor is potentially smaller than the filter inductors.

The relative volume increase of the ABDB with respect to a conventional interleaved converter can be determined by combining the result of (5.39) with the area products of (5.37) and (5.38), resulting in

$$\frac{V_{L_a} + V_{L_f}}{\min\left(V_{L_f}\right)} = \frac{\left(A_{PL_f}(\lambda_{L_f})\right)^{3/4} + \left(A_{PL_a}(\lambda_{L_a}, \lambda_{L_f})\right)^{3/4}}{\left(A_{PL_f}(\lambda_{L_{f_{\mathrm{opt}}}})\right)^{3/4}} \tag{5.40}$$



(a)

Figure 5.10: Normalized volume of the inductive components of the ABDB for $\lambda_{\text{th}} = 1.5$, $R_R = 2$, and $\lambda = \lambda_{L_f} = \lambda_{L_a}$.

where K_{vol} is again assumed the same for all inductors.

Figure 5.11 shows the relative volume increase of the inductive components of the ABDB with respect to a conventional parallel-connected converter, again for $\lambda_{\text{th}} = 1.5$ and $R_R = 2$. The normalized inductor volume as function of both ripple ratios for $\hat{m}_{\text{bias}} = 0.01 U_{\text{DC}}$ is depicted in Figure 5.11a. The black line indicates the value of λ_{L_a} that minimizes the inductor volume.

Figure 5.11b shows the normalized volume as function of λ_{L_f} for different $\hat{m}_{\text{bias}}$, with the value of λ_{L_a} that minimizes the volume. The crosses indicate the minima; also the corresponding λ_{L_a} is given. From Figure 5.11b it can be seen that the expected volume increase of the inductive components is in the range of 1.5 to 2.5, which is comparable to the results obtained in Section 5.3, where the inductor volume of the DB is compared to the conventional HB. Therefore, the total inductor volume of two parallel-connected DB legs and the ABDB is comparable for practical bias voltage values. The peak current in the main switches of the ABDB (S_1 & S_2) is approximately two times higher than for two parallel-connected DB legs, which in turn leads to increased losses in the semiconductor switches. However, the ABDB separates the bias current from the main output current, which in some designs might allow less-strict linearity demands for the auxiliary inductors, in turn leading to a further reduction of total inductor volume.

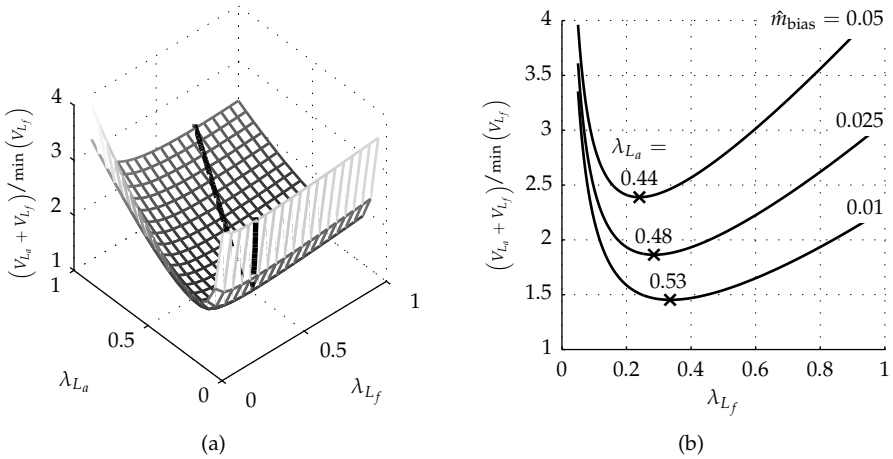


Figure 5.11: Relative volume increase of the inductive components of the ABDB for $\lambda_{\text{th}} = 1.5$ and $R_R = 2$, as function of (a) λ_{L_a} and λ_{L_f} with $\hat{m}_{\text{bias}} = 0.01$, and (b) λ_{L_f} for different $\hat{m}_{\text{bias}}$ and the λ_{L_a} that minimizes the volume, which is also indicated in black in (a).

5.4.2 Results

A prototype ABDB was built for testing purposes. The same control and power-electronics hardware as in the DB setup was used. Details about the experimental setup are described in Appendix A.4.

The air-cored filter inductors of the DB setup described in Appendix A.5 were reused, doubling the maximum output current rating of the setup. The optimal ripple ratio for L_a was determined from (5.40), resulting in $\lambda_{La_{\text{opt}}} = 0.22$. However, with no significant volume increase the ripple ratio $\lambda_{La_{\text{opt}}}$ can be decreased to 0.1. To be able to determine L_a, the maximum expected bias voltage should be specified. When assuming steady-state, $\hat{m}_{\text{bias}}$ can be approximated by

$$\hat{m}_{\text{bias}_x} \approx \frac{1}{U_{\text{DC}}} \max\left(\langle \hat{u}_{\text{bias}_x} \rangle\right) \approx \frac{1}{U_{\text{DC}}} \left(V_f + V_{\text{on}} + (R_f + R_{\text{on}} + R_{L_a}) i_{L_{a_x}}\right). \quad (5.41)$$

Equation (5.41) requires R_{L_a} as parameter, which in turn depends on L_a. Therefore, an iterative approach is required to determine L_a. After a few iterations, L_a is chosen to be 42 µH with $\hat{m}_{\text{bias}} = 0.04$. Figure 5.12 depicts a picture of both L_f and L_a. The air-cored filter inductors (L_f) were not optimized for volume, being chosen for linearity. However, from (5.37) and (5.38) it can be determined that the expected volume ratio for L_a with respect to L_f is 0.38, when taking the dif-

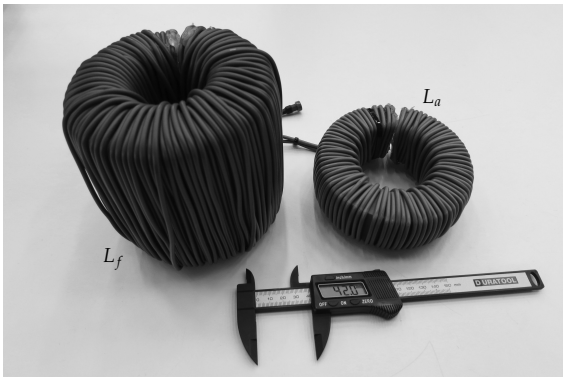


Figure 5.12: Close-up picture of the realized inductors L_a and L_f.

ferent values of $\hat{B}$ of both inductors into account. The measured volume ratio is 0.34, which is 11 % smaller than calculated. The difference can be attributed to the unequal K_{vol}.

The proposed modulation strategy was implemented on the dSPACE platform and simulations and measurements were done to verify the proposed modulation strategy in combination with the constructed inductors. Figures 5.13 and 5.14 depict the simulated and measured waveforms of the ABDB, using the inductors shown in Figure 5.12, with $U_{\text{DC}} = 100\,\text{V}$, 10 kHz switching frequency, and 10 A output current.

The measured waveforms in Figure 5.14 are formatted the same as in Figure 4.13a. In that figure the auxiliary inductors (L_a) and filter inductors (L_f) have the same values. After optimization L_a became approximately 19 times smaller, resulting in a larger current ripple on i_{L_a}, which is visible in Figure 5.13 and Figure 5.14. From the measurements it can be seen that in the waveforms of u_a and i_{L_a} slightly higher resistive losses occur. Furthermore spikes are present on the measured voltages which are induced by the switching transients. Otherwise, the measurements are in good agreement with the simulation results depicted in Figure 5.13.

5.5 Summary

This chapter shows that the inductor volume of the DB can be reduced significantly by using coupled inductors and non-interleaved u_{sn}. It is also shown that the smallest volume can be obtained using tightly negative-coupled inductors, as proposed in [16]. The volume of the inductive components of the DB is larger than

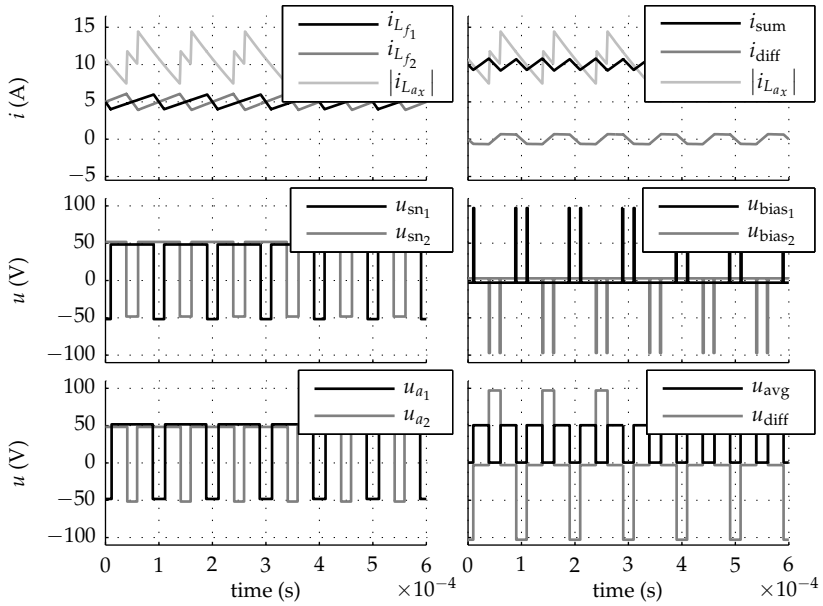


Figure 5.13: Simulated voltage and current waveforms for the ABDB.

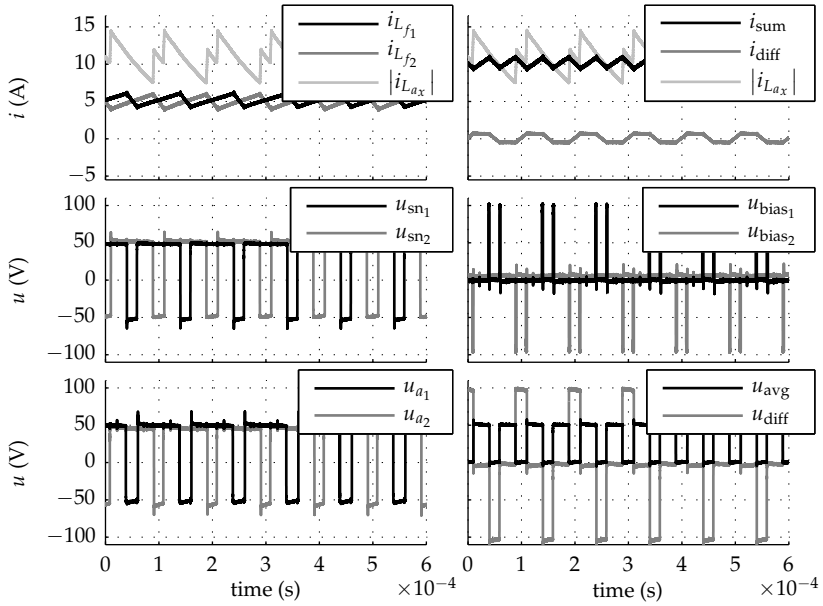


Figure 5.14: Measured voltage and current waveforms for the ABDB.

that of its conventional equivalent HB.

Analysis of the volumetric impact of the magnetic components of the ABDB shows that a similar total volume can be obtained as with two parallel-connected DBs. A volume increase of approximately 1.5 must be expected when applying the DB or ABDB topology instead of a conventional HB. Later in Chapter 7 the harmonic signature of both the DB and ABDB will be compared, also showing that similar results can be achieved with both topologies. Furthermore, when minimizing inductor volume one should take into account the effects on the currents. Reduced inductor volume might lead to increased (RMS) currents and consequently more losses in the semiconductor switches and other passive components in the converter.

In this chapter inductor volumes are determined using the area-product method with the assumption that core geometric constants are equal. In practice, different core shapes might be used. Furthermore, the area products presented in this chapter do not include magnetic core losses and many assumptions were made to express the peak and RMS currents in terms of switching ripple ratios and maximum output current. The results obtained in this chapter are, therefore, mostly indicative. They can be used as a starting point for a design that can be optimized further through iteration, if desirable.

Chapter 6

Trade-off between output quality and losses

"Things are not always as they seem."

(Phaedrus)

Abstract — The blanking time required to prevent short circuit when switching is a significant source of distortion in conventional switching legs. The DB does not suffer from blanking-time-related distortion, however, blanking time is not the only source of switching-leg-induced distortion. This chapter focuses on the effects of semiconductor device parameters on the output quality of the DB. It is shown that, ideally, the forward voltages of the diodes and switches have no effect on the output quality. Furthermore, the relation between the bias current and the amount of distortion introduced by the DB is investigated.

Contributions of this chapter are published in:

– J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Harmonics in opposed current converters," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 439–445.

6.1 Introduction

The DB does not require blanking time and, therefore, does not suffer from zero-crossing distortion due to blanking time. However, other sources, like non-ideal switches, diodes and inductors, contribute to harmonic distortion as well. In conventional converters these effects are, in practice, often neglected, since their contribution is relatively small compared to the effect of the device parameters, or simply because accuracy is not an issue. In [27] and more extensively in [28] different sources of distortion in switching amplifiers are treated. These studies focus on the effects of BJT switches. However, many of the ideas can be applied to other types of semiconductor switches too. Later in [74, chapter 4] a detailed analysis of distortion introduced by power MOSFETs in class-D audio amplifiers is made. All mentioned studies concentrate on the conventional HB switching leg, and do not apply to the DB.

In this chapter the effects of forward voltage and series resistance of the semiconductor diodes and switches, and the series resistances of the filter components on the output quality of a DB are investigated. The importance of the various parameters is determined by a local sensitivity analysis. Finally the theory is verified with simulation results, which also include the effects of switching transients. Other sources of distortion, such as inductor saturation, nonlinear behavior of semiconductors, nonlinear node capacitance, and temperature are not treated in this thesis.

6.2 Impact of conduction losses on the output quality

In this section the effects of the forward voltages and series resistances of the diodes and switches (V_f, V_{on}, R_f, R_{on}), and the series resistance (R_{L_f}, R_{C_f}) of the filter components (L_f, C_f) , are investigated based on the model presented in Figure 6.1.

Since current can flow only in one direction through the switch in each of the split legs, no antiparallel diodes are required. This means that the model depicted in Figure 6.1 can be applied to investigate the effects of the voltage drops across the components for both unipolar current switches, such as IGBTs, and bipolar-current switches, such as MOSFETs.

The dual-buck leg does not require blanking time and even allows overlapping gating signals, as was already pointed out in Chapter 4. This leads to additional interleaving flexibility compared to the conventional HB, which requires blanking

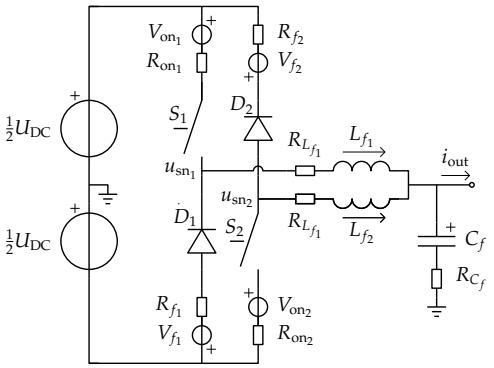


Figure 6.1: DB switching leg with parasitic components.

time and, therefore, does not allow overlapping gating signals. Figure 6.2 depicts slightly exaggerated switching waveforms of the DB with both non-interleaved and interleaved currents. The visible difference in pulse width between u_{sn_1} and u_{sn_2} is due to the bias voltage, which is required to compensate for the losses in the switches, diodes, and filter inductors. Figure 6.2 also illustrates the deviation of the switch-node voltages from a perfect square wave due to the voltage drop across the semiconductors.

6.2.1 Periodically averaged model

The state-space averaging method from Chapter 2 is used to derive an average model that describes the impact of the component parameters shown in Figure 6.1. The following piecewise-linear state-space model is used to describe the behavior of the DB

$$\dot{\mathbf{x}} = \mathbf{A}_k \mathbf{x} + \mathbf{b}_k \tag{6.1}$$

where the subscript $k \in K$ indicates the switching state of the converter. When assuming CCM, four switching states can be identified, resulting in the set $K = \{1, 2, 3, 4\}$, which is detailed in Table 6.1. The output current i_{out} is modeled as a disturbance input and the state vector is chosen as

$$\mathbf{x} = \begin{pmatrix} i_{L_{f_1}} & i_{L_{f_2}} & u_{C_f} \end{pmatrix}^\mathsf{T}. \tag{6.2}$$

The averages of the state matrix and input vector are obtained from

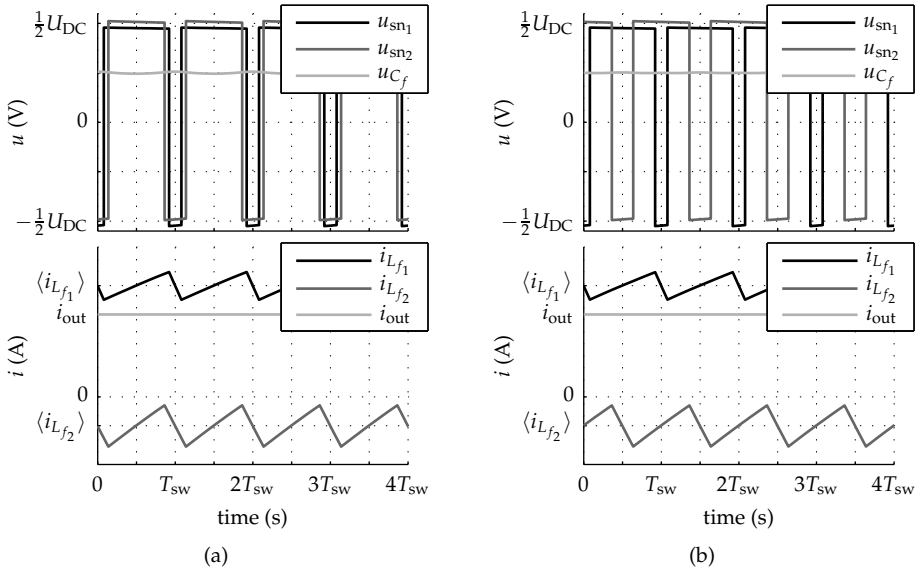


Figure 6.2: Detailed DB switching waveforms, for (a) non-interleaved switching, and (b) interleaved switching.

$$\langle \mathbf{A} \rangle = \frac{1}{T_{sw}} \sum_{k=K} \mathbf{A}_k T_k \tag{6.3}$$

and

$$\langle \mathbf{b} \rangle = \frac{1}{T_{sw}} \sum_{k=K} \mathbf{b}_k T_k \tag{6.4}$$

where T_k represents the time that the corresponding switching state is active. The state matrix and input vector can be split into a matrix that is dependent and a matrix that is not dependent on the switching state k as

$$\langle \mathbf{A} \rangle = \mathbf{A}'' + \frac{1}{T_{sw}} \sum_{k=K} \mathbf{A}'_k T_k \tag{6.5}$$

and

$$\langle \mathbf{b} \rangle = \mathbf{b}'' + \frac{1}{T_{sw}} \sum_{k=K} \mathbf{b}'_k T_k. \tag{6.6}$$

For the chosen state vector $\mathbf{A}''$ and $\mathbf{b}''$ equal

$$\mathbf{A}'' = \begin{pmatrix} -\frac{R_{L_{f_1}}+R_{C_f}}{L_{f_1}} & -\frac{R_{C_f}}{L_{f_1}} & -\frac{1}{L_{f_1}} \\ -\frac{R_{C_f}}{L_{f_2}} & -\frac{R_{L_{f_2}}+R_{C_f}}{L_{f_2}} & -\frac{1}{L_{f_1}} \\ \frac{1}{C_f} & \frac{1}{C_f} & 0 \end{pmatrix} \tag{6.7}$$

and

$$\mathbf{b}'' = \begin{pmatrix} \frac{R_{C_f}}{L_{f_1}} & \frac{R_{C_f}}{L_{f_2}} & -\frac{1}{C_f} \end{pmatrix}^{\mathsf{T}} i_{\text{out}}. \tag{6.8}$$

The matrices and vectors that depend on the switching state are in turn given by

$$\mathbf{A}'_1 = \text{diag}\left(-\frac{R_{f_1}}{L_{f_1}}, -\frac{R_{\text{on}_2}}{L_{f_2}}, 0 \right) \tag{6.9}$$

$$\mathbf{A}'_2 = \text{diag}\left(-\frac{R_{f_1}}{L_{f_1}}, -\frac{R_{f_2}}{L_{f_2}}, 0 \right) \tag{6.10}$$

$$\mathbf{A}'_3 = \text{diag}\left(-\frac{R_{\text{on}_1}}{L_{f_1}}, -\frac{R_{\text{on}_2}}{L_{f_2}}, 0 \right) \tag{6.11}$$

$$\mathbf{A}'_4 = \text{diag}\left(-\frac{R_{\text{on}_1}}{L_{f_1}}, -\frac{R_{f_2}}{L_{f_2}}, 0 \right) \tag{6.12}$$

and

$$\mathbf{b}'_1 = \begin{pmatrix} \frac{-\frac{1}{2}U_{\text{DC}}-V_{f_1}}{L_{f_1}} & \frac{-\frac{1}{2}U_{\text{DC}}+V_{\text{on}_2}}{L_{f_2}} & 0 \end{pmatrix}^{\mathsf{T}} \tag{6.13}$$

$$\mathbf{b}'_2 = \begin{pmatrix} \frac{-\frac{1}{2}U_{\text{DC}}-V_{f_1}}{L_{f_1}} & \frac{\frac{1}{2}U_{\text{DC}}+V_{f_2}}{L_{f_2}} & 0 \end{pmatrix}^{\mathsf{T}} \tag{6.14}$$

$$\mathbf{b}'_3 = \begin{pmatrix} \frac{\frac{1}{2}U_{\text{DC}}-V_{\text{on}_1}}{L_{f_1}} & \frac{-\frac{1}{2}U_{\text{DC}}+V_{\text{on}_2}}{L_{f_2}} & 0 \end{pmatrix}^{\mathsf{T}} \tag{6.15}$$

$$\mathbf{b}'_4 = \begin{pmatrix} \frac{\frac{1}{2}U_{\text{DC}}-V_{\text{on}_1}}{L_{f_1}} & \frac{\frac{1}{2}U_{\text{DC}}+V_{f_2}}{L_{f_2}} & 0 \end{pmatrix}^{\mathsf{T}} \tag{6.16}$$

in which 'diag' represents a diagonal matrix starting from the top left. The elements of the matrices and vectors correspond to the component values found in Figure 6.1.

The times that the switching states are active can be expressed in terms of the

Table 6.1: Switching states of the DB.

k	T_x	Conducting
1	T_1	D_1 & S_2
2	T_2	D_1 & D_2
3	T_3	S_1 & S_2
4	T_4	S_1 & D_2

duty ratios or the modulation indices of the corresponding switching legs using the following system of equations

$$\delta_1 T_{\text{sw}} = \tfrac{1}{2}\left(1 + m_1\right) T_{\text{sw}} = T_3 + T_4 \tag{6.17a}$$
$$\left(1 - \delta_1\right) T_{\text{sw}} = \tfrac{1}{2}\left(1 - m_1\right) T_{\text{sw}} = T_1 + T_2 \tag{6.17b}$$
$$\delta_2 T_{\text{sw}} = \tfrac{1}{2}\left(1 + m_2\right) T_{\text{sw}} = T_2 + T_4 \tag{6.17c}$$
$$\left(1 - \delta_2\right) T_{\text{sw}} = \tfrac{1}{2}\left(1 - m_2\right) T_{\text{sw}} = T_1 + T_3 \tag{6.17d}$$

where the duty ratios δ_x are the normalized times that the top switch or diode is conducting, and where m_x are the corresponding modulation indices.

Finally the results of (6.17) are used in (6.5) and (6.6) to obtain the following averaged state-space representation

$$\langle \dot{\mathbf{x}} \rangle \approx \langle \mathbf{A}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle + \langle \mathbf{b}(\mathbf{u}) \rangle. \tag{6.18}$$

When $\mathbf{u}$ is chosen to be

$$\mathbf{u} = \begin{pmatrix} m_1 & m_2 & i_{\text{out}} \end{pmatrix}^{\mathsf{T}} \tag{6.19}$$

the corresponding average state matrix is given by

$$\langle \mathbf{A}(\mathbf{u}) \rangle = \begin{pmatrix} -\frac{R_1'(m_1)}{L_{f_1}} & -\frac{R_{C_f}}{L_{f_1}} & -\frac{1}{L_{f_1}} \\ -\frac{R_{C_f}}{L_{f_2}} & -\frac{R_2'(m_2)}{L_{f_2}} & -\frac{1}{L_{f_2}} \\ \frac{1}{C_f} & \frac{1}{C_f} & 0 \end{pmatrix} \tag{6.20}$$

where

$$R_1'(m_1) = R_{L_{f_1}} + R_{C_f} + R_{\text{on}_1} + R_{\text{on}_1} - \left(R_{f_1} - R_{\text{on}_1}\right) m_1 \tag{6.21}$$

and

$$R_2'(m_2) = R_{L_{f_2}} + R_{C_f} + R_{\text{on}_2} + R_{\text{on}_2} + \left(R_{f_2} - R_{\text{on}_2}\right) m_2. \tag{6.22}$$

Finally, the averaged input vector becomes

$$\langle \mathbf{b}(\mathbf{u}) \rangle = \begin{pmatrix} \frac{-\frac{1}{2}\left(V_{f_1}+V_{\text{on}_1}\right)+\frac{1}{2}\left(U_{\text{DC}}+V_{f_1}-V_{\text{on}_1}\right)m_1-R_{C_f}i_{\text{out}}}{L_{f_1}} \\ \frac{\frac{1}{2}\left(V_{f_2}+V_{\text{on}_2}\right)+\frac{1}{2}\left(U_{\text{DC}}+V_{f_2}-V_{\text{on}_2}\right)m_2+R_{C_f}i_{\text{out}}}{L_{f_2}} \\ -\frac{i_{\text{out}}}{C_f} \end{pmatrix}. \tag{6.23}$$

As already pointed out in Chapter 2, it should be noted that the averaged result is an approximation. However, when $\langle \mathbf{A} \rangle$ is time-invariant, that is when it is not a function of $\mathbf{u}(t)$, the averaged model given in (6.18) exactly describes the moving-average behavior of the DB model depicted in Figure 6.1. For this case the state matrix becomes time-invariant when $R_{f_1} = R_{\text{on}_1}$ and $R_{f_2} = R_{\text{on}_2}$.

6.2.2 Steady-state solution

When assuming steady-state, I_{out} equals $\langle I_{L_{f_1}} \rangle + \langle I_{L_{f_2}} \rangle$, where the capitals represent steady-state values. After substituting I_{out} by $\langle I_{L_{f_1}} \rangle + \langle I_{L_{f_2}} \rangle$ in (6.23), the bottom row of the summation of $\langle \mathbf{A}(\mathbf{u}) \rangle \langle \mathbf{x} \rangle$ and $\langle \mathbf{b}(\mathbf{u}) \rangle$ in (6.18) becomes zero, and can therefore be removed. The remaining two steady-state equations can be expressed in terms of desired voltages by application of the transformations given in (4.13) and (4.10), and applying

$$M_{avg} = \frac{2}{U_{\text{DC}}} U^*_{\text{avg}} \tag{6.24}$$

$$M_{bias} = \frac{2}{U_{\text{DC}}} U^*_{\text{bias}}. \tag{6.25}$$

The two resulting expressions of the voltage references, for a given steady-state operating point, can be written in the form

$$U^*_{\text{avg}} = f\left(\mathbf{x}_o\right) \tag{6.26}$$

$$U^*_{\text{bias}} = g\left(\mathbf{x}_o\right) \tag{6.27}$$

where $\mathbf{x}_o$ is the average steady-state state-vector, which in turn is given by

$$\mathbf{x}_o = \begin{pmatrix} \langle I_{\text{sum}} \rangle & \langle I_{\text{bias}} \rangle & \langle U_{C_f} \rangle \end{pmatrix}^\mathsf{T}. \tag{6.28}$$

Equations (6.26) and (6.27) are straightforward to solve but the results are not insightful. For brevity they are not given in this thesis. However, when assuming equal forward voltages and on-resistances for the diodes and switches, that is when $V_f = V_{f_1} = V_{f_2}$, $R_f = R_{f_1} = R_{f_2}$, $V_{\text{on}} = V_{\text{on}_1} = V_{\text{on}_2}$, and $R_{\text{on}} = R_{\text{on}_1} = R_{\text{on}_2}$, (6.26) and (6.27) respectively become

$$U^*_{\text{avg}} = \tfrac{1}{2} U_{\text{DC}} \frac{k\langle I_{L_{f_1}} \rangle + l\langle I_{L_{f_2}} \rangle - a(R_{L_{f_1}} - R_{L_{f_2}})\langle I_{L_{f_1}} \rangle \langle I_{L_{f_2}} \rangle + c2\langle U_{C_f} \rangle}{\left(c + a\langle I_{L_{f_1}} \rangle\right)\left(c - a\langle I_{L_{f_2}} \rangle\right)} \tag{6.29}$$

and

$$U^*_{\text{bias}} = \quad U_{\text{DC}} \frac{m\langle I_{L_{f_1}} \rangle - n\langle I_{L_{f_2}} \rangle - a(R_{L_{f_1}} + R_{L_{f_2}} + R_f + R_{\text{on}})\langle I_{L_{f_1}} \rangle \langle I_{L_{f_2}} \rangle + d}{\left(c + a\langle I_{L_{f_1}} \rangle\right)\left(c - a\langle I_{L_{f_2}} \rangle\right)} \tag{6.30}$$

where

$$a = R_f - R_{\text{on}} \tag{6.31a}$$
$$b = \tfrac{1}{2}\left(R_f + R_{\text{on}}\right) \tag{6.31b}$$
$$c = U_{\text{DC}} + V_f - V_{\text{on}} \tag{6.31c}$$
$$d = (V_f + V_{\text{on}})U_{\text{DC}} + V_f^2 - V_{\text{on}}^2 \tag{6.31d}$$

and

$$k = bU_{\text{DC}} + a\langle U_{C_f} \rangle + cR_{L_{f_1}} + R_{\text{on}}V_f - R_f V_{\text{on}} \tag{6.31e}$$
$$l = bU_{\text{DC}} - a\langle U_{C_f} \rangle + cR_{L_{f_2}} + R_{\text{on}}V_f - R_f V_{\text{on}} \tag{6.31f}$$
$$m = bU_{\text{DC}} - a\langle U_{C_f} \rangle + cR_{L_{f_1}} + R_f V_f - R_{\text{on}}V_{\text{on}} \tag{6.31g}$$
$$n = bU_{\text{DC}} + a\langle U_{C_f} \rangle + cR_{L_{f_2}} + R_f V_f - R_{\text{on}}V_{\text{on}}. \tag{6.31h}$$

Notice that, due to the steady-state assumption, inductances L_{f_1} and L_{f_2}, capacitance C_f, and resistance R_{C_f} do not appear in (6.29) and (6.30), and that there is a nonlinear relation between reference voltage and operating-point.

However, when the resistances of the switches and diodes are made equal, that

is $R' = R_f = R_{\text{on}}$, (6.29) and (6.30) respectively simplify to

$$U^*_{\text{avg}} = \frac{U_{\text{DC}}}{U_{\text{DC}} + V_f - V_{\text{on}}} \left(\langle U_{C_f} \rangle + \left(\tfrac{1}{4}(R_{L_{f_1}} + R_{L_{f_2}}) + \tfrac{1}{2}R' \right) \langle I_{\text{sum}} \rangle + \ldots \right.$$
$$\left. \tfrac{1}{2} \left(R_{L_{f_1}} - R_{L_{f_2}} \right) \langle I_{\text{bias}} \rangle \right) \quad (6.32)$$

and

$$U^*_{\text{bias}} = \frac{U_{\text{DC}}}{U_{\text{DC}} + V_f - V_{\text{on}}} \left(V_f + V_{\text{on}} + \left(R_{L_{f_1}} + R_{L_{f_2}} + 2R' \right) \langle I_{\text{bias}} \rangle + \ldots \right.$$
$$\left. \tfrac{1}{2} \left(R_{L_{f_1}} - R_{L_{f_2}} \right) \langle I_{\text{sum}} \rangle \right) \quad (6.33)$$

where

$$\langle I_{\text{sum}} \rangle = \langle I_{L_{f_1}} \rangle + \langle I_{L_{f_2}} \rangle \quad (6.34)$$
$$\langle I_{\text{bias}} \rangle = \tfrac{1}{2} \left(\langle I_{L_{f_1}} \rangle - \langle I_{L_{f_2}} \rangle \right). \quad (6.35)$$

Both (6.32) and (6.33) are linear. Furthermore, it can be seen that the forward voltages of the semiconductor switches and diodes only lead to an additional static gain error and, therefore, do not result in harmonic distortion like in conventional switching legs, as was already pointed out in [27]. The forward voltage loss, however, needs to be compensated by the bias voltage reference (6.33) and, therefore, imposes a restriction of the maximum output voltage range of the DB switching leg, as pointed out in (4.15). There is, however, cross coupling between U^*_{avg} and $\langle I_{\text{bias}} \rangle$, and U^*_{bias} and $\langle I_{\text{sum}} \rangle$.

By choosing the series resistances of the inductors equal, that is $R_{L_f} = R_{L_{f_1}} = R_{L_{f_2}}$, the cross-coupling can be removed, as can be seen from

$$U^*_{\text{avg}} = \frac{U_{\text{DC}}}{U_{\text{DC}} + V_f - V_{\text{on}}} \left(\langle U_{C_f} \rangle + \tfrac{1}{2} \left(R_{L_f} + R' \right) \langle I_{\text{sum}} \rangle \right) \quad (6.36)$$

and

$$U^*_{\text{bias}} = \frac{U_{\text{DC}}}{U_{\text{DC}} + V_f - V_{\text{on}}} \left(V_f + V_{\text{on}} + 2 \left(R_{L_f} + R' \right) \langle I_{\text{bias}} \rangle \right) \quad (6.37)$$

respectively, which are both linear and have no cross coupling between the bias current and U^*_{avg}, and between output current and U^*_{bias}. Again, the forward voltage drops of the switches and diodes only lead to an additional static gain error.

In practice the series resistances of the switches and diodes are not equal. This can be compensated by matching the resistances of the switches and diodes. Adding an additional transistor, which is always on, in series with the diodes, and an extra diode in series with the transistors, results in a perfectly matched switching leg. However, both cost and losses will increase. Furthermore, the temperature of the devices needs to be matched as close as possible, which is challenging in practice, due to the operating-point dependency of the semiconductor losses.

In practice the voltage drop of the diodes and switches depends nonlinearly on temperature and current. Also component variations have to be taken into account, as will be shown later in this chapter. Still, the results of this section can be used to calculate precise operating-point-dependent steady-state feed-forward references for the DB.

6.2.3 Sensitivity analysis

The bias voltage is only used to prevent DCM and is, therefore, less critical. However, it is useful to know the relative impact of component variation on the required reference voltage U^*_{avg}. Therefore, a local sensitivity analysis is performed on (6.26) to determine the impact of component variation. The normalized sensitivity to the relative variation of the components can be determined using

$$S_{c_{o_i}} = \frac{2}{U_{\text{DC}}} \left| \frac{\partial U^*_{\text{avg}}\left(\mathbf{x}_o, \mathbf{c}\right)}{\partial c_i} \right|_{\mathbf{c}_o} c_{o_i} \tag{6.38}$$

where $\mathbf{c}$ is a vector containing the parameters for which the sensitivities are determined, and where the vector $\mathbf{c}_o$ contains the nominal component values. Both c_i and c_{o_i} are the i^{th} element of $\mathbf{c}$ and $\mathbf{c}_o$ respectively. Furthermore, the relative variation of a component is $\Delta c_i / c_i$.

The component vector is chosen to be

$$\mathbf{c} = \begin{pmatrix} V_{\text{on}_1} & V_{\text{on}_2} & V_{f_1} & V_{f_2} & R_{\text{on}_1} & R_{\text{on}_2} & R_{f_1} & R_{f_2} & R_{L_{f_1}} & R_{L_{f_2}} \end{pmatrix} \tag{6.39}$$

and when assuming R_{on} and R_f equal the nominal values are given by

$$\mathbf{c}_o = \begin{pmatrix} V_{\text{on}} & V_{\text{on}} & V_f & V_f & R' & R' & R' & R' & R_{L_f} & R_{L_f} \end{pmatrix}. \tag{6.40}$$

For (6.39) and (6.40), the sensitivities become

$$S_{V_{\text{on}x}} = \frac{V_{\text{on}} \left| \langle U_{C_f} \rangle + \frac{1}{2} U_{\text{DC}} + V_f + |\langle I_{L_{fx}} \rangle| (R_{L_f} + R') \right|}{\left(U_{\text{DC}} + V_f - V_{\text{on}} \right)^2} \tag{6.41}$$

$$S_{V_{fx}} = \frac{V_f \left| \langle U_{C_f} \rangle - \frac{1}{2} U_{\text{DC}} + V_{\text{on}} + |\langle I_{L_{fx}} \rangle| (R_{L_f} + R') \right|}{\left(U_{\text{DC}} + V_f - V_{\text{on}} \right)^2} \tag{6.42}$$

$$S_{R_{\text{on}x}} = \frac{R' \left| \langle I_{L_{fx}} \rangle \right| \left| \langle U_{C_f} \rangle + \frac{1}{2} U_{\text{DC}} + V_f + |\langle I_{L_{fx}} \rangle| (R_{L_f} + R') \right|}{\left(U_{\text{DC}} + V_f - V_{\text{on}} \right)^2} \tag{6.43}$$

$$S_{R_{fx}} = \frac{R' \left| \langle I_{L_{fx}} \rangle \right| \left| \langle U_{C_f} \rangle - \frac{1}{2} U_{\text{DC}} + V_{\text{on}} + |\langle I_{L_{fx}} \rangle| (R_{L_f} + R') \right|}{\left(U_{\text{DC}} + V_f - V_{\text{on}} \right)^2} \tag{6.44}$$

$$S_{R_{L_{fx}}} = \frac{R_{L_f} \left| \langle I_{L_{fx}} \rangle \right|}{U_{\text{DC}} + V_f - V_{\text{on}}} \tag{6.45}$$

where $x = \{1, 2\}$ indicates the corresponding P-cell or N-cell of the DB.

The sensitivities are operating-point dependent and it can be seen that (6.41) through (6.44) depend on $\langle U_{C_f} \rangle$. When using the fact that $\langle U_{C_f} \rangle$ is always within $\pm \frac{1}{2} U_{\text{DC}}$, and assuming that U_{DC} is large compared to V_{on}, V_f, and the maximum voltages across R_{on} and R_f, the peak sensitivities can be approximated as

$$\hat{S}_{V_{\text{on}x}} \approx \frac{V_{\text{on}}}{U_{\text{DC}}} \tag{6.46}$$

$$\hat{S}_{V_{fx}} \approx \frac{V_f}{U_{\mathrm{DC}}} \tag{6.47}$$

$$\hat{S}_{R_{\mathrm{on}x}} = \hat{S}_{R_{fx}} \approx \frac{R' \left| \langle \hat{I}_{L_{fx}} \rangle \right|}{U_{\mathrm{DC}}} \tag{6.48}$$

$$\hat{S}_{R_{L_{fx}}} \approx \frac{R_{L_f} \left| \langle \hat{I}_{L_{fx}} \rangle \right|}{U_{\mathrm{DC}}}. \tag{6.49}$$

The maximum sensitivities can be used to determine the relative importance of the various parasitic components. The resulting relative errors can be determined by multiplying the sensitivities with the relative variation of the corresponding parameter. The maximum sensitivities, given in (6.46) to (6.49), are equal to the ratio between the resulting voltage drop of the corresponding parameter and the supply voltage, which is plausible.

It should be noted that higher sensitivities do not always lead to more harmonic distortion. In (6.32) it was already shown that when R_f and R_{on} are equal the steady-state average model becomes linear and, therefore, does not lead to harmonic distortion.

6.2.4 Resulting output voltage error

To illustrate the resulting output voltage error of a DB, (6.29) is evaluated using the parameters given in Table 6.2, where the parameters for the IGBT case correspond to the experimental setup detailed in Chapter 9.

Figure 6.3 depicts the normalized output voltage error of a DB switching leg, as function of m_{avg} and the normalized output current for modulated bias current. It can be seen that the normalized steady-state voltage error appears to be a plane and is, therefore, dominantly linear. From Figure 6.3 it can also be seen that the maximum expected steady-state voltage error for the prototype is approximately 10 % of the output voltage range. Of course, the voltage error can be compensated to a great extent by feed-forward and/or feed-back control. However, it remains interesting to determine the nonlinear part of the voltage error, since it will determine the open-loop harmonic performance of the experimental setup.

The remaining errors after subtraction of the linear parts of the steady-state voltage errors are depicted in Figures 6.4 to 6.7. The normalized steady-state nonlin-

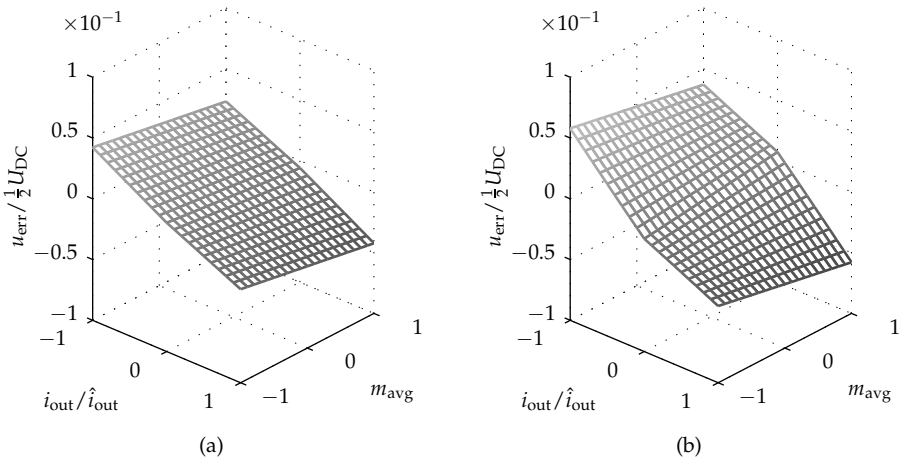


Figure 6.3: Normalized steady-state voltage error for a DB ($u_{\mathrm{err}} = u_{C_f} - u^*_{\mathrm{avg}}$) as function of m_{avg} and normalized output current, for (a) IGBT and (b) MOSFET switches. The results of (a) are based on the device parameters of the experimental setup. For (b) a MOSFET with the same voltage capability was scaled to match the current capability of the IGBT used in the experimental setup of Chapter 9. Both graphs are for modulated bias current, with $\lambda_{L_f} = 0.094$, $\lambda_{\mathrm{th}} = 1.5$, and $\hat{i}_{\mathrm{out}} = 40$ A.

earity errors ϵ_{err} for constant bias voltage are depicted in Figure 6.4 for the IGBT case, and in Figure 6.5 for the MOSFET case. In those figures (a) illustrates the error over the complete operating range. The black lines in (a) and (b) indicate the error as function of m_{avg}, for the case off maximum resistive loading.

It can be seen that, in the case of resistive loading, the nonlinear parts of the voltage errors are significantly smaller for constant bias current than for modulated bias current, which are depicted in Figure 6.6 for the IGBT case, and Figure 6.7 for the MOSFET case. Therefore, modulated bias will result in significantly more harmonic distortion than constant bias current.

For the IGBT case, modulated bias results in a nonlinear voltage error that is over 50 dB than for the constant bias case. For the MOSFET case this difference is 38 dB. Furthermore, for both constant and modulated bias the MOSFET case results in 27 and 14 dB higher nonlinear voltage error, respectively, compared to the IGBT case. This is due to the larger mismatch between R_{on} and R_f for the MOSFET cases.

Nonlinear voltage errors cause harmonic distortion. Therefore, constant bias current results in better THD. However, this comes at the cost of additional losses, as already explained in Section 4.2. For completeness it should again be noted that the nonlinear voltage error becomes zero for both constant and modulated bias

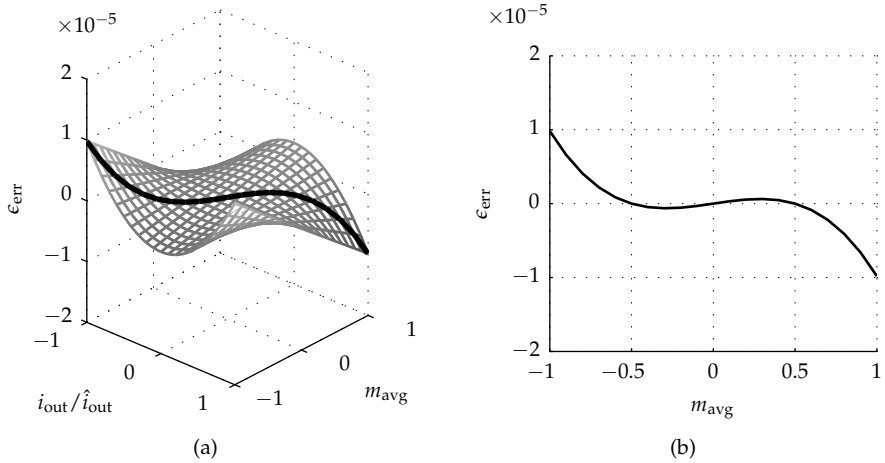


Figure 6.4: Nonlinear part of the normalized steady-state voltage error ϵ_{err} with constant bias current and IGBT switches, (a) as function of m_{avg} and normalized output current, and (b) as function of m_{avg}, assuming maximum resistive loading, as also indicated by the black line in (a). All parameters are the same as in Figure 6.3.

current in the case that $R_{\text{on}} = R_f$.

6.3 Impact of switching transients on the output signal quality

In the previous sections instantaneous switching transients are assumed. In this section it will be shown that the voltage commutation that occurs during switching is a significant source of distortion, and that a minimum current is required before a switch is allowed to be turned off. The switching transients are analyzed for IGBT switches, as depicted in Figure 6.8. However, since the currents through the switches have a fixed polarity, the model is also valid for bidirectional current switches, such as MOSFETs.

The diodes and IGBTs are modeled as depicted in Figure 6.9. When conducting both are approximated by a linear model containing a series-connected voltage source (V_f, V_{on}) and resistance (R_f, R_{on}), with parallel-connected parasitic capacitance (C_{AC}, C_{CE}), and wire resistance (R_w), respectively. Nonlinear effects, such as the voltage dependency of the parasitic capacitance, temperature effects, and exponential behavior are not included in this model. The emitter is split in a

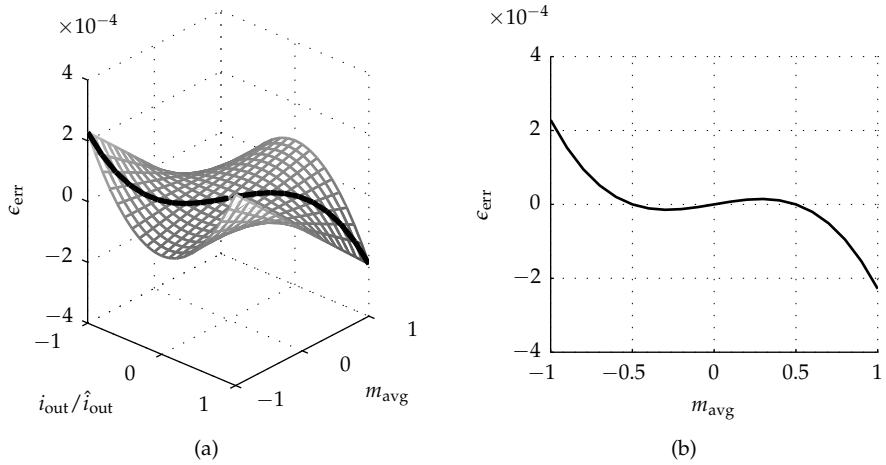


Figure 6.5: Nonlinear part of the normalized steady-state voltage error ϵ_{err} with constant bias current and MOSFET switches, (a) as function of m_{avg} and normalized output current, and (b) as function of m_{avg}, assuming maximum resistive loading, as also indicated by the black line in (a). All parameters are the same as in Figure 6.3.

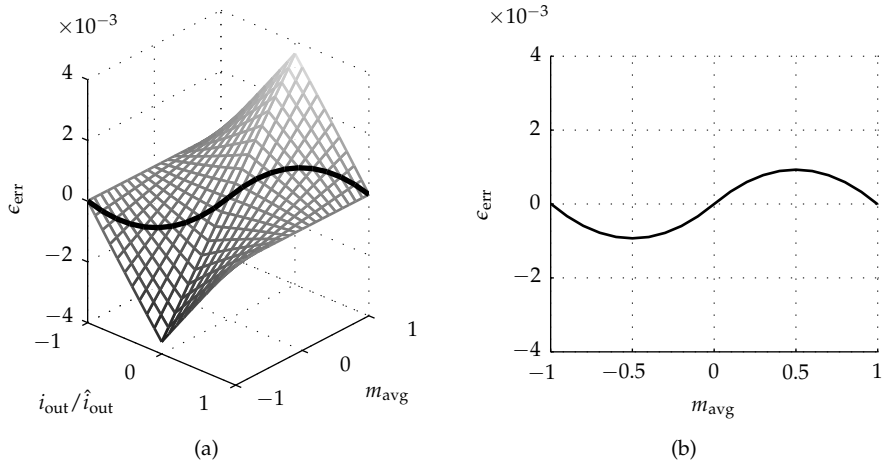


Figure 6.6: Nonlinear part of the normalized steady-state voltage error ϵ_{err} with modulated bias current and IGBT switches, (a) as function of m_{avg} and normalized output current, and (b) as function of m_{avg}, assuming maximum resistive loading, as also indicated by the black line in (a). All parameters are the same as in Figure 6.3.

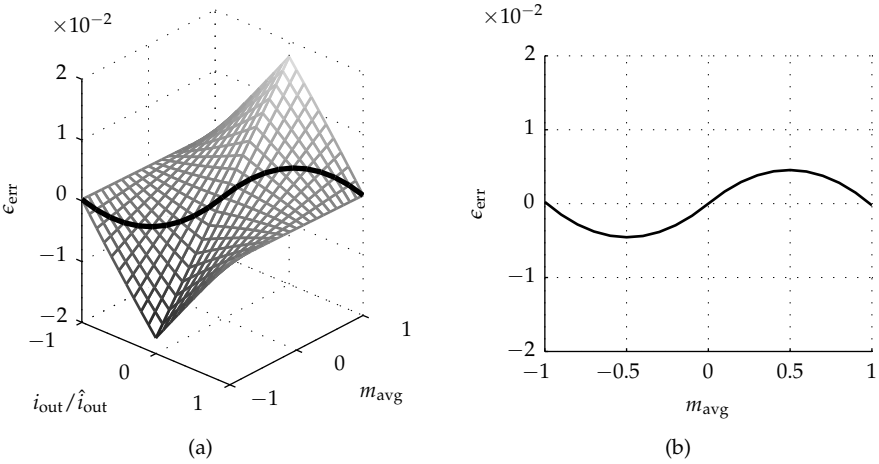


Figure 6.7: Nonlinear part of the normalized steady-state voltage error ϵ_{err} with modulated bias current and MOSFET switches, (a) as function of m_{avg} and normalized output current, and (b) as function of m_{avg} assuming maximum resistive loading, as also indicated by the black line in (a). All parameters are the same as in Figure 6.3.

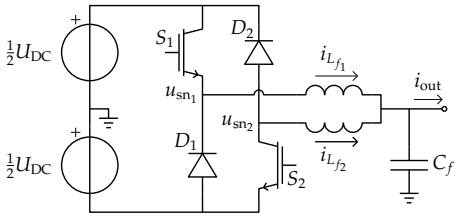


Figure 6.8: Schematic of the DB with IGBT switches.

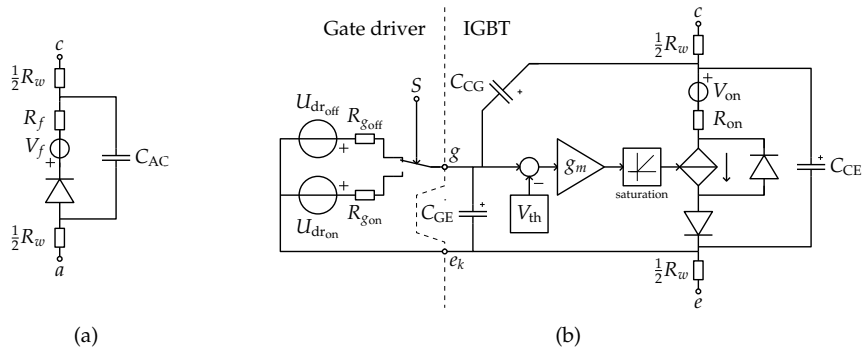


Figure 6.9: Models of the diode (a), and IGBT gate-driver combination (b) used for the analysis of switch-node voltage commutation.

power emitter (e), and a gating emitter (e_k). The gate emitter voltage u_{GE} is the voltage that appears across C_{GE}. The wire resistance is added to the model to prevent possible dependencies between states and sources when switching.

In the active region of the IGBT model, that is the region where the collector current i_C is limited by the gate emitter voltage u_{GE}, the IGBT is modeled as a linear voltage-controlled current source. The ideal diode in parallel with the controlled source is not conducting, and the current flowing through the switch is given by

$$i_{C_{\mathrm{sat}}} = g_m(u_{\mathrm{GE}} - V_{\mathrm{th}}) \tag{6.50}$$

where $i_{C_{\mathrm{sat}}}$ is the saturation-collector-current, g_m is the transconductance of the IGBT, and V_{th} is the device threshold voltage, as also depicted in Figure 6.10a.

The output characteristic of the IGBT model is depicted in Figure 6.10b. It can be seen that u_{CE} is not dependent on the gate voltage in the linear region, and that the transition from the linear to the active region is instantaneous. Both assumptions are of course approximations.

The IGBT model has an integrated gate driver model with different turn-on and turn-off voltage and resistance. When S is active the gate is connected to $U_{\mathrm{dr_{on}}}$ via resistance $R_{g_{\mathrm{on}}}$, otherwise the gate is connected to $U_{\mathrm{dr_{off}}}$ through $R_{g_{\mathrm{off}}}$. The turn-on and turn-off transients were simulated using the PLECS block-set for SIMULINK [1] and the resulting waveforms for the switching leg that supplies positive current are depicted in Figure 6.11.

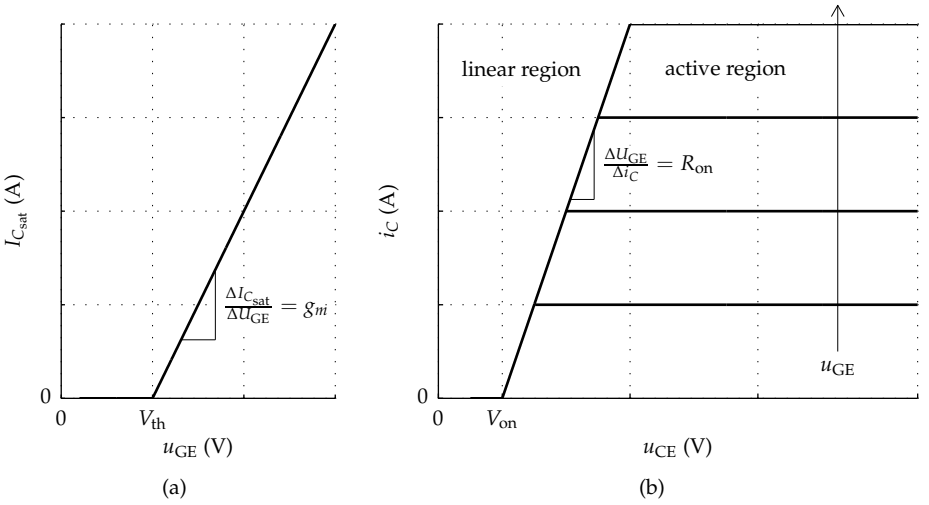


Figure 6.10: Characteristics of the IGBT model, (a) transfer characteristic, and (b) output characteristic.

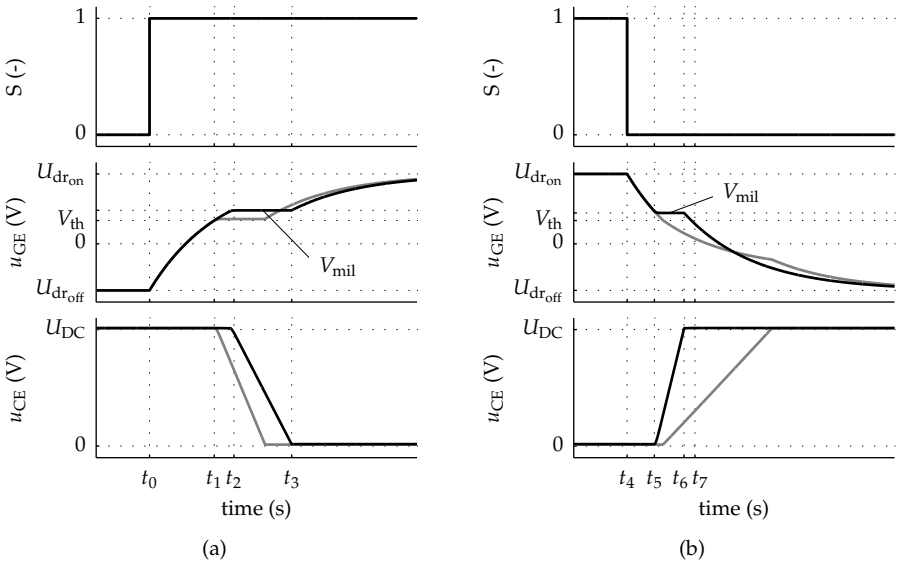


Figure 6.11: P-cell IGBT switching waveforms of the, (a) turn-on, and (b) turn-off transient, for both high (black) and low (gray) filter inductor current.

6.3.1 Turn-on transient

The turn-on event can be split in four intervals. These are indicated in Figure 6.11a for the black trace. At t_0 the gating signal S becomes active, u_{GE} equals $U_{\mathrm{dr_{off}}}$, and C_{GE} and C_{CG} start to be charged and discharged respectively by the current flowing through $R_{g_{\mathrm{on}}}$. When the threshold voltage V_{th} is reached at t_1 the IGBT starts conducting, as given by (6.50). The switch-node voltage $u_{\mathrm{sn_1}}$ remains clamped to the negative rail until $i_{C_{\mathrm{sat}}} = i_{L_{f_1}}$, after that switch-node voltage commutation starts. At t_2 an equilibrium occurs between the current flowing through $R_{g_{\mathrm{on}}}$ and C_{CG}.

During this equilibrium C_{CG} continues to be discharged, and the slew rate is determined by $i_{C_{\mathrm{sat}}}$, which in turn depends on u_{GE}. The gate emitter voltage u_{GE}, in turn, depends on the current flowing through C_{CG}, which in turn is dependent on the slew rate of the switch-node voltage. This results in a feedback mechanism where the rate of commutation is determined by $R_{g_{\mathrm{on}}}$ and the so-called Miller voltage (V_{mil}) for turn-on, which in turn depends on the collector current during commutation. The slew rate of u_{CE} during the equilibrium is given by

$$\frac{\mathrm{d}u_{\mathrm{CE}}}{\mathrm{d}t} = \frac{V_{\mathrm{mil}} - U_{\mathrm{dr_{on}}}}{R_{g_{\mathrm{on}}} C_{\mathrm{CG}}}. \tag{6.51}$$

After the commutation, $t \geq t_3$, C_{GE} and C_{CG} continue to be charged and discharged respectively until u_{GE} reaches $U_{\mathrm{dr_{on}}}$. For $t \geq t_3$ the semiconductor switch is considered conducting and operates in its linear region, as indicated in Figure 6.10b. Now, the voltage across the switch is determined by V_{on} and R_{on}.

6.3.2 Turn-off transient

Similarly to the turn-on transient, also the turn-off transient can be split in four intervals, which are indicated for the black line in Figure 6.11b. At t_4 the gating signal S becomes zero, and C_{GE} and C_{CG} are discharged and charged respectively by the current flowing through $R_{g_{\mathrm{off}}}$. The switch-node voltage $u_{\mathrm{sn_1}}$ remains clamped to the positive rail until $i_{C_{\mathrm{sat}}} = i_{L_{f_1}}$. At t_5, due to the same feedback mechanism as for turn-on, an equilibrium occurs between the current flowing through $R_{g_{\mathrm{off}}}$ and the current flowing through C_{CG}, and the semiconductor switch goes into its active region, as indicated in Figure 6.10b.

During the equilibrium u_{GE} equals the so-called Miller voltage V_{mil} or Miller

plateau for turn-off, and the voltage slew rate of the commutation is given by

$$\frac{\mathrm{d}u_{\mathrm{CE}}}{\mathrm{d}t} = \frac{V_{\mathrm{mil}} - U_{\mathrm{dr_{off}}}}{R_{g_{\mathrm{off}}} C_{\mathrm{CG}}}. \tag{6.52}$$

At t_6 the switch-node voltage commutates to the diode, and C_{GE} and C_{CG} continue to discharge and charge respectively. However, at t_6 the semiconductor switch is still conducting part of the current. At t_7, u_{GE} reaches the threshold voltage and the semiconductor switch stops conducting.

6.3.3 Distortion due to switching transients

From (6.51) and (6.52) it can be seen that the turn-on and turn-off slew rate can be set by the gate turn-on and turn-off resistors. However, V_{mil} depends on the current that has to be switched, resulting in a nonlinear operating-point-dependent delay and slew rate of the switching transients. Moreover, since the inductor currents at turn-on ($i_{L_{f_1}}(t_2)$) and at turn-off ($i_{L_{f_1}}(t_5)$) are different in practice, differences occur between the turn-on and turn-off transients within one switching cycle. This is illustrated for high current (black) and low current (gray) in Figure 6.11.

The black line in Figure 6.11a represents high inductor current during turn-on, while the the gray line corresponds with low inductor current. The operating-point-dependent switching delay and commutation rate result in harmonic distortion of the output voltage of the DB. The Miller voltage becomes less dependent on the inductor current for higher g_m. Therefore, increasing g_m results in decreased harmonic distortion. Also current-controlled gate drivers, as proposed in [55] and [54], can be used to control the switching transients and consequently mitigate harmonic distortion.

Figure 6.11b depicts the turn-off transients for high and low inductor current in black and gray respectively. The gray line, however, shows no Miller plateau. This is because at turn-off the commutation rate was limited by the filter inductor current and the total switch-node capacitance, in this case the combination of C_{CE} and C_{AC}, instead of the driver. This soft-commutation occurs for low inductor current. To include soft commutation, equation (6.52) is extended to

$$\frac{\mathrm{d}u_{\mathrm{CE}}}{\mathrm{d}t} = \min\left(\frac{V_{\mathrm{mil}} - U_{\mathrm{dr_{off}}}}{R_{g_{\mathrm{off}}} C_{\mathrm{CG}}}, \frac{i_{L_{f_1}}(t_5)}{C_{\mathrm{CE}} + C_{\mathrm{AC}}}\right) \tag{6.53}$$

where the driver determines the rate of commutation when the right term inside

the brackets in (6.53) is higher than the left term. Since the driver has no influence on the turn-off transient when it is limited by the inductor current, it is not possible to reduce harmonic distortion by gate current control, or by simply choosing a switch with sufficient g_m.

In the conventional half-bridge with fixed frequency PWM it is not possible to prevent inductor-current-limited turn-off transients during the blanking-time periods. For the DB, however, the bias current can be chosen to guarantee gate-driver-limited turn-off transients. The minimum current required to guarantee driver-limited commutation might result in larger losses than when the bias current is chosen only to guarantee CCM. The minimum inductor current required to guarantee driver-limited rate of turn-off is found by combining (6.53) and (6.50) and equals

$$i_{L_{f_1}}(t_5) \geq \frac{\left(V_{\text{th}} - U_{\text{dr}_{\text{off}}}\right)\left(C_{\text{CE}} + C_{\text{AC}}\right)}{R_{g_{\text{off}}} C_{\text{CG}} - g_m^{-1}\left(C_{\text{CE}} + C_{\text{AC}}\right)}. \tag{6.54}$$

From (6.54) it can be seen that for large g_m the minimum turn-off current can be set by choosing $R_{g_{\text{off}}}$ sufficiently large, resulting in additional losses, or by selecting semiconductor switches and diodes that minimize the total switch-node capacitance $C_{\text{CE}} + C_{\text{AC}}$. Similar equations then the ones presented above can be deduced for the N-cell. These are however not included in this thesis.

6.4 Harmonic distortion

The averaged steady-state voltage error model introduced earlier in this chapter is verified using simulation results of the DB model depicted in Figure 6.1, with a resistive load. Also simulations were performed with the switch and diode models depicted in Figure 6.9.

The device parameters for the IGBT case are extrapolated from the graphs in the Semikron SKM75GB123D device datasheet, the device that is also used in the experimental setup. For the MOSFET case, parameters are taken from the IXYS IXFL32N120P, however, these were scaled to the same current rating as the IGBT used in the setup. The diode parameters for all three cases were also taken from the integrated diode of the Semikron SKM75GB123D device. However, for the matched case R_f was chosen equal to the IGBT's on resistance. The parameters used for simulation are summarized in Table 6.2 and Table 6.3.

Figure 6.12 depicts the simulated open-loop output voltage spectrum, for asym-

Table 6.2: Conduction-related parameters of switches, diodes and inductors (L_f) used in simulations.

	V_{on} (V)	R_{on} (mΩ)	V_f (V)	R_f (mΩ)	R_{L_f} (mΩ)
Matched	1.7	40	1.2	40	50
IGBT	1.7	40	1.2	22	50
MOSFET	0	109	1.2	22	50

Table 6.3: Commutation-related parameters of switches and diodes used in simulations, $R_{g_{\text{off}}}$ and $R_{g_{\text{on}}}$ are 10 and 20 Ω respectively.

	V_{th} (V)	g_m (Ω^{-1})	C_{ies} (nF)	C_{oes} (nF)	C_{res} (pF)	U_{dr} (V)
Matched	6.0	10	3.3	0.5	220	$-10\ldots15$
IGBT	6.0	10	3.3	0.5	220	$-10\ldots15$
MOSFET	6.5	10	66	3.4	241	$0\ldots12$

metrical regular-sampled PWM, as described in [38, chapter 3] and treated in more detail in the next chapter. The output voltage (u_{out}) that appears across the load resistance was modulated to $0.75\frac{1}{2}U_{\text{DC}}\sin(2\pi f_o t)$, with $f_o = f_{\text{sw}}/1000$. The resistive load was chosen such that the resulting current was also modulated to 75 % of $\hat{i}_{\text{out}}$. The switches and diodes were modeled as depicted in Figure 6.1. The top graphs are without parameter variation and the bottom graphs are the result of a Monte Carlo analysis with 10 % parameter variation. The spectra in dB are normalized to the amplitude of the voltage setpoint. Figure 6.12a depicts the constant-bias-current case and Figure 6.12b the modulated-bias case.

The top graphs show that the matched case does not suffer from harmonic distortion, as was predicted earlier in this chapter. For constant bias current all harmonics of the IGBT case are smaller than −110 dB. This agrees with Figure 6.4 from which it can be seen that the expected nonlinear voltage error is approximately −110 dB for 75 % excitation. From Figure 6.12a it can be seen that the third harmonic for the MOSFET case appears at approximately −90 dB, which is slightly lower than the −83 dB that can be read from Figure 6.5.

The harmonic distortion for modulated bias current is much higher, as was already predicted in Section 6.2.4. From Figure 6.6 and Figure 6.7 it can be seen that the maximum nonlinear steady-state voltage errors are −79 dB and −59 dB for the IGBT and MOSFET case respectively, which again is approximately 6 dB lower than the maximum error predicted for 75 % excitation in Figure 6.12b.

The slightly better simulation result can be explained by the fact that the absolute nonlinear voltage error is not a measure of the amplitude of the third harmonic. It is, however, a maximum bound. Furthermore, it should be noted that the analysis was made assuming steady-state, which is not the case for the simulation results.

The bottom graphs in Figure 6.12 depict the same cases as shown in the top graphs but with component variation. The results were generated using the Monte Carlo method, where for every simulation run the parameters were varied 10 % using an uniform distribution. Per case 1729 simulations were conducted and only the maximum values of the spectral components were saved. The component variation results in even harmonic components, which occur due to component asymmetry. The second harmonic in the matched case with 10 % parameter variation has a similar amplitude as for the IGBT case. Hence, when matching of components is required to achieve the desired output quality, component tolerance should be taken into account. However, it should be noted that the simulated open-loop output voltage quality is more than sufficient for most practical applications.

The simulation results for the switch and diode models with commutation are depicted in Figure 6.13. The switching transients add significant distortion, especially for the MOSFET case for which (6.54) is not satisfied. For the MOSFET case spectral components of approximately $-80\,\mathrm{dB}$ appear up to the 11^{th} harmonic. Even for the matched and IGBT case spectral components appear up to approximately $-100\,\mathrm{dB}$. For those cases (6.54) was satisfied. Even with the switching transients added to the model the open-loop results look promising. However, it should be noted that the model still is piecewise linear, and does not include the nonlinear behavior of the semiconductors and temperature effects.

When MOSFET switches are used, the conventional HB converters suffer less from mismatch between R_{on} and R_f [74, chapter 4]. However, the blanking time required, and the forward voltages present in the case that IGBTs are used [27], result in significantly more harmonic distortion than the DB: typically several percents of the DC supply voltage, as already detailed in Part I of this thesis.

6.5 Summary

In this chapter the effects of non-ideal components in the DB switching leg are investigated. It is shown that the output of the DB is not influenced by the forward voltages of the switching devices. The forward voltages only appear in the bias of the DB, which is not the case for the conventional HB. Furthermore it is shown

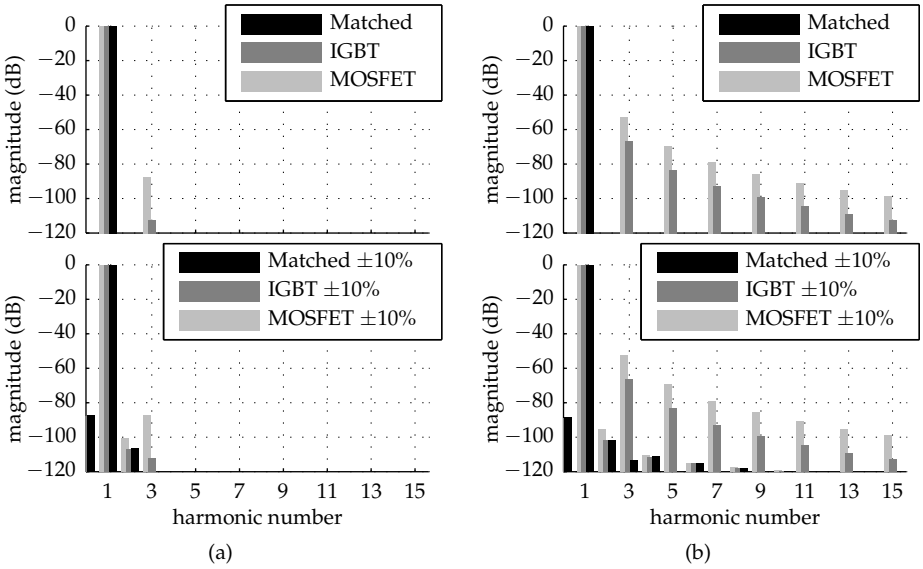


Figure 6.12: Simulated normalized output voltage spectrum of a DB switching leg, with ideal components and components with 10 % parameter variation. Subfigure (a) shows the result for constant bias and (b) illustrates modulated bias.

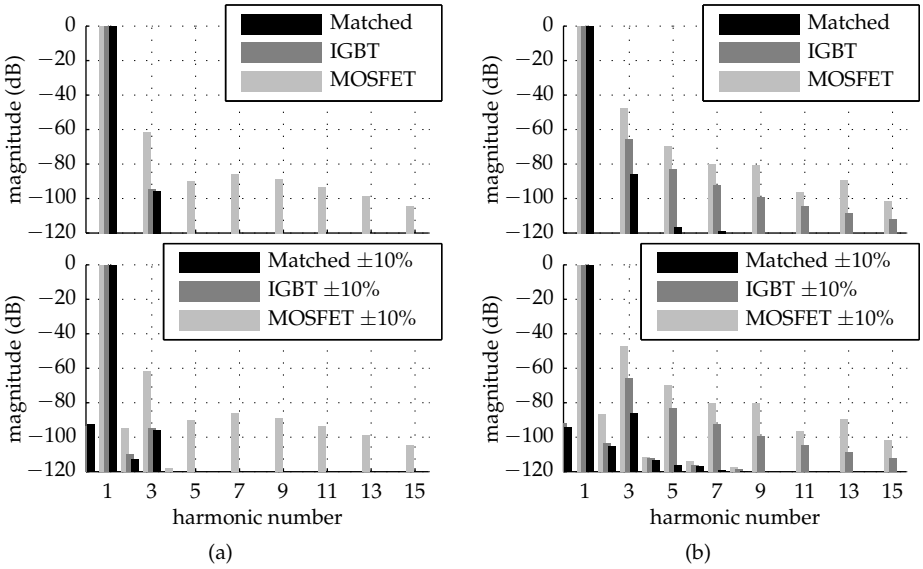


Figure 6.13: Simulated normalized output voltage spectrum of a DB switching leg using switch and diode models that include commutation, with ideal components and components with 10 % parameter variation. Subfigure (a) shows the result for constant bias and (b) illustrates modulated bias.

that the average behavior of the DB becomes linear when the resistances in the switches and diodes are made equal. Moreover, when the series resistances of the filter inductors are also equal there is no cross coupling between the bias and output of the DB. This enables decoupled control of bias and output current.

It is shown that modulated bias results in significantly more distortion than constant bias. However, in Chapter 2 it is pointed out that modulated bias results in a significant reduction of the losses.

A model that includes the switching transients is introduced. It is shown that a minimum turn-off current is required to ensure gate-driver-limited commutation of the switch-node voltage. Gate-driver-limited commutation is less operating-point dependent and, therefore, results in less harmonic distortion. The turn-off current required to guarantee driver limited commutation may require increased offset current i_{th}, and may therefore result in additional losses. There is thus a trade-off between output quality and losses of a DB.

The analytical results are verified with simulations. The simulation results support the analytical models deduced in this chapter.

Chapter 7

The impact of PWM generation and bias voltage

"Symmetry is what we see at a glance; based on the fact that there is no reason for any difference..."

(Blaise Pascal)

Abstract — Switching in switched-mode power amplifiers comes with a substantial amount of distortion and electromagnetic interference. Distortion is unwanted power that is transferred to the load and is due to a difference between the desired and the actually generated signals. Electromagnetic interference affects other electrical circuits and is a consequence of conducted or radiated emissions. This chapter focuses on the effects of the modulation strategy on the output voltage quality under open-loop conditions, including the effects of the bias voltage. It is shown that by selecting the appropriate interleaving strategy it is possible to achieve 3-level PWM with doubled output ripple frequency, which reduces distortion, together with a constant common-mode voltage at the output of the converter, which results in reduced electromagnetic interference.

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- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Harmonics in opposed current converters," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 439–445.

7.1 Introduction

Switching in SMPCs comes with a substantial amount of distortion and EMI. Distortion is the unwanted power that is transferred to the load. EMI affects electrical circuits outside and also inside the amplifier and is a consequence of conducted or radiated emissions. Signal degradation and even temporary malfunction or permanent failure of a device can occur as a result of EMI.

The amount of allowed distortion is in most cases specified by the user or manufacturer. Different norms exist for EMI, which are defined in so-called electromagnetic compatibility (EMC) standards. These standards are application related, e.g. industrial, medical, or consumer, and can also differ per country. In some application areas, even stricter rules may apply than encountered in any EMC standard. This can be the case for military or space equipment, and in some cases also for subsystems of high-precision equipment.

There are different ways to deal with output distortion and EMI due to switching in SMPCs. It is possible to apply different forms of filtering or, in the case of EMI, to use shielded cabling to the load. However, also the modulation strategy of the switching legs influences distortion and EMI. In [105] different PWM strategies for the DB are discussed. The analysis there, however, does not include the influence of the bias voltage that turns out to be an important source of additional distortion compared to an ideal DB.

This chapter focuses on the effects of the modulation strategy on the DB output voltage quality under open-loop conditions, including the impact of the bias voltage. Different modulation strategies for the full-bridge equivalent of both the conventional and auxiliary-bias DB are compared to each other and to the conventional FB converter, in order to determine the modulation strategies that are best suited for the compared topologies.

7.2 Integrated-bias dual-buck converter

7.2.1 Full-bridge-equivalent circuit

Switching converters with filtered output are often applied to drive voice-coil actuators in lithographic equipment, or gradient coils for MRI, and in high-precision equipment, where loss power restrictions preclude using linear amplifiers because of bounds on volume and cost. A FB has advantages over a single switching leg or HB because it does not suffer from power supply pumping, as explained

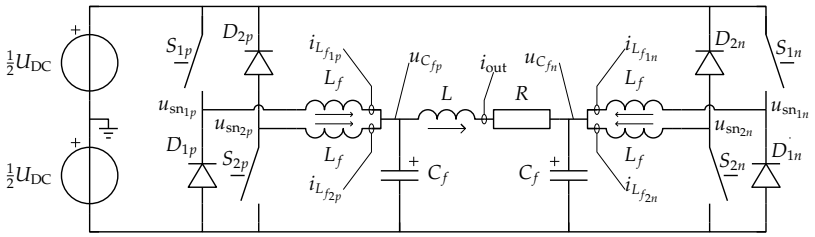


Figure 7.1: Schematic overview of full-bridge equivalent DB.

in [39] and in Section 3.3. For high power ratings the FB becomes even more attractive because for the same power level switches with half of the current rating can be used [67, chapter 8].

The FB can be used as a building block where the required power level determines the number of FBs that are put in series and/or in parallel. In Part I of this thesis it was shown that FBs suffer from output distortion due to the required blanking time. The DB, as introduced in Chapter 4, does not suffer from this distortion at the cost of one extra inductor per DB leg, and some additional losses.

Figure 7.1 depicts a DB with similar functionality as a FB, where p and n represent the positive side and negative side currents and voltages. All voltages are referenced to the mid-point of the symmetrical power supply. The voice coil or inductive load is represented by L and R, and is connected to the outputs of the positive- and negative-side filters. It should be noted that a symmetrical supply is not a requirement for the full-bridge equivalent of the DB. This particular supply configuration is used here to simplify the explanation.

There are many ways to filter the switch-node voltages in full-bridge and equivalent converters, however, in this chapter only the symmetrical second-order filter, as depicted in Figure 7.1, is treated. As will be explained later in this chapter, that filter leads to equal cut-off frequency and order for both the differential-mode (DM) and common-mode (CM) voltages. In some cases where stricter requirements are placed on the DM voltage an additional capacitor can be connected across the load. This results in a lower cut-off frequency for the switched DM voltage, as discussed in Appendix B.

7.2.2 PWM generation

Usually some sort of filter is included in SMPCs to suppress undesired frequency components due to switching. Since passive filters require bulky and costly com-

ponents, it is attractive to aim at higher switching frequencies to achieve smaller filter sizes.

Increasing the output ripple frequency of the converter results in better output voltage quality and relaxes the filter requirements. The output ripple frequency of a converter can be increased by e.g. series or parallel connection of multiple switching cells. In the case of a conventional FB converter it is possible to double the output ripple frequency by appropriately aligning the PWM waveforms of the positive and negative side switching legs with respect to each other. This is also known as unipolar switching or three-level PWM.

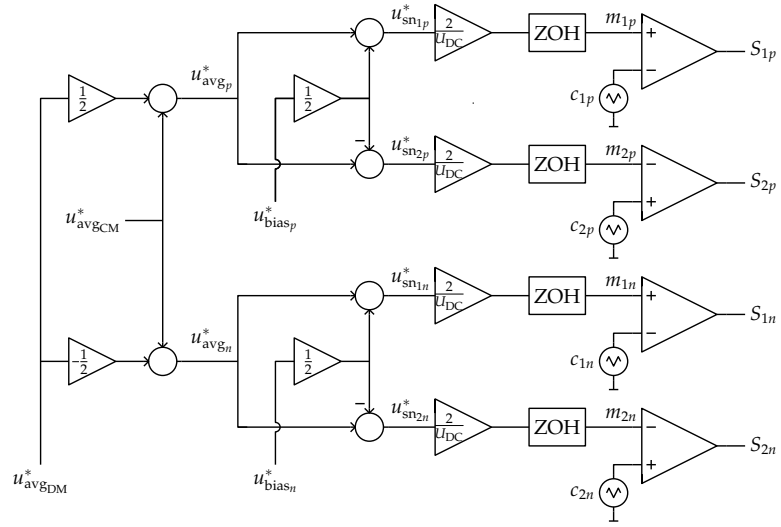
Generation of PWM commonly involves comparison of a carrier with a modulating signal m. Normally a sawtooth or triangular carrier is used that is generated with analog means in PWM or digitally in DPWM. The modulating signal can be sampled naturally, i.e. continuously, or regularly, i.e. with zero-order-hold (ZOH) dynamics. In case of regular-sampled triangular carrier modulation the modulating signal can be updated once, called symmetrical, or twice, asymmetrical, per carrier cycle time. Figure 7.2b depicts the waveforms for asymmetrical regular-sampled triangular-carrier PWM. A detailed overview of different available PWM modulation methods and their resulting output spectra can be found in [38].

With the arrival of low-cost digital signal processors (DSPs) with integrated DPWM modulators and FPGAs, digital control and regular-sampled DPWM made its way into SMPCs. Asymmetrical regular-sampled triangular-carrier PWM is the best regular-sampled PWM method available with respect to the total harmonic spectrum [38, page 150]. This method will therefore be used in this thesis.

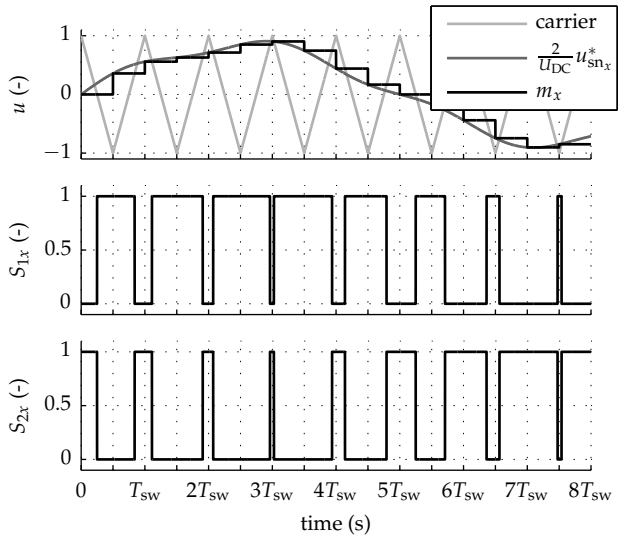
The full-bridge equivalent DB, as shown in Figure 7.1, consists of four legs that can be modulated individually. This results in increased interleaving flexibility compared to the conventional FB. In [105] it is shown that the output ripple frequency of an ideal full-bridge equivalent DB can be increased by a factor four. The analysis in [105], however, neglects the bias voltage that is required to prevent DCM and is necessary to ensure linear operation.

Figure 7.2a depicts the schematic overview of an asymmetrical regular-sampled PWM modulator, as explained in [38, chapter 3], based on the variable transformation given in (4.9), and using four independent triangular carrier generators. The desired or reference voltage values are marked with a superscript asterisk.

The corresponding waveforms are depicted in Figure 7.2b and illustrate the sampling moments of the zero-order holds, which align with the positive and negative extremes of the carrier signals. The carrier signals are triangularly shaped with unit amplitude, have equal frequency f_{sw}, and their phase shifts ϕ_c can be



(a)



(b)

Figure 7.2: Schematic overview of the PWM generation with coordinate transformation (a), and corresponding waveforms (b).

set arbitrarily. Without loss off generality $\phi_{c_{1p}}$ can be set to zero. From here on the carrier phases are denoted as $\phi_c = (0 \quad \phi_{c_{2p}} \quad \phi_{c_{1n}} \quad \phi_{c_{2n}})$. The gating signals S_x correspond to those of the switches in Figure 7.1.

Because of the four independently modulated switching legs, there are four degrees of freedom; the bias and average voltages of the positive and negative side, indicated by u_{bias_x} and u_{avg_x}, respectively.

It is convenient to reformulate u_{avg_x} in terms of a DM voltage that is applied across the load and a CM voltage that does not contribute to the output power as

$$u_{\text{avg}_{\text{DM}}} = u_{\text{avg}_p} - u_{\text{avg}_n} \tag{7.1a}$$

$$u_{\text{avg}_{\text{CM}}} = \tfrac{1}{2}\left(u_{\text{avg}_p} + u_{\text{avg}_n}\right). \tag{7.1b}$$

Consequently, the average voltage references of the p and n side are modulated as

$$u^*_{\text{avg}_p} = \quad \tfrac{1}{2}u^*_{\text{avg}_{\text{DM}}} + u^*_{\text{avg}_{\text{CM}}} \tag{7.2a}$$

$$u^*_{\text{avg}_n} = -\tfrac{1}{2}u^*_{\text{avg}_{\text{DM}}} + u^*_{\text{avg}_{\text{CM}}}. \tag{7.2b}$$

Since $u_{\text{avg}_{\text{CM}}}$ does not contribute to the power that is transferred to or from the load, in practice its reference is kept constant at 0 V to maximize the DM output voltage range.

The output voltage quality can be characterized by the differential mode ($u_{\text{sn}_{\text{DM}}}$) and common mode ($u_{\text{sn}_{\text{CM}}}$) switching voltage waveforms, given by

$$u_{\text{sn}_{\text{DM}}} = \tfrac{1}{2}\left(u_{\text{sn}_{1p}} + u_{\text{sn}_{2p}} - u_{\text{sn}_{1n}} - u_{\text{sn}_{2n}}\right) \tag{7.3a}$$

$$u_{\text{sn}_{\text{CM}}} = \tfrac{1}{4}\left(u_{\text{sn}_{1p}} + u_{\text{sn}_{2p}} + u_{\text{sn}_{1n}} + u_{\text{sn}_{2n}}\right). \tag{7.3b}$$

The switch-node voltages do not include the effect of the output filter and can therefore be used to describe the output voltage quality for any filter. The DM voltage $u_{\text{sn}_{\text{DM}}}$ is the unfiltered switching voltage that appears across the load. The CM voltage $u_{\text{sn}_{\text{CM}}}$ is the average of all the switching voltages and is a common source of EMI [41].

Five representative cases of interleaving are investigated for the DB, with

$$\phi_c = \frac{\pi}{2} \begin{cases} \begin{pmatrix} 0 & 0 & 2 & 2 \end{pmatrix}, & \textit{case 1} \\ \begin{pmatrix} 0 & 0 & 0 & 0 \end{pmatrix}, & \textit{case 2} \\ \begin{pmatrix} 0 & 2 & 0 & 2 \end{pmatrix}, & \textit{case 3} \\ \begin{pmatrix} 0 & 2 & 2 & 0 \end{pmatrix}, & \textit{case 4} \\ \begin{pmatrix} 0 & 2 & 1 & 3 \end{pmatrix}, & \textit{case 5}. \end{cases}$$

A comparison of these modulation methods is made for three distinct levels of u_{bias}, namely $u_{\text{bias}} = 0\,\text{V}$, $u_{\text{bias}} = 0.05U_{\text{DC}}$, and $u_{\text{bias}} = 0.2U_{\text{DC}}$. The output is modulated to $u^*_{\text{avg}_{\text{DM}}} = 0.75U_{\text{DC}} \sin(2\pi f_o t)$, with $f_o = f_{\text{sw}}/100$.

To take into account the effect of the DB output filter, a weighted total harmonic distortion (WTHD) and a weighted harmonic distortion (WHD) are defined as

$$\text{WTHD} = \sqrt{\sum_{n=2}^{\infty} \min\left(1, \frac{1}{n^2}\left(\frac{f_{\text{sw}}}{f_o}\right)^2\right)\left(\frac{U_{\text{sn}_{\text{DM}}}(nf_o)}{U_{\text{sn}_{\text{DM}}}(f_o)}\right)^2} \tag{7.4a}$$

$$\text{WHD} = \sqrt{\sum_{n=1}^{\infty} \min\left(1, \frac{1}{n^2}\left(\frac{f_{\text{sw}}}{f_o}\right)^2\right)\left(\frac{U_{\text{sn}_{\text{CM}}}(nf_o)}{\frac{1}{2}U_{\text{DC}}}\right)^2} \tag{7.4b}$$

where f_{sw}/f_o is the ratio between the switching frequency (f_{sw}) and the frequency of $u^*_{\text{avg}_{\text{DM}}}$, and $U_{\text{sn}_{\text{DM}}}$ and $U_{\text{sn}_{\text{CM}}}$ are the magnitude spectra of $u_{\text{sn}_{\text{DM}}}$ and $u_{\text{sn}_{\text{CM}}}$, respectively. The weighting accomplished by the minimum operators in (7.4) represents the LC output filter of the DB (L_f, C_f), as depicted in Figure 7.1, with its cut-off frequency equal to f_{sw}. When assuming no significant spectral components between f_o and f_{sw}, the cut-off frequency of the output filter (f_c) can be set in between f_o and f_{sw} by scaling the WTHD and WHD with $(f_c/f_{\text{sw}})^2$.

7.2.3 Simulation results

First, open-loop simulations are presented, where the bias voltage was realized by setting the saturation and forward voltages of the switches and diodes equal to $\frac{1}{2}u_{\text{bias}}$. Furthermore, all other components are assumed lossless. The PWM is implemented as depicted in Figure 7.2a with ideal triangular carrier waveforms. The DM and CM spectra are normalized to U_{DC} and $\frac{1}{2}U_{\text{DC}}$, respectively. The WTHD and WHD are determined from (7.4) with only the harmonics of f_o up to $10f_{\text{sw}}$.

When assuming ideal components, $u_{\text{bias}} = 0$ for the DB, and no blanking time for

the FB for *case 1* and *case 2*, the DB and conventional FB switching waveforms are identical. Figure 7.3 depicts the switching waveforms and corresponding spectra of both the DM and CM voltages for *case 1*. The modulation of *case 1* is also known in the literature as bipolar or two-level PWM. The simulation results of *case 2*, also known as unipolar or three-level PWM, are shown in Figure 7.3. The black traces indicate the ideal case when $u_{\text{bias}} = 0\,\text{V}$, the dark gray trace indicates $u_{\text{bias}} = 0.05U_{\text{DC}}$, and the light gray trace is related to $u_{\text{bias}} = 0.2U_{\text{DC}}$.

Figures 7.3 and 7.4 illustrate the trade-off between the voltage ripple amplitudes and spectral content of $u_{\text{sn}_{\text{CM}}}$ and $u_{\text{sn}_{\text{DM}}}$. Unipolar switching leads to doubling of the output ripple frequency and halving the DM voltage ripple amplitude. However, the spectral components that are removed from the DM voltage reappear in the CM voltage. Addition of the u_{bias} leads to a slightly lower WTHD and WHD for bipolar and unipolar switching.

The DB has more modulation flexibility compared to the conventional FB, resulting in *cases 3* to *5*. Figures 7.5 and 7.6 illustrate *case 3* and *case 4*, respectively. Both methods ideally have constant CM voltage, as with bipolar switching, and three-level DM and double output ripple frequency, as for unipolar switching. However, when bias voltage is required, additional spectral components occur. For *case 3* these spectral components appear in the DM voltage. Moreover, the fundamental switching frequency component reappears, which will limit the update frequency of a controller in a closed-loop configuration.

A closer look reveals that *case 4* features harmonic cancellation in the DM voltage when a bias voltage is present. Also in the presence of a bias voltage the common-mode WHD is significantly lower than *case 2*.

One would expect that the best results are achieved for *case 5*, because it leads to five-level PWM. This is true for the ideal case, as depicted by the black traces in Figure 7.7. However, the fundamental switching frequency reappears when the required bias voltage is included, as indicated with dark gray traces for $u_{\text{bias}} = 0.05U_{\text{DC}}$, and light gray traces for $u_{\text{bias}} = 0.2U_{\text{DC}}$. Depending on the amount of bias voltage, after filtering *case 5* might even result in more DM voltage ripple than *case 4*. Also, when closed-loop control is added, the appearance of the fundamental switching frequency might limit the update frequency of the controller. This method also suffers from a higher CM voltage ripple than the output voltage ripple, which in some applications might require additional CM filtering.

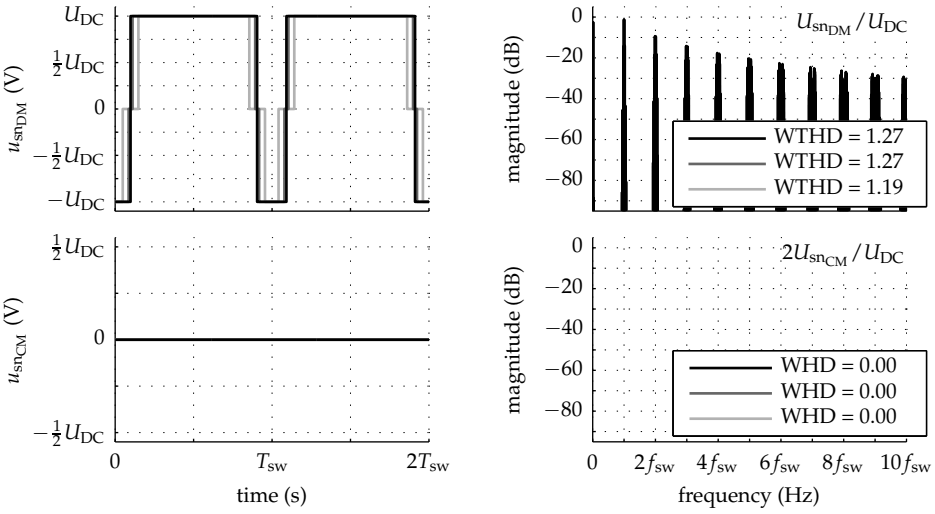


Figure 7.3: Simulation results for *case 1* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray). In (b), the cases illustrated in gray are not visible (behind the black case) but have approximately equal magnitude.

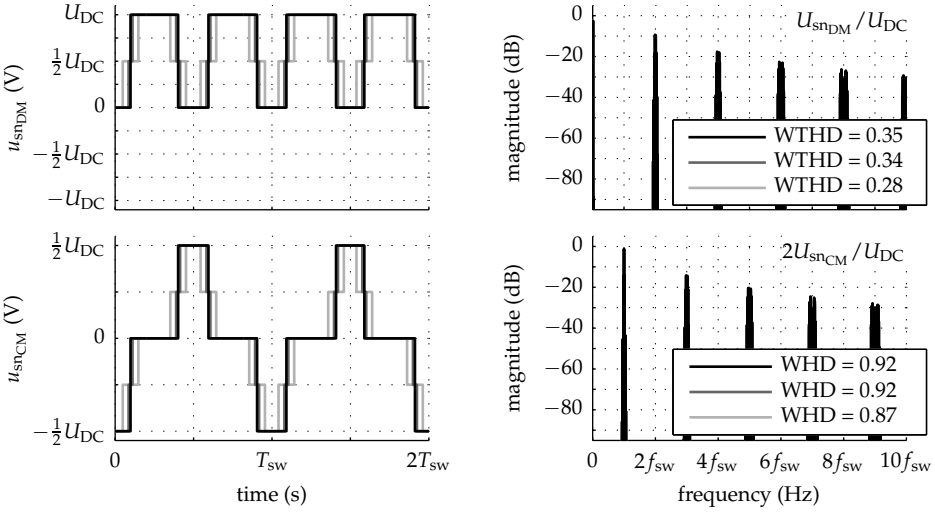


Figure 7.4: Simulation results for *case 2* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (light gray), and $u^*_{bias} = 0.2U_{DC}$ (gray). In (b), the cases illustrated in gray are not visible (behind the black case) but have approximately equal magnitude.

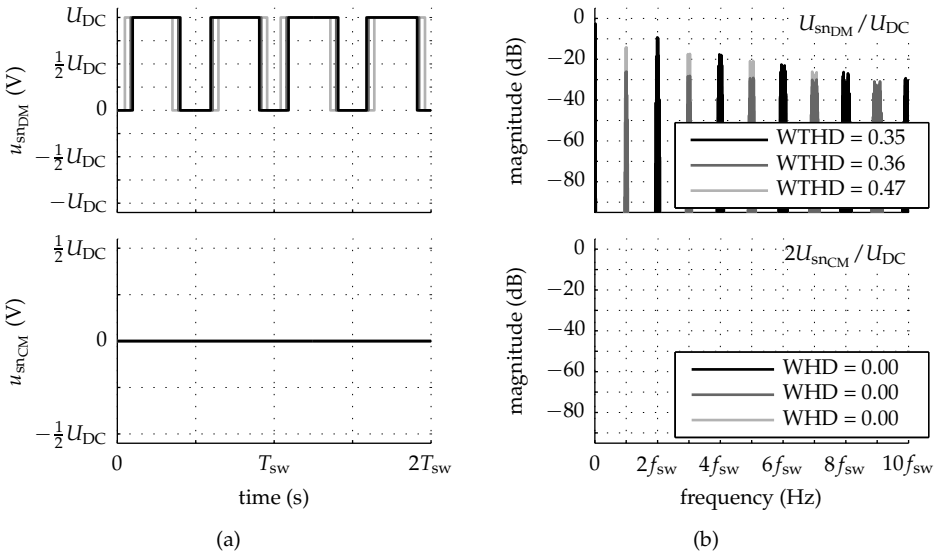


Figure 7.5: Simulation results for *case 3* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray).

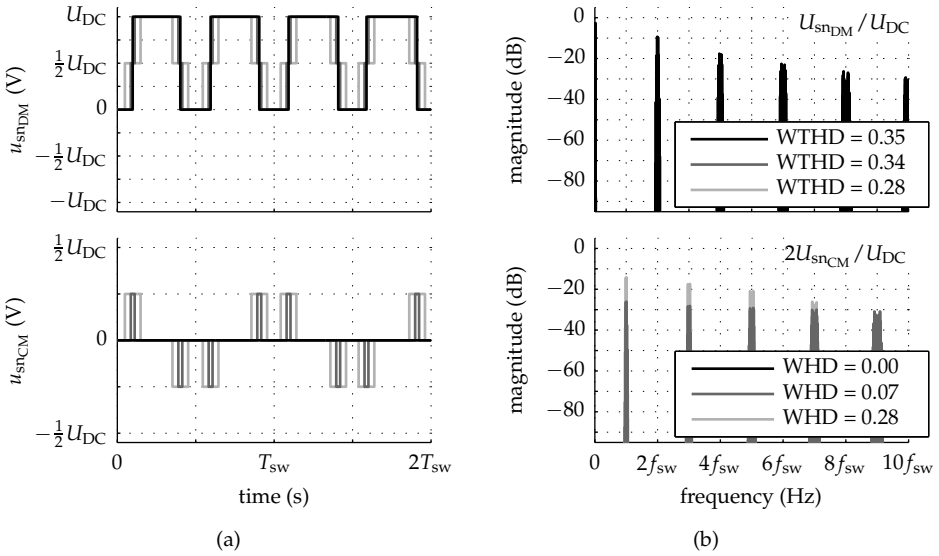


Figure 7.6: Simulation results for *case 4* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray).

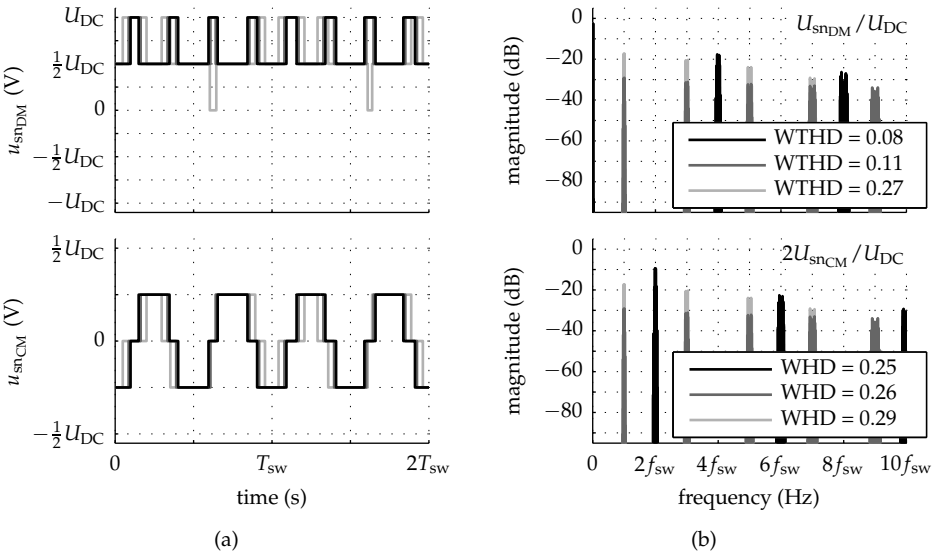


Figure 7.7: Simulation results for *case 5* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray).

7.2.4 Experimental results

The verification was accomplished using the experimental setup described in Appendix A.5. The bias current was chosen such that the required bias voltage equaled 5 V, which is $0.05U_{DC}$. The load has no significant influence; therefore a resistance of 100 Ω was used, resulting in low output current (approximately 1 A).

The spectra of the DM and CM voltages were measured by means of a Stanford Research Systems SR785 signal analyzer in swept-sine mode with 101 ms integration time. Tektronix isolated differential voltage probes (P5200A) with their gain set to 50:1 were used in combination with the two differential inputs of the analyzer to measure the results. The time waveforms were measured using a LeCroy Waverunner 44MXi-A oscilloscope. All measurement results have been post-processed in MATLAB.

Figures 7.8 and 7.9 depict measurement results for *case 1* and *2*. The time waveforms are in good agreement with the simulation results for both cases, except for some spikes on the CM voltage for *case 1*. The CM spectrum has small additional components with amplitudes smaller than 0.5 V, which do not significantly con-

Table 7.1: Overview of the simulation and (measurement) results of $u_{\mathrm{sn_{DM}}}$.

u^*_{bias}	WTHD				
	case 1	*case 2*	*case 3*	*case 4*	*case 5*
$0.00U_{\mathrm{DC}}$	1.27	0.35	0.35	0.35	0.08
$0.05U_{\mathrm{DC}}$	1.27 (1.26)	0.34 (0.34)	0.36 (0.36)	0.34 (0.34)	0.11 (0.11)
$0.20U_{\mathrm{DC}}$	1.19	0.28	0.47	0.28	0.27

tribute to the WTHD and WHD due to their small amplitude. These non-perfect harmonic eliminations might occur because of not perfectly aligned switching voltages, due to unequal delay in the driver circuits or IGBTs, component variation, or insufficient common-mode rejection ratio (CMRR) of the measurement equipment. The same applies for the DM spectrum of *case 2*.

Figures 7.10 and 7.11 show measurement results of *case 3* and *4*, respectively. The WTHDs and WHDs of the measurements are in good agreement with the simulation results. The spurious spectral components are small compared to the expected ones. Therefore, they do not influence the WTHDs significantly. Also the time measurements are in good agreement with the simulation results, except for the small spikes on the CM voltage for *case 3*, as already explained.

The last verified case, *case 5*, is depicted in Figure 7.12. The time waveforms agree quite well with the simulation results, and also both WTHD and WHD match the simulation results. Small spurious spectral components are again present on both spectra, but do not significantly contribute to the WTHD and WHD.

Tables 7.1 and 7.2 contain an overview of the simulated and measured data. It shows the trade-off between the DM and CM distortion for *cases 1* and *2*. For applications that have stricter CM requirements *cases 3* or *4* can be used. When a constant CM voltage is a requirement *cases 3* and *1* should be used. Applications that require the least amount of DM distortion are better off with *case 5*. However, care should be taken in closed-loop systems, since the additional spectral components due to u_{bias} can lead to undesired oscillations or an offset at the output of the converter when the sampling points are not chosen carefully. The best PWM strategy is thus application dependent.

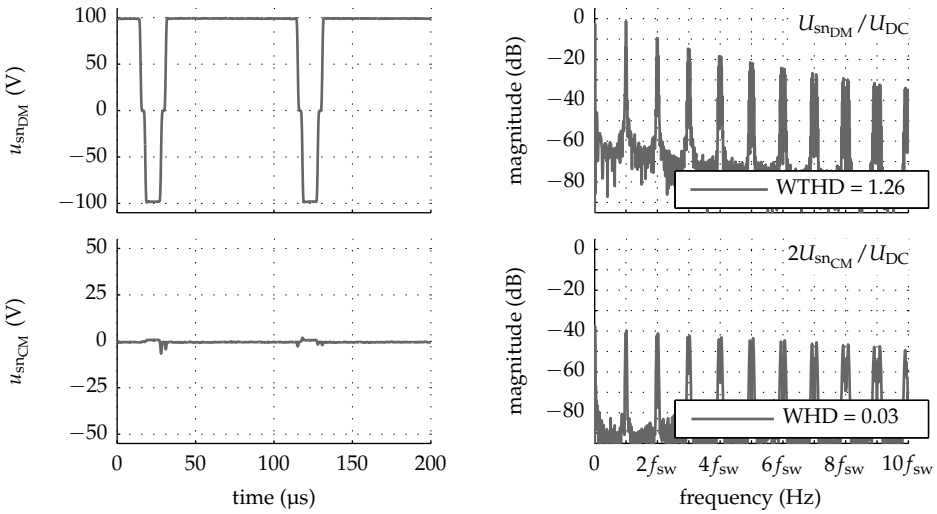


Figure 7.8: Measurement results of *case 1*: Switching waveforms (a) and corresponding normalized spectrum (b), for $u^*_{\mathrm{bias}} = 0.05U_{\mathrm{DC}}$.

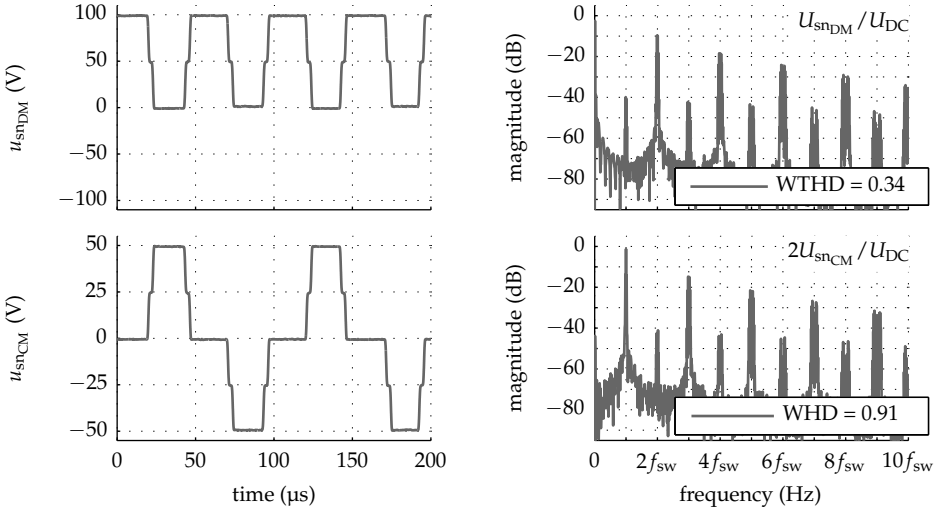


Figure 7.9: Measurement results of *case 2*: Switching waveforms (a) and corresponding normalized spectrum (b), for $u^*_{\mathrm{bias}} = 0.05U_{\mathrm{DC}}$.

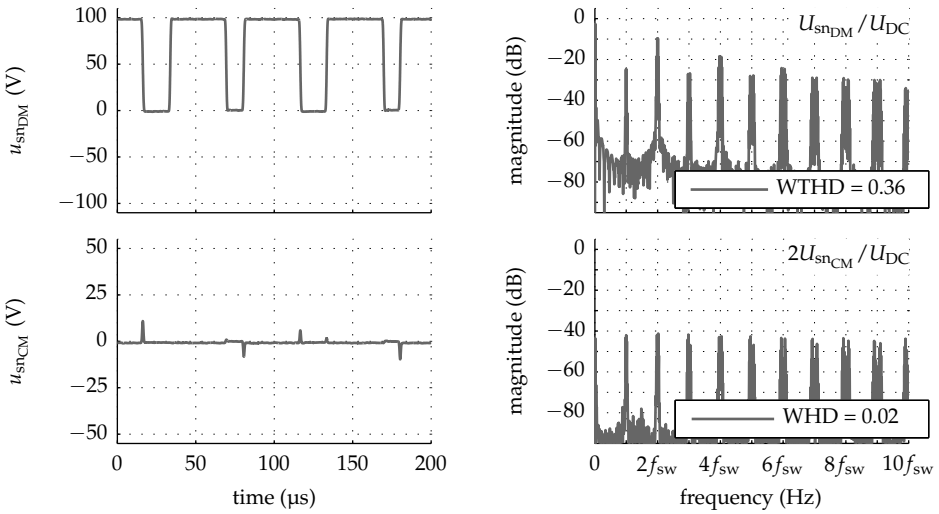


Figure 7.10: Measurement results of *case 3*: Switching waveforms (a) and corresponding normalized spectrum (b), for $u^*_{bias} = 0.05U_{DC}$.

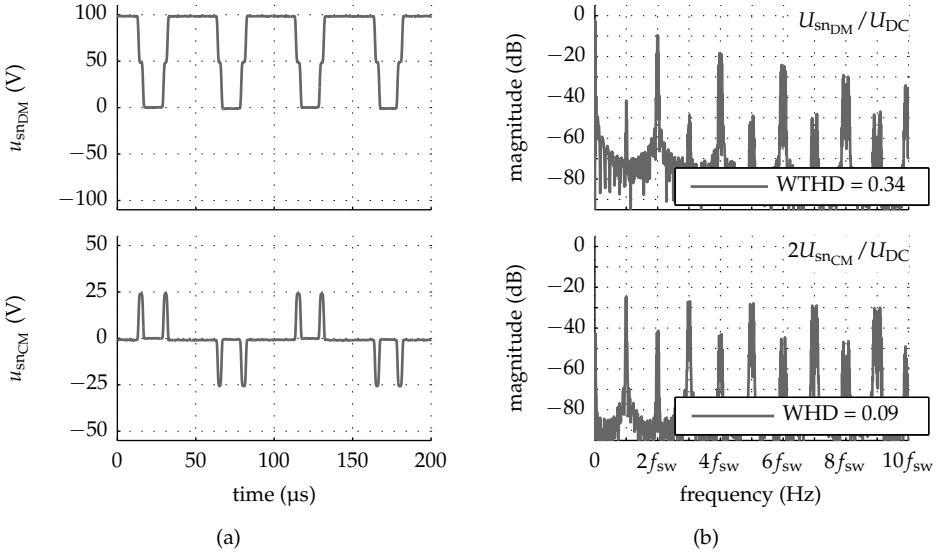


Figure 7.11: Measurement results of *case 4*: Switching waveforms (a) and corresponding normalized spectrum (b), for $u^*_{bias} = 0.05U_{DC}$.

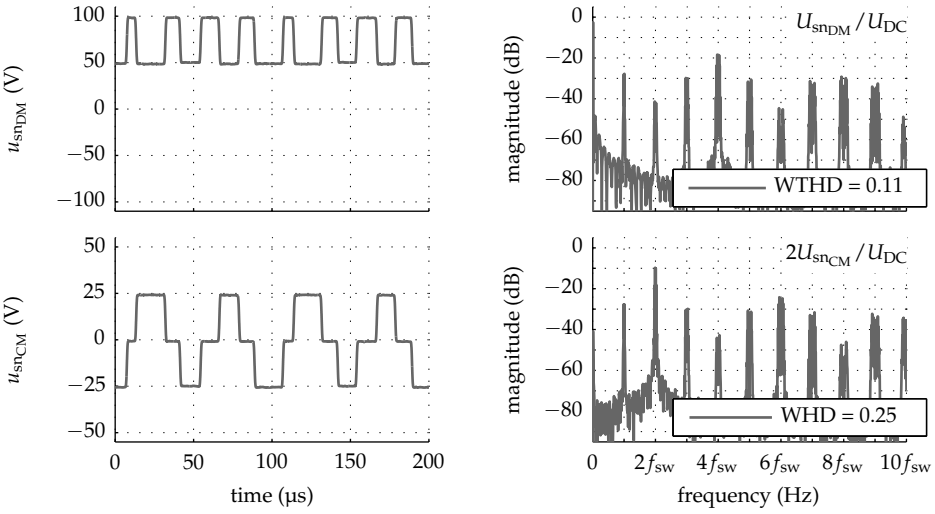


Figure 7.12: Measurement results of *case 5* with switching waveforms (a) and corresponding normalized spectrum (b), for $u^*_{\mathrm{bias}} = 0.05U_{\mathrm{DC}}$.

Table 7.2: Overview of the simulation and (measurement) results of $u_{\mathrm{sn_{CM}}}$.

u^*_{bias}	WHD				
	case 1	*case 2*	*case 3*	*case 4*	*case 5*
$0.00U_{\mathrm{DC}}$	0	0.92	0	0	0.25
$0.05U_{\mathrm{DC}}$	0 (0.03)	0.92 (0.91)	0 (0.02)	0.07 (0.09)	0.26 (0.25)
$0.20U_{\mathrm{DC}}$	0	0.87	0	0.28	0.29

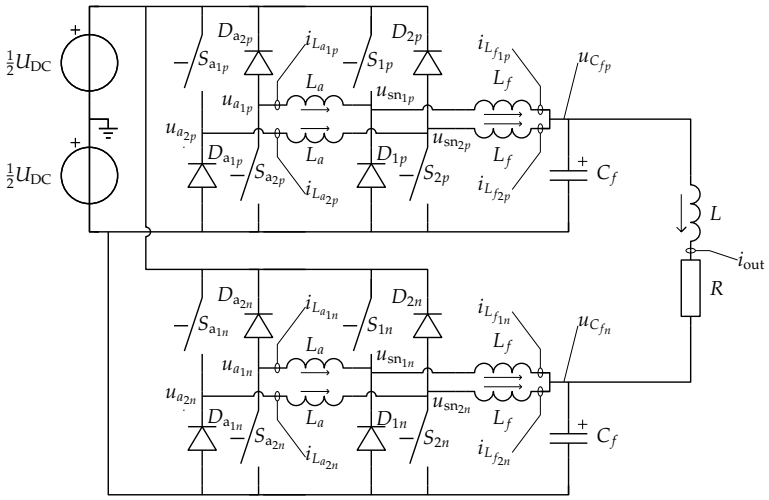


Figure 7.13: Schematic overview of full-bridge equivalent of the auxiliary-bias dual-buck converter.

7.3 Auxiliary-bias dual-buck converter

7.3.1 Full-bridge-equivalent circuit

Figure 7.13 depicts the full-bridge equivalent of the ABDB. The circuit consists basically of two sets of legs as introduced in Section 4.3. The positive and negative sets are indexed p and n, respectively. The resistive-inductive load is connected between the output terminals of the positive and negative filters. As for the conventional DB, for ease of explanation all voltages are again referenced to the mid-point of the symmetrical supply.

7.3.2 PWM generation

The full-bridge equivalent ABDB has two times more switching legs than the conventional DB. This leads to a more complex PWM modulator, as depicted in Figure 7.14. The gating signals, S_x, correspond to those of the switches in Figure 7.13. The carrier signals are triangularly shaped with unity amplitude, and the phase shift, ϕ_c, can be set arbitrarily. Furthermore, the variable transformation as discussed in Section 7.2.2 is also applied.

In Section 4.3 it was already shown that, in most cases, the best choice is to operate each auxiliary switching leg with the same frequency and PWM carrier phase

shift as the corresponding main leg, as indicated in Figure 7.14. The sampling points of the zero-order holds are aligned as depicted in Figure 7.2b. Since the ABDB does not require a voltage difference, u_{diff}, between its main legs, it is convenient to operate with interleaved switch-node voltages. Therefore, only three representative cases for PWM modulation remain for the ABDB:

$$\phi_c = \frac{\pi}{2} \begin{cases} \begin{pmatrix} 0 & 2 & 0 & 2 \end{pmatrix}, & \textit{case 3} \\ \begin{pmatrix} 0 & 2 & 2 & 0 \end{pmatrix}, & \textit{case 4} \\ \begin{pmatrix} 0 & 2 & 1 & 3 \end{pmatrix}, & \textit{case 5} \end{cases}$$

where the cases are labeled in accordance with the notation in Section 7.2, and the carrier phases are given by

$$\phi_c = \begin{pmatrix} 0 & \phi_{c_{2p}} & \phi_{c_{1n}} & \phi_{c_{2n}} \end{pmatrix}.$$

A comparison of the modulation methods is performed for three distinct levels of u_{bias}, namely $u_{\text{bias}} = 0\,\text{V}$, $u_{\text{bias}} = 0.05U_{\text{DC}}$, and $u_{\text{bias}} = 0.2U_{\text{DC}}$. The output is modulated to $u^*_{\text{avg}_{\text{DM}}} = 0.75U_{\text{DC}} \sin(2\pi f_o t)$, with $f_o = f_{\text{sw}}/100$, which results in a maximum modulation depth of the individual switching legs of 85 % for $u_{\text{bias}} = 0.2U_{\text{DC}}$. The DM and CM voltages are determined from (7.1), and WTHD and WHD from (7.4).

7.3.3 Simulation results

The WTHD and WHD are determined from simulated data, using only the harmonics of f_o up to $10f_{\text{sw}}$. Figures 7.15 and 7.16 depict the simulation results for *cases 3* and *4*. The results are equal to the $u_{\text{bias}} = 0\,\text{V}$ cases of the conventional DB. However, when bias voltage is present the spectrum remains unchanged for the ABDB. This is because the bias voltages are generated by the auxiliary legs, and not the legs that are connected to the output as for the DB. For the ABDB the results of PWM modulation *cases 3* and *4* are therefore identical.

For the ABDB it is thus possible to achieve a 3-level output voltage waveform with constant CM component, even with bias voltage present. The same result can be achieved using a conventional interleaved full-bridge converter. However, the latter will still suffer from output distortion due to blanking time. Moreover, it should be noted that the number of discrete semiconductors is the same as for the conventional interleaved FB and the full-bridge equivalent DB. However, the ABDB requires twice the amount of inductors compared to its conventional FB equal.

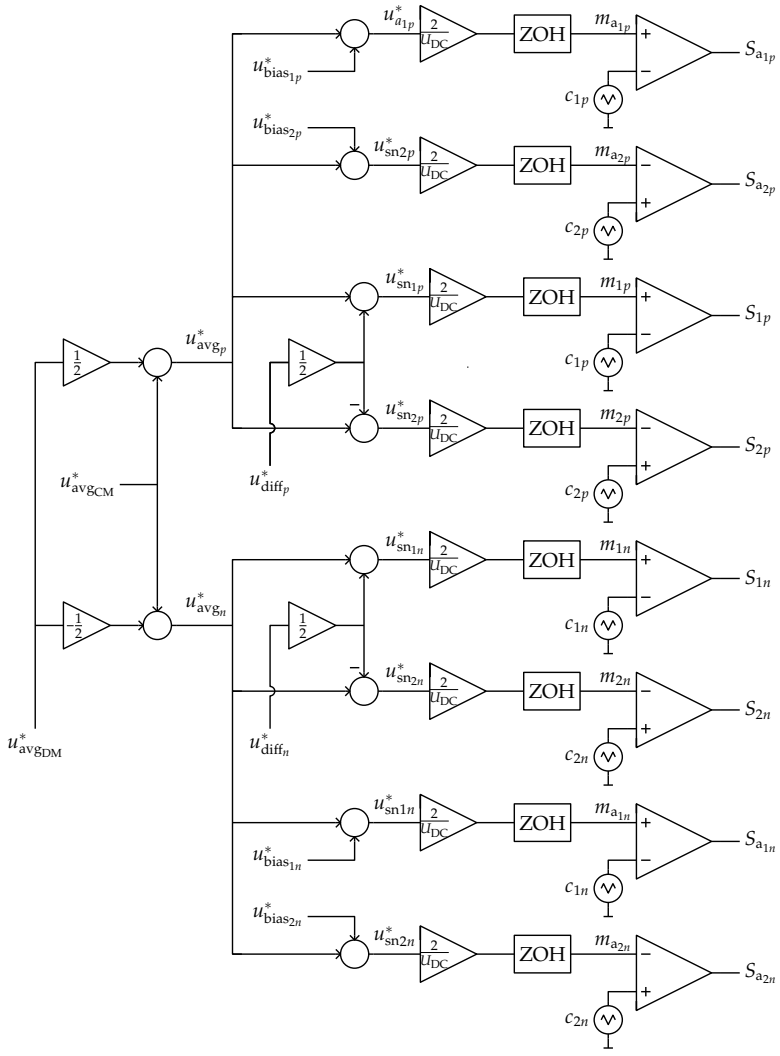


Figure 7.14: Schematic overview of the inverse decoupling and PWM generation.

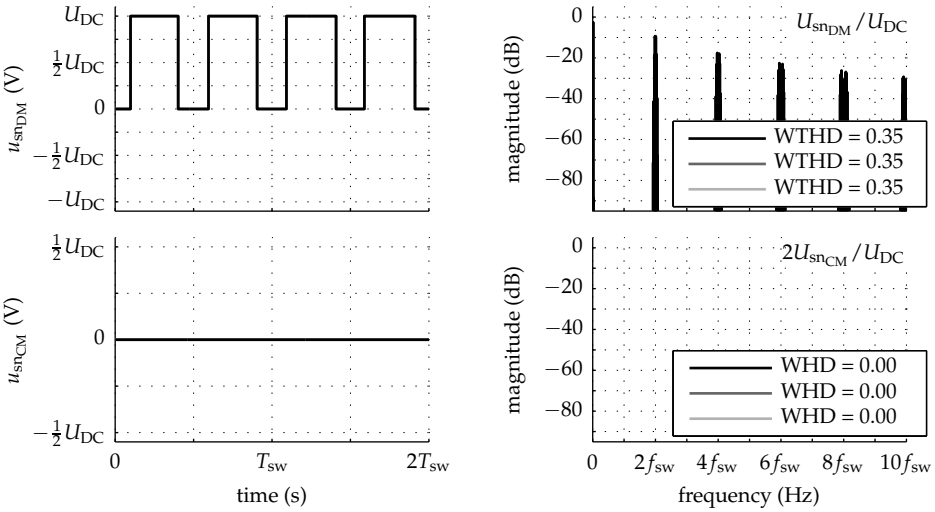


Figure 7.15: Simulation results for *case 3* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray). The cases illustrated in gray are not visible and exactly equal to the black case.

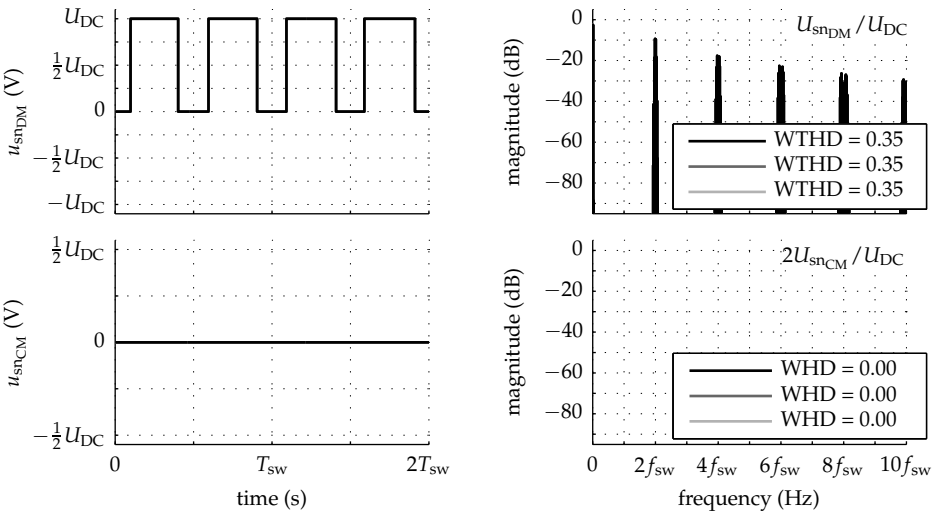


Figure 7.16: Simulation results for *case 4* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray). The cases illustrated in gray are not visible and exactly equal to the black case.

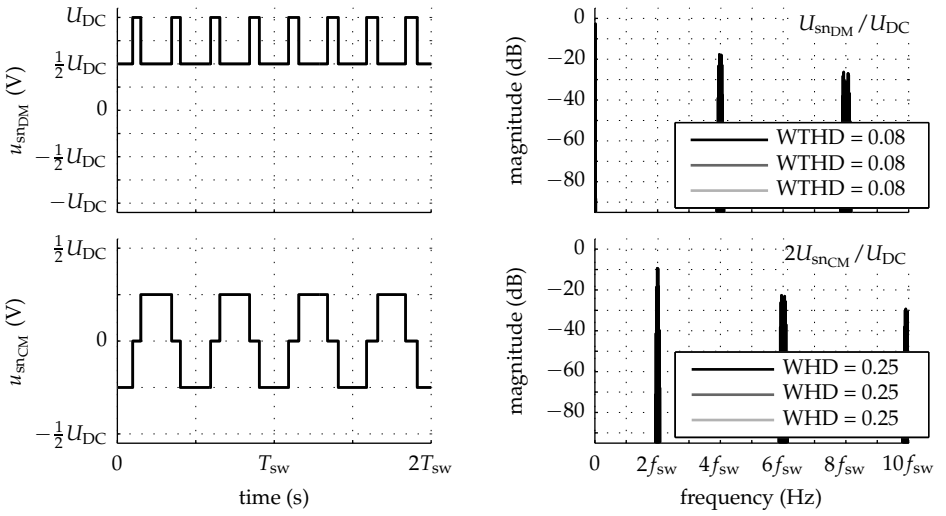


Figure 7.17: Simulation results for *case 5* with switching waveforms (a) and corresponding normalized spectra (b), for $u^*_{bias} = 0$ (black), $u^*_{bias} = 0.05U_{DC}$ (gray), and $u^*_{bias} = 0.2U_{DC}$ (light gray). The cases illustrated in gray are not visible and exactly equal to the black case.

Figure 7.17 depicts the simulation results for *case 5*. For this case the voltage waveforms and spectra are not dependent on the bias voltage level that is required. Of course it is assumed that u_{diff_x} is zero volts, which is true for equal $i_{L_{f_{1x}}}$ and $i_{L_{f_{2x}}}$.

An overview of the simulation results is presented in Tables 7.3 and 7.4. It shows that the weighted distortion is not dependent on the bias voltage. Furthermore, for *cases 3* to *5*, the amount of distortion for the ABDB is equal to a conventional DB that does not require a bias voltage. The ABDB, however, uses two times more switching legs than the conventional DB. Due to limitations of the experimental setup no measurements were performed for the ABDB

7.4 Summary

This chapter compares five different regular-sampled PWM modulation strategies for the DB and ABDB, with the aim to determine the output spectra. The DB features more interleaving flexibility with respect to conventional converters. However,

Table 7.3: Overview of the simulation results of $u_{\mathrm{sn_{DM}}}$.

u^*_{bias}	WTHD		
	case 3	*case 4*	*case 5*
$0.00U_{\mathrm{DC}}$	0.35	0.35	0.08
$0.05U_{\mathrm{DC}}$	0.35	0.35	0.08
$0.20U_{\mathrm{DC}}$	0.35	0.35	0.08

Table 7.4: Overview of the simulation results of $u_{\mathrm{sn_{CM}}}$.

u^*_{bias}	WHD		
	case 3	*case 4*	*case 5*
$0.00U_{\mathrm{DC}}$	0	0	0.25
$0.05U_{\mathrm{DC}}$	0	0.07	0.25
$0.20U_{\mathrm{DC}}$	0	0.28	0.25

care should be taken when significant bias voltage is required since it adds additional spectral components to the output voltage, depending on the interleaving strategy.

For bipolar and unipolar switching, the bias voltage has a positive effect on the DB output voltage spectra. By selecting the appropriate interleaving strategy it is even possible to achieve 3-level PWM with doubled output ripple frequency and constant, or nearly perfect, CM voltage at the output of the converter. That is to say, the best features of both unipolar and bipolar switching can be retained.

The ABDB is functionally equivalent to a conventional interleaved FB. The bias voltage has no influence on the output spectra, thus no concessions need to be made in that respect. However, it should be noted that when comparing the ABDB to two parallel-connected DBs, the same spectral performance can be obtained. The ABDB requires two inductors more per switching leg compared to the conventional FB interleaved converter and leads to a similar inductor volume as can be obtained with parallel-connected DBs, as was discussed in Chapter 5.

Chapter 8

Feedback control

"It is a mistake to think you can solve any major problems just with potatoes."

(Douglas Adams)

Abstract — Switched-mode power electronic converters process electric power efficiently by directing energy flow between intermediate storage components. Even though accurate models can be obtained, simple feedforward control is in most cases insufficient because of uncertainties and/or unmodeled dynamics of the connected sources, loads, and the converter itself. This chapter describes basic modeling of the dual-buck topology and presents two different output current feedback control strategies. The first strategy applies decoupled single-input single-output control of output and bias current, and the second approach is based on full state feedback with its dynamics chosen such that a constant group delay is obtained over a wide frequency range.

Contributions of this chapter are published in:

– J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "High-precision current control through opposed current converters," in *Proceedings of the 14th European conference on Power Electronics and applications (EPE)*, 2011, pp. 1–10.

8.1 Introduction

Switched-mode power electronic converters are non-linear due to their switching nature. However, small-signal input-to-output behavior can be captured quite accurately for moderate switching frequencies, by application of the state-space averaging method [65]. When averaging cannot be used or does not provide the desired accuracy, the sampled-data modeling method [26,43] can be used instead.

Even when the switching components are assumed ideal, models tend to be relatively accurate, which is related to the high efficiency that can be obtained with modern semiconductor devices. However, feedforward control is in many cases not sufficient, because uncertainties and unmodeled dynamics can result in poor performance or undesired behavior. Therefore, most converters have some kind of feedback control to regulate their outputs to the desired values.

Depending on the desired system specifications and allowed system cost different sorts of feedback control are applied in SMPCs. Such controllers contain digital and/or analog, linear and/or nonlinear feedback loops. Amplifiers for systems that require high precision and good reproducibility often rely on well established techniques such as fixed-frequency DPWM in combination with discrete single-input single-output (SISO) or full state-feedback control.

However, the increasing availability of low-cost computational power bundled with recent innovations in the control systems field permit considerable improvement of control algorithms for next-generation power amplifiers. For example, customization of real-time solvers made the use of implicit model-predictive control (MPC) with sampling rates in the tens of kHz range possible [25,59,83]. Moreover, the advances in the computation and real-time implementation of explicit MPC and its approximations permit sampling rates in the MHz range for simple converters [58,104].

Solutions have been proposed to extend the domain of safe operation of a power amplifier under constraints, by application of reference governors [102], and by using set-theoretic methods [2,103]. Furthermore, steps have been made to incorporate the information on the available computational resources in the controller design procedure [101], with the aim to fully exploit the capabilities of the control hardware, to achieve the highest performance while guaranteeing the safety constraints of the converter.

This chapter presents two classical control approaches. First, a linear decoupled control of both output and bias current for DBs is introduced, using fixed-frequency DPWM and relatively low-bandwidth measurement of the filter induc-

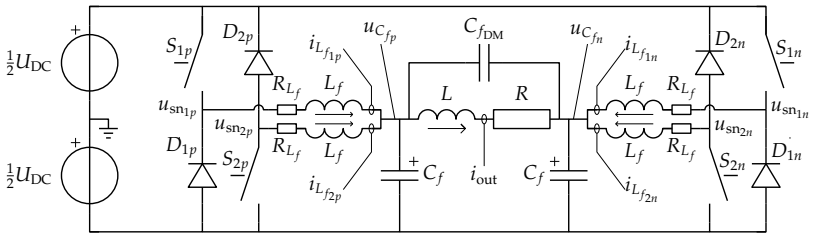


Figure 8.1: Schematic overview of full-bridge equivalent DB.

tor current. Second, a full-state-feedback controller is proposed that is based on a prototype system approach as suggested in [120]. The dynamics of the closed-loop system are chosen such that there is a constant group delay from output current reference to output current. The resulting closed-loop system is especially suited for systems that require low distortion and a constant group delay from input to output, like studio-quality audio amplification and gradient amplifiers in MRI systems.

8.2 Small-signal model of the full-bridge dual-buck converter

Figure 8.1 depicts a schematic overview of the full-bridge equivalent DB used in this chapter. The full-bridge equivalent DB consists of two DB legs with the load, represented by R and L, connected in between. Separate cut-off frequencies can be set for the differential-mode and common-mode voltages across the load by means of $C_{f_{\mathrm{DM}}}$ and C_f.

When neglecting the effects of the load impedance, the cut-off frequencies for the differential-mode and common-mode voltages across the load are given by

$$f_{o_{\mathrm{DM}}} = \frac{1}{2\pi\sqrt{L_f\left(C_{f_{\mathrm{DM}}} + \frac{1}{2}C_f\right)}} \tag{8.1a}$$

$$f_{o_{\mathrm{CM}}} = \frac{1}{2\pi\sqrt{\frac{1}{2}L_f C_f}} \tag{8.1b}$$

where L_f are the filter inductances, and C_f and $C_{f_{\mathrm{DM}}}$ are the filter capacitors. The CM cut-off frequency is determined by L_f and C_f, and the DM cut-off frequency depends on L_f and the combination of C_f and the filter capacitance across the

Figure 8.2: Switch (a) and diode (b) model used for state-space averaging.

load $C_{f_{DM}}$.

The controllers developed in this chapter are based on linear models. Switched-mode converters are nonlinear and, therefore, a linearizion of the plant is required. There are various methods to obtain linear models of switching converters. In Chapter 2 the state-space averaging method was highlighted. State-space averaging results in time-continuous analytical models that are dependent on the operating point being described as

$$\dot{\tilde{\mathbf{x}}} = \mathbf{A}(\mathbf{u}_o)\tilde{\mathbf{x}} + \mathbf{B}(\mathbf{x}_o, \mathbf{u}_o)\tilde{\mathbf{u}} + \mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) \tag{8.2a}$$

$$\dot{\tilde{\mathbf{y}}} = \mathbf{C}\tilde{\mathbf{x}} \tag{8.2b}$$

where $\tilde{\mathbf{x}}$ represents a small-signal perturbation from the operating point $\mathbf{x}_o$, the same notation applies for input vector $\mathbf{u}$, and $\mathbf{w}_o$ represents a constant disturbance input. The state, input and output matrices in (8.2) can be obtained using the method explained in Chapter 2. In (8.2) it is assumed that the output matrix ($\mathbf{C}$) is not operating-point dependent, which is true for the models derived in this section.

The switches and diodes depicted in Figure 8.1 are ideal. To be able to determine the influence of the first-order effects of these components on the developed small-signal model the switches and diodes are modeled as ideal switches and diodes with parasitic series resistance in series with a voltage source, as shown in Figure 8.2.

The state and input vectors are chosen as

$$\mathbf{x} = \begin{pmatrix} i_{\text{out}} & i_{L_{f_{1p}}} & i_{L_{f_{2p}}} & i_{L_{f_{1n}}} & i_{L_{f_{2n}}} & u_{C_{fp}} & u_{C_{fn}} \end{pmatrix}^\mathsf{T} \tag{8.3}$$

$$\mathbf{u} = \begin{pmatrix} m_{1p} & m_{2p} & m_{1n} & m_{2n} \end{pmatrix}^\mathsf{T} \tag{8.4}$$

where m_{xy} are the modulation indexes of the corresponding switching legs.

When assuming CCM the state and input matrices can be deduced by applying the

state-space averaging and linearizing procedure explained in Chapter 2, resulting in

$$\mathbf{A}(\mathbf{u}_o) = \begin{pmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & \frac{1}{L} & -\frac{1}{L} \\ 0 & -\frac{R_{1p}}{L_f} & 0 & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & -\frac{R_{2p}}{L_f} & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & 0 & -\frac{R_{1n}}{L_f} & 0 & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_{2n}}{L_f} & 0 & -\frac{1}{L_f} \\ -a_1 & a_2 & a_2 & a_3 & a_3 & 0 & 0 \\ a_1 & a_3 & a_3 & a_2 & a_2 & 0 & 0 \end{pmatrix} \tag{8.5}$$

and

$$\mathbf{B}(\mathbf{x}_o) = \begin{pmatrix} 0 & 0 & 0 & 0 \\ \frac{U_{1p}}{L_f} & 0 & 0 & 0 \\ 0 & \frac{U_{2p}}{L_f} & 0 & 0 \\ 0 & 0 & \frac{U_{1n}}{L_f} & 0 \\ 0 & 0 & 0 & \frac{U_{2n}}{L_f} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \tag{8.6}$$

with

$$a_1 = \frac{1}{C_f + 2C_{f_{\mathrm{DM}}}} \tag{8.7a}$$

$$a_2 = \tfrac{1}{2C_f} + \tfrac{1}{2}a_1 \tag{8.7b}$$

$$a_3 = \tfrac{1}{2C_f} - \tfrac{1}{2}a_1 \tag{8.7c}$$

where R_{1p} to R_{2n} represent equivalent resistances which depend on the operating

point, given by

$$R_{1p} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\text{on}}\right) - \frac{1}{2}\left(R_f - R_{\text{on}}\right) M_{1p} \tag{8.8a}$$

$$R_{2p} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\text{on}}\right) + \frac{1}{2}\left(R_f - R_{\text{on}}\right) M_{2p} \tag{8.8b}$$

$$R_{1n} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\text{on}}\right) - \frac{1}{2}\left(R_f - R_{\text{on}}\right) M_{1n} \tag{8.8c}$$

$$R_{2n} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\text{on}}\right) + \frac{1}{2}\left(R_f - R_{\text{on}}\right) M_{2n} \tag{8.8d}$$

and where U_{1p} to U_{2n} denote the operating-point-dependent switching-leg voltages, which in turn are given by

$$U_{1p} = \frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right) + \frac{1}{2}\left(R_f - R_{\text{on}}\right) I_{L_{f_{1p}}} \tag{8.9a}$$

$$U_{2p} = \frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right) - \frac{1}{2}\left(R_f - R_{\text{on}}\right) I_{L_{f_{2p}}} \tag{8.9b}$$

$$U_{1n} = \frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right) + \frac{1}{2}\left(R_f - R_{\text{on}}\right) I_{L_{f_{1n}}} \tag{8.9c}$$

$$U_{2n} = \frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right) - \frac{1}{2}\left(R_f - R_{\text{on}}\right) I_{L_{f_{2n}}}. \tag{8.9d}$$

The disturbance input is given by (8.10)

$$\mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) = \mathbf{A}(\mathbf{u}_o)\mathbf{x}_o + \mathbf{B}(\mathbf{0})\mathbf{u}_o + \mathbf{B}_\omega(\mathbf{0})\boldsymbol{\omega}_o \tag{8.10}$$

with

$$\mathbf{B}_\omega(\mathbf{0}) = \frac{1}{\frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right)}\mathbf{B}(\mathbf{0}) \tag{8.11}$$

where $\mathbf{B}(\mathbf{0})$ is determined by (8.6) and (8.9). The disturbance input $\boldsymbol{\omega}_o$ is given by

$$\boldsymbol{\omega}_o = \frac{1}{2}\left(V_f + V_{\text{on}}\right)\begin{pmatrix} -1 & 1 & -1 & 1 \end{pmatrix}^{\mathsf{T}}. \tag{8.12}$$

From (8.8) and (8.9) it can be seen that the operation-point dependency of the small-signal model is removed when R_f equals R_{on}, which is in agreement with the results presented in Chapter 6. Moreover, when $R_f = R_{\text{on}}$ the averaged state matrix becomes time-invariant, making the averaging procedure exact, as explained in Section 2.2. A complete derivation of the state-space averaged model can be found in Appendix C.

Power amplifiers generally have a broad operating range that covers most of the output voltage and current plane. In this case there is no fixed operating point for the design of the control system, and the chosen operating point is the center of the range of the elements of $\mathbf{x}_o$ and $\mathbf{u}_o$, in this particular case $\mathbf{x}_o = \mathbf{0}$ and $\mathbf{u}_o = \mathbf{0}$. For the sake of simplicity of notation, (8.2) is expressed as

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} + \mathbf{B}_\omega \boldsymbol{\omega}_o \tag{8.13a}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} \tag{8.13b}$$

from here on, where $\mathbf{A} = \mathbf{A}(\mathbf{0})$, $\mathbf{B} = \mathbf{B}(\mathbf{0})$, and $\mathbf{B}_\omega = \mathbf{B}_\omega(\mathbf{0})$. It should again be noted that when R_{on} equals R_f the average model is exact over the complete operating range. However, when $R_{\text{on}} \neq R_f$ the model becomes inaccurate when deviating from the chosen operating point. The amount of error introduced depends on the relative contribution of the operating-point-dependent terms in $\mathbf{A}(\mathbf{u})$ and $\mathbf{B}(\mathbf{x})$ and can be taken into account in the feedback controller design.

The feedback methods discussed in this chapter require only measurement of the currents in the state vector, as a result $\mathbf{y}$ is given by

$$\mathbf{y} = \begin{pmatrix} i_{\text{out}} & i_{L_{f_{1p}}} & i_{L_{f_{2p}}} & i_{L_{f_{1n}}} & i_{L_{f_{2n}}} \end{pmatrix} \tag{8.14}$$

and consequently

$$\mathbf{C} = \begin{pmatrix} \mathbf{I}_5 & \mathbf{0} \end{pmatrix} \tag{8.15}$$

where $\mathbf{I}_5$ is an 5×5 identity matrix, and $\mathbf{0}$ is a 5×2 matrix with zeros.

8.2.1 Discretization

The obtained averaged model is time-continuous. However, for discrete control the time-continuous model needs to be discretized. Figure 8.3 depicts the discretized model assuming zero-order hold inputs. One control update cycle delay is added to incorporate the time required for the data acquisition, and calculation of the new modulation indices for the PWM modulators.

The ADCs sample simultaneously and are triggered two times per switching cycle, at the maximum and minimum value of the carrier signal of the PWM modulator of switching leg $1p$. Consequently, the sample and controller update cycle time T_s equals $\frac{1}{2}T_{\text{sw}}$. When the ADCs finish converting the measured data the controller is executed, which calculates new modulation indices for the PWM modulators. The new modulation indices are applied by the PWM modulators simultaneously

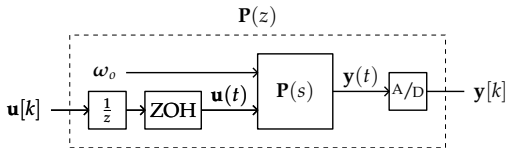


Figure 8.3: Zero order hold discretized model of the DB with one control cycle delay.

at the next trigger.

The resulting discrete state-space model is given by

$$\mathbf{x}[k+1] = \mathbf{\Phi}\mathbf{x}[k] + \mathbf{\Gamma}\mathbf{u}[k] + \mathbf{\Gamma}_\omega \boldsymbol{\omega}_o \tag{8.16a}$$

$$\mathbf{y}[k] = \mathbf{C}\mathbf{x}[k] \tag{8.16b}$$

where a zero-order hold for the inputs is assumed; that is to say, the inputs remain constant over a sampling-time interval. The matrices $\mathbf{\Phi}$, $\mathbf{\Gamma}$, and $\mathbf{\Gamma}_\omega$ can be obtained from the time-continuous model by the procedure described in Chapter 2.

When implementing control systems based on state-space averaged models the measured signals need to be sampled at their periodic average value. Therefore, for a PWM converter the sampling time T_s of the discrete model and its switching time T_{sw} are usually integer multiples of each other. For PWM with a triangular carrier waveform, the periodic average of the current through an inductor that is connected to a switching leg, with a voltage source as input, occurs approximately at the maximum and minimum values of the carrier signal.

Figure 8.4 depicts the regular-sampled PWM signals together with the corresponding steady-state filter inductor currents and capacitor voltage of one DB leg, as illustrated in Figure 8.1, for both one sample per PWM cycle and two samples per PWM cycle. A small offset is added to the gating signals to increase visibility in the picture. The overlap in the gating signals is due to the exaggerated bias voltage, in this case 20 % of U_{DC}. The inductor currents and capacitor voltage are offset by their average value.

Figures 8.4a and 8.4b illustrate that the sampled inductor current approximates the periodic average value. The error of the sampled currents with respect to the periodic average is operating-point-dependent. This can be seen for both inductor currents in Figure 8.4a, where the modulation indices of both legs differ because of the bias voltage. The operating-point dependency of the measurement error of the sampled data leads to harmonic distortion when feedback is applied.

However, when no resistive losses are present and when the capacitor voltage is constant over each switching cycle the sampled currents are exactly equal to the periodic average values, resulting in no harmonic distortion.

The same does not apply for capacitor voltage, as can be seen in Figure 8.4a. The sampled capacitor voltage does not approximate the periodic average value of the voltage. In fact, when no resistive losses are present the capacitor voltages in the DB are exactly sampled at the tops or valleys of the switching ripple. The offset error of the sampled data of the capacitor voltage is also operating-point dependent, which again leads to harmonic distortion when feedback is applied.

A better measurement of the periodic average values can be obtained by taking two samples per PWM cycle. Figure 8.4b depicts the sampled data for the filter inductor currents and capacitor voltage when two samples are taken per switching cycle. The average value of two successive samples is a much better approximate of the cycle average value, resulting in less low-frequency harmonic distortion when feedback is applied. This comes at the cost of additional harmonic distortion at the switching frequency when asymmetrical regular-sampled PWM is applied. It should be noted that, in practice, the sampled inductor currents better approximate their average value than the sampled capacitor voltages.

Also a delay of the sample positions with respect to the current and voltage waveforms leads to an operating-point-dependent measurement error. This error can also be reduced when using two samples per switching cycle.

In practice resistive losses are small in converters, and sampling delay can be compensated if desired. Furthermore, the filter capacitors are chosen such that the ripple is small compared to the supply voltage, or the capacitor voltages can be estimated with an observer. Therefore, error of the sampled signals can in many cases be neglected. Better periodic average values can of course be obtained by filtering of the measured signals, or by applying a combination of oversampling and digital filtering, as in Δ-Σ ADCs. This is, however, not treated in this thesis.

8.2.2 Modulator gain

The inputs of the discretized state-space averaged model (8.4) that are required for control are dimensionless modulation indices. Desired voltages as inputs of the system provide more insight. By introducing a modulator gain $\mathbf{T}$, as depicted in Figure 8.5, the inputs are normalized to the desired voltages $\mathbf{u}_{\mathrm{sn}}^{*}$.

The resulting control input vector $\mathbf{u}_{\mathrm{sn}}^{*}$ and the modulator gain matrix $\mathbf{T}$ are given

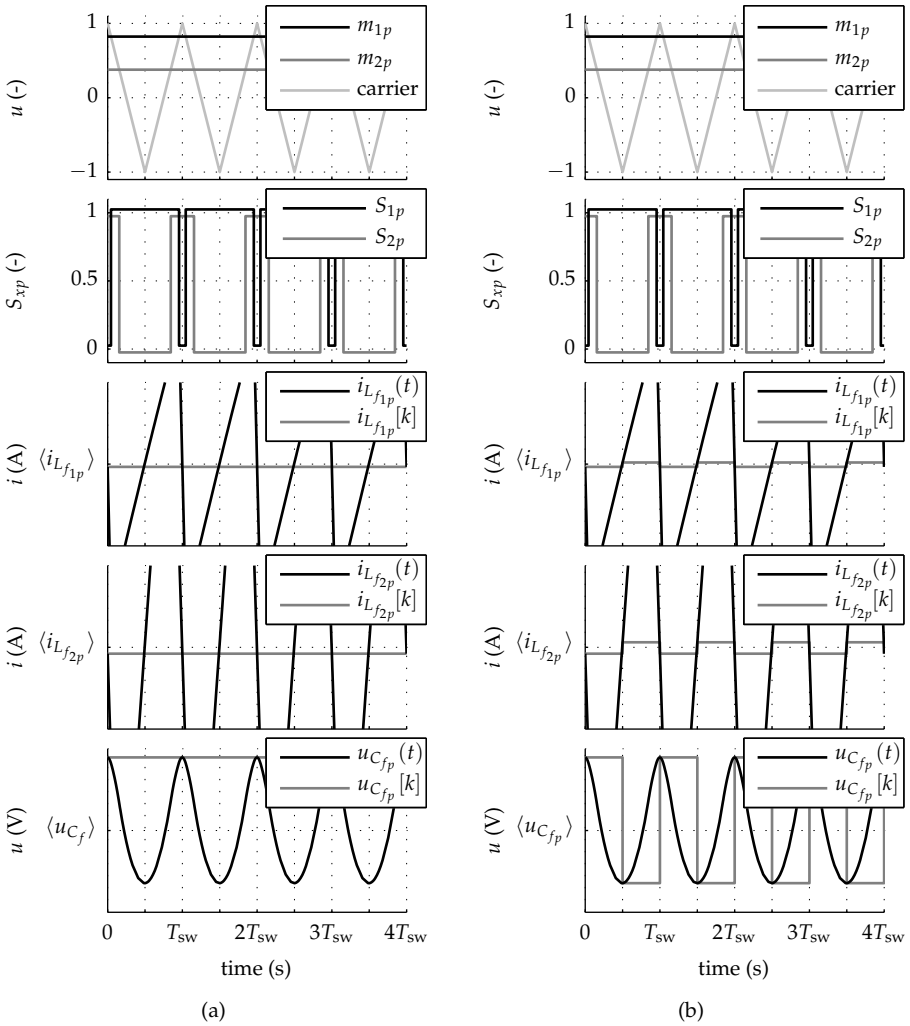


Figure 8.4: Time-continuous and sampled filter inductor current and capacitor voltage waveforms with the corresponding PWM signals for (a) one sample per switching cycle, and (b) two samples per switching cycle.

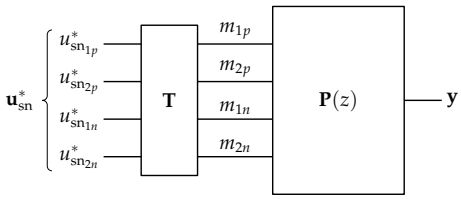


Figure 8.5: Discrete DB model with PWM modulator gain (**T**).

by

$$\mathbf{u}^*_{\text{sn}} = \begin{pmatrix} u^*_{\text{sn}_{1p}} & u^*_{\text{sn}_{2p}} & u^*_{\text{sn}_{1n}} & u^*_{\text{sn}_{2n}} \end{pmatrix}^{\mathsf{T}} \tag{8.17}$$

and

$$\mathbf{T} = \frac{1}{K_{\text{PWM}}}\mathbf{I}_4 \tag{8.18}$$

where $\mathbf{I}_4$ is a (4×4) identity matrix. For the discrete averaged model deduced in this chapter K_{PWM} becomes

$$K_{\text{PWM}} = \frac{1}{2}U_{\text{DC}} + \frac{1}{2}\left(V_f - V_{\text{on}}\right) \tag{8.19}$$

which can be approximated as $K_{\text{PWM}} \approx \frac{1}{2}U_{\text{DC}}$ when $V_f - V_{\text{on}}$ is small compared to U_{DC}.

8.3 A classical approach

The full-bridge equivalent DB model introduced in Section 8.2 is a multiple-input multiple-output (MIMO) system with 4 inputs in $\mathbf{u}^*_{\text{sn}}$, and 3 control objectives: DCM should be prevented for both the positive and the negative side switching legs, and the voltage across, or the current through the load must be regulated to the desired value.

Due to their simplicity, classical SISO controllers are often applied in an industrial environment. Before classical SISO control can be applied on the MIMO DB it is essential to be able to decouple the control of the output current and the current required to prevent DCM.

The input and output decoupling proposed here is based in the transformations given in (4.9), (4.10), and (7.1). The decoupled input and output vectors are given

by

$$\mathbf{u}' = \begin{pmatrix} u^*_{\mathrm{avg}_{\mathrm{DM}}} & u^*_{\mathrm{avg}_{\mathrm{CM}}} & u^*_{\mathrm{bias}_p} & u^*_{\mathrm{bias}_n} \end{pmatrix}^\mathsf{T} \tag{8.20}$$

$$\mathbf{y}' = \begin{pmatrix} i_{\mathrm{out}} & i_{C_{f_{\mathrm{DM}}}} & i_{C_{f_{\mathrm{CM}}}} & i_{\mathrm{bias}_p} & i_{\mathrm{bias}_n} \end{pmatrix}^\mathsf{T} \tag{8.21}$$

where the input vector $\mathbf{u}'$ corresponds to the input of the PWM modulator proposed in Chapter 7, which is given in Figure 7.2a. The output vector contains the output current (i_{out}), both bias currents (i_{bias_p} & i_{bias_n}), and the decoupled capacitor currents ($i_{C_{f_{\mathrm{DM}}}}$ & $i_{C_{f_{\mathrm{CM}}}}$), which in turn are given by

$$i_{C_{f_{\mathrm{DM}}}} = \tfrac{1}{2}\left(i_{C_{fp}} - i_{C_{fn}}\right) \tag{8.22a}$$

$$i_{C_{f_{\mathrm{CM}}}} = i_{C_{fp}} + i_{C_{fn}}. \tag{8.22b}$$

The input and output decoupling is given by

$$\mathbf{u}' = \mathbf{G}\mathbf{u}_{\mathrm{sn}} \tag{8.23a}$$

$$\mathbf{y}' = \mathbf{H}\mathbf{y} \tag{8.23b}$$

where corresponding transformation matrices $\mathbf{G}$ and $\mathbf{H}$ are given by

$$\mathbf{G} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{pmatrix} \tag{8.24}$$

and

$$\mathbf{H} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 \\ -1 & \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ 0 & 1 & 1 & 1 & 1 \\ 0 & \frac{1}{2} & -\frac{1}{2} & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2} & -\frac{1}{2} \end{pmatrix} \tag{8.25}$$

resulting in the following decoupled state-space representation

$$\mathbf{x}[k+1] = \mathbf{\Phi}\mathbf{x}[k] + \mathbf{\Gamma}\mathbf{T}\mathbf{G}^{-1}\mathbf{u}'[k] + \mathbf{\Gamma}\mathbf{T}\mathbf{G}^{-1}\boldsymbol{\omega}'_o \tag{8.26a}$$

$$\mathbf{y}' = \mathbf{H}\mathbf{C}\mathbf{x}[k] \tag{8.26b}$$

where $\mathbf{\Gamma T} = \mathbf{\Gamma}_\omega$, and the decoupled constant disturbance input becomes

$$\boldsymbol{\omega}_o' = \left(V_f + V_{\text{on}}\right) \begin{pmatrix} 0 & 0 & -1 & -1 \end{pmatrix}^\mathsf{T}. \tag{8.27}$$

From (8.27) it can be seen that the forward voltage of the diodes and switches have to be compensated only for the bias voltage references ($u^*_{\text{bias}_p}$ & $u^*_{\text{bias}_n}$), as was already pointed out in Chapter 6. When integrating control is applied for the bias current regulation no further compensation is required for the forward voltages of the switches and diodes.

Figure 8.6 depicts the Bode diagrams of the non-zero transfer functions of the decoupled plant, using the component values of the experimental setup described in Chapter 9. Figure 8.6a shows the resonance, which is mainly due to the output filter (L_f & C_f). The real pole, mainly due to the load (R & L), is not clearly visible because in this case it is close the resonance frequency of the filter. As a result the roll-off of the Bode magnitude is 3^{th} order, that is -60 dB per decade.

The Bode diagram of the transfer function from $u^*_{\text{bias}_x}$ to i_{bias_x}, depicted in Figure 8.6b, has a first-order response which is mainly determined by (L_f & R_{L_f}). Figures 8.6c and 8.6d depict the Bode diagrams of the transfer functions from the DM and CM voltage references to the corresponding capacitor currents, respectively. From Figure 8.6c and Figure 8.6d it can be seen that the CM resonance appears at a higher frequency and is damped less than the DM resonance. This is due to R and L, which do not appear in the CM transfer functions. The transfer functions of the capacitor currents will be fed back to actively damp both resonances. The other transfer functions are zero as will be shown later in this section. Furthermore, it should be noted that $\mathbf{P}(z)$ includes one control cycle delay resulting in more phase lag than normally expected from third-, second-, and first-order responses.

The block diagram of the decoupled control system is depicted in Figure 8.7. As already pointed out the decoupled capacitor currents are fed back to damp oscillations of the system. Two bias current controllers K_{bias} regulate the bias currents (i_{bias_p} & i_{bias_n}) and K_{out} regulates the output current (i_{out}). The modulator gain matrix ($\mathbf{T}$), and the decoupling matrices ($\mathbf{G}$ & $\mathbf{H}$) appear at the inputs and outputs of the discretized plant ($\mathbf{P}$). The common-mode output voltage is set to zero by $u^*_{\text{out}_{\text{CM}}}$, which maximizes the output voltage range for the proposed scheme.

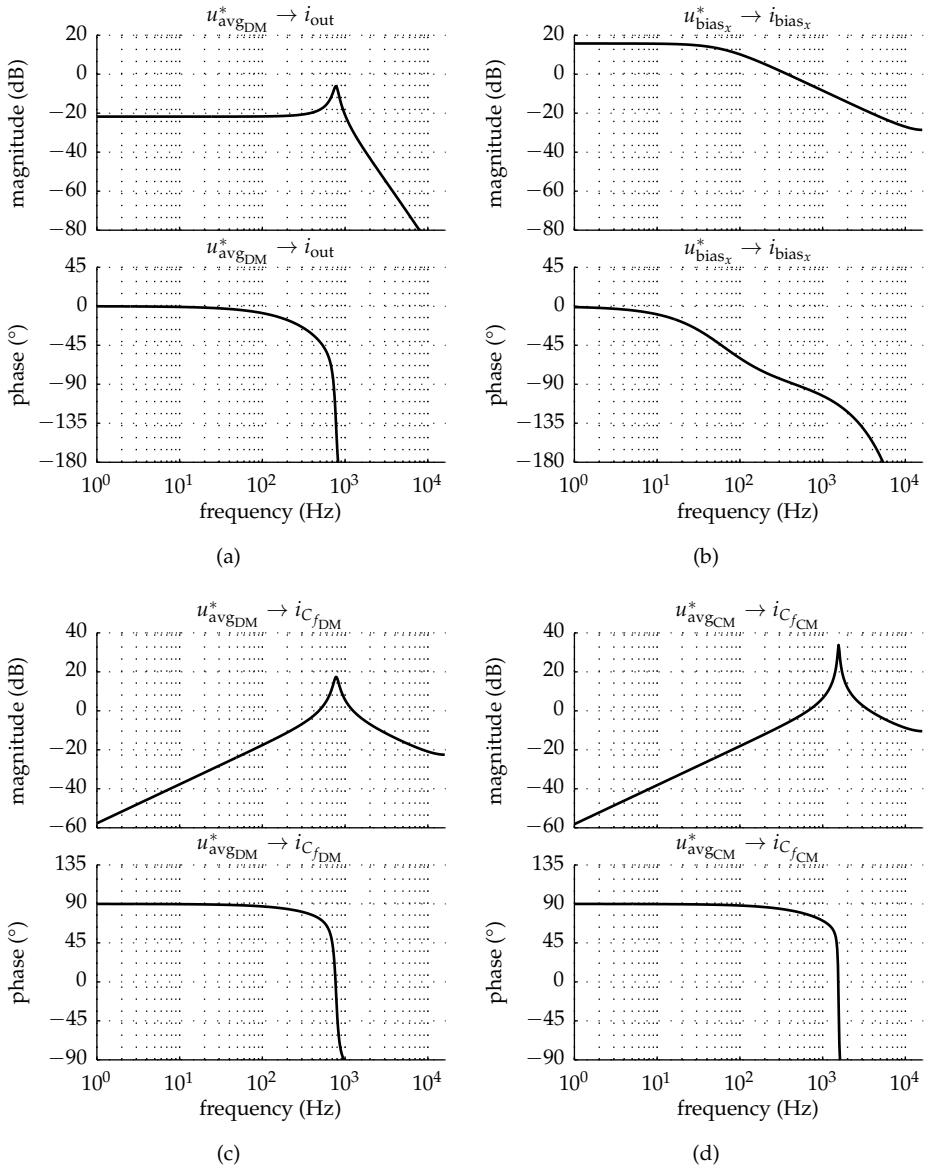


Figure 8.6: Bode diagrams of the open-loop decoupled transfer functions, from (a) $u^*_{\text{avg}_{\text{DM}}}$ to i_{out}, (b) $u^*_{\text{bias}_x}$ to i_{bias_x}, (c) $u^*_{\text{avg}_{\text{DM}}}$ to $i_{C_{f_{\text{DM}}}}$, and (d) $u^*_{\text{avg}_{\text{CM}}}$ to $iC_{f_{\text{CM}}}$.

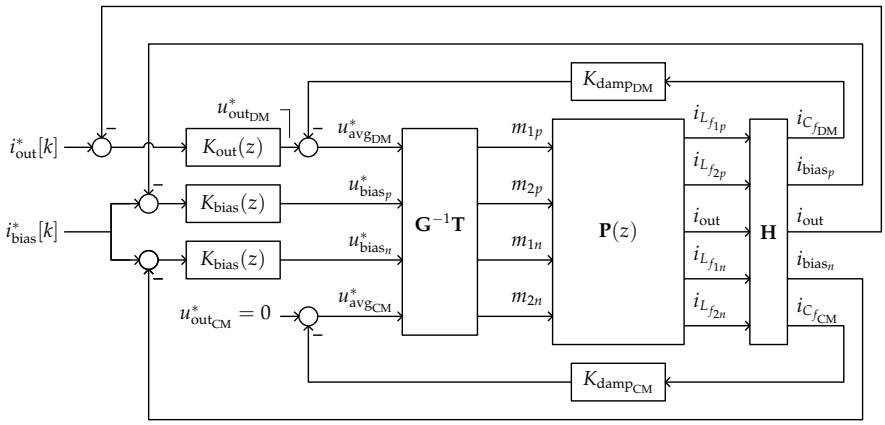


Figure 8.7: Block diagram for the proposed decoupled current control for the dual-buck converter.

8.3.1 Analytical verification of the decoupling

Analytical calculation of the decoupling on the discrete model given in (8.26) is challenging, since it involves computation of symbolic matrix exponentials. However, the decoupling can also be shown using the time-continuous model (8.13).

When neglecting ω_o, the transfer function matrix of the average model (8.13) becomes

$$\mathbf{P}'(s) = \frac{\mathbf{Y}'(s)}{\mathbf{U}'(s)} = \mathbf{HC}\left(s\mathbf{I} - \mathbf{A}\right)^{-1}\mathbf{BTG}^{-1} = \begin{pmatrix} \mathbf{G}'_{\text{out}} & \mathbf{0} \\ \mathbf{G}'_C & \mathbf{0} \\ \mathbf{0} & \mathbf{G}'_{\text{bias}} \end{pmatrix} \tag{8.28}$$

with sub matrices

$$\mathbf{G}'_{\text{out}} = G'_{\text{out}} \begin{pmatrix} 1 & 0 \end{pmatrix} \tag{8.29}$$

$$\mathbf{G}'_C = \begin{pmatrix} G'_{C_{\text{DM}}} & 0 \\ 0 & G'_{C_{\text{CM}}} \end{pmatrix} \tag{8.30}$$

$$\mathbf{G}'_{\text{bias}} = G'_{\text{bias}} \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \tag{8.31}$$

where $\mathbf{G}'_{\text{out}}$ and $\mathbf{G}'_C$ are the transfer functions from $u^*_{\text{avg}_x}$ to i_{out}, and $i_{C_{fx}}$ respectively, and where $\mathbf{G}'_{\text{bias}}$ is the transfer function from $u^*_{\text{bias}_x}$ to i_{bias_x}.

From (8.28) to (8.31) it can be seen that there is no coupling between $\mathbf{G}'_{\text{out}}$ and $\mathbf{G}'_{\text{bias}}$, and the individual elements of $\mathbf{G}'_{\text{bias}}$. Since the system $\mathbf{P}'$ is decoupled, separate SISO controllers can be applied to control i_{out} and i_{bias_x} independently.

When assuming ideal switching devices and diodes the transfer functions, G'_{out}, $G'_{C_{\text{DM}}}$, $G'_{C_{\text{CM}}}$, and G'_{bias} become

$$G'_{\text{out}} = \frac{1}{aLL_f s^3 + abs^2 + \left(L + L_f + aRR_{L_f}\right) s + R + R_{L_f}} \tag{8.32}$$

$$G'_{C_{\text{DM}}} = \frac{aLs^2 + aRs}{aLL_f s^3 + abs^2 + \left(L + L_f + aRR_{L_f}\right) s + R + R_{L_f}} \tag{8.33}$$

with

$$a = \left(C_{f_{\text{DM}}} + \tfrac{1}{2}C_f\right) \tag{8.34a}$$

$$b = \left(L_f R + LR_{L_f}\right) \tag{8.34b}$$

and

$$G'_{C_{\text{CM}}} = \frac{2C_f s}{\frac{1}{2}C_f L_f s^2 + \frac{1}{2}C_f R_{L_f} s + 1} \tag{8.35}$$

$$G'_{\text{bias}} = \frac{1}{2\left(L_f s + R_{L_f}\right)}. \tag{8.36}$$

The DM voltage related transfer functions (8.32) and (8.33) are of third order and depend on the load resistance and inductance (R & L). The transfer function (8.35) is second order, and, as pointed out earlier in this section, does not depend on the load. Moreover, the bias current transfer function (8.36) is first order and does not depend on the load and the filter capacitors, making bias current control straightforward. From here on the discretized model given in (8.26) will be used.

8.3.2 Applying damping by feedback

Figures 8.6c and 8.6d show the resonances that occur due to the output filters. To damp those resonances, in our simulation experiments the DM and CM capacitor currents are fed back to the corresponding input through K_{damp_x}, as depicted in Figure 8.7.

When $K_{\text{damp}_{\text{DM}}}$ and $K_{\text{damp}_{\text{CM}}}$ are proportional gains, their units are Ω and they

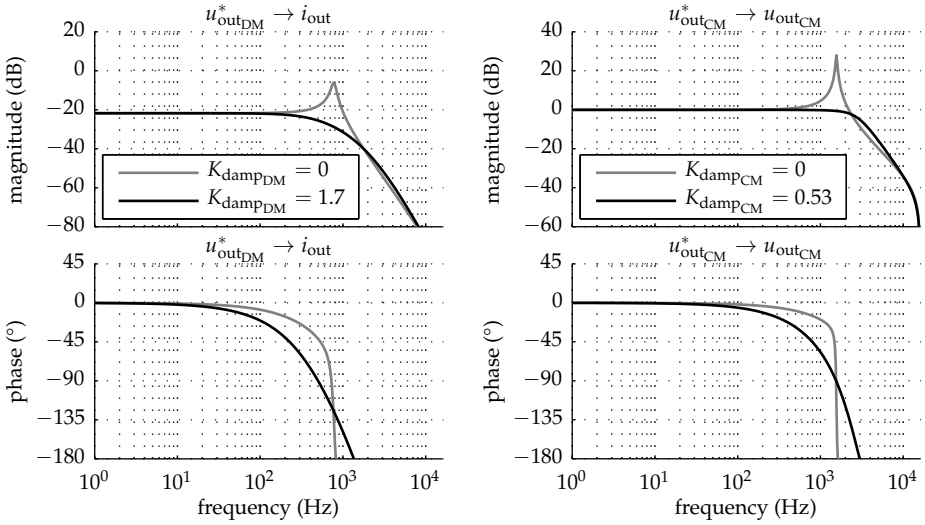


Figure 8.8: Bode diagrams of the DM (a) and CM (b) damping feedback loops, without (gray) and with (black) feedback, and where $u_{\text{out}_{\text{CM}}} = \frac{1}{2}(u_{C_{fp}} + u_{C_{fn}})$.

can, therefore, be regarded as virtual damping resistances. The damping gains are chosen such that the dominant poles have the highest damping ratio ζ. In this particular case $K_{\text{damp}_{\text{DM}}} = 1.7$, resulting in $\zeta = 1$, and $K_{\text{damp}_{\text{CM}}} = 0.53$, resulting in $\zeta = 0.57$. The Bode diagrams of the resulting systems are depicted in Figure 8.8. It shows that the resonances are indeed damped by the virtual resistance that is added through K_{damp_x}.

Proportional feedback of i_{sum_x} can also be applied to damp the system. However, that leads to a lower output impedance after feedback of i_{out} because the filter inductors also carry current that is flowing to the output. Addition of a high-pass filter in the damping loop can increase the output impedance for both damping methods, if desired.

After closing the damping loops the decoupled input and output vectors become

$$\mathbf{u}' = \begin{pmatrix} u^*_{\text{out}_{\text{DM}}} & u^*_{\text{bias}_p} & u^*_{\text{bias}_n} \end{pmatrix}^\mathsf{T} \tag{8.37}$$

$$\mathbf{y}' = \begin{pmatrix} i_{\text{out}} & i_{\text{bias}_p} & i_{\text{bias}_n} \end{pmatrix}^\mathsf{T} \tag{8.38}$$

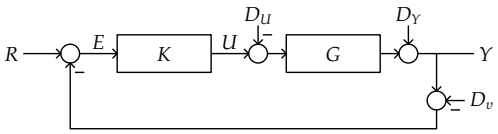


Figure 8.9: Block diagram for the output and bias current control loops of the dual-buck converter.

with

$$\mathbf{P}'_D(z) = \begin{pmatrix} G'_{\text{out}_D} & 0 & 0 \\ 0 & G'_{\text{bias}} & 0 \\ 0 & 0 & G'_{\text{bias}} \end{pmatrix}. \tag{8.39}$$

From (8.29) it can be seen that $u^*_{\text{avg}_{\text{CM}}}$ is not coupled with the output and is, therefore, chosen such that the output voltage range of the proposed control scheme is maximum, that is, $u^*_{\text{avg}_{\text{CM}}} = 0\,\text{V}$.

8.3.3 Output and bias current control

The output- and bias current control loops are illustrated in Figure 8.7. The two distinct control loops that need to be designed have the shape depicted in Figure 8.9, where K is the (discrete) controller and G represents the corresponding (discretized) transfer function of the plant.

The useful transfer functions that can be deduced from Figure 8.9 are given by

$$T = \frac{Y}{R} = \frac{GK}{1+GK} = \frac{\text{num}(GK)}{\text{den}(GK)+\text{num}(GK)} \tag{8.40a}$$

$$S_K = \frac{U}{R} = \frac{K}{1+GK} = \frac{\text{num}(K)\text{den}(G)}{\text{den}(GK)+\text{num}(GK)} \tag{8.40b}$$

$$S = \frac{Y}{D_Y} = \frac{E}{R} = \frac{E}{D_v} = \frac{1}{1+GK} = \frac{\text{den}(GK)}{\text{den}(GK)+\text{num}(GK)} \tag{8.40c}$$

$$S_G = \frac{E}{D_u} = \frac{G}{1+GK} = \frac{\text{den}(K)\text{num}(G)}{\text{den}(GK)+\text{num}(GK)} \tag{8.40d}$$

where K represents the controller, G the plant, and 'num' and 'den' denote the numerator and denominator of the corresponding transfer function, respectively.

Equation (8.40a) is the transfer function from input R to output Y and is known as the complementary sensitivity T. The transfer function from D_Y to Y (8.40c) is known as the output sensitivity S of the closed-loop system, which is a measure of the amount of rejection to a disturbance at the output. The complementary

sensitivity and output sensitivity are related as $S = 1 - T$.

The control sensitivity S_K is a measure of the effort that is required to track an input signal and is given by (8.40b), and (8.40d) is the process sensitivity S_G which is a measure for the sensitivity to disturbances on the input of the plant G.

Furthermore, it should be noted that the transfer function from D_v (sensor noise) to the output Y is equal to T, which implies that it is not possible to have both good tracking of the reference and, at the same time, good rejection of sensor noise at a given frequency [100, page 44].

From (8.40c) it can be seen that the error becomes zero when K or G contains the poles of the Laplace transform of the dynamics that need to be tracked or rejected. This is known at the internal model principle [12, page 310]. However, for disturbances on the input of the plant (D_U) the dynamics should always be in the controller K, since the plant poles are not present in the numerator of process sensitivity (8.40d).

In this chapter the aim is to track a ramping signal for i^*_{out} with zero error, because ramping reference signals are commonly used in both motion and MRI systems. Tracking of a ramp with zero error requires for $G'_{\text{out}_D} K_{\text{out}}$ to have at least two poles at 1 in the z-plane. The bias control is less critical, thus an arbitrarily small constant error for a ramping signal is sufficient. Furthermore, the constant disturbance $\boldsymbol{\omega}'_o$ needs to be compensated. As a result only a single pole at 1 in the z-plane is sufficient for $K_{\text{bias}} G'_{\text{bias}}$ [77, chapter 10]. Since both G'_{out_D} and $G'_{\text{bias}} K_{\text{bias}}$ have no poles that match the desired dynamics, the following controller structures are used:

$$K_{\text{out}}(z) = K_o \frac{(z - b_{o1})(z - b_{o2})}{(z-1)^2} \tag{8.41a}$$

$$K_{\text{bias}}(z) = K_b \frac{z - b_b}{z - 1} \tag{8.41b}$$

where the pole locations are fixed according to the dynamics that need to be tracked and disturbances that need to be rejected. The parameters K_o, b_{o1}, b_{o2}, K_b, b_{b1}, need to be chosen such that the closed-loop system is stable and has the desired dynamic response.

Loop-shaping the controllers

A fast and simple procedure for determining the parameters in (8.41) is based on the Bode diagram of the open-loop transfer functions [100, page 44]. Such a loop-

shaped controller is a good initial design for further optimization. First the zero locations (b_{o1}, b_{o2}) and the gain K_o are determined. The time constants of both zeros are chosen the same and such that the maximum phase is $-135°$. After that, the gain K_o is adjusted such that the open-loop Bode magnitude $K_{\text{out}}G'_{\text{out}_D}$ crosses zero dB at the frequency where the phase is maximum, as shown in Figure 8.10a. Of course, when desired, less phase margin can be allowed. In this example 45° is used, resulting in

$$K_{\text{out}}(z) = 10.5\frac{(z-0.954)^2}{(z-1)^2}. \tag{8.42}$$

The obtained closed-loop Bode diagrams of the sensitivity and complementary sensitivity are depicted in Figure 8.10b, where

$$S_{\text{out}} = \frac{1}{1+G'_{\text{out}_D}K_{\text{out}}} \tag{8.43a}$$

$$T_{\text{out}} = \frac{G'_{\text{out}_D}K_{\text{out}}}{1+G'_{\text{out}_D}K_{\text{out}}}. \tag{8.43b}$$

The magnitude of the complementary sensitivity $|T_{\text{out}}|$ has a maximum peaking of 3.5 dB, and the open-loop magnitude $|K_{\text{out}}G'_{\text{out}_D}|$ crosses 0 dB at 330 Hz. The corresponding rejection of disturbances at the output is shown in the sensitivity magnitude plot $|S_{\text{out}}|$. The phase of S_{out} is omitted intentionally for clarity.

The resulting magnitude of the output impedance $|Z_{\text{out}}|$ is shown in Figure 8.10a and is determined by evaluating the transfer function from a disturbance voltage source in series with the load to i_{out}. When neglecting the input delay of $G'_{\text{out}_D}(z)$, if present, the output impedance becomes

$$Z_{\text{out}} = \frac{1+G'_{\text{out}_D}K_{\text{out}}}{G'_{\text{out}_D}}. \tag{8.44}$$

From (8.44) it can be observed that the output impedance is determined by K_{out} for low frequencies where the controller is dominant. However, for higher frequencies, where $|G'_{\text{out}_D}K_{\text{out}}|$ is significantly smaller than one, the Z_{out} becomes approximately equal to $(G'_{\text{out}_D})^{-1}$.

Finally, the bias controllers K_{bias} should be tuned. The time constant of the zero in K_{bias} is chosen such that a phase lag of $-135°$ occurs at the highest frequency. This is done by moving the zero from an arbitrarily high frequency back to lower frequencies until this desired phase margin is reached. After that the gain is adjusted such that the open-loop Bode magnitude $|K_{\text{bias}}G'_{\text{bias}}|$ crosses zero dB at the

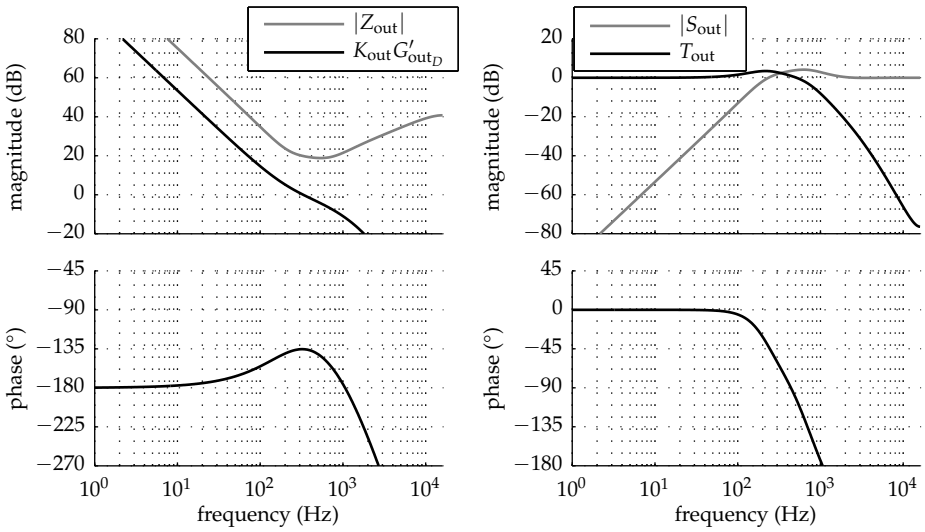


Figure 8.10: Bode diagrams of (a) the open-loop transfer function $K_{\text{out}}G'_{\text{out}_D}$ with the resulting closed-loop output impedance Z_{out}, and (b) the closed-loop system T_{out}, with sensitivity to disturbances at the output S_{out}.

frequency where the phase margin is 45°. The resulting controller is found to be

$$K_{\text{bias}}(z) = 3\frac{z - 0.8819}{z - 1}. \tag{8.45}$$

Figure 8.11 shows the resulting open-loop ($K_{\text{bias}}G'_{\text{bias}}$), and closed-loop ($T_{\text{bias}}$ & S_{bias}) Bode diagrams. The bandwidth where $|K_{\text{bias}}G'_{\text{bias}}|$ crosses 0 dB is limited by the input delay, in this case one control cycle. The resulting bandwidth is 1212 Hz, as can be seen in Figure 8.11a. That is well above the bandwidth of the output current loop.

The bandwidth of the bias current controllers is not critical when the bias currents are kept constant, as in (4.20). However, for modulated bias currents, as given in (4.21), the bias controller needs to track the absolute value of the fundamental output frequency, which requires at least two times the amount of bandwidth as the output current controller. In this case the bandwidth of the bias current controllers needs to be more than two times larger than that of the output current controller.

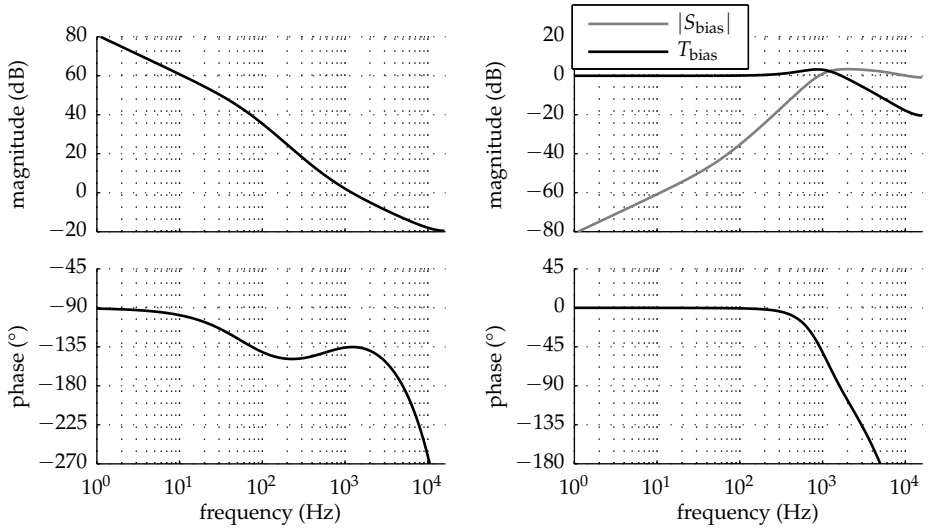


Figure 8.11: Bode diagrams of (a) the open-loop systems $K_{\text{bias}}G'_{\text{bias}}$, and (b) the closed-loop system T_{bias}, with the corresponding sensitivity S_{bias}.

8.3.4 Optimization of control parameters

The controllers in the previous section were designed in a conservative way, without any constraints on bandwidth, gain flatness, phase delay, and output impedance. Finding control parameters that satisfy constraints can be a cumbersome job, especially for higher-order systems. Moreover, in most cases constraints, read specifications, do not result in a unique set of control parameters. In such cases a performance criterion that can be minimized is useful to determine the best controller from the feasible set. The resulting minimization problem can be formulated as [11, chapter 1]

$$\min_{\boldsymbol{\lambda}} g(\boldsymbol{\lambda}) \text{ subject to } \begin{cases} c(\boldsymbol{\lambda}) \leq \mathbf{0} \\ \check{\boldsymbol{\lambda}} \leq \boldsymbol{\lambda} \leq \hat{\boldsymbol{\lambda}} \end{cases} \tag{8.46}$$

where c is the constraints function containing the specifications that must be met, and $\check{\boldsymbol{\lambda}}$ and $\hat{\boldsymbol{\lambda}}$ are the lower and upper bounds on the parameters that need to be found.

Many criteria exist for optimization of controllers [77, chapter 8]. In this section the integral of the squared error exponential weighted over time is used because it puts higher penalties on larger errors, and is exponentially weighted with time,

to put an additional penalty on errors that occur later in the response, to prevent large settling time. Otherwise stated,

$$g(\boldsymbol{\lambda}) = \frac{1}{T}\int_0^T e^{\tau^{-1}t} e_{\text{out}}^2(t,\boldsymbol{\lambda})\mathrm{d}t \tag{8.47}$$

where $e_{\text{out}} = i_{\text{out}} - i_{\text{out}}^*$, which in turn depends on $\boldsymbol{\lambda}$, τ sets the settling time of the step response, and T is the integration interval. In this particular case the output current tracking error is used to evaluate g, however, also the error as a result of disturbance can be used if desired.

A performance index g can also include penalties on state variables and control effort, however, bounds on those can also be included in the constraints. From the set of controllers that satisfy the constraints the one with the lowest g is chosen. The control of the bias current and the CM damping are less critical and are, therefore, not further optimized.

The excitation signal used to determine the performance index should be selected carefully. The excitation signal can for instance be the worst-case expected waveform, a ramp, or a step. For the optimization of the output current controller the response to a unit step on the reference is used, because a step excites the high-frequency dynamics more than a ramp. The integration interval T is chosen equal to $100L/R$, and τ^{-1} was chosen 500 Hz. When the power amplifier is part of a digital (servo) control loop that runs on a lower frequency, that control loop sample time can be used for T too.

Constraints are put on the sensitivity and bandwidth, and are given by

$$c(\boldsymbol{\lambda}) = \max\begin{bmatrix} -\text{BW}(K_{\text{out}}(\omega,\boldsymbol{\lambda})G'_{\text{out}_D}(\omega)) + \text{BW}(K_{\text{out}}(\omega,\boldsymbol{\lambda}_0)G'_{\text{out}_D}(\omega)) \\ \max\left(|S_{\text{out}}(\omega,\boldsymbol{\lambda})| - |S_{\text{out}}(\omega,\boldsymbol{\lambda}_0)|\right) \end{bmatrix} \tag{8.48}$$

where BW $(X(\omega))$ is the bandwidth of system $X(\omega)$, which is defined as the frequency where $|X(\omega)|$ crosses 0 dB, S_{out} is the sensitivity of the closed-loop system, and max is the maximum value. The bandwidth after optimization should be larger than the initial bandwidth, and the magnitude of the sensitivity S_{out} for frequencies ω should be smaller than the initial sensitivity at those frequencies. The frequency interval is chosen 1 to 200 Hz, which is within the bandwidth of the controller.

The frequency interval for the chosen constraint on the sensitivity should be limited. This is due to the Bode sensitivity integral [100, page 176], which states that when the sensitivity is lowered at some frequencies it goes up at other frequen-

cies. This procedure basically results in a final controller with smaller or equal g, equal or higher bandwidth, and equal or less sensitivity within the chosen frequency interval.

The K_{out} is assigned such that complex zeros are not excluded as a possible solution to the optimization problem, and is given by

$$K_{\text{out}}(z, \boldsymbol{\lambda}) = K_o \frac{\left(z - c_o + \sqrt{\text{sgn}\,(d_o)}|d_o|\right)\left(z - c_o - \sqrt{\text{sgn}\,(d_o)}|d_o|\right)}{(z-1)^2} \tag{8.49}$$

where a negative d_o results in complex conjugated zeros and positive d_o results in real zeros centered around c_o.

All together, the vector $\boldsymbol{\lambda}$ for optimization is found to become

$$\boldsymbol{\lambda} = \begin{pmatrix} K_d & K_o & c_o & d_o \end{pmatrix}^{\mathsf{T}}. \tag{8.50}$$

To help the algorithm to reach convergence, the following bounds are added to the optimization problem

$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ -1 \end{pmatrix} \leq \boldsymbol{\lambda} \leq \begin{pmatrix} 20 \\ 20 \\ 1 \\ 1 \end{pmatrix}. \tag{8.51}$$

The upper bounds on the gains K_x are set to 20 based on observations during the loop-shaping procedure, plus a robust margin added. The locations of the zeros of the output current controller are limited to a rectangular area, which includes the right half of the stable region of the z-plane. To prevent unstable systems as a optimization result, g, in (8.47), is made infinite when the resulting system is unstable.

The optimal control parameters $\boldsymbol{\lambda}$ are found using the *pattern search* algorithm of MATLAB as described in [4]. Pattern-search numerical optimization algorithms do not require information about the gradient of the performance index. Pattern search searches a set of points around the current point to determine were the performance index is lower than in the current point and stops when a specified tolerance is reached. There is of course no guarantee that the obtained solution is the global minimum of the optimization problem.

The user-defined initial conditions were chosen equal to those of the loop-shaped

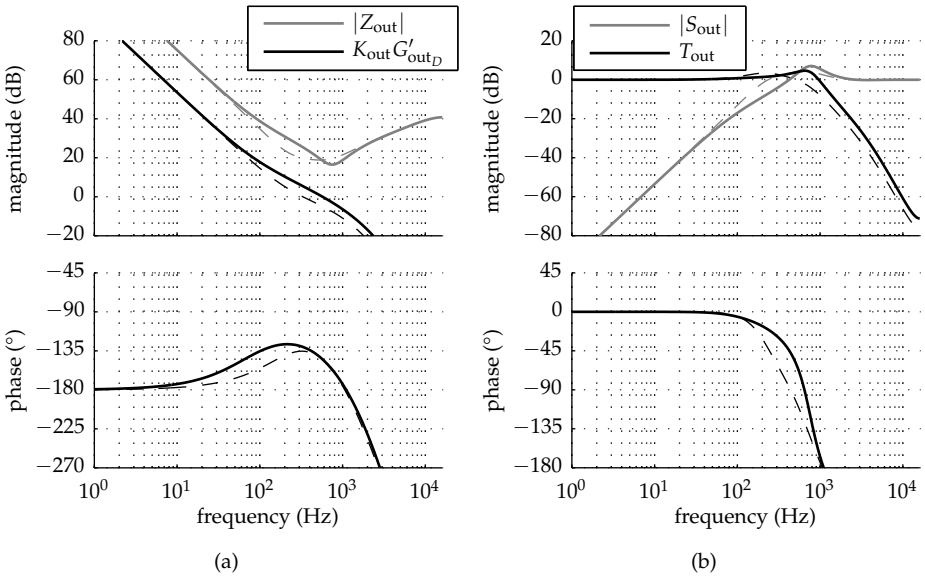


Figure 8.12: Bode diagrams of the open-loop system $K_{\text{out}}G'_{\text{out}_D}$ with the resulting closed-loop output impedance Z_{out} (a), and T_{out} and S_{out} (b) after (solid) and before (dashed) optimization.

controller. The optimization resulted in

$$K_{\text{damp}_{\text{DM}}} = 1.9559 \tag{8.52a}$$

$$K_{\text{out}}(z) = 20\frac{(z-0.9852)\,(z-0.9247)}{(z-1)^2} \tag{8.52b}$$

where $K_{\text{damp}_{\text{DM}}}$ is higher than for the loop-shaped controller. The gain of K_{out} is increased significantly to compensate for the damping and the zeros are shifted slightly apart, resulting in a sharper phase transition.

After optimization the open-loop system $K_{\text{out}}G'_{\text{out}_D}$ has a significantly higher bandwidth, 569 Hz compared to 330 Hz of the loop-shaped controller, and a better sensitivity within the bandwidth of the system, as can be seen from Figure 8.12. The sensitivity is increased for frequencies higher than the bandwidth, as can be expected from the Bode sensitivity integral [100, page 176].

8.3.5 Robustness of the closed-loop system

In practice components differ from nominal values. To ensure stability of a perturbed closed-loop system, a safety margin is added. A rule of thumb is to add at least 30 to 40° phase and 6 to 8 dB gain margin to the open-loop system [77].

A Monte Carlo experiment was performed to determine the impact of parameter variations on the closed-loop system. Each Monte Carlo analysis involved 1764 calculations of the discrete plant. For each iteration the parameters were pseudo-randomly chosen from a uniform distribution. Two cases of parameter variation were compared. Table 8.1 shows the used component values and the corresponding parameter deviations. The nominal component values are the same as the ones in the experimental set-up described in Chapter 9.

The variation on the supply voltage and filter components is assumed 5 and 10 %, respectively. Furthermore, to include the strong effect of temperature, semiconductor device parameter deviations are allowed in the range of 25 and 50 %, respectively. To include both moderate and large load variations, 10 and 25 % are used for R and L respectively. Also the operating point is varied by randomly assigning the modulation indices (M_x) on the interval $[-1 \ldots 1]$. The currents of the inductors that are indexed 1 and 2 are assigned between i_{th} and $\hat{i}_{\text{out}} + i_{\text{th}}$, and $-i_{\text{th}}$ and $-\hat{i}_{\text{out}} - i_{\text{th}}$, respectively, as illustrated in Figure 4.4.

Figure 8.13 shows the expected deviations of the Bode magnitude and phase due to the component variations given in Table 8.1. The feedback attenuates the influence of the parameter variations for frequencies where the sensitivity to the disturbances is sufficiently low. Especially the bias current shows little influence of the component variation.

The proposed decoupling is also affected by component variation, as illustrated in Figure 8.14a. The unwanted coupling between $u^*_{\text{bias}_x}$ and i_{out} is shown in the top graph of Figure 8.14a, and is worst-case -38 dB for *case 1* and -31 dB for *case 2*, respectively. The bottom graph shows the maximum coupling between $u^*_{\text{avg}_{\text{DM}}}$ and i_{bias}, which is slightly higher but less critical, since i_{bias} is only required to prevent DCM. The decoupling is most sensitive to a mismatch between the filter inductors, as already pointed out in Chapter 6.

From Figure 8.14b it can be seen that the applied feedback improves the decoupling. However, for frequencies where the open-loop gain is lower than 10 dB the cross coupling from i^*_{bias} to i_{out} becomes significant. This suggests that for high-precision applications it is better not to excite $u^*_{\text{bias}_x}$ at those frequencies. The cross coupling from i^*_{out} to i_{bias_x} can become close to zero dB. The bias current is

Table 8.1: Component values and variation used for Monte Carlo analysis.

Item	Nominal value		Variation (%)	
			case 1	*case 2*
U_{DC}	100	V	5	10
$\hat{i}_{\mathrm{out}}$	7.5	A		
L	1.7	mH	10	25
R	12.1	Ω	10	25
L_f	208	µH	5	10
R_{L_f}	50	mΩ	5	10
C_f	100	µF	5	10
$C_{f_{\mathrm{DM}}}$	160	µF	5	10
V_{on}	1.7	V	25	50
V_f	1.2	V	25	50
R_{on}	40	mΩ	25	50
R_f	22	mΩ	25	50

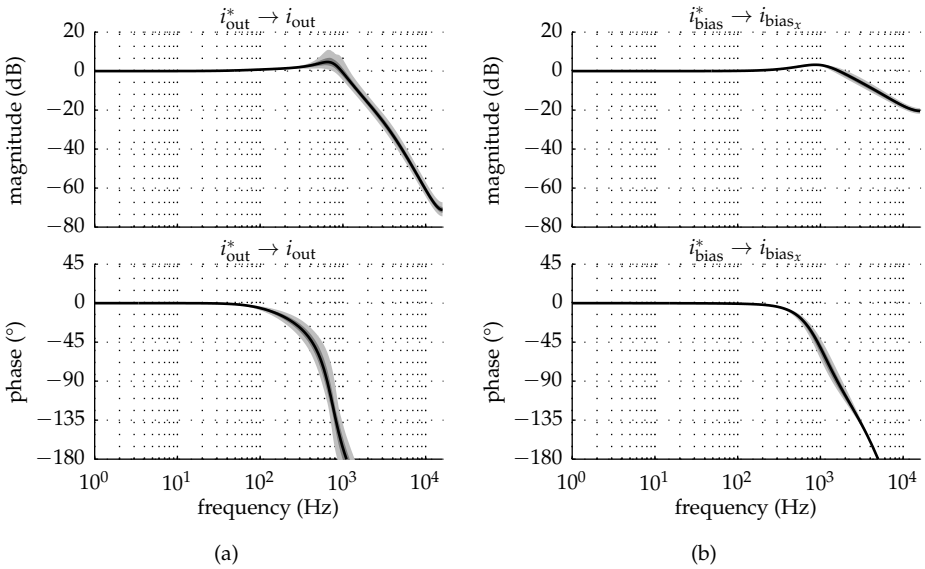


Figure 8.13: Bode diagrams illustrating the influence of component variation on, T_{out} (a), and T_{bias} (b) for *case 1* (gray) and *case 2* (light gray). The intended magnitudes and phases are indicated with black lines.

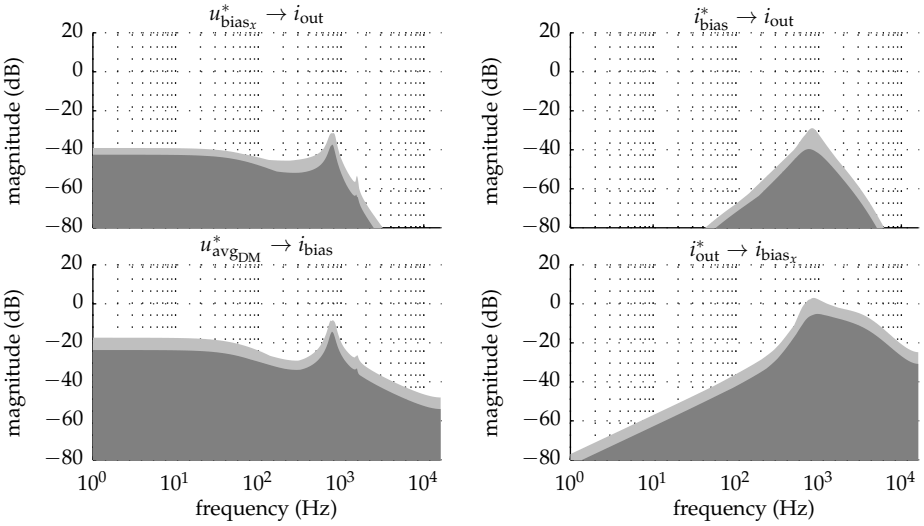


Figure 8.14: Bode magnitude diagrams illustrating the influence of component variation on the cross coupling between inputs and outputs of the (a) open-loop plant ($\mathbf{P}'(s)$), and (b) closed-loop optimized system, for *case 1* (gray) and *case 2* (light gray).

not critical, however, a higher offset (i_{th}) might be required for the bias current to compensate for the cross coupling at those frequencies.

Figure 8.15 illustrates the variation that can be expected on the step responses for both cases of component variation investigated in this section. The output current step responses, depicted in Figure 8.15a, are well damped for all experiments and do not show significant oscillations, which suggests that the performance criterion is sufficient to guarantee acceptable settling behavior. The step response of the loop-shaped controller is depicted with a dashed line for reference. The bias current step response, depicted in Figure 8.15b, shows almost no influence of the component variation.

8.4 A full-state-feedback approach

Full-state feedback is often associated with optimal control, which was developed in the early 1960's [42] to cope with nonlinear MIMO systems. Since its introduction, state-feedback has been applied in switching converters, however examples

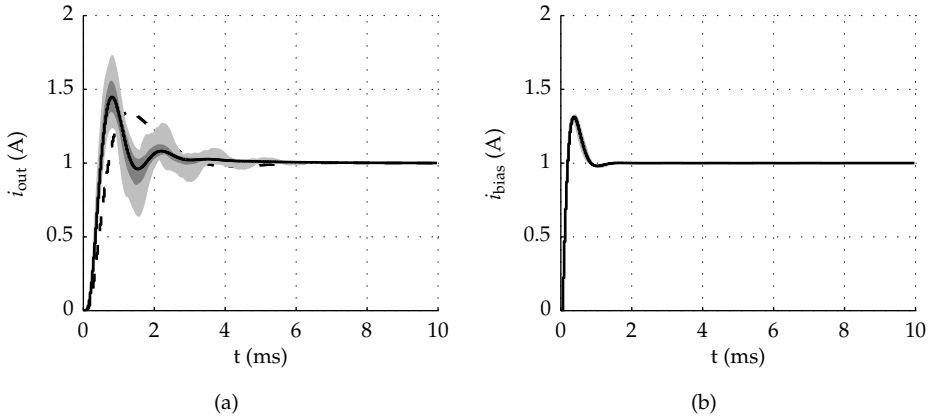


Figure 8.15: The influence of component variation on the step response of T_{out} (a) and T_{bias} (b), for *case 1* (gray) and *case 2* (light gray). The solid and black lines represent the intended step responses after optimization. The dashed line in (a) represents the step response before optimization.

are few. More recently, due to the availability of low-cost micro-controllers and FPGAs, in power electronics, state feedback is getting renewed attention.

Figure 8.16 illustrates a basic full-state-feedback diagram, where **P** is the plant, and $\mathbf{K}_p$ is the feedback matrix. Full state feedback requires the complete state vector. In many cases the state vector is only partly available, because some state dynamics are not measurable, or not explicitly measured for cost reasons. In that case the state vector needs to be estimated using an observer **O**, which produces an estimate of the state vector ($\hat{\mathbf{x}}$) based on the plant input (**u**) and output (**y**).

In case of observer feedback, as depicted in Figure 8.16, the design procedure is split in two stages. First a state feedback design is made, assuming availability of the full state vector. Second, a state observer is designed to obtain the full state vector from the plant's inputs and outputs. The state feedback and observer can be designed independently. When used together in observer feedback the poles of the total system contain the poles of the plant and the poles of the observer. This is known as the separation principle [12, page 43]. For observer feedback the plant **P** must be observable [12, page 34] and stabilizable, that is, all uncontrollable modes have stable dynamics.

The discretized plant **P**, shown in Figure 8.16, represents the full-bridge equivalent DB. A discretized model of the DB was already shown in Section 8.2. The DB

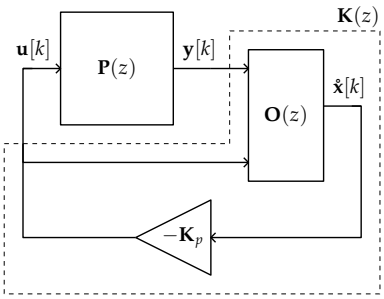


Figure 8.16: Schematic diagram of the full state-feedback control with a state estimator (observer). The state vector $\hat{\mathbf{x}}$ is estimated from the inputs $\mathbf{u}$ and outputs $\mathbf{y}$ of the plant $\mathbf{P}(z)$ by a state observer $\mathbf{O}(z)$.

model of 8.16 is repeated here for convenience:

$$\mathbf{x}[k+1] = \mathbf{\Phi}\mathbf{x}[k] + \mathbf{\Gamma}\mathbf{u}[k] + \mathbf{\Gamma}_\omega \boldsymbol{\omega}_o \tag{8.53a}$$

$$\mathbf{y}[k+1] = \mathbf{C}\mathbf{x}[k]. \tag{8.53b}$$

The poles, or eigenvalues, of the discretized model are given by the characteristic polynomial, $\det(s\mathbf{I} - \mathbf{\Phi})$, where $\det(\cdot)$ is the determinant of a matrix. When the pair $\mathbf{\Phi}$ and $\mathbf{\Gamma}$ is controllable the open-loop poles can be moved to any location by applying full state feedback, given by

$$\mathbf{u}[k] = -\mathbf{K}_p \mathbf{x}[k] \tag{8.54}$$

where $\mathbf{K}_p$ is the feedback matrix.

With state feedback the closed-loop discrete state-space representation becomes

$$\mathbf{x}[k+1] = \left(\mathbf{\Phi} - \mathbf{\Gamma}\mathbf{K}_p\right)\mathbf{x}[k] + \mathbf{\Gamma}_\omega \boldsymbol{\omega}_o \tag{8.55a}$$

$$\mathbf{y}[k+1] = \mathbf{C}\mathbf{x}[k]. \tag{8.55b}$$

The closed-loop characteristic polynomial is given by $\det\left(s\mathbf{I} - \mathbf{\Phi} + \mathbf{\Gamma}\mathbf{K}_p\right)$, which has real or complex conjugate roots for real valued $\mathbf{\Phi}$, $\mathbf{\Gamma}$, and $\mathbf{K}_p$. From (8.55) it can be seen that, when disregarding $\boldsymbol{\omega}_o$, the state feedback drives the states to zero when the absolute values of the eigenvalues of $\mathbf{\Phi} - \mathbf{\Gamma}\mathbf{K}_p$ are smaller than one. The state feedback law given in (8.54) has no reference input and is, therefore, not a tracking system.

Steady-state reference tracking can be achieved by applying a coordinate transla-

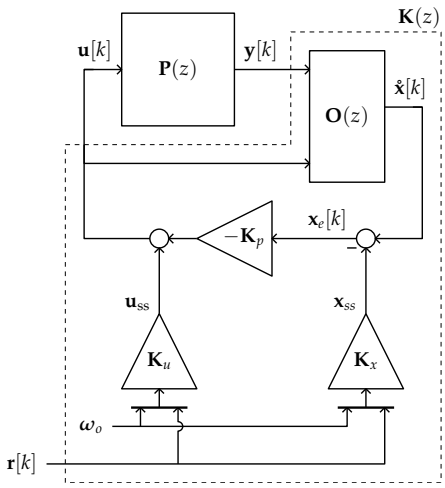


Figure 8.17: Schematic diagram of the full-state-feedback controller of Figure 8.16, with reference tracking by a combination of state-error feedback and feedforward control. The black bars represent vector a concatenation.

tion, resulting in the following control law

$$\mathbf{u}[k] = -\mathbf{K}_p \left(\mathbf{x}[k] - \mathbf{x}_{\text{ss}}[k]\right) + \mathbf{u}_{\text{ss}}[k] \tag{8.56}$$

where $\mathbf{x}_{\text{ss}}$, is the desired steady-state state, and $\mathbf{u}_{\text{ss}}$ represents the required steady-state input, respectively. Instead of the state of the plant, the state error $\mathbf{x}_e = \mathbf{x} - \mathbf{x}_{\text{ss}}$ is fed back. When the state of the plant ($\mathbf{x}$) becomes equal to the desired state ($\mathbf{x}_{\text{ss}}$) the state error and consequently the plant input ($\mathbf{u}$) becomes zero. Zero tracking error can, therefore, only be achieved when $\mathbf{x}_{\text{ss}}$ belongs to the zero-input dynamics of $\mathbf{P}$, or when the corresponding input is fed forward through $\mathbf{u}_{\text{ss}}$.

The steady-state desired input and state vector can be expressed in terms of the reference $\mathbf{r}$ and disturbance inputs $\boldsymbol{\omega}_o$ as

$$\mathbf{u}[k] = -\mathbf{K}_p \left(\mathbf{x}[k] - \mathbf{K}_x \begin{pmatrix} \boldsymbol{\omega}_o \\ \mathbf{r}[k] \end{pmatrix} \right) + \mathbf{K}_u \begin{pmatrix} \boldsymbol{\omega}_o \\ \mathbf{r}[k] \end{pmatrix} \tag{8.57}$$

where $\mathbf{K}_x$ and $\mathbf{K}_u$ are the matrices that determine the $\mathbf{u}_{\text{ss}}$ and $\mathbf{x}_{\text{ss}}$ from the disturbance and reference inputs.

Figure 8.17 depicts the resulting state-error feedback scheme, where the desired steady-state inputs ($\mathbf{u}_{\text{ss}}$) are fed forward to the plant, and the desired steady-state state vector ($\mathbf{x}_{\text{ss}}$) is subtracted from the state of the plant. The state-space

representation of the state error feedback can be determined by combining (8.57) with (8.53), resulting in

$$\mathbf{x}[k+1] = \left(\mathbf{\Phi} - \mathbf{\Gamma}\mathbf{K}_p\right)\mathbf{x}[k] + \mathbf{\Gamma}_t\mathbf{r}[k] + \mathbf{\Gamma}_\Omega\boldsymbol{\omega}_o \tag{8.58a}$$

$$\mathbf{y}[k] = \mathbf{C}\mathbf{x}[k] \tag{8.58b}$$

with

$$\mathbf{\Gamma}_t = \mathbf{\Gamma}\left(\mathbf{K}_{ru} + \mathbf{K}_p\mathbf{K}_{rx}\right) \tag{8.59a}$$

$$\mathbf{\Gamma}_\Omega = \mathbf{\Gamma}\left(\mathbf{K}_{\omega u} + \mathbf{K}_p\mathbf{K}_{\omega x}\right) + \mathbf{\Gamma}_\omega \tag{8.59b}$$

and where $\mathbf{K}_x = \begin{pmatrix}\mathbf{K}_{\omega x} & \mathbf{K}_{rx}\end{pmatrix}$, and $\mathbf{K}_u = \begin{pmatrix}\mathbf{K}_{\omega u} & \mathbf{K}_{ru}\end{pmatrix}$.

From (8.58) it can be seen that the closed-loop poles are not affected by the added reference tracking. The state error and feedforward matrices can be determined as described in [37, page 342]. When assuming steady state and no tracking error, that is $\mathbf{x}[k] = \mathbf{x}_{\text{ss}}$, $\mathbf{u}[k] = \mathbf{u}_{\text{ss}}$, and $\mathbf{y}[k] = \mathbf{r}_{\text{ss}}$, (8.53) can be rewritten as

$$\mathbf{x}_{\text{ss}} = \mathbf{\Phi}^p\mathbf{x}_{\text{ss}} + \mathbf{\Gamma}^{p\times n}\mathbf{u}_{\text{ss}} + \mathbf{\Gamma}_\omega^{p\times l}\boldsymbol{\omega}_o \tag{8.60a}$$

$$\mathbf{r}_{\text{ss}} = \mathbf{C}_r^{k\times p}\mathbf{x}_{\text{ss}} \tag{8.60b}$$

where $\mathbf{C}_r$ translates the state vector to the outputs that need to be tracked, and the subscripts $[\cdot]_{\text{ss}}$ denote steady-state values. The superscripts of the matrices indicate their dimensions, where p represents the number of states, n the number of inputs, k the number of references and outputs, and l the number of constant disturbance inputs.

For the special case that the number of plant inputs and references are equal ($n = k$) and the system of equations is invertible, a unique solution for (8.60) exists, given by

$$\begin{pmatrix}\mathbf{x}_{\text{ss}}\\ \mathbf{u}_{\text{ss}}\end{pmatrix} = \begin{pmatrix}\mathbf{\Phi} & \mathbf{\Gamma}\\ \mathbf{C}_r & \mathbf{0}\end{pmatrix}^{-1}\begin{pmatrix}-\mathbf{\Gamma}_\omega & \mathbf{0}\\ \mathbf{0} & \mathbf{I}\end{pmatrix}\begin{pmatrix}\boldsymbol{\omega}_o\\ \mathbf{r}\end{pmatrix} = \begin{pmatrix}\mathbf{K}_{\omega x} & \mathbf{K}_{rx}\\ \mathbf{K}_{\omega u} & \mathbf{K}_{ru}\end{pmatrix}\begin{pmatrix}\boldsymbol{\omega}_o\\ \mathbf{r}\end{pmatrix}. \tag{8.61}$$

When the number of references is smaller than the number of inputs, that is $n \leq k$, and the columns of the matrix that needs to be inverted are linearly independent, a least-square solution exists given by the Moore-Penrose pseudo inverse. It should be noted that $\mathbf{K}_{ru}$ becomes zero when the transfer functions of all reference inputs to their corresponding outputs have at least one pole at $z = 1$.

For the controller designed in this section the number of references is chosen

equal to the number of inputs. The references are chosen as

$$\mathbf{r} = \begin{pmatrix} i^*_{\text{out}} & i^*_{\text{bias}_p} & i^*_{\text{bias}_n} & u^*_{\text{out}_{\text{CM}}} \end{pmatrix}^\mathsf{T} \tag{8.62}$$

which are the same references as for the decoupled SISO control treated in Section 8.3. The output current (i_{out}) is the main control objective, the bias current references ($i^*_{\text{bias}_p}$ & $i^*_{\text{bias}_n}$) are calculated based on (4.20) or (4.21). The reference input $u^*_{\text{out}_{\text{CM}}}$ is assigned equal to zero, as in the SISO case. For the references ($\mathbf{r}$) the output matrix becomes

$$\mathbf{C}_r = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{2} & -\frac{1}{2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2} & -\frac{1}{2} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 \end{pmatrix} \tag{8.63}$$

where the zeros in the last four columns correspond to the states of the input delay that is added to the discrete plant.

The combination of state error feedback and input feed-forward, depicted in Figure 8.17, results in zero steady-state tracking error. However, a tracking error occurs in the presence of model uncertainties, disturbances, or a dynamic reference signal. To obtain zero steady-state tracking error in the presence of model uncertainties, to track dynamic references, or suppress disturbances, the poles of the Laplace transforms of the references that need to be tracked, and disturbances that need to be suppressed, should be present in the corresponding open-loop transfer functions. This is known as the internal model principle [12, page 310].

8.4.1 Adding reference dynamics and disturbance rejection

Figure 8.18 shows the block diagram of the state error feedback with input feed-forward and reference/disturbance dynamics $\mathbf{R}[z]$. The state-space model of the reference dynamics is given by

$$\mathbf{x}_r[k+1] = \mathbf{\Phi}_r \mathbf{x}_r[k] + \mathbf{\Gamma}_r \mathbf{e}[k] \tag{8.64a}$$

$$\mathbf{y}_r[k] = \mathbf{x}_r[k] \tag{8.64b}$$

where $\mathbf{e}[k] = \mathbf{r}[k] - \mathbf{C}_r \mathbf{x}[k]$.

The transformed state vector of the plant $\mathbf{x}_e$ and the states of the reference vector $\mathbf{x}_r$ are combined into a single augmented state-vector $\mathbf{x}_a$, with $\mathbf{x}_a = \begin{pmatrix} \mathbf{x}_e & \mathbf{x}_r \end{pmatrix}^\mathsf{T}$.

The state-space representation of the resulting closed-loop system $\mathbf{T}(z)$ becomes

$$\mathbf{x}_a[k+1] = \left(\mathbf{\Phi}_a - \mathbf{\Gamma}_a\mathbf{K}_p\right)\mathbf{x}_a[k] + \begin{pmatrix}\mathbf{\Gamma}_t \\ \mathbf{\Gamma}_r\end{pmatrix}\mathbf{r}[k] + \begin{pmatrix}\mathbf{\Gamma}_\Omega \\ \mathbf{0}\end{pmatrix}\boldsymbol{\omega}_o \tag{8.65a}$$

$$\mathbf{y}[k] = \mathbf{C}_a\mathbf{x}_a[k] \tag{8.65b}$$

where the matrices with subscript a are given by

$$\mathbf{\Phi}_a = \begin{pmatrix}\mathbf{\Phi} & \mathbf{0} \\ -\mathbf{\Gamma}_r\mathbf{C}_r & \mathbf{\Phi}_r\end{pmatrix}, \qquad \mathbf{\Gamma}_a = \begin{pmatrix}\mathbf{\Gamma} \\ \mathbf{0}\end{pmatrix} \tag{8.66}$$

and

$$\mathbf{C}_a = \begin{pmatrix}\mathbf{C} & \mathbf{0}\end{pmatrix}. \tag{8.67}$$

As for the SISO case, presented in the previous section, it is chosen to be able to track a ramping output current reference without error. This requires two poles at $z = 1$ in the z-plane. The bias currents are only required to prevent DCM, therefore, tracking requirements are less strict. Since the constant disturbance $\boldsymbol{\omega}_o$ and references are fed forward no additional reference dynamics is added for the bias current control.

The state-space representation of the reference dynamics can easily be expressed in controller or observer canonical form. In this case the observer canonical form given in [120, page 401] is used, resulting in

$$\mathbf{\Phi}_d = \begin{pmatrix}2 & 1 \\ -1 & 0\end{pmatrix}, \qquad \mathbf{\Gamma}_d = \begin{pmatrix}2 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0\end{pmatrix} \tag{8.68}$$

where it is assumed that the numerator of the discrete transfer function of the reference dynamics equals z^2, which corresponds to backward Euler integration.

8.4.2 Pole placement based on a prototype Bessel system

Different methods to determine the feedback matrix $\mathbf{K}_p$ are known in literature. The two most widely used methods for MIMO systems [42, 44] require that the whole state vector of the plant under control is known or observable, and that the plant is stabilizable.

The method described in [42] became known as the linear-quadratic regulator (LQR) problem. This method determines $\mathbf{K}_p$ by minimizing a quadratic cost func-

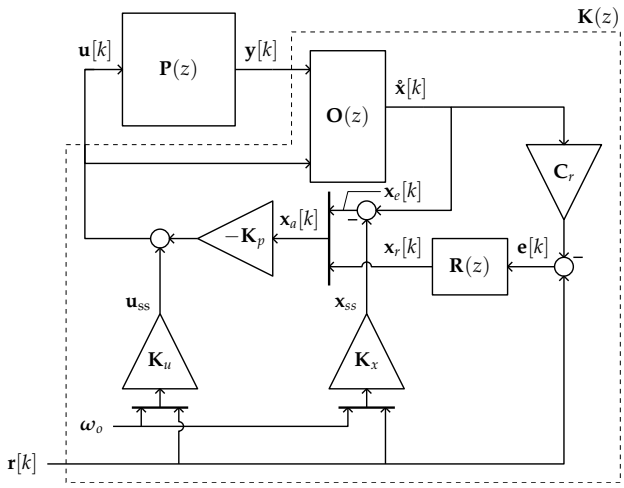


Figure 8.18: Schematic diagram of the full-state-feedback controller of Figure 8.17, with added reference dynamics $\mathbf{R}(z)$. The black bars represent vector a concatenation.

tion and is, therefore, a kind of optimal control. The method described in [44] can be used to place the closed-loop poles at arbitrary positions, with the restriction that the multiplicity of the closed-loop poles cannot be greater that the number of inputs of the plant. When a plant has multiple inputs, infinite solutions exist to the pole placement problem. The algorithms described in [44] iteratively determine the feedback matrix $\mathbf{K}_p$ that minimizes the sensitivity of the closed-loop pole locations to model uncertainties.

In this case study the MATLAB function *place*, which is based on [44], is used to place the closed-loop poles at the desired locations. The dominant poles are placed according to a Bessel prototype system as explained in [120, page 233]. Because the transfer function from $u^*_{\text{avg}_{\text{DM}}}$ to i_{out} is third order, a 3$^{\text{rd}}$-order Bessel prototype system with $22T_s$ settling time is used. The settling time was chosen such that the resulting closed-loop system is robust for component variations, as will be shown later in this section. The four poles associated with the input delay are left in the origin of the z-plane, the remaining poles are positioned on the real axes on frequencies that are at least a factor three higher than the real pole of the Bessel prototype system.

The desired closed-loop pole locations are chosen as

$$p_{\text{cl}} = \begin{pmatrix} 0^{\times 4} & 0.4509^{\times 4} & 0.5052^{\times 2} & 0.7965 & 0.8228 \pm 0.1429j \end{pmatrix} \tag{8.69}$$

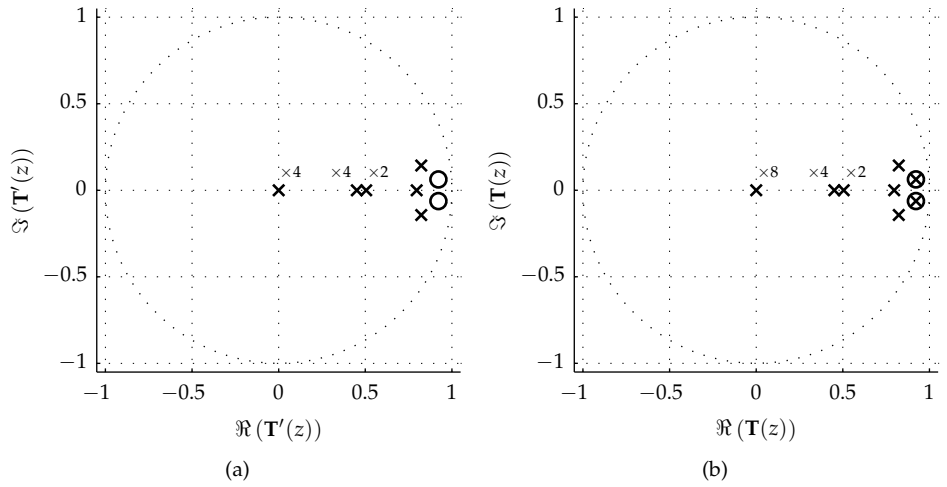


Figure 8.19: Pole-zero map of (a) the closed-loop system without observer ($\mathbf{T}'(z)$), and (b) closed-loop system with observer ($\mathbf{T}(z)$). The closed-loop poles and zeros are indicated with crosses and circles respectively. The superscripts $\times n$ indicate a multiplicity of the poles and zeros respectively.

where the superscript $\times n$ represents the pole multiplicity.

Figure 8.19 depicts the resulting closed-loop pole and (transmission) zero [100, page 141] locations of the system without observer $\mathbf{T}'(z)$ and observer feedback system $\mathbf{T}(z)$, which will be explained later in this section. The superscripts and subscripts in Figure 8.19 denote the pole and zero multiplicities respectively.

The closed-loop poles in Figure 8.19a appear at the desired locations, given by (8.69). However, even though the plant ($\mathbf{P}(z)$) does not have any zeros[1], two complex-conjugate zeros appear in the closed-loop z-plane. The zeros do not influence the settling-time of the closed-loop system, however, they do influence the transient response. From Figure 8.19b it can be seen that the pole locations of the system without observer are not affected by the added observer dynamics, as predicted by the separation principle. It should be noted that, for clarity, non-significant sampling zeros are not displayed in Figure 8.19.

[1]When assuming that the full state vector is measured.

8.4.3 Reduced-order observer implementation

Up to now it was assumed that the complete state vector is known. This is not the case for the DB model given in (8.16), where only the currents are measured. In this example a reduced-order observer (ROO) is used to estimate the remaining part of the state vector ($u_{C_{fp}}$ & $u_{C_{fn}}$). The resulting ROO requires only two states instead of the seven states that would be required when a full-order observer would be implemented.

The design procedure for reduced-order observers is described in detail in [120, chapter 7]. First the state-space model of the discrete plant (8.16) is partitioned as

$$\begin{pmatrix}\mathbf{x}_1\\ \mathbf{x}_2\end{pmatrix}[k+1] = \begin{pmatrix}\mathbf{\Phi}_{11} & \mathbf{\Phi}_{12}\\ \mathbf{\Phi}_{21} & \mathbf{\Phi}_{22}\end{pmatrix}\begin{pmatrix}\mathbf{x}_1\\ \mathbf{x}_2\end{pmatrix}[k] + \begin{pmatrix}\mathbf{\Gamma}_1\\ \mathbf{\Gamma}_2\end{pmatrix}\mathbf{u}_o[k]$$
$$\mathbf{y}_o[k] = \begin{pmatrix}\mathbf{C}_o & \mathbf{0}\end{pmatrix}\begin{pmatrix}\mathbf{x}_1\\ \mathbf{x}_2\end{pmatrix}[k]$$

where $\mathbf{x}_1$ are the measured states and/or known states, $\mathbf{x}_2$ are the states that need to be estimated, and $\mathbf{u}_o[k] = \begin{pmatrix}\boldsymbol{\omega}_o & \mathbf{u}[k]\end{pmatrix}^\mathsf{T}$. The delayed plant inputs do not need to be estimated. Therefore, $\mathbf{y}_o$ includes the delayed inputs, and as a result $\mathbf{C}_o$ is found to become

$$\mathbf{C}_o = \operatorname{diag}\left(\mathbf{C}, \mathbf{I}^4\right). \tag{8.71}$$

The general form of a reduced-order observer is given by

$$\mathbf{z}[k+1] = \mathbf{F}\mathbf{z}[k] + \mathbf{G}\mathbf{y}_o[k] + \mathbf{H}\mathbf{u}_o[k] \tag{8.72a}$$
$$\mathring{\mathbf{x}}_2[k] = \mathbf{I}\mathbf{z}[k] + \mathbf{L}\mathbf{y}_o[k] \tag{8.72b}$$

where $\mathring{\mathbf{x}}_2$ contains the estimated states, $\mathbf{z}$ is the observer state vector, and $\mathbf{L}$ is the observer feedback matrix. The system matrices of the ROO are derived in [120] and can be expressed in terms of the partitioned matrices and observer feedback matrix $\mathbf{L}$ as

$$\mathbf{F} = \mathbf{\Phi}_{22} - \mathbf{L}\mathbf{\Phi}_{12}$$
$$\mathbf{G} = (\mathbf{\Phi}_{21} - \mathbf{L}\mathbf{\Phi}_{11} + \mathbf{F}\mathbf{L})$$
$$\mathbf{H} = \mathbf{\Gamma}_2 - \mathbf{L}\mathbf{\Gamma}_1.$$

The estimation error of the ROO is given by

$$\mathbf{e}_2[k+1] = \mathbf{F}\mathbf{e}_2[k] \tag{8.74}$$

where $\mathbf{e}_2[k] = \mathbf{x}_2[k] - \hat{\mathbf{x}}_2[k]$. From (8.74) it can be seen that the estimation error becomes zero when the eigenvalues of $\mathbf{F}$ are inside the unit circle. Moreover, the ROO requires only feedback when $\mathbf{\Phi}_{22}$ is not stable, or when its the pole locations are not desired. When no observer feedback is applied, that is $\mathbf{L} = \mathbf{0}$, the estimated states only depend on the estimator state ($\mathbf{z}$).

Figure 8.20 depicts a schematic diagram of the ROO and $\mathbf{O}(z)$. From Figure 8.20 it can be seen that the delayed inputs are determined outside the ROO. The fully estimated state vector $\hat{\mathbf{x}}$, containing both the measured/known states $\mathbf{x}_1$ and estimated states ($\hat{\mathbf{x}}_2$), is obtained from the ROO state vector and the measured/known plant outputs as

$$\hat{\mathbf{x}}[k] = \mathbf{U}\mathbf{z}[k] + \mathbf{V}\mathbf{y}_o[k] \tag{8.75}$$

where the matrices $\mathbf{U}$ and $\mathbf{V}$ are partitioned such that the estimated state vector ($\hat{\mathbf{x}}$) is ordered such as the plant state vector ($\mathbf{x}$).

The separation principle states that the closed-loop pole locations of the total observer feedback system is the collection of the observer poles and the closed-loop poles of the system without observer. The observer poles, however, do influence the robustness of the system to perturbations, as will become clear later in this section. A rule of thumb is to place te observer poles at three to five times higher frequencies than the closed-loop system poles, as suggested in [120, page 285] and [12, page 45]. However, in [120] it is also suggested to place observer poles on zeros that are close to the dominant poles of the system.

Figure 8.19b depicts the pole-zero map of the complete observer feedback system. From Figure 8.19 it can be seen that the ROO poles are placed on the (transmission) zeros, the input delays in $\mathbf{O}(z)$ appear in the origin of the z-plane.

8.4.4 Closed-loop frequency responses

Figure 8.21 illustrates the output sensitivity and complementary sensitivity from i^*_{out} to i_{out} (S_{out} & T_{out}) and $i^*_{\text{bias}_p}$ to i_{bias_p} (S_{bias} & T_{bias}). The dashed lines represent the results for the optimized SISO controller proposed in the previous section, and the phase information for the sensitivities is omitted for clarity. The sensitivity to output disturbances of the bias is higher for the state-feedback controller than for the SISO case. This is due to the lack of integrating reference dynamics for the bias

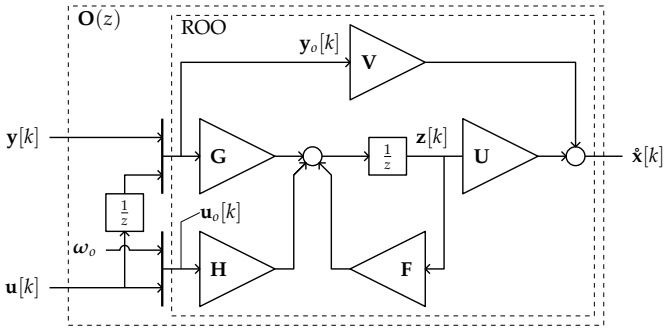


Figure 8.20: Schematic diagram of the reduced-order observer. The black bars represent vector concatenation.

currents in the state-feedback controller. However, the bandwidth of the state-feedback bias current regulation is 1.6 times higher than the SISO case. For both cases the bias current controllers have more bandwidth than the output current controller, which is required when the bias current is modulated as given in (4.21).

The bandwidth of the output current control for the state-feedback controller has increased a factor 2.7 with respect to the SISO controller. Furthermore, the sensitivity to disturbances on the output current, within the bandwidth of the controller, is much lower than the SISO case, presented in the previous section, which comes at the cost of higher gain peaking, i.e. 7.9 dB instead of 4.7 dB.

Also the output impedance of the state-feedback controller has increased significantly for most frequencies with respect to the SISO case, which can be expected from the lower sensitivity to disturbances on the output current (i_{out}).

When applying state feedback the transfer functions from $i^*_{\text{bias}_p}$ to i_{bias_p} and $i^*_{\text{bias}_n}$ to i_{bias_n} are not generally equal. However, the closed-loop pole locations given in (8.69) result in a perfectly decoupled system with identical bias controllers, for both the positive (p) and negative (n) side.

8.4.5 Zero cancellation with reference prefilter

Ideally a Bessel system exhibits nearly no overshoot and a constant group delay. As a result the output is a delayed band-limited representation of its input. This property is especially useful in applications that require low distortion and reproducibility, and do not suffer from delay, as in high-quality audio and MRI, where the reference signal can be advanced to compensate for the group delay of the Bessel system.

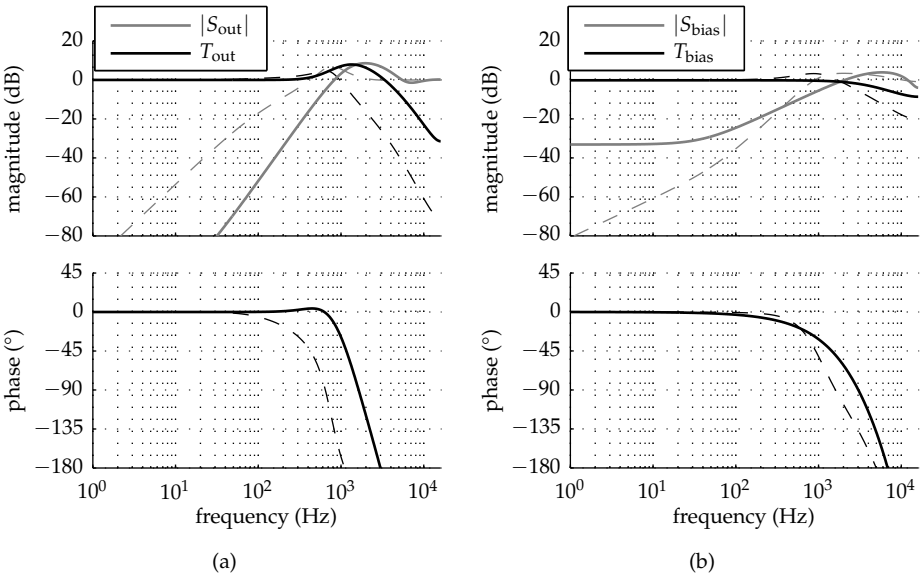


Figure 8.21: Bode diagrams of the sensitivity (S) and complementary sensitivity (T) from i^*_{out} to i_{out} (a), and $i^*_{\text{bias}_p}$ to i_{bias_p} (b) of the closed-loop system. The solid lines represent the state-feedback presented in this section, the dashed lines represent the optimized SISO approach suggested in the previous section.

Figure 8.22a depicts the step response of the output current of the observer feedback system ($\mathbf{T}(z)$). The dashed line indicates the step response of the SISO controller which is added for reference. The step response shows significant overshoot, which would not be expected for a Bessel system. The overshoot in the step response is caused by significant zeros in the transfer function from i^*_{out} to i_{out} (T_{out}). A Bessel system should have no zeros in its transfer function.

Figure 8.22a also depicts the required input $m_{\text{avg}_{\text{DM}}}$ for the step response[2]. The decoupled input required for the step is given by

$$m_{\text{avg}_{\text{DM}}} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \end{pmatrix} \mathbf{u} \tag{8.76}$$

which has a maximum range of ± 2. From the required control action it can be seen that it is not possible to achieve the simulated response for a 1 A step on the output current, because it requires too much control effort. The input required for a unit step does not exceeds its maximum value for the optimized SISO controller designed in the previous section.

Figure 8.23 shows in black the pole-zero map of the minimum realization of the transfer function T_{out}, i.e. with all pole-zero cancellations removed. It can be seen that the two complex conjugate zeros, which cause the overshoot in Figure 8.22a, and the poles associated with the Bessel system are present in T_{out}.

Canceling of the zeros by poles in the controller leads to unwanted dynamics, because, in practice, it is not possible to exactly cancel the zeros perfectly, even when the zeros are not affected by model uncertainties, which is true in this particular case. However, when the zeros are not affected by model uncertainties the zeros can be canceled with a prefilter, as is commonly applied in classical proportional-integral-differential (PID) control [120, page 254].

In this case two complex zeros need to be canceled by the prefilter. The resulting prefilter has two poles at the complex zero location, as indicated by gray crosses in Figure 8.23. The prefilter has a low-pass response and basically limits the slew rate of i^*_{out} by canceling high frequencies in the reference signal.

Figure 8.22b depicts the step response of i_{out} with the prefilter. The dashed line indicates the output current step response of the system without prefilter. From Figure 8.22b it can be seen that there is nearly no overshoot, as would be expected from a Bessel response. Furthermore, the settling time of the closed-loop system is not affected by the prefilter. Moreover, the control effort required for the unit step on the output current reference is reduced significantly with respect the sys-

[2]Because the proposed state-feedback controller is perfectly decoupled $m_{\text{avg}_{\text{DM}}}$ can be used to compare control efforts.

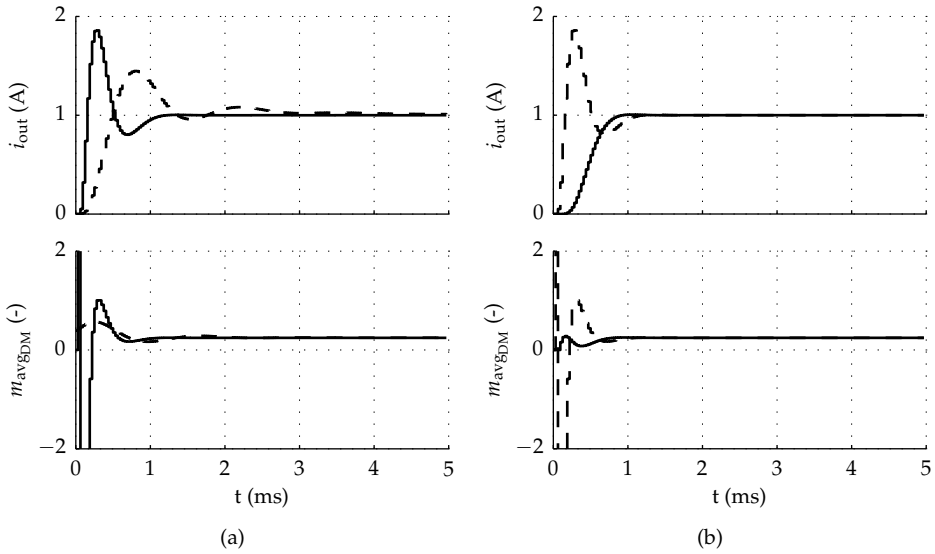


Figure 8.22: Step responses of i_{out} and corresponding control action $m_{\text{avg}_{\text{DM}}}$. The solid lines represent the observer feedback system ($\mathbf{T}(z)$), (a) without prefilter, and (b) with prefilter. The dashed lines are added for reference and correspond to the optimized SISO system of the previous section in (a), and the observer feedback system ($\mathbf{T}(z)$) without prefilter in (b), which is the same as the solid line in (a).

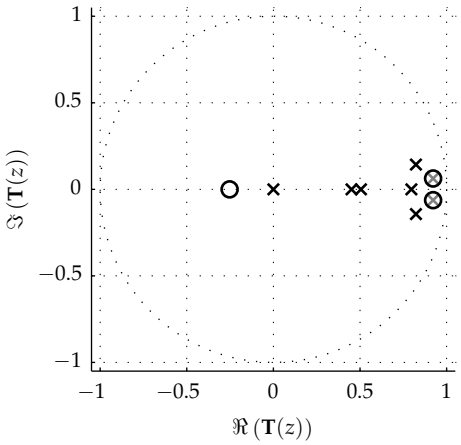


Figure 8.23: Pole zero map of T_{out} and the prefilter $F(z)$, depicted in black and gray respectively. The poles are indicated with crosses and the zeros with circles.

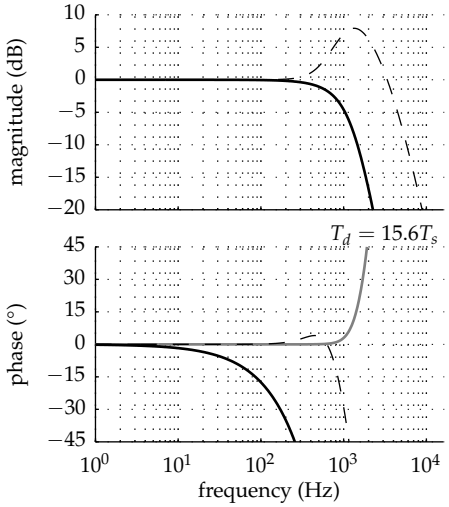


Figure 8.24: Bode diagram of T_{out} with prefilter $F(z)$. The gray line indicates the phase response of T_{out} after compensation for delay T_d. The response without prefilter is indicated with dashed lines for reference.

tem without prefilter, and is even less than the optimized SISO controller of the previous section.

In this case a 3$^{\text{rd}}$-order Bessel filter was chosen because all Bessel poles appear uncanceled in T_{out}. However, it is not necessarily true that no zero cancellations of Bessel poles occur in T_{out} when pole placement is applied. Figure 8.24 depicts the Bode diagram of T_{out}. To show the constant group delay property of the Bessel response, the phase after compensation for the delay T_d is given in gray. From Figure 8.24 it can be seen that the Bessel system has a constant group delay of $15.6T_s$ for frequencies up to almost 1 kHz. The response without prefilter is indicated by the dashed lines for reference.

Due to the added prefilter, ramps are not tracked with zero error anymore. Moreover, the delay added by the Bessel response makes the approach unsuitable for systems with multiple control loops, like in servo systems. However, in many industrial applications the prefilter dynamics can be incorporated in the reference generation, instead of in the amplifier, because the reference signals are known a-priori. Also a reference governor, as suggested in [102], can be used to augment the reference such that the required control effort stays within limits. As a result, zero tracking error can be achieved without the delay associated with the Bessel system.

8.4.6 Robustness of the closed-loop system

To illustrate the impact of parameter variations on the closed-loop system, a similar Monte Carlo experiment was performed as for the SISO control system. Each Monte Carlo analysis involves 1764 calculations of the discrete plant. For each iteration the parameters are pseudo-randomly chosen from a uniform distribution. The same cases of parameter variation are used as for the SISO control system. Table 8.1 shows the used component values and the corresponding parameter deviations.

Figure 8.25 depicts the poles of the feedback system ($\mathbf{T}'$) in (a) and observer feedback system ($\mathbf{T}$) in (b), for *case 1* in dark gray, and *case 2* in light gray. From the pole locations it can be seen that both systems are robust for the simulated parameter variations.

Figure 8.26 depicts the impact of component variation on the Bode diagrams of transfer functions T_{out} and T_{bias}. As in the SISO case the influence of component variation is negligible for frequencies where the sensitivity to disturbances is sufficiently low. Again the Bode diagram of T_{bias} shows very little influence of the component variation.

The response to a step of T_{out}, without prefilter, and T_{bias} with component variation is depicted in Figure 8.27. All simulated step responses of i_{out} settle within reasonable time. Again the step response of the bias current shows very little effect of the component variation.

From Figure 8.28 it can be seen that the applied feedback improves the decoupling. However, for frequencies where the open-loop gain is lower than 10 dB the cross coupling from i^*_{bias} to i_{out} becomes significant. This suggests that for high-precision applications it is best not to excite $u^*_{\text{bias}_x}$ at those frequencies. The cross coupling from i^*_{out} to $i^*_{\text{bias}_x}$ peaks at over 20 dB. Therefore, a higher offset (i_{th}) might be required for the bias current to compensate for the cross coupling at those frequencies.

8.5 Summary

In this chapter a discrete model and two control methods are proposed for the DB. The derived discrete model is only valid for CCM, and includes the effects of the forward voltages and resistances of the switches and diodes. The discrete model also includes the delay required for data acquisition, and calculation of new modulation indices.

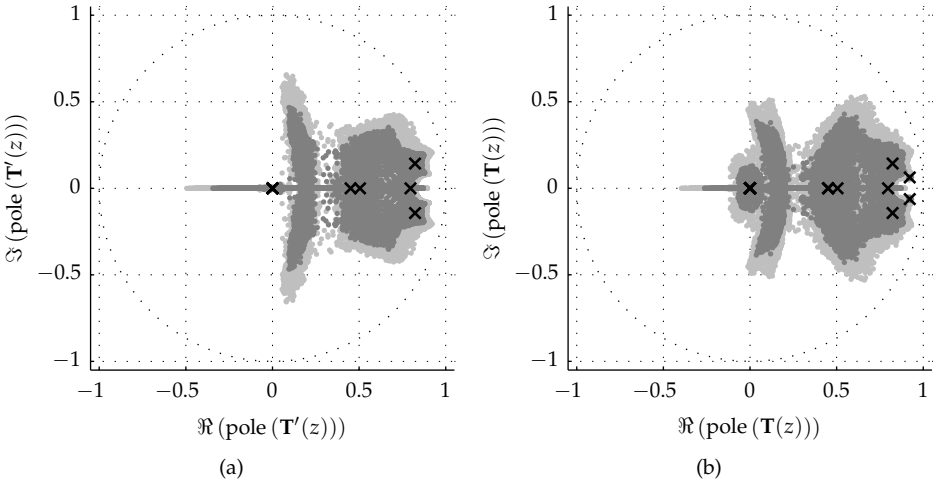


Figure 8.25: Closed-loop pole locations with component variation, for *case 1* (gray) and *case 2* (light gray). The intended pole locations are indicated with black crosses. In graph (a) it is assumed that the complete state-vector is measured and that no observer is required (**T**′), and (b) is with observer (**T**).

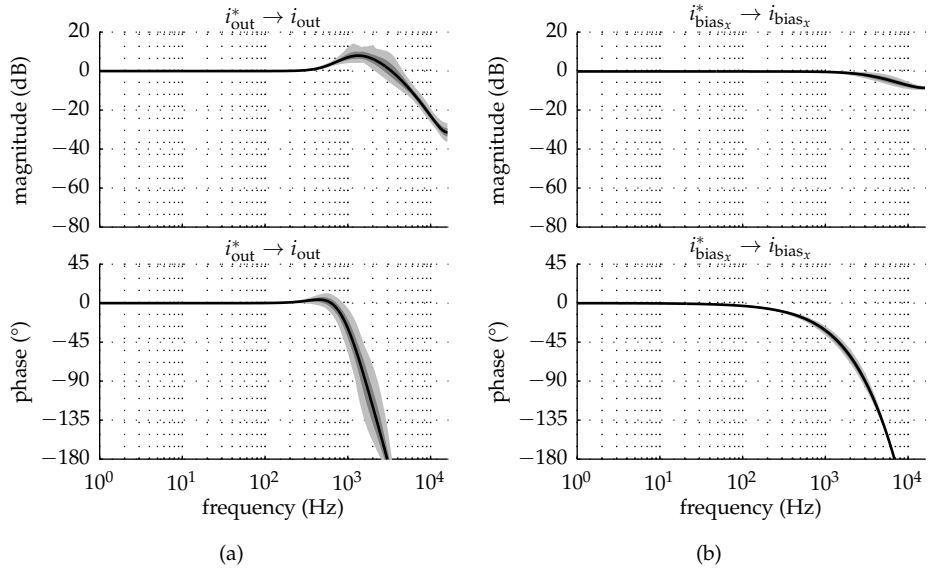


Figure 8.26: Bode diagrams illustrating the influence of component variation on (a) T_{out} without prefilter, and (b) T_{bias}, for *case 1* (gray) and *case 2* (light gray). The intended magnitudes and phases are indicated with black lines. Both graphs apply to the control system with observer (**O**).

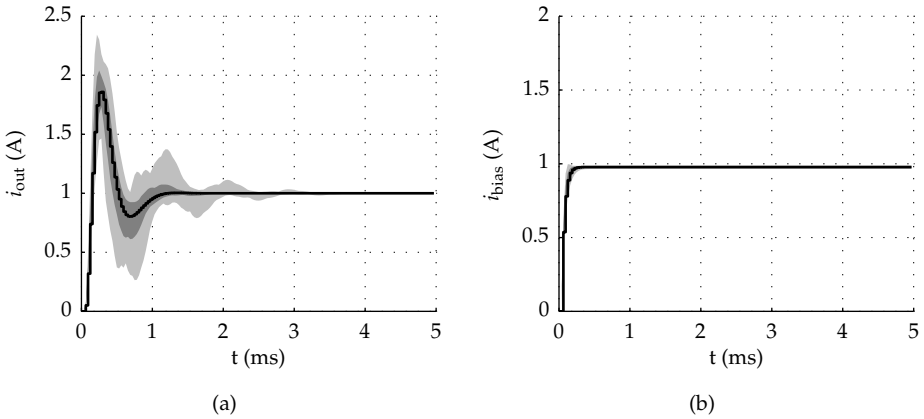


Figure 8.27: The influence of component variation on the step response of (a) T_{out}, and (b) *Tbias*, for *case 1* (gray) and *case 2* (light gray). The solid and black lines represent the intended step responses.

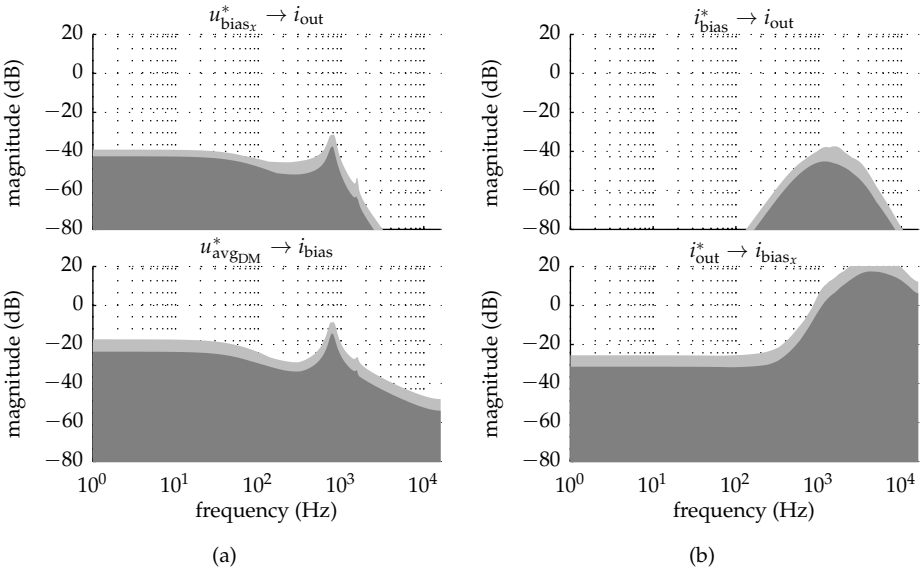


Figure 8.28: Bode magnitude diagrams illustrating the influence of component variation on the cross coupling between inputs and outputs of the (a) open-loop plant ($\mathbf{P}'(s)$), and (b) closed-loop system with observer ($\mathbf{T}$), for *case 1* (gray) and *case 2* (light gray).

The first feedback method is based on a decoupled control of bias and output current. It is shown that ideally the output current and bias current are perfectly decoupled, and even in the presence of considerable component variation the decoupling is sufficient to achieve excellent regulation of the output current.

The output current control scheme consists of multiple loops. Two damping loops are applied to damp the DM and CM resonances of the output filter. The output current is regulated by a controller with double integrating action. The two bias currents are regulated by separate proportional integrating controllers. The control parameters are found by a loop-shaping procedure. Furthermore, minimization of the time-weighted squared error of the step response is applied to optimize the gain and zero locations of the output current controller. The proposed output current control can also be applied to conventional FB converters.

The second feedback method is a full state feedback with reduced-order observer to estimate the capacitor voltages. Steady-state reference tracking is implemented by a combination of state error feedback and input feedforward. Double integrating reference dynamics are added for the output current. The dominant closed-loop poles are placed according to a Bessel prototype system with a specified settling time.

Bessel systems have a constant group delay and step response with nearly no overshoot. A prefilter is added to cancel significant zeros from the transfer function corresponding to the output current. The combination of the observer feedback system with the prefilter results in both a low sensitivity to disturbances and a Bessel output current step response.

The robustness of both control methods was verified with an extensive Monte Carlo simulation experiment. The experiment showed that both controllers are robust for the simulated variations. Especially the bias current regulation showed to be insensitive to model perturbations in both experiments.

Chapter 9

Experimental results

"A learning experience is one of those things that say, 'You know that thing you just did? Don't do that.'"

(Douglas Adams)

Abstract — This chapter deals with the practical results obtained from a dual-buck converter prototype. First, the average model and the controllers, detailed in Chapter 8, are verified with measurements. It is shown that the measured frequency and step responses agree well with the analytical and simulation results from Chapter 8. Next, various aspects of the open-loop harmonic performance are measured and compared to the simulation results and analytical expressions given in Chapter 6. It is shown that the DB topology can achieve an open-loop THD better than 0.01 %, which is an over 40 dB improvement compared to the conventional full-bridge converter.

9.1 Experimental setup

A prototype converter was built that can be configured as a full-bridge equivalent DB or a conventional FB by connecting the switch nodes of the P- and N-cell of each side of the full-bridge by means of a relay contact. Figure 9.1 depicts the schematic diagram of the prototype converter. The switch nodes can be connected with the relays designated FB. The rest of the setup is similar to the circuits analyzed in Chapter 8. However, the output filter consists of five capacitors, not three as depicted in Figure 8.1. These capacitor values are chosen such that the behavior of both realizations is equivalent. The measured currents, required for feedback, are indicated in the figure. Instead of a symmetrical supply, a single power supply is used in the experimental setups.

The nominal component values of the experimental setup are summarized in Table 9.1. The power supply voltage is chosen to be 100 V, low enough to amplify the effects of the forward voltages of the switches and diodes. In order to increase the voltage stability for some measurements the output of the power supply was compensated, as described in Appendix A.2. A resistor-inductor load was used to represent the voice-coil actuator that is often used as load circuit in short-stroke positioning systems. Note that the value of C_f in Table 9.1 is half the value shown in Table 8.1. The switching frequency was chosen 16 kHz and the modulators are updated twice per switching cycle. For the full-bridge configuration the blanking time (T_{bt}) was set to 2 % of T_{sw} (1.25 µs). Unless otherwise noted, the offset current i_{th} was set to 5.5 A for the dual-buck configuration, which is enough to guarantee CCM and driver-limited voltage commutation as discussed in Chapter 6.

Figure 9.2 shows details of the experimental setup. The converter is based on an off-the-shelf Semikron SEMISTACK SKS40FB2C07V6 IGBT stack with a custom-designed gate-driver board, as described in Appendix A.1. It should be noted that this commercially available stack is by no means intended for generating low distortion waveforms.

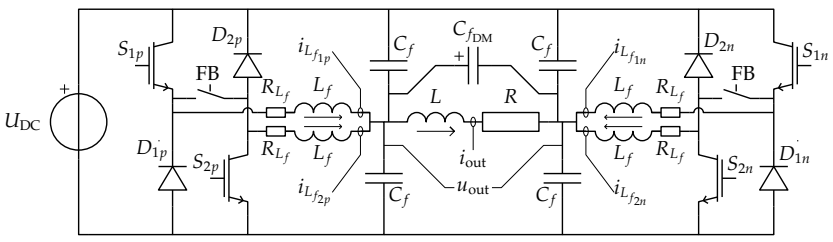


Figure 9.1: Schematic overview of the reconfigurable full-bridge equivalent DB and conventional FB setup.

Table 9.1: Component values used in the experimental setup.

Item	Value		Description
U_{DC}	100	V	Delta Elektronika SM 120-50[I]
C_{DC}	6	mF	Rifa PEH200VH410AMB3[II]
L	1.7	mH	Air-cored inductor
R	12.1	Ω	Vishay LPS 300 thick film[III]
	2.5	Ω	1.5 kW wire wound resistor [IV]
L_f	208	µH	See separate inductors on page 99
R_{L_f}	50	mΩ	
C_f	50	µF	Vishay MKP1848650094Y5
$C_{f_{\mathrm{DM}}}$	160	µF	Vishay MKP1848716704Y5
S_x	-		Semikron SKM75GB123D
D_x	-		

[I]For some measurements a low-voltage linear amplifier was connected in series with the power supply to improve its voltage stability.
[II]six parallel strings of two series-connected capacitors.
[III]Parallel connection of four 100 Ω and two 47 Ω resistors.
[IV]Stainless steel conductor.

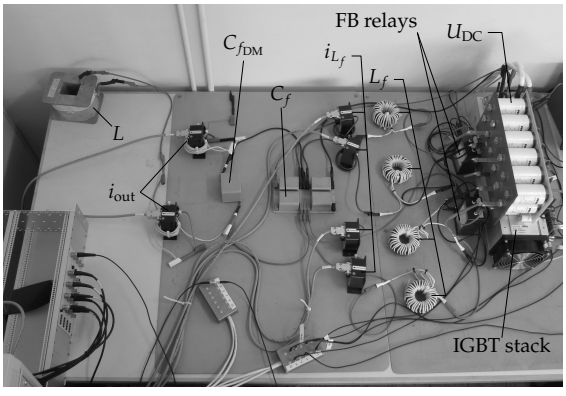


Figure 9.2: Picture of the reconfigurable full-bridge equivalent DB, and conventional FB setup.

The PWM generation and control are implemented on a dSPACE rapid prototyping system, as described in Appendix A.3. For the experimental verification the PWM carrier phase shifts were set to bipolar switching, *case 1* in Chapter 7, unless otherwise stated. Two separate current sensors were used to measure the output current. One is connected to the feedback control system, if active, and the other is connected to the signal analyzer. The time-domain graphs in this chapter have been captured using a LeCroy Waverunner 44MXi-A and the frequency responses and spectra were measured using a Stanford Research Systems SR785 dynamic signal analyzer. This analyzer is capable to automatically range its inputs to the maximum range of its 16-bits ADCs from 3 mV to 50 V in 2 dB steps. As a result this signal analyzer typically has better than 90 dB dynamic range.

The spectra and distortion are the most critical measurements and are therefore performed using the dynamic signal analyzer. The output voltage spectra (u_{out}) of the setup were directly measured using the differential input of the signal analyzer, through a 1/3 high-precision attenuator[1]. The output current was measured using an LEM IT200 fluxgate sensor with a 5 Ω burden resistor. Depending on the required measurement range, either 6 or 12 primary turns were used. All spectra were averaged 21 times using the RMS averaging function of the analyzer. This preserves the level of the (uncorrelated) noise while reducing fluctuations in the (correlated) spectral components.

9.2 Model and controller verification

In Chapter 8 a state-space averaged model was presented and two feedback control methods were suggested for the DB topology. The first control system is based on separate decoupled SISO controllers and the second is based on MIMO full state feedback. In this section the state-space model and both feedback controllers are compared to measurements done on the experimental setup.

9.2.1 Averaged model

Figure 9.3 depicts the measured open-loop Bode diagrams from reference input[2] $u^*_{\text{avg}_{\text{DM}}}$ to i_{out}, and from $u^*_{\text{bias}_p}$ to i_{bias_p}, in black. The measurements were made using the swept-sine function of the SR785 signal analyzer using a frequency span

[1] The attenuator consists of 3 Vishay Y006220K0000T9L, 20 kΩ 0.01 % resistors with 1 ppm/K temperature coefficient.

[2] The schematic diagram of the PWM modulator with the corresponding reference signals is given in Figure 7.2a.

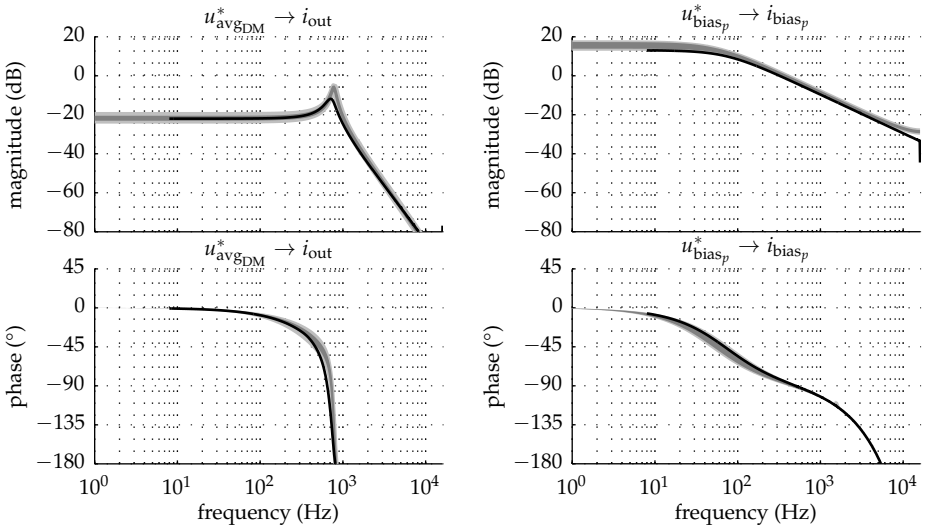


Figure 9.3: Measured Bode diagrams of the open-loop decoupled transfer functions, from (a) $u^*_{\mathrm{avg}_{\mathrm{DM}}}$ to i_{out}, and (b) u^*_{bias} to i_{bias_p}. Also the simulated influence of component variations is illustrated for *case 1* (gray) and *case 2* (light gray).

from 8 Hz to 16 kHz. Figure 9.3 also shows the simulated Bode diagrams for two cases of component variations, as given in Figure 8.13 considering the parameter variations shown in Table 8.1.

The Bode diagram from input $u^*_{\mathrm{avg}_{\mathrm{DM}}}$ to i_{out} is in good agreement with the expected result. Some additional damping can be observed because less gain peaking occurs at the DM resonance frequency of the output filter. The extra damping is caused by additional resistance in the bias path. This can also be seen from the measured magnitude, depicted in Figure 9.3b, which illustrates the frequency response from input $u^*_{\mathrm{bias}_p}$ to i_{bias_p}. The measured magnitude is slightly lower than expected when including the simulated component variation. Also for higher frequencies the measured magnitude of the bias current is slightly lower than expected. This difference can be attributed to discontinuous inductor currents that occurred during the measurements for frequencies close to f_{sw}. The spike at 16 kHz might be due to the switching of the converter. Otherwise the measured Bode diagram is in good agreement with the results of Chapter 8.

9.2.2 Decoupled SISO control

Figure 9.4 depicts the closed-loop Bode diagrams from i^*_{out} to i_{out} (T_{out}) and i^*_{bias} to i_{bias_p} (T_{bias}) for the decoupled feedback control presented in Section 8.3[3]. The measured magnitude of T_{out} falls within the expected curves. However, the measured phase is slightly out of the expected tolerance band for frequencies close to the gain peaking. This difference is again likely caused by the slightly higher damping in the bias path. The closed-loop Bode diagram of T_{bias} falls within the expected tolerance bands, except for effects due to DCM that occurred for frequencies close to f_{sw}, and the spikes at 16 kHz, which can again be attributed to the switching of the converter.

The open- and closed-loop cross coupling were also measured and compared to the simulations in Figure 8.14. Figure 9.5 illustrates the measurements on top of the simulated results that include the parameter variation. The open-loop cross coupling from $u^*_{\text{bias}_p}$ to i_{out}, in Figure 9.5a, follows the expected trend up to approximately 1 kHz. For higher frequencies the dynamic range of the measurement was not sufficient to accurately measure the response. The cross coupling from $u^*_{\text{avg}_{\text{DM}}}$ to i_{bias_p} was better scaled and could be measured with relatively good accuracy over the entire frequency span. The peaks which occur at 8 and 16 kHz in the measurements are caused by the sampling of the ADCs of the dSPACE platform and switching transients of the converter, and can be ignored.

From Figure 9.5 it can be seen that even though the damping was slightly higher than expected, the practical component values are quite symmetrical, i.e. the variation between individual components with the same nominal value is significantly lower than expected. The same applies for the closed-loop cross coupling shown in Figure 9.5b for frequencies higher than 100 Hz. The higher-than-expected coupling for frequencies below 100 Hz is most probably due to the limited resolution of the output current control system. Otherwise, the measured cross coupling follows the expected trends very well.

Figure 9.6 shows the measured unit step responses for the output and the bias current superimposed on top of the simulated responses, including parameter variation. The measured output current step response falls withing the expected tolerance band. The measured step-response of the bias current is in good agreement with the simulated results, given the higher damping in the bias path that was discussed before.

Figures 9.7a, 9.7b, and 9.9a depict measured waveforms under closed-loop conditions, for the DB with constant bias current, DB with modulated bias current,

[3]For reference, the control diagram is given in Figure 8.7.

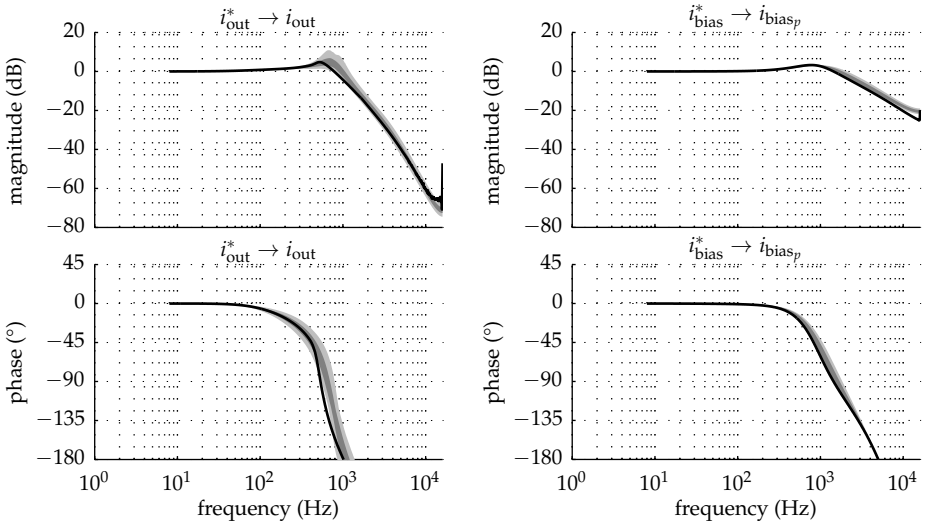


Figure 9.4: Measured Bode diagrams (black) of the closed-loop systems (a) T_{out}, and (b) T_{bias}. Also the simulated influence of component variation is illustrated for *case 1* (gray) and *case 2* (light gray), as also shown in Figure 8.13.

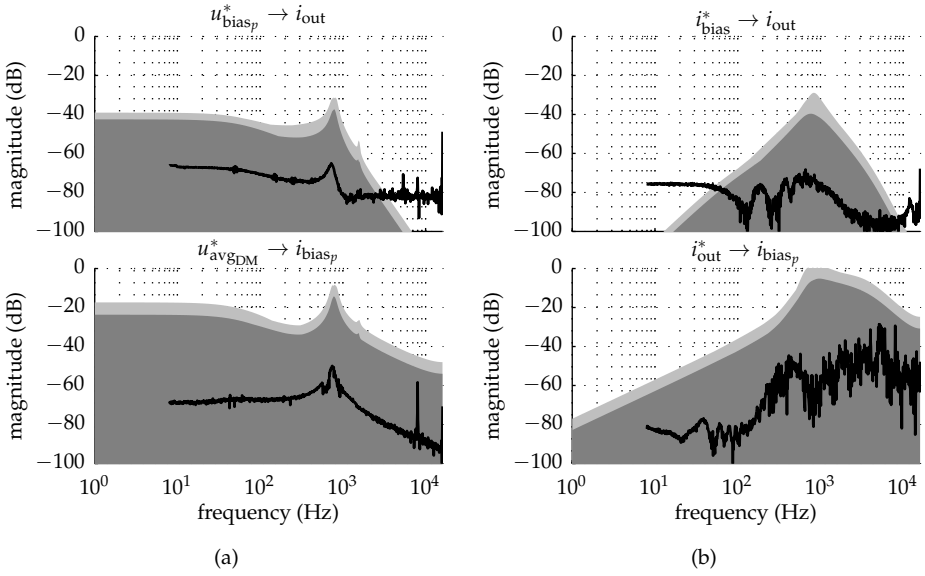


Figure 9.5: Measured Bode magnitude diagrams of the cross coupling between inputs and outputs (black) for (a) the open-loop system, and (b) closed-loop system. The simulated results illustrating the influence of component variation for case 1 (gray) and case 2 (light gray), as in Figure 8.14, are also shown.

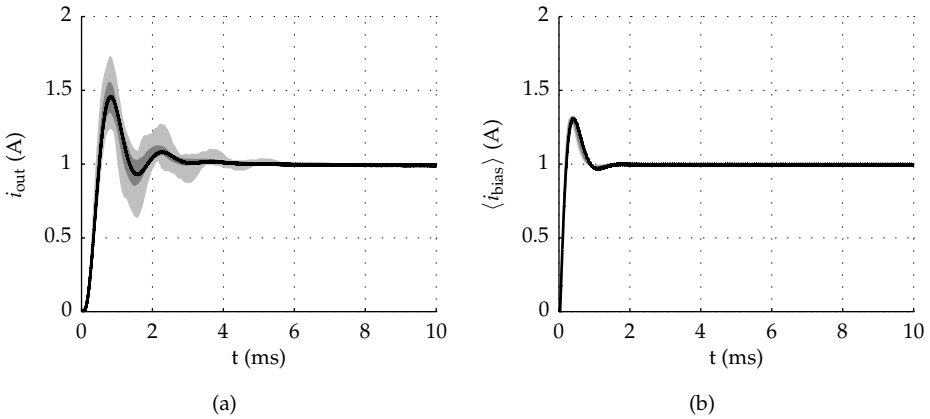


Figure 9.6: Measured step responses (black) of the closed-loop systems (a) T_{out}, and (b) T_{bias}. The influence of component variation on the responses for *case 1* (gray) and *case 2* (light gray), as are also illustrated in Figure 8.15.

and FB, respectively. A sinusoidal reference of 6 A/21 Hz was used. The measured waveforms of the DB resemble the simulation results shown in Figure 4.9 and Figure 4.10 in Chapter 4. However, it should be noted that those simulations were made with different load conditions and component values. Nevertheless, the presented results validate the results of Chapter 4.

The filter inductor current of the FB ($i_{L_{\text{HB}_p}}$) in Figure 9.9a shows some zero-current clamping effects. This is due to the blanking time, which was set to 1.25 µs. However, the output voltage and current waveforms of the FB appear to be sinusoidal. A closer look at the corresponding output current spectrum in Figure 9.9b reveals significant distortion, and a THD of 0.5 %, which was calculated by means of (3.1).

The corresponding output current spectra for the DB with constant and modulated bias current are given in Figure 9.8. The spurious harmonics of the DB are over 20 dB lower than for the conventional FB, resulting in over 10 times lower THDs. It should be noted that the closed-loop performance of the DB is determined by the measurement resolution of the dSPACE system in combination with the sensor, which was limited to approximately 13 effective bits. This will become more clear in the next section which treats the performance of the DB under open-loop conditions. However, first the full-state-feedback control system explained in Section 8.4 is verified.

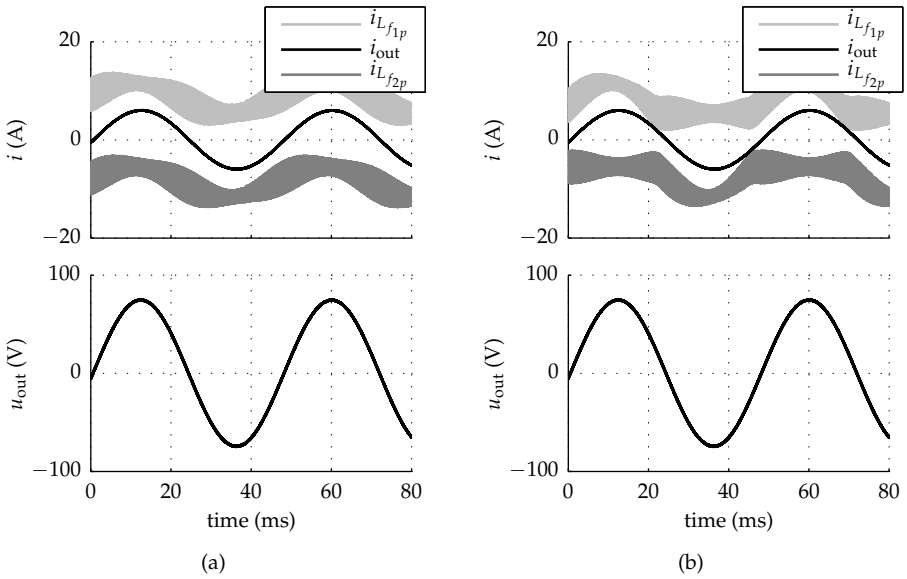


Figure 9.7: Measured waveforms for the DB, with constant bias current (a), and modulated bias (b), under closed-loop conditions. A sinusoidal reference of 6 A, 21 Hz was used, and the offset current was set to $i_{\text{th}} = 5.5$ A.

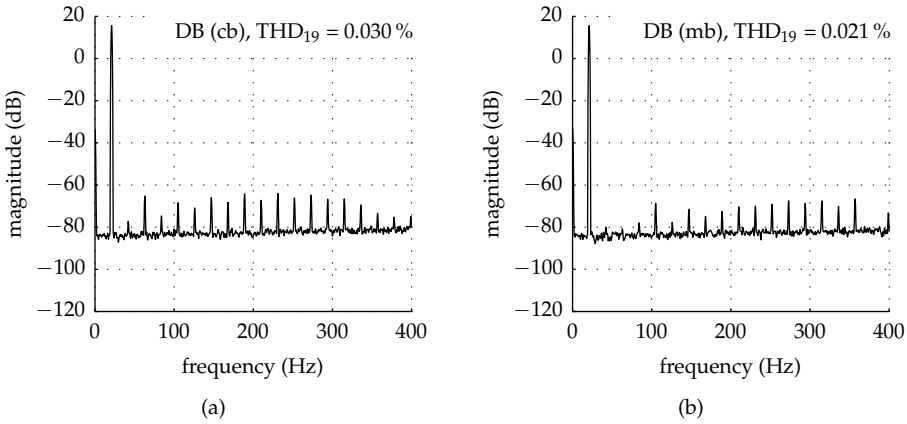


Figure 9.8: Measured output current (i_{out}) magnitude spectra for the DB, with constant bias current (a), and modulated bias (b), corresponding the output current waveforms in Figure 9.7. The current spectrum is normalized to 1 A.

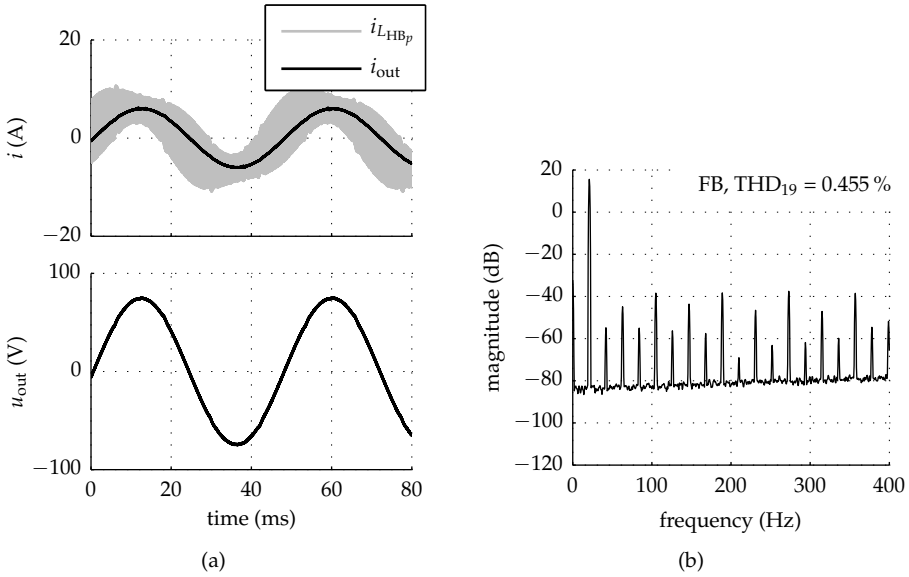


Figure 9.9: Measured waveforms for the FB (a), and the corresponding output current spectrum. The same output current controller as for the DB was used. The blanking time was set to 1.25 µs. The spectrum in (b) is normalized to 1 A, and the same reference was used as for the DB.

9.2.3 Full-state-feedback control

Figure 9.10 depicts the closed-loop Bode diagram of T_{out}, with and without prefilter, for the full-state-feedback control system treated in Section 8.4. The measured Bode diagrams stay within the simulated tolerance bands, which were determined in Section 8.4. However, the gain peaking occurs at a slightly lower frequency than expected, which can again be attributed to the higher-than-expected damping in the bias path.

The measured Bode diagram of T_{bias} in Figure 9.11a is also in agreement with the simulations done in Section 8.4. However, the magnitude for higher frequencies is slightly lower. This can again be attributed due to discontinuous inductor currents, which occur at higher frequencies.

When comparing the tolerance band of T_{bias} in Figure 9.11a with the decoupled control in Figure 9.4b, it can be seen that parameter variation has less impact on the feedback control. This is because the state-feedback controller uses only proportional feedback of the bias currents, as explained in Chapter 8.

The cross coupling between i^*_{bias} and i_{out}, and i^*_{out} and i_{bias_x} was measured. As was also observed for the SISO controllers, the cross coupling is much less than the worst case from the Monte Carlo analysis performed in Chapter 8. In Section 8.4 it was shown that the worst-case cross coupling from i^*_{out} to i_{bias_x} peaked at over 20 dB, suggesting that extra bias current might be required to prevent DCM. The measured cross coupling peaks at -20 dB, which is factor 100 less than worst case simulated. However, it should be noted that the component variation of the experimental setup is much less than assumed in the Monte Carlo experiment. Furthermore, to include the strong effects of temperature, the switching device parameter variation was chosen large in the Monte Carlo experiment. However, in practice the temperature differences between the semiconductors are relatively small leading to better matching between the semiconductor devices.

Figure 9.12 depicts the measured unit-step responses of the state-feedback system, without and with prefilter, superimposed on top of the expected curves, including the parameter variation investigated in Section 8.4. The oscillation of the step response without prefilter in Figure 9.12a has a slightly lower frequency due to the higher than expected damping in the bias path. Because of the high loop gain of state-feedback control, a step of only 75 mA was applied to prevent saturation of the controller. The step response with prefilter, depicted in Figure 9.12b, has a small overshoot. However, both step responses fall within the predicted tolerance band.

The measured step response of the bias current is shown in Figure 9.13. The

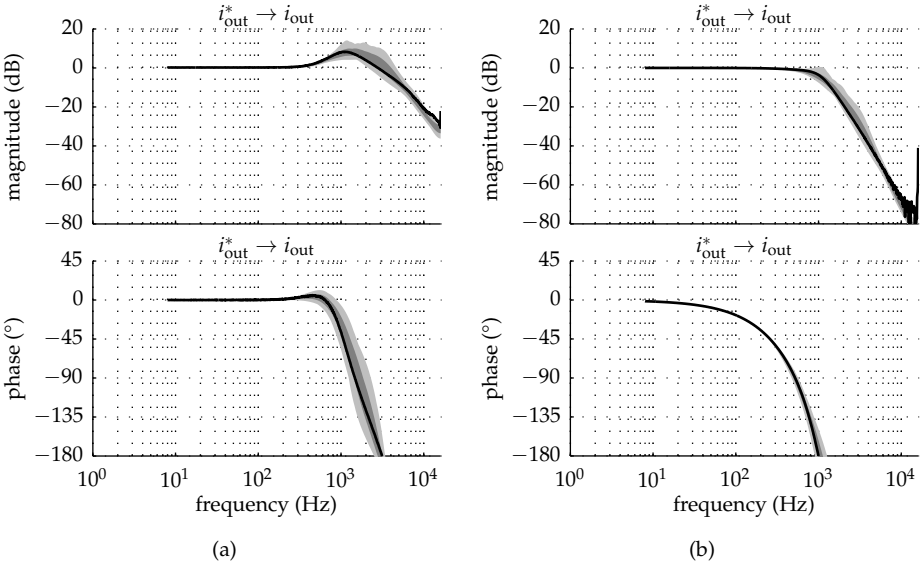


Figure 9.10: Measured Bode diagrams of T_{out} (a) without prefilter, and (b) with prefilter. The influence of component variation on the responses is also shown for *case 1* (gray) and *case 2* (light gray). This was also shown in Figure 8.26a for the case without prefilter.

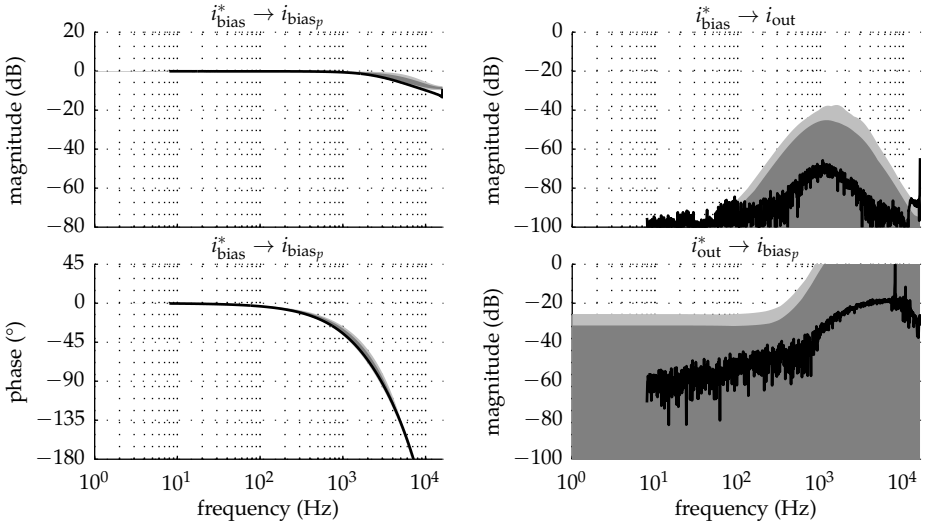


Figure 9.11: Measured Bode diagram of T_{bias} (a), and the measured Bode magnitude diagrams of the cross coupling of the closed-loop system with observer (**T**) (b). The influence of component variation on the responses is shown in gray and light gray, same as it was indicated in Figures 8.26b and 8.28b.

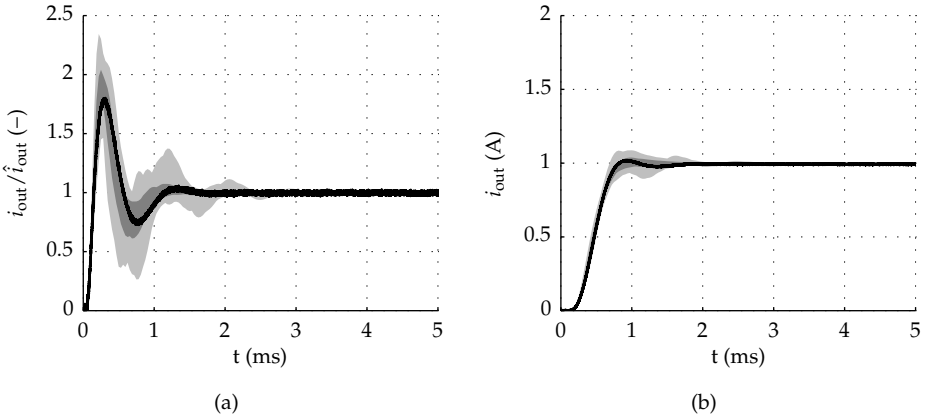


Figure 9.12: Measured step responses (black) of the closed-loop system T_{out}, without prefilter (a), and with prefilter (b). The influence of component variation on the responses for *case 1* (gray) and *case 2* (light gray) are also illustrated just as in Figure 8.27a for T_{out} without prefilter.

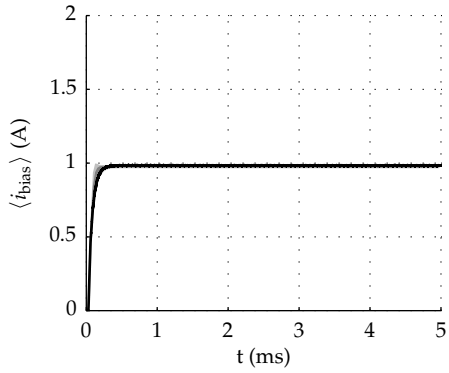


Figure 9.13: Measured step responses (black) of the closed-loop system T_{bias}. The influence of component variation on the responses for *case 1* (gray) and *case 2* (light gray) is illustrated in the same way as it was done in Figure 8.27b.

influence of component variation on the step response is small, as was the case for the corresponding Bode diagram, and falls within the expected tolerance bands. Because only proportional control is used no overshoot is present. However, due to the lack of integrating action the final value of 1 A is not reached. The final error, however, is very small because of the steady-state feed-forward term in the controller.

The measured output current spectra for constant and modulated bias current are shown in Figure 9.14. Some spurious harmonic components appear just above the noise floor. The THD improved significantly compared to the SISO case presented in Figure 9.8. This is due to the lower sensitivity of the state-feedback controller, resulting in better noise shaping of the output. Therefore, the noise floor in Figure 9.14 is slightly higher than for the SISO case shown in Figure 9.8.

Again it should be noted that the closed-loop results of Figure 9.14 are limited by the measurement resolution of the feedback system. The next section deals with the open-loop harmonic distortion of the DB under various output conditions, and shows the true potential of the topology.

9.3 Open-loop harmonic distortion

The previous section verified the state-space averaged model and the two feedback control strategies proposed in Chapter 8. This section verifies the open-loop performance of the DB topology and compares it to the results presented in Chap-

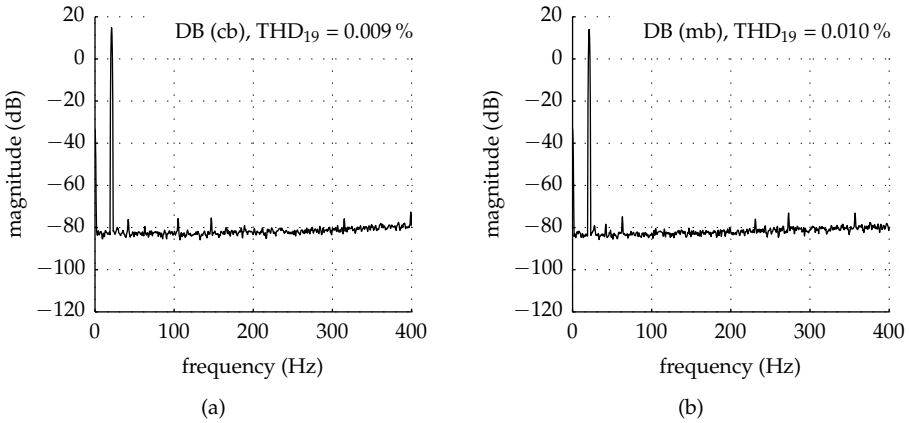


Figure 9.14: Measured output current (i_{out}) magnitude spectra for the DB , with constant bias current (a), and modulated bias (b), of the closed-loop system with the proposed state-feedback controller. A sinusoidal reference of 6 A 21 Hz was used and the offset current was set to $i_{\text{th}} = 5.5$ A.

ters 4, 6, and 7. Furthermore, the performance of the DB is compared to its conventional equivalent, the FB.

To ensure CCM and good tracking of i_{bias} for modulated bias, the SISO bias current controllers were enabled for the measurements done in this section. The bias controllers were assisted with a simple first-order feed-forward action, as given by

$$u^*_{\text{bias}} = V_{\text{bias}} + R_{\text{bias}} i^*_{\text{bias}} + L_{\text{bias}} \frac{\mathrm{d}i^*_{\text{bias}}}{\mathrm{d}t} \tag{9.1}$$

where V_{bias} was set to 2.2 V, $R_{\text{bias}} = 0.16\,\Omega$, and $L_{\text{bias}} = 400\,\mu\text{H}$.

Furthermore, to increase the PWM resolution noise shapers were implemented to dither the PWM. Figure 9.15 depicts a schematic diagram of the used noise shaper. First the voltage reference is converted to a modulation index by the $2/U_{\text{DC}}$ gain. After that the calculated modulation index is quantized to the resolution of the modulator, in this case to 12 bits. To compensate for the error due to the finite PWM resolution, at the next modulation-index update the difference (σ) is added to the new reference.

The THDs in this section are calculated using (3.1). The THD diagrams are expressed in dB, where -80 dB corresponds to a THD of 0.01 %. The harmonic dis-

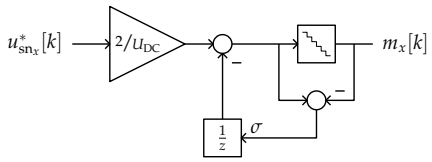


Figure 9.15: Schematic diagram of the noise shaper used to dither the PWM.

tortion (HD) of the power supply is calculated as

$$\mathrm{HD}_N = \frac{\sqrt{\sum_{n=1}^{N} \left(U_{\mathrm{DC}}(nf_o)\right)^2}}{\langle U_{\mathrm{DC}} \rangle} \tag{9.2}$$

where $\langle U_{\mathrm{DC}} \rangle$ represents the average supply voltage, in this case 100 V, and the magnitude spectrum of the power supply voltage is indicated by $U_{\mathrm{DC}}(f)$.

9.3.1 Output quality under different load and output conditions

Figure 9.16a depicts the THD evaluated over 38 harmonics as a function of output voltage reference amplitude $u^*_{\mathrm{avg}_{\mathrm{DM}}}$, for the FB, and the DB with modulated and constant bias current. In all cases the load resistance is 12.1 Ω, and the reference frequency 21 Hz, the same as for the closed-loop measurements in the previous section. The dashed line indicates the HD of the power supply as given in (9.2). It can be seen that the output spectrum of the converter is not significantly influenced by the power supply. To achieve this voltage stability the correction amplifier explained in Appendix A.2 was used.

The DB with constant bias current results in the best output quality, as was predicted in Chapter 6. The lowest THD is achieved between 30 and 40 % modulation and reaches −90 dB (0.003 %). The THD steadily grows to −70 dB for 90 % output voltage modulation, which is still exceptionally good for an open-loop switching converter. The DB with modulated bias current has a slightly lower-quality output.

The distortion of the FB increases rapidly for increasing voltage amplitudes up to 60 V, and the distortion decreases again for higher amplitudes. This is because the FB operates in the ZVS regime for voltages up to 20 V. As a result there is no blanking-time-related distortion, as explained in Section 3.4. For amplitudes higher than 60 V the distortion decreases again because the error due to blanking time becomes smaller relative the amplitude of the output voltage.

Figures 9.16b, 9.16c, and 9.16d show the corresponding output voltage spectra for 50 V amplitude. The output spectra of the DB are comparable to the simulation results given in Figure 6.13. It should be noted that different set points were used for the simulation results. Nevertheless, the outcomes confirm the validity of the simulations.

The closed-loop THD in the previous section was -70 dB for the SISO case, and -81 dB for the state feedback-controller. The reference voltage required for 6 A closed-loop output current is approximately 73 V. From Figure 9.16a it can be seen that better or similar results can be obtained without feedback control. This is because the closed-loop results are limited by the resolution of the measured states. The closed-loop system would perform significantly better if higher resolution measurements were available. However, this is not the case for the FB, which is limited by the distortion created by the conventional switching leg, as detailed in Chapter 3.

To determine the effect of higher output current the same measurements were repeated with 2.5 Ω load resistance, as depicted in Figure 9.17. From Figure 9.17a it can be seen that in this case the FB starts suffering from blanking-time-related distortion for amplitudes above 10 V. Because of the higher loading the correction could not be used. As a result the power supply plays a significant role in the distortion of the DB. Especially for constant bias current the impact of the power supply is severe.

The dominant spurious harmonic components in Figure 9.17d originate from the power supply. However, the performance of the DB with constant bias current is still impressive when considering that the setup is based on high-power 1200 V IGBTs and operated at only 100 V.

For the modulated-bias case, shown in Figure 9.17c, the first two odd harmonics can be attributed to the prototype converter, the rest is likely to originate from the power supply. When comparing the harmonic performance of the DB to the FB it can be seen that the DB performs over 100 times better for constant bias current and over 30 times better with modulated bias current.

The corresponding time waveforms for both load resistances are shown in Figures 9.18, 9.19, and 9.20 for 80 % output voltage modulation. The distortion of the output voltage and current waveforms is barely visible for the FB case and not visible for the DB cases.

9.3.2 Output quality as function of frequency

The THD as function of the reference frequency was measured using the 12.1 Ω load resistance and 50 V amplitude. Figure 9.21a depicts the resulting harmonic distortion for power-of-2 frequencies ranging from 8 to 256 Hz. Unfortunately the power supply in combination with the correction amplifier was not able to sufficiently stabilize the voltage for the higher frequencies. As a result the distortion of the DB can be attributed for a large part to the power supply. The output frequency was limited to 256 Hz because the open-loop gain peaking resulted in excessive reactive current.

The same measurement was repeated with the damping loops of the SISO control system enabled, as detailed in Section 8.3. With the damping loops active the frequency could be increased significantly. Figure 9.21b shows the measurement results with the active damping loops for frequencies up to 1024 Hz. Again the power supply was the limiting factor for the DB with constant bias current. However, the THD of the DB with constant bias current was still more than 20 dB lower than that of to the conventional FB. For modulated bias current the DB is about two times better than the FB.

It should be noted that the switching frequency of the IGBT stack was set to 16 kHz. Therefore, for higher frequencies the distortion caused by the PWM modulation starts to play a significant role too, as already explained in Chapter 3. This especially impacts the DB because of its intrinsic high-quality output.

9.3.3 Impact of bias current on output quality

In Chapter 6 the impact of the offset current (i_{th}) was investigated. It was shown that there is a trade-off between losses and output quality. Figure 9.22 depicts the THD of the DB with constant bias current as function of i_{th} with a 50 V/21 Hz reference. For $i_{\text{th}} = 0$ A the bias controller, including feed forward, was disabled. For the other cases both the controller and the feed forward were active. Figure 9.22 clearly illustrates the distortion that occurs due to DCM when i_{th} is lower than the inductor current ripple amplitudes. Continuous inductor currents occur for 3 A and higher offset current.

As explained in Chapter 6, the THD improves for higher i_{th} even when the inductor currents are continuous. This is due to the faster switching transients. For offset currents higher than 5 A the turn-off transient slew rate is limited by the gate driver, as explained in Chapter 6, and the improvement of the THD becomes

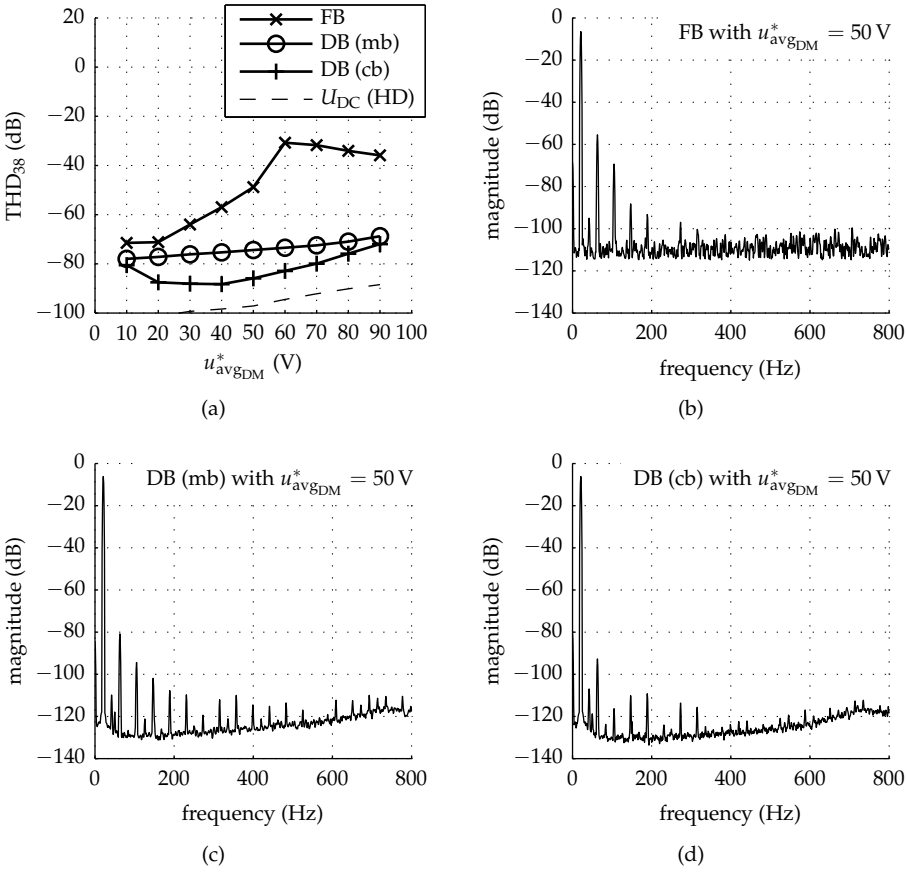


Figure 9.16: Measured HD of the output voltage (u_{out}) under open-loop conditions (a) using a 12.1 Ω load. Plots (b) to (d) show the corresponding output voltage magnitude spectra for the FB, and DB with modulated (mb) and constant (cb) bias current, respectively. The dashed line in (a) represents the HD of the power supply for the DB (cb) case, which is insignificant in this case. The markers in (a) indicate the measured points. All voltages are normalized to U_{DC}.

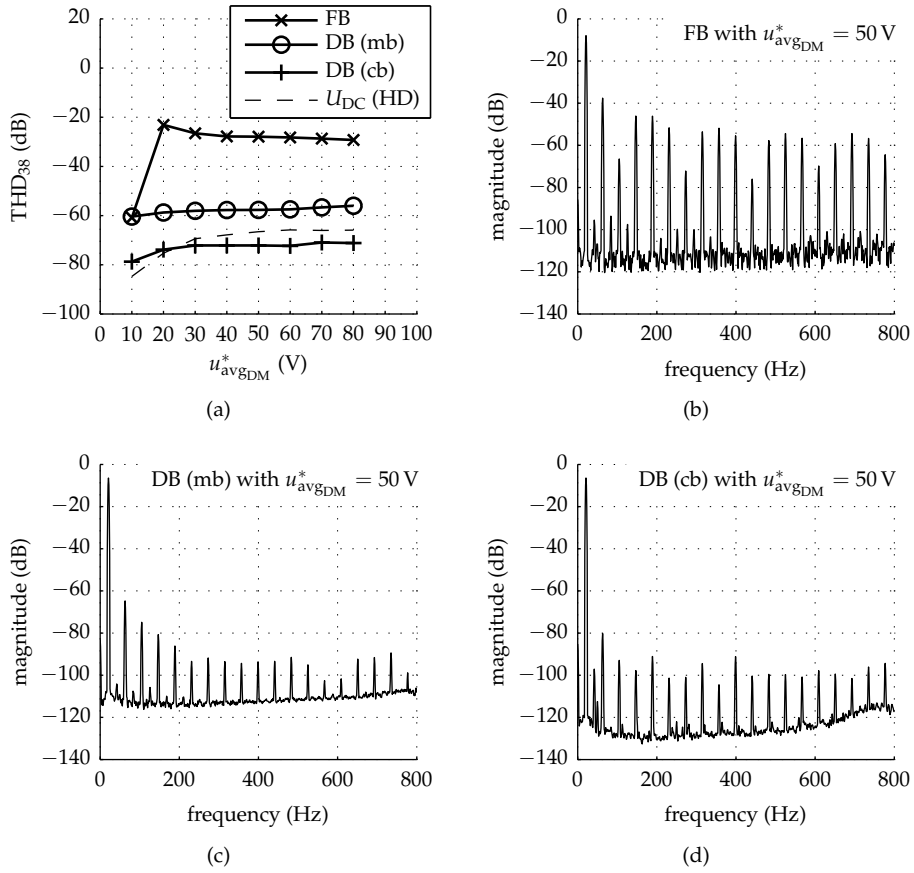


Figure 9.17: Measured HD of the output voltage (u_{out}) under open-loop conditions (a) using a 2.5 Ω load. Plots (b) to (d) show the corresponding output voltage magnitude spectra for the FB, and DB with modulated (mb) and constant (cb) bias current, respectively. The dashed line in (a) represents the HD of the power supply for the DB (cb) case. The markers in (a) indicate the measured points. All voltages are normalized to U_{DC}. It should be noted that the power supply is a significant source of distortion for the DB with constant bias current.

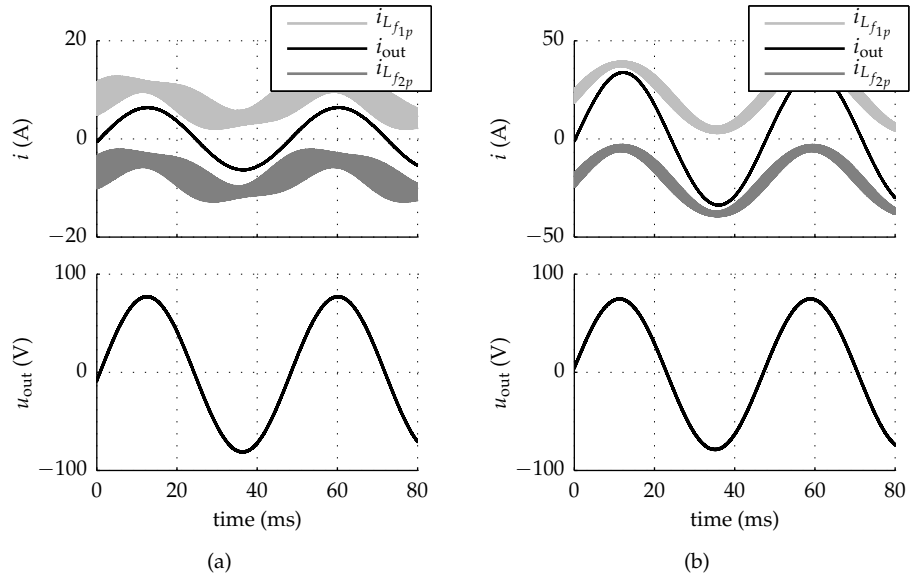


Figure 9.18: Measured waveforms with constant bias current and sinusoidal reference with 80 V amplitude and 21 Hz frequency for (a) 12.1 Ω, and (b) 2.5 Ω load resistance. The pictures correspond to the spectra shown in Figures 9.16d and 9.17d.

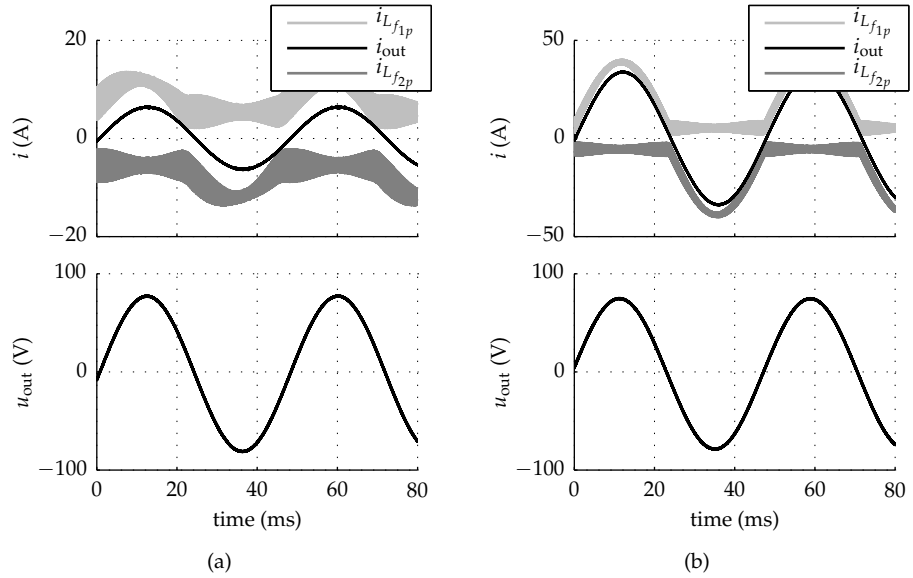


Figure 9.19: Measured waveforms with modulated bias current and sinusoidal reference with 80 V amplitude and 21 Hz frequency for (a) 12.1 Ω, and (b) 2.5 Ω load resistance. Corresponding to the spectra shown in Figures 9.16c and 9.17c.

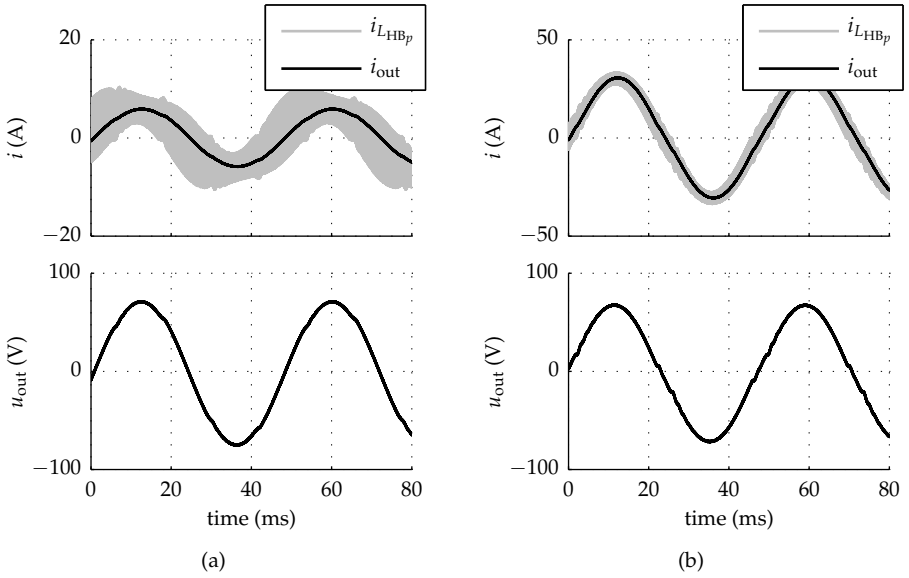


Figure 9.20: Measured waveforms for the FB with sinusoidal reference with 80 V amplitude and 21 Hz frequency for (a) 12.1 Ω, and (b) 2.5 Ω load resistance. Corresponding to the spectra shown in Figures 9.16b and 9.17b.

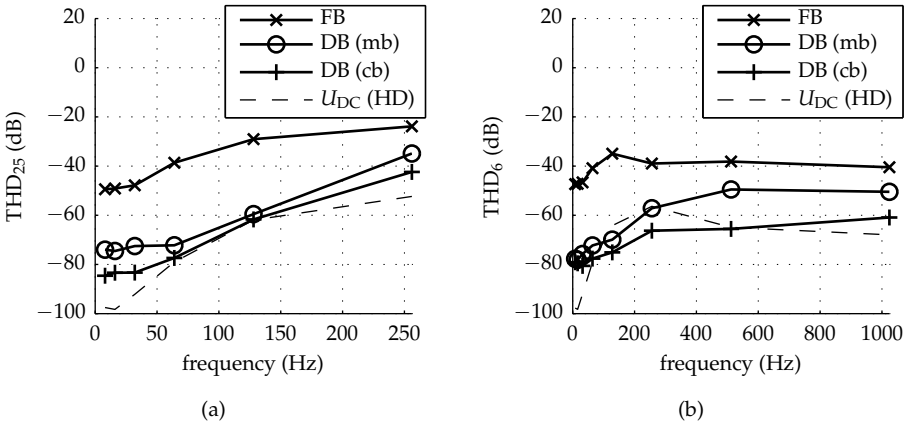


Figure 9.21: Measured output voltage THD as function of output frequency (f_o) for sinusoidal reference with $u^*_{\mathrm{avg}_{\mathrm{DM}}} = 50\,\mathrm{V}$, 21 Hz. Plot (a) shows the results without the damping loops enabled, and (b) shows the result with damping loops enabled. The bias current controller was enabled to ensure CCM, and the output quantity was not regulated. The markers indicate the measured frequencies. The dashed line indicates the HD of the power supply for the DB (cb) case, which leads to significant distortion for frequencies higher than 32 Hz.

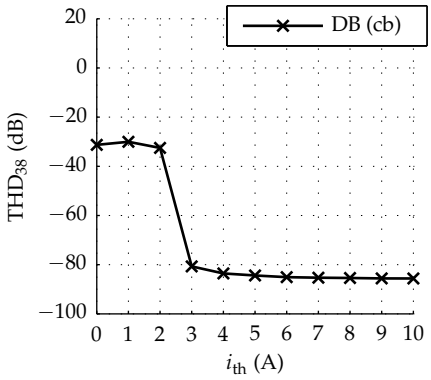


Figure 9.22: Measured open-loop output voltage THD as function of offset current i_{th} for the DB with constant bias current. For $i_{\text{th}} = 0$ the bias controllers were disabled (no bias voltage), the bias controller was enabled for the other cases. A 21 Hz sinusoidal reference was used with $u^*_{\text{avg}_{\text{DM}}} = 50\,\text{V}$.

very small. Therefore, the offset current was chosen at 5.5 A for all other measurements conducted in this chapter. As discussed in Section 6.3.3 the extra bias current required to ensure driver-limited turn-off transients results in additional losses.

When comparing Figure 9.22 with the THD of the FB in Figure 9.16a, it becomes clear that it is essential to operate the DB in CCM to achieve significantly better results than possible with a conventional FB.

The output waveforms and the corresponding output voltage spectra for $i_{\text{th}} = 0$ and 3 A are given in Figure 9.23. Figure 9.23a clearly shows that the inductor currents clamp to 0 A. The corresponding spectrum in Figure 9.23c illustrates the impact of the discontinuous currents on the output spectrum, stressing again the need of good bias current control.

9.3.4 Impact of the carrier phase shift on output quality

In Chapter 7 the impact of different PWM modulation strategies on the output voltage spectrum is investigated. However, this analysis was focused on harmonics due to switching and not on the baseband distortion of the converter stage. Figure 9.24 depicts the impact of the modulation strategy on the baseband THD for the five modulation strategies compared in Chapter 7. From Figure 9.24 it can be seen that the impact of the modulation strategy is relatively small. This was to be expected from the analysis in Chapter 6, which showed that the averaged

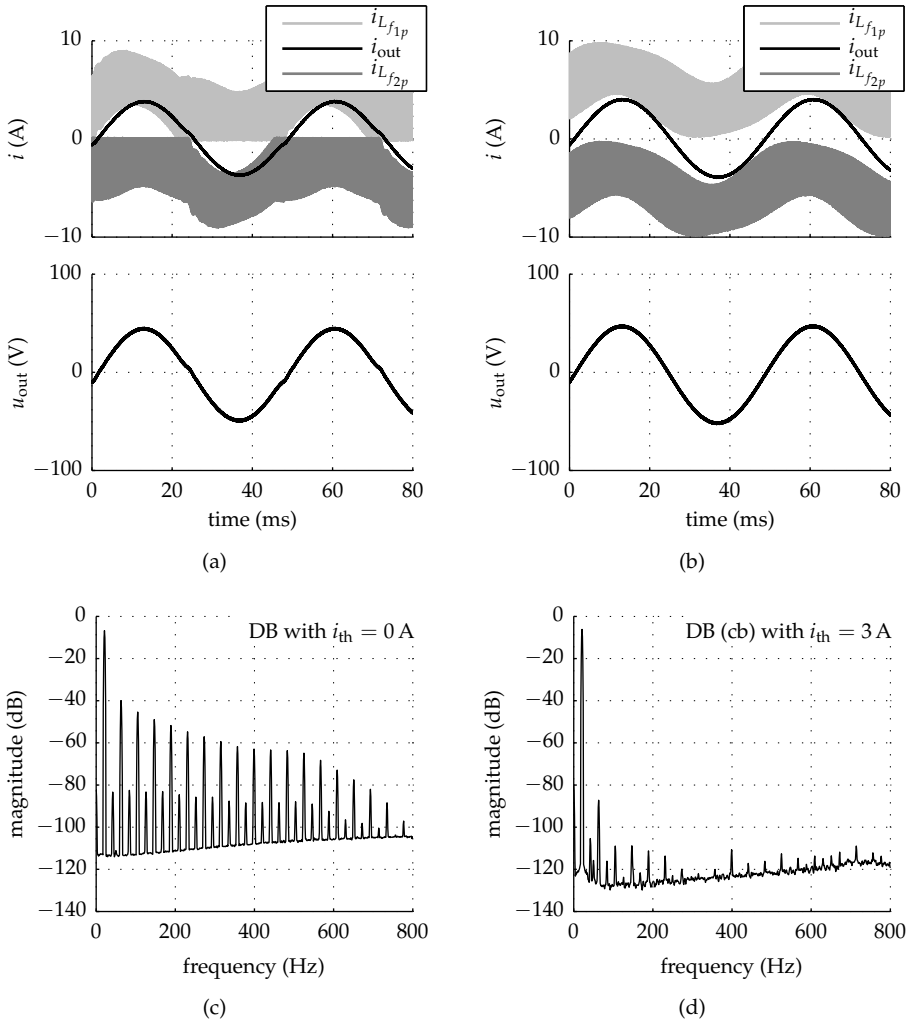


Figure 9.23: Measured waveforms (a) and (b) and their output voltage spectra (c) and (d) corresponding to the cases with $i_{\text{th}} = 0$ and $i_{\text{th}} = 3$, receptively, in Figure 9.22. The voltage spectra are normalized to U_{DC}.

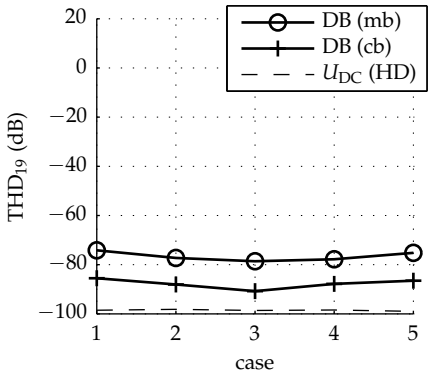


Figure 9.24: Measured open-loop output voltage THD for the five cases of PWM carrier phase shifts suggested in Chapter 7, for constant (cb) and modulated (mb) bias current. The markers indicate the measured points. The dashed line indicates the (insignificant) HD of the power supply for the DB (cb) case. All voltages are normalized to U_{DC}.

model used to evaluate the distortion does not depend on the chosen modulation strategy.

However, the best performance is achieved for *case 3*, which results in unipolar switching with zero CM voltage. Cases 2 and 4 are comparable and result in slightly higher THD compared to *case 3*. Cases 1 and 5 have the highest THD. In Chapter 7 cases 3 and 4 were suggested as the best modulation strategies. However, reducing volume by using coupled inductors, as suggested in Chapter 5, is only possible for bipolar and unipolar switching, i.e. cases 1 and 2, resulting in a trade-off between volume and output quality.

9.3.5 Intermodulation distortion

Finally, to illustrate the linearity of the DB topology the output was measured for a reference signal with two frequencies, 50 V/42 Hz, and 10 V/38 Hz. The resulting spectra for constant and modulated bias current are depicted in Figure 9.25. For constant bias current only one intermodulation harmonic can be observed at 46 Hz. However, its amplitude is almost 90 dB lower than the 42 Hz reference signal and barely visible. The other spectral components are harmonics of the reference signal.

For modulated bias current two intermodulation products are present, one at 46 Hz and another at 138 Hz. However, the intermodulation harmonics are at

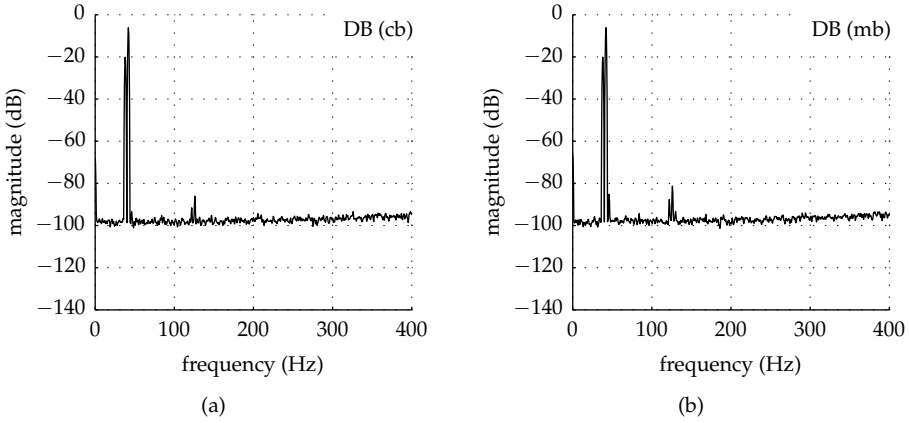


Figure 9.25: Open-loop voltage magnitude spectra for the DB with constant bias current (a) and modulated bias current (b) using a two-tone sinusoidal reference of 50 V 42 Hz and 10 V 38 Hz.

least two times lower than the other spurious harmonics of the reference signal. Figure 9.25 illustrates the high linearity that can be achieved with the DB when operated properly.

When comparing Figure 9.25 to the spectra in Figure 9.16a it can be seen that the noise floor of the experiment is higher than the other measurements in this chapter. This is because the reference was supplied externally from the analog output of the analyzer through one of the ADC inputs of the setup. The noise floor is, therefore, determined by the quantization noise of the ADC, in this case 16 effective bits. The single-frequency measurements in this chapter were made using a digitally implemented sine-wave generator in the dSPACE platform, which has a several orders of magnitude better resolution.

9.4 Summary

In this chapter the measurement results were presented. The small-signal model was verified and proved to be accurate. Two feedback control strategies as derived in Chapter 8 were tested in practice and compared to the analytical and simulation results. Furthermore, the open-loop harmonic performance was measured under different load and output conditions. It was shown that the DB is superior over the conventional FB, as expected. When operated properly, over 40 dB improvement in the open-loop output quality can be achieved compared to

the conventional FB. The DB is therefore a suitable candidate topology for high-precision power converters.

Part III

Closing

Chapter 10

Conclusions and recommendations

"I may not have gone where I intended to go, but I think I have ended up where I needed to be."

(Dirk Gently, cited by Douglas Adams)

This chapter deals with the conclusions of the thesis. The main contributions are summarized, and finally, recommendations for future work are given.

10.1 Conclusions

In Part I the different sources of distortion, present in the conventional HB, have been highlighted. Blanking time was identified as one of the most dominant sources of distortion. Over time, numerous modulation strategies, compensations, and topologies have been proposed that do not suffer from blanking-time-related distortion. All of the suggested compensations reduce the effects of blanking time, but none of them fully eliminates the effects. Topologies and modulation strategies that do not suffer from blanking-time-related distortion have either a nonlinear relation between modulation index and output, are not robust for shoot-through currents, or allow only unidirectional power flow. In [136] a topology was suggested based on unidirectional switching legs operated in parallel, also known as the dual-buck (DB) converter. This circuit does not require blanking time, is robust for shoot-through, and allows bidirectional power flow.

10.1.1 A class of robust converters

In Part II of this thesis the DB topology has been treated in detail. The following conclusions can be drawn from Chapter 4:

- When assuming ideal switches, and continuous filter inductor currents, while neglecting switching transients, the DB exhibits a linear relation between modulation index and output.
- A bias current is required to ensure continuous inductor currents, and consequently linear behavior.
- The bias current can flow between the two legs of the DB through the filter inductors, can be supplied from an auxiliary circuit as in the ABDB, or, as suggested in [50], can flow through an additional differentially connected bias inductor.
- The bias and output current and voltage quantities can be separated using a power-invariant variable transformation.
- The bias current can be changed (modulated) as function of the sum of the filter inductor currents. This reduces the losses due to the bias current by

approximately 30 %.

- When the DB is operated with continuous inductor currents, significant additional conduction losses occur compared to its conventional equivalent. It is shown that over three times higher losses occur in the inductive components, and 1.4 times higher conduction losses occur in the switching devices, even for modulated bias current. This is the major disadvantage of the DB topology.

- The DB has more losses than its conventional equivalent switching leg. However, because the integrated antiparallel diodes of the semiconductor switches are not used, the DB allows separate optimization of the discrete diodes and switches. In case of MOSFET switches, this is not possible in the conventional switching leg.

- The DB switching leg is a standard building block that can be used to replace a conventional switching leg in many topologies, as in parallel- and series-connected half- and full-bridge converters, and flying-capacitor or neutral-point-clamped multi-level converters.

Chapter 5 focuses on the selection of the inductive components. The combination of interleaved voltages and coupled inductors has been investigated with the aim to integrate the functionality of both the filter and bias current inductors in a single coupled device, while reducing the total volume. The following conclusions can be drawn from Chapter 5:

- It is shown that the area product has a minimum between 20 to 30 % inductor current ripple ratio, which is not the case for the filter inductor of the classical HB. As such, the area product can be used unmodified to determine an initial magnetic design with good volumetric properties and low additional losses in the switching devices. This is not possible for the filter inductors of the conventional HB, where the optimum area-product occurs for inductor current ripple amplitudes higher than 100 % of the output current. This can lead to excessive hysteresis losses in the inductors, which are not included in the area product *pur sang*.

- By magnetically coupling the DB filter inductors, the total magnetic volume can be reduced from approximately 2.6 times to 1.6 times the total inductive volume of the conventional HB, for modulated bias current.

- The total magnetic volume for the ABDB is comparable to that of the DB with coupled inductors.

10.1.2 Output waveform quality

Distortion is unwanted power that is transferred to the load, or in other words: a difference between the desired and the actually generated signal. The DB does not suffer from blanking-time-related distortion, however, blanking time is not the only source of switching-leg-induced distortion. The semiconductor device properties can be a significant source of output signal distortion too. Chapter 6 explained how semiconductor device characteristics affected the output waveform accuracy and quality for baseband frequencies. The following conclusions can be drawn:

- When the on-resistances of the semiconductor switches and diodes are assumed equal, ideally the relation between modulation index and the output is linear. As a result no harmonic distortion occurs when the resistances of the diodes and switches are matched.
- When the on-resistances of the semiconductor switches and diodes are not equal, using modulated bias current results in significantly more distortion than constant bias current.
- The forward voltages of the semiconductor switches and diodes do not contribute to harmonic distortion. This is not true for the conventional HB, where forward voltages can result in significant errors depending on the supply voltage.
- When the series resistances of the filter inductors are matched, there is no cross-coupling between the bias and output quantities.
- The minimum absolute current level at which a semiconductor switch is turned off can be chosen such that the switching transient slew rate is determined by the turn-off resistance of the driver. This results in less operating-point-dependent commutation speeds, and consequently less distortion.

Measurements made on an experimental setup in Chapter 9 support the conclusions above.

The switching in switched-mode power amplifiers (SMPAs) comes with a substantial amount of distortion and electromagnetic interference, however, these effects occur at higher frequencies. The harmonics of the switching frequency due to voltage commutation transients for a full-bridge-equivalent of the DB and ABDB are detailed in Chapter 7. The following conclusions can be drawn:

- With respect to conventional converters the DB features more interleaving flexibility. However, care should be taken when significant bias voltage is

required, since it adds additional harmonics of the switching frequency to the output voltage, depending on the interleaving strategy.

- For bipolar and unipolar switching, the bias voltage has a positive effect on the DB output voltage spectra.
- With the DB it is possible to achieve 3-level PWM with doubled output ripple frequency and a constant, or nearly perfect, CM voltage at the output of the converter. That is to say, the best features of both unipolar and bipolar switching can be retained.
- For the ABDB, bias voltage has no influence on the output spectra, thus no concessions need to be made in that respect.
- The ABDB is functionally equivalent to a conventional interleaved converter.

10.1.3 Modeling, feedback control, and verification

In Chapter 8 a small-signal model for the full-bridge-equivalent DB has been given. Two feedback control strategies have been proposed. One strategy is based on decoupled single-input single-output controllers that are often used in industry. The second method is based on full state-feedback with its dynamics chosen such that the closed-loop system behaves like a Bessel-filter prototype. The model and both controllers were verified with measurements in Chapter 9. The following conclusions can be drawn for the modeling and SISO control system.

- It has been shown that ideally the output current and bias current are perfectly decoupled. Even in the presence of considerable component variation this decoupling is sufficient to achieve excellent regulation of the output current.
- Two decoupled damping loops are applied, one for the DM, and one for the CM resonances of the output filter. It is shown that the amount of damping can be set separately for both resonances, without the concessions which are normally made when the damping loops are not decoupled. This leads to more freedom for the design of the output current controller that only acts on the DM voltage across the load.

For the full-state-feedback control system it was shown that:

- By placing the dominant closed-loop poles according to a Bessel prototype system, and compensation of the closed-loop zeros, a constant group delay

can be obtained over a broad frequency range. Consequently, the resulting step response has nearly no overshoot.

The experimental results in Chapter 9 verified the small-signal model and feedback controllers given in Chapter 8. Moreover, they have confirmed the superior output waveform quality of the DB. It was shown that, compared to the conventional FB, over 40 dB improvement of the THD can be obtained under open-loop conditions. Also the intermodulation distortion was measured to be negligible, i.e. the intermodulation products were more than 90 dB lower than the reference amplitude for constant bias current.

10.2 Scientific contributions

The scientific contributions of this thesis can be summarized as:

- Variable transformations are proposed that separate the output quantity of the DB from the bias current required for high-quality output. The variable transformations allow separate analysis and control of the output and bias quantities.
- Methods to reduce the volume of passive components in a DB are investigated and compared to existing studies.
- The state-space averaging method is applied to develop a model of the DB that predicts steady-state error contributions of the different circuit parameters for continuous inductor currents.
- Multiple PWM modulation strategies for the DB are compared. The effects of bias voltage on the output of the converter are analyzed and verified with measurements.
- Feedback strategies are proposed that allow separate control of the output quantity and bias current. Furthermore, a procedure is given to design closed-loop systems with Bessel-filter prototype dynamics, i.e. a constant group delay. Both methods are verified with measurements.
- Experimental verification of the DB topology on a high-power IGBT stack that by no means is intended for generating high-quality output. The experimental results have shown that, even without feedback control, excellent signal quality can be obtained.

The results of this research have been published in journals and presented at conferences, as listed below:

- J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. A. Lomonova, "High precision switched-mode amplifier with an auxiliary bias circuit," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Volume reduction of opposed current converters through coupling of inductors and interleaved switching," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 852–857.

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Harmonics in opposed current converters," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 439–445.

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Elimination of zero-crossing distortion for high-precision amplifiers," in *Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2011, pp. 3370–3375.

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "High-precision current control through opposed current converters," in *Proceedings of the 14th European conference on Power Electronics and applications (EPE)*, 2011, pp. 1–10.

Other contributions made during this research are:

- E. Lemmen, J. M. Schellekens, C. G. E. Wijnands, and J. L. Duarte, "The extra L opposed current converter," in *Proceedings of the 29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 1304–1311.

- V. Spinu, J. M. Schellekens, M. Lazar, and M. A. M. Hendrix, "On real-time optimal control of high-precision switching amplifiers," in *Proceedings of the 17th International Conference on System Theory, Control and Computing (ICSTCC)*, 2013.

- M. L. A. Caris, H. Huisman, J. M. Schellekens, and J. L. Duarte, "Generalized harmonic elimination method for interleaved power amplifiers," in *Proceedings of the 38th annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 4961–4966.

- J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Fast-shared current transient response in high-precision interleaved inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3308–3317, 2011.

- J. M. Schellekens, R. A. M. Bierbooms, and J. L. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *Proceedings of the XIXth International Conference on Electrical Machines (ICEM)*, 2010, pp. 1–6.
- J. M. Schellekens, J. L. Duarte, M. A. M. Hendrix, and H. Huisman, "Interleaved switching of parallel ZVS hysteresis current controlled inverters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE Asia)*, 2010, pp. 2822–2829.
- J. M. Schellekens, J. L. Duarte, and M. A. M. Hendrix, "Interleaved switching of parallel ZVS hysteresis current controlled inverters," in *Proceedings of the 5th IEEE Young Researchers Symposium (YRS)*, 2010.

10.3 Recommendations for future work

This thesis proposes a non-conventional converter topology together with modulation and control strategies that significantly improve output waveform quality. Experimental results showed a 20 to 40 dB improvement of THD compared to converters based on conventional switching legs. However, for lithographic equipment the smallest feature size that it can print on a wafer is halving roughly every three years, as predicted by Moore's law. Simultaneously, the throughput of lithographic equipment has been increasing over time, roughly doubling every five years. As a result the dynamic range of power amplifiers used to position the wafers in lithographic machines needs to increase too.

Assuming that the current required for accelerating the wafer stage increases with the square of the throughput, and the current error allowed for the positioning accuracy decreases with the feature size, it can be shown that the dynamic range of the power amplifiers needs to increase with roughly 20 dB every five years. Similar trends can also be observed in medical imaging, where both the resolution and frame rates are increasing over time. Therefore, to keep up with the demands from industry, continuous research is required on power amplifiers for high-precision equipment.

Even though very good experimental results have been obtained, there is still room to further improve and extend this research.

The investigation of the output quality of the DB focused on first-order effects. A next step towards even better waveform quality would require to include nonlinear effects like saturation of the filter inductors, exponential behavior of semi-

conductors, and the influence of temperature. Better understanding of the effects of the switching transients on the signal quality, including the effects of reverse recovery of diodes and voltage dependency of the parasitic capacitances of the semiconductors, would be welcome. All these effects were neglected in this work.

The recommendations so far focused on the converter stage. However, the employed closed-loop control strategy can also influence output waveform quality. Chapter 8 highlights the effects of sampling of the measured states for feedback on the accuracy of the closed-loop system. Sampled signals are often also amplitude quantized. There are studies on the effects of quantization due to DPWM and analog-to-digital conversion of the measured states, like [81] and [128]. However, a detailed analysis of the influence of sampling and quantization on the output signal quality under closed-loop conditions still needs to be done.

In Chapter 9 it is stated that the closed-loop output waveform quality was limited by the resolution of the measurements. The output signal quality under closed-loop conditions was not investigated in this thesis and the measurement results were only included for reference. However, it would be interesting to determine the maximum signal quality that can be obtained with the DB topology under closed-loop conditions, given that the measurements are not the limiting factor.

In Chapter 3 the power supply is identified as a potentially significant source of distortion. For many of the experimental results in Chapter 9 the power supply was indeed the limiting factor. Nevertheless, the results were still very good. However, the maximum output waveform quality that can be obtained by the DB for the experimental results where the power supply was the limiting factor still needs to be determined.

In Chapter 3 a method to compensate for the power supply distortion is explained and an alternative method referred to in the literature was mentioned. However, both these methods have limitations. More research on compensation of the effects of the power supply is important to further improve the output quality.

In Chapter 4, modulating the bias current is proposed to decrease losses. The suggested method is based on a fixed offset current i_{th}. Making the offset current operating-point-dependent will result in even lower losses. This is, however, not detailed in this thesis.

Conduction losses in the passive components and inductor volume of the DB are compared to its conventional equivalent in Chapters 4 and 5, respectively. It is shown that when scaling the DB to the conventional HB losses and/or volume will increase significantly. No design optimization was conducted in this thesis when comparing the DB and HB with respect to losses and total volume. Such a

comparison would lead to valuable information about the competitiveness of the DB. It should be noted that for an honest comparison the conventional converter should have similar output waveform quality.

Appendices

Appendix A

Experimental setups

This appendix describes the experimental setups that are used to generate the measurement results in this thesis. First the power electronic inverter is described that is used in the setups in Section A.1. After that the control platform and PWM generation is detailed in Section A.3. Finally, per chapter, details are given of the different experiments.

A.1 IGBT stack and gate drivers

The setups used for the measurements are based on an off-the-shelve two phase Semikron SEMISTACK SKS40FB2C07V6 inverter, as depicted in Figure A.1. Each phase consists of three parallel connected Semikron SKM-75-GB-123D IGBT modules and a Semikron SKHI-22-A gate driver. The power supply is decoupled with 3 mF bus capacitance consisting of six parallel strings of two series connected 400 V 1000 µF Rifa PEH200VH410AMB3 electrolytic capacitors. Each IGBT module has a 470 nF local film capacitor across its DC voltage terminals. The inverter module is designed for a maximum DC bus voltage of 690 V and each leg is capable of delivering 180 A, totaling to 124 kW maximum instantaneous output power.

To amplify the distortion due to the forward voltage drops across the IGBTs and

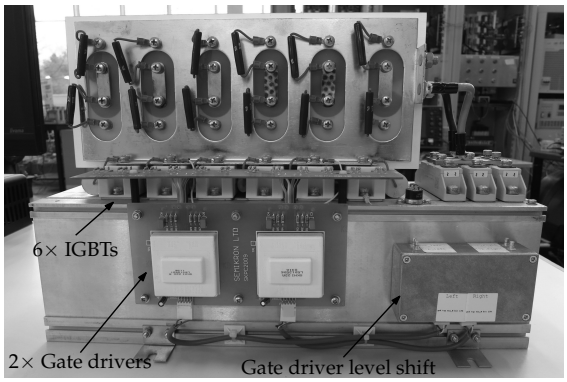


Figure A.1: Two phase inverter with two sets of three parallel connected Semikron SKM-75-GB-123D IGBT modules and two two-channel Semikron SKHI-22-A gate drivers.

integrated diodes all measurements were done using 100 V DC bus voltage. The maximum output current capability depends on the used inductors and is in the range of 20 to 40 A. This totals to 4 kW maximum instantaneous output power, which is only a small fraction of the maximum power capability of the off-the-shelve inverter. The DC supply voltage is generated by a Delta Elektronika SM 6000 series 120 V 50 A power supply.

Initially two of these inverters were used as a reconfigurable setup that could be used as a conventional full bridge converter and a full-bridge equivalent of a DB. Only one IGBT per leg was actively driven. For the P-cells only the top switch was driven and for the N-cells the bottom switch was actively driven. In conventional full bridge mode the switch nodes of the P- and N-cells of each DB leg were connected.

Only the measurements in Chapter 7 were made with this initial setup. The Semikron SKHI-22-A gate drivers have an internal 8 MHz clock, which is asynchronous to the clock of the PWM generator, which in turn is discussed in the next section. The clock of the gate drivers severely limited the resolution of the PWM generation. Moreover, because it was asynchronous to the PWM clock it resulted in significant distortion due to aliasing.

To increase the resolution of the PWM generation and prevent aliasing the clocked Semikron drivers were replaced by Concept 2SC042ST2C0-17 gate drivers. These drivers are not clocked and have less than 3 ns jitter, which is more than three times better than the PWM resolution. Furthermore, because each IGBT module has sufficient current capability for the setups, the parallel connected IGBTs of

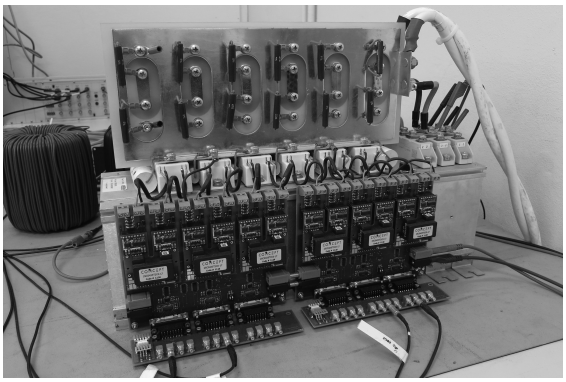


Figure A.2: Six phase inverter with six Semikron SKM-75-GB-123D IGBT modules and six two-channel Concept 2SC042ST2C0-17 gate drivers.

the Semikron inverter were separated. Figure A.2 depicts the resulting six phase inverter with the custom designed driver interface board.

All experiments, except those in Chapter 7, are based on the six phase inverter depicted in Figure A.2. Only one switch was actively driven of each module. In case of a P-cell only the top switch was used and in case of an N-cell only the bottom switch was used. For the conventional FB case the switch nodes of the sets of P- and N-cells of each DB leg were connected.

A.2 Series compensation amplifier

The Delta Elektronika power supply has under certain conditions trouble to sufficiently stabilize the supply voltage of the experimental setup. Therefore, for the measurements described in Chapter 9 a low-power linear amplifier was used to stabilize the DC power supply. Figure A.3 illustrates the schematic overview of the power-supply compensation. A linear correction amplifier (A_c) is connected in series with the DC power-supply, as suggested in [135]. The correction amplifier regulates it output (u_c) such that the voltage across the DC bus capacitors of the IGBT stack of the setup equals U_{DC}.

The DC bus voltage is measured differentially and compared to a precise reference voltage, in the correction amplifier. The linear correction amplifier compensates both the voltage drop due to the finite output impedance of the power supply (Z_{DC}, and the voltage drop due to the wire impedance (Z_w). The correction amplifier is supplied from a single isolated 10 V supply, therefore, the power supply

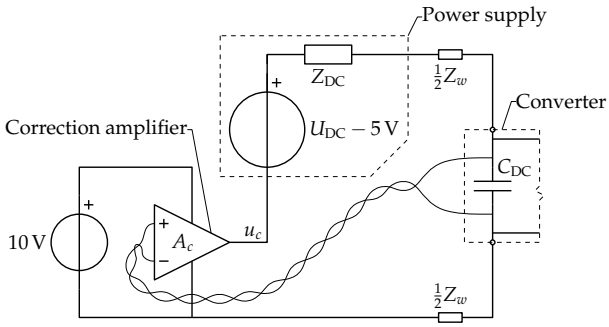


Figure A.3: Schematic overview of the series compensation of the DC power supply.

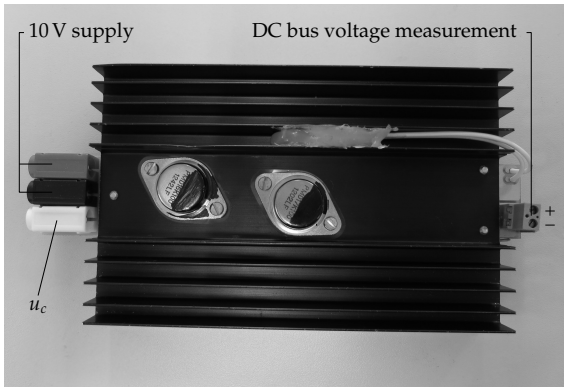


Figure A.4: Picture of the linear amplifier used for series compensation of the DC power supply.

voltage is set 5 V lower than U_{DC}. The supply voltage used for the measurements is 100 V as a result the correction amplifier has to supply approximately 5 % of the power delivered to the setup.

Figure A.4 depicts the linear correction amplifier. It basically consists of an operational amplifier in series with a class-B Darlington end stage. The transistors of the setup can handle a continuous current of 20 A, however, the heat sink is designed for approximately 10 A continuous current. The amplifier can be short term overloaded to 40 A. The voltage stability of the DC-bus is improved 20 dB by the series voltage compensation, which was sufficient for the measurements described in Chapter 9.

A.3 PWM generation, measurement and control

The configurable PWM generators are implemented in a dSPACE DS5203 FPGA board. The FPGA has a clock frequency of 100 MHz resulting in 10 ns PWM resolution. Each PWM generator consists of a triangular carrier generator, based on a simple up-down counter, and a comparator that compares the modulation index with the carrier signal. The frequency and phase shift of the triangular carriers can be set arbitrary with 10 ns resolution and the modulation index can be updated once (symmetrical triangular carrier PWM) or twice (asymmetrical triangular carrier PWM) per period. The modulation index updates normally occur when the carrier reaches its maximum value for symmetrical PWM, or its maximum and minimum value for asymmetrical PWM. Simultaneously with the update of the modulation indeces, a trigger pulse is generated that performs a sample and hold on all ADC channels. However, if desired, also a phase shift can be added to the trigger pulse to compensate for delay in the gate drivers.

The sampling of the measured signals is done by a dSPACE DS2004 high-speed 16 channel 16 bit analog to digital conversion board. The input voltage range of the ADCs is configurable to 5 or 10 V. When the conversion is finished an interrupt is generated on the dSPACE DS1006 processor board. The digital controller, implemented on the processor board, is executed each time the interrupt is triggered, and calculates new modulation indexes, which are transferred to the PWM generators implemented in the FPGA.

Next to the controller also a sinusoidal reference generator is implemented on the processor board, which is also executed synchronously with the controller. However, also an ADC channel can be used to supply an external reference signal if desired. Because reference generation, measurement, and control are all triggered from the PWM generator no aliasing occurs due to mismatch between the clocks of the different boards in the modular dSPACE system.

For feedback purposes only currents are measured. The voltages are estimated with a reduced order observer when necessary for the feedback, as described in Chapter 8. For the output current measurement LEM Ultrastab IT 200-S flux-gate sensors are used in combination with a 5 Ω shunt resistor. The filter inductor currents are measured with LEM Ultrastab IT 60-S sensors with 10 Ω shunt resistors. The current sensors are connected to the ADCs through a Signaltec multi-channel transducer system.

A.4 Details of the setups used in Chapter 5

In Chapter 5 the relative inductor volumes of the DB an ABDB are compared to the conventional HB. For the DB a set of separate and a set of coupled toroidal inductors were constructed with a distributed air-gap core. For the ABDB air-cored toroidal filter- and auxiliary-inductors were made. Simulated waveforms were compared to measurements done on the experimental setups discussed in this section.

Three experimental setups were made based on a full-bridge topology. The right legs of the full-bridges were operated in CCM and such that $u_{C_{fn}} = \frac{1}{2}U_{\mathrm{DC}}$. Measurements were taken from the left sides of the full-bridges, the voltages were measured referenced to $\frac{1}{2}U_{\mathrm{DC}}$.

The experiments were conducted with 10 kHz switching frequency (f_{sw}) and at a supply voltage (U_{DC}) of 100 V. Furthermore, the setups were loaded with a 2.5 Ω resistor R, and the filter capacitors C_f were chosen 100 µF. The right side filter inductors have no magnetic core which leads to the highest linearity. The specifications of the right side filter inductors are given in Table A.1. The air cored inductors are wound with flexible electrical (building) wire, because the relatively thick insulation helps to keep the parasitic capacitance low, and consequently the resonance frequency high.

Figures A.5a and A.6a depict the schematic overview and a picture of the DB setup with separate inductors. The specifications of the separate inductors are given in Table A.2. Figures A.5b and A.6b depict the schematic overview and a picture of the DB setup with separate inductors. The specifications of the separate inductors are given in Table A.2.

The filter inductors for both the separate and coupled case are based on a toroidal magnetic core with a distributed air-gap. The inductance was chosen such that $\lambda_{L_f} = 0.15$ with $\hat{i}_{\mathrm{out}} = 40\,\mathrm{A}$, as already pointed out in Chapter 5. The output current was set to 10 A using the feed-forward equations (6.36) and (6.37), where $V_{\mathrm{on}} = V_f = 1.2\,\mathrm{V}$, $R_{\mathrm{on}} = R_f = 0\,\Omega$, $R_{L_f} = 15\,\mathrm{m}\Omega$, and $R = 2.6\,\Omega$. Figure 7.2a depicts a full-bridge equivalent PWM modulator for the DB. The offset current i_{th} was chosen 8.9 A.

The schematic diagram and picture of the ABDB setup are depicted in figures A.5c and A.6c. Since the filter inductors (L_f) are air-cored also air-cored auxiliary inductors were constructed. The specification of the filter- and auxiliary-inductors (L_f & L_a) are given in Table A.1.

The voltage references were calculated using (6.36) and (5.41), where $V_{\mathrm{on}} = V_f =$

Table A.1: Inductor specifications of L_f and L_a. The core is a non-magnetic not conducting 120 mm diameter hollow cylinder with a 75 mm diameter center hole. To simplify the winding process a gap was made in the wall of the cylinder.

	L_f	L_a
Number of turns	202	92
Inductance L_{f_s}	800 µH	42 µH
Resistance $R_{L_{fs}}$	500 mΩ	81 mΩ
Core's height	120 mm	41 mm
Core's cross section	5400 mm^2	1845 mm^2
Core's relative permeability	1	
Core's effective length	613 mm	
Wire's cross sectional area	2.5 mm^2	
Maximum current	20 A	

Table A.2: Inductor specifications of L_{f_s} and L_{f_c}. The magnetic core was ordered from Magnetics inc., the core material is XFlux, and the order number is 0078737A7.

	L_{f_s}	L_{f_c}
Coupling factor	-	0.71
Number of turns	32	23
Inductance L_{f_s}	206 µH	129 µH
Resistance $R_{L_{fs}}$	17 mΩ	14 mΩ
Core's relative permeability	60	
Core's effective cross section	497 mm^2	
Core's effective length	184 mm	
Wire's diameter per strand	0.28 mm	
Wire's number of strands	100	
Maximum current	40 A	

1.2 V, $R_{\text{on}} = R_f = 0\,\Omega$, $R_{L_f} = 15\,\text{m}\Omega$, and $R = 2.6\,\Omega$. To compensate for the voltage drop across the switches the following correction term was applied $u^*_{\text{diff}} = V_{\text{on}} + V_f + (R_{\text{on}} + R_f)i_{\text{out}}$. Figure 7.14 depicts a full-bridge equivalent PWM modulator for the ABDB. The offset current i'_{th} was chosen 9.5 A.

A.5 Details of the setup used in Chapter 7

The measurements results in Chapter 7 are collected using the initial DB setup with two two-phase inverters as described in the beginning of this appendix, and depicted in Figure A.7. The full-bridge equivalent DB set-up used the air-cored filter inductors (L_f), as detailed in Table A.1.

The experiments were conducted with 10 kHz switching frequency (f_{sw}) and at a supply voltage (U_{DC}) of 100 V. Furthermore, the filter capacitors C_f were chosen 100 µF, and to limit the output current the setup was loaded with a 100 Ω resistor R. The bias voltage was set to 5 % of U_{DC} and the output voltage reference ($u^*_{\text{avg}_{\text{DM}}}$) was set to $0.75U_{\text{DC}} \sin(\pi 200t)$. Figure 7.2a depicts the corresponding full-bridge equivalent PWM modulator for the DB.

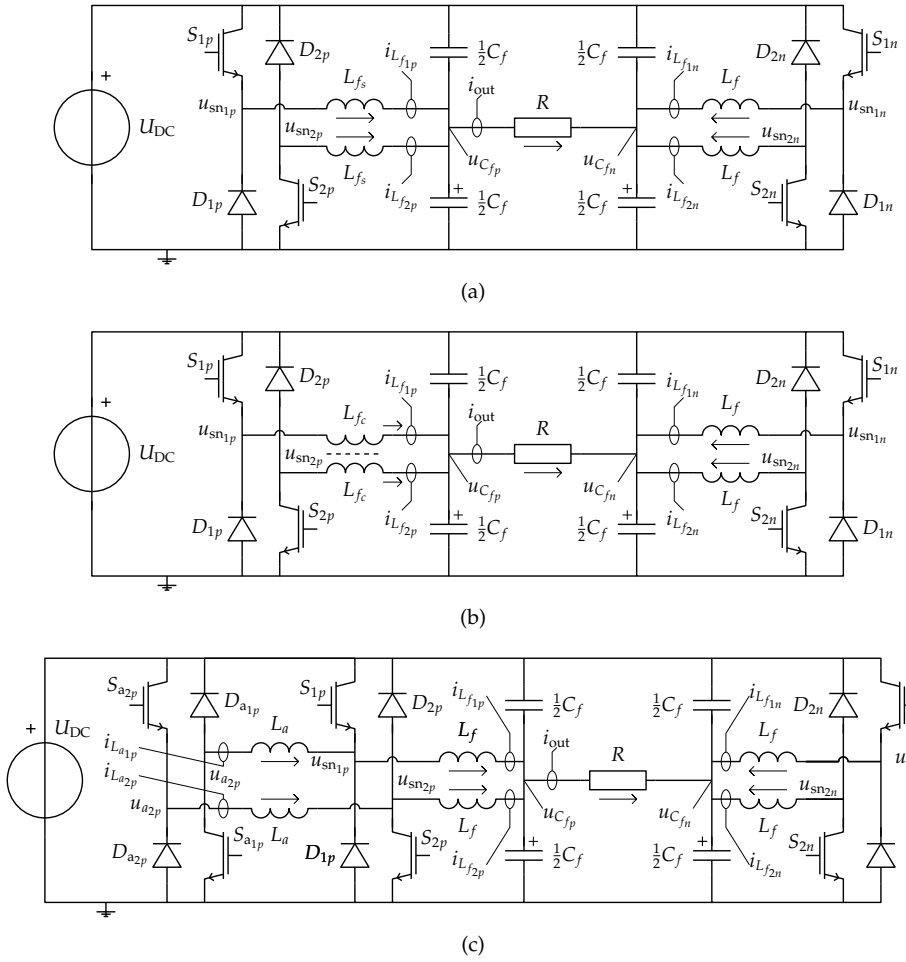
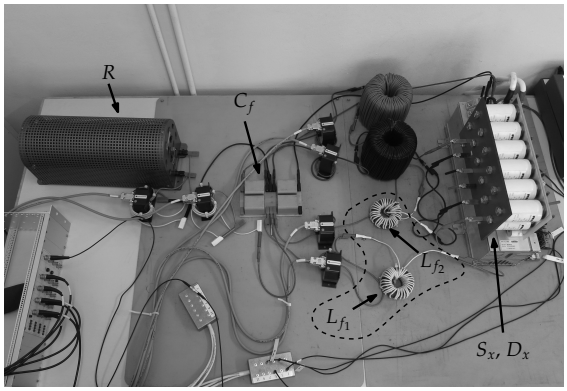
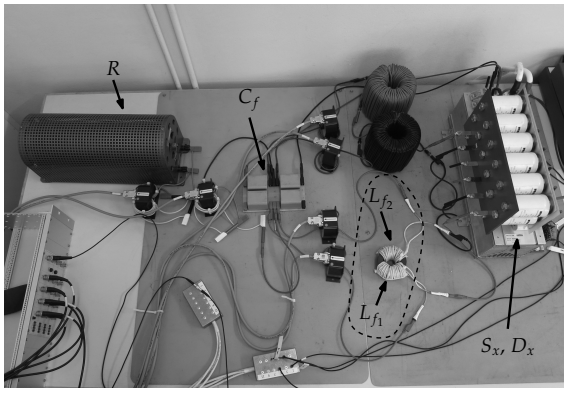


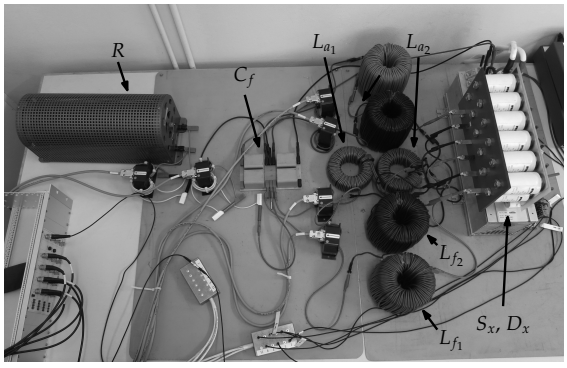
Figure A.5: Schematic of (a) the DB setup with the separate inductors, (b) the DB setup with the coupled inductors, and (c) the ABDB setup with the auxiliary inductors, as described in Chapter 5.



(a)



(b)



(c)

Figure A.6: Picture of (a) the DB setup with the separate inductors, (b) the DB setup with the coupled inductors, and (c) the ABDB setup with the auxiliary inductors, as described in Chapter 5.

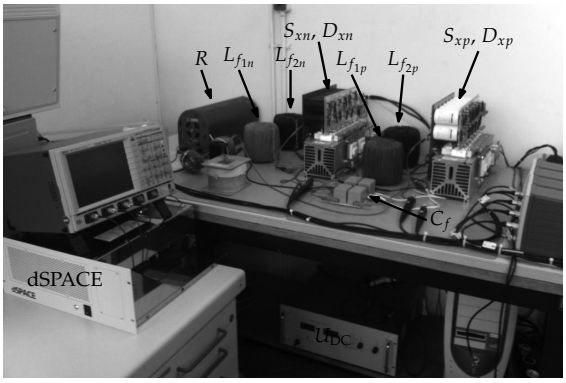


Figure A.7: Experimental DB setup with the auxiliary inductors used in Chapter 7.

Appendix B

Removing superfluous states

B.1 Example 1, removing superfluous inductor currents

The first example involves the elimination of two superfluous states. Figure B.1 depicts a FB interleaved converter, with three parallel switching legs on each side of the converter. Just from counting the storage elements one might think that this circuit has 7 states. However, due to Kirchhoff's current law applied to the two nodes marked with u_p and u_n, the current in two of the inductors cannot be chosen freely, resulting in 5 actual states.

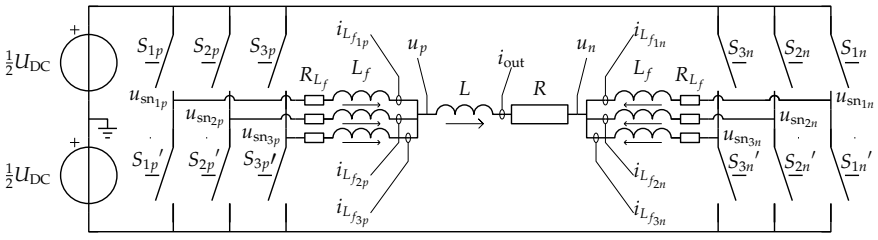


Figure B.1: Schematic overview of a FB converter consisting of six parallel converters coupled with inductors. The seven inductors present in the circuit result form two nodes, resulting in five actual states instead of seven.

Determining state-space equations without constraints for such a system is labor intensive. A common engineering solution to prevent such constraints is to add capacitors and/or resistances, to the circuit to fix the potential on nodes u_p and u_n. The added components are normally chosen such that the currents due the added components have negligible effect on the system dynamics. Doing so adds complexity since the actual number of states, after the change to the circuit, is ≥ 7. Moreover, the added components have a negative effect on the accuracy of the model, and often produce a stiff system that is hard to simulate. The procedure in this section yields explicit solutions for the voltages on the nodes that need to be removed, and reduces the number of states in the example to five.

Without loss of generality, let's first assume ideal switches and no blanking time. As a result the average behavior of the switching legs can be modeled using six controlled voltage sources $\langle u_{\mathrm{sn}_x}(t)\rangle$ [67], where for clarity the indication of time and the averaging operator are omitted from hereon. First, the two unknown node voltages are added to the input vector, resulting in

$$\begin{aligned}\mathbf{u}_d &= \begin{pmatrix}\mathbf{u}_s & \mathbf{u}\end{pmatrix}^\mathsf{T} \\ &= \begin{pmatrix}u_p & u_n & u_{\mathrm{sn}_{1p}} & u_{\mathrm{sn}_{2p}} & u_{\mathrm{sn}_{3p}} & u_{\mathrm{sn}_{1n}} & u_{\mathrm{sn}_{2n}} & u_{\mathrm{sn}_{3n}}\end{pmatrix}^\mathsf{T}.\end{aligned} \tag{B.1}$$

Next the state vector is chosen as

$$\begin{aligned}\mathbf{x}_d &= \begin{pmatrix}\mathbf{x}_s & \mathbf{x}\end{pmatrix}^\mathsf{T} \\ &= \begin{pmatrix}i_{\mathrm{out}} & i_{L_{f_{1p}}} & i_{L_{f_{2p}}} & i_{L_{f_{3p}}} & i_{L_{f_{1n}}} & i_{L_{f_{2n}}} & i_{L_{f_{3n}}}\end{pmatrix}^\mathsf{T}\end{aligned} \tag{B.2}$$

where the first two elements will be removed from the state vector. It should be noted that by changing the state order other inductor currents can be removed from the state vector. However, the nodes u_p and u_n should be connected to at least one state that is going to be removed from the state vector.

To show the effectiveness of the approach, all states in $\mathbf{x}_d$, and the node voltages u_p and u_n are chosen as outputs of the model, resulting in

$$\mathbf{y} = \begin{pmatrix}u_p \\ u_n \\ \mathbf{x}_d\end{pmatrix}. \tag{B.3}$$

Given the model depicted in Figure B.1 and the chosen state and input vector the

state-space matrices become

$$\mathbf{A}_d = \operatorname{diag}\left(-\frac{R}{L}, -\frac{R_{L_f}}{L_f}, -\frac{R_{L_f}}{L_f}, -\frac{R_{L_f}}{L_f}, -\frac{R_{L_f}}{L_f}, -\frac{R_{L_f}}{L_f}, -\frac{R_{L_f}}{L_f}\right) \tag{B.4a}$$

$$\mathbf{B}_d = \begin{pmatrix} \frac{1}{L} & -\frac{1}{L} & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & \frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & \frac{1}{L_f} & 0 & 0 & 0 & 0 \\ -\frac{1}{L_f} & 0 & 0 & 0 & \frac{1}{L_f} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & \frac{1}{L_f} & 0 & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{L_f} & 0 & 0 & 0 & 0 & 0 & \frac{1}{L_f} \end{pmatrix} \tag{B.4b}$$

$$\mathbf{C}_d = \begin{pmatrix} \mathbf{0}^{2\times 7} \\ \mathbf{I}^7 \end{pmatrix} \tag{B.4c}$$

$$\mathbf{D}_d = \begin{pmatrix} \mathbf{I}^2 & \mathbf{0}^{2\times 6} \\ \mathbf{0}^{7\times 2} & \mathbf{0}^{7\times 6} \end{pmatrix} \tag{B.4d}$$

where $\mathbf{I}^n$ represents an $n \times n$ and identity matrix, and $\mathbf{0}^{n\times m}$ an $n \times m$ zero matrix respectively.

Two Kirchhoff current law equations that apply to the dependent states can be deduced, which results in the following matrix

$$\mathbf{K} = \begin{pmatrix} -1 & 1 & 1 & 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & -1 & -1 & -1 \end{pmatrix}. \tag{B.5}$$

To reduce the number of states a basis of the null-space of $\mathbf{K}$ is required. In this case the rational basis using Gaussian elimination is chosen since it preserves the

states $\mathbf{x}$ in $\mathbf{x}_d$. The resulting transformation matrix $\mathbf{G}$ is given by

$$\mathbf{G} = \begin{pmatrix} 0 & 0 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}. \tag{B.6}$$

Using (2.10) the reduced state-space representation of Example 1 becomes

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{B.7a}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{B.7b}$$

with

$$\mathbf{x} = \begin{pmatrix} i_{L_{f_{2p}}} & i_{L_{f_{3p}}} & i_{L_{f_{1n}}} & i_{L_{f_{2n}}} & i_{L_{f_{3n}}} \end{pmatrix}^\mathsf{T} \tag{B.7c}$$

$$\mathbf{u} = \begin{pmatrix} u_{\mathrm{sn}_{1p}} & u_{\mathrm{sn}_{2p}} & u_{\mathrm{sn}_{3p}} & u_{\mathrm{sn}_{1n}} & u_{\mathrm{sn}_{2n}} & u_{\mathrm{sn}_{3n}} \end{pmatrix}^\mathsf{T} \tag{B.7d}$$

and where the state-space matrices are given by

$$\mathbf{A} = \begin{pmatrix} -\frac{R_{L_f}}{L_f} & 0 & a_1 & a_1 & a_1 \\ 0 & -\frac{R_{L_f}}{L_f} & a_1 & a_1 & a_1 \\ 0 & 0 & a_2 & a_1 & a_1 \\ 0 & 0 & a_1 & a_2 & a_1 \\ 0 & 0 & a_1 & a_1 & a_2 \end{pmatrix} \tag{B.8a}$$

$$\mathbf{B} = \begin{pmatrix} b_2 & b_3 & b_2 & -b_1 & -b_1 & -b_1 \\ b_2 & b_2 & b_3 & -b_1 & -b_1 & -b_1 \\ -b_1 & -b_1 & -b_1 & b_3 & b_2 & b_2 \\ -b_1 & -b_1 & -b_1 & b_2 & b_3 & b_2 \\ -b_1 & -b_1 & -b_1 & b_2 & b_2 & b_3 \end{pmatrix} \tag{B.8b}$$

$$\mathbf{C} = \begin{pmatrix} 0 & 0 & a_1 & a_1 & a_1 \\ 0 & 0 & -a_1 & -a_1 & -a_1 \\ 0 & 0 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix} \tag{B.8c}$$

$$\mathbf{D} = \begin{pmatrix} \frac{1}{3}-L_f b_1 & \frac{1}{3}-L_f b_1 & \frac{1}{3}-L_f b_1 & L_f b_1 & L_f b_1 & L_f b_1 \\ L_f b_1 & L_f b_1 & L_f b_1 & \frac{1}{3}-L_f b_1 & \frac{1}{3}-L_f b_1 & \frac{1}{3}-L_f b_1 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \tag{B.8d}$$

with

$$a_1 = -\frac{LR_{L_f} - L_f R}{L_f \left(3L + 2L_f\right)} \tag{B.9a}$$

$$a_2 = -\frac{LR_{L_f} + L_f R + 2L_f R_{L_f}}{L_f \left(3L + 2L_f\right)} \tag{B.9b}$$

$$b_1 = \frac{1}{9L + 6L_f} \tag{B.9c}$$

$$b_2 = b_1 - \frac{1}{3L_f} \tag{B.9d}$$

$$b_3 = b_1 + \frac{2}{3L_f}. \tag{B.9e}$$

From (B.8c) and (B.22) it can be seen that the outputs, i_{out} and $i_{L_{f_{1p}}}$, are expressed in terms of $\mathbf{x}$, and that voltages, u_p and u_n, are expressed in terms of the inputs $\mathbf{u}$.

Simulation results of the reduced state-space model were compared to circuit simulation results obtained from PLECS blockset, with the switching legs modeled as

Table B.1: Component values that are used for the simulation results.

Item	Value	Unit	Item	Value	Unit
U_{DC}	100	V	L_f	800	µH
$\hat{m}$	0.75		R_{L_f}	500	mΩ
f_o	100	Hz	C_f	10	µF
R	2	Ω	C_{f_o}	100	µF
L	2	mH			

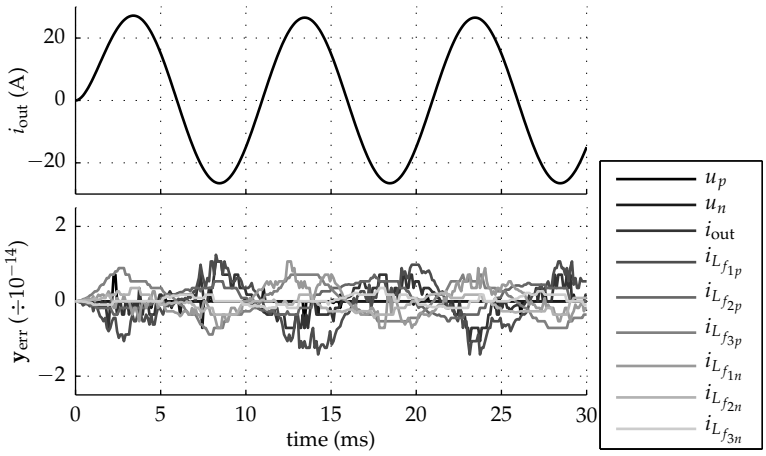


Figure B.2: Results showing the difference between the obtained MATLAB model and a PLECS simulation.

controlled voltage sources. The models were simulated using the ODE45 solver of MATLAB SIMULINK with default settings. The component values for simulation are given in Table B.1, where $\hat{m}$, and f_o are the peak modulation index, and frequency of the reference signal, respectively.

Figure B.2 depicts the simulation results of the output current (i_{out}) and the difference of the output vector ($\mathbf{y}$) of both models. It can be clearly seen that both models are matching with very high accuracy. In this example symmetrical components were used. It should be noted that the proposed procedure also works for asymmetrical circuits with component variation.

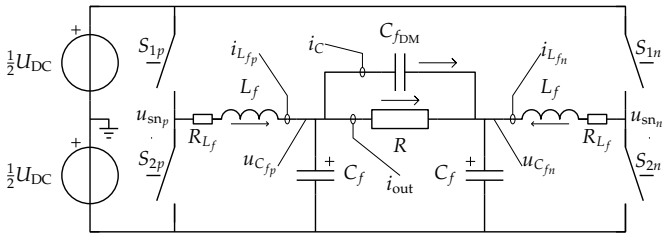


Figure B.3: Schematic overview of a FB converter with a 2nd order filter. The three filter capacitors form a loop, resulting in two actual states instead of three.

B.2 Example 2, removing superfluous capacitor voltages

The second example involves removing one superfluous state. Figure B.3 depicts a FB class-D amplifier with a 2nd order filter with an additional capacitor connected across the load, where all indicated voltages are referenced to the ground of the symmetrical supply. Such filters often appear in class-D amplifiers in combination with bipolar switching [114]. A capacitor is placed directly across the load to filter the large DM voltage ripple. Due to the bipolar switching only little CM voltage ripple is present. Therefore, much less CM voltage filtering is required to comply with EMC regulations. Such a filter results in more design freedom when selecting the DM and CM cut-off frequencies.

Similar to Example 1 one might think at first inspection that this circuit has 5 states. However, the voltage of the capacitor across the load resistance (R) is fixed by the voltages across the filter capacitors (C_f) that are connected to the negative supply rail. As a result this circuit has only 4 states. Again resistors can be added to the circuit to be able to model it without constraints, resulting in a stiff model with 5 states and reduced accuracy.

Also in this case the proposed method can be used to remove the superfluous capacitor voltage from the state-space equations without loss of accuracy.

As in the previous example, the average behavior of the switching legs is modeled using controlled voltage sources u_{sn_x}. First, the current through the capacitor that needs to be eliminated is added to the input vector as

$$\begin{aligned} \mathbf{u}_d &= \begin{pmatrix} \mathbf{u}_s & \mathbf{u} \end{pmatrix}^\mathsf{T} \\ &= \begin{pmatrix} i_C & u_{\mathrm{sn}_p} & u_{\mathrm{sn}_n} \end{pmatrix}^\mathsf{T}. \end{aligned} \tag{B.10}$$

Next the state vector is chosen as

$$\begin{aligned}\mathbf{x}_d &= \begin{pmatrix}\mathbf{x}_s & \mathbf{x}\end{pmatrix}^\mathsf{T} \\ &= \begin{pmatrix}u_{C_{f_{\mathrm{DM}}}} & u_{C_{f_p}} & u_{C_{f_n}} & i_{L_{f_p}} & i_{L_{f_n}}\end{pmatrix}^\mathsf{T}\end{aligned} \tag{B.11}$$

where the first element, which will be removed from the state vector, is the voltage across the capacitor connected in parallel to the load resistance.

As in Example 1 all states in $\mathbf{x}_d$ combined with the mesh current, i_C, are chosen as outputs of the model, resulting in

$$\mathbf{y} = \begin{pmatrix} i_C \\ \mathbf{x}_d \end{pmatrix}. \tag{B.12}$$

Given the model depicted in Figure B.3 and the chosen state and input vector, the state-space matrices become

$$\mathbf{A}_d = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{RC_f} & \frac{1}{RC_f} & \frac{1}{C_f} & 0 \\ 0 & \frac{1}{RC_f} & -\frac{1}{RC_f} & 0 & \frac{1}{C_f} \\ 0 & -\frac{1}{L_f} & 0 & -\frac{R_{L_f}}{L_f} & 0 \\ 0 & 0 & -\frac{1}{L_f} & 0 & -\frac{R_{L_f}}{L_f} \end{pmatrix} \tag{B.13a}$$

$$\mathbf{B}_d = \begin{pmatrix} \frac{1}{C_{f_{\mathrm{DM}}}} & 0 & 0 \\ -\frac{1}{C_f} & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f} \end{pmatrix} \tag{B.13b}$$

$$\mathbf{C}_d = \begin{pmatrix} \mathbf{0}^{1\times 5} \\ \mathbf{I}^5 \end{pmatrix} \tag{B.13c}$$

$$\mathbf{D}_d = \begin{pmatrix} 1 & \mathbf{0}^{1\times 2} \\ \mathbf{0}^{5\times 1} & \mathbf{0}^{5\times 2} \end{pmatrix}. \tag{B.13d}$$

The Kirchhoff voltage law equation that applies to the dependent states is given by

$$\mathbf{K} = \begin{pmatrix} -1 & 1 & -1 & 0 & 0 \end{pmatrix}. \tag{B.14}$$

Finally a basis of the null-space of $\mathbf{K}$ needs to be determined. Again the rational basis using Gaussian elimination is used. The resulting transformation matrix $\mathbf{G}$ is given by

$$\mathbf{G} = \begin{pmatrix} 1 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}. \tag{B.15}$$

Using (2.10) the reduced state-space representation of Example 2 becomes

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{B.16}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{B.17}$$

with

$$\mathbf{x} = \begin{pmatrix} u_{C_{fp}} & u_{C_{fn}} & i_{L_{fp}} & i_{L_{fn}} \end{pmatrix}^\mathsf{T} \tag{B.18}$$

$$\mathbf{u} = \begin{pmatrix} u_{\mathrm{sn}_p} & u_{\mathrm{sn}_n} \end{pmatrix}^\mathsf{T}. \tag{B.19}$$

Finally, the state-space matrices are given by

$$\mathbf{A} = \begin{pmatrix} -a_3 & a_3 & a_4 & a_5 \\ a_3 & -a_3 & a_5 & a_4 \\ -\frac{1}{L_f} & 0 & -\frac{R_{L_f}}{L_f} & 0 \\ 0 & -\frac{1}{L_f} & 0 & -\frac{R_{L_f}}{L_f} \end{pmatrix} \tag{B.20}$$

$$\mathbf{B} = \begin{pmatrix} 0 & 0 \\ 0 & 0 \\ \frac{1}{L_f} & 0 \\ 0 & \frac{1}{L_f} \end{pmatrix} \tag{B.21}$$

$$\mathbf{C} = \begin{pmatrix} -c_1 & c_1 & c_2 & -c_2 \\ 1 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix} \tag{B.22}$$

$$\mathbf{D} = \mathbf{0} \tag{B.23}$$

with

$$a_3 = \frac{1}{R\left(C_f + 2C_{f_{\mathrm{DM}}}\right)} \tag{B.24a}$$

$$a_4 = \frac{1}{2C_f} + \frac{1}{2C_f + 4C_{f_{\mathrm{DM}}}} \tag{B.24b}$$

$$a_5 = \frac{1}{2C_f} - \frac{1}{2C_f + 4C_{f_{\mathrm{DM}}}} \tag{B.24c}$$

$$c_1 = 2C_{f_{\mathrm{DM}}} a_3 \tag{B.24d}$$

$$c_2 = \frac{C_{f_{\mathrm{DM}}}}{C_f + 2C_{f_{\mathrm{DM}}}}. \tag{B.24e}$$

From (B.22) it can be seen that both i_C and $u_{C_{f_{\mathrm{DM}}}}$ are expressed in terms of $\mathbf{x}$.

As in Example 1 the simulation results of the reduced state-space model were compared to circuit simulation results from PLECS, using the component values given in Table B.1. Figure B.4 depicts the simulation results of the output current i_{out} and the difference of the output vectors of both models. Like Example 1 both models are matching with very high accuracy.

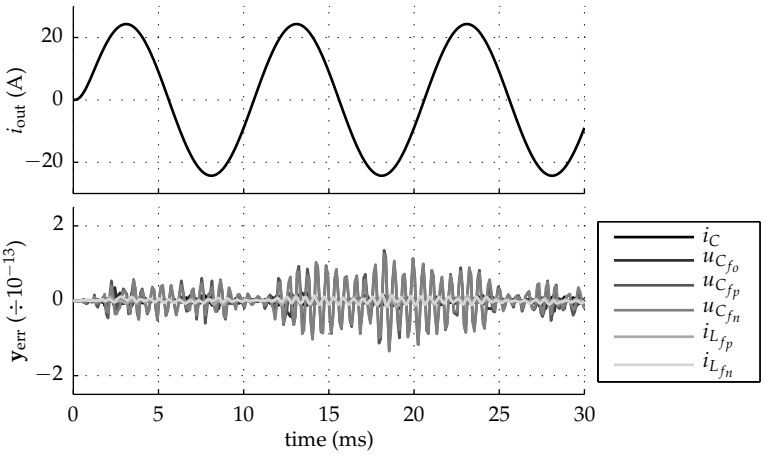


Figure B.4: Simulation results showing the difference between the reduced state space and the PLECS model of Example 2.

Appendix C

State-space averaging

C.1 Introduction

Many textbooks treat the state-space averaging method [29, 43, 67]. However, in most of them only simple converters with two modes of operation, like the buck converter in CCM, are considered. In Chapter 2 the general state-space averaging approach for any number of switching states is treated in an abstract mathematical form, and a method to remove superfluous storage elements is introduced. This appendix details the complete state-space averaging procedure for a converter with 16 switching states and one state dependency, and can be used as a procedure to follow for many other classes of converters.

C.2 Full-bridge equivalent of the DB

The DB consists of two parallel connected switching legs with unipolar complementary current flow. Figure C.1, depicts the full bridge equivalent of the DB where the switching legs that support positive current are indexed with 1 and the legs that support negative current are indexed 2. In Chapter 4 the DB is introduced as a converter topology that does not suffer from distortion due to blanking time. Furthermore, when CCM is guaranteed there is a linear relation between

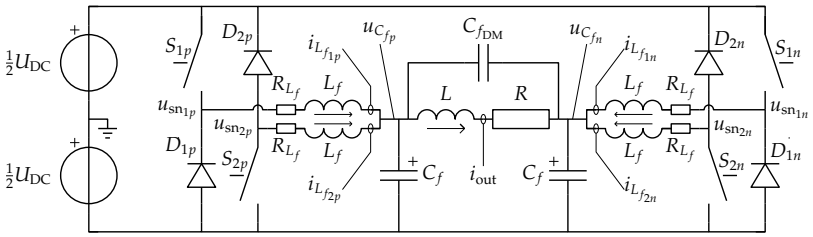


Figure C.1: Schematic overview of full-bridge equivalent DB.

Figure C.2: Switch (a) and diode (b) model used for state-space averaging.

modulation index and output voltage. Later in Chapter 6 it was shown that the DB, ideally, does not suffer from distortion due to the forward/saturation voltage of the semiconductor devices.

In Chapter 8 two control approaches are presented for the DB that rely on a linear model for the converter. The next sections describe a procedure to obtain an operating point dependent linearized small-signal model for the DB using state-space averaging. It assumes CCM and ideal switches and diodes, the characteristics of which are modeled with series connected voltage source and resistance, as depicted in Figure C.2.

C.3 Averaging procedure

Switched mode converters can be described as piecewise linear systems as

$$\dot{\mathbf{x}} = \mathbf{F}_k\mathbf{x} + \mathbf{g}_k \tag{C.1a}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} \tag{C.1b}$$

where $\mathbf{F}$ is the state-matrix, $\mathbf{g}$ is the input vector, $\mathbf{C}$ is the output matrix. Without loss of generality no direct feed through ($\mathbf{d} = \mathbf{0}$), and a time-invariant output

matrix $\mathbf{C}$ is assumed. The index k is the switch state of the converter that changes cyclically over time.

For the small signal modeling of the DB, depicted in Figure C.1, the following state vector is chosen

$$\mathbf{x} = \begin{pmatrix} i_{\text{out}} & i_{L_{f_{1p}}} & i_{L_{f_{2p}}} & i_{L_{f_{1n}}} & i_{L_{f_{2n}}} & u_{C_{f_p}} & u_{C_{f_n}} \end{pmatrix} \tag{C.2}$$

where i_{out} is the current flowing through the load, $i_{L_{f_{xy}}}$ are the filter inductor currents, and $u_{C_{f_y}}$ are the output voltages that appear across the load. The voltage across $C_{f_{\text{DM}}}$ depends on $u_{C_{f_p}}$ and $u_{C_{f_n}}$, and is therefore not a state.

The state-space averaging procedure involves obtaining the moving average of the vectors and matrices in (2.1) over a switching cycle. When a matrix or vector is dependent on the switching state k, the moving average is given by

$$\langle \mathbf{\Lambda} \rangle = \frac{1}{T_{\text{sw}}} \sum_{k \in K} \mathbf{\Lambda}_k T_k, \text{ with} \tag{C.3a}$$

$$T_{\text{sw}} = \sum_{k \in K} T_k \tag{C.3b}$$

where $\mathbf{\Lambda}_k$ is a matrix or vector that is cyclically switched, T_{sw} is the switching time of the converter, K is the set of cyclically switched states that occur during each cycle, and T_k is the time that each switching-state is active. Furthermore, during the averaging procedure the time T_k will be expressed in terms of the modulation indices of the corresponding switching legs, which are given by

$$\mathbf{u} = \begin{pmatrix} m_{1p} & m_{2p} & m_{1n} & m_{2n} \end{pmatrix}^{\mathsf{T}} \tag{C.4}$$

where m_{xy} are the modulation indices of the corresponding switching legs, which are restricted to the interval $[-1 \dots 1]$

When assuming CCM, that is the filter inductor currents i_{L_f} do not clamp to 0 A, $N = 16$ switching states and corresponding times can be identified, as shown in Table C.1. A 1 in the (switching) state represents that the corresponding leg is connected to $+\frac{1}{2}U_{\text{DC}}$ and a 0 represents a connection to $-\frac{1}{2}U_{\text{DC}}$. The switching state is ordered $\begin{pmatrix} 1p & 2p & 1n & 2n \end{pmatrix}$, using the same notation as in Figure C.1. The corresponding times that the states are active are coded such that they directly reflect the switching state, where a 1 means that both legs of the corresponding side are connected to $+\frac{1}{2}U_{\text{DC}}$, a 4 means that both legs are connected to $-\frac{1}{2}U_{\text{DC}}$, while 2 and 3 are the states that generate bias voltage, in which $-U_{\text{DC}}$, or $+U_{\text{DC}}$ is applied between the switching legs, respectively, and where consequently zero

Table C.1: Switching states of the DB.

T_x	state	T_x	state	T_x	state	T_x	state
T_{11}	0000	T_{21}	0100	T_{31}	1000	T_{41}	1100
T_{12}	0001	T_{22}	0101	T_{32}	1001	T_{42}	1101
T_{13}	0010	T_{23}	0110	T_{33}	1010	T_{43}	1110
T_{14}	0011	T_{24}	0111	T_{34}	1011	T_{44}	1111

average voltage is generated.

C.3.1 Moving average of the state matrix

The moving averages of the state matrix can be split as

$$\langle \mathbf{F} \rangle = \frac{1}{T_{\text{sw}}} \sum_{k=1}^{N} \mathbf{F}_k T_k = \mathbf{F}'' + \frac{1}{T_{\text{sw}}} \sum_{k=1}^{N} \mathbf{F}'_k T_k \tag{C.5}$$

where $\mathbf{F}''$ and $\mathbf{F}'_k$ are the parts of $\mathbf{F}_k$ that are dependent and not dependent on the switching state, respectively.

Since the circuit contains one state dependency the method described in Section 2.3 is used to determine the state-space matrices. Because the states corresponding to filter capacitors do not depend in the switching state, the method is applied to $\mathbf{F}''$ only, resulting in

$$\mathbf{F}'' = \begin{pmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & \frac{1}{L} & -\frac{1}{L} \\ 0 & -\frac{R_{L_f}}{L_f} & 0 & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & -\frac{R_{L_f}}{L_f} & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & 0 & -\frac{R_{L_f}}{L_f} & 0 & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_{L_f}}{L_f} & 0 & -\frac{1}{L_f} \\ -a_1 & a_2 & a_2 & a_3 & a_3 & 0 & 0 \\ a_1 & a_3 & a_3 & a_2 & a_2 & 0 & 0 \end{pmatrix} \tag{C.6}$$

with

$$a_1 = \frac{1}{C_f + C_{f_{\mathrm{DM}}}} \tag{C.7a}$$

$$a_2 = \tfrac{1}{2C_f} + \tfrac{1}{2}a_1 \tag{C.7b}$$

$$a_3 = \tfrac{1}{2C_f} - \tfrac{1}{2}a_1 \tag{C.7c}$$

where the parameters correspond to the components depicted in Figure C.1.

The 16 switching state dependent matrices $\mathbf{F}'_k$ are given by

$$\begin{aligned}
\mathbf{F}'_{11} &= \mathbf{F}^p_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{12} &= \mathbf{F}^p_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{13} &= \mathbf{F}^p_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{14} &= \mathbf{F}^p_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{21} &= \mathbf{F}^p_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{22} &= \mathbf{F}^p_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{23} &= \mathbf{F}^p_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{24} &= \mathbf{F}^p_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{31} &= \mathbf{F}^n_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{32} &= \mathbf{F}^n_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{33} &= \mathbf{F}^n_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{34} &= \mathbf{F}^n_{1p} + \mathbf{F}^p_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{41} &= \mathbf{F}^n_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{42} &= \mathbf{F}^n_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^p_{1n} + \mathbf{F}^n_{2n} \\
\mathbf{F}'_{43} &= \mathbf{F}^n_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^p_{2n} & \mathbf{F}'_{44} &= \mathbf{F}^n_{1p} + \mathbf{F}^n_{2p} + \mathbf{F}^n_{1n} + \mathbf{F}^n_{2n}
\end{aligned} \tag{C.8}$$

where in turn the matrices $\mathbf{F}^y_x$ are given by

$$\begin{aligned}
\mathbf{F}^p_{1p} &= -\frac{R_{\mathrm{on}}}{L_f}\,\mathrm{diag}(0,1,0,0,0,0,0,0) & \mathbf{F}^n_{1p} &= -\frac{R_f}{L_f}\,\mathrm{diag}(0,1,0,0,0,0,0,0) \\
\mathbf{F}^p_{2p} &= -\frac{R_f}{L_f}\,\mathrm{diag}(0,0,1,0,0,0,0,0) & \mathbf{F}^n_{2p} &= -\frac{R_{\mathrm{on}}}{L_f}\,\mathrm{diag}(0,0,1,0,0,0,0,0) \\
\mathbf{F}^p_{1n} &= -\frac{R_{\mathrm{on}}}{L_f}\,\mathrm{diag}(0,0,0,1,0,0,0,0) & \mathbf{F}^n_{1n} &= -\frac{R_f}{L_f}\,\mathrm{diag}(0,0,0,1,0,0,0,0) \\
\mathbf{F}^p_{2n} &= -\frac{R_f}{L_f}\,\mathrm{diag}(0,0,0,0,1,0,0,0) & \mathbf{F}^n_{2n} &= -\frac{R_{\mathrm{on}}}{L_f}\,\mathrm{diag}(0,0,0,0,1,0,0,0).
\end{aligned} \tag{C.9}$$

The subscripts x indicate the corresponding switching leg and the superscript p or n denotes whether the corresponding leg is connected to the positive or negative supply respectively. The diag operator represents a diagonal matrix where the parameters between the braces start from the top left of the matrix.

Because each index x in (C.9) has the same structure, that is the same diagonal

matrix, the moving average of $\mathbf{F}'_k$ can be rewritten as

$$\frac{1}{T_{\text{sw}}}\sum_{k=1}^{N}\mathbf{F}'_k = \frac{1}{T_{\text{sw}}}\Big(\mathbf{F}^p_{1p}T^p_{1p} + \mathbf{F}^n_{1p}T^n_{1p} + \mathbf{F}^p_{2p}T^p_{2p} + \mathbf{F}^n_{2p}T^n_{2p} + \dots . \\ \mathbf{F}^p_{1n}T^p_{1n} + \mathbf{F}^n_{1n}T^n_{1n} + \mathbf{F}^p_{2n}T^p_{2n} + \mathbf{F}^n_{np}T^n_{np}\Big) \quad \text{(C.10)}$$

where T^p_x, and T^n_x are the times that the corresponding matrices are active, which in turn can be expressed in terms of modulation indices as

$$T^p_{xy} = \tfrac{1}{2}\left(1 + m_{xy}\right)T_{\text{sw}} \quad \text{(C.11a)}$$
$$T^n_{xy} = \tfrac{1}{2}\left(1 - m_{xy}\right)T_{\text{sw}}. \quad \text{(C.11b)}$$

By combining the results of (C.6), (C.10), and (C.11) the moving average of the state matrix becomes

$$\langle\mathbf{F}(\mathbf{u})\rangle = \mathbf{F}'' + \tfrac{1}{2}\Big(\mathbf{F}^p_{1p} + \mathbf{F}^n_{1p} + \left(\mathbf{F}^p_{1p} - \mathbf{F}^n_{1p}\right)m_{1p} + \dots \\ \mathbf{F}^p_{2p} + \mathbf{F}^n_{2p} + \left(\mathbf{F}^p_{2p} - \mathbf{F}^n_{1p}\right)m_{2p} + \dots \\ \mathbf{F}^p_{1n} + \mathbf{F}^n_{1n} + \left(\mathbf{F}^p_{1n} - \mathbf{F}^n_{1n}\right)m_{1n} + \dots \\ \mathbf{F}^p_{2n} + \mathbf{F}^n_{2n} + \left(\mathbf{F}^p_{2n} - \mathbf{F}^n_{1n}\right)m_{2n}\Big). \quad \text{(C.12)}$$

C.3.2 Moving average of the input vector

In the piecewise linear model given by (C.1) the input is modeled as a vector that depends on the switching state k of the converter. The moving average over one switching cycle can be determined using a similar procedure as used for the state matrix. Similar to the procedure followed above the average becomes,

$$\langle\mathbf{g}\rangle = \frac{1}{T_{\text{sw}}}\sum_{k=1}^{N}\mathbf{g}_k T_k = \mathbf{g}'' + \frac{1}{T_{\text{sw}}}\sum_{k=1}^{N}\mathbf{g}'_k T_k \quad \text{(C.13)}$$

where $\mathbf{g}''$ and $\mathbf{g}'_k$ are the parts of the input vector that do and do not depend on the switching state respectively. For the DB, as depicted in Figure C.1, the vector $\mathbf{g}'' = \mathbf{0}$, however, for generality the same procedure is applied as for the state matrix.

The 16 switching state dependent vectors $\mathbf{g}'_k$ are given by

$$\begin{aligned}
\mathbf{g}'_{11} &= \mathbf{g}^p_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{12} &= \mathbf{g}^p_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{13} &= \mathbf{g}^p_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{14} &= \mathbf{g}^p_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{21} &= \mathbf{g}^p_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{22} &= \mathbf{g}^p_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{23} &= \mathbf{g}^p_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{24} &= \mathbf{g}^p_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{31} &= \mathbf{g}^n_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{32} &= \mathbf{g}^n_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{33} &= \mathbf{g}^n_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{34} &= \mathbf{g}^n_{1p} + \mathbf{g}^p_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{41} &= \mathbf{g}^n_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{42} &= \mathbf{g}^n_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^p_{1n} + \mathbf{g}^n_{2n} \\
\mathbf{g}'_{43} &= \mathbf{g}^n_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^p_{2n} & \mathbf{g}'_{44} &= \mathbf{g}^n_{1p} + \mathbf{g}^n_{2p} + \mathbf{g}^n_{1n} + \mathbf{g}^n_{2n}
\end{aligned} \tag{C.14}$$

where in turn the matrices $\mathbf{g}^y_x$ are given by

$$\begin{aligned}
\mathbf{g}^p_{1p} &= \frac{\frac{1}{2}U_{\mathrm{DC}} - V_{\mathrm{on}}}{L_f}\begin{pmatrix}0 & 1 & 0 & 0 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^p_{2p} &= \frac{\frac{1}{2}U_{\mathrm{DC}} - V_f}{L_f}\begin{pmatrix}0 & 0 & 1 & 0 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^p_{1n} &= \frac{\frac{1}{2}U_{\mathrm{DC}} - V_{\mathrm{on}}}{L_f}\begin{pmatrix}0 & 0 & 0 & 1 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^p_{2n} &= \frac{\frac{1}{2}U_{\mathrm{DC}} - V_f}{L_f}\begin{pmatrix}0 & 0 & 0 & 0 & 1 & 0 & 0\end{pmatrix}^\mathsf{T}
\end{aligned} \tag{C.15a}$$

and

$$\begin{aligned}
\mathbf{g}^n_{1p} &= \frac{-\frac{1}{2}U_{\mathrm{DC}} - V_f}{L_f}\begin{pmatrix}0 & 1 & 0 & 0 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^n_{2p} &= \frac{-\frac{1}{2}U_{\mathrm{DC}} - V_{\mathrm{on}}}{L_f}\begin{pmatrix}0 & 0 & 1 & 0 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^n_{1n} &= \frac{-\frac{1}{2}U_{\mathrm{DC}} - V_f}{L_f}\begin{pmatrix}0 & 0 & 0 & 1 & 0 & 0 & 0\end{pmatrix}^\mathsf{T} \\
\mathbf{g}^n_{2n} &= \frac{-\frac{1}{2}U_{\mathrm{DC}} - V_{\mathrm{on}}}{L_f}\begin{pmatrix}0 & 0 & 0 & 0 & 1 & 0 & 0\end{pmatrix}^\mathsf{T}.
\end{aligned} \tag{C.15b}$$

The subscripts, x, indicate the corresponding switching leg and the superscripts, y, determine whether that leg is connected to the positive supply rail, p, or negative rail, n.

Again, because each index x in (C.15a) and (C.15b) has the same structure, the moving average of $\mathbf{g}'_k$ can be rewritten as

$$\frac{1}{T_{\text{sw}}}\sum_{k=1}^{N}\mathbf{g}'_k T_k = \frac{1}{T_{\text{sw}}}\Big(\mathbf{g}^p_{1p}T^p_{1p} + \mathbf{g}^n_{1p}T^n_{1p} + \mathbf{g}^p_{2p}T^p_{2p} + \mathbf{g}^n_{2p}T^n_{2p} + \dots . \\ \mathbf{g}^p_{1n}T^p_{1n} + \mathbf{g}^n_{1n}T^n_{1n} + \mathbf{g}^p_{2n}T^p_{2n} + \mathbf{g}^n_{2n}T^n_{2n}\Big) \quad \text{(C.16)}$$

where T^p_x and T^n_x can be expressed in terms of modulation indices using (C.11).

By combining the results of (C.16), and (C.11) the moving average of the input matrix becomes

$$\langle \mathbf{g}(\mathbf{u})\rangle = \mathbf{g}' + \tfrac{1}{2}\Big(\mathbf{g}^p_{1p} + \mathbf{g}^n_{1p} + (\mathbf{g}^p_{1p} - \mathbf{g}^n_{1p})m_{1p} + \dots \\ \mathbf{g}^p_{2p} + \mathbf{g}^n_{2p} + (\mathbf{g}^p_{2p} - \mathbf{g}^n_{1p})m_{2p} + \dots \\ \mathbf{g}^p_{1n} + \mathbf{g}^n_{1n} + (\mathbf{g}^p_{1n} - \mathbf{g}^n_{1n})m_{1n} + \dots \\ \mathbf{g}^p_{2n} + \mathbf{g}^n_{2n} + (\mathbf{g}^p_{2n} - \mathbf{g}^n_{1n})m_{2n}\Big) \quad \text{(C.17)}$$

where in this particular case $\mathbf{g}' = \mathbf{0}$.

Using (C.12) and (C.17), the averaged model becomes

$$\langle \dot{\mathbf{x}}\rangle \approx \mathbf{f}(\langle \mathbf{x}\rangle, \mathbf{u}) = \langle \mathbf{F}(\mathbf{u})\rangle\langle \mathbf{x}\rangle + \langle \mathbf{g}(\mathbf{u})\rangle \quad \text{(C.18a)}$$

$$\langle \mathbf{y}\rangle \approx \mathbf{C}\langle \mathbf{x}\rangle \quad \text{(C.18b)}$$

where the approximation becomes an equality when $\langle \mathbf{x}\rangle$ or $\langle \mathbf{F}\rangle$ is time-invariant, which is not true. However, from (C.9) and (C.12) it can be seen that $\langle \mathbf{F}\rangle$ becomes time-invariant when $R_{\text{on}} = R_f$, making (C.18) an equality instead of an approximation.

C.4 Linearization around an operating point

The averaged model in (C.18) is nonlinear because both the averaged state matrix and input vector depend on the modulation indices of the switching legs. A linear model can be obtained by linearizion about an operating point, using the Taylor

expansion given by

$$\langle \dot{\mathbf{x}} \rangle \approx \mathbf{f}(\mathbf{x}_o, \mathbf{u}_o) + \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{x} \rangle}\right|_{\mathbf{u}_o} (\langle \mathbf{x} \rangle - \mathbf{x}_o) + \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{\mathbf{x}_o} (\mathbf{u} - \mathbf{u}_o) \tag{C.19}$$

where the capitals $\mathbf{x}_o$, and $\mathbf{u}_o$ represent the steady-state operating-point for linearizion of the DB.

When expressing perturbations from steady-state as $\tilde{\mathbf{x}} = \langle \mathbf{x} \rangle - \mathbf{x}_o$, $\tilde{\mathbf{u}} = \mathbf{u} - \mathbf{u}_o$, and including that for steady-state $\dot{\mathbf{X}} = 0$, (C.19) simplifies to

$$\dot{\tilde{\mathbf{x}}} \approx \mathbf{A}(\mathbf{u}_o)\tilde{\mathbf{x}} + \mathbf{B}(\mathbf{x}_o)\tilde{\mathbf{u}} + \mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) \tag{C.20a}$$

$$\tilde{\mathbf{y}} = \mathbf{C}\tilde{\mathbf{x}} \tag{C.20b}$$

where the state and input matrices, and constant disturbance input equal

$$\mathbf{A}(\mathbf{u}_o) = \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \langle \mathbf{x} \rangle}\right|_{(\mathbf{u}_o)} \tag{C.21a}$$

$$\mathbf{B}(\mathbf{x}_o) = \left.\frac{\partial \mathbf{f}(\langle \mathbf{x} \rangle, \mathbf{u})}{\partial \mathbf{u}}\right|_{(\mathbf{x}_o)} \tag{C.21b}$$

$$\mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) = \mathbf{f}(\mathbf{x}_o, \mathbf{u}_o). \tag{C.21c}$$

For the DB modeled in this appendix the state matrix in (C.21) becomes

$$\mathbf{A}(\mathbf{u}_o) = \begin{pmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & \frac{1}{L} & -\frac{1}{L} \\ 0 & -\frac{R_{1p}}{L_f} & 0 & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & -\frac{R_{2p}}{L_f} & 0 & 0 & -\frac{1}{L_f} & 0 \\ 0 & 0 & 0 & -\frac{R_{1n}}{L_f} & 0 & 0 & -\frac{1}{L_f} \\ 0 & 0 & 0 & 0 & -\frac{R_{2n}}{L_f} & 0 & -\frac{1}{L_f} \\ -a_1 & a_2 & a_2 & a_3 & a_3 & 0 & 0 \\ a_1 & a_3 & a_3 & a_2 & a_2 & 0 & 0 \end{pmatrix} \tag{C.22}$$

with

$$a_1 = \frac{1}{C_f + C_{f_{\mathrm{DM}}}} \tag{C.23a}$$

$$a_2 = \tfrac{1}{2C_f} + \tfrac{1}{2}a_1 \tag{C.23b}$$

$$a_3 = \tfrac{1}{2C_f} - \tfrac{1}{2}a_1 \tag{C.23c}$$

and where R_{1p} to R_{2n} represent equivalent resistances, which depend on the operating point, being given by

$$R_{1p} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\mathrm{on}}\right) - \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) M_{1p} \tag{C.24a}$$

$$R_{2p} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\mathrm{on}}\right) + \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) M_{2p} \tag{C.24b}$$

$$R_{1n} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\mathrm{on}}\right) - \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) M_{1n} \tag{C.24c}$$

$$R_{2n} = R_{L_f} + \frac{1}{2}\left(R_f + R_{\mathrm{on}}\right) + \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) M_{2n} \tag{C.24d}$$

The input matrix of (C.21), in turn, is given by

$$\mathbf{B}(\mathbf{x}_o) = \frac{1}{L_f}\begin{pmatrix} 0 & 0 & 0 & 0 \\ U_{1p} & 0 & 0 & 0 \\ 0 & U_{2p} & 0 & 0 \\ 0 & 0 & U_{1n} & 0 \\ 0 & 0 & 0 & U_{2n} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \tag{C.25}$$

where U_{1p} to U_{2n} denote the operating-point dependent switching-leg voltages, which in turn are given by

$$U_{1p} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_f - V_{\mathrm{on}}\right) + \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) I_{L_{f_{1p}}} \tag{C.26a}$$

$$U_{2p} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_f - V_{\mathrm{on}}\right) - \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) I_{L_{f_{2p}}} \tag{C.26b}$$

$$U_{1n} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_f - V_{\mathrm{on}}\right) + \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) I_{L_{f_{1n}}} \tag{C.26c}$$

$$U_{2n} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_f - V_{\mathrm{on}}\right) - \frac{1}{2}\left(R_f - R_{\mathrm{on}}\right) I_{L_{f_{2n}}}. \tag{C.26d}$$

Finally the constant disturbance term in (C.21) equals

$$\mathbf{w}_o(\mathbf{x}_o, \mathbf{u}_o) = \langle \mathbf{F}(\mathbf{u}_o) \rangle \mathbf{x}_o + \langle \mathbf{g}(\mathbf{u}_o) \rangle \tag{C.27}$$

where

$$\langle \mathbf{F}(\mathbf{u}_o) \rangle = \mathbf{A}(\mathbf{u}_o) \tag{C.28}$$

and

$$\langle \mathbf{g}(\mathbf{u}_o) \rangle = \frac{g_1}{L_f} \begin{pmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \mathbf{u}_o + \frac{g_2}{L_f} \begin{pmatrix} 0 \\ -1 \\ 1 \\ -1 \\ 1 \\ 0 \\ 0 \end{pmatrix} \tag{C.29}$$

with

$$g_1 = \frac{1}{2} U_{\text{DC}} + \frac{1}{2} \left(V_f - V_{\text{on}} \right) \tag{C.30a}$$

$$g_2 = \frac{1}{2} \left(V_f + V_{\text{on}} \right). \tag{C.30b}$$

From (C.24) and (C.26) it can be seen that the state and input matrix become operating-point independent when $R_{\text{on}} = R_f$, which agrees with the results presented in Chapter 6. Thus when $R_{\text{on}} = R_f$ the average state-space representation in (C.20) becomes valid for the full operating range and is, therefore, not a small-signal approximation. Moreover, when $R_{\text{on}} = R_f$ $\langle \mathbf{F}(\mathbf{u}) \rangle$ becomes time-invariant, as a result the approximation in (2.5) becomes an equality. Thus the averaged model exactly describes the moving-average behavior of the piecewise linear model.

Furthermore, when choosing the steady-state operating point at half of the range,

that is $\mathbf{x}_o = \mathbf{0}$ and $\mathbf{u}_o = \mathbf{0}$ the disturbance input reduces to

$$\mathbf{w}_o = \frac{\frac{1}{2}\left(V_f + V_{\text{on}}\right)}{L_f} \begin{pmatrix} 0 \\ -1 \\ 1 \\ -1 \\ 1 \\ 0 \\ 0 \end{pmatrix} \tag{C.31}$$

which is a constant voltage due to the forward voltage of the semiconductor switches and diodes. From the signs of the disturbance voltage is can be seen that they appear only in the bias voltages and not at the output of the DB, which also supports the results of Chapter 6. It should again be noted that the state-space models in this thesis are only valid for CCM, DCM should, therefore, be prevented.

C.5 Including component variation

The model derived in the previous section does not include component variation. Without further detail both the state and input matrix with component variation are given by

$$\mathbf{A}(\mathbf{u}_o) = \begin{pmatrix} -\frac{R}{L} & 0 & 0 & 0 & 0 & \frac{1}{L} & -\frac{1}{L} \\ 0 & -\frac{R_{1p}}{L_{f_{1p}}} & 0 & 0 & 0 & -\frac{1}{L_{f_{1p}}} & 0 \\ 0 & 0 & -\frac{R_{2p}}{L_{f_{2p}}} & 0 & 0 & -\frac{1}{L_{f_{2p}}} & 0 \\ 0 & 0 & 0 & -\frac{R_{1n}}{L_{f_{1n}}} & 0 & 0 & -\frac{1}{L_{f_{1n}}} \\ 0 & 0 & 0 & 0 & -\frac{R_{2n}}{L_{f_{2n}}} & 0 & -\frac{1}{L_{f_{2n}}} \\ -a_3 & a_6 & a_6 & a_4 & a_4 & 0 & 0 \\ a_2 & a_4 & a_4 & a_5 & a_5 & 0 & 0 \end{pmatrix} \tag{C.32}$$

$$\mathbf{B}(\mathbf{x}_o) = \begin{pmatrix} 0 & 0 & 0 & 0 \\ \frac{U'_{1p}}{L_{f_{1p}}} & 0 & 0 & 0 \\ 0 & \frac{U'_{2p}}{L_{f_{2p}}} & 0 & 0 \\ 0 & 0 & \frac{U'_{1n}}{L_{f_{1n}}} & 0 \\ 0 & 0 & 0 & \frac{U'_{2n}}{L_{f_{2n}}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{pmatrix} \tag{C.33}$$

with

$$a_1 = \frac{1}{C_{f_p}C_{f_{\mathrm{DM}}} + C_{f_n}C_{f_{\mathrm{DM}}} + C_{f_p}C_{f_n}} \tag{C.34a}$$

$$a_2 = C_{f_p}a_1 \tag{C.34b}$$

$$a_3 = C_{f_n}a_1 \tag{C.34c}$$

$$a_4 = C_{f_{\mathrm{DM}}}a_1 \tag{C.34d}$$

$$a_5 = \left(C_{f_p} + C_{f_{\mathrm{DM}}}\right)a_1 \tag{C.34e}$$

$$a_6 = \left(C_{f_n} + C_{f_{\mathrm{DM}}}\right)a_1 \tag{C.34f}$$

and where R_{1p} to R_{2n} represent equivalent resistances, which depend on the operating point, being given by

$$R'_{1p} = R_{L_{f_{1p}}} + \frac{1}{2}\left(R_{f_{1p}} + R_{\mathrm{on}_{1p}}\right) - \frac{1}{2}\left(R_{f_{1p}} - R_{\mathrm{on}_{1p}}\right)M_{1p} \tag{C.35a}$$

$$R'_{2p} = R_{L_{f_{2p}}} + \frac{1}{2}\left(R_{f_{2p}} + R_{\mathrm{on}_{2p}}\right) + \frac{1}{2}\left(R_{f_{2p}} - R_{\mathrm{on}_{2p}}\right)M_{2p} \tag{C.35b}$$

$$R'_{1n} = R_{L_{f_{1n}}} + \frac{1}{2}\left(R_{f_{1n}} + R_{\mathrm{on}_{1n}}\right) - \frac{1}{2}\left(R_{f_{1n}} - R_{\mathrm{on}_{1n}}\right)M_{1n} \tag{C.35c}$$

$$R'_{2n} = R_{L_{f_{2n}}} + \frac{1}{2}\left(R_{f_{2n}} + R_{\mathrm{on}_{2n}}\right) + \frac{1}{2}\left(R_{f_{2n}} - R_{\mathrm{on}_{2n}}\right)M_{2n} \tag{C.35d}$$

and U_{1p} to U_{2n} denote the operating-point dependent switching-leg voltages, which in turn are given by

$$U'_{1p} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_{f_{1p}} - V_{\mathrm{on}_{1p}}\right) + \frac{1}{2}\left(R_{f_{1p}} - R_{\mathrm{on}_{1p}}\right) I_{L_{f_{1p}}} \tag{C.36a}$$

$$U'_{2p} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_{f_{2p}} - V_{\mathrm{on}_{2p}}\right) - \frac{1}{2}\left(R_{f_{2p}} - R_{\mathrm{on}_{2p}}\right) I_{L_{f_{2p}}} \tag{C.36b}$$

$$U'_{1n} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_{f_{1n}} - V_{\mathrm{on}_{1n}}\right) + \frac{1}{2}\left(R_{f_{1n}} - R_{\mathrm{on}_{1n}}\right) I_{L_{f_{1n}}} \tag{C.36c}$$

$$U'_{2n} = \frac{1}{2}U_{\mathrm{DC}} + \frac{1}{2}\left(V_{f_{2n}} - V_{\mathrm{on}_{2n}}\right) - \frac{1}{2}\left(R_{f_{2n}} - R_{\mathrm{on}_{2n}}\right) I_{L_{f_{2n}}}. \tag{C.36d}$$

Similarly $\mathbf{w}_o$ can be extended to include component variation.

C.6 Small-signal model of the conventional FB

A detailed model for the conventional FB, as depicted in Figure C.3, is not derived in this thesis. However, when assuming ideal switches, $V_{\mathrm{on}} = V_f = 0$ and $R_{\mathrm{on}} = R_f = 0$, and neglecting blanking time, the small-signal model of the conventional FB is related to the model valid for CCM of the DB by the following transformations on the state and input vectors

$$\mathbf{x}_{\mathrm{FB}} = \mathbf{M}\mathbf{x} \tag{C.37a}$$

$$\mathbf{u}_{\mathrm{FB}} = \mathbf{N}\mathbf{u} \tag{C.37b}$$

resulting in the following small-signal model of the FB

$$\dot{\tilde{\mathbf{x}}}_{\mathrm{FB}} = \mathbf{M}\mathbf{A}\mathbf{M}^{+}\tilde{\mathbf{x}}_{\mathrm{FB}} + \mathbf{M}\mathbf{B}\mathbf{N}^{+}\tilde{\mathbf{u}}_{\mathrm{FB}} \tag{C.38}$$

where $\mathbf{M}^{+}$ and $\mathbf{N}^{+}$ are the Moore-Penrose pseudo inverses of the non-square matrices $\mathbf{M}$ and $\mathbf{N}$, respectively.

For matrices with linearly independent rows or columns, as in this case, the pseudo-inverse is given by

$$\mathbf{M}^{+} = \begin{cases} \mathbf{M}^{\mathsf{T}}(\mathbf{M}\mathbf{M}^{\mathsf{T}})^{-1}, & \text{linear independent rows} \\ (\mathbf{M}^{\mathsf{T}}\mathbf{M})^{-1}\mathbf{M}^{\mathsf{T}}, & \text{linear independent columns.} \end{cases} \tag{C.39}$$

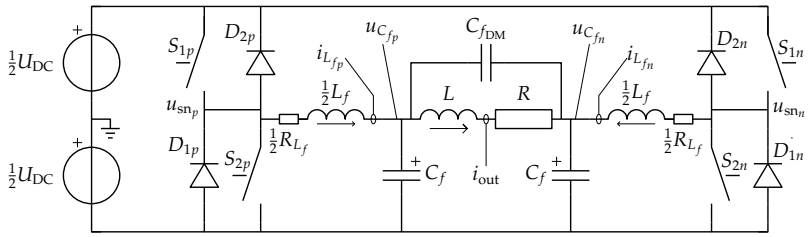


Figure C.3: Schematic overview of the conventional FB.

When the state and input vectors of the conventional FB are chosen as

$$\mathbf{x}_{\mathrm{FB}} = \begin{pmatrix} i_{\mathrm{out}} & i_{L_{f_p}} & i_{L_{f_n}} & u_{C_{f_p}} & u_{C_{f_n}} \end{pmatrix} \tag{C.40a}$$

$$\mathbf{u}_{\mathrm{FB}} = \begin{pmatrix} m_p & m_n \end{pmatrix} \tag{C.40b}$$

the transformation matrices $\mathbf{M}$ and $\mathbf{N}$ become

$$\mathbf{M} = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \tag{C.41}$$

and

$$\mathbf{N} = \begin{pmatrix} \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{1}{2} \end{pmatrix}. \tag{C.42}$$

From (C.41) and (C.42) it can be seen that the inductor current of the FB is the sum of the inductor currents and that the bias current is removed from the model. The FB with ideal switches is thus equivalent to the DB without bias. Therefore, the same output current/voltage controller can be used for both the FB and DB. However, the DB requires means to guarantee CCM by ensuring sufficient bias current.

Appendix D

The area product

D.1 The area-product method

The area-product method proposed in [21], and later treated in more detail in [61], results in a closed form equation that can be used to determine inductor volume.

The area product A_P is expressed as the product of the effective core area A_C and the winding area W_A, as indicated in Figure D.1a and Figure D.1b. When neglecting leakage the flux in a core can be expressed as

$$n\hat{\Phi} = L\hat{i} \tag{D.1}$$

where $\hat{\Phi}$ is the peak magnetic flux in the core, L represents the inductance, n is the number of turns, and $\hat{i}$ is the peak current in the wire, as depicted in Figure D.1d.

When, in turn, assuming a homogeneous flux distribution in the core, (D.1) can be rewritten to

$$A_C = \frac{L}{n\hat{B}}\hat{i} \tag{D.2}$$

where $\hat{B}$ is the peak magnetic flux density, and A_C the effective core area as indicated in Figure D.1a.

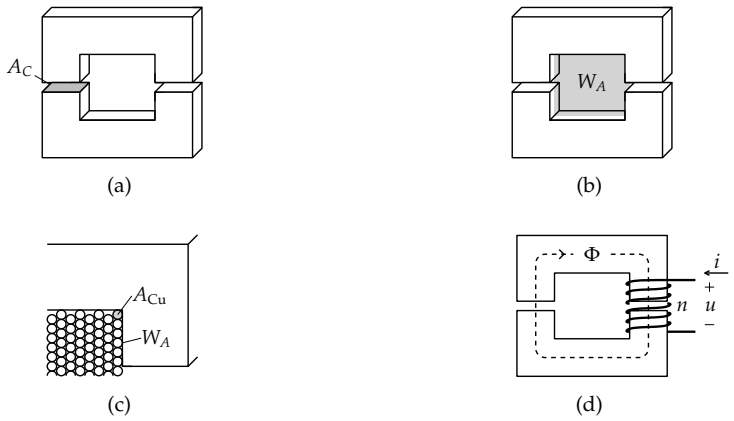


Figure D.1: Area-product parameters, geometric (a) & (b), electric and magnetic (c).

The winding area can be determined from

$$K_u W_A = n A_{Cu} \tag{D.3}$$

where W_A represents the window area for the windings, as indicated in Figure D.1a. The wire cross-sectional area is represented by A_{Cu} and K_u is the window utilization factor, which is the ratio between W_A and n times A_{Cu}, as illustrated in Figure D.1c.

Rewriting (D.3) in terms of current results in

$$W_A = \frac{n}{J K_u} I \tag{D.4}$$

where the current density and the RMS current in the wire are represented by J and I respectively.

Multiplication of (D.2) and (D.4) results in the area product, which is given by

$$A_P = \frac{L}{\hat{B} J K_u} \hat{\imath} I. \tag{D.5}$$

From (D.5) it can be seen that the area-product does not depend on the number of turns. Finally the total core volume V_L can be determined from

$$V_L = K_{vol} A_P^{3/4} \tag{D.6}$$

where K_{vol} is the core's geometrical constant.

D.2 The peak and RMS currents for a DB

Both inductors are subject to the same current except for the polarity, therefore, only the inductor carrying positive current is considered in this section. The filter inductor current for a DB can be split in a periodic average and a high frequency ripple as

$$i_{L_{f_1}} = \langle i_{L_{f_1}} \rangle + \tilde{i}_{L_{f_1}} \tag{D.7}$$

where $\langle i_{L_f} \rangle$ is a periodic average inductor current and $\tilde{i}_{L_f}$ represents the high frequency ripple due to switching.

Using the variable transformation given in (4.10), equation (D.7) can be rewritten to

$$i_{L_{f_1}} = \tfrac{1}{2}\langle i_{\text{sum}} \rangle + \langle i_{\text{bias}} \rangle + \frac{1}{2}\tilde{i}_{\text{sum}} + \tilde{i}_{\text{bias}} \tag{D.8}$$

which in turn equals

$$i_{L_{f_1}} = \tfrac{1}{2}\langle i_{\text{sum}} \rangle + \langle i_{\text{bias}} \rangle + \tilde{i}_{L_{f_1}}. \tag{D.9}$$

When assuming the periodic average capacitor current $\langle i_{C_{fp}} \rangle$, which is small in practice, to be zero, (D.9) becomes

$$i_{L_{f_1}} \approx \tfrac{1}{2} i_{\text{out}} + \langle i_{\text{bias}} \rangle + \tilde{i}_{L_{f_1}} \tag{D.10}$$

when choosing the bias current as given in (4.20) and (4.21), equation (D.10) becomes

$$i_{L_{f_1}} \approx \tfrac{1}{2} i_{\text{out}} + \tilde{i}_{L_{f_1}} + \begin{cases} \frac{1}{2}\hat{i}_{\text{out}} + \lambda_{\text{th}}\hat{\Delta} i_{L_f}, & \text{constant bias} \\ \frac{1}{2}|i_{\text{out}}| + \lambda_{\text{th}}\hat{\Delta} i_{L_f}, & \text{modulated bias.} \end{cases} \tag{D.11}$$

D.2.1 Peak current

When assuming that maximum output current coincides with the maximum filter inductor current ripple, the peak current for both constant and modulated bias

becomes

$$\hat{i}_{L_{f_1}} \approx \hat{i}_{\text{out}} + (1 + \lambda_{\text{th}})\,\hat{\Delta} i_{L_f} \tag{D.12}$$

which is worst-case and only occurs for a purely inductive load. Therefore, in all other cases a conservative penalty on inductor current ripple is applied.

D.2.2 RMS current for constant bias

The RMS current over a cycle time (T_o) is given by

$$I_{L_{f_1}} \approx \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(i_{L_{f_1}}(\tau)\right)^2 \mathrm{d}\tau} \tag{D.13}$$

which for constant bias current becomes

$$I_{L_{f_1}} \approx \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tfrac{1}{2}\hat{i}_{\text{out}} + \lambda_{\text{th}}\hat{\Delta} i_{L_f} + \tilde{i}_{L_{f_1}}(\tau)\right)^2 \mathrm{d}\tau.} \tag{D.14}$$

When assuming a zero average output current with cycle time T_o and zero average inductor current ripple with switching cycle time T_{sw}, that is

$$0 = \int_t^{t+T_o} i_{\text{out}}(\tau)\mathrm{d}\tau \tag{D.15}$$

$$0 = \int_t^{t+T_{\text{sw}}} \tilde{i}_{L_f}(\tau)\mathrm{d}\tau \tag{D.16}$$

where T_{sw} is an integer multiple of T_o, (D.14) becomes

$$I_{L_{f_1}} \approx \left(\frac{1}{T_o} \int_t^{t+T_o} \tfrac{1}{4}\left(i_{\text{out}}(\tau)\right)^2 + \tfrac{1}{4}\hat{i}_{\text{out}}^2 + \left(\lambda_{\text{th}}\hat{\Delta} i_{L_f}\right)^2 + \left(\tilde{i}_{L_{f_1}}(\tau)\right)^2 + \dots \right.$$
$$\left. i_{\text{out}}(\tau)\tilde{i}_{L_{f_1}}(\tau) + \hat{i}_{\text{out}}\lambda_{\text{th}}\hat{\Delta} i_{L_f}\mathrm{d}\tau\right)^{\frac{1}{2}}. \tag{D.17}$$

Moreover, when assuming $T_{\text{sw}} \ll T_o$ the following cross term can be neglected

$$0 \approx \int_{t}^{t+T_{\text{sw}}} i_{\text{out}}(\tau)\tilde{i}_{L_f}(\tau)\mathrm{d}\tau \tag{D.18}$$

and the RMS current simplifies to

$$I_{L_{f_1}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}\left(i_{\text{out}}(\tau)\right)^2 + \tfrac{1}{4}\hat{i}_{\text{out}}^2 + \left(\lambda_{\text{th}}\hat{\Delta}i_{L_f}\right)^2 + \left(\tilde{i}_{L_{f_1}}(\tau)\right)^2 + \hat{i}_{\text{out}}\lambda_{\text{th}}\hat{\Delta}i_{L_f}\mathrm{d}\tau} \tag{D.19}$$

which in turn equals

$$I_{L_{f_1}} \approx \sqrt{\tfrac{1}{4}\left(I_{\text{out}}\right)^2 + \tfrac{1}{4}\hat{i}_{\text{out}}^2 + \left(\tfrac{1}{3} + \lambda_{\text{th}}^2\right)\left(\hat{\Delta}i_{L_f}\right)^2 + \hat{i}_{\text{out}}\lambda_{\text{th}}\hat{\Delta}i_{L_f}}. \tag{D.20}$$

When, furthermore, assuming maximum inductor current ripple, the RMS value for ideal triangular shaped currents is given by

$$\tfrac{1}{3}\Delta i_{L_f} = \int_{t}^{t+T_{\text{sw}}} \left(\tilde{i}_{L_{f_1}}(\tau)\right)^2 \mathrm{d}\tau \tag{D.21}$$

which finally, when assuming sinusoidal output current (D.20), becomes

$$I_{L_{f_1}} \approx \sqrt{\tfrac{3}{8}\hat{i}_{\text{out}}^2 + \left(\tfrac{1}{3} + \lambda_{\text{th}}^2\right)\left(\hat{\Delta}i_{L_f}\right)^2 + \hat{i}_{\text{out}}\lambda_{\text{th}}\hat{\Delta}i_{L_f}}. \tag{D.22}$$

D.2.3 RMS current for modulated bias

The RMS filter inductor current for modulated bias current equals

$$I_{L_{f_1}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \left(\tfrac{1}{2}i_{\text{out}}(\tau) + \tfrac{1}{2}|i_{\text{out}}(\tau)| + \lambda_{\text{th}}\hat{\Delta}i_{L_f} + \tilde{i}_{L_{f_1}}(\tau)\right)^2 \mathrm{d}\tau}. \tag{D.23}$$

When assuming a zero average output current with cycle time T_o and zero average inductor current ripple with switching cycle time T_{sw}, as given by (D.15) and (D.16), and furthermore assuming that T_{sw} is an integer multiple of T_o, (D.23)

becomes

$$I_{L_{f_1}} \approx \left(\frac{1}{T_o} \int_t^{t+T_o} \tfrac{1}{4} \left(i_{\text{out}}(\tau)\right)^2 + \tfrac{1}{4}|i_{\text{out}}|(\tau)^2 + \left(\lambda_{\text{th}} \hat{\Delta} i_{L_f}\right)^2 + \left(\tilde{i}_{L_{f_1}}(\tau)\right)^2 + \dots \right.$$
$$\left. i_{\text{out}}(\tau)\tilde{i}_{L_{f_1}}(\tau) + |i_{\text{out}}(\tau)|\lambda_{\text{th}} \hat{\Delta} i_{L_f} + |i_{\text{out}}(\tau)|\tilde{i}_{L_{f_1}}(\tau) \mathrm{d}\tau \right)^{\frac{1}{2}}. \quad \text{(D.24)}$$

Moreover, when assuming $T_{\text{sw}} \ll T_o$, this simplifies to

$$I_{L_{f_1}} \approx \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \tfrac{1}{2} \left(i_{\text{out}}(\tau)\right)^2 + \left(\lambda_{\text{th}} \hat{\Delta} i_{L_f}\right)^2 + \left(\tilde{i}_{L_{f_1}}(\tau)\right)^2 + \left(i_{\text{out}}(\tau)\right) \lambda_{\text{th}} \hat{\Delta} i_{L_f} \mathrm{d}\tau} \quad \text{(D.25)}$$

which in turn, when assuming maximum inductor current ripple, becomes

$$I_{L_{f_1}} \approx \sqrt{\tfrac{1}{2} I_{\text{out}}^2 + \left(\tfrac{1}{3} + \lambda_{\text{th}}^2\right) \left(\hat{\Delta} i_{L_f}\right)^2 + \frac{1}{T_o} \int_t^{t+T_o} |i_{\text{out}}(\tau)| \lambda_{\text{th}} \hat{\Delta} i_{L_f} \mathrm{d}\tau}. \quad \text{(D.26)}$$

Finally, when assuming sinusoidal output current, (D.20) becomes

$$I_{L_{f_1}} \approx \sqrt{\tfrac{1}{4} \hat{i}_{\text{out}}^2 + \left(\tfrac{1}{3} + \lambda_{\text{th}}^2\right) \left(\hat{\Delta} i_{L_f}\right)^2 + \frac{2}{\pi} \hat{i}_{\text{out}} \lambda_{\text{th}} \hat{\Delta} i_{L_f}}. \quad \text{(D.27)}$$

D.3 The area product for a DB with coupled inductors

The area product for a DB with coupled inductors as given in (5.22), is

$$A_{P_{\text{DB}}} = \frac{2L_{\text{sum}}}{\hat{B} J K_{\text{u}}} \frac{1}{1+\kappa} \hat{i} I \quad \text{(D.28)}$$

and the peak and RMS inductor currents are represented by

$$\hat{i} = \max_t \left(\left(1 + \kappa_f\right) \frac{1}{2} i_{\text{sum}}(t) + \left(1 - \kappa_f\right) i_{\text{bias}}(t) \right) \quad \text{(D.29)}$$

and

$$I = \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o}\left(\tfrac{1}{2}i_{\text{sum}}(\tau)+i_{\text{bias}}(\tau)\right)^2 \mathrm{d}\tau}. \tag{D.30}$$

D.3.1 Peak inductor current

The peak current can be expressed in periodic average and switching ripple components as

$$\hat{i} = \max_t\left(\left(1+\kappa_f\right)\frac{1}{2}\left(\langle i_{\text{sum}}(t)\rangle + \tilde{i}_{\text{sum}}(t)\right) + \left(1-\kappa_f\right)\left(\langle i_{\text{bias}}(t)\rangle + \tilde{i}_{\text{bias}}(t)\right)\right) \tag{D.31}$$

which in turn, when assuming $\langle i_{C_f}\rangle = 0$, becomes

$$\hat{i} = \max_t\left(\left(1+\kappa_f\right)\frac{1}{2}\left(i_{\text{out}}(t)+\tilde{i}_{\text{sum}}(t)\right) + \left(1-\kappa_f\right)\left(\frac{1}{2}\hat{i}_{\text{out}} + i_{\text{th}} + \tilde{i}_{\text{bias}}(t)\right)\right) \tag{D.32a}$$

for constant bias current, and

$$\hat{i} = \max_t\left(\left(1+\kappa_f\right)\frac{1}{2}\left(i_{\text{out}}(t)+\tilde{i}_{\text{sum}}(t)\right) + \left(1-\kappa_f\right)\left(\frac{1}{2}|i_{\text{out}}(t)| + i_{\text{th}} + \tilde{i}_{\text{bias}}(t)\right)\right) \tag{D.32b}$$

for modulated bias current.

Equations (D.32a) and (D.32b) can be expressed in time independent parameters as

$$\hat{i} = \hat{i}_{\text{out}} + \max_{m_{\text{avg}}}\Big(\left(1+\kappa_f\right)\frac{1}{2}\Delta i_{\text{sum}}(m_{\text{avg}}) + \left(1-\kappa_f\right)\Delta i_{\text{bias}}(m_{\text{avg}}) + \ldots \left(1-\kappa_f\right) i_{\text{th}}(m_{\text{avg}})\Big) \tag{D.33}$$

where in turn i_{th} is expressed as (4.22). When furthermore using

$$\hat{\Delta} i_{L_f} = \max_{m_{\text{avg}}}\left(\tfrac{1}{2}\Delta i_{\text{sum}}(m_{\text{avg}}) + \Delta i_{\text{bias}}(m_{\text{avg}})\right) \tag{D.34}$$

which is based on (4.17), $\hat{i}$ becomes

$$\hat{i} = \hat{i}_{\text{out}} + \max_{m_{\text{avg}}} \Big(\Big(1+\kappa_f\Big) \frac{1}{2} \Delta i_{\text{sum}}(m_{\text{avg}}) + \Big(1-\kappa_f\Big) \Delta i_{\text{bias}}(m_{\text{avg}}) + \dots \\ \Big(1-\kappa_f\Big) \Big(\tfrac{1}{2} \Delta i_{\text{sum}}(m_{\text{avg}}) + \Delta i_{\text{bias}}(m_{\text{avg}}) \Big) \Big) \quad \text{(D.35)}$$

which can be rewritten to

$$\hat{i} = \hat{i}_{\text{out}} + \Big(1-\kappa_f\Big) \max_{m_{\text{avg}}} \Bigg(\Bigg(\frac{1+\kappa_f}{1-\kappa_f} + \lambda_{\text{th}} \Bigg) \tfrac{1}{2} \Delta i_{\text{sum}}(m_{\text{avg}}) + \dots \\ (1+\lambda_{\text{th}}) \, \Delta i_{\text{bias}}(m_{\text{avg}}) \Bigg). \quad \text{(D.36)}$$

Using (4.18), (4.19), and (5.28), (D.36) becomes

$$\hat{i} = \hat{i}_{\text{out}} + \tfrac{1}{2} \Big(1-\kappa_f\Big) \lambda_{\text{th}} \lambda_{\text{sum}} \hat{i}_{\text{out}} + \tfrac{1}{2} \Big(1+\kappa_f\Big) \lambda_{\text{sum}} \hat{i}_{\text{out}} \quad \text{(D.37a)}$$

for non-interleaved u_{sn}, and

$$\hat{i} = \hat{i}_{\text{out}} + 2 \Big(1-\kappa_f\Big) \max_{m_{\text{avg}}} \Bigg(\Bigg(\frac{1+\kappa_f}{1-\kappa_f} + \lambda_{\text{th}} \Bigg) \Big(|m_{\text{avg}}| - m_{\text{avg}}^2 \Big) + \dots \\ (1+\lambda_{\text{th}}) \, \frac{1+\kappa_f}{1-\kappa_f} \, (1 - |m_{\text{avg}}|) \Bigg) \lambda_{\text{sum}} \hat{i}_{\text{out}} \quad \text{(D.37b)}$$

for interleaved u_{sn}

D.3.2 RMS inductor current

Equation (D.30) can be written in terms of periodic average and switching ripple components as

$$I = \sqrt{\frac{1}{T_o} \int_{t}^{t+T_o} \Big(\tfrac{1}{2} \langle i_{\text{sum}}(\tau) \rangle + \tfrac{1}{2} \tilde{i}_{\text{sum}}(\tau) + \langle i_{\text{bias}}(\tau) \rangle + \tilde{i}_{\text{bias}}(\tau) \Big)^2 \, \mathrm{d}\tau} \quad \text{(D.38)}$$

which, when assuming $\langle i_{C_f} \rangle = 0$, becomes

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tfrac{1}{2} \tilde{i}_{\text{sum}}(\tau) + \tfrac{1}{2} \hat{i}_{\text{out}} + i_{\text{th}} + \tilde{i}_{\text{bias}}(\tau) \right)^2 \mathrm{d}\tau} \tag{D.39a}$$

for constant bias current, and

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tfrac{1}{2} \tilde{i}_{\text{sum}}(\tau) + \tfrac{1}{2} |i_{\text{out}}(\tau)| + i_{\text{th}} + \tilde{i}_{\text{bias}}(\tau) \right)^2 \mathrm{d}\tau} \tag{D.39b}$$

for modulated bias current.

Similarly as in (4.17) it can be shown that $\frac{1}{2}\tilde{i}_{\text{sum}} + \tilde{i}_{\text{bias}} = \tilde{i}_{L_{f_1}}$, which in turn results in

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tfrac{1}{2} \hat{i}_{\text{out}} + i_{\text{th}} + \tilde{i}_{L_f}(\tau) \right)^2 \mathrm{d}\tau} \tag{D.40a}$$

for constant bias current, and

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tfrac{1}{2} |i_{\text{out}}(\tau)| + i_{\text{th}} + \tilde{i}_{L_f}(\tau) \right)^2 \mathrm{d}\tau} \tag{D.40b}$$

for modulated bias current. From here on for clarity τ will be omitted from the equations.

When assuming $\langle i_{C_f} \rangle = 0$, (D.40) expands to

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \tfrac{1}{4} {i_{\text{out}}}^2 + \tfrac{1}{4} \hat{i}_{\text{out}}^2 + i_{\text{th}}^2 + \tilde{i}_{L_f}^2 + i_{\text{out}} \tilde{i}_{L_f} + \hat{i}_{\text{out}} i_{\text{th}} \mathrm{d}\tau} \tag{D.41a}$$

for constant bias current, and

$$I = \sqrt{\frac{1}{T_o} \int_t^{t+T_o} \tfrac{1}{4} {i_{\text{out}}}^2 + \tfrac{1}{4} |i_{\text{out}}|^2 + i_{\text{th}}^2 + \tilde{i}_{L_f}^2 + i_{\text{out}} \tilde{i}_{L_f} + |i_{\text{out}}| i_{\text{th}} \mathrm{d}\tau} \tag{D.41b}$$

for modulated bias. When, furthermore, assuming $T_o \gg T_{\text{sw}}$, then (D.41) simpli-

fies to

$$I \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}{i_{\text{out}}}^2 + \tfrac{1}{4}\tilde{i}_{\text{out}}^2 + i_{\text{th}}^2 + \tilde{i}_{L_f}^2 + \hat{i}_{\text{out}} i_{\text{th}} \mathrm{d}\tau} \tag{D.42a}$$

for constant bias current, and

$$I \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}{i_{\text{out}}}^2 + \tfrac{1}{4}|i_{\text{out}}|^2 + i_{\text{th}}^2 + \tilde{i}_{L_f}^2 + |i_{\text{out}}| i_{\text{th}} \mathrm{d}\tau} \tag{D.42b}$$

for modulated bias.

For sinusoidal i_{out}, when assuming peak switching current ripple, and by using (4.22), (D.42) becomes

$$I \approx \sqrt{\tfrac{3}{8}\tilde{i}_{\text{out}}^2 + \left(\lambda_{\text{th}}^2 + \tfrac{1}{3}R_R\right)\left(\hat{\Delta} i_{L_f}\right)^2 + \hat{i}_{\text{out}} \lambda_{\text{th}} \hat{\Delta} i_{L_f}} \tag{D.43a}$$

for constant bias current, and

$$I \approx \sqrt{\tfrac{1}{4}\tilde{i}_{\text{out}}^2 + \left(\lambda_{\text{th}}^2 + \tfrac{1}{3}R_R\right)\left(\hat{\Delta} i_{L_f}\right)^2 + \tfrac{2}{\pi}\hat{i}_{\text{out}} \lambda_{\text{th}} \hat{\Delta} i_{L_f}} \tag{D.43b}$$

for modulated bias current, where $\hat{\Delta} i_{L_f}$ is given by (D.34), and where R_R is the ratio between AC and DC wire resistance to take into account the skin and proximity effects.

The maximum inductor current ripple $\hat{\Delta} i_{L_f}$ can be rewritten using (4.18), (4.19), (5.12), and (5.13), resulting in

$$\hat{\Delta} i_{L_f} = \tfrac{1}{2}\lambda_{\text{sum}} \hat{i}_{\text{out}} \tag{D.44a}$$

for non-interleaved u_{sn}, and

$$\hat{\Delta} i_{L_f} = 2\lambda_{\text{sum}} \hat{i}_{\text{out}} \max_{m_{\text{avg}}} \left(\frac{1+\kappa_f}{1-\kappa_f} - \frac{2\kappa_f}{1-\kappa_f}|m_{\text{avg}}| - m_{\text{avg}}^2 \right) \tag{D.44b}$$

for interleaved u_{sn}.

D.3.3 Area product

Using (D.28), (D.37), (D.43), and (D.44), the area product for a DB with coupled inductors can be rewritten to

$$A_{P_{\mathrm{DB}}} = \frac{U_{\mathrm{DC}}\hat{i}_{\mathrm{out}}T_{\mathrm{sw}}}{8\hat{B}JK_{\mathrm{u}}}\frac{1}{1+\kappa}\hat{i}_{\mathrm{DB}}I_{\mathrm{DB}} \tag{D.45}$$

where the peak and RMS terms in (5.23) are given by

$$\hat{i}_{\mathrm{DB}} = 2\lambda_{\mathrm{sum}}^{-1} + \left(1-\kappa_f\right)\lambda_{\mathrm{th}} + \left(1+\kappa_f\right) \tag{D.46a}$$

and

$$I_{\mathrm{DB}} = \begin{cases} \sqrt{\frac{3}{8} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)\frac{1}{4}\lambda_{\mathrm{sum}}^2 + \frac{1}{2}\lambda_{\mathrm{th}}\lambda_{\mathrm{sum}}}, & \text{constant bias} \\ \sqrt{\frac{1}{4} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)\frac{1}{4}\lambda_{\mathrm{sum}}^2 + \frac{1}{\pi}\lambda_{\mathrm{th}}\lambda_{\mathrm{sum}}}, & \text{modulated bias} \end{cases} \tag{D.46b}$$

for non-interleaved u_{sn}, and

$$\hat{i}_{\mathrm{DB}} = \tfrac{1}{2}\lambda_{\mathrm{sum}}^{-1} + \left(1-\kappa_f\right)\max_{m_{\mathrm{avg}}}\left(\left(\frac{1+\kappa_f}{1-\kappa_f}+\lambda_{\mathrm{th}}\right)\left(|m_{\mathrm{avg}}| - m_{\mathrm{avg}}^2\right) + \ldots \right.$$
$$\left. (1+\lambda_{\mathrm{th}})\,\frac{1+\kappa_f}{1-\kappa_f}\left(1-|m_{\mathrm{avg}}|\right)\right) \tag{D.46c}$$

and

$$I_{\mathrm{DB}} = \begin{cases} \sqrt{\frac{3}{8} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)4\lambda_{\Delta}^2\lambda_{\mathrm{sum}}^2 + 2\lambda_{\mathrm{th}}\lambda_{\Delta}\lambda_{\mathrm{sum}}}, & \text{constant bias} \\ \sqrt{\frac{1}{4} + \left(\lambda_{\mathrm{th}}^2 + \frac{1}{3}R_R\right)4\lambda_{\Delta}^2\lambda_{\mathrm{sum}}^2 + \frac{4}{\pi}\lambda_{\mathrm{th}}\lambda_{\Delta}\lambda_{\mathrm{sum}}}, & \text{modulated bias} \end{cases} \tag{D.46d}$$

for interleaved u_{sn}. Finally, the ratio λ_{Δ} is given by

$$\lambda_{\Delta} = \max_{m_{\mathrm{avg}}}\left(\frac{1+\kappa_f}{1-\kappa_f} - \frac{2\kappa_f}{1-\kappa_f}\langle m_{\mathrm{avg}}\rangle - m_{\mathrm{avg}}^2\right). \tag{D.47}$$

D.4 The area product for a DB with tightly coupled inductors and an extra filter inductor

In [16] tight negative coupling is suggested for L_{bias} in combination with an external filter inductor for L_{sum}. Since this configuration needs two separate magnetic structures, (D.28) is expressed in terms of L_{bias} with perfect negative coupling ($\kappa_f = -1$), resulting in

$$A_{P_L} = \frac{L_{\text{bias}}}{2\hat{B}JK_{\text{u}}}\hat{i}I \tag{D.48}$$

where

$$\hat{i} = \max_t \left(i_{\text{bias}}(t)\right) \tag{D.49}$$

and

$$I = \sqrt{\frac{1}{T_o}\int_t^{t+T_o} \left(\tfrac{1}{2}i_{\text{sum}}(\tau) + i_{\text{bias}}(\tau)\right)^2 \mathrm{d}\tau}. \tag{D.50}$$

The total relative core volume, when assuming equal core geometric constants, becomes

$$V_N = \frac{{A_{P_L}}^{3/4} + {A_{P_{L_f}}}^{3/4}}{V_{\text{HB}}} \tag{D.51}$$

where V_{HB} is the inductor volume of the conventional equivalent HB, A_{P_L} is the area product of the tight negative coupled inductor, given by (D.48), and $A_{P_{L_f}}$ is the area product of the external filter inductor.

D.4.1 Peak currents

The peak current can be determined similarly as discussed in Section D.3.1, resulting in

$$\hat{i} = \tfrac{1}{2}\hat{i}_{\text{out}} + \tfrac{1}{2}\lambda_{\text{th}}\lambda_{L_f}\hat{i}_{\text{out}} \tag{D.52a}$$

for non-interleaved u_{sn}, and

$$\hat{i} = \tfrac{1}{2}\hat{i}_{\text{out}} + \max_{m_{\text{avg}}} \left(2\lambda_{\text{th}}\lambda_{L_f} \left(|m_{\text{avg}}| - m_{\text{avg}}^2 \right) + (1 + \lambda_{\text{th}})\, \lambda_{\text{bias}} \left(1 - |m_{\text{avg}}| \right) \right) \hat{i}_{\text{out}} \tag{D.52b}$$

for interleaved u_{sn}. The inductor current ripple ratio for the bias component λ_{bias}, is given by

$$\lambda_{\text{bias}} = \frac{\hat{\Delta} i_{\text{bias}}}{\hat{i}_{\text{out}}} \tag{D.53}$$

and is introduced because A_{P_L} is expressed in terms of L_{bias} instead of L_{sum}, which in turn is added externally.

D.4.2 RMS currents

The RMS currents are equal to (D.43a) for constant bias current and (D.43b) for modulated bias. However, $\hat{\Delta} i_{L_f}$ becomes $\hat{\Delta} i_L$ which is given by

$$\hat{\Delta} i_L = \max_{m_{\text{avg}}} \left(\tfrac{1}{2}\Delta i_{\text{sum}} + \Delta i_{\text{bias}} \right). \tag{D.54}$$

Using the above $\hat{\Delta} i_L$ becomes

$$\hat{\Delta} i_L = \tfrac{1}{2}\lambda_{L_f}\hat{i}_{\text{out}} \tag{D.55a}$$

for non-interleaved u_{sn}, and

$$\hat{\Delta} i_L = \max_{m_{\text{avg}}} \left(2\lambda_{L_f} \left(|m_{\text{avg}}| - m_{\text{avg}}^2 \right) + \lambda_{\text{bias}} \left(1 - |m_{\text{avg}}| \right) \right) \hat{i}_{\text{out}} \tag{D.55b}$$

for interleaved u_{sn}.

D.4.3 Area product

For the area products L_{bias} needs to be expressed in terms of λ_{bias}. Using (4.19) L_{bias} becomes

$$L_{\text{bias}} = \frac{U_{\text{DC}} T_{\text{sw}}}{4\lambda_{\text{bias}}\hat{i}_{\text{out}}} \tag{D.56}$$

for interleaved u_{sn}. For non-interleaved u_{sn}, Δi_{bias} is assumed zero, however, the maximum bias ripple can still be expressed in terms of λ_{bias} as

$$L_{\mathrm{bias}} = \frac{U_{\mathrm{DC}} T_{\mathrm{sw}}}{8\lambda_{\mathrm{bias}} \hat{i}_{\mathrm{out}}}. \tag{D.57}$$

Using the results of (D.48), (D.52b), (D.53), and (D.55), the area product A_{P_L} becomes

$$\frac{U_{\mathrm{DC}} \hat{i}_{\mathrm{out}} T_{\mathrm{sw}}}{8\hat{B}JK_{\mathrm{u}}} \hat{i}_N I_N \tag{D.58}$$

with

$$\hat{i}_N = \tfrac{1}{4}\lambda_{\mathrm{bias}}^{-1} + \tfrac{1}{4}\lambda_{\mathrm{th}} \frac{\lambda_{L_f}}{\lambda_{\mathrm{bias}}} \tag{D.59a}$$

for non-interleaved u_{sn} and

$$\hat{i}_N = \tfrac{1}{2}\lambda_{\mathrm{bias}}^{-1} + \max_{m_{\mathrm{avg}}} \left(2\lambda_{\mathrm{th}} \frac{\lambda_{L_f}}{\lambda_{\mathrm{bias}}} \left(|m_{\mathrm{avg}}| - m_{\mathrm{avg}}^2 \right) + (1 + \lambda_{\mathrm{th}}) \left(1 - |m_{\mathrm{avg}}| \right) \right) \tag{D.59b}$$

for interleaved u_{sn}, and

$$I_N = \sqrt{\tfrac{3}{8} + \left(\lambda_{\mathrm{th}}^2 + \tfrac{1}{3} R_R \right) \lambda_\Delta^2 \lambda_{\mathrm{bias}}^2 + \lambda_{\mathrm{th}} \lambda_\Delta \lambda_{\mathrm{bias}}} \tag{D.60a}$$

for constant bias current and

$$I_N = \sqrt{\tfrac{1}{4} + \left(\lambda_{\mathrm{th}}^2 + \tfrac{1}{3} R_R \right) \lambda_\Delta^2 \lambda_{\mathrm{bias}}^2 + \tfrac{2}{\pi} \lambda_{\mathrm{th}} \lambda_\Delta \lambda_{\mathrm{bias}}} \tag{D.60b}$$

for modulated bias current, with

$$\lambda_\Delta = \tfrac{1}{2} \frac{\lambda_{L_f}}{\lambda_{\mathrm{bias}}} \tag{D.60c}$$

for non interleaved u_{sn} and

$$\lambda_\Delta = \max_{m_{\mathrm{avg}}} \left(2 \frac{\lambda_{L_f}}{\lambda_{\mathrm{bias}}} \left(|m_{\mathrm{avg}}| - m_{\mathrm{avg}}^2 \right) + 1 - |m_{\mathrm{avg}}| \right) \tag{D.60d}$$

for interleaved u_{sn}.

The area product of the external filter inductor equals

$$A_{P_{L_f}} = A_{P_{\text{HB}}} \tag{D.61a}$$

for non-interleaved u_{sn}, and

$$A_{P_{L_f}} = \tfrac{1}{2} A_{P_{\text{HB}}} \tag{D.61b}$$

for interleaved u_{sn}.

The area product of the HB is given by (5.8) and the factor 1/2 in the area product for interleaved u_{sn} is used because of the ratio between $\hat{\Delta} i_{L_f}$ for non-interleaved and interleaved u_{sn}. The volume increase with respect to the conventional HB can be determined using (D.51)

D.5 The peak and RMS currents for an ABDB

For the derivation of the peak and RMS inductor currents of the ABDB the same assumptions and notations are used as described in the previous sections for the conventional DB. Again the inductor currents can be separated in a periodic average and a high frequency ripple as

$$i_{L_{fx}} = \langle i_{L_{fx}} \rangle + \tilde{i}_{L_{fx}} \tag{D.62}$$

$$i_{L_{a_x}} = \langle i_{L_{a_x}} \rangle + \tilde{i}_{L_{a_x}} \tag{D.63}$$

which, when assuming that $i_{\text{diff}} = 0$, equals

$$i_{L_{fx}} = \tfrac{1}{2} \langle i_{\text{sum}} \rangle + \tilde{i}_{L_{fx}} \tag{D.64}$$

$$i_{L_{a_x}} = \langle i_{\text{bias}_x} \rangle + \tilde{i}_{L_{a_x}}. \tag{D.65}$$

When neglecting $\langle i_{C_f} \rangle$, which is small in practice, i_{L_f} becomes

$$i_{L_{fx}} = \tfrac{1}{2} i_{\text{out}} + \tilde{i}_{L_{fx}}. \tag{D.66}$$

The absolute peak and RMS current of L_{a_1} and L_{a_2} are equal, therefore only the

inductor that carries positive current is considered from here on, resulting in

$$i_{L_{a_2}} = \begin{cases} \frac{1}{2}\hat{i}_{\text{out}} + \lambda_{\text{th}} \left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f} \right) + \tilde{i}_{L_a}, & \text{constant bias} \\ \frac{1}{2}|i_{\text{out}}| + \lambda_{\text{th}} \left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f} \right) + \tilde{i}_{L_a}, & \text{modulated bias} \end{cases} \tag{D.67}$$

where the sum of the peak inductor current ripples $\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f} \right)$ is the minimum required current for CCM, and λ_{th} is an additional safety factor to prevent DCM during transients.

D.5.1 Peak current

When assuming that maximum output current coincides with the maximum filter inductor current ripple, the peak current L_f becomes

$$\hat{i}_{L_{fx}} = \tfrac{1}{2}\hat{i}_{\text{out}} + \hat{\Delta} i_{L_f} \tag{D.68}$$

$$\hat{i}_{L_{a_2}} = \tfrac{1}{2}\hat{i}_{\text{out}} + (1 + \lambda_{\text{th}})\hat{\Delta} i_{L_a} + \lambda_{\text{th}} \hat{\Delta} i_{L_f} \tag{D.69}$$

which is worst-case and only valid for a pure inductive load. Therefore, in all other cases a conservative penalty on inductor current ripple is applied.

D.5.2 RMS current filter inductor current

The RMS value of $i_{L_{fx}}$ over a cycle time T_o is given by

$$I_{L_{fx}} \approx \sqrt{\frac{1}{T_o} \int_{t}^{t+T_o} \left(\tfrac{1}{2} i_{\text{out}}(\tau) + \tilde{i}_{L_{fx}}(\tau) \right)^2 \mathrm{d}\tau}. \tag{D.70}$$

Expansion of the quadratic term in the integral leads to

$$I_{L_{fx}} \approx \sqrt{\frac{1}{T_o} \int_{t}^{t+T_o} \tfrac{1}{4} \left(i_{\text{out}}(\tau) \right)^2 + \left(\tilde{i}_{L_{fx}}(\tau) \right)^2 + i_{\text{out}}(\tau) \tilde{i}_{L_{fx}}(\tau) \mathrm{d}\tau}. \tag{D.71}$$

When assuming $T_{\text{sw}} \ll T_o$ the cross term becomes zero and (D.71) can be approx-

imated by

$$I_{L_{fx}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}\left(i_{\text{out}}(\tau)\right)^2 + \left(\tilde{i}_{L_{fx}}(\tau)\right)^2 \mathrm{d}\tau} \tag{D.72}$$

which in turn when assuming sinusoidal output current and maximum inductor current ripple, becomes

$$I_{L_{fx}} \approx \sqrt{\tfrac{1}{8}\hat{i}_{\text{out}}^2 + \tfrac{1}{3}(\hat{\Delta} i_{L_f})^2}. \tag{D.73}$$

D.5.3 RMS auxiliary inductor current for constant bias

The RMS value of $i_{L_{a_x}}$ for constant bias current over a cycle time T_o is given by

$$I_{L_{a_x}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \left(\tfrac{1}{2}\hat{i}_{\text{out}} + \lambda_{\text{th}}\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f}\right) + \tilde{i}_{L_a}(\tau)\right)^2 \mathrm{d}\tau}. \tag{D.74}$$

When assuming that the switching ripple has zero average, (D.74) becomes

$$I_{L_{a_x}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}\hat{i}_{\text{out}}^2 + \lambda_{\text{th}}^2\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f}\right)^2 + \left(\tilde{i}_{L_a}(\tau)\right)^2 + \hat{i}_{\text{out}}\lambda_{\text{th}}\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f}\right) \mathrm{d}\tau} \tag{D.75}$$

which in turn, when assuming maximum inductor current ripple, becomes

$$I_{L_{a_x}} \approx \sqrt{\tfrac{1}{4}\hat{i}_{\text{out}}^2 + \lambda_{\text{th}}^2\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f}\right)^2 + \frac{1}{3}\left(\hat{\Delta} i_{L_a}\right)^2 + \hat{i}_{\text{out}}\lambda_{\text{th}}\left(\hat{\Delta} i_{L_a} + \hat{\Delta} i_{L_f}\right)}. \tag{D.76}$$

In this thesis only modulated bias current is considered for the ABDB.

D.5.4 RMS auxiliary inductor current for modulated bias

The RMS value of $i_{L_{a_x}}$ for modulated bias current over a cycle time T_o is given by

$$I_{L_{a_x}} \approx \sqrt{\frac{1}{T_o}\int_{t}^{t+T_o}\left(\tfrac{1}{2}|i_{\text{out}}(\tau)| + \lambda_{\text{th}}\left(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f}\right) + \tilde{i}_{L_a}(\tau)\right)^2 \mathrm{d}\tau}. \tag{D.77}$$

When assuming that the switching ripple has zero average and $T_{\text{sw}} \ll T$, (D.77) can be approximated as

$$I_{L_{a_x}} \approx \left(\frac{1}{T_o}\int_{t}^{t+T_o} \tfrac{1}{4}\left(i_{\text{out}}(\tau)\right)^2 + \lambda_{\text{th}}^2\left(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f}\right)^2 + \left(\tilde{i}_{L_a}(\tau)\right)^2 + \ldots \right.$$
$$\left. |i_{\text{out}}|\lambda_{\text{th}}\left(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f}\right)\mathrm{d}\tau\right)^{\frac{1}{2}} \tag{D.78}$$

which in turn, when assuming sinusoidal output current, becomes

$$I_{L_{a_x}} \approx \sqrt{\tfrac{1}{8}\hat{i}_{\text{out}}^2 + \lambda_{\text{th}}^2\left(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f}\right)^2 + \tfrac{1}{3}\left(\hat{\Delta}i_{L_a}\right)^2 + \tfrac{2}{\pi}\hat{i}_{\text{out}}\lambda_{\text{th}}\left(\hat{\Delta}i_{L_a} + \hat{\Delta}i_{L_f}\right)}. \tag{D.79}$$

Nomenclature

Operators

Operator	Description
$\lvert \cdot \rvert$	absolute value
$\angle \cdot$	argument of a complex number
$\langle \cdot \rangle$	(moving/periodic) average value
$\Delta \cdot$	ripple amplitude, or deviation from a nominal value
$\tilde{\cdot}$	ripple or small signal perturbation
$\hat{\cdot}$	peak or maximum value (over one switching cycle)
$\check{\cdot}$	lowest or minimum value (over one switching cycle)
$\mathring{\cdot}$	estimated or measured value
$\cdot^*$	reference input or desired value
$\cdot^\sim$	disturbance input or signal
$\cdot^\mathsf{T}$	(conjugate) transpose of a vector or matrix
$\cdot^{-1}$	inverse of a nonsingular matrix
$\cdot^+$	Moore-Penrose pseudo inverse of a matrix
$\operatorname{diag}(a_1, \ldots, a_n)$	$n \times n$ diagonal matrix whose diagonal entries starting in the upper left corner are $a_1, \ldots, a_n$
$\det(\cdot)$	determinant of a square matrix
$\operatorname{null}(\cdot)$	a matrix columns of which are a basis of the null space

Operator	Description
sgn $(\cdot)$	sign of a scalar or of vector elements
min $(\cdot)$	minimum value of a function or vector
max $(\cdot)$	maximum value of a function or vector
num $(\cdot)$	numerator of a polynomial
den $(\cdot)$	denominator of a polynomial
pole $(\cdot)$	poles of a dynamic system
zero $(\cdot)$	zeros of a dynamic system
$\Re(\cdot)$	real part
$\Im(\cdot)$	imaginary part
BW $(\cdot)$	bandwidth of a dynamic system

Notation

Notation	Description
$\mathbf{x}$	vectors are denoted by bold lower case variables
$\mathbf{X}$	matrices are denoted by bold capital variables
$\mathbf{I}^n$	Identity matrix of size $n \times n$
$\mathbf{0}^{n\times m}$	Zero matrix of size $n \times m$
$U_x,\ I_x$	denote RMS, DC, or magnitude spectra of u_x and i_x respectively
j	imaginary unit, $j = \sqrt{-1}$

Symbols

Arabic

Symbol	Unit	Description	First use on page
A_C	m^2	effective magnetic core cross-section area	87
A_{Cu}	m^2	wire core cross-section area	87
A_P	m^4	area-product of an inductor	87
B	T	magnetic flux density (1 T=1 Wb m^{-2})	87
C_{AC}	F	anode-cathode capacitance of a diode	124
C_{CE}	F	collector-emitter capacitance of an IGBT	124
C_{CG}	F	collector-gate capacitance of an IGBT	129
C_{DC}	F	DC bus capacitance of a switching leg or converter	33

Symbol	Unit	Description	First use on page
C_f	F	filter capacitance	26
$C_{f_{\text{DM}}}$	F	DM filter capacitance, connected across the load	161
C_{GE}	F	gate-emitter capacitance of an IGBT	127
D_x	-	semiconductor diode x	26
f_c	Hz	cut-off frequency of a filter	143
f_d	Hz	frequency of a disturbance signal	32
f_o	Hz	reference or output frequency	27
f_{clk}	Hz	clock frequency of PWM generator	27
f_{sw}	Hz	switching frequency	28
g_m	A V^{-1}	transconductance (of a semiconductor switch)	127
i_{bias}	A	bias current required for a DB	58
i_{bias_x}	A	bias current of switching leg x required for a DB	170
i_C	A	collector current	127
$i_{C_{\text{sat}}}$	A	saturation collector current	127
i_{C_f}	A	current flowing through a filter capacitor	66
$i_{C_{f_{\text{DM}}}}$	A	decoupled CM filter capacitor current	170
$i_{C_{f_{\text{CM}}}}$	A	decoupled DM filter capacitor current	170
i_{diff}	A	current difference between $i_{L_{f_1}}$ and $i_{L_{f_2}}$ of an ABDB	82
i_{D_x}	A	current flowing through diode x	76
i_{L_a}	A	current flowing through L_a	82
$i_{L_{a_x}}$	A	current flowing through auxiliary inductor x	78
i_{L_f}	A	current flowing through L_f	62
$i_{L_{f_x}}$	A	current flowing through filter inductor x	58
$i_{L_{\text{HB}}}$	A	current flowing through L_{HB}	30
$i_{L_{\text{HB}_x}}$	A	current flowing through L_{HB_x}	214
i_{out}	A	current flowing to the load circuit	7
i_{sum}	A	sum of the inductor currents of a DB	66
i_{sum_x}	A	sum of the inductor currents of switching leg x of a DB	175
i_{S_x}	A	current flowing through switch x	76
i_{th}	A	offset current that is added to i_{bias} of a DB	59
i'_{th}	A	offset current that is added to i_{L_a} of an ABDB	79
J	A m^{-2}	current density in a wire	87
K_{u}	-	winding-window utilization factor	87
K_{vol}	-	magnetic core volumetric constant	87
L	H	(load) inductance	87
L_a	H	auxiliary inductance of an ABDB	80
L_{a_x}	H	auxiliary inductance of switching leg x of an ABDB	82
L_{bias}	H	inductance present in the bias current path	67

Symbol	Unit	Description	First use on page
L_f	H	filter inductances of a DB or ABDB	61
L_{f_x}	H	DB or ABDB filter inductance x	57
L_{HB}	H	filter inductances of an HB	26
L_{sum}	H	inductance present in the sum current path	67
M	H	mutual inductance	92
m	-	modulation index of an HB switching leg, $m = 2\delta - 1$	27
m_x	-	modulation index of switching leg x, $m_x = 2\delta_x - 1$	62
m_{avg}	-	modulation index that drives the output of a DB	66
$m_{\text{avg}_{\text{DM}}}$	-	modulation index that drives the DM output of a FB equivalent DB	199
m_{bias}	-	modulation index that drives i_{bias} of a DB	66
m_{bias_x}	-	modulation index that drives i_{bias_x} of a DB or $i_{L_{a_x}}$ of an ABDB switching leg	80
n	-	number of turns in a winding	289
P_D^{con}	W	diode conduction losses	76
$P_{R_{L_f}}$	W	power dissipated in R_{L_f}	71
$P_{R_{L_{\text{HB}}}}$	W	power dissipated in $R_{L_{\text{HB}}}$	75
P_S^{con}	W	switch conduction losses	76
$\mathfrak{R}$	H^{-1}	magnetic reluctance (1 Turns/H=1 A$\cdot$ Turns /Wb)	93
R	Ω	(load) resistance	33
R_{C_f}	Ω	series resistance of a filter capacitor	46
R_f	Ω	on-resistance of a diode	46
$R_{g_{\text{on}}}$	Ω	gate turn-on resistance	127
$R_{g_{\text{off}}}$	Ω	gate turn-off resistance	127
R_{L_a}	Ω	series resistance of L_a	106
$R_{L_{\text{bias}}}$	Ω	series resistance of L_{bias}	74
R_{L_f}	Ω	series resistance of L_f	74
$R_{L_{\text{HB}}}$	Ω	series resistance of L_{HB}	46
$R_{L_{\text{sum}}}$	Ω	series resistance of L_{sum}	74
R_{on}	Ω	on-resistance of a semiconductor switch	46
R_R	-	ratio between the AC and DC wire resistance	89
R_w	Ω	wire and/or output resistance of a power supply	32
S_x	-	semiconductor switch x or its corresponding gating/control signal	6
T_{bt}	s	blanking time added between switching to prevent short circuit	29
T_o	s	reference or output cycle time	49
T_s	s	sampling time of a discrete control system	165

Symbol	Unit	Description	First use on page
T_{sw}	s	switching time of a switching leg, $T_{sw} = 1/f_{sw}$	17
T_x^n	s	on-time of a low-side switch or diode of leg x	76
T_x^p	s	on-time of a high-side switch or diode of leg x	62
t	s	time	17
U_{DC}	V	DC supply voltage	26
$U_{dr_{on}}$	V	Gate driver turn-on voltage	127
$U_{dr_{off}}$	V	Gate driver turn-off voltage	127
u_a	V	switch-node voltage on the auxiliary-leg of an ABDB	107
u_{a_x}	V	switch-node voltage of auxiliary-leg x of an ABDB	80
u_{avg}	V	average voltage that drives the load of a DB or ABDB	66
u_{avg_x}	V	u_{avg} corresponding to converter side x	142
$u_{avg_{CM}}$	V	common mode u_{avg}, source of EMI	142
$u_{avg_{DM}}$	V	differential mode u_{avg}, contributes to output power	142
u_{bias}	V	bias voltage that drives i_{bias} of a DB	66
u_{bias_x}	V	bias voltage that drives i_{bias_x} of a DB, or $i_{L_{a_x}}$ for an ABDB switching leg	80
u_{bt}	V	voltage error due to blanking time	45
u_c	V	output voltage of power supply series compensation	251
u_{CE}	V	collector emitter voltage of an IGBT	127
u_{C_f}	V	filter capacitor voltage	61
$u_{C_{fx}}$	V	filter capacitor voltage of converter side x	195
u_{diff}	V	voltage that drives i_{diff}	153
u_{diff_x}	V	voltage that drives i_{diff} of converter side x	156
u_{DS}	V	drain source voltage of a MOSFET	78
u_{GE}	V	gate emitter voltage of an IGBT	127
u_{out}	V	output voltage of the converter, i.e. DM voltage across the load	7
$u_{out_{CM}}$	V	CM output voltage of the converter, i.e. CM voltage across the load	171
u_{sn}	V	switch-node voltage of a switching leg	6
u_{sn_x}	V	switch-node voltage of switching leg x	66
$u_{sn_{CM}}$	V	common-mode switching voltage	142
$u_{sn_{DM}}$	V	differential mode switching voltage	142
V	m^3	volume	290
V_f	V	on-voltage of a diode	46
V_{mil}	V	Miller voltage of a semiconductor switch	129
V_{on}	V	on-voltage of a semiconductor switch	46
V_{th}	V	gate turn-on threshold voltage of a semiconductor switching device	127

Symbol	Unit	Description	First use on page
W_A	m^2	magnetic core winding cross-section area	87
Z_{DC}	Ω	output impedance of DC power supply	251
Z_w	Ω	wiring impedance	251

Greek

Symbol	Unit	Description	First use on page
δ	-	duty ratio of a switching leg, i.e. the relative on-time of the high-side switch or diode	17
δ_x	-	duty ratio of switching leg x	116
ζ	-	damping ratio	175
κ_f	-	coupling coefficient of inductors including the sign of the coupling	92
λ_Δ	-	correction for the relative current ripple amplitude in case of interleaved u_{sn} for the calculation of the area-product of the DB with coupled inductors	95
λ_{bias}	-	inductor current ripple ratio $\lambda_{bias} = \hat{\Delta}i_{bias}/\hat{i}_{out}$	301
λ_{L_a}	-	inductor current ripple ratio $\lambda_{L_a} = \hat{\Delta}i_{L_a}/\hat{i}_{out}$	104
λ_{L_f}	-	inductor current ripple ratio $\lambda_{L_f} = \hat{\Delta}i_{L_f}/\hat{i}_{out}$	89
$\lambda_{L_{HB}}$	-	inductor current ripple ratio $\lambda_{L_{HB}} = \hat{\Delta}i_{L_{HB}}/\hat{i}_{out}$	89
λ_{sum}	-	inductor current ripple ratio $\lambda_{L_f} = \hat{\Delta}i_{sum}/\hat{i}_{out}$	95
λ_{th}	-	relative amount added to the minimum offset current required to prevent DCM, $\lambda_{th} = i_{th}/\hat{\Delta}i_{L_x}$	70
Φ	Wb	magnetic flux (1 Wb=1 Vs)	93
ϕ	rad	phase (shift)	140
ϕ_d	rad	phase of a disturbance frequency	32
ϕ_o	rad	phase of a reference or output frequency	32

Acronyms

Acronym	Description	First use on page
ABDB	auxiliary-bias dual-buck converter	78
AC	alternating current	61
ADC	analog-to-digital converter	100
BCM	boundary conduction mode	65
BJT	bipolar junction transistor	78

Acronym	Description	First use on page
CCM	continuous conduction mode	59
CM	common-mode	139
CMRR	common-mode rejection ratio	148
CSI	current-source inverter	52
CT	computer tomography	8
DAE	differential algebraic equation	20
DB	dual-buck converter	52
DC	direct current	4
DCM	discontinuous conduction mode	40
DM	differential-mode	139
DPWM	digital (or discrete) pulse-width modulation	27
DSP	digital signal processor	140
EMC	electromagnetic compatibility	138
EMI	electromagnetic interference	51
FB	full-bridge converter	34
FPGA	field-programmable gate array	98
HB	half-bridge converter	26
HD	harmonic distortion	221
IC	integrated-circuit	27
IGBT	insulated-gate bipolar-transistor	46
LTI	linear time-invariant	16
LQR	linear-quadratic regulator	192
MIMO	multiple-input multiple-output	169
MOSFET	metal-oxide semiconductor field-effect transistor	46
MPC	model-predictive control	160
MRI	(nuclear) magnetic resonance imaging	50
OCC	opposed-current converter	61
ODE	ordinary differential equation	20
PID	proportional-integral-differential control	199
PWM	pulse-width-modulation/modulated	17
RMS	root mean square	28
ROO	reduced-order observer	195
RPI	resonant-pole inverter	51
SEB	single-event burn-out	8
SEM	scanning-electron-microscope	60
SISO	single-input single-output	160
SMPA	switched-mode power amplifier	240
SMPC	switched-mode power converter	16
SNR	signal-to-noise ratio	29

Acronym	Description	First use on page
THD	total harmonic distortion	28
WHD	weighted harmonic distortion	143
WTHD	weighted total harmonic distortion	143
ZOH	zero-order-hold	140
ZVS	zero-voltage switching	40

Bibliography

[1] J. H. Allmeling and W. P. Hammer, "PLECS-piece-wise linear electrical circuit simulation for Simulink," in *Proceedings of the IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, vol. 1. IEEE, 1999, pp. 355–360. Cited on page 127.

[2] F. Amato, C. Cosentino, F. A. S., and A. Merola, "Stabilization of bilinear systems via linear state-feedback control," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 1, pp. 76–80, 2009. Cited on page 160.

[3] C. Attaianese, V. Nardi, and G. Tomasso, "A novel SVM strategy for VSI dead-time-effect reduction," *IEEE Transactions on Industry Applications*, vol. 41, no. 6, pp. 1667 –1674, nov.-dec. 2005. Cited on pages 50 and 51.

[4] C. Audet and J. E. Dennis Jr, "Analysis of generalized pattern searches," *SIAM Journal on Optimization*, vol. 13, pp. 889–903, 2002. Cited on page 182.

[5] M. Berkhout, "A class D output stage with zero dead time," in *Digest of technical papers of the IEEE International Solid-State Circuits Conference (ISSCC)*, 2003, pp. 134–135. Cited on page 51.

[6] B. Bidoggia, R. Maheshwari, R. Nielsen, S. Munk-Nielsen, and F. Blaabjerg, "Steady-state analysis of dead-time effect on bidirectional buck converters," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 792–797. Cited on page 38.

[7] V. Biolkova, Z. Kolka, and D. Biolek, "State-space averaging (SSA) revisited: on the accuracy of SSA-based line-to-output frequency responses of switched DC-DC converters," *WSEAS Transactions on Circuits and Systems*, vol. 2, p. 1, 2010. Cited on page 18.

[8] T. H. Blakesley, "A new electrical theorem," *Proceedings of the Physical Society of London*, vol. 13, no. 1, pp. 65–67, 1894. Cited on page 58.

[9] N. Bouhalli, "Etude et intégration de convertisseurs multicellulaires parallèles entrelacés et magnétiquement couplés," Ph.D. dissertation, Institut National Polytechnique de Toulouse, 2009. Cited on pages 86 and 91.

[10] N. Bouhalli, E. Sarraute, T. Meynard, M. Cousineau, and E. Laboure, "Optimal multi-phase coupled buck converter architecture dedicated to strong power system integration," in *Proceedings of the 4th Institute of Engineering and Technology conference on Power Electronics, Machines and Drives (PEMD)*, 2008, pp. 352–356. Cited on page 57.

[11] S. Boyd and L. Vandenberghe, *Convex Optimization*. Cambridge University Press, 2009. Cited on page 180.

[12] J. B. Burl, *Linear optimal control: H_2 and H_∞ methods*. Menlo Park, CA: Addison Wesley Longman, 1999. Cited on pages 177, 187, 191, and 196.

[13] S. Buso and P. Mattavelli, "Digital control in power electronics," *Lectures on Power Electronics*, vol. 1, no. 1, pp. 1–158, 2006. Cited on pages 27 and 28.

[14] H. Butler, "Position control in lithographic equipment [applications of control]," *IEEE Control Systems*, vol. 31, no. 5, pp. 28–47, 2011. Cited on page 8.

[15] M. L. A. Caris, H. Huisman, J. M. Schellekens, and J. L. Duarte, "Generalized harmonic elimination method for interleaved power amplifiers," in *Proceedings of the 38th annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 4961–4966. Cited on pages 80 and 243.

[16] C. Chapelsky, J. Salmon, and A. M. Knight, "High-quality single-phase power conversion by reconsidering the magnetic components in the output stage, building a better half-bridge," *IEEE Transactions on Industry Applications*, vol. 45, no. 6, pp. 2048–2055, nov. 2009. Cited on pages 86, 91, 96, 97, 107, and 300.

[17] J. Cho, D. Hu, and G. Cho, "Three phase sine wave voltage source inverter using the soft switched resonant poles," in *Proceedings of the 15th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, nov 1989, pp. 48–53 vol.1. Cited on pages 51 and 56.

[18] K. M. Cho, W. S. Oh, Y. T. Kim, and H. J. Kim, "A new switching strategy for pulse width modulation (PWM) power converters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 330–337, 2007. Cited on page 51.

[19] C.-H. Choi and J.-K. Seok, "Compensation of zero-current clamping effects in high-frequency-signal-injection-based sensorless pm motor drives," *IEEE Transactions on Industry Applications*, vol. 43, no. 5, pp. 1258–1265, 2007. Cited on page 48.

[20] S. Ćuk, "General topological properties of switching structures," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, 1979, pp. 109–130. Cited on page 56.

[21] S. Ćuk, "New magnetic structures for switching converters," *IEEE Transactions on Magnetics*, vol. 19, no. 2, pp. 75–83, 1983. Cited on pages 87 and 289.

[22] R. W. De Doncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Conference record of the IEEE Industry Applications Society (IAS) annual meeting*, 1990, pp. 1228–1235. Cited on pages 51 and 56.

[23] C. A. Desoer and E. S. Kuh, *Basic Circuit Theory*. Tata McGraw-Hill Education, 1984. Cited on page 58.

[24] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Transactions on Industry Applications*, vol. 25, no. 4, pp. 634–643, 1989. Cited on pages 51 and 56.

[25] A. Domahidi, "FORCES: Fast optimization for real-time control on embedded systems," http://forces.ethz.ch, Oct. 2012. Cited on page 160.

[26] J. L. Duarte, "Small-signal modelling and analysis of switching converters using MATLAB," *International Journal of Electronics*, vol. 85, no. 2, pp. 231–269, 1998. Cited on pages 16, 20, and 160.

[27] R. W. Erickson and R. D. Middlebrook, "Origins of harmonic distortion in switching amplifiers," in *Proceedings of the 4^{th} annual International Power Conversion Conference*, 1982, pp. 567–582. Cited on pages 112, 119, and 133.

[28] R. W. Erickson, "Large signals in switching converters," Ph.D. dissertation, California Institute of Technology, 1983. Cited on page 112.

[29] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics. Second Edition.* Kluwer Academic Publishers, 2000. Cited on pages 46 and 273.

[30] J. Ewanchuk, J. Salmon, and B. Vafakhah, "A five/nine-level twelve-switch neutral point clamped inverter for high speed electric drives," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 2333–2340. Cited on page 61.

[31] C. W. Gear and L. R. Petzold, "ODE methods for the solution of differential/algebraic systems," *SIAM Journal on Numerical Analysis*, vol. 21, no. 4, pp. 716–728, 1984. Cited on page 20.

[32] C. W. Gear, "Differential-algebraic equation index transformations," *SIAM Journal on Scientific and Statistical Computing*, vol. 9, no. 1, pp. 39–47, 1988. Cited on page 20.

[33] A. Griffoni, J. van Duivenbode, D. Linten, E. Simoen, P. Rech, L. Dilillo, F. Wrobel, P. Verbist, and G. Groeseneken, "Neutron-induced failure in silicon IGBTs, silicon super-junction and SiC MOSFETs," *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, pp. 866–871, 2012. Cited on page 8.

[34] S. Guo and A. Q. Huang, "Control and analysis of the high efficiency split phase PWM inverter," in *Proceedings of the 19th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014. Cited on page 61.

[35] W. Hammer, "Dynamic modeling of line and capacitor commutated converters for HVDC power transmission," Ph.D. dissertation, Swiss Federal Institute of technology (ETH) Zürich, 2003. Cited on page 20.

[36] M. Hartmann, S. Round, H. Ertl, and J. Kolar, "Digital current controller for a 1 MHz, 10 kW three-phase VIENNA rectifier," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2496–2508, 2009. Cited on page 29.

[37] J. L. Hellerstein, Y. Diao, S. Perekh, and D. M. Tilbury, *Feedback Control of Computing Systems*. John Wiley & Sons, Inc., 2004. Cited on page 190.

[38] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice (IEEE Press Series on Power Engineering)*. Wiley-IEEE Press, 2003. Cited on pages 27, 132, and 140.

[39] J. Honda and J. Adams. Class D audio amplifier basics. Application note AN-1071. International rectifier. http://www.irf.com/technical-info/appnotes/an-1071.pdf. Cited on pages 34 and 139.

[40] K. Hyun-Soo, M. Hyung-Tae, and Y. Myung-Joong, "On-line dead-time compensation method using disturbance observer," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1336–1345, nov. 2003. Cited on page 50.

[41] C. Jettanasen, F. Costa, and C. Vollaire, "Common-mode emissions measurements and simulation in variable-speed drive systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2456–2464, 2009. Cited on page 142.

[42] R. E. Kalman, "Contributions to the theory of optimal control," in *Control Theory: Twenty-Five Seminal Papers (1932-1981)*. Wiley-IEEE Press, 2001, pp. 147–166. Cited on pages 186 and 192.

[43] J. G. Kassakian, M. F. Schlecht, and G. C. Verghese, *Principles of Power Electronics*. Pearson Education, 1992. Cited on pages 16, 18, 20, 160, and 273.

[44] J. Kautsky, N. Nichols, and P. Van Dooren, "Robust pole assignment in linear state feedback," *International Journal of Control*, vol. 41, no. 5, pp. 1129–1155, 1985. Cited on pages 192 and 193.

[45] F. H. Khan, L. M. Tolbert, and F. Z. Peng, "Deriving new topologies of dc-dc converters featuring basic switching cells," in *IEEE Workshops on Computers in Power Electronics (COMPEL)*, july 2006, pp. 328 –332. Cited on page 56.

[46] A. Knott, T. Stegenborg-Andersen, O. C. Thomsen, D. Bortis, J. W. Kolar, G. Pfaffinger, and M. A. E. Andersen, "Modeling distortion effects in class-D amplifier filter inductors," in *Audio Engineering Society Convention 128*, 2010. Cited on page 38.

[47] F. Koeslag, H. T. du Mouton, H. J. Beukes, and P. Midya, "A detailed analysis of the effect of dead time on harmonic distortion in a class D audio amplifier," in *Proceedings of the AFRICON conference*, 2007, pp. 1–7. Cited on page 48.

[48] E. E. Landsman, "A unifying derivation of switching DC-DC converter topologies," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, 1979, pp. 239–243. Cited on page 56.

[49] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compensator for PWM voltage inverters," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 2, pp. 191–197, apr 1997. Cited on pages 50 and 51.

[50] E. Lemmen, J. M. Schellekens, C. G. E. Wijnands, and J. L. Duarte, "The extra L opposed current converter," in *Proceedings of the 29th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 1304–1311. Cited on pages 55, 59, 238, and 243.

[51] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1320–1333, 2008. Cited on page 7.

[52] J. Liu and Y. Yan, "A novel hysteresis current controlled dual buck half bridge inverter," in *Proceedings of the 34th Annual IEEE Power Electronics Specialist Conference (PESC)*, vol. 4, 2003, pp. 1615–1620. Cited on pages 61 and 86.

[53] M. Liu, F. Hong, and C. Wang, "A novel flying-capacitor dual buck three-level inverter," in *Proceedings of the 28th annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 502–506. Cited on page 61.

[54] Y. Lobsiger and J. W. Kolar, "Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4754–4761. Cited on page 130.

[55] Y. Lobsiger and J. Kolar, "Closed-loop di/dt & dv/dt control and dead time minimization of IGBTs in bridge leg configuration," in *Proceedings of the 14th IEEE workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2013, pp. 1–7. Cited on pages 51 and 130.

[56] T. Mannen and H. Fujita, "Dead time compensation method based on current ripple estimation," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, pp. 775–782. Cited on pages 50 and 51.

[57] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, 1988, pp. 122–129. Cited on page 51.

[58] S. Mariéthoz, U. Mäder, and M. Morari, "High-speed FPGA implementation of observers and explicit model predictive controllers," in *Proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2009. Cited on page 160.

[59] J. Mattingley and S. Boyd, "CVXGEN: a code generator for embedded convex optimization," *Optimization and Engineering*, vol. 13, no. 1, pp. 1–27, Mar 2012. Cited on page 160.

[60] S. E. Mattsson and G. Söderlind, "Index reduction in differential-algebraic equations using dummy derivatives," *SIAM Journal on Scientific Computing*, vol. 14, no. 3, pp. 677–692, 1993. Cited on page 20.

[61] C. W. T. McLyman, *Transformer and Inductor Design Handbook*, M. O. Thurston, Ed. Marcel Dekker, Inc., 2004. Cited on pages 87 and 289.

[62] P. H. Mellor, S. P. Leigh, and B. M. G. Cheetham, "Reduction of spectral distortion in class D amplifiers by an enhanced pulse width modulation sampling process," *IEE Proceedings–G Circuits, Devices and Systems*, vol. 138, no. 4, pp. 441–448, 1991. Cited on page 29.

[63] T. Meynard, "Design of series/parallel multicell converters for improved power conversion (tutorial 1)," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012. Cited on pages 87, 89, 90, and 104.

[64] R. D. Middlebrook and S. Ćuk, *Advances in switched-mode power conversion, Volumes I and II*. TESLAco, 1983, no. v. 1-2. Cited on pages 18, 52, and 56.

[65] R. Middlebrook and S. Ćuk, "A general unified approach to modelling switching-converter power stages," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, 1976, pp. 18–34. Cited on pages 16, 62, and 160.

[66] S. Mishra, R. Adda, and A. Joshi, "Inverse Watkins–Johnson topology-based inverter," *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1066–1070, 2012. Cited on pages 52 and 56.

[67] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: converters, applications, and design*. Wiley, 1995. Cited on pages 27, 30, 48, 71, 78, 139, 262, and 273.

[68] D. C. Moore, M. Odavic, and S. M. Cox, "Dead-time effects on the voltage spectrum of a PWM inverter," *IMA Journal of Applied Mathematics*, vol. 78, pp. 1–16, 2013. Cited on page 48.

[69] I. Mori, K. Kimura, Y. Yamada, H. Kobayashi, Y. Kobori, S. Wibowo, K. Shimizu, M. Kono, and H. San, "High-resolution DPWM generator for digitally controlled DC-DC converters," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems APCCAS 2008*, 2008, pp. 914–917. Cited on page 29.

[70] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, "Reliability of power cycling for IGBT power semiconductor modules," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 665–671, 2003. Cited on page 8.

[71] I. D. Mosely, P. H. Mellor, and C. M. Bingham, "Effect of dead time on harmonic distortion in class-D audio power amplifiers," *Electronics Letters*, vol. 35, no. 12, pp. 950–952, 1999. Cited on page 48.

[72] J. Mühlethaler, "Modeling and multi-objective optimization of inductive power components," Ph.D. dissertation, Swiss Federal Institute of technology (ETH) Zürich, 2012. Cited on page 86.

[73] D. Navarro, Ó. Lucía, L. A. Barragán, J. I. Artigas, I. Urriza, and Ó. Jiménez, "Synchronous FPGA-based high-resolution implementations of digital pulse-width modulators," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2515–2525, 2012. Cited on page 29.

[74] K. Nielsen, "Audio power amplifier techniques with energy efficient power conversion, volume I," Ph.D. dissertation, Technical University of Denmark (DTU), 1998. Cited on pages 27, 29, 48, 112, and 133.

[75] E. H. Nordholt, *Design of High-Performance Negative Feedback Amplifiers*. Delft Academic Press, 2007. Cited on pages 4 and 5.

[76] M. Norris, L. Platon, E. Alarcon, and D. Maksimovic, "Quantization noise shaping in digital PWM converters," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, 2008, pp. 127–133. Cited on page 29.

[77] W. J. Palm III, *Modeling, Analysis, and Control of Dynamic Systems*. Wiley, 1999. Cited on pages 177, 180, and 184.

[78] G. Pellegrino, R. I. Bojoi, P. Guglielmi, and F. Cupertino, "Accurate inverter error compensation and related self-commissioning scheme in sensorless induction motor drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1970–1978, 2010. Cited on page 50.

[79] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504–510, 2003. Cited on pages 52 and 56.

[80] D. Perreault, J. Kassakian, and H. Martin, "A soft-switched parallel inverter architecture with minimal output magnetics," in *Proceedings of the 25th Annual IEEE Power Electronics Specialist Conference (PESC)*, vol. 2, 1994, pp. 970 –977. Cited on page 51.

[81] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 301–308, 2003. Cited on page 245.

[82] A. Pratt and G. Drummond, "Full-bridge DC-DC converter with common mode chokes," in *Proceedings of the 20th annual IEEE Applied Power Electronics Conference and exposition (APEC)*, vol. 2, 2005, pp. 1227–1232. Cited on pages 86 and 91.

[83] S. Richter, S. Mariéthoz, and M. Morari, "High-speed online MPC based on a fast gradient method applied to power converter control," in *Proceedings of the American Control Conference (ACC)*, 2010, pp. 4737–4743. Cited on page 160.

[84] L. Risbo and T. Mørch, "Performance of an all-digital power amplification system," in *Presented at the 104th Audio Engineering Society Convention*. Audio Engineering Society, 1998. Cited on pages 32 and 38.

[85] M. Rose, J. Krupar, H. Guldner, and E. Brenner, "Effects of varying load conditions on adaptive gate control methods," in *Proc. 2011-14th European Conf. Power Electronics and Applications (EPE 2011)*, 2011, pp. 1–7. Cited on page 51.

[86] J. Rovers, J. Jansen, and E. Lomonova, "Multiphysical analysis of moving-magnet planar motor topologies," *IEEE Transactions on Magnetics*, vol. 49, no. 12, pp. 5730–5741, 2013. Cited on page 8.

[87] J. Salmon, A. M. Knight, and J. Ewanchuk, "Single-phase multilevel PWM inverter topologies using coupled inductors," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, pp. 1259–1266, may 2009. Cited on pages 86 and 91.

[88] S. R. Sanders, M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 251–259, 1991. Cited on page 20.

[89] M. Sandler, "Digital-to-analogue conversion using pulse width modulation," *Electronics & Communication Engineering Journal*, vol. 5, no. 6, pp. 339–348, 1993. Cited on pages 29 and 49.

[90] J. M. Schellekens, R. A. M. Bierbooms, and J. L. Duarte, "Dead-time compensation for PWM amplifiers using simple feed-forward techniques," in *Proceedings of the XIXth International Conference on Electrical Machines (ICEM)*, 2010, pp. 1–6. Cited on pages 45, 50, 51, and 244.

[91] J. M. Schellekens, M. L. A. Caris, J. L. Duarte, H. Huisman, M. A. M. Hendrix, and E. A. Lomonova, "High precision switched-mode amplifier with an auxiliary bias circuit," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10. Cited on pages 55, 85, and 243.

[92] J. M. Schellekens, J. L. Duarte, and M. A. M. Hendrix, "Interleaved switching of parallel ZVS hysteresis current controlled inverters," in *Proceedings of the 5th IEEE Young Researchers Symposium (YRS)*, 2010. Cited on page 244.

[93] J. M. Schellekens, J. L. Duarte, M. A. M. Hendrix, and H. Huisman, "Interleaved switching of parallel ZVS hysteresis current controlled inverters," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE Asia)*, 2010, pp. 2822–2829. Cited on page 244.

[94] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Elimination of zero-crossing distortion for high-precision amplifiers," in *Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2011, pp. 3370–3375. Cited on pages 55 and 243.

[95] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Fast-shared current transient response in high-precision interleaved inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3308–3317, 2011. Cited on pages 51, 90, and 243.

[96] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "High-precision current control through opposed current converters," in *Proceedings of the 14th European conference on Power Electronics and applications (EPE)*, 2011, pp. 1–10. Cited on pages 30, 159, and 243.

[97] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Harmonics in opposed current converters," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 439–445. Cited on pages 111, 137, and 243.

[98] J. M. Schellekens, J. L. Duarte, H. Huisman, and M. A. M. Hendrix, "Volume reduction of opposed current converters through coupling of inductors and interleaved switching," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2012, pp. 852–857. Cited on pages 85 and 243.

[99] R. F. Shea, *Amplifier handbook*. McGraw-Hill New York, 1966. Cited on page 5.

[100] S. Skogestad and I. Postlethwaite, *Multivariable Feedback Control - Analysis and design*. John Wiley & Sons, 1996. Cited on pages 177, 181, 183, and 194.

[101] V. Spinu and M. Lazar, "Integration of real-time and stability constraints via hybrid polytopic partitions," in *Proceedings of the IEEE International Conference on Control Applications (CCA)*, 2012, pp. 226–233. Cited on page 160.

[102] V. Spinu, J. M. Schellekens, M. Lazar, and M. A. M. Hendrix, "On real-time optimal control of high-precision switching amplifiers," in *Proceedings of the 17th International Conference on System Theory, Control and Computing (ICSTCC)*, 2013. Cited on pages 160, 201, and 243.

[103] V. Spinu, N. Athanasopoulos, M. Lazar, and G. Bitsoris, "Stabilization of bilinear power converters by affine state feedback under input and state constraints," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 8, pp. 520–524, 2012. Cited on page 160.

[104] V. Spinu, A. Oliveri, M. Lazar, and M. Storace, "FPGA implementation of optimal and approximate model predictive control for a buck-boost DC-DC converter," in *Proceedings of the IEEE International Conference on Control Applications (CCA)*, 2012, pp. 1417–1423. Cited on page 160.

[105] G. Stanley and K. M. Bradshaw, "Precision DC-to-AC power conversion by optimization of the output current waveform - the half bridge revisited," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 372–380, mar 1999. Cited on pages 60, 61, 86, 138, and 140.

[106] M. Steinbuch, "Dynamic modelling and robust control of a wind energy conversion system," Ph.D. dissertation, Technische Universiteit Delft, 1989. Cited on page 20.

[107] N. Sun, L. Zhang, Y. Xing, M. Xu, Y. Fang, and X. Ma, "A five level dual buck full bridge inverter with neutral point clamp for grid connected PV application," in *Proceedings of the 37th annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2011, pp. 1041–1045. Cited on page 61.

[108] P. Sun, C. Liu, J.-S. Lai, and C.-L. Chen, "Cascade dual buck inverter with phase-shift control," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2067–2077, april 2012. Cited on pages 60 and 61.

[109] K. J. Szwarc, A. Cichowski, J. Nieznanski, and P. Szczepankowski, "Modeling the effect of parasitic capacitances on the dead-time distortion in multilevel NPC inverters," in *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE)*, 2011, pp. 1869–1874. Cited on page 38.

[110] M. Takamatsu and S. Iwata, "Index reduction for differential–algebraic equations by substitution method," *Linear Algebra and its Applications*, vol. 429, no. 8, pp. 2268–2277, 2008. Cited on page 20.

[111] M. T. Tan, J. S. Chang, H. C. Chua, and B. H. Gwee, "An investigation into the parameters affecting total harmonic distortion in low-voltage low-power class-D amplifiers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 10, pp. 1304–1315, 2003. Cited on page 27.

[112] C. A. Teixeira, B. P. McGrath, and D. G. Holmes, "Topologically reduced multilevel converters using complementary unidirectional phase-legs," in *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE)*, 2012, pp. 2007–2012. Cited on page 61.

[113] C. A. Teixeira, B. P. McGrath, and D. G. Holmes, "Closed-loop current control of multilevel converters formed by parallel complementary unidirectional phase-legs," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013, pp. 978–985. Cited on page 61.

[114] Class-D LC filter design. Application note SLOA119A. Texas Instruments Incorporated. http://www.ti.com/lit/an/sloa119a/sloa119a.pdf. Cited on page 267.

[115] (2009) Tms320x2802x, 2803x piccolo high resolution pulse width modulator (HRPWM). Reference guide SPRUGE8E. Texas Instruments Incorporated. http://www.ti.com/lit/ug/spruge8e/spruge8e.pdf. Cited on page 29.

[116] L. M. Tolbert, F. Z. Peng, F. H. Khan, and S. Li, "Switching cells and their implications for power electronic circuits," in *Proceedings of the 6th IEEE International Power Electronics and Motion Control Conference (IPEMC)*, 2009, pp. 773–779. Cited on pages 57 and 86.

[117] G. Tong and J. S. Chang, "Modeling and technique to improve PSRR and PS-IMD in analog PWM class-D amplifiers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, no. 6, pp. 512–516, 2008. Cited on page 37.

[118] N. Urasaki, T. Senjyu, T. Kinjo, T. Funabashi, and H. Sekine, "Dead-time compensation strategy for permanent magnet synchronous motor drive taking zero-current clamp and parasitic capacitance effects into account," *IEE Proceedings – Electric Power Applications*, vol. 152, no. 4, pp. 845–853, july 2005. Cited on pages 48, 50, and 51.

[119] N. Urasaki, T. Senjyu, K. Uezato, and T. Funabashi, "Adaptive dead-time compensation strategy for permanent magnet synchronous motor drive," *IEEE Transactions on Energy Conversion*, vol. 22, no. 2, pp. 271–280, june 2007. Cited on pages 48 and 50.

[120] R. J. Vaccaro, *Digital Control: A state-space approach*. Mcgraw-Hill College, 1995. Cited on pages 24, 161, 192, 193, 195, 196, and 199.

[121] J. van Duivenbode and B. Smet, "An empiric approach to establishing MOSFET failure rate induced by single-event burnout," in *Proceedings of the 13th Power Electronics and Motion Control Conference (EPE-PEMC)*, 2008, pp. 102–107. Cited on page 8.

[122] C. Van Loan, "Computing integrals involving the matrix exponential," *IEEE Transactions on Automatic Control*, vol. 23, no. 3, pp. 395–404, 1978. Cited on page 24.

[123] B. J. D. Vermulst and E. A. Lomonova, "Design, simulation and evaluation of GLIM-type self-oscillating audio amplifier," in *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9. Cited on page 87.

[124] B. Vermulst, C. Wijnands, and J. Duarte, "Isolated high-efficiency DC/DC converter for photovoltaic applications," in *Proceedings of the 38th Annual Conference of the IEEE Industrial Electronics Society*, 2012, pp. 506–511. Cited on page 7.

[125] C.-M. Wang, "A novel single-stage full-bridge buck-boost inverter," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 150–159, 2004. Cited on pages 52 and 56.

[126] M. Wang, X. Jiang, J. Song, and T. Brooks, "A 120 dB dynamic range 400 mW class-D speaker driver with fourth-order PWM modulator," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1427–1435, 2010. Cited on page 27.

[127] G. Wanner and E. Hairer, *Solving Ordinary Differential Equations II - second revised edition*. Springer-Verlag, Berlin, 2010, vol. 1. Cited on page 20.

[128] B. Widrow, I. Kollar, and M.-C. Liu, "Statistical theory of quantization," *IEEE Transactions on Instrumentation and Measurement*, vol. 45, no. 2, pp. 353–361, 1996. Cited on page 245.

[129] C. M. Wu, W.-H. Lau, and H. Shu-Hung Chung, "Analytical technique for calculating the output harmonics of an H-bridge inverter with dead time," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 46, no. 5, pp. 617–627, 1999. Cited on page 48.

[130] Y. Xinmei, I. Brown, R. D. Lorenz, and Q. Arui, "Observer-based inverter disturbance compensation," in *Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE)*, 2009, pp. 2520–2527. Cited on page 50.

[131] Z. Yao and G. Hu, "Comparison of dual-buck full-bridge inverter with different inductor structures," in *Power and Energy Engineering Conference (APPEEC), 2011 Asia-Pacific*, 2011, pp. 1–3. Cited on page 86.

[132] Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full-bridge inverter with hysteresis current control," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3153–3160, aug. 2009. Cited on page 61.

[133] L. Yong-Kai and L. Yen-Shin, "Dead-time elimination of PWM-controlled inverter/converter without separate power sources for current polarity detection circuit," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2121–2127, june 2009. Cited on pages 50 and 51.

[134] V. Yousefzadeh and D. Maksimovic, "Sensorless optimization of dead times in DC-DC converters with synchronous rectifiers," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 994–1002, 2006. Cited on page 51.

[135] G. B. Yundt, "Series- or parallel-connected composite amplifiers," *IEEE Transactions on Power Electronics*, vol. PE-1, no. 1, pp. 48 –54, jan. 1986. Cited on page 251.

[136] N. R. Zargari, P. D. Ziogas, and G. Joos, "A two switch high performance current regulated DC/AC converter module," in *Conference record of the IEEE Industry Applications Society (IAS) annual meeting*, 1990, pp. 929–934. Cited on pages 61 and 238.

[137] N. R. Zargari, P. D. Ziogas, and G. Joos, "A two-switch high-performance current regulated DC/AC converter module," *IEEE Transactions on Industry Applications*, vol. 31, no. 3, pp. 583–589, 1995. Cited on pages 52 and 61.

[138] X. Zhang and C. Gong, "Dual-buck half-bridge voltage balancer," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 3157–3164, 2013. Cited on page 61.

[139] C. Zhu, F. Zhang, and Y. Yan, "A novel split phase dual buck half bridge inverter," in *Proceedings of the 20th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 2, 2005, pp. 845–849. Cited on page 61.

[140] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda, "Tight magnetic coupling in multiphase interleaved converters based on simple transformers," in *Proceedings of the 20th annual IEEE Applied Power Electronics Conference and exposition (APEC)*, vol. 1, 2005, pp. 385–391. Cited on page 91.

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