Wake-up receiver based ultra-low-power WBAN

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Maarten Lont

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CONTENTS

LIST OF SYMBOLS

$a_{f,n}$	n^{th} order Fourier cosine coefficient of function $f(t)$	75
α_n	Phase of the receiver generated noise vector	49
a_n	Bit n from the bipolar bit sequence	42
α_r	Phase of the received FSK signal corrupted by the LO phase noise	49
BAW	Bulk Acoustic Wave filter	39
$b_{f,n}$	n^{th} order Fourier sine coefficient of function $f(t)$	75
$c_{f,n}$	n^{th} order complex Fourier series coefficient	77
C_{LO}	Phase noise thermal noise parameter	45
$\Delta\omega$	FSK frequency deviation	42
ΔP_x	Power consumption increase in mode x compared to sleep mode $P_x - P_{sleep}$	16
$\Delta T[n]$	Cycle-to-cycle jitter of the nth period	46
ε	I/Q phase error	43
F	Noise factor	43
f_{osc}	Oscillator oscillation frequency	87
g	I/Q gain error	43

G_{BB}	Gain in the baseband stage	49
G_{RF}	RF gain	44
G_t	Mixer transducer power gain	80
G_v	Mixer voltage conversion gain	75
h	FSK modulation index $h = \frac{\Delta\omega}{\pi R_b}$	42
$H_{I\&D}(\omega)$	Integrate-and-Dump filter	41
$H_{IF}(\omega)$	Intermediate frequency filter	40
k	Packet length	16
k_B	Boltzmann's constant $1.38065 \times 10^{-23}\, m^2\, kg\, s^{-2}\, K^{-1}$	42
K_{LO}	Phase noise 1/f noise parameter	45
$\mathscr{L}(f)$	Phase noise at f Hz offset given in dBc/Hz	45
l	Address length	12
λ	Average packet rate	11
$\boldsymbol{M}_{rx}(t)$	Receiver matrix	44
μ	Electron mobility	125
μ_{ACK}	Expected number of acknowledgments	154
μ_{ACKx}	Expected number of acknowledgment retransmissions	18
$\mu_{bcn/pkt}$	Expected number of synchronization beacons per received packet	24
μ_{FACKx}	Expected number of retransmitted false acknowledgments	18
μ_{slot}	Expected number of TDMA slots per received packet	18
μ_{WUC}	Expected number of wake-up calls	18
n_{bb}	Baseband input related noise	43
$n_i(t)$	Receiver input noise	42
N_{node}	Number of nodes in the network	11
n_{rf}	RF input related noise	43
N^+_{WUC}	Maximal number of wake-up call transmissions	18
ω_o	Carrier frequency	42

ω_{off}	FSK frequency offset	95
P_{1dBc}	Input referred 1dB compression point	112
$p_{ACK\geq 1}$	Probability of initial acknowledgment transmission	18
$P_{BB}(\tau)$	Baseband generated noise power at the output of the FSK demodulator	58
$P_{click}(\tau)$	Click noise power at the output of the FSK demodulator	54
$p_{FACK\geq 1}$	Probability of at least one false acknowledgment transmission	18
$p_{FACK,\,n}$	Probability that n false acknowledgment packets are send	155
p_{false}	False wake-up probability	18
$\varphi(t)$	Instantaneous phase of FSK modulated signal	42
$\varphi(t)$	FSK signal phase	42
P_{IIP3}	Input referred third order interception point	112
P_{LO}	Local oscillator power used to drive the mixer	71
p_{miss}	Packet miss probability	18
P_R	Power consumption in receive mode	16
$P_{RF}(\tau)$	RF generated noise power at the output of the FSK demodulator	57
P_{Rset}	Power consumption when settling to receive mode	16
$P_s(\tau)$	Signal power at the output of the FSK demodulator	58
P_{sleep}	Power consumption in sleep mode	16
$P_{standby}$	Power consumption in standby mode	16
P_T	Power consumption in transmit mode	16
$P_{\dot{\theta}}(\tau)$	Phase noise power at the output of the FSK demodulator	58
P_{Tset}	Power consumption when settling to standby mode	16
P_{wake}	Power consumption when switching between sleep and standby mode	16
r	Radius of gyration	55

$R_{\dot{\alpha}_n}(\tau)$	Autocorrelation of the total demodulator output noise	51
$R_{\alpha_{nbb}}(\tau)$	Autocorrelation of the baseband noise phase component at the output of the receiver front-end	52
$R_{\alpha_{nrf}}(\tau)$	Autocorrelation of the RF noise phase component at the output of the receiver	51
R_b	Bit rate	16
R_{bw}	Wake-up receiver bit rate	20
$R_f(\tau)$	Autocorrelation of the transfer function from the baseband noise source to the signal phase at the receiver output	52
$R_g(\tau)$	Autocorrelation of the transfer function from the RF noise source to the signal phase at the receiver output	52
ρ	Carrier to noise ratio	42
R'_L	Normalized load impedance	73
$R_{nbb}(\tau)$	Autocorrelation of the baseband noise source	52
$R_{nrf}(\tau)$	Autocorrelation of the RF noise source	51
r_{sw}	Switch on-resistance	70
$r(t)$	Received signal	40
$\boldsymbol{s}$	Signal vector at the output of the receiver front-end	49
SAW	Surface Acoustic Wave filter	39
σ_{abs}	Absolute time jitter standard deviation	46
σ_{bb}	Standard deviation of the baseband generated noise	43
σ_i	Standard variation of the receiver input noise	42
σ_{pn}	Standard deviation of the receiver generated phase noise	44
σ_{rf}	Standard deviation of the RF generated noise	43
$\boldsymbol{s_n}$	Receiver generated noise vector	49
$S_{nbb}(\omega)$	Power spectral density of the baseband noise at the FSK demodulator output	53
$S_{nrf}(\omega)$	Power spectral density of the RF noise at the FSK demodulator output	53
$\boldsymbol{s_r}$	FSK signal vector corrupted by LO phase noise	49

$S_y(\omega)$	Power spectral density of the FSK demodulator output	52
T	Address decoding threshold	13
$T_{abs}[n]$	Absolute jitter measure over n periods	46
T_b	Bit period $\left(\frac{1}{R_b}\right)$	42
T_{beacon}	Maximal time between two TDMA synchronization beacons	23
$\theta(t)$	Local oscillator phase noise	43
T_{lat}	Maximally allowed link-setup latency	10
T_{mavg}	Integration time constant of the moving-average filter	128
τ_{off}	Mixer time constant when the switch is turned off	73
$T_{off,n}$	Mixer switch turn-off time of phase n	72
τ'_{off}	Mixer normalized off-state RC time constant	73
τ_{on}	Mixer time constant when the switch is turned on	73
$T_{on,n}$	Mixer switch turn-on time of phase n	72
τ'_{on}	Mixer normalized on-state RC time constant	73
T_s	Sample time	97
T_{set}	Receiver or transmitter settling period	16
T_{skew}	Maximal allowed clock skew between a TDMA master and sensor node	23
T_{wake}	Transition time between sleep and standby mode	16
V_T	Thermal voltage $\left(\frac{kT}{q}\right)$	125
$y(t)$	FSK demodulator output signal	49
Z_{in}	Mixer input impedance at the carrier frequency	77

LIST OF ABBREVIATIONS

ACK	Acknowledgment	18
AFC	Automatic Frequency Control	94
ARE	Average relative error	63
BAN	Body Area Network	9
BAW	Bulk Acoustic Wave	36
BER	Bit Error Rate	15
CNR	Carrier to noise ratio	42
CW	Continuous-Wave interferer	138
DCDM	Digital Cross-Differentiate Multiply FSK demodulator	93
DCO	Digitally Controlled Oscillator	119
DNL	Differential Non-Linearity	119
EVM	Error Vector Magnitude	39
FACK	False Acknowledgment	18
FOM	Figure of Merit	114
FSK	Frequency Shift Keying	35
FSPL	Free Space Path Loss	64
IC	Inversion Coefficient	122

IIP3	Input referred third order interception point	111
LO	Local Oscillator	44
MAC	Media Access Control	9
OOK	On-Off Keying	35
pdf	Probability Density Function	54
PLL	Phase Locked Loop	36
PSD	Power spectral density	45
PVT	Process, Voltage and Temperature variation.	98
RSSI	Received Signal Strength Indicator	98
SIR	Signal-to-Interferer-ratio	138
TDMA	Time Division Multiple Access	11
VGA	Variable Gain Amplifier	122
WBAN	Wireless Body Area Network	9
WUC	Wake-up call used to wake-up the sensor nodes	11
WURx	Wake-up Receiver	11

CHAPTER 1

INTRODUCTION

WIRELESS Body Area Networks (WBAN) are small-scale, in both area and node count, networks centered on a human body. The low-power wireless nodes can contain many different sensors, for example: ECG, EEG, blood-pressure and temperature sensors. This is graphically depicted in figure 1.1. While the required bit rate of the different sensors varies from a few kilobits per second up to a few hundred kilobits per second, most applications require a bit rate around 100kbps, see [1] and [2]. Additionally, the average packet rate of a sensor node is very low. Some nodes like temperature sensors may only transmit the measured data a couple of times a day, hence they are in sleep mode for more than 90% of the time. Other sensor types like EEG and ECG might have high peak bit rates when they are active. However they are not activated most of the time. Additionally the required link to link setup latency requirement is relaxed, which favors asynchronous networks.

The sensor nodes are battery powered and have to operate for a long period of time, while it is often impossible or impractical to recharge or replace the batteries on a regular basis. Therefore, the sensor nodes need to have very low power consumption. Furthermore, since the network is centered around the human body, it is a small scale network by definition. The maximal distance between two nodes is approximately 10m. Combining the small network scale with the low power requirement, a single-hop star network topology is a good fit. In such a network there is one master node, for example a smart phone, with a bigger power supply and higher processing capabilities. Thus the body area sensor

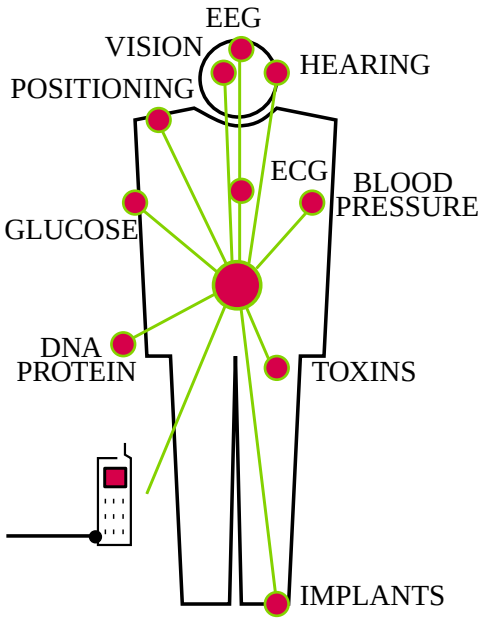


Figure 1.1: *Example of a Wireless Body Area Network in which different sensor nodes around the body cooperate in a small-scale network.*

network is highly asymmetric. The asymmetric nature of the network can be used to reduce the power consumption of the sensor nodes by mapping power intensive tasks on the high power master node or by choosing a synchronization scheme to make maximal use of the asymmetric power supply. Additionally, the sensitivity of the sensor node can be decreased by increasing the transmit power of the master node.

1.1 Wake-up Receiver

To reduce the sensor node power consumption to a level where the node can operate for months on a small battery the node needs to sleep as long and often as possible. A low-power Wake-up Receiver (WURx) is added to the sensor node which wakes up the node when it receives a Wake-up Call (WUC) transmitted by the master node. Figure 1.2 gives the overview of a general wireless sensor node. Depending on the application the main transceiver might be omitted. A remote control application might only need a WURx for example.

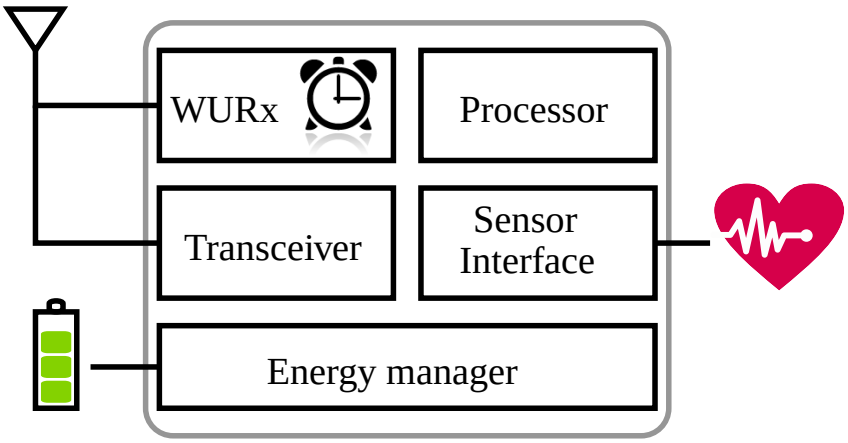


Figure 1.2: *A general wireless sensor node overview.*

The WURx should be capable of receiving and decoding a wake-up call containing an address and possibly a few bits of settings and information. An address should be sent since we do not want to wake-up all the nodes in the network, as this would lead to a waste of power. In fact, the WURx is used to synchronize the master and sensor nodes only during the transmission of a packet. In between packet transmissions the network is not synchronized in order to save power.

This thesis focuses on the design and implementation of the wake-up receiver, both on the system level and circuit level.

1.2 Wake-up Receiver Challenges

Figure 1.3 shows a schematic overview of the required bit rates and corresponding power consumption of current wireless standards. The depicted bit rate is the bit rate over the air. From the application point of view the actual bit rate may be lower because of channel coding, and synchronization overhead such as packet headers. It has to be noted that besides the bit rate and power consumption also sensitivity and linearity are important parameters. There is a clear trade-off between bit rate and power consumption. The figure also shows the three IMEC application scenarios, depicted by the blue clouds. Within this thesis we target the low-power WURx application scenarios and low-bit-rate narrow-band (NB) applications. As can be seen the targeted power consumption is much lower than state-of-the-art low-power standards like Zigbee, while still fulfilling the WBAN specific receiver requirements. The stars show the measurement results of the

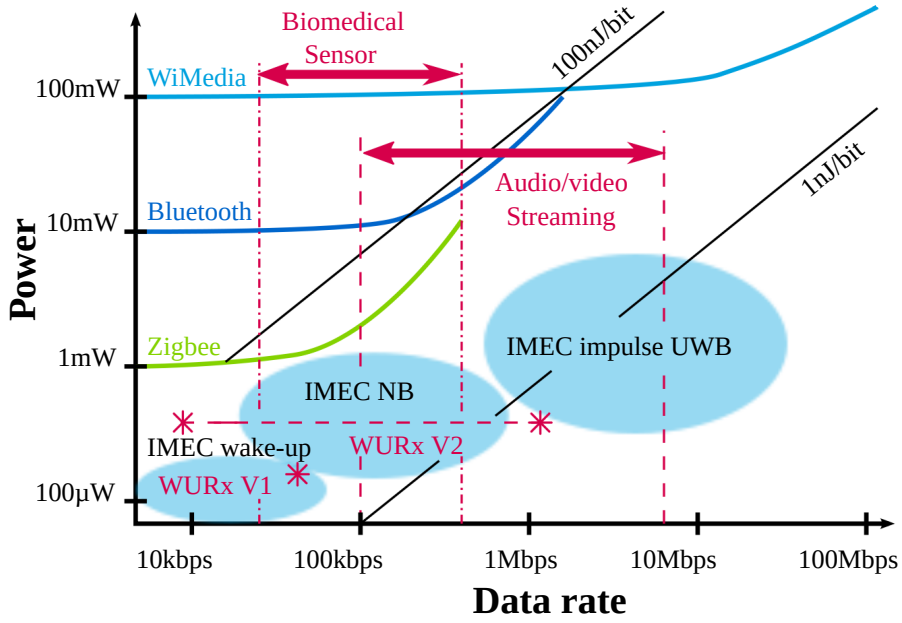


Figure 1.3: *Schematic overview of wireless standards and the low-power IMEC application areas.*

first (WURxV1) and second (WURxV2.1) wake-up receiver presented in chapters 5 and 6 in this thesis. The first version of the wake-up receiver front-end has a fixed bit rate of 50kbps with a power consumption of 126µW. While the second version has a constant power consumption of 329.6µW with a variable bit rate between 6.25kbps and 1250kbps. Therefore, the second WURx is denoted by a region confined by two stars. For more information on the first and second version of the wake-up receiver front-end see chapters 5 and 6, respectively.

A small scale Wireless Body Area Network (WBAN) is targeted. Since the WBAN is inherently small-scale, the maximal transmission distance is 10m. To reduce the power in the sensor nodes an asymmetric star-topology network is chosen. Moreover, there is a clear trade-off between power consumption and linearity. To reduce the power consumption the linearity is sacrificed. To avoid in-band interferer collision the master node manages the network, making sure that only one node is active. Additionally, the master node can avoid collisions with other networks by means of carrier sensing. The WURx itself should be able to cope with out-of-band interference. For a more in-depth discussion on the WURx specifications and requirements see section 3.6.

1.3 Aims of the Thesis

As shown in the introduction wireless sensor nodes targeted towards WBAN applications can profit from a low-power wake-up receiver. However, the power consumption of the WURx should be lower than standard compliant receivers. The aim of this thesis is to study the feasibility of low-power wake-up receivers, with special attention on power reduction techniques. To attain the desired power consumption, the network, system and circuit levels are taken into account. The following aspects are addressed:

- Typical WBAN requirements (chapter 2)
- Effects of media access control (MAC) layer synchronization on the power consumption (chapter 2)
- The interaction between wideband FSK modulation and receiver front-end design (chapter 3)
- Power consumption reduction, by removing the low-noise-amplifier from the receiver front-end and using a mixer-first architecture (chapter 4)
- Low-power synchronization by replacing power-consuming phase-locked-loops by a low-power automatic frequency control loop (chapter 4)
- Implementation and evaluation of the proposed power reduction techniques (chapters 5 and 6)

1.4 Scope of the Thesis

Within this thesis the implications of MAC layer synchronization on the power consumption will be studied, but the implementation of MAC protocols is beyond the scope of this thesis. Furthermore, there exists a large variety of wireless sensor networks with widely different requirements and characteristics. Each different network type demands different design trade-offs in order to come to an optimal low-power receiver front-end. Therefore, the thesis will only focus on small scale wireless networks, like wireless body area networks, and the design of low-power receiver front-ends used in the low-power sensor nodes in these networks. Moreover, this thesis focuses on the optimal circuit design of low-power Frequency Shift Keying (FSK) modulation based wake-up receivers. On-Off Keying (OOK) modulation will be mentioned but not analyzed in further detail since it is less robust against interferers. Circuits will only be implemented

in silicon with the aim of validating proposed power reduction strategies. This thesis does not have as a goal to demonstrate a fully-integrated transceiver system. The circuits will only be implemented in CMOS technology since it is the most widely used technology and the technology of choice for highly integrated mixed-signal systems.

1.5 Original Contributions

The original contributions of this thesis are:

- Closed-form energy consumption models of network synchronization.
- Modeling and analysis of the interaction between wideband-FSK modulation and receiver impairments.
- Mixer-first architecture geared towards low-power receiver front-ends and time-domain based modeling of the key performance parameters transducer power gain and noise figure.
- Optimal design strategy for mixer-first front-ends targeted towards low power consumption.
- Analysis of power consumption and phase noise performance differences between LC and ring oscillators taking technology scaling and limitations into account.
- Implementation and evaluation of mixer-first receiver front-ends.
- Design and implementation of an automatic frequency control loop using the in-place FSK demodulator as an alternative for power-hungry phase locked loops.
- Graphical comparison between different receiver front-ends as an extension to Figure of Merit (FOM) based comparison.

1.6 Thesis Outline

The thesis outline is depicted in figure 1.4.

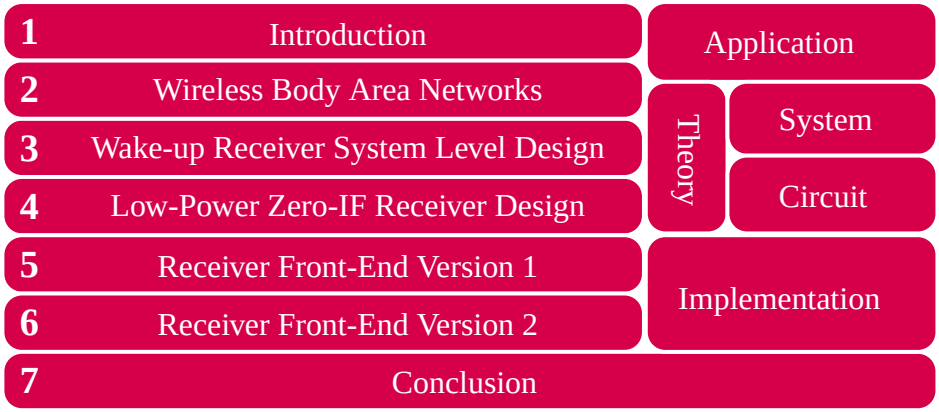


Figure 1.4: *Thesis outline.*

Chapter 1 introduces Wireless Body Area Networks and the Wake-up Receiver concept. Furthermore, the trends in both industrial and academic research are summarized and remaining research challenges are identified.

In chapter 2 several network and applications aspects of body area networks are studied. Since low energy consumption is essential, the impact of network synchronization on the energy consumption is studied at the Media Access Control (MAC) level. Additionally, common application related requirements are extracted from literature. By combining the application related WURx requirements and the MAC layer study the WURx solution space is derived.

Chapter 3 delves into the system-level aspects of the WURx design, starting with a literature study of state-of-the-art low-power receivers with special attention on the chosen modulation schemes. A Zero-IF receiver architecture is chosen, because of the low power consumption target. Additionally, wideband-FSK modulation is proposed to overcome the inherent zero-IF design challenges like DC offset, self-mixing and 1/f noise, and the effects of receiver impairments on the Bit Error Rate (BER) are analyzed. The chapter concludes with WURx circuit level design specifications.

Chapter 4 focuses on circuit level design and modeling with special attention on power consumption reduction. The power consumption is reduced at circuit level by omitting the Low Noise Amplifier (LNA) from the receiver front-end, leading to a mixer-first architecture. The input impedance, transducer power

gain and noise figure of a passive mixer are modeled and used in the presented optimal design methodology for mixer-first receivers. Additionally, the power-consuming local oscillator is studied, and the LC and ring oscillator topologies are compared. Also an Automatic Frequency Control (AFC) loop which makes use of the FSK demodulator is presented as a power-efficient alternative for a power hungry PLL.

The feasibility of the mixer-first architecture is studied in chapter 5, by implementing and measuring a low-power receiver front-end. Furthermore, a graphical method for comparing different receiver front-ends given application requirements is presented.

In chapter 6 a second version of the mixer-first receiver front-end with decreased noise figure is presented. The AFC loop introduced in chapter 4 is implemented in an FPGA and tested in combination with the receiver front-end.

At the end of the thesis conclusions are drawn in chapter 7.

CHAPTER 2

WIRELESS BODY AREA NETWORKS

THERE has been a lot of research into Wireless Body Area Networks (WBAN) ; see for example the surveys presented in by [3] and [4]. In a WBAN, sensors are placed on or near the body. Each node needs to be very small; hence it can only have a small battery. Additionally, it is impractical or even impossible to replace the batteries on a regular basis. Alternatively, the node can make use of energy harvesting. In both cases the power consumption needs to be very low. This is one of the biggest challenges in the design of WBAN nodes and can only be achieved by making use of the special properties of WBANs.

In this chapter different sensor network aspects and reported WBAN applications are analyzed and summarized. Additionally, several Media Access Control (MAC) protocols are compared using the WBAN properties. Since low power consumption is of primary importance, the sensor node energy consumption of the different MAC-layers are compared. With the energy consumption models, the solution space is examined. At the end of the chapter the receiver requirements are obtained.

2.1 Wireless Sensor Network Properties

The power consumption of wireless sensor nodes can be greatly reduced by optimizing the nodes with respect to network symmetry, synchronization, scale and packet rate.

Firstly, the network symmetry has a big impact on the system design. In a symmetric network the wireless sensor nodes have similar power supply and processing power. On the other hand, in an asymmetric network there can be large differences between nodes. In other words, the network is heterogeneous. Body area networks (BAN) usually are asymmetric [3]. In such a network at least one node has a bigger power supply and more processing power, and can take over energy-consuming tasks from the low-power simple sensor nodes.

Additionally, the network size is an important network property. Unlike environmental sensor networks, a WBAN is inherently small-scale. The maximal distance between two nodes is less than 10m, and each network has less than 100 nodes [1]. In such a small network, it is more power efficient to use single-hop communication instead of multi-hop.

Since the network is small-scale, asymmetric and single-hop, a star topology is suitable, which is used by most WBANs [3, 5]. In a star topology there is only one master node which manages the network, as is depicted in figure 1.1. Since the master has a bigger power supply it can transmit with higher power and acts as a gateway to the outside world. The rest of the network consists of low-power, simple sensor nodes. Additionally, the master can be used for in-band interference avoidance. Firstly the master node manages the network and makes sure that only one sensor node is active at any given moment. Secondly, the master can implement carrier sensing to reduce collisions with other networks operating in the same band.

Finally, the packet rate λ and maximal allowed link setup latency T_{lat} are important in WBAN design. When the packet rate is low and the allowed network latency is high, the nodes can sleep for very long periods to save power. In such a network the network does not have to stay synchronized the entire time, because there is enough time to synchronize before each transmission. Since the network does not need to be kept synchronized in the long pauses between two consecutive packages, the synchronization overhead is reduced. On the other hand, when the latency needs to be very low or when the packet rate is very high, there is no time to synchronize the network before every transmission. A more in-depth analysis of network synchronization, with special attention for the Media Access Control (MAC) layer, is given in the next section.

2.2 MAC Layer Energy Consumption Model

Before data can be transferred between two nodes, they need to be synchronized. This can be achieved in either of two ways: synchronize the network just before the data transfer takes place, or keep the network synchronized continuously. The first case is an asynchronous or contention-based network; the sensor nodes ask for permission to start transmitting or the master node polls the sensor nodes for data when needed. The latter type is a synchronized, or schedule-based network, i.e. each node knows when it can transfer the data, for example in a Time Division Multiple Access (TDMA) protocol.

The MAC-layer protocol, and therefore synchronization type, has a big influence on the power consumption. Depending on the type of synchronization, power is wasted because of:

- idle listening
- overhearing
- synchronization overhead

In an asynchronous network the idle listening and overhearing penalties can have a big influence on the power consumption. Since each node does not know when it needs to listen for incoming data it needs to listen regularly even when there is no data present. Additionally, a node also does not know when other nodes do get a transmission slot. Therefore, the sensor nodes can overhear packets meant for another node and react on it. Examples of asynchronous MAC protocols targeted towards sensor networks are B-MAC [6] and X-MAC [7].

The idle listening can be reduced by adding a very-low-power receiver to the wireless sensor node. The receiver only listens for wake-up calls (WUC) from the master node and wakes-up the rest of the sensor when needed. Additionally, this wake-up receiver (WURx) can reduce the overhearing penalty when an address is added to the WUC. It is only beneficial to add a WURx, when its power consumption is less than the idle listening and overhearing penalties.

On the other hand, in a synchronous network, the master needs to assign slots to nodes and the nodes need to listen for synchronization beacons. This synchronization overhead consumes power. Furthermore, when the synchronization between a sensor node and the network master is lost, the node needs to listen continuously for the next synchronization beacon.

Within this section the power consumption of each type of network synchronization is modeled. The energy consumption of the node is calculated per received packet, taking into account the maximally allowed link-setup latency T_{lat}, the

number of nodes N_{node} and the average packet rate λ. The energy needed to transmit the data is not taken into account since it is equal for both synchronization schemes.

Firstly, address coding and required address length are discussed. Next, the traffic statistics and generic radio model are presented. The radio and traffic model are used to obtain the energy consumption models for the different network types. These models are eventually used in the following sections to explore the design space and determine in what cases which network type is optimal.

2.2.1 Address Coding

Each node has a unique address to reduce the overhearing penalty. The node correlates the received address with its own address, and compares the result to a threshold. If the correlation is higher than the threshold, the node is woken up.

Although maximum likelihood decoding leads to more reliable results than correlation decoding, it is also much more complex and power consuming. Therefore, correlation decoding is chosen. Correlation coding is very similar to minimum distance or Hamming codes.

A correlation decoding function can be implemented power efficiently by NXOR operations,

$$C = \sum_{n=1}^{l} a_n \text{ NXOR } r_n \,,$$

where l is the address length, r_n the received address bit and a_n the address bit of the node. The output of the correlation function is the number of correct bits, and the maximal value is l. The minimum number of bits that differ between two addresses is called the Hamming distance, and is denoted by M. A code can correct $\lfloor \frac{1}{2}(M-2) \rfloor$ errors and detect $(M-1)$ errors. It is better to choose an odd Hamming distance M, since it can correct as many bits as a longer code with distance $M+1$. The correlator threshold T has to be in the range: $l-M \leq T < l$ to make sure the node wakes up only if its own address is received. In practice, noise will induce bit errors which can lead to a missed wake-up call or a false wake-up, with probabilities p_{miss} and p_{false} respectively.

Number of Nodes

The maximum number of addresses, and therefore sensor nodes, depends on the address length l and the minimal number of different bits between two addresses

M. It is impossible to give an exact number of possible addresses, this problem is known as the sphere packing problem; the number of available addresses is equal to the number of spheres with diameter M that can be packed in a l dimensional space where each dimension has only two states: "0" or "1".

However, an upper bound can be given: the number of addresses with Hamming distance M (N_{nodes}) is less than the total number of nodes divided by the number of nodes in a sphere with radius $\lfloor \frac{M-1}{2} \rfloor$. The radius is rounded half down, since the number of bits is integer and the radius of two neighboring addresses should be less or equal to the Hamming distance between the addresses. The radius is the Hamming distance divided by two, since the distance between the centers of two equally sized and neighboring spheres is the sum of their radii.

The total number of possible unique nodes without taking into account the Hamming distance is

$$N_{nodes,max} = 2^l, \tag{2.1}$$

and the number of addresses in a sphere with radius $\lfloor \frac{M-1}{2} \rfloor$ is

$$N_{nodes,sphere} = \sum_{n=0}^{\lfloor \frac{M-1}{2} \rfloor} \binom{l}{n}.$$

Combining the total number of nodes and the nodes per sphere, an upper bound on the number of nodes with Hamming distance M is

$$N_{nodes} \leq \frac{2^l}{\sum_{n=0}^{\lfloor \frac{M-1}{2} \rfloor} \binom{l}{n}}. \tag{2.2}$$

Coding Performance

A WUC is missed when the correct address was sent but the output X of the correlator is smaller than the threshold T. Noting that the bit errors have a binomial distribution with success probability p and number of trials n, and the probability of a single bit error is given by p_e, the miss probability is

$$p_{miss} = P(X \leq T \,|\, p = 1 - p_e, n = l). \tag{2.3}$$

Additionally, the probability a WUC is missed after N^+_{WUC} attempts is

$$p_{wuc,miss} = p_{miss}^{N^+_{WUC}}.$$

It is more difficult to calculate the false wake-up probability than the packet miss probability. The probability of a false wake-up is highest when a 'neighboring' address with Hamming distance M is received; this case is taken as a conservative false wake-up estimation. Since the distance is equal to M the received and actual addresses share $l-M$ bits. It is assumed that the false wake-up probability when a non-neighboring address is send is negligible.

The false wake-up event can be divided in two independent events: a false wake-up with all the shared bits correctly received, and one with the shared bits containing bit errors. The false wake-up probability is the sum of the probabilities of these two events. Assuming none of the shared bits change and only the unique bits change, the node is woken up when bit errors change $T-(l-M)$ unique bits and p_{false} is

$$p_{false}\big|_{\text{No shared bits change}} = P(X > T-(l-M)|p=p_e, n=M)\times P(Y=0|p=p_e, n=l-M)\,, \tag{2.4}$$

where X specifies the number of unique bits that change and Y specifies the number of shared bits that change, see figure 2.1. When c shared bits change also c extra unique bits have to change. The probability on this event is

$$p_{false}\big|_{\text{c shared bits change}} = P(X > T+c-(l-M)|p=p_e, n=M)\times P(Y=c|p=p_e, n=l-M)\,. \tag{2.5}$$

The maximal number of changed shared bits is by definition smaller than the number of shared bits

$$c < l-M\,.$$

Additionally, for a false wake-up to occur,

$$c+T < l\,,$$

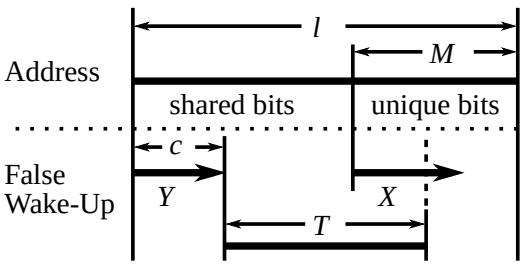


Figure 2.1: *Address coding and the false wake-up event*

should hold, see figure 2.1. Combining these bounds, c is bound by

$$c < \min\{l-M, l-T\}\,.$$

No longer assuming that only the shared bits can change, p_{false} becomes

$$p_{false} = \sum_{c=0}^{\min(l-M,l-T)} P(X > T+c-(l-M)|p=p_e, n=M)\times P(Y=c|p=p_e, n=l-M)\,. \tag{2.6}$$

When the bit error probability is less than 1% and the address length is large enough, e.g. larger than 10, p_{false} can be approximated

$$p_{false} \approx P(X > T-(l-M)|p=p_e, n=M)P(Y=0|p=p_e, n=l-M)\,.$$

The approximation error is less than 0.4% when $l=10$ and $p_e = 1\%$.

It is clear that the probabilities p_{miss} and p_{false} depend on the address length and the bit error rate (BER). Depending on the application the threshold T can be changed to sacrifice p_{miss} for p_{false} or vice versa. Here we assume that both probabilities need to be low, thus the threshold T is chosen in a way to equate

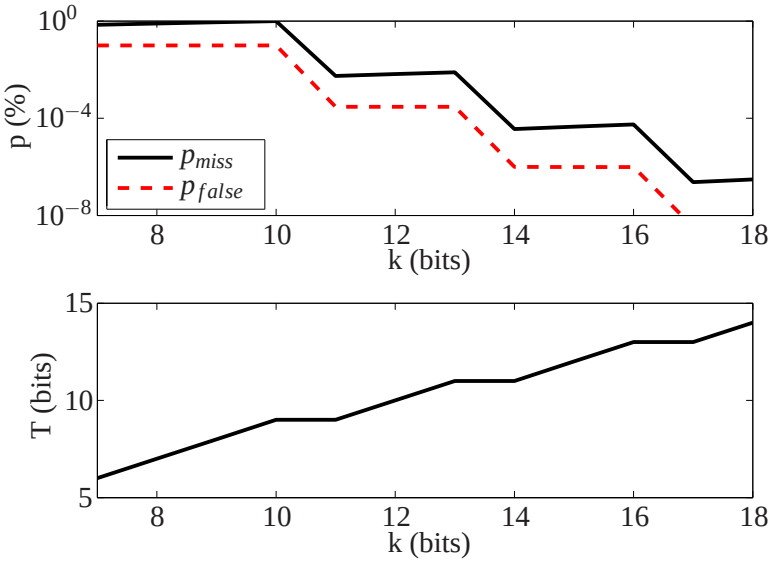


Figure 2.2: *p_{miss}, p_{false} and T as function of the address length l for a network of 100 nodes and a BER of 0.1%. T is chosen in a way to equate both error probabilities.*

both error probabilities. Taking into account that most WBAN have less than 100 nodes [1] and a BER of 10^{-3}, figure 2.2 gives the error probabilities as a function of the address length. For the minimal address length both p_{miss} and p_{false} are less than 1%, which is already acceptable. Adding extra bits decreases both the probabilities. However, the effect on the energy dissipation will be negligible since the error is already very low. Taking a Hamming distance of 3, an address length of 10 bits is good enough.

2.2.2 Radio Model

The state-transition diagram of a generic radio is shown in figure 2.3, and the corresponding parameters are listed in table 2.1. The initial start-up behavior is not shown; it is assumed that the radio is already initialized and that the main radio starts in the sleep state. There are two radios depicted in the diagram: the main radio and the WURx. Since the wake-up receiver is optional, it is placed outside the main radio whose states are depicted within the large dashed rectangle. The additional WURx can trigger the main radio to wake up or go into

Table 2.1: *Radio platform parameters*

Parameter	Explanation
T_{wake}	Switching duration: Sleep $\rightarrow$ Standby
T_{set}	Switching duration: Settling period when switching to Rx or Tx.
P_{sleep}	Power consumption in sleep mode.
$P_{standby}$	Power consumption in standby mode.
P_R	Power consumption in receive mode.
P_T	Power consumption in transmit mode.
P_{Rset}	Power consumption when switching to Rx mode.
P_{Tset}	Power consumption when switching to Tx mode.
P_{wake}	Power consumption when switching between sleep and standby mode.
ΔP_x	Power increase in mode x compared to sleep mode $P_x - P_{sleep}$
k	Length of minimal packet in bits. Used for: sync, ACK, WUC
R_b	Bit rate of main radio

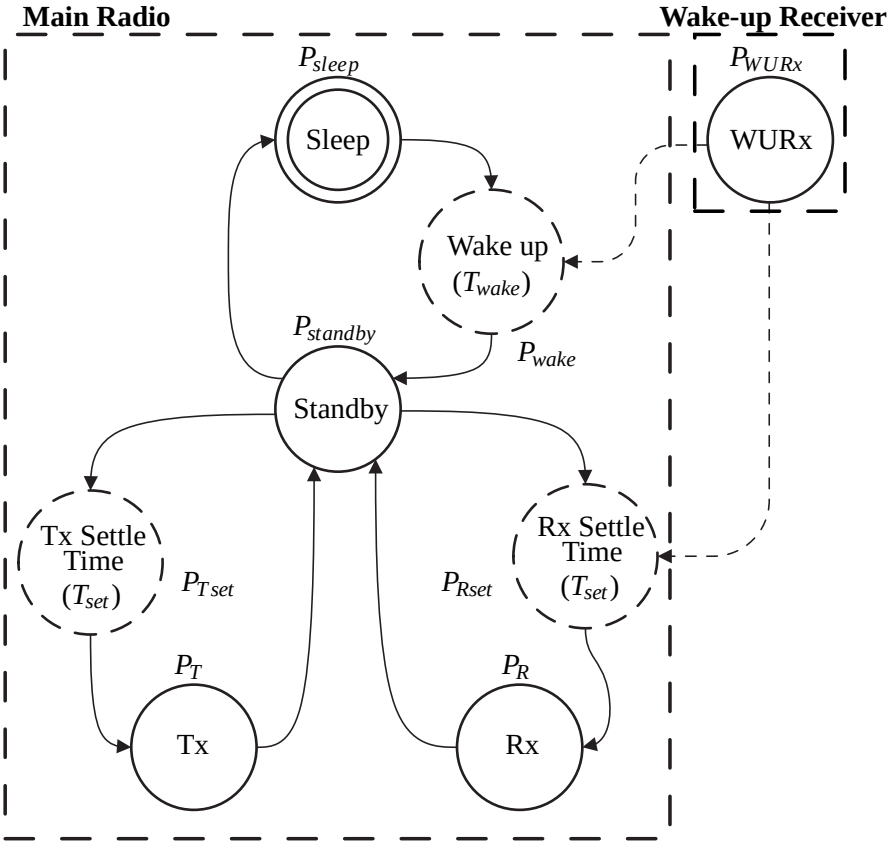


Figure 2.3: *General radio state-transition diagram.*

receive mode depending on the current state of the main radio.

The states with a solid line are stable radio states, i.e. the radio can be in these states for an arbitrary amount of time. The dotted lines are transition states, and the time spent in this state is given within brackets. Furthermore, the power consumption in each state is given outside the states.

In the sleep mode the radio is in its lowest power down state, while in the standby mode the receiver consumes more power. On the other hand, the radio can wake-up faster from the standby mode than from the sleep mode. Therefore, using the sleep mode can be disadvantageous because the energy needed for waking up might be larger than the energy saved by staying in the sleep mode instead of the standby mode. In the following sections the conditions for which the sleep mode is advantageous are analyzed.

Some radios may not provide a sleep and standby mode or may not need settling time between receive and transmit modes. T_{wake} should be set to zero in the former case and T_{set} should be set to zero in the latter case. When the radio is always on and does not need to settle, both of the parameters should be set to zero.

In this thesis the Nordic nRF24L01 radio chip is used in the application analysis, but the radio parameters are general enough to allow for other radios.

2.2.3 Network Statistics

In an asynchronous network the master node transmits wake-up calls (WUC) and waits for the node to transmit an acknowledgment (ACK). When a WUC or ACK packet gets missed with probability p_{miss}, they need to be retransmitted. However the maximum number of transmissions is limited to N^+_{WUC}; after this number of transmissions the transmitter quits and the wake-up process has failed. In each WUC a counter value is transmitted which specifies the number of transmissions left. Using this counter value the receiver knows exactly how many times it can try to transmit an acknowledgment. The node will transmit the acknowledgments until either the connection is set-up or the maximum number of transmissions is reached.

It is also possible for the node to wake up when a WUC is received which was meant for another node: a false wake up. After such an event the node starts transmitting false acknowledgment (FACK) packets. The false wake-up event leads to the overhearing penalty previously mentioned. The probability of a false wake up is given by p_{false}.

Table 2.2 gives a list of asynchronous and synchronous MAC layer packet statistics expressed as functions of p_{miss}, p_{false} and the maximal number of transmissions N^+_{WUC}. The probabilities and statistics are derived in appendix A.

The synchronous MAC protocol is discussed in-depth in section 2.2.6. The expected number of TDMA slots per received packet is given by μ_{slot}, which is very similar to the expected number of wake up calls. The variable μ_{slot} is derived in appendix A.4 and is approximately

$$\mu_{slot} \approx \frac{1 - p_{miss}^{N^+_{WUC}}}{1 - p_{miss}},$$

assuming $N^+_{WUC} > 1$ and $p_{miss} \lesssim 1\%$.

Table 2.2: *List of the used asynchronous (top) and synchronous (bottom) MAC layer packet statistics.*

Statistic	Probability/Value	Explanation
μ_{WUC}	$\approx \frac{1+p_{miss}}{1-p_{miss}}$	Average number of WUC transmissions per received packet.
$p_{ACK\geq 1}$	$1-p_{miss}^{N^+_{WUC}}$	Probability that the sensor node transmits at least one ACK packet.
$p_{FACK\geq 1}$	$\approx p_{false}$	Probability that the sensor node transmits at least one false ACK packet.
μ_{ACKx}	$\approx \frac{p_{miss}}{1-p_{miss}}$	Average number of retransmitted acknowledgments per received packet.
μ_{FACKx}	$\approx p_{false}\left(N^+_{WUC}-1\right)$	Average number of retransmitted false acknowledgments per received packet and node in the network.
μ_{slot}	$\approx \frac{1-p_{miss}^{N^+_{WUC}}}{1-p_{miss}}$	Expected number of TDMA slots per received packet.

2.2.4 WURx-enhanced Asynchronous Network

In the WURx-enhanced scheme, a WURx is added to the sensor node, which is used to listen for wake-up calls and waking up the sensor node when needed. There are two sub-categories of the WURx-enhanced MAC scheme: with and without main receiver. When the node needs to receive a lot of data and the low bit rate of the WURx is not sufficient an additional receiver can be added at the cost of higher power consumption. When the node is woken-up it transmits an acknowledgment and the data transfer can commence. Figure 2.4 shows a

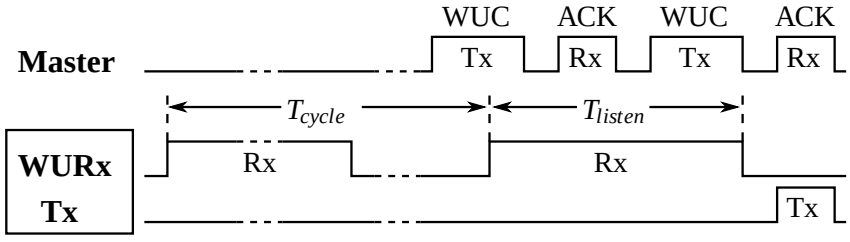


Figure 2.4: *Wake-up event for a WURx-enhanced MAC protocol.*

simplified overview of a wake-up event when the WURx enhanced scheme is used. To save power the WURx can be duty-cycled when the latency requirement allows for it, as is shown in the figure. The duty cycle period is chosen as long as possible to minimize the power consumption. Additionally the master needs to be able to transmit N^{+}_{WUC} calls within the latency requirement. Therefore, the cycle period is chosen equal to the latency requirement T_{lat} divided by the maximum number of attempts, i.e.

$$T_{cycle} = \frac{T_{lat}}{N^{+}_{WUC}} .$$

A detailed wake-up cycle is shown in figure 2.5. The radio parameters correspond with the parameters used in the radio state model depicted in figure 2.3. The wake-up periods are only present when the nodes go to the deep sleep mode. To ensure that the WURx will also wake up the node when the listen cycle starts in the middle of a WUC packet, at least two WUCs have to fit within the listen period T_{listen},

$$T_{listen} > 2\,(T_{set} + T_{wuc}) + T_{pkt} + T_{wake} . \tag{2.7}$$

Additionally, the listen period can never be longer than the complete cycle

$$T_{listen} \leq T_{cycle} , \tag{2.8}$$

and the duty cycle ratio η, the fraction of time a sensor node is active, is

$$\begin{aligned} \eta &= \frac{N^{+}_{WUC} T_{listen}}{T_{lat}} \\ &= \frac{T_{listen}}{T_{cycle}} . \end{aligned}$$

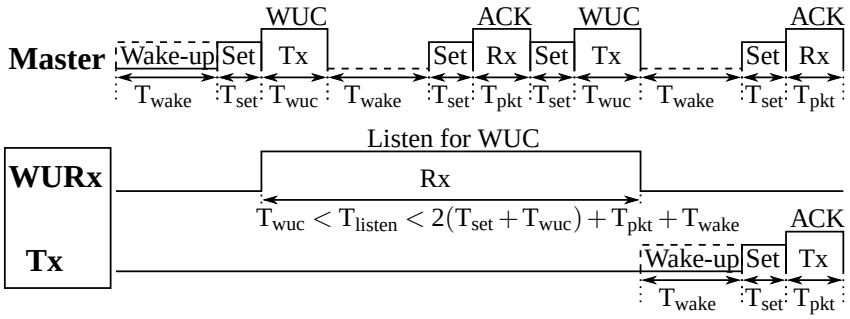


Figure 2.5: *Detailed view of a wake-up event.*

The packet lengths k of the WUC and ACK are assumed to be equal. However, the bit rates of the main radio R_b and WURx R_{bw} can be different and therefore the WUC and ACK packet durations can be different,

$$T_{wuc} = \frac{k}{R_{bw}}$$
$$T_{pkt} = \frac{k}{R_b}.$$

A lower bound on the required R_{bw} is obtained by combining (2.7) and (2.8)

$$R_{bw} \geq \frac{2k}{T_{cycle} - 2T_{set} - T_{wake} - T_{pkt}}. \tag{2.9}$$

The average energy dissipation per received packet is obtained by assuming that on average each node receives the same number of packets and a packet is received every $\frac{1}{\lambda}$ seconds. The dissipation of the sensor node is divided in 4 parts,

$$\begin{aligned} E_{node} = &\frac{P_{sleep}}{\lambda} + \eta \frac{P_{WURx}}{\lambda} + \left[p_{ACK\geq 1} + p_{FACK\geq 1}\left(N_{nodes} - 1\right)\right] E_{ACK1} \\ &+ \left[\mu_{ACKx} + \mu_{FACKx}\left(N_{nodes} - 1\right)\right] E_{ACKx}, \end{aligned} \tag{2.10}$$

the first term specifies the transceiver energy consumption in sleep mode, the second term the energy consumption of the duty-cycled WURx, the third term is the energy required when transmitting the first acknowledgment and the fourth and final term specifies the energy needed for retransmitting the acknowledgments. The false acknowledgment statistics $p_{FACK\geq 1}$ and μ_{FACKx} were defined per 'other node' in the network. Therefore, they are multiplied by number of 'other nodes', or the total number of nodes minus 1. The expected number of transmitted acknowledgments and retransmitted acknowledgments are derived in section 2.2.3, and the energy consumed per acknowledgment is

$$\begin{aligned} E_{ACK1} &= \Delta E_{wake} + \Delta E_{Tset} + T_{pkt}\Delta P_T \\ E_{ACKx} &= \left(T_{wake} + T_{WUC} + T_{set}\right)\Delta P_{standby} + \Delta E_{Tset} + T_{pkt}\Delta P_T. \end{aligned}$$

2.2.5 WURx-less Asynchronous Network

The asynchronous network scheme is very similar to the WURx-enhanced scheme, with the difference that the WURx is not present and the main receiver

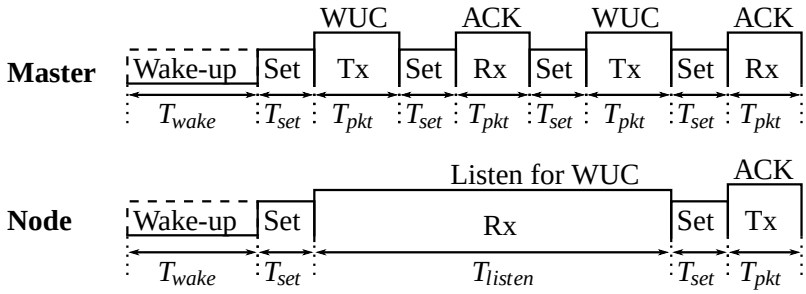


Figure 2.6: *Detailed view of a synchronization cycle for the WURx-less asynchronous MAC protocol.*

listens for the wake-up calls. Therefore, in the asynchronous MAC protocol the WUC and ACK packets duration is the same. Although this scheme consumes more power than the WURx enhanced scheme, it has benefits for systems with very strict latency requirements since the wake-up time is shorter. Figure 2.6 shows the synchronization cycle.

The energy consumption of the sensor node is similar to the WURx-enhanced case (2.10)

$$E_{node} = \frac{P_{sleep}}{\lambda} + \frac{1}{\lambda T_{cycle}} E_{cycle} + \left[p_{ACK\geq 1} + p_{FACK\geq 1}\left(N_{nodes}-1\right)\right] E_{ACK1} + \left[\mu_{ACKx} + \mu_{FACKx}\left(N_{nodes}-1\right)\right] E_{ACKx},$$

where the values $p_{ACK\geq 1}$ and μ_{ACKx} were derived in appendix A and summarized in table 2.2, and

$$\begin{aligned} E_{ACK1} &= \Delta E_{Tset} + T_{pkt}\Delta P_T \\ E_{ACKx} &= \left(T_{pkt} + T_{set}\right)\Delta P_{standby} + \Delta E_{Tset} + T_{pkt}\Delta P_T \\ E_{cycle} &= \Delta E_{wake} + \Delta E_{Rset} + T_{listen}\Delta P_R\,. \end{aligned}$$

2.2.6 Synchronous Network

The synchronous MAC scheme is different from the two MAC schemes mentioned in the previous sections. The main difference is that the whole network is always synchronized, whereas in the asynchronous MAC protocols the transmitter and receiver are only synchronized before a transmission. Furthermore,

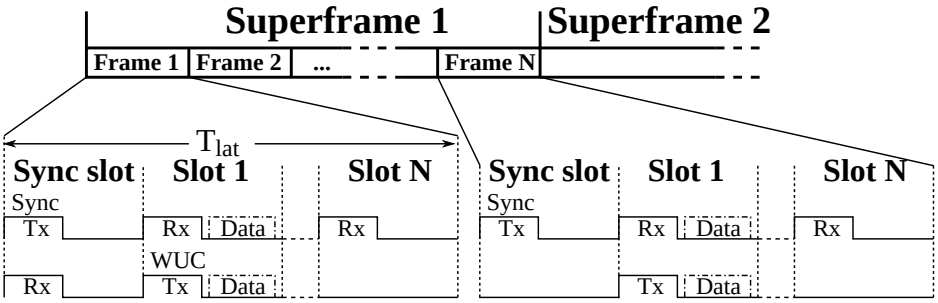


Figure 2.7: *Synchronous MAC scheme in case of a wake-up event. As an example the timing diagrams of the master and node 1 are shown.*

the system is highly asymmetric. Within this section the energy consumption of a sensor node in a low-power TDMA MAC protocol similar to [8] is presented. The energy consumption of the master node is not taken into account, since it is assumed that its power supply is much bigger than that of a wireless sensor node.

Figure 2.7 shows an overview of the synchronous scheme. The master node transmits synchronization beacons at known intervals to keep the network synchronized. Additionally, the master node assigns the time slots to the nodes in the network. Each frame is divided in multiple time slots; one for every node, within these slots only the assigned nodes can transmit their data. The nodes notify the master they have data to transmit using a wake-up call and then start sending the data.

A receiving node only needs to receive a synchronization beacon every superframe; the time between two beacons is determined by the stability of the local clock. The local clock accuracy given by Θ is expressed in ppm. The maximally allowed clock skew is given by T_{skew}, which is used as guard time. A more detailed view is shown in figure 2.8. Again the wake-up periods are only present when the nodes go to deep sleep mode. The gray areas are needed to deal with clock skew. The latency has to be smaller than T_{lat}, and within the latency period all the N_{node} nodes need to be able to transmit N^{+}_{WUC} wake-up calls. Therefore, the TDMA slot time is

$$T_{slot} = \frac{T_{lat}}{N^{+}_{WUC}\,(N_{node}+1)}\,.$$

It is assumed that the minimal time between two beacons is large enough to ensure correct transmission: $T_{beacon} \gg \frac{T_{lat}}{N^{+}_{WUC}}$. On the other hand, the maximum time between two synchronization beacons to keep the network synchronized is

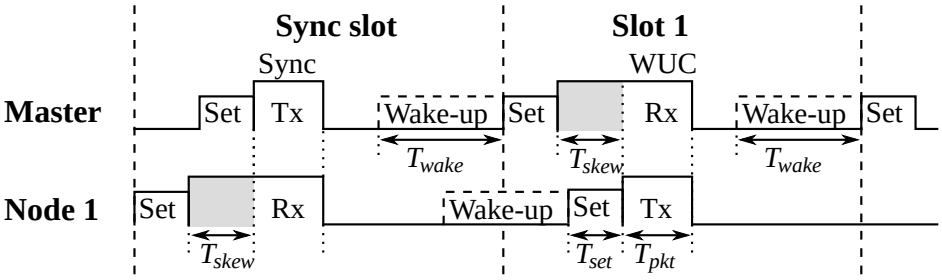


Figure 2.8: *Detailed view of the synchronous MAC scheme in case of a wake-up event with the radio state variables. The clocks of the master node and Node 1 are not fully synchronized.*

a function of the clock accuracy and the time reserved for the clock skew:

$$T_{beacon} \leq \frac{T_{skew}}{\Theta(\text{ppm})} 10^6 .$$

In the following analysis we assume the time between beacons is minimal to reduce the energy consumption. The average number of beacons per received packet $\mu_{bcn/pkt}$ is

$$\mu_{bcn/pkt} = \frac{1}{\lambda T_{beacon}} .$$

When a node misses the synchronization beacon it stays in receive mode until it receives the next beacon in order to resynchronize. While resynchronizing, all the packets are lost. The probability of this event is assumed to be equal to the packet miss probability p_{miss}. If T_{beacon} is large, the resynchronization penalty is severe.

The average energy consumption of a sensor node, calculated per received packet is:

$$E_{node} = \frac{P_{sleep}}{\lambda} + \mu_{bcn/pkt} E_{sync} + p_{miss} \frac{\Delta P_R}{\lambda} + \mu_{slot} E_{slot} , \qquad (2.11)$$

where

$$E_{sync} = \Delta E_{wake} + \Delta E_{Rset} + \left(T_{skew} + T_{pkt}\right) \Delta P_R$$
$$E_{slot} = \Delta E_{wake} + \Delta E_{Tset} + T_{pkt} \Delta P_T .$$

2.2.7 Application Example

In this section the average power consumption per packet is calculated for a typical application. The application resembles the Holst ECG demonstrator. It is a network of sensor nodes attached to the human body, which consists of one master node and three sensor nodes. The application parameters are listed in table 2.3. The WURx front-end presented in chapter 6 and Nordic radio given in appendix B are used when comparing the power consumption in synchronous WURx-enhanced networks.

Table 2.3: *Application and WURx parameters*

Parameter	Value
λ	33 pkt/sec
T_{lat}	30 ms
N_{nodes}	3 sensor + 1 master
p_{miss}, p_{false}	1%
N^{+}_{WUC}	3
P_{WURx}	329 µW
R_{bw}	625 kbps

The average power consumption per packet depicted in figure 2.9 is calculated using the model presented in section 2.2. The average power consumption

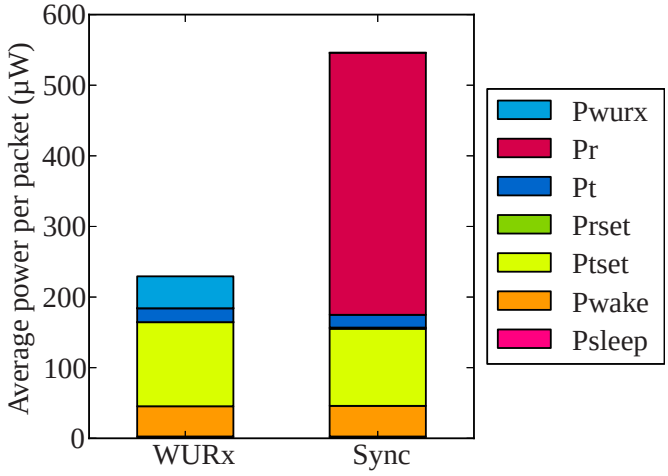


Figure 2.9: *Average power consumption per packet for the WURx-enhanced and synchronous networks.*

needed for the synchronization is split in the different modes used in the radio model given in figure 2.3. The power needed to transmit the acknowledgments, consisting of P_{tset} and P_t, is the same in both cases, since the same retransmission scheme and transmitter are used. The penalty for a false wake-up in the WURx-enhanced scheme only attributes 4.5% to the total power consumption. Thus the simple address coding scheme suffices. Moreover, the Nordic radio wake-up power P_{wake} and sleep power P_{sleep} are almost equal in both synchronization schemes. However, the power is reduced by using the WURx (P_{WURx}) to listen for wake-up calls instead of the Nordic radio ($P_{rset} + P_r$). When using the WURx-enhanced synchronization the power is reduced by 58% when compared to the synchronous network. Note that the amount of power saved strongly depends on the packet rate λ and latency T_{lat} requirements.

2.3 Applications

Many different applications for WBAN can be found in literature. An overview of required transmission distances and latency requirements reported in the overview papers [1] and [2] are given in table 2.4. From the given literature

Table 2.4: *WBAN network parameters*

Ref	# nodes typ/max	Distance	Latency
[1]	10 / <100	2m / 5m	10ms / 1s setup
[2]	6 / <256	<3m	125ms (medical) / 250ms (non-medical)

it can be concluded that a typical WBAN network consists of 10 nodes and the transmission distance is less than 10m.

Furthermore, the application space of WBAN networks can be divided in three scenarios:

Multimedia Applications in this scenario have a very high bit rate, which is not supported by the WURx. Therefore, an additional high bit rate, high power receiver needs to be added to the sensor node for the data transfer.

Active RFID In this category, the application bit rate is relatively low and the WURx can handle the data transfer. Most data is transmitted from the low-power sensor node to the master node. Application examples are fitness sensors, medical sensors and a 'forgotten things' network.

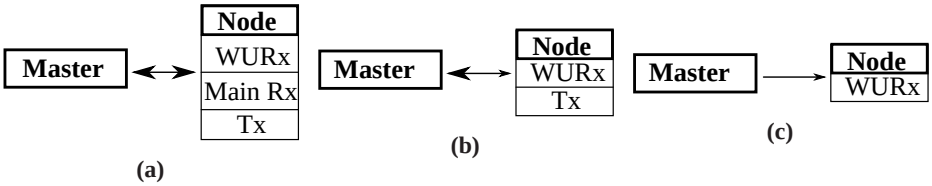


Figure 2.10: *Radio topologies used in the three different application scenarios, where the arrow sizes depict the amount of data transfer from master to sensor node or vice versa. a) Multimedia b) Active RFID c) Remote control.*

Remote control The master sends very simple commands to peripheral devices, for example to turn devices on or off, select a radio station and control hands-free devices.

The radio topologies used in the three different scenarios are depicted in figure 2.10. Additionally, the data transfer is schematically depicted by the size of the arrows.

In literature many WBAN applications are presented, although most of them target medical applications. A short survey is given in table 2.5. It is interesting to note that the estimated data rate for ECG applications ranges from 3kbps to 288kbps. This can partly be explained by the number of leads used. It could be that in some applications the raw data is processed locally and only the measured parameters are transmitted, thereby greatly reducing the amount of data to transmit. From the reported applications it can be concluded that most applications fall into the active-RFID category.

2.4 Solution Space

Since the targeted WBAN network is asymmetric and uses a star topology, only the power consumption of the low-power sensor nodes are of concern. Furthermore, since the data transfer phase is the same for the MAC protocols, only the power consumption of the synchronization phase is taken into account.

Depending on the application parameters, one of the MAC protocols leads to the lowest power consumption of the wireless sensor nodes. The most important application parameters are the number of nodes N_{node}, packet rate λ and the maximal latency requirement T_{lat}. Even without making assumptions about the specific radios used, the solution space can be divided between the different

Table 2.5: *Typical WBAN application parameters as seen from the sensor node perspective.*

Ref	Scenario	Application	Sensor	Data rate
[1]	Active RFID	Fitness	Speed, distance, heart rate	<500 kbps
		Mobile	Sensor, headset, handsfree	<500 kbps
	Remote ctrl	Remote control	Headset ctrl, printers, ID	
	Multimedia	Video	Video communications	<20 Mbps
[3]	Active RFID	Medical	ECG (12 leads)	288 kbps
			ECG (6 leads)	71 kbps
			EMG	320 kbps
			EEG (6 leads)	43.2 kbps
			Blood saturation	16 bps
			Glucose sensor	1600 bps
			Temperature	120 bps
			Motion sensor	35 kbps
			Cochlear implant	100 kbps
			Artificial retina	50-700 kbps
	Multimedia	Audio	Audio streaming	1 Mbps
[4]	Active RFID	In-body	Glucose sensor	Few kbps
			Pacemaker	Few kbps
		Medical	ECG	3 kbps
			SpO2	32 kbps
			Blood pressure	<10 bps
		Non-medical	Forgotten things	256 kbps
			Social networking	<200 kbps
		In-body	Endoscope capsule	>2 Mbps
		Non-medical	Music for headset	1.4Mbps

MAC protocols. A schematic overview of these regions is shown in figure 2.11 (the axes are not drawn to scale).

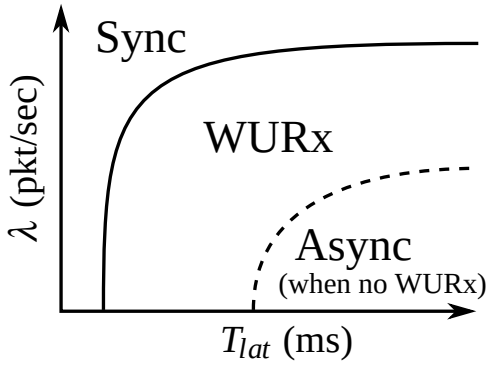


Figure 2.11: *Solution space showing the most optimal MAC synchronization scheme as a function of the latency and packet rate, note that the axes are not drawn to scale.*

The practical boundary conditions are not taken into account yet, they will be discussed later in this section. Three different regions can be distinguished:

Sync In this region the synchronous scheme is the best alternative. The WURx and main transceiver in the asynchronous scheme cannot be duty cycled, either because the maximally allowed latency is too low and the radio can not wake up fast enough, or the packet rate is too high. Therefore the transceiver does not spend a lot of time in the sleep mode in the asynchronous MAC protocols, and the WURx-enhanced MAC protocol consumes a lot of power.

WURx When the packet rate is lower and the latency is higher the WURx becomes a better alternative, since the sensor node is in sleep mode for longer periods. Additionally, a lot of time slots are assigned but not used in the synchronous TDMA protocol. Therefore, the TDMA synchronization overhead per received packet increases. Consequently, adding a WURx to the sensor node reduces the power consumption.

Async When the latency and packet rate requirements are further relaxed, even the WURx-less asynchronous MAC protocol is more power efficient than the TDMA MAC. However, adding a WURx always reduces the power consumption as long as the WURx consumes less power than the main radio.

The WURx-enhanced protocol is the best choice when its energy consumption given by (2.10) is less than the energy consumption of the TDMA protocol given

by (2.11). After multiplying both equations by the packet rate to obtain the power consumption, and assuming $\mu_{slot} \approx 1$ and $\mu_{ACK1} + \mu_{FACK1} \approx 1$, the inequality becomes

$$P_{WURx} + \underbrace{\lambda\,(\mu_{ACKx} + \mu_{FACKx})\,E_{ACKx}}_{\text{ACK retransmission}} < \underbrace{\frac{1}{T_{beacon}} E_{sync}}_{\text{Sync overhead}} + \underbrace{p_{miss}\,\Delta P_R}_{\text{Resync penalty}} .$$

In other words, the WURx-enhanced protocol is more power efficient when its synchronization overhead is less than the TDMA overhead. Furthermore, the WURx power budget is

$$P_{WURx} = \frac{1}{T_{beacon}} E_{sync} + p_{miss}\,\Delta P_R - \lambda\,(\mu_{ACKx} + \mu_{FACKx})\,E_{ACKx}\,.$$

It is assumed there is only one synchronization channel. This introduces limits on the maximal number of nodes, packet rate and minimal latency requirements. The boundary conditions are schematically depicted in figure 2.12. Again, the axes are not drawn to scale. The boundary conditions are:

Above I; high packet rate; low latency At a very low latency and high packet rate the channel will be utilized more than 100%, hence there is no viable solution.

Between I and II The synchronous TDMA MAC scheme can manage with the lowest latency, and is the only viable MAC scheme. An asynchronous MAC scheme needs additional time to listen for WUCs. Also the WURx is not viable in this region since additional time is needed for waking up

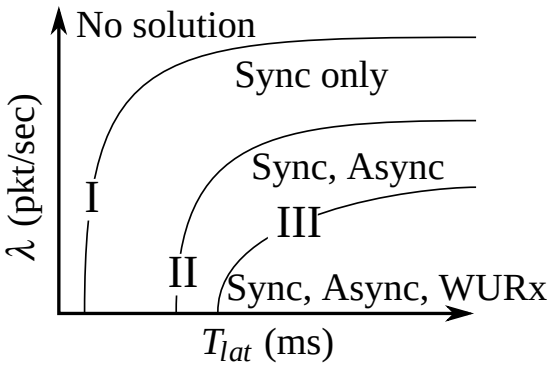


Figure 2.12: *Feasible synchronization schemes as a function of the link-setup latency and packet rate.*

the main radio after the WUC is received and the WUC itself takes longer to transmit because of the lower WURx bit rate. In the TDMA protocol at least the WUC and settling time has to fit within one time slot. Therefore in this region the following conditions hold:

$$\begin{aligned} T_{slot} &> T_{pkt} + T_{set} \\ \frac{T_{lat}}{N^{+}_{WUC}} &> (N_{node} + 1)\left(T_{pkt} + T_{set}\right) . \end{aligned}$$

Between II and III The latency requirement is more relaxed and the packet rate is lower. The WURx-less asynchronous protocol can be used when the listen period and wake-up time fits within the synchronization cycle:

$$\begin{aligned} T_{cycle} &> T_{wake} + T_{set} + T_{listen} \\ \frac{T_{lat}}{N^{+}_{WUC}} &> T_{wake} + 3T_{set} + 3T_{pkt} . \end{aligned}$$

Below III The bit rate of the WURx is not a problem anymore, because higher latency is tolerated. Therefore the boundary condition III is the same as the boundary condition on the WURx bit rate given by (2.9), and the following holds:

$$\frac{T_{lat}}{N^{+}_{WUC}} > 2T_{wake} + 3T_{set} + T_{pkt} + 2T_{WUC} .$$

In order to calculate the average synchronization power consumption of wireless sensor nodes, the actual power consumption of the transceivers need to be known. A typical low-power transceiver is the Nordic nRF24L01 radio chip. Its power consumption and other specifications are given in appendix B. Additionally, the second WURx version described in section 6, with a data rate of 625kbps is used to calculate the average power consumption.

Table 2.6: *WBAN network parameters*

Parameter	N_{node}	Packet size k	N^{+}_{WUC}	p_{miss} and p_{false}
Value	10	32	3	0.1%

Using a typical network size of 10 nodes and the network parameters given in table 2.6 the power consumptions shown in figure 2.13 are obtained. Note that the latency axis is inverted for ease of reading. The WURx-enhanced MAC protocol leads to the lowest power consumption when the packet rate is low and the

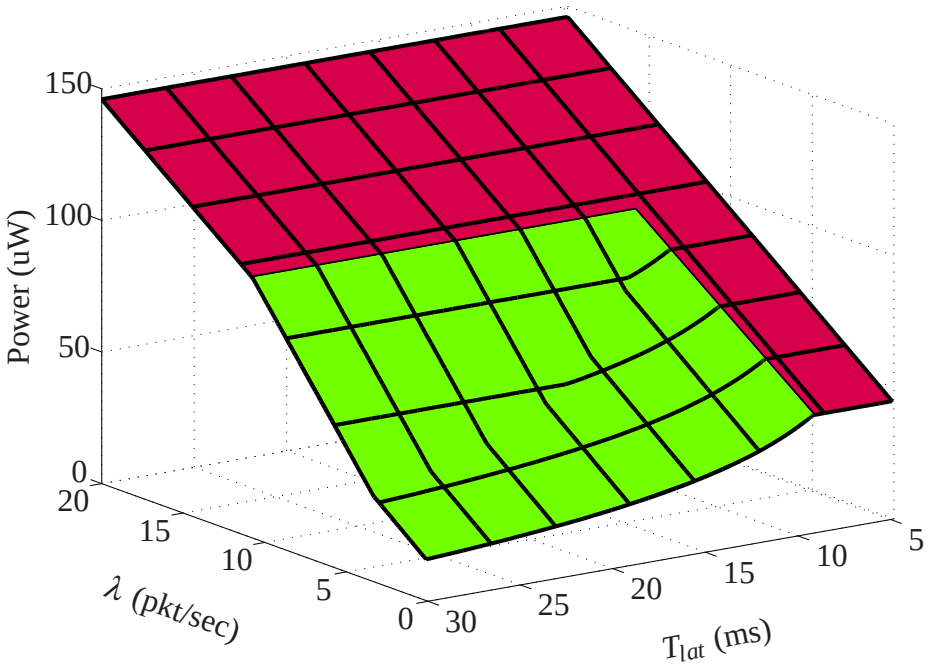


Figure 2.13: *Average synchronization power consumption using the Nordic nRF24L01 transceiver, WURx V2 and the parameters given in table 2.6. In the green (light) area the WURx-enhanced MAC is the best choice and in the red (dark) area the synchronous TDMA MAC protocol leads to lower power consumption.*

latency requirement is not strict, i.e. when T_{lat} is high. In this region the sensor node can sleep for prolonged periods of time and the WURx can be duty cycled to save power. From the application table 2.5 it is clear that many applications fit these properties.

2.5 Conclusion

In this chapter, the WBAN and WURx concepts were introduced, and a literature overview of WBAN applications was given. Additionally, the energy consumption of both asynchronous and synchronous MAC layer protocols were analyzed. The targeted WBAN applications for the Wake-up Receiver consist of a small number of nodes, approximately 10, and has a short transmission distance, i.e. less than 10m. Additionally, the network is highly asymmetric, i.e. the master node has a large power supply and processing capability, whereas the sensor

node has only a very small power supply and should be kept as simple as possible. Therefore, the network uses a single-hop star topology. Furthermore, the packet rate is low, namely less than 10 (pkt/sec) and the latency requirement T_{lat} is not very strict.

MAC-layer protocols used for network synchronization have a big influence on the energy dissipation needed for node-to-node communication. Energy is wasted in the link synchronization because of:

- idle listening
- overhearing
- synchronization overhead

The idle listening energy consumption is the main contributor in asynchronous network protocols. In synchronous networks most energy is consumed in the frame synchronization, thus in the synchronization overhead. In both network types the overhearing problem can be neglected when assuming a small network size, i.e. no more than a few hundred nodes, packet error rate of less than 1%, and address coding with a few bits Hamming distance.

In the proposed WBAN scenario the WURx-enhanced MAC scheme leads to the lowest power consumption.

CHAPTER 3

WAKE-UP RECEIVER SYSTEM LEVEL DESIGN

In the previous chapter the WBAN system and application parameters were discussed. In this chapter the focus lays on the high-level wake-up receiver (WURx) system design. The goal is to make choices on the modulation and receiver specifications, which can be used in the circuit design discussed in the following chapters.

In the first section, a state-of-the-art literature survey of ultra-low-power receivers is presented. Next, the modulation complexity is discussed; it is shown that On-Off Keying (OOK) and Frequency Shift Keying (FSK) are viable modulation schemes for ultra-low-power receiver design.

The zero-IF architecture is a good candidate for low-power receivers, since only one frequency down-conversion stage is needed. Additionally the baseband bandwidth is minimal, leading to a low power consumption in the baseband stage. On the other hand, zero-IF receivers are sensitive to DC offsets partly caused by LO feed-through, amplitude modulated interferers, and low frequency 1/f noise. Using wideband-FSK modulation the DC offset and 1/f noise problems can be alleviated, as is discussed in section 3.3. Therefore, wideband FSK modulation is chosen for the WURx design. In section 3.4 a mathematical model of the FSK receiver and demodulator including receiver impairments such as receiver noise figure, I/Q imbalance and phase noise is developed. The receiver model is used within section 3.5 to develop a closed-form analytical model, which is

then used to study the influence of the receiver impairments on the bit error rate (BER) and the output signal-to-noise-ratio (SNR) both below and above the FM threshold. When the input SNR drops below the FM threshold the output SNR degrades rapidly. The closed-form models can be used when deriving minimal receiver specs for low-power FSK receivers. Additionally the models are a means of gaining insight into the influences of the receiver impairments on its performance. The results are used to estimate the required SNR at the output of the receiver for a specified BER, which can be used to obtain the noise figure and phase noise requirements as is done in section 3.6.

3.1 State of the Art

Over the last years, many low-power receivers have been reported. Almost all of the reported receivers use either FSK or OOK modulation, as listed in table 3.1 and 3.2 respectively. It is clear that the reported FSK receivers in general consume more power than the reported OOK systems. This is mainly caused by the frequency reference, for example an on-chip Phase Locked Loop (PLL) [9], needed by the FSK receivers. However in general, the reported FSK receivers have a higher bit rate than the OOK receivers.

Almost all reported low-power OOK receivers use envelope-detectors. The non-linear nature of the envelope detectors is used to demodulate the OOK signals, which makes them very sensitive to interferers. Hence, external, i.e. off-chip, bulk acoustic wave (BAW) filters are necessary to filter the interferers at the input of the OOK receivers. An exception is [20] which uses a mixer-first architecture to obtain a very high linearity at the cost of high power consumption.

Other low-power receivers use FSK modulation [9, 12–15], which is slightly more interferer-robust than OOK modulation [27]. Because the frequency reference needs to be stable, most FSK receivers use power consuming PLLs [9]. Receivers using injection-locking [14] have a lower power consumption, but are more sensitive to blockers.

Table 3.1: *Reported state-of-the-art low-power FSK receivers.*

REF	CMOS (nm)	Power (V / μW)	Frequency (MHz)	NF (dB)	P_{-1dBc} (dBm)	P_{sens} (dBm)	R_b (kbps)
[9]	130	1.2 / 1920	825-983	10	-10	-83	45-48
[10]	180	1.0-1.6 / 2100	434/868	2.5/4.5	-45/-42*	-111/-108	12.5-100
[11]	250	2.7 / 800	900	12	-13	-90	20
[12]	180	1.0 / 500	2400	10.1	-31	-	100
[13]	130	0.4 / 330	1950-2380	7	-17.5*	-	300
[14]	180	0.7 / 420	920	-	-	-73	5000
[15]	180	0.7 / 490	398-408	-	-	-68	250
[16]	130	0.25 / 352	1500-1650	7.2	-48	-	-
[17]	Sim	1.5 / 281	900	-	-	-73	250
[18]	180	1.8 / 11700	760-1000	19	-15	-	-
[19]	180	0.7 & 1.0 / 1088	2220-2450	10.1	-31	-	100

* Since the 1dB compression point was not given it is estimated by subtracting 10dB from the reported IIP3.

Table 3.2: *Reported state-of-the-art low-power OOK receivers.*

REF	CMOS (nm)	Power (V / μW)	Frequency (MHz)	NF (dB)	P_{-1dBc} (dBm)	P_{sens} (dBm)	R_b (kbps)
[20]	65	1.2 / 67000	200-2000	6.5	1[†]	-	0.1-10
[21]	-	0.9-1.3 / 400	1900	-	-	-100.5	5
[22]	90	- / 400	402-450	-	-	-93	120
[23]	90	0.5 / 52	1900-2100	-	-	-72	100
[24]	90	0.5 / 65	1900	-	-	-49	20-100
[25]	90	1.0 / 64 (146)	780-950	-	-30	-45 (-86)	1-100
[26]	90	1.0 / 51	915 / 2400	-	-	-75 / -64	100

[†] Since the 1dB compression point was not given it is estimated by subtracting 10dB from the reported IIP3.

3.2 Modulation Complexity

Since the main design goal is low power consumption, the modulation complexity should be kept as low as possible. The higher the complexity, the more stringent the receiver and transmitter requirements on various performance parameters, for example error vector magnitude (EVM), phase noise and I/Q imbalance. Figure 3.1 shows the complexity of many digital modulation types that are discussed in [27]. When comparing the modulation complexity shown in figure 3.1

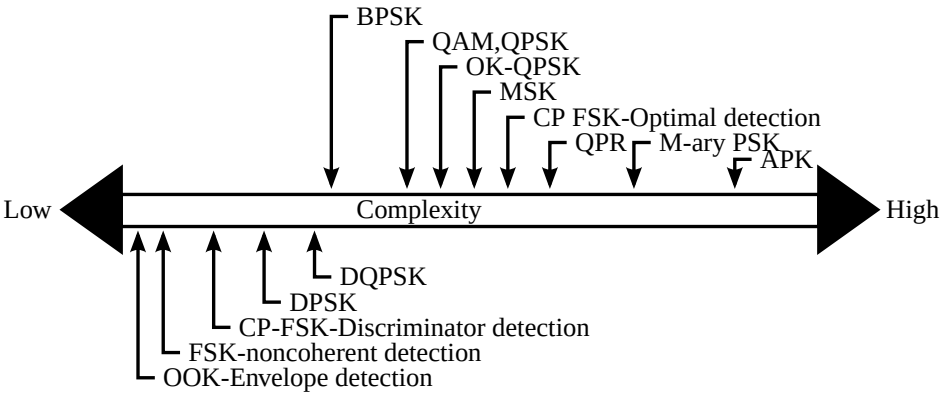


Figure 3.1: *Modulation complexity for various modulation types; this figure is adopted from [27]. OK-QPSK is also known as O-QPSK.*

with the state of the art receivers summarized in tables 3.1 and 3.2, it can be noted that the reported low-power receivers use, indeed, the two least complex demodulation schemes: envelope detector based OOK and non-coherent FSK demodulation. Therefore, in the view of low-power receiver design, either OOK or FSK modulation should be considered.

While envelope detector based OOK receivers have a lower average power consumption, they require bulky and costly bulk acoustic wave (BAW) or surface acoustic wave (SAW) filters. The reported ultra-low-power OOK receivers use an envelope detector instead of a down-conversion mixer to translate the received signal from the carrier frequency down to the baseband frequency. The nonlinear nature of the used envelope detectors make the OOK receivers more vulnerable to interferers than FSK receivers, which increases their packet error rate and increases the retransmission power consumption.

Considering the power consumption, required external filters and frequency selectivity, FSK modulation is chosen. The power consumption is reduced by generating signal gain at lower frequencies and removing the LNA from the RF

front-end as will be explained in section 4.1, and replacing the PLL with a power-efficient automatic frequency control (AFC) loop, see section 4.4.

3.3 Zero-IF Architecture

The zero-IF architecture lends itself for low-power integrated CMOS receivers. In a zero-IF receiver the received signal is directly down-converted to DC, as can be seen in the block diagram depicted in figure 3.2. The same architecture is used in low-IF receivers where the received signal is down-converted to higher frequencies. The receiver architecture is very power efficient since only one

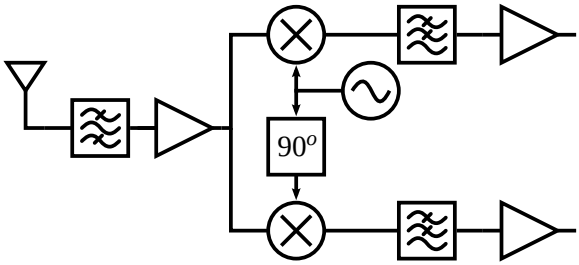


Figure 3.2: *Simplified block diagram of the zero-IF receiver analog front-end.*

frequency down-conversion stage and oscillator are needed. Moreover, the baseband signal bandwidth is very low and hence the ADC and baseband amplifiers and filters consume less power when compared to low-IF architectures.

However, the zero-IF architecture has some down-sides. For one, the receiver is sensitive to DC offsets caused by offsets in the baseband amplifiers and self-mixing of the LO signal. Additionally, the receiver is sensitive to 1/f noise since most of the signal is concentrated around DC where the 1/f noise is highest. When a modulation scheme is used which has as little signal power round DC as possible a high-pass filter can be used to remove the DC offset and decrease the 1/f noise. An additional benefit is the faster start-up time, which helps reducing the overall power consumption in duty-cycled systems. Therefore, wideband FSK modulation is chosen for the design of the system in this thesis. The modulation index

$$h = \frac{2\Delta f}{R_b} \tag{3.1}$$

depends on the frequency deviation Δf and the bit rate R_b. When h increases, the power spectral density concentrates more and more around the frequency deviation as can be seen in figure 3.3.

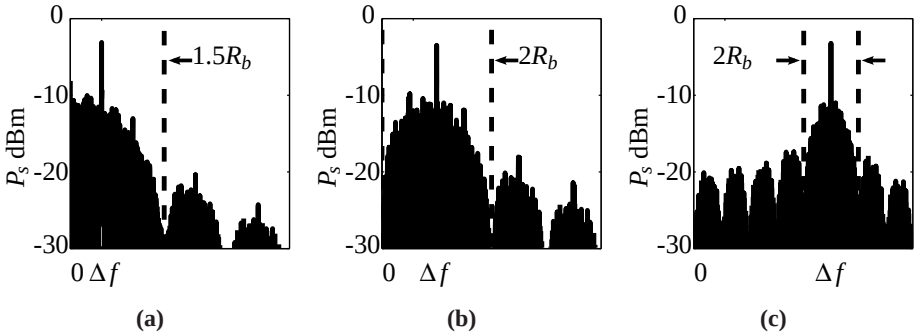


Figure 3.3: *Power spectral density of random modulated FSK signals for different modulation indices a) h=1 b) h=2 c) h=10.*

3.4 FSK Receiver Model

Figure 3.4 shows a simplified schematic of a limiter-discriminator FSK receiver; the receiver impairments are neglected for the moment. The limiter-discriminator is used since it is an optimal FSK demodulator [28]. All the signals are represented in the power domain, not in the voltage or current domains. First, the

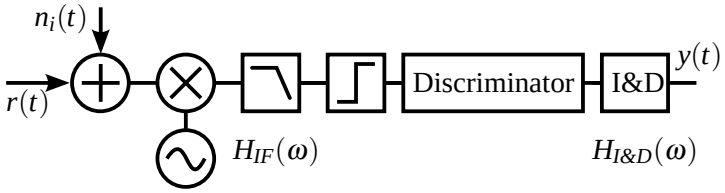


Figure 3.4: *Schematic overview of an FSK receiver.*

received signal $r(t)$ is down-converted to baseband frequencies, where the low-pass IF filter $H_{IF}(\omega)$ ensures that only the down-converted signal remains and all the higher harmonics are filtered out. The IF filter is modeled as an ideal brick-wall filter and the modulus of its transfer function is

$$|H_{IF}(\omega)| = \text{rect}\left(\frac{\omega}{2B_{IF}}\right), \tag{3.2}$$

where B_{IF} is the IF filter bandwidth. The down-converted bandwidth-limited signal is then demodulated using the frequency discriminator and finally filtered by an integrate-and-dump (I&D) filter $H_{I\&D}(\omega)$, which is a matched filter for

block-pulse data with added white Gaussian noise. The modulus of the integrate and dump filter is given below, where $R_b = \frac{1}{T_b}$ is the bit rate,

$$|H_{I\&D}(\omega)| = \operatorname{sinc}\left(\frac{\omega}{2R_b}\right).$$

The incoming signal $r(t)$ and input noise $n_i(t)$ are expressed as real functions of the complex RF signal, i.e.

$$r(t) = \operatorname{Re}\{[A\exp\{-j\varphi(t)\}]\exp\{j\omega_o t\}\}$$
$$n_i(t) = \operatorname{Re}\{[n_{i,I}(t) - jn_{i,Q}(t)]\exp\{j\omega_o t\}\},$$

where the variance, and power of $n_i(t)$ is

$$\sigma_i^2 = k_B T_o B_{IF},$$

and $\frac{A^2}{2}$ is the received signal power, ω_o the carrier frequency and $\varphi(t)$ the FSK signal phase. Furthermore, the additive white Gaussian input noise with power spectral density $\frac{k_B T_o}{2}$ is given by $n_i(t)$. The real noise processes $n_{i,I}(t)$ and $n_{i,Q}(t)$ are uncorrelated and their variances are equal to the variance of the real-valued process $n_i(t)$. The carrier-to-noise-ratio (CNR) is given by

$$\rho = \frac{A^2}{2\sigma_i^2}. \tag{3.3}$$

The low-pass equivalent signals can be written as vectors

$$\boldsymbol{r}(t) = A\begin{bmatrix} \cos(\varphi(t)) \\ \sin(\varphi(t)) \end{bmatrix}$$
$$\boldsymbol{n_i}(t) = \begin{bmatrix} n_{i,I}(t) \\ n_{i,Q}(t) \end{bmatrix}.$$

The first element represents the in-phase component and the second element the quadrature-phase component; they are denoted by subscripts I and Q respectively.

In this chapter we analyze binary modulated data and assume that the bits a_n are rectangular pulses with an amplitude ± 1 and a bit period T_b. The corresponding FSK phase φ is

$$\varphi(t) = \Delta\omega \int_{-\infty}^{t} \sum_{n=-\infty}^{\infty} a_n \operatorname{rect}\left(\frac{\tau - nT_b}{T_b}\right) d\tau, \tag{3.4}$$

where $\Delta\omega$ is the frequency deviation and the modulation index is defined in (3.1) as

$$h = \frac{\Delta\omega}{\pi R_b}.$$

FSK modulation is called "Wideband FSK" when the modulation index is larger than 1 [29].

3.4.1 Non-Ideal Receiver Front-End

Figure 3.5 shows the real front-end with impairments; four impairments are taken into account: the gain g and phase ε mismatch between the I and Q paths, the local oscillator phase noise $\theta(t)$, noise generated before the I/Q split n_{rf}, and noise generated after the I/Q split n_{bb} with noise power σ_{rf}^2 and σ_{bb}^2. The noise factor is a measure of signal to noise ratio degradation, and given the input noise is thermal it is:

$$F \stackrel{\text{def}}{=} \frac{SNR_{in}}{SNR_{out}},$$

which is relatively high in low-power mixer-first topologies, where noise performance is traded for lower power-consumption, see [30] and [31]. The RF and baseband noise variances as a function of the noise factor are:

$$\begin{aligned} \sigma_{rf}^2 &= F_{RF}\ \sigma_i^2 \\ \sigma_{bb}^2 &= (F_{BB} - 1)\sigma_i^2. \end{aligned} \tag{3.5}$$

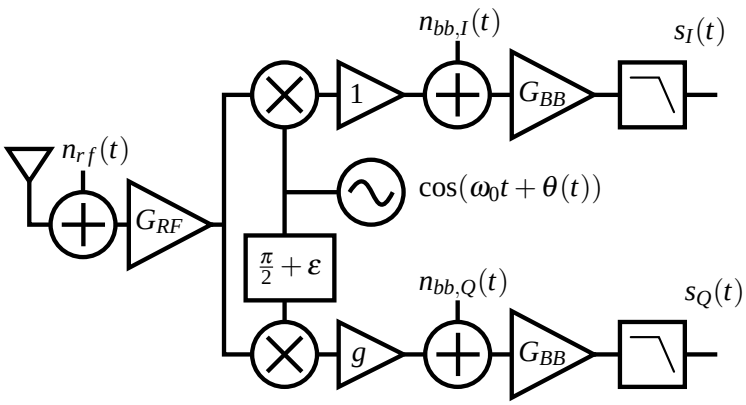


Figure 3.5: *Block diagram of the non-ideal receiver front-end.*

The LO phase noise model is discussed in more depth in section 3.4.2. In an ideal receiver front-end the phase mismatch ε equals zero and the gain g equals one. The output signal vector $\boldsymbol{s}(t)$ of the receiver front-end is

$$\boldsymbol{s}(t) = G_{BB}\left\{\boldsymbol{M}_{rx}(t)\left[\boldsymbol{r}(t)+\boldsymbol{n}_{rf}(t)\right]+\boldsymbol{n}_{bb}(t)\right\}, \tag{3.6}$$

where the matrix $\boldsymbol{M}_{rx}$ incorporates the receiver I/Q imbalance and phase noise

$$\boldsymbol{M}_{rx}(t) = \frac{G_{RF}}{2}\begin{bmatrix} 1 & 0 \\ -g\sin[\varepsilon] & g\cos[\varepsilon] \end{bmatrix} \times \begin{bmatrix} \cos[\theta(t)] & -\sin[\theta(t)] \\ \sin[\theta(t)] & \cos[\theta(t)] \end{bmatrix},$$

which is simplified to

$$\boldsymbol{M}_{rx}(t) = \frac{G_{RF}}{2}\begin{bmatrix} \cos[\theta(t)] & -\sin[\theta(t)] \\ g\sin[\theta(t)-\varepsilon] & g\cos[\theta(t)-\varepsilon] \end{bmatrix}. \tag{3.7}$$

A factor of $\frac{1}{2}$ is present in the RF gain G_{RF}, since only the down-converted signal after the mixer passes through the filter, whereas the up-converted signal is filtered out.

3.4.2 Receiver Phase Noise and Jitter

There is a clear trade-off between power consumption and LO phase noise that has been discussed in literature [32, 33]. Therefore, in ultra-low-power receivers, the LO phase noise cannot be neglected.

Oscillator Phase Noise

Figure 3.6 shows a typical LO phase noise power spectral density (PSD). In the three regions I to III, different noise sources are dominant: in region I the LO-internal 1/f noise sources, in region II the LO-internal thermal noise sources, and in region III the LO-external thermal noise sources. The total phase noise contribution in region III is filtered by the receiver low-pass filters and can be neglected.

In the analysis of the impact of local oscillator phase noise on the SNR at the output of the FSK demodulator, not the phase noise itself but the change in phase noise over a time difference τ is of interest. The phase difference, defined as

$$\theta(\tau)|_{\tau=t_1-t_2} \stackrel{\text{def}}{=} \theta(t_1)-\theta(t_2),$$

is normally distributed ($\mathcal{N}$) with zero mean, and the variance is approximated by $\sigma_{pn}(\tau)^2$, see [34] and [35]; note that the variance depends on the time difference τ:

$$\begin{aligned}\theta(\tau) &\sim \mathcal{N}\left(0, \sigma_{pn}(\tau)^2\right)\\ \sigma_{pn}^2(\tau) &= C_{LO}\,|\tau| + K_{LO}\,\tau^2.\end{aligned} \tag{3.8}$$

The parameter K_{LO} accounts for internal 1/f noise (region I in figure 3.6), and the C_{LO} parameter for the white, thermal phase noise (region II in figure 3.6).

It is well known, see e.g. [34], that the PSD of thermally generated phase noise, region II in figure 3.6, can be written as

$$S_{\theta,white}(\omega) = \frac{C_{LO}}{\omega^2}, \tag{3.9}$$

which can be used to obtain C_{LO} from a phase noise measurement:

$$C_{LO} = \omega_{offset}^2 10^{\frac{\mathscr{L}(\omega_{offset})}{10}}, \tag{3.10}$$

where ω_{offset} is the frequency offset, relative to the center frequency ω_o, where the phase noise is measured. Additionally, the 1/f noise parameter K_{LO} is

$$K_{LO} = C_{LO}\,\omega_{1/f}\,\frac{1-\Gamma}{\pi},$$

where $\omega_{1/f}$ is the frequency at which the 1/f noise power is equal to the thermal noise power, and Γ is Euler's constant (≈ 0.5772).

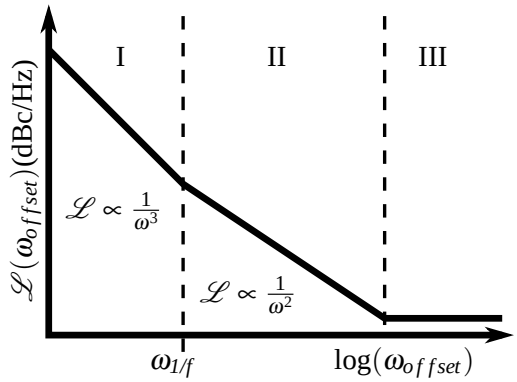


Figure 3.6: *Typical local oscillator phase noise power spectral density.*

Oscillator Jitter

The instantaneous oscillator period of the n-th cycle is

$$T[n] = T_0 + \Delta T[n],$$

where T_0 is the nominal period and $\Delta T[n]$ is the cycle-to-cycle jitter of period n. The absolute jitter is defined as the time difference between the n-th nominal zero crossing and the zero crossing corrupted by jitter:

$$T_{abs}[n] = \sum_{k=1}^{n} \Delta T[k],$$

and is a measure for long-term oscillator stability. Using equation (3.8) the absolute jitter variance can be related to the oscillator phase noise variance by equation

$$\sigma_{pn}^2 = \omega_o^2 \sigma_{abs}^2. \tag{3.11}$$

After rearranging (3.11), the absolute time jitter variance is given by a second order polynomial

$$\sigma_{abs}^2(\tau) = \frac{C_{LO}}{\omega_o^2}|\tau| + \frac{K_{LO}}{\omega_o^2}\tau^2, \tag{3.12}$$

which is similar to the model presented in [35]. In this thesis the parameters C_{LO} and K_{LO} are not normalized to the center frequency. The dependence of the variance on the period τ resembles the fact that the jitter is accumulated.

3.4.3 Limiter Discriminator Model

The complex amplitude of an FSK modulated signal does not contain any information. When the modulation index is larger than 0.5, the amplitude can be limited by a hard limiter. The output signal of the limiter is subsequently demodulated by a frequency discriminator, which returns the time derivative of the phase information. The transfer of the ideal limiter-discriminator is

$$LD[\boldsymbol{s}(t)] = \frac{\partial}{\partial t}\angle \boldsymbol{s}(t).$$

3.5 Effects of Receiver Imperfections on FSK BER

The receiver bit error rate increases with receiver impairments. Especially in low-power applications, the receiver impairments cannot be neglected. The receivers may have high noise figures and I/Q imbalance, since performance is traded for low power consumption. For example, there is a clear trade-off between the local oscillator power consumption and its phase noise [32, 33].

The performance of FSK modulation has been studied since the 1940's when modern communication systems came into use, see Rice [36–38], Blachman [39, 40] and Middleton [41]. The well-known FM threshold effect and click noise was studied in-depth in [38] and a simpler derivation was presented in [40]. Furthermore, a closed-form bit-error-rate (BER) including the inter-symbol-interference (ISI) effect was presented in [42, 43]. However, these works assumed high performance systems and did not take receiver imperfections into account; they only considered channel noise.

The influence of the phase noise on the click noise was studied in [44] and [45]. It was shown in [44] that phase noise does not influence the click noise in binary FSK modulation in practical cases. However, [45] showed that phase noise in combination with narrow baseband filters does have a small effect on the click noise. This is caused by the influence of the phase noise on the signal envelope. However, the effect is shown to be small. Therefore, we neglect the phase noise influence on the click noise process.

I/Q imbalance not only influences the susceptibility to interference in low-IF systems, see for example [46], but also lowers the signal-to-noise-ratio (SNR) and therefore deteriorates the BER. Additionally, practical receivers add noise in the signal paths and introduce LO phase noise.

Within this section the impact of receiver impairments on the output SNR and BER of an FSK limiter-discriminator demodulator are analyzed, both above and below the FM threshold. The closed-form analytical models can be used in an iterative design process, since the design space is very large and it is infeasible to simulate every possible parameter combination. Additionally the models are a means of gaining insight into the influences of the receiver impairments on its performance.

The limiter-discriminator demodulator is chosen since it is often used and easy to implement in practical receivers and can be designed to achieve near-optimal performance [47]. Additionally it was shown in [48] section II and [28] section 4.4.3 that the fixed-time-delay demodulator can be described by the same

equations as the limiter-discriminator demodulator. Moreover, since no information is present in the signal amplitude, the limiter-discriminator demodulator can be implemented using an energy-efficient 1-bit demodulator [49], or using low-power fixed-time-delay cells [28, 48]. The presented model gives insight into the impact of receiver impairments on the SNR, which can be used to make a trade-off between performance and power consumption and to obtain minimal circuit requirements for I/Q imbalance and phase noise. The model is compared against simulation results and shown to be in good agreement.

Within this thesis, we mainly focus on wideband FSK, since it has a larger FM modulation gain at the cost of bandwidth efficiency [29]. This trade-off benefits low-power receiver design. However, it is shown in section 3.5.2 that the obtained models also fit well for narrow-band FSK.

The FSK receiver model presented in section 3.4 is used throughout the SNR and BER analysis. Moreover, the I/Q imbalance, receiver generated noise and the phase noise model is presented. The signal-to-noise-ratio and bit error rate analysis is discussed in section 3.5.1. In this section, the SNR is obtained by applying the Wiener-Khinchin theorem to the autocorrelation of the demodulator output signal. Although the presented model assumes binary FSK modulation, it can be generalized to M-ary FSK modulation. All the analysis steps presented in section 3.5.1 still hold for M-ary FSK. However, the click noise and signal power become a function of the transmitted symbol. Therefore, the output SNR should be averaged over all the possible symbols. Additionally the BER analysis should be altered to include M-ary modulation. In section 3.5.2 the results of the analysis are presented, which are then used in section 3.6 to derive the WURx specifications.

3.5.1 Bit Error Rate Analysis

The SNR and BER of the FSK receiver with impairments given in section 3.4 is obtained by the following steps:

1. Obtain the relationship between the demodulated output signal and the received input signal.
2. Calculate the autocorrelation of the demodulated output.
3. Obtain the power spectral density (PSD) of the demodulated signal by taking the Fourier transform of the autocorrelation function using the Wiener-Khinchin theorem.
4. Model the click noise, which is the cause of the FM threshold effect.
5. Use the obtained PSD to calculate the SNR of the output signal.

6. The obtained output SNR is used to predict the receiver BER.

Throughout this section we assume a quasi-stationary modulation, as was done in [28], meaning that the modulated signal $\varphi(t)$ varies slowly compared to the deviation frequency. Using the quasi-stationary approximation, the frequency of the FSK modulated signal is considered to be constant within a bit period and therefore,

$$\begin{aligned} \varphi(t_0+\tau)-\varphi(t_0) &= \Delta\omega\ \tau \\ \dot{\varphi}(t) &= \Delta\omega \end{aligned}$$

In this section the noise sources are denoted by n_x, the signal vectors by $\boldsymbol{s_x}$, and the signal phases by α_x, where x is the name of the noise or signal source. The corresponding autocorrelations and power spectral densities are denoted by R_x and S_x respectively.

Demodulated Output Signal

The signal $\boldsymbol{s} = \begin{bmatrix} s_I \\ s_Q \end{bmatrix}$ at the output of the receiver front-end depicted in figure 3.5 is divided in a signal component corrupted by LO phase noise $\boldsymbol{s_r}$ and a receiver generated noise component $\boldsymbol{s_n}$ multiplied by the baseband gain G_{BB}:

$$\begin{aligned} \boldsymbol{s}(t) &= G_{BB}\left[\boldsymbol{s_r}(t)+\boldsymbol{s_n}(t)\right] \\ \boldsymbol{s_r}(t) &= \boldsymbol{M}_{rx}(t)\boldsymbol{r}(t) \\ \boldsymbol{s_n}(t) &= \underbrace{\boldsymbol{M}_{rx}(t)\boldsymbol{n}_{rf}(t)}_{\boldsymbol{s}_{nrf}} + \underbrace{\boldsymbol{n}_{bb}(t)}_{\boldsymbol{s}_{nbb}}. \end{aligned}$$

Since the baseband gain equally affects the noise and signal components, it can be neglected in the SNR calculations. Figure 3.7 graphically depicts the vector representation of the signal and noise components. The output of an ideal FSK demodulator is the rate of change of the received signal phase:

$$y(t) = \frac{\partial}{\partial t}\left(\alpha_r+\alpha_n\right). \tag{3.13}$$

The noise vector $\boldsymbol{s_n}$ can be divided in a part with the same orientation as the signal component (n_1) and a component perpendicular on the signal component

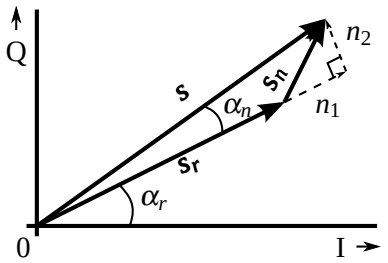


Figure 3.7: *Vector representation of the output signal of the receiver front-end.*

(n_2). These two components are

$$n_1 = \widehat{\boldsymbol{s_r}} \bullet \boldsymbol{s_n} \tag{3.14}$$

$$n_2 = \widehat{\boldsymbol{s_r}} \times \boldsymbol{s_n}, \tag{3.15}$$

where $\bullet$ is the dot-product, $\times$ represents the cross-product and $\widehat{\boldsymbol{x}}$ a unit vector. Assuming the noise component is smaller than the signal component, the noise induced phase shift α_n can be approximated by

$$\sin(\alpha_n) = \frac{n_2}{|\boldsymbol{s_r}|}$$

$$\alpha_n|_{|\boldsymbol{s_r}|>|\boldsymbol{s_n}|} \approx \frac{\boldsymbol{s_r} \times \boldsymbol{s}_n}{|\boldsymbol{s_r}|^2}, \tag{3.16}$$

where the squared signal vector length $|\boldsymbol{s_r}|^2$ is

$$|\boldsymbol{s_r}|^2 = A^2 \left(\frac{G_{RF}}{2}\right)^2 \Big\{ \cos^2[\varphi(t)+\theta(t)] + g^2 \sin^2[\varphi(t)+\theta(t)-\varepsilon] \Big\}.$$

The time derivative of the signal phase is

$$\frac{\partial}{\partial t} \angle \boldsymbol{s_r}(t) = \frac{\partial}{\partial t} \arctan\left(\frac{s_{r,Q}(t)}{s_{r,I}(t)}\right)$$

$$\frac{\partial}{\partial t} \angle \boldsymbol{s_r}(t) \approx \dot{\varphi}(t) + \dot{\theta}(t), \tag{3.17}$$

where the subscripts I and Q represent the in-phase and quadrature-phase components respectively. As was to be expected the signal component contains the demodulated signal $\dot{\varphi}(t)$ corrupted by the LO phase noise $\dot{\theta}(t)$.

There are two noise sources in the receiver, noise generated before (n_{rf}) and after (n_{bb}) the I/Q mixer. These two components are modulated by the FSK phase $\varphi(t)$ when they are passed through the non-linear limiter discriminator

$$\alpha_n \approx \frac{AG_{RF}^2}{4|\boldsymbol{s_r}|^2}\left\{g\cos(\varepsilon)\left[n_{rf,Q}\cos(\varphi)-n_{rf,I}\sin(\varphi)\right]+\right.$$
$$\left.\frac{2}{G_{RF}}\left[n_{bb,Q}\cos(\varphi+\theta)-g\,n_{bb,I}\sin(\varphi+\theta-\varepsilon)\right]\right\}. \tag{3.18}$$

The noise n_{rf} is affected by the I/Q imbalance in the same way as the signal component. Furthermore, the baseband noise contribution n_{bb} is divided by the receiver gain G_{RF}, which is in accordance with the Friis equation.

Autocorrelation

As was mentioned before, the noise sources are denoted by n_x, the signal vectors by $\boldsymbol{s_x}$, and the signal phases by α_x, where x is the name of the noise or signal source. The corresponding autocorrelations and power spectral densities are denoted by R_x and S_x respectively.

The time derivative of the phase of the receiver generated noise $\dot{\alpha}_n$ term on the right hand side of equation (3.13) is a linear combination of the time derivatives of the phase of two noise contributions: RF noise generated before the I/Q mixer α_{nrf} and baseband noise generated after the I/Q mixer α_{nbb}, see figure 3.5. Since the contributions are independent, their autocorrelation can be be obtained separately and then added together to obtain the total noise autocorrelation

$$R_{\dot{\alpha}_n}(\tau)=\frac{\partial^2}{\partial\tau^2}R_{\alpha_{nrf}}(\tau)+\frac{\partial^2}{\partial\tau^2}R_{\alpha_{nbb}}(\tau).$$

The FSK signal and RF noise source are independent processes and the FSK signal transfer function is linear. Thus the autocorrelation $R_{\alpha_{nrf}}(\tau)$ of the receiver output phase caused by the RF noise source n_{rf} is a product of the FSK-signal transfer function autocorrelation $R_g(\tau)$ and RF noise source autocorrelations $R_{nrf}(\tau)$:

$$R_{\alpha_{nrf}}(\tau)=\mathbf{E}\left\{\frac{\boldsymbol{s_r}(t_1)\times\boldsymbol{s}_{nrf}(t_1)}{|\boldsymbol{s_r}(t_1)|^2}\frac{\boldsymbol{s_r}(t_2)\times\boldsymbol{s}_{nrf}(t_2)}{|\boldsymbol{s_r}(t_2)|^2}\right\}$$
$$=R_g(\tau)R_{nrf}(\tau),$$

with $\tau = t_1 - t_2$. Using the quasi-stationary approximation the autocorrelation $R_g(\tau)$ is approximately

$$\begin{aligned} R_g(\tau) &= \frac{2(1+g^2)g\cos(\varepsilon)}{A^2} \frac{\cos(\Delta\omega\tau)}{(1+g^2)^2\sin^2(\Delta\omega\tau) + 4g^2\cos^2(\varepsilon)\cos^2(\Delta\omega\tau)} \\ &\approx \frac{1}{A^2}\frac{1+g^2}{2g\cos(\varepsilon)}\cos(\Delta\omega\ \tau)\,. \end{aligned} \tag{3.19}$$

In a similar manner the autocorrelation of the baseband noise is obtained as a product of the autocorrelations of the transfer function, baseband noise source and phase noise source:

$$\begin{aligned} R_{\alpha_{nbb}}(\tau) &= R_f(\tau)R_{nbb}(\tau)R_\theta(\tau) \\ R_f(\tau) &= \frac{4g\cos(\varepsilon)}{A^2\left(\frac{G_{RF}}{2}\right)^2} \frac{\cos(\Delta\omega\ \tau)}{(1+g^2)^2\sin^2(\Delta\omega\tau) + 4g^2\cos^2(\varepsilon)\cos^2(\Delta\omega\tau)} \\ &\approx \frac{1}{A^2\left(\frac{G_{RF}}{2}\right)^2}\frac{1}{g\cos(\varepsilon)}\cos(\Delta\omega\ \tau). \end{aligned} \tag{3.20}$$

Power Spectral Density

Using the Wiener-Khinchin theorem, the PSD can be obtained from the autocorrelation of the demodulator output

$$S_y(\omega) = \mathbf{F}\{R_{yy}(\tau)\}\,.$$

The output PSD can be evaluated in parts as was done for the autocorrelation of the demodulator output. Equations (3.21), (3.22) and (3.23) give the signal, RF noise and baseband noise PSD components respectively, where the notation $*$ is used to indicate the convolution operation:

$$S_y(\omega)|_{\boldsymbol{r}} = \omega^2\left[S_\varphi(\omega) + S_\theta(\omega)\right] \tag{3.21}$$

$$S_y(\omega)|_{\boldsymbol{n}_{rf}} = \frac{\omega^2}{2\pi}\left[S_g(\omega) * S_{nrf}(\omega)\right] \tag{3.22}$$

$$S_y(\omega)|_{\boldsymbol{n}_{bb}} = \frac{\omega^2}{(2\pi)^2}\left[S_f(\omega) * S_{nbb}(\omega) * S_\theta(\omega)\right]. \tag{3.23}$$

All the PSD components have a quadratic frequency shaping (ω^2), which is caused by the time derivative operation in the demodulator. This quadratic shaping was already observed and is the cause of the FSK modulation gain.

If the 1/f noise in the oscillator is neglected the phase noise contribution leads to a white white noise floor at the output of the demodulator, since the phase noise has the well known $1/\omega^2$ shape. The additional 1/f noise contribution leads to an increased noise floor near DC. Thus, when the receiver noise is absent, the phase-noise-induced noise floor will limit the maximal output SNR.

Assuming wideband FSK modulation, the noise PSD given by (3.23) can be simplified. In the wideband FSK case the phase noise bandwidth is much smaller than the receiver noise bandwidth. Therefore, the phase noise, although it modulates the whole baseband noise, only influences the "tail" of the baseband noise which falls outside the message bandwidth and therefore is filtered out. In this case the convolution $S_{nbb}(\omega) * S_\theta(\omega)$ can be approximated, see [28]

$$\frac{1}{2\pi}\int_{-\infty}^{\infty} S_{nbb}(\omega-\Omega)S_\theta(\Omega)d\Omega \approx S_{nbb}(\omega)\int_{-\infty}^{\infty}\frac{S_\theta(\Omega)}{2\pi}d\Omega. \tag{3.24}$$

The integral on the right-hand side equals one by definition[‡].

The PSDs of the two noise components are a function of the spectral densities of RF noise $S_{nrf}(\omega)$ and baseband noise $S_{nbb}(\omega)$, which are assumed to be white with a bandwidth B_{IF} caused by the brick-wall filter at the input of the demodulator:

$$S_{nrf}(\omega) = \frac{\pi\sigma_i^2}{B_{IF}}\,\mathrm{rect}\left(\frac{\omega}{2B_{IF}}\right)$$
$$S_{nbb}(\omega) = \frac{\pi\sigma_{rx}^2}{B_{IF}}\,\mathrm{rect}\left(\frac{\omega}{2B_{IF}}\right).$$

By applying the convolutions in the noise PSDs and using the autocorrelations given by (3.19) and (3.20), the output noise PSD before the integrate-and-dump filter of the noise generated before the I/Q mixer is:

$$S_y(\omega)|_{\boldsymbol{n}_{rf}} = \omega^2\frac{\pi\sigma_i^2}{2A^2B_{IF}}\frac{1+g^2}{2g\cos(\varepsilon)}\int_{-B_{IF}}^{B_{IF}}\left[\delta(\Delta\omega-\Omega+\omega)+\delta(\Delta\omega+\Omega-\omega)\right]d\Omega,$$

[‡]The phase-noise spectrum is defined relative to the carrier power and given in dBc/Hz. Thus the integrated spectral density should be one.

and the noise PSD caused by the noise after the I/Q imbalance is:

$$S_y(\omega)|_{\boldsymbol{n}_{bb}} = \omega^2 \frac{\pi\sigma_{rx}^2}{2A^2\left(\frac{G_{RF}}{2}\right)^2 B_{IF}} \frac{1}{g\cos(\varepsilon)} \times \int_{-B_{IF}}^{B_{IF}} [\delta(\Delta\omega - \Omega + \omega) + \delta(\Delta\omega + \Omega - \omega)]\, d\Omega .$$

Click Noise

At low CNR, below 13dB, the output SNR of the FSK demodulator decreases significantly. This is explained by the click noise phenomenon analyzed by Rice [38]. Clicks are introduced by the limiter in the demodulator. At low CNR's the noise vector $\boldsymbol{s_n}$ shown in figure 3.7 is of comparable length with the signal vector $\boldsymbol{s_r}$ and can introduce additional encirclements of the origin. Rice modeled the click noise as a train of delta functions with area $\pm 2\pi$ and the occurrence as a Poison process with rate N^+ (N^-) for positive (negative) clicks. Rice did not include false clicks, but it is shown in [50] that this effect can be neglected.

The effect of phase noise on the click noise was studied in [44] and [45]. Mazo [44] showed that for FSK modulation and practical values of phase noise the effect of phase noise on the click noise process can be neglected. The work in [45] showed that in the case of narrow-band FSK the phase noise has a small influence on the click noise, since the filter bandwidth is of the same order as the bit rate and the phase noise leads to a variance in the signal's envelope. The envelope variation does have a small effect on the click noise. However, within this thesis we mainly focus on wideband FSK and therefore neglect the influence of phase noise on the click noise process.

The demodulator output is filtered by an integrate and dump filter, which integrates the positive and negative clicks each with power $(2\pi)^2$ over a bit period $\frac{1}{R_b}$. Therefore, the click noise power at the output of the I&D filter is given by

$$P_{click} = (2\pi)^2 \left(N^+ - N^-\right) R_b.$$

From figure 3.7 it can be deduced that a positive click occurs when

$$|\boldsymbol{s_n}| > |\boldsymbol{s_r}| \tag{3.25}$$

$$\pi < \alpha_n \leq \pi + d(\alpha_n + \varphi) \tag{3.26}$$

$$\dot{\alpha}_n + \dot{\varphi} > 0 \tag{3.27}$$

and a negative click when

$$|\boldsymbol{s_n}| > |\boldsymbol{s_r}| \tag{3.28}$$

$$\pi > \alpha_n \geq \pi + d(\alpha_n + \varphi) \tag{3.29}$$

$$\dot{\alpha}_n + \dot{\varphi} < 0. \tag{3.30}$$

A good click noise model was obtained by Rice [38, 51]. The reported click rate as a function of the carrier to noise ratio ρ defined in (3.3) without I/Q mismatch and phase noise is

$$N = \left[\frac{\dot{\varphi}}{2\pi} + \frac{r\exp\{-a\rho\}I_0\{a\rho\}}{\sqrt{4\pi\rho}}\right]\exp\{-\rho\}\,, \tag{3.31}$$

in which r is the radius of gyration, as defined in [38] and [28],

$$r^2 = \left(\frac{1}{2\pi}\right)^2 \frac{\int_{-\infty}^{\infty}\omega^2 S_n(\omega)\,|H_{IF}(\omega)|^2\,d\omega}{\int_{-\infty}^{\infty} S_n(\omega)\,|H_{IF}(\omega)|^2\,d\omega}\,,$$

and a is defined as

$$a = -\frac{1}{2}\left(\frac{\dot{\varphi}}{r}\right)^2,$$

where $S_n(\omega)$ is the PSD of the noise. The receiver used in this chapter, depicted in figure 3.4, has a rectangular low pass IF filter with noise bandwidth B_{IF} and $r = \frac{B_{IF}}{\sqrt{3}}$. This click noise model can also be used for the presented receiver with I/Q imbalance, by incorporating the receiver imperfections in ρ.

In case there is an I/Q imbalance in the receiver, the vector length is also a function of the instantaneous signal phase $\varphi(t)$. However, the bit rate is much lower than the FSK frequency deviation. Therefore, the click rate is calculated with φ as parameter and then the average is taken over φ. The envelope of the noise vector is given by

$$|\boldsymbol{s_n}| = \sqrt{n_1^2 + n_2^2},$$

where n_1 and n_2 are the perpendicular noise components as given by (3.14) and (3.15) respectively. They are correlated zero-mean Gaussian processes with variances $\sigma_{n_1}^2$ and $\sigma_{n_2}^2$. The probability density function (pdf) of the envelope of two correlated Gaussian processes was given in [52]. However when the noise generated in the RF front-end is large enough, the correlation between the noise

components n_1 and n_2 can be neglected. Thus when the RF noise figure F_{RF} is larger than a few dB, both n_1 and n_2 are approximately two uncorrelated zero-mean Gaussian noise sources, and the pdf of the noise vector $|\boldsymbol{s_n}|$ can be approximated by the Rayleigh distribution with variance σ^2:

$$f_{|\boldsymbol{s_n}|}(z) \approx \frac{z}{\sigma^2} \exp\left(-\frac{z^2}{2\sigma^2}\right) U(z)$$
$$\sigma^2 \approx \frac{\sigma_{n_1}^2 + \sigma_{n_2}^2}{2}.$$

Using the approximation, the equivalent carrier to noise ratio including the I/Q gain imbalance and noise figure is

$$\rho_{nf} = \rho \frac{1}{(F_{BB}-1)\left(\frac{2}{G_{RF}}\right)^2 + F_{RF}\frac{1+g^2}{2}}. \tag{3.32}$$

Using the Rayleigh distribution, the probability with φ as parameter is obtained:

$$\mathscr{P}\left(\ |\boldsymbol{s_n}| > |\boldsymbol{s_r}| \ \middle|\ \varphi\right) = \exp\left\{-\rho_{nf}\left[\cos^2(\varphi) + g^2\sin^2(\varphi-\varepsilon)\right]\right\}. \tag{3.33}$$

The probability distribution approximation is compared against Matlab simulation results, as depicted in figure 3.8. In the Matlab simulation 200.000 noise samples were generated per φ value. Two cases were simulated: high I/Q imbalance, see figure 3.8a, and a practical receiver, see figure 3.8b. Only in the case of extremely high I/Q imbalance and low noise figure the correlation between n_1 and n_2 can not be neglected. However, in practical situations (3.33) holds. Figure 3.8 clearly shows the impact of I/Q imbalance on the click noise. Because of the I/Q imbalance, the signal trajectory in the I and Q space is no longer a circle but becomes more and more elliptic; therefore the vector length $|\boldsymbol{s_r}|$ varies with the FSK phase φ. At φ where the vector is very short, the probability $\mathscr{P}\left(|\boldsymbol{s_n}| > |\boldsymbol{s_r}| \ \middle|\ \varphi\right)$ increases leading to an increased click rate.

After substituting (3.32) in the Rice click rate model given by (3.31) and averaging over the phase φ, the average click noise power is approximated by

$$P_{click} \approx (2\pi)^2 R_b \frac{\dot{\varphi}}{2\pi} \exp\{-\rho_x\} I_0\{\rho_y\} \left[1 + \frac{\exp\{-a\rho_x\} I_0\{a\rho_x\}}{\sqrt{a\rho_x}}\right] \tag{3.34}$$

$$\rho_x = \rho_{nf}\frac{1+g^2\cos(\varepsilon)^2}{2}$$
$$\rho_y = \rho_{nf}\frac{g^2\cos(\varepsilon)^2 - 1}{2}.$$

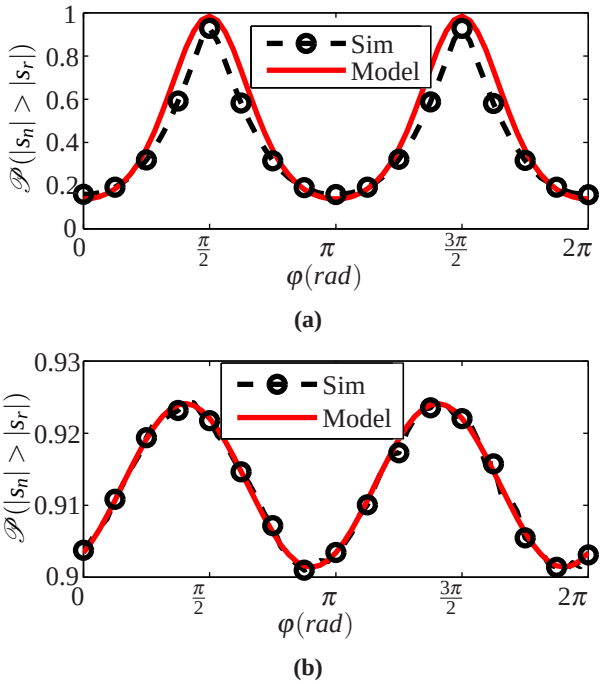


Figure 3.8: *Simulation and model results of* $\mathscr{P}\left(|\boldsymbol{s_n}| > |\boldsymbol{s_r}| \middle| \varphi\right)$ *for low CNR,* $G_{RF} = 2$, $F_{RF} = 0dB$ *and* $\rho = 0dB$. *(a) The results for large I/Q imbalance:* $g = 0.1$, $\varepsilon = 25\,\text{deg}$ *and* $F_{BB} = 0dB$ *(b) The results for practical I/Q imbalance:* $g = 0.9$, $\varepsilon = 5\,\text{deg}$ *and* $F_{BB} = 10dB$

SNR

The noise power consists of four contributions: the local oscillator phase noise, RF noise generated before the I/Q mixer, baseband noise generated after the I/Q mixer and the click noise contribution. Each contribution can be obtained by substituting the PSDs given by (3.21) to (3.23) in (3.35), where $H_{I\&D}(\omega)$ is the integrate-and-dump filter at the output of the demodulator:

$$P_x = \frac{1}{2\pi}\int_{-\infty}^{\infty} S_y(\omega)|_x |H_{I\&D}(\omega)|^2 \, d\omega. \tag{3.35}$$

By substituting the RF noise PSD $S_{nrf}(\omega)$ and the Fourier transform $\mathbf{F}\{R_g(\tau)\}$

in (3.35), the RF noise power integral is obtained:

$$\begin{aligned}P_{RF} =& \frac{\sigma_{rf}^2}{4A^2 B_{IF}} \frac{1+g^2}{2g\cos(\varepsilon)} \\ & \int_{-B_{IF}}^{B_{IF}} \int_{-\infty}^{\infty} \omega^2 \left|H_{I\&D}(\omega)\right|^2 \left[\delta(\Delta\omega - \Omega + \omega) + \delta(\Delta\omega + \Omega - \omega)\right] d\omega d\Omega \\ =& \frac{F_{RF}}{8\rho B_{IF}} \frac{1+g^2}{2g\cos(\varepsilon)} \times \\ & \int_{-B_{IF}}^{B_{IF}} \left[(\Omega - \Delta\omega)^2 \left|H_{I\&D}(\Omega - \Delta\omega)\right|^2 + (\Omega + \Delta\omega)^2 \left|H_{I\&D}(\Omega + \Delta\omega)\right|^2\right] d\Omega .\end{aligned}$$

Solving the integral and using the fact that $\omega^2 \left|H_{I\&D}(\omega)\right|^2$ is an even function, the RF noise contribution after the I&D filter is

$$\begin{aligned}P_{RF} &= \frac{F_{RF}}{4\rho B_{IF}} \frac{1+g^2}{2g\cos(\varepsilon)} \int_{-B_{IF}+\Delta\omega}^{B_{IF}+\Delta\omega} \gamma^2 \left|H_{I\&D}(\gamma)\right|^2 d\gamma \\ &= \frac{R_b^2 F_{RF}}{\rho} \frac{1+g^2}{2g\cos(\varepsilon)} \left[1 - \frac{\Delta\omega}{B_{IF}} \operatorname{sinc}\left(\frac{2\Delta\omega}{R_b}\right)\right] . \end{aligned} \tag{3.36}$$

For wideband FSK the sinc term can be neglected and the RF noise contribution becomes

$$P_{RF} \approx \frac{R_b^2}{\rho} F_{RF} \frac{1+g^2}{2g\cos(\varepsilon)} .$$

In a similar way the baseband noise contribution is obtained:

$$\begin{aligned}P_{BB} &= \frac{R_b^2}{\rho} \frac{F_{BB} - 1}{\left(\frac{G_{RF}}{2}\right)^2} \frac{1}{g\cos(\varepsilon)} \left[1 - \frac{\Delta\omega}{B_{IF}} \operatorname{sinc}\left(\frac{2\Delta\omega}{R_b}\right)\right] \\ &\approx \frac{R_b^2}{\rho} \frac{F_{BB} - 1}{\left(\frac{G_{RF}}{2}\right)^2} \frac{1}{g\cos(\varepsilon)} , \end{aligned} \tag{3.37}$$

where the receiver noise variance given by (3.5) is used.

Using the definitions of the phase noise variance σ_{pn}^2 in [34] the phase noise power after the I&D filter is

$$\begin{aligned}P_{\dot{\theta}} &= \frac{1}{T_b^2} \sigma_{pn}^2(T_b) \\ &= R_b C_{LO} + K_{LO} . \end{aligned} \tag{3.38}$$

The signal power is

$$\begin{aligned} P_s &= \frac{1}{T_b}\int_0^{T_b} |\dot{\varphi}(\tau)|^2 \, d\tau \\ &= \Delta\omega^2, \end{aligned} \tag{3.39}$$

using the quasi-stationary approach and assuming the FSK signal $\dot{\varphi}(t)$ passes through the filter.

Combining the signal power and all the noise power contributions the SNR is

$$SNR = \frac{P_s}{P_{RF} + P_{BB} + P_{\dot{\theta}} + P_{click}}. \tag{3.40}$$

Bit Error Rate

The limiter-discriminator demodulator shown in figure 3.4 converts the FSK modulated input signal to an OOK modulated output signal. Therefore, the bit error rate of the received signal can be calculated in a similar manner as the BER of an OOK signal with a SNR given by (3.40). Contrary to the narrow-band case presented in [42], the received wideband-FSK signal $\boldsymbol{s}(t)$ depicted in figure 3.7 encircles the origin $\frac{h}{2}$ times per received bit. Consequently, a few FM clicks do not necessarily lead to a bit error when the modulation index is high. Therefore, the click noise power after the integrate-and-dump filter is added to the power of the other noise sources.

The output amplitude $y(t)$ of the FSK demodulator has a normal distribution $\mathcal{N}\left(\mu, \sigma^2\right)$ with mean

$$\mu = \pm\Delta\omega$$

for a transmitted '0' and '1', variance

$$\sigma^2 = P_{RF} + P_{BB} + P_{\dot{\theta}} + P_{click},$$

and probability density function

$$f_y(x|\,\mu) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left\{-\frac{(x-\mu)^2}{2\sigma^2}\right\}.$$

Analogous to OOK demodulation, the receiver decides whether a '0' or '1' is transmitted by comparing the received signal with a threshold level. Assuming

the 50% of the transmitted data is '0' and 50% is '1' the optimal threshold value is 0. Subsequently, the BER is given by

$$BER = \frac{1}{2}\int_{-\infty}^{0} f_y(x|\Delta\omega)\,dx + \frac{1}{2}\int_{0}^{\infty} f_y(x|-\Delta\omega)\,dx.$$

The BER can be rewritten as

$$BER = \frac{1}{2}\,\mathrm{Erfc}\left\{\sqrt{\frac{SNR}{2}}\right\}, \tag{3.41}$$

where SNR is the signal-to-noise ratio at the output of the integrate-and-dump filter given by (3.40), see [29]. The complementary error function is

$$\mathrm{Erfc}\{z\} \overset{\text{def}}{=} \frac{2}{\sqrt{\pi}}\int_{x}^{\infty} e^{-x^2}dx.$$

3.5.2 Simulation and Model Results

In the previous sections we have studied three effects of a non-ideal receiver on the performance of FSK modulation: receiver generated noise both in RF and baseband, I/Q imbalance and phase noise. In this section the model is compared against simulation results.

Simulation setup

The Matlab simulation was an implementation of equations (3.6) and (3.7). Per simulation 1.900 million samples of the noise sources n_{rf}, n_{bb} and θ were generated, and the SNR and BER were simulated for various values of the receiver parameters g, ε and G_{RF}. The simplified pseudo-code of the Matlab script is given in appendix C.

Signal to noise ratio model

A typical example of the SNR as a function of the input carrier to noise ratio is depicted in figure 3.9. From the figure it is clear that there are three regions, labeled I to III.

Between regions I and II the FM threshold is visible. Below the threshold, in region I, the click noise is the dominant noise source, see figure 3.9b, and the

output SNR is severely degraded. Above the threshold the click noise can be neglected. In region III the phase noise dominates the output noise power and the channel and receiver noise contributions can be neglected. Therefore, the output SNR flattens and an improvement in input CNR is no longer beneficial.

Figure 3.10a shows the simulation and model results of the output SNR for different bit rates and modulation indices, but equal frequency deviation. It is clear that the FSK modulation gain increases for smaller bit rates, which shows a trade-off between bandwidth efficiency and modulation gain.

Unless otherwise stated, the bit rate used for the simulations is 10kbps and the FSK frequency deviation is 250kHz. With this frequency deviation the signal fits within the largest band in the 915MHz (USA) / 868MHz (Europe) ISM band. Additionally, unless otherwise specified, the receiver parameters are: $G_{RF} = 10$(dB), $N_{RF} = 5$(dB), $N_{BB} = 20$(dB) and $\mathscr{L}(1MHz) = -130$(dBc/Hz), which are practical numbers.

As said, below the FM threshold, region I in figure 3.9, the click noise is dominant, whereas above the FM threshold, regions II and III in figure 3.9, the click noise can be neglected. We will study the regions above and below the threshold separately, because the results are very different.

Above Threshold Above the FM threshold the click noise can be neglected, which eases the analysis of the receiver impairments. Firstly, we will study the effect of the receiver generated noise and assume there is no I/Q imbalance and

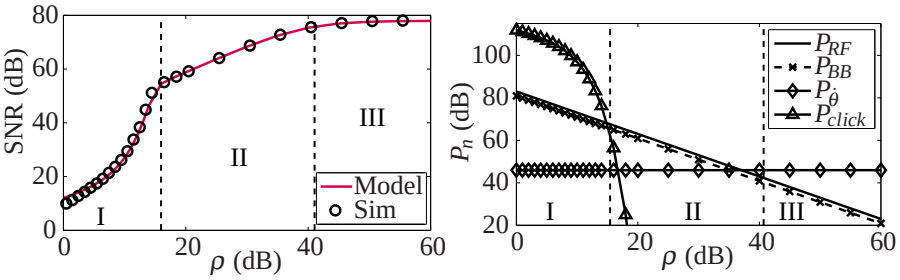


Figure 3.9: *(a) Output SNR as function of the carrier to noise ratio ρ, with: $\Delta f = 250$(kHz), $R_b = 10$(kbps), $G_{RF} = 10$(dB), $g = 1$, $\varepsilon = 0$ deg, $F_{RF} = 3$(dB), $F_{BB} = 15$(dB) and $\mathscr{L}(1MHz) = -130$(dBc/Hz) (b) Modeled output noise used in equation (3.40).*

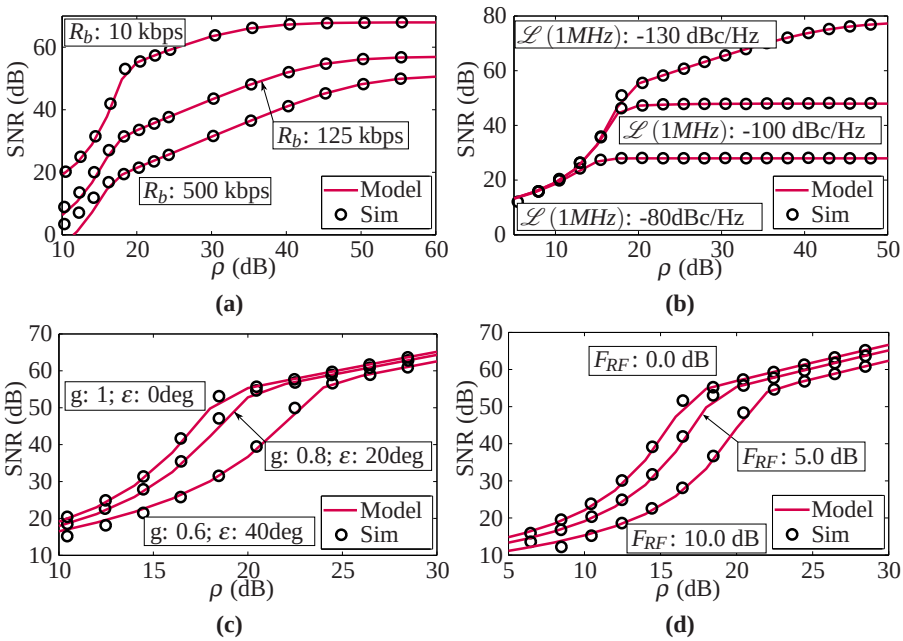


Figure 3.10: *Simulated and modeled output SNR as function of input carrier-to-noise-ratio ρ. (a) Shows results for different bit rates and constant frequency deviation. (b) Shows the implications of LO phase noise without I/Q imbalance, i.e. $g = 1$, $\varepsilon = 0\,\text{deg}$. As can be seen, the LO phase noise limits the maximal output SNR. (c) The FM-threshold shifts towards higher ρ when the I/Q imbalance increases. (d) The RF noise factor F_{RF} degrades the carrier-to-noise-ratio linearly and shifts the FM-threshold towards higher ρ.*

phase noise. In this situation the SNR is simplified to

$$SNR_F = \frac{\rho \Delta\omega^2}{R_b^2} \frac{1}{F_{tot}}, \tag{3.42}$$

where F_{tot} is the receiver noise factor described in section 3.4.1:

$$F_{tot} = F_{RF} + \frac{F_{BB} - 1}{\left(\frac{G_{RF}}{2}\right)^2}.$$

The noise factor F_{tot} could also be obtained using Friis' formula.

The effect is as would be expected; the noise factor reduces the carrier to noise ratio ρ. It becomes more interesting when also the I/Q imbalance is taken into

account:

$$SNR_{F,IQ} = \frac{\rho\Delta\omega^2}{R_b^2}\frac{1}{F_{eff}} \tag{3.43}$$
$$F_{eff} = \frac{1}{g\cos(\varepsilon)}\left(F_{RF}\frac{1+g^2}{2} + \frac{F_{BB}-1}{\left(\frac{G_{RF}}{2}\right)^2}\right).$$

Effectively, the receiver noise factor is increased by the I/Q imbalance. The I/Q imbalance has a larger influence on the noise generated after the mixer (F_{BB}) than before the I/Q mixer (F_{RF}). The factor $\frac{1+g^2}{2}$ can be regarded as the effective power gain for the noise generated before the I/Q mixer. Additionally, the factor $g\cos(\varepsilon)$ can be thought of as the "decorrelation" factor between the noise in the I and Q paths. When the factor is 1 the noise in both paths is completely uncorrelated and when the factor is 0 both paths are completely correlated. The simulation results for three different gain and phase errors are shown in figure 3.10c. It is clear that above the FM threshold the output SNR only slightly varies. The degradation is much smaller than the SNR degradation caused by the receiver noise factor. Thus, FSK receivers are robust against I/Q imbalance, implying that FSK is a good candidate for energy-restricted systems.

The SNR with the phase noise included is

$$SNR_{F,IQ,PN} = \frac{\Delta\omega^2}{\frac{R_b^2}{\rho}F_{eff} + (R_bC_{LO} + K_{LO})}. \tag{3.44}$$

It can be seen that the phase noise adds a white noise floor, see region III in figure 3.9; for very high input carrier to noise ratio ρ the SNR saturates. The maximal SNR,

$$\max\{SNR_{F,IQ,PN}\} = \frac{\Delta\omega^2}{R_bC_{LO} + K_{LO}}, \tag{3.45}$$

shows, as expected, that the receiver becomes less susceptible to phase noise when the deviation frequency $\Delta\omega$ increases. Thus, the LO phase noise can be increased, and the power consumption decreased at the cost of higher frequency deviation and therefore lower spectral efficiency.

Below Threshold Below the FM threshold, region I in figure 3.9, the click noise dominates the noise power. Therefore, we will only study the effects of the

receiver impairments on the click noise in this section. The click noise model was discussed in section 3.5.1.

From the approximation for the click noise given in (3.34) it appears that the phase noise does not have an influence on the click noise and the FM threshold. This is in agreement with the simulation result depicted in figure 3.10b and the work presented in [44].

However, the I/Q imbalance deteriorates the output SNR below the FM threshold, as can be seen in figure 3.10c. This is in contrast to the situation above the FM threshold. Again, the model is reasonably accurate except for very low ρ where the click noise model presented in [38] does not hold anymore.

The third receiver impairment studied, the noise figure, shifts the FM threshold to higher carrier to noise ratios, see figure 3.10d.

SNR Model Accuracy

The accuracy of the SNR model is analyzed by calculating the average relative error (ARE),

$$ARE = \frac{1}{M}\sum_{n=1}^{M}\frac{|SNR_{mod} - SNR_{sim,n}|}{|SNR_{sim,n}|},$$

where M is the number of simulation results, for different CNR. The model is more accurate for high input CNR ρ than for low CNR. Therefore the relative error decreases when higher CNR are taken into account. Since the required BER usually is below 10^{-3} this is taken as a lower bound on the input CNR. The upper bound on CNR is taken to be 70dB; higher values will only decrease the ARE.

The average relative error for various gain and phase imbalances is shown in figure 3.11a. In subfigure (a) the ARE is shown as function of I/Q imbalance and in (b) as a function of phase noise and bit rate. In both cases the ARE is shown for input CNRs such that the BER $< 10^{-3}$ or $< 10^{-5}$. It can be seen that the SNR model presented in this section in in agreement with the simulation results, and that the model gets more accurate for lower BER. The error increases as the I/Q imbalance increases, but is still sufficiently low to get an impression on the influence of the I/Q imbalance on the output SNR.

The ARE for different phase noise, bit rates and therefore modulation indices is shown in figure 3.11b. Although we used three assumptions based on wideband FSK:

- neglect the modulation of baseband noise by phase noise (3.24);
- neglect the phase noise effect on click noise;
- neglect the sinc part in (3.36) and (3.37);

their effect indeed also turns out to be very small for low modulation indices and hence can be neglected, which validates our assumptions.

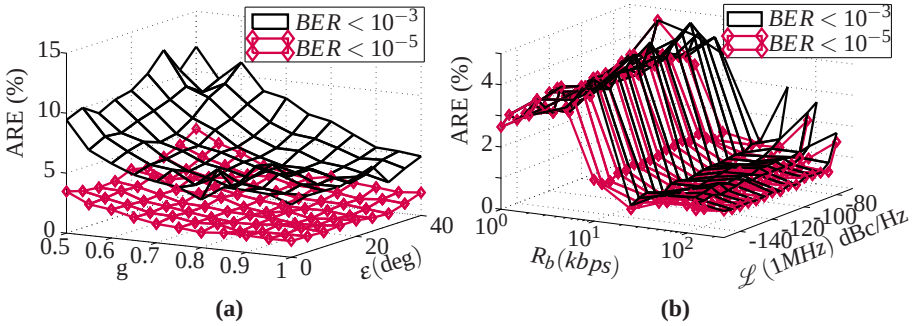


Figure 3.11: *Average relative error of the SNR model for carrier to noise ratios such that: BER* $< 10^{-3}$ *and* $< 10^{-5}$ *(a) as function of I/Q imbalance. (b) as function of phase noise and bit rate.*

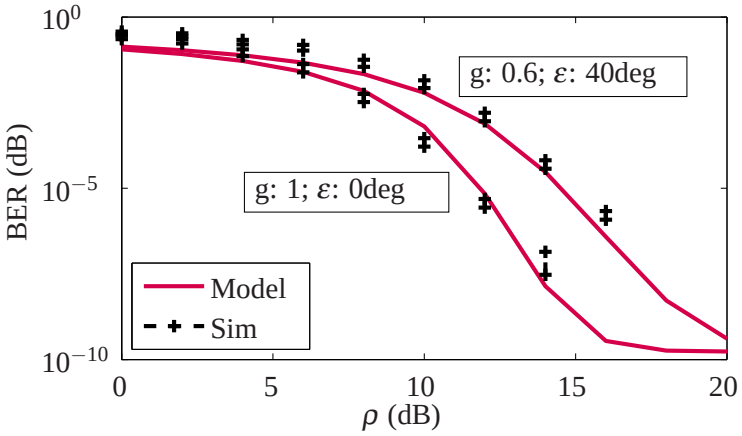


Figure 3.12: *Modeled and simulated bit error rate for a receiver with high I/Q imbalance and a receiver without I/Q imbalance, with:* $\Delta f = 250(kHz)$, $R_b = 50(kbps)$, $G_{RF} = 10(dB)$, $F_{RF} = 5(dB)$, $F_{BB} = 20(dB)$ *and* $\mathscr{L}(1MHz) = -75(dBc/Hz)$.

Bit error rate model

The effect of the I/Q imbalance on the BER is depicted in figure 3.12, where the length of the simulated lines give the 90% confidence interval. It is infeasible to simulate BER for even higher input CNR(ρ), since the simulation time would increase exponentially. The effective input CNR degrades by approximately 3dB when the I/Q imbalance is very high, $g = 0.6$ and $\varepsilon = 40\,\text{deg}$. Additionally, it is shown that the presented BER model is accurate enough to predict the effects of receiver impairments.

3.6 Wake-up Receiver Specifications

The main design goal of the wake-up receiver is low power consumption, while maintaining a BER below 0.1%. In this section the required sensitivity and noise figure is calculated in section 3.6.2. Additionally, the maximally allowed phase noise is important since the required phase noise is proportional to the local oscillator power consumption as will be discussed in section 4.2. The maximal allowed phase noise is given in section 3.6.3.

3.6.1 Interferer robustness

There is a clear trade-off between linearity, needed for a high interferer robustness, and power consumption. To greatly reduce the power consumption, the interference robustness needs to be sacrificed. There are two different interferer scenarios: in-band and out-of-band interferers. The out-of-band interferers are partly rejected by the filtering operation of the zero-IF architecture. This would not have been the case in an envelope-based OOK receiver. In such a receiver an external filter, for example a BAW or SAW is needed. To cope with the in-band interferers we partly rely on the inherent linearity of the mixer-first architecture. Additionally, we assume that the master node implements a form of interference avoidance, for example by means of carrier sensing. However, this is beyond the scope of this thesis and requires additional research.

3.6.2 Sensitivity and Noise Figure

In chapter 2 it was derived that a transmission distance of 10m and a bit rate of 125kbps is enough for most WBAN applications. Given a modulation index of 2

the frequency deviation is 250kHz and the signal bandwidth BW is 1MHz. Using the free-space path loss (FSPL) model and carrier frequency f_c of 915MHz the path loss is calculated to be 51.7dB using

$$FSPL = 20\log_{10}\left(\frac{4\pi d\, f_c}{c}\right),$$

where the transmission distance and speed of light are given by d and c respectively. Combining the path loss, and 10dB link margin transmit power P_{TX} of -10dBm, the sensitivity P_{sens} should be better than -72dBm.

The received carrier-to-noise-ratio is obtained using

$$\rho = P_{sens} - 10\log_{10}(k_B T) - 10\log_{10}(BW),$$

given an omnidirectional antenna, thus an antenna gain of 0dBi. The received CNR is 42dB assuming room temperature.

After substituting the required BER of 0.1% in equation (3.41) the required demodulator output SNR (SNR_o) is calculated to be be 9.8dB. Additionally, the local oscillator is designed such that its phase noise is not a limiting factor at a BER of 0.1% and the gain and phase errors are taken to be 20% and 20 degrees as a safety margin. Using the SNR model presented in 3.5.1, the maximally allowed noise figure is 40dB. However, some margin should be taken into account when designing the receiver.

3.6.3 Phase Noise

As was discussed in section 3.5.2 the phase noise adds a BER floor; no matter how high the input CNR is, the BER will never be lower than this BER floor. Using equation (3.45) and ignoring the 1/f noise the maximal thermally induced phase noise parameter is obtained

$$C_{LO} < \frac{\Delta\omega^2}{R_b \max\{SNR\}}.$$

The phase noise at a frequency offset of 1MHz is calculated using 3.10,

$$\mathscr{L}(\omega_{offset}) = 10\log_{10}\left(\frac{C_{LO}}{\omega_{offset}^2}\right).$$

Tolerating a BER floor of 0.001%, the maximum demodulator output SNR is calculated using (3.41) to be 12.6dB, leading to a maximal phase noise requirement of $\mathscr{L}(1MHz) < -75.6$ dBc/Hz assuming a deviation frequency of 1MHz and bit rate of 50kbps.

3.7 Conclusion

In this chapter the system level design of the low-power wake-up receiver was discussed. From the modulation complexity and state-of-the-art literature study it was derived that either OOK or FSK modulation lends itself well for low-power receivers. When using wideband-FSK modulation in combination with a zero-IF receiver most signal power is concentrated around the deviation frequency instead of DC. Therefore, a high pass filter can be used to remove the DC-offset and 1/f noise in the baseband stage.

Additionally SNR and BER models have been presented and shown to be accurate both above and below the FM threshold. Besides the wideband-FSK case, the models also work well for non-wideband FSK modulation. The presented model is very useful in defining the minimally required receiver specifications as was done in section 3.6. It facilitates the design of a low-power receiver. Moreover, the model can be used when making a decision on the trade-off between transceiver performance and power consumption.

The I/Q imbalance increases the effective receiver noise figure, and has a larger influence on the IF noise than on the RF noise. Additionally, it mainly deteriorates the SNR and BER below the FM threshold. The receiver noise figure has the same effect as was given by Friis' noise equation, and deteriorates the performance for all values of input carrier-to-noise ratio. On the other hand the phase noise only influences the output SNR and BER for very high input carrier-to-noise ratios. It effectively adds a noise floor at the output of the modulator and saturates the output SNR. The noise floor can be decreased by increasing the frequency deviation. Hence a trade-off between spectral efficiency and LO phase noise, and indirectly LO power consumption, is shown to exist.

CHAPTER 4

LOW-POWER ZERO-IF RECEIVER DESIGN

In the previous chapter, the system-level design choices were analyzed. In this chapter the circuit-level design choices and circuit optimizations are studied given the system-level boundary conditions, whereas the actual circuit implementations and measurement results will be presented in chapters 5 and 6.

In a short-range sensor network the receiver sensitivity is allowed to be relatively low, as has been discussed in section 3.6.2. Therefore, the network will still operate when the receiver has a high noise figure of up to 40dB. To save power the high frequency RF LNA can be replaced by a low-power gain stage in the low-frequency baseband domain. This makes the mixer the first stage in the receiver and therefore the input RF port needs to be matched to the off-chip antenna. In section 4.1, the mixer input impedance, conversion power gain and noise figure are modeled. Additionally the optimal mixer-first design procedure is given.

Also, the local frequency reference in a receiver usually consumes a lot of power. By increasing the modulation index of the wideband-FSK modulation, the phase noise requirement can be reduced considerably, see sections 3.5.2 and 3.6.3. The reduced phase noise requirement is exploited in section 4.2 to reduce the power consumption of the local oscillator. Moreover it is shown that for the same high phase noise value, ring oscillators consume less power than LC oscillators, because of technology limitations.

Besides the phase noise also the frequency stability of the local oscillator is important. Therefore, most FSK receivers use power consuming phase-locked-loops (PLL) [9]. Receivers using injection-locking [14] are less power hungry but more sensitive to blockers. To overcome these challenges, an on-chip FSK demodulator (section 4.3) is used to measure the frequency offset between the received signal and the local frequency reference. The measured frequency offset is fed-back to the local oscillator inside the automatic frequency control (AFC) loop. In section 4.4 the stability and performance of the AFC loop is studied.

4.1 Passive Mixer-First Design

By omitting the LNA from the receiver chain, the mixer becomes the first sub-circuit, and is therefore directly connected to the antenna. A disadvantage is the reduced isolation from the oscillator to the antenna. However, in low-power sensor nodes the oscillator is also low-power and the isolation of the passive mixer is good enough; in the second WURx described in chapter 6 the oscillator signal power measured at the antenna input was below the noise floor of the measurement equipment.

Since it is the first sub-circuit, its available power gain has a big influence on the overall noise figure, according to Friis' noise figure equation. A passive voltage domain mixer topology is chosen instead of a Gilbert cell mixer, for its low 1/f noise and power consumption and its high linearity.

Since the available power gain of a passive mixer can not be higher than 0dB, also the available power gain of the following amplifier and the matching between the mixer and baseband amplifier are important. Taking the mixer output matching into account, the design goal is to maximize the transducer power gain.

In this section an analytical model for the passive mixer input impedance, conversion voltage and power gain and noise figure is presented. The model is valid for both voltage domain and current domain mixers. This is different from the analysis presented in [53] in which an infinite load impedance is assumed and the transducer power gain is not analyzed. The presented model is used to design a passive mixer with maximal transducer power gain. Firstly, the time-domain mixer model is discussed, which is subsequently used to model the voltage conversion gain, input impedance and transducer power gain. Finally, these analytical models are used to come to an optimal mixer design.

4.1.1 Time-Domain Passive Mixer Model

Figure 4.1 shows an equivalent circuit model of the four phase passive quadrature mixer. The mixing transistors are modeled by switches with an on-resistance r_{sw}.

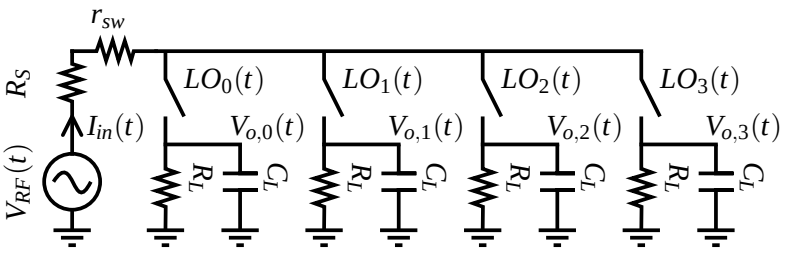


Figure 4.1: *Simplified schematic of the I and Q mixer, where the transistors are modeled as switches with resistance r_{sw}.*

There is a trade-off between the switch on-resistance

$$r_{sw} \propto \frac{L}{W}, \tag{4.1}$$

and the LO power P_{LO} needed to drive the switch gate capacitance

$$C_{switch} \propto WL. \tag{4.2}$$

As shown in the above equations, when the transistor width W, the resistance decreases and the switch gate capacitance increases. It is clear that the length L should be minimized for both the on-resistance as well as the LO power consumption.

The mixer load R_L and C_L include the input impedance of the next stage. Furthermore, the RF input signal source is modeled by a voltage source

$$V_{RF}(t) = A_{RF}\cos(\omega_c t + \varphi),$$

and series resistance R_S. At the carrier frequency, the signal input comprises both the external signal source and optional matching circuit. The phase of the RF signal is represented by φ, which can contain phase or frequency modulation and thus φ can be time dependent. Since the modulation bandwidth is much smaller than the carrier frequency ω_c, it is assumed that the RF carrier frequency is equal to the LO frequency with period $T_c = \frac{2\pi}{\omega_c}$, and φ is constant during one RF carrier cycle. The in-phase (I) and quadrature-phase (Q) differential output signals are $V_{o,0}(t) - V_{o,2}(t)$ and $V_{o,1}(t) - V_{o,3}(t)$, respectively.

Besides the circuit elements, also the LO duty cycle has a big influence on the mixer gain and input impedance. The duty cycle η is specified as a percentage of the LO-cycle during which a single switch is closed. The duty cycle has to be lower than 50% since otherwise the differential output paths are shorted every cycle, reducing the output voltage and conversion gain. On the other hand, the duty cycle should be larger than 25%. Otherwise, the RF input is not connected to one of the outputs during some time and the input impedance will have large peaks during each LO period.

The four corresponding local oscillator phases given by $LO_n(t)$ are depicted for both 25% and 50% duty-cycle schemes in figure 4.2. To avoid I/Q cross-talk, none of the LO signal phases should overlap each other, leading to a 25% duty cycle scheme, see [54]. Within this chapter the source and switch resistances

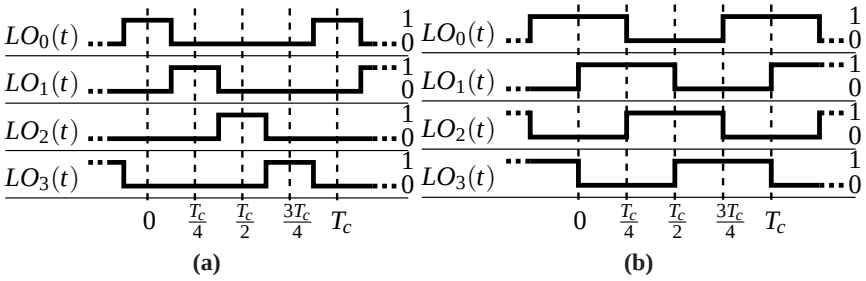


Figure 4.2: *In-phase $LO_{0,2}(t)$ and quadrature phase $LO_{1,3}(t)$ local oscillator phases, where the LO period is given by T_c for two different duty cycles: a) 25% b) 50%.*

are combined $(r_{on} = R_S + r_{sw})$, which holds when there is no overlap current between the in-phase and quadrature-phase outputs. This is the case when either there is no LO overlap or the switch resistance r_{sw} is large compared to the source resistance R_S.

The switch turn-on time moment of LO phase n is

$$T_{on,n} = \frac{T_c}{2}\left(\frac{n}{2} - \eta\right),$$

and turn-off time instance is

$$T_{off,n} = \frac{T_c}{2}\left(\frac{n}{2} + \eta\right),$$

where η is the duty cycle.

Each of the four output phases are modeled by two time-domain differential equations: one for the on-state and one for the off-state. In the on-state the

switch is closed and the differential equation is:

$$[V_{RF}(t) - V_{o,n}(t)]\frac{1}{r_{on}} = V_{o,n}(t)\frac{1}{R_L} + C_L\frac{\partial}{\partial t}V_{o,n}(t). \tag{4.3}$$

When the switch is opened, the equation becomes

$$0 = V_{o,n}(t)\frac{1}{R_L} + C_L\frac{\partial}{\partial t}V_{o,n}(t). \tag{4.4}$$

The differential equations can be solved separately, assuming the mixer is in the steady state, and there is no overlap current, while taking into account the boundary conditions between the switch on and off states. In the on-state the output voltage is

$$V_{o,n}(t) = A_c\left[A_{on,n}\exp\left\{-\frac{t - T_{on,n}}{\tau_{on}}\right\} + \cos(\omega_c t + \phi - \theta)\right],$$

and in the off-state the output voltage is

$$V_{o,n}(t) = A_c A_{off,n}\exp\left\{-\frac{t - T_{off,n}}{\tau_{off}}\right\},$$

where A_c denotes the RF output amplitude and the factors $A_{on,n}$ and $A_{off,n}$ are used to represent the boundary conditions originating from the memory effect caused by the load capacitances. The corresponding mixer time constants for both states are

$$\tau_{off} = R_L C_L$$
$$\tau_{on} = \frac{r_{on}R_L}{r_{on} + R_L}C_L\,.$$

It will be shown in later sections that the mixer power gain and input impedance can be described by just three input parameters: normalized on-state RC time constant

$$\tau'_{on} = \omega_c \tau_{on}\,, \tag{4.5}$$

normalized load impedance

$$R'_L = \frac{R_L}{r_{on}}\,,$$

and switch resistance r_{sw}. All the other constants can be written as functions of these three parameters. In particular the normalized off-state RC time constant

$$\tau'_{off} = \tau'_{on}\left(1+R'_L\right).$$

The constants $A_{on,n}$ and $A_{off,n}$ are obtained by solving the boundary conditions at the turn-on and turn-off instants:

$$V_{o,n}(T_{on,n})\big|_{on} = V_{o,n}(T_c+T_{on,n})\big|_{off}$$
$$V_{o,n}(T_{off,n})\big|_{on} = V_{o,n}(T_{off,n})\big|_{off}.$$

After solving the boundary conditions, the constants are

$$A_{on,n} = \frac{\cos([\tfrac{n}{2}+\eta]\pi+\varphi-\theta)C_{off} - \cos([\tfrac{n}{2}-\eta]\pi+\varphi-\theta)}{1-C_{on}C_{off}}$$
$$A_{off,n} = \frac{\cos([\tfrac{n}{2}+\eta]\pi+\varphi-\theta) - \cos([\tfrac{n}{2}-\eta]\pi+\varphi-\theta)C_{on}}{1-C_{on}C_{off}},$$

where

$$C_{on} = \exp\left\{-\frac{2\eta\pi}{\tau'_{on}}\right\}$$
$$C_{off} = \exp\left\{-\frac{2(1-\eta)\pi}{\tau'_{off}}\right\}.$$

The output RF amplitude is

$$A_c = A_{RF}\frac{R'_L}{1+R'_L}\frac{1}{\sqrt{1+{\tau'_{on}}^2}}, \tag{4.6}$$

and the phase shift

$$\theta = \arctan(\tau'_{on}).$$

Thanks to the fact that all the outputs have equal impedances and the switching instances are symmetrical, the transfer model is similar to a resistive divider $\frac{R'_L}{1+R'_L}$ and a low pass filter with time constant τ_{on}.

The modeled output voltages $V_{o,n}(t)$ are compared against Cadence transient simulations to validate the analysis correctness. The voltage signals are depicted in figure 4.3. The circuit parameters used for the validation are similar to the parameters of the implementation of the receiver front-end presented in chapter 6.

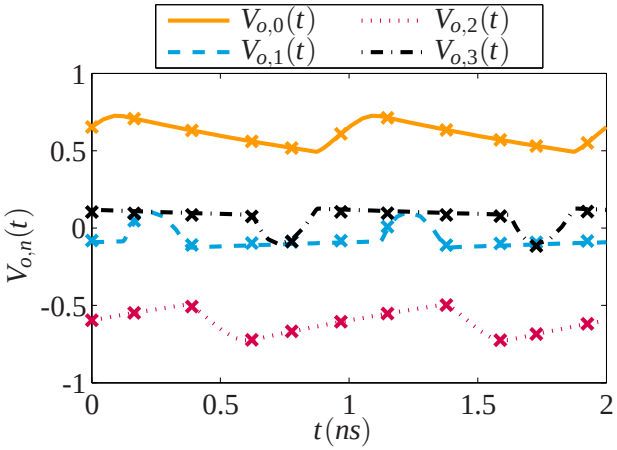


Figure 4.3: *Model (line) and Cadence simulation (markers) results for the transient output waveforms, for* $\varphi = 0$, $R_S = 405\Omega$, $r_{sw} = 100\Omega$, $R_L = 4670\Omega$ *and* $C_L = 420\,fF$ *and a 25% duty cycle.*

4.1.2 Voltage Conversion Gain

Since the RF and baseband signals are periodic, they can be written as a Fourier series. Within this section we use the following Fourier series definition for function $f(t)$:

$$\hat{f}(t) = \frac{a_{f,0}}{2} + \sum_{n=1}^{\infty} \left[a_{f,n}\cos(n\omega_c t + n\phi) + b_{f,n}\sin(n\omega_c t + n\phi)\right]$$

$$a_{f,n} = \frac{2}{T_c}\int_0^{T_c} f(t)\cos(n\omega_c t + n\phi)\,dt \tag{4.7}$$

$$b_{f,n} = \frac{2}{T_c}\int_0^{T_c} f(t)\sin(n\omega_c t + n\phi)\,dt\,, \tag{4.8}$$

where the initial phase $n\phi$ is included to achieve simpler coefficients; with this definition, the Fourier coefficients of the RF signal are zero except for $a_{Vrf,1} = A_{RF}$.

The voltage conversion gain from the RF input to zero-IF output is defined as

$$G_v \stackrel{\text{def}}{=} \frac{\max\left\{\frac{a_{Vi,0}(\varphi)}{2}\right\}}{a_{Vrf,1}}. \tag{4.9}$$

Either the in-phase or quadrature-phase output could be taken for the voltage conversion gain; here we use the in-phase signal: $V_I(t) = V_{o,0}(t) - V_{o,2}(t)$. The

output DC Fourier coefficient of the in-phase component is

$$a_{Vi,0}(\varphi) = \frac{A_c}{\pi}\left\{A\cos(\varphi-\theta)+B\sin(\varphi-\theta)\right\}.$$

From the equation it can be seen that the DC output voltage varies with the modulated RF phase. Therefore, the maximum of $a_{Vi,0}(\varphi)$ is taken with respect to φ to obtain the amplitude of the down-converted signal

$$\max\left\{\frac{a_{Vi,0}(\varphi)}{2}\right\} = \frac{A_c}{\pi}\sqrt{A^2+B^2}, \tag{4.10}$$

where

$$A = 2\sin(\eta\pi)+\cos(\eta\pi)R'_L\tau'_{on}\frac{(1-C_{on})(1-C_{off})}{1-C_{on}C_{off}}$$
$$B = \sin(\eta\pi)\left[\tau'_{on}(2+R'_L)-R'_L\tau'_{on}\frac{C_{on}-C_{off}}{1-C_{on}C_{off}}\right].$$

After substituting (4.6) and (4.10) into the voltage conversion gain definition (4.9), the voltage gain is obtained as

$$G_v = \frac{1}{\pi}\frac{R'_L}{1+R'_L}\sqrt{\frac{A^2+B^2}{1+{\tau'_{on}}^2}}.$$

The voltage conversion gain only depends on the parameters τ'_{on} and R'_L as was discussed before.

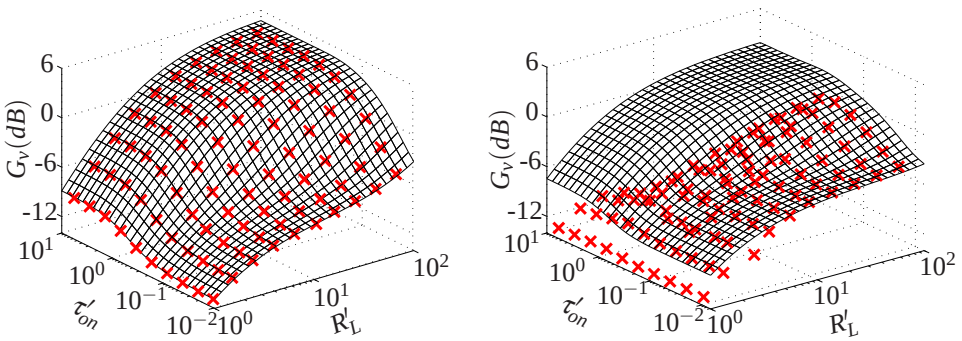


Figure 4.4: *Modeled (mesh) and simulated (red crosses) voltage conversion gain G_v for a) 25% and b) 50% duty-cycling.*

The voltage conversion gain can be higher than 0dB, see figure 4.4, because the differential-ended output is taken while the input is single ended, leading to a maximal gain of 6dB. In deriving the voltage conversion gain it was assumed that the overlap current was negligible. When this assumption holds, i.e. when either the duty cycle is 25% or the normalized on-state time constant τ'_{on} is small and the load resistance is large, the model fits well. In the case of high overlap current, the model is not valid anymore as can be seen in figure 4.4b. However, the gain is higher when there is no overlap between the four LO phases. Therefore, 25% duty cycling will be used in the rest of this chapter, and the model is valid. Moreover, from the figure and the underlying equations it is clear that the voltage gain reaches its maximum when $\tau'_{on} \to \infty$

$$\begin{aligned} G_{v,lim} &= \lim_{\tau'_{on}\to\infty} G_v \\ &= \frac{2}{\pi}\frac{R'_L \sin(\eta\pi)}{1+R'_L\eta}. \end{aligned} \tag{4.11}$$

However, the maximum of τ'_{on} is limited by practical values of R_L and C_L.

4.1.3 Input Impedance

The complex input impedance seen from the RF voltage source is defined as the voltage divided by the current at the RF frequency ω_c:

$$Z_{RF} \stackrel{\text{def}}{=} \frac{V_{RF}|_{@\omega_c}}{I_{in}|_{@\omega_c}},$$

and the mixer input impedance is

$$Z_{in} = Z_{RF} - R_S. \tag{4.12}$$

The voltage and current were depicted in figure 4.1, and source impedance R_S is subtracted since it is in series with the input impedance of the passive mixer.

It is more convenient to calculate the input admittance using the complex Fourier coefficients of the RF voltage and current, which can be expressed in terms of the sin and cos Fourier coefficients $a_{f,n}$ and $b_{f,n}$, respectively defined as (4.7) and (4.8)

$$\begin{aligned} \hat{f}(t) &= \sum_{n=-\infty}^{\infty} c_{f,n} \exp\{j\, n(\omega_c t + \varphi)\} \\ c_{f,n} &= \frac{a_{f,n} - j\, b_{f,n}}{2}. \end{aligned}$$

By using the complex Fourier components, the input admittance is

$$\begin{aligned} Y_{RF} &= \frac{c_{Irf,1}}{c_{Vrf,1}} \\ &= \frac{a_{Irf,1} - j\, b_{Irf,1}}{a_{Vrf,1} - j\, b_{Vrf,1}}\,. \end{aligned}$$

The RF voltage Fourier coefficients $a_{Vrf,1}$ and $b_{Vrf,1}$ were already given in section 4.1.2 and are copied below for convenience

$$\begin{aligned} a_{Vrf,1} &= A_{RF} \\ b_{Vrf,1} &= 0. \end{aligned}$$

The input current is

$$I_{in}(t) = \frac{V_{RF}(t) - V_{BB}(t)}{r_{on}},$$

and $V_{BB}(t)$ is the virtual baseband voltage seen at the passive mixer input,

$$V_{BB}(t) = \sum_{n=0}^{3} V_{o,n}(t)\, LO_n(t)\,,$$

where $LO_n(t)$ is the switch function shown in figure 4.2. The complex RF impedance is

$$Y_{RF} = \frac{1}{r_{on}} \frac{1+\gamma R'_L}{1+R'_L}, \tag{4.13}$$

where the complex γ coefficient is

$$\gamma = \frac{\tau'_{on}\,(\tau'_{on}+j)}{1+{\tau'_{on}}^2} \left\{ 1 - \frac{2}{\pi} \frac{1-j\,\tau'_{on}}{1+{\tau'_{on}}^2} \left[j \frac{1+C_{on}C_{off}}{1-C_{on}C_{off}} - \frac{C_{on}-C_{off}}{1-C_{on}C_{off}} \right] \right\}. \tag{4.14}$$

Equation (4.14) is complex valued and the real and imaginary parts of γ are plotted in figure 4.5. When the on-state bandwidth is very high, i.e. τ'_{on} is low, γ approaches 0 and the mixer input impedance can be modeled as a series circuit of r_{on} and R_L. In this case, the load capacitance C_L can be neglected. On the other hand, when the on-state bandwidth is very low, i.e. τ'_{on} is high, γ approaches 1 and the input impedance becomes equal to r_{on}. Thus, C_L is dominant and the steady-state baseband output voltage saturates to a DC voltage.

The limit case where $\tau'_{on} \to \infty$ is of interest, since the gain reaches its maximum value. In the limit γ becomes real valued,

$$\lim_{\tau'_{on}\to\infty} \gamma = 1 - \frac{8}{\pi^2}\frac{1+R'_L}{4+R'_L}.$$

Although τ'_{on} will never reach infinity, γ will approach the limit value when $\tau'_{on} > 10$ as can be seen in figure 4.5. As a results, the imaginary part of the input impedance also becomes zero and the real part R_{in} becomes,

$$\lim_{\tau'_{on}\to\infty} R_{in} = R_S\frac{8R'_L}{R'_L(\pi^2-8)+4\pi^2} + r_{sw}\frac{R'_L\pi^2+4\pi^2}{R'_L(\pi^2-8)+4\pi^2}. \tag{4.15}$$

In case of an ideal switch ($r_{sw} = 0\Omega$) and infinite load impedance the input impedance reduces to

$$\begin{aligned}\lim_{\tau'_{on}\to\infty, R'_L\to\infty} R_{in}(r_{sw}=0) &\approx R_S\frac{8}{\pi^2-8}\\ &\approx 4.28R_S,\end{aligned}$$

which corresponds with the result in [53]. It is interesting to note that the input impedance is a function of the source impedance. Moreover, a conjugate power match between the power source and passive mixer is only possible when the load impedance is finite.

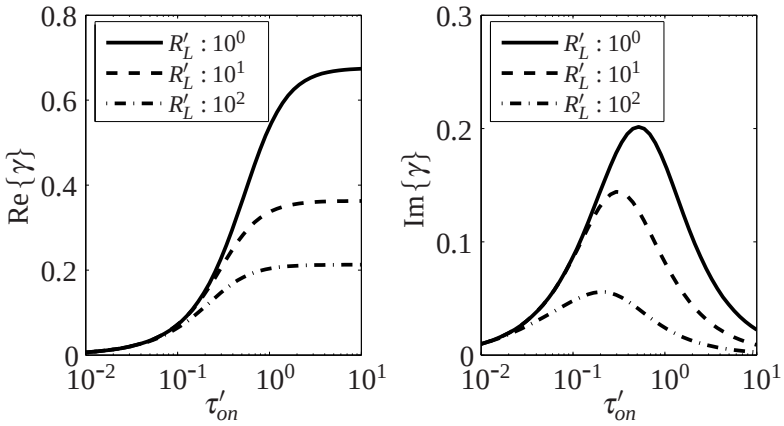


Figure 4.5: *Real and imaginary part of γ as a function of τ'_{on} and R'_L.*

4.1.4 Transducer Power Gain

The complex part of the input impedance can be matched with an inductor between the RF source and the passive mixer. Additionally, the inductor can tune out the bondpad and other parasitic capacitances, reducing the imaginary part of the input impedance to zero. Therefore, the imaginary part will be neglected when calculating the transducer power gain:

$$G_t = \left(\frac{R_{in}}{R_{in}+R_S}\right)^2 \frac{2R_S}{R_L} G_v^2, \tag{4.16}$$

assuming the load resistance R_L is much larger than the output impedance of the mixer. After substituting $r_{on} = R_S + r_{sw}$ in (4.11) and (4.15), the gain in the limit case $\tau'_{on} \to \infty$ becomes

$$\lim_{\tau'_{on}\to\infty} G_t = \left(\frac{\frac{8}{\pi^2}\frac{R'_L}{4+R'_L}R_S + r_{sw}}{R_S + r_{sw}}\right)^2 \frac{2R_S}{R'_L\,(R_S+r_{sw})} G_{v,lim}^2. \tag{4.17}$$

4.1.5 Maximal Transducer Power Gain

The transducer power gain depends on the switch resistance r_{sw}, source resistance R_S, normalized on-state time constant τ'_{on} and the normalized load resistance R'_L. Because the four parameters are independent, their optimal values can be obtained separately.

It was already shown that the gain increases as τ'_{on} increases. The optimal R_S is obtained by solving

$$\frac{\partial}{\partial R_S}\left[\lim_{\tau'_{on}\to\infty} G_t\right] = 0\,.$$

There is no solution when the switch resistance r_{sw} is 0Ω; in fact the transducer power gain no longer is a function of R_S. On the other hand, when $r_{sw} > 0$ the optimal source impedance equals

$$R_{S,opt} = \frac{r_{sw}}{2}\left|\frac{1}{1-\frac{12}{\pi^2}\frac{R'_{L,opt}}{4+R'_{L,opt}}}\right|. \tag{4.18}$$

The absolute value of R_S was taken, since the source impedance cannot be negative. Similarly, the optimal R'_L is found by substituting the obtained $R_{S,opt}$ and solving

$$\frac{\partial}{\partial R'_L}\left[\lim_{\tau'_{on}\to\infty} G_t(R_{S,opt})\right] = 0\,,$$

leading to

$$R'_{L,opt} = \frac{4\pi}{\sqrt{\pi^2-8}}\,.$$

Figure 4.6 shows the modeled and simulated transducer gain $G_t(R_{S,opt})$ where the optimal source resistance given by (4.18) is used. The modeled and simulated transducer gain results are depicted by the black mesh and red crosses respectively. The thick black line plotted at maximal τ'_{on} shows the limit case

$$\lim_{\tau'_{on}\to\infty} G_t(R_{S,opt}) = \left(\frac{2}{3}\right)^3 \frac{1}{R'_L\left(1-\frac{8}{\pi^2}\frac{R'_L}{4+R'_L}\right)} G^2_{v,lim}\,,$$

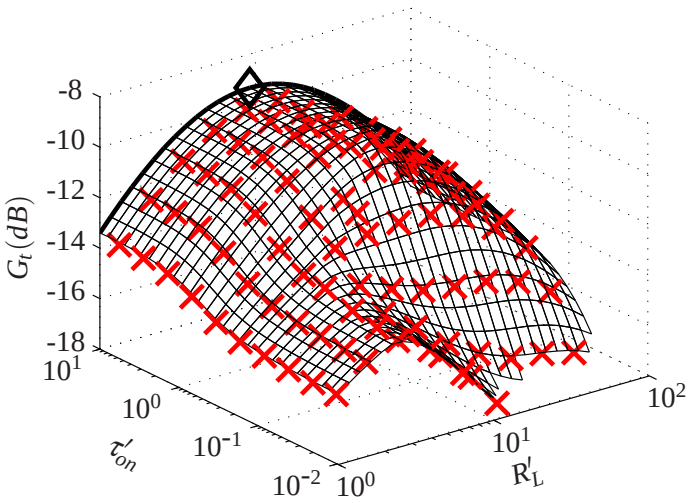


Figure 4.6: *Modeled (mesh) and simulated (red crosses) transducer power gain G_t with switch resistance $r_{sw} = 100\Omega$. The thick line gives $\lim_{\tau'_{on}\to\infty} G_t(R_{S,opt})$ and the black diamond marks the maximal transducer power gain.*

and the black diamond marks the maximal transducer power gain

$$\lim_{\tau'_{on}\to\infty} G_t(R_{S,opt}, R'_{L,opt}) = \left(\frac{4}{3}\right)^3 \frac{1}{\left(\pi^2+\sqrt{\pi^2-8}\right)^2}.$$

The figure shows that the transducer power gain G_t increases as τ'_{on} increases, as was the case for the voltage conversion gain G_v shown in figure 4.4. Although the gain still increases as $\tau'_{on} > 10^0$, the additional increase becomes negligible.

4.1.6 Noise Figure

The differential output noise of the mixer consists of three thermal noise contributions: noise generated in the source $\left(\overline{V^2_{n,s}}\right)$, the switches $\left(\overline{V^2_{n,sw}}\right)$ and in the load $\left(\overline{V^2_{n,l}}\right)$. The noise generated by the source R_S and switch r_{sw} shown in figure 4.1 are both located at the input of the mixer and therefore are both multiplied by the mixer voltage gain G_v given by (4.9). Not only the input noise concentrated round the first harmonic of the oscillator signal but also the noise around all the other harmonics are down-converted to the DC output. Taking the harmonic down-conversion into account, the noise contribution of the input noise becomes

$$\overline{V^2_{n,s}} = 4kTR_S G_v^2 \sum_{n=1,3,\ldots}^{\infty} \frac{2}{n^2}$$
$$\overline{V^2_{n,sw}} = 4kTr_{sw} G_v^2 \sum_{n=1,3,\ldots}^{\infty} \frac{2}{n^2}$$

where the harmonic down-conversion factor takes into account both the positive and negative harmonics, and can be further simplified:

$$\sum_{n=1,3,\ldots}^{\infty} \frac{2}{n^2} = \frac{\pi^2}{4}.$$

The transfer function H_L of the noise generated by the load to the baseband output is obtained by solving the time-domain differential equations similarly as was done in section 4.1.1, i.e.

$$H_L = \frac{1+\alpha R'_L}{1+R'_L},$$

where α is

$$\alpha = \frac{3}{4} + \frac{(1-C_{on})(1-C_{off})}{1-C_{on}C_{off}} \frac{\tau'_{on} - \tau'_{off}}{2\pi}$$
$$\approx \frac{3}{4} - (1-C_{off}) \frac{R'_L \tau'_{on}}{2\pi}.$$

Using the transfer function, the load contribution to the output noise is

$$\overline{V^2_{n,l}} = 4kTR_L H_L^2.$$

The noise figure of the mixer is obtained by dividing the total differential output noise by the source noise generated at the fundamental frequency

$$NF = 10\log\left\{\left(1+\frac{r_{sw}}{R_S}\right)\frac{\pi^2}{4} + \frac{2R_L}{R_S}\frac{H_L^2}{G_v^2}\right\}. \tag{4.19}$$

Note that the differential output contains two load resistances.

The simulated and modeled noise figure is shown in figure 4.7, where the axes are rotated compared to the gain plots shown before, for better readability. The

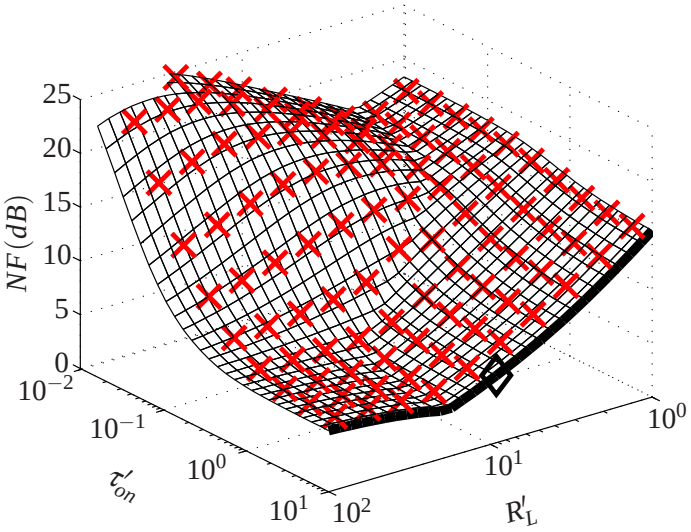


Figure 4.7: *Modeled (mesh) and simulated (red crosses) noise figure NF with switch resistance* $r_{sw} = 100\Omega$. *The thick line gives* $\lim_{\tau'_{on}\to\infty} NF(R_{S,opt})$ *and the black diamond marks the noise figure belonging to the maximal transducer power gain.*

thick black line denotes the noise figure belonging to the limit case discussed in section 4.1.4

$$\lim_{\tau'_{on}\to\infty} NF = 10\log\left\{\frac{\pi^2}{4}\left(1+\frac{r_{sw}}{R_{S,opt}}\left[1+\frac{4}{R'_L}\right]\right)\right\},$$

and the diamond symbol denotes the noise figure belonging to the maximal transducer gain.

The noise figure can be modeled by a two cascaded networks. The first network has a noise factor $F_1 = \frac{4}{\pi^2}$ and available power gain $G_{A,1} = \frac{\pi^2}{4}$, and the second network has the noise factor $F_2 = 1+\frac{r_{sw}}{R_S}\left(1+\frac{4}{R'_L}\right)$.

The first network represents the ideal mixing function, and the second network represents the noise generated by the circuit losses. The fundamental limit on the noise factor of the presented 4-phase passive mixer is set by the noise factor of the first network, which reduces as the number of mixer phases increases [53]. Note that there is a 3dB difference in minimal noise figure, because here we use the output SNR of one differential output phase, whereas [53] uses the combined SNR of all the output phases.

4.1.7 Optimal Design

As is visible from figure 4.7 the noise figure given by (4.19) is close to minimal at the maximal transducer gain. Therefore, the maximal transducer gain is chosen as the optimal design point. Additionally, there should be no overlap between LO phases for a maximal power gain, thus a duty cycle η of 25%. Recapitulating, the optimal normalized load resistance and source resistance are

$$R'_{L,opt} = \frac{4\pi}{\sqrt{\pi^2-8}}$$
$$R_{S,opt} = \frac{r_{sw}}{2}\frac{1}{1-\frac{12}{\pi^2}\frac{R'_{L,opt}}{4+R'_{L,opt}}}.$$

It is interesting to note that, for a fixed duty cycle, the optimal normalized load resistance $R'_{L,opt}$ is a constant and does not depend on other parameters. Therefore the actual non-normalized load resistance only is a function of the source resistance:

$$R_L = R'_{L,opt}\left(R_S + r_{sw}\right),$$

which is similar to the conjugate impedance matching required for optimal power transfer. The source and load resistances are proportional to the switch on-resistance r_{sw}, and the maximal gain is independent of r_{sw}. Taking into account the trade-off between the LO power needed to drive the switch and r_{sw} discussed in section 4.1.1, the switch should be made as small as possible to minimize the LO power consumption. However, the minimal size is limited by the impedance transformation ratio between $R_{S,opt}$ and the external signal source; at some point r_{sw} becomes too high and the external signal source can no longer be matched to the passive mixer using practical discrete components. Once all the resistances

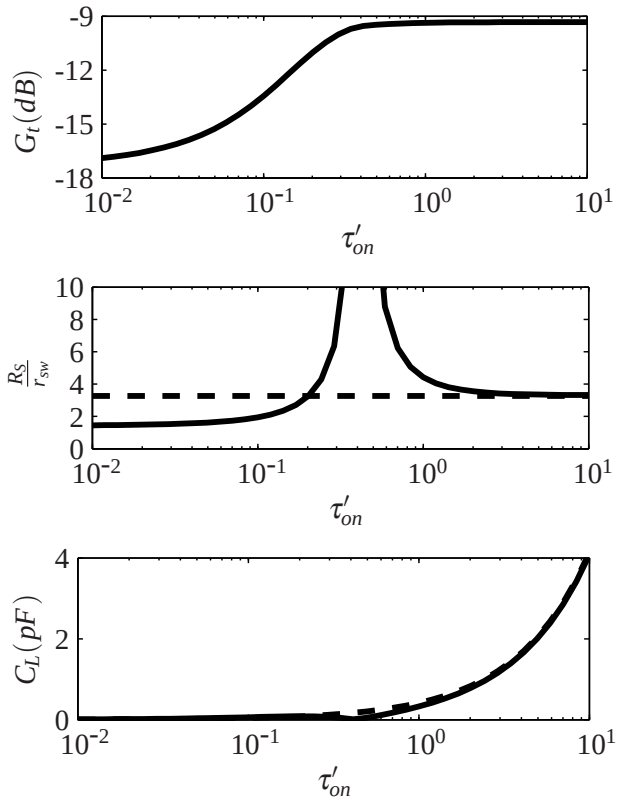


Figure 4.8: *The transducer power gain G_t, normalized source resistance $\frac{R_S}{r_{sw}}$ and load capacitance C_L as function of the normalized on-state time constant τ'_{on} using the optimal normalized load resistance $R'_{L,opt}$. The solid line represents the model results and the dashed line shows the result when $R_{S,opt}$ is substituted.*

are known, the required load capacitance is obtained from τ'_{on} as

$$C_L = \frac{\tau'_{on}}{\omega_c} \frac{1}{R_{S,opt} + r_{sw}} \left(1 + \frac{1}{R'_{L,opt}}\right).$$

The transducer power gain G_t given in (4.16) increases as τ'_{on} increases, see figure 4.8(a). A large τ'_{on} is equivalent to a low bandwidth of the low-pass mixer output filter. When the bandwidth is low the input RF signal is converted more efficiently to the DC output and the harmonics of the RF signal at the output of the mixer are reduced. However, also the required C_L increases, which can lead to impractical large sizes, see figure 4.8. The gain does not increase significantly when $\tau'_{on} > 1$. It is beneficial for the impedance matching between R_S and the mixer input impedance to choose τ'_{on} slightly larger than one, because it leads to a reduced impedance ratio.

4.2 Low-Power Local Oscillator Design

By relaxing the oscillator requirements, most notably the phase noise performance, the power consumption can be decreased. The main target is to obtain a low power oscillator that satisfies all the minimal requirements, without being over-designed. Within this section the traditional cross-coupled LC oscillator is compared to the ring oscillator topology. Both are designed to have differential quadrature outputs. The theoretical background is given in section 4.2.1.

In the case of an LC oscillator, energy is only needed to start the oscillation and replenish the energy loss in its tank. Fundamentally, the ring oscillator charges and discharges the load capacitance each cycle, in other words energy is wasted every cycle. Therefore, it is usually assumed that the ring oscillator is less power efficient than the LC type. However, technological limits on the maximal impedance change this conclusion, as will be explained in more depth in sections 4.2.4 and 4.2.5. Additionally, section 4.2.4 gives theoretical lower bounds on the power consumption of the two oscillator types.

4.2.1 Oscillator Design Considerations for Minimum Power

The parameters given in table 4.1 are used throughout this section. These parameters give a common basis on which different oscillator topologies can be compared.

Table 4.1: *Parameters used for the comparison of the LC and ring oscillators.*

Parameter	Meaning
f_{osc}	Oscillation frequency
ΔV	Differential signal voltage amplitude
P_{sig}	Signal power
$\mathscr{L}(\Delta f)$	Phase noise in dBc/Hz at frequency offset Δf

For stable oscillations to occur, the oscillator needs to comply with Barkhausen's criteria given by

$$|H(f_{osc})| = 1$$
$$\angle H(f_{osc}) = \pi + 2k\pi\,,\, k \in \mathbb{Z}\,.$$

In these equations, the oscillation frequency is given by f_{osc}. Note that the loop gain, i.e. $|H(f_{osc})|$, should be designed larger than one in order for the oscillation to start, but reduces to one in steady state oscillation either due to non-linearities of the system that occur when the amplitude of the signal becomes significant, or by means of an amplitude control loop.

Leeson's phase noise model

$$\mathscr{L}(\Delta f) = \frac{2FkT}{P_{sig}}\left(\frac{f_{osc}}{2Q\Delta f}\right)^2 \tag{4.20}$$

is used to determine the quality of the oscillator. It can be applied to both the LC and the ring oscillator. It is important to note that the phase noise is inversely proportional to the signal power P_{sig}; assuming the oscillator efficiency stays constant, the signal power and therefore dc power can be decreased by relaxing the phase noise requirements.

4.2.2 LC Oscillator Design

A widely used LC oscillator topology is depicted in figure 4.9, where C_L encompasses both the tuning capacitance and parasitic capacitances. It is assumed that two of these oscillator cores are used to generate the required I and Q outputs, and that the coupling between these two cores consumes no power and has no influence on the operation of the separate cores.

The oscillator will oscillate at the resonance frequency of the LC tank

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_L}}\,,$$

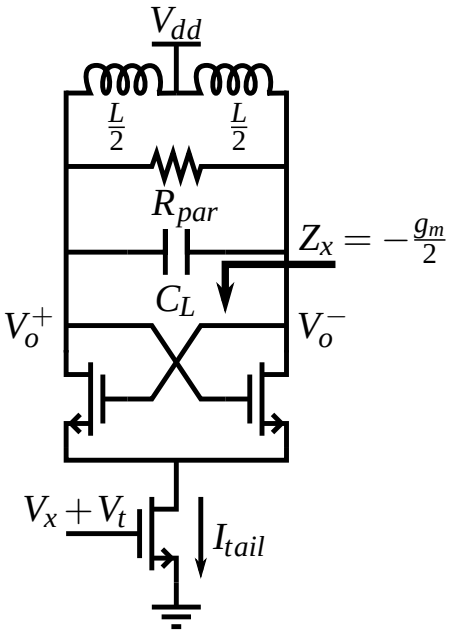


Figure 4.9: *Cross coupled LC oscillator schematic.*

when the negative resistance looking into the cross coupled pair compensates the tank losses

$$\frac{g_m}{2} \geq \frac{1}{2\pi f_{osc} QL}\,.$$

When the LC oscillator operates in the current limited regime, the differential voltage amplitude in case of ideal switching [55] is

$$\Delta V \approx \frac{4}{\pi} I_{tail} R_{par}\,.$$

The parasitic LC tank resistance R_{par} is approximately equal to

$$R_{par} \approx 2\pi f_{osc} QL\,,$$

when assumed that the inductor dominates the Q factor. In this regime the DC-to-RF efficiency of the oscillator is maximal.

4.2.3 Ring Oscillator Design

A ring oscillator is a cascade of N inverting amplifier stages, where the output of the last stage is connected to the input of the first stage. In case of an even number

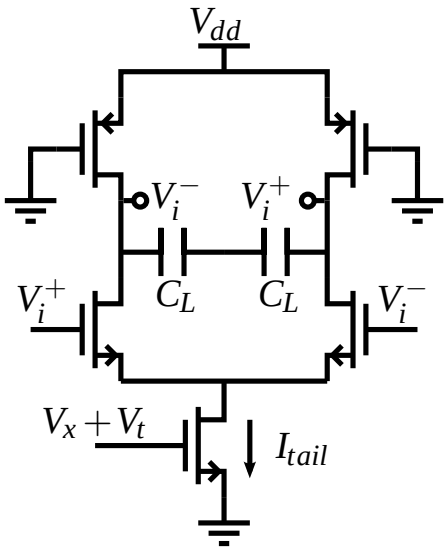


Figure 4.10: *A single stage of a ring oscillator.*

of stages, the polarity of one of these stages needs to be inverted to satisfy the Barkhausen criteria. Each of the stages has a frequency dependent phase shift and is modeled as a single pole amplifier with transfer function

$$H_1(j\omega) = \frac{A_v}{1 + \frac{j\omega}{2\pi f_p}},$$

where A_V is the DC gain and f_p is the frequency of the most dominant pole. Combining the transfer function with Barkhausen's criteria leads to a condition on the DC gain:

$$|A_v| = \sqrt{1 + \tan^2\left(\frac{\pi}{N}\right)}.$$

An amplifier stage including parasitic capacitances C_L is depicted in figure 4.10. The two P-type transistors in the load are biased in the triode region.

At RF frequencies the ring oscillator will never reach the full output voltage swing, but will always be a factor ε smaller, as was discussed in [56]. This effect is shown in figure 4.11, where A is the theoretical amplitude and εA is the actual amplitude.

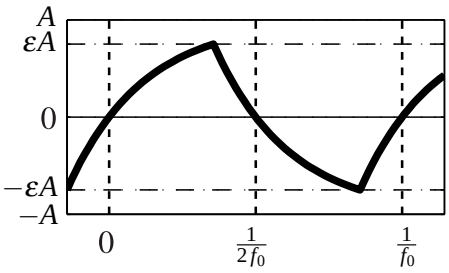


Figure 4.11: *In a ring oscillator the amplitude is a factor ε times the theoretical amplitude A.*

The swing parameters used in [56] are given below. The parameters only depend on N; for a 4-stage ring oscillator, $\varepsilon \approx 0.839$.

$$1 = (1+\varepsilon)^{N-1}(1-\varepsilon) \tag{4.21}$$

$$\xi = \left(\frac{1+\eta^{2N}}{1-\eta}\right)^2 \tag{4.22}$$

$$\eta = \frac{1-\varepsilon}{1+\varepsilon}. \tag{4.23}$$

Using the models presented in this section, the differential voltage amplitude is

$$\Delta V = \varepsilon R_L I_{tail},$$

and the oscillation frequency is given by

$$f_{osc} = \frac{\varepsilon I_{tail}}{2N\ln(1+\varepsilon)C_L\Delta V}. \tag{4.24}$$

4.2.4 LC and Ring Oscillator Design Approach

The total power consumption of the LC and ring oscillator systems are

$$P_{LC} = 2V_{dd}I_{tail} \tag{4.25}$$

$$P_{ring} = NV_{dd}I_{tail}. \tag{4.26}$$

A factor 2 is added to the LC oscillator (4.25) since two LC cores are needed to generate the I and Q outputs. Moreover, the ring oscillator should have an even number of stages N. To minimize the power consumption of the oscillator, the product of the number of stages N, supply voltage V_{dd} and tail current I_{tail}

should be minimized for a given phase noise requirement. The best trade-off between power consumption and phase noise is obtained at the lowest number of oscillator stages [57]. Since a quadrature output is needed, the number of stages is chosen to be 4. Additionally the supply voltage is shared with other circuits, and therefore is fixed. This leaves the tail current as the only degree of freedom for the designer.

A lower bound for the tail current is obtained from the maximally acceptable phase noise level. Leeson's phase noise model was given by (4.20) and copied below for convenience:

$$\mathscr{L}(\Delta f) = \frac{2FkT}{P_{sig}} \left(\frac{f_{osc}}{2Q\Delta f} \right)^2 .$$

The mapping of the circuit components to the noise factor F for the LC oscillator was given in [58]. For the ring oscillator the phase noise model was presented in [59] and extended in [56], respectively. The quality factor Q for the LC oscillator is approximately equal to the quality factor of the tank inductor. The quality factor for the ring oscillator is used to fit Leeson's equation to the ring oscillator phase noise model given in [56]. The parameters for the ring and LC oscillators are given in table 4.2. In this parameter table γ is the factor used in the mosfet channel noise model and ε and ξ were given by equations 4.21 and 4.22 respectively. To obtain the lowest phase noise for a given current, the quality factor

Table 4.2: *Phase noise parameters for both the LC and ring oscillator.*

	LC	**Ring**
P_{sig}	$\frac{2}{\pi}\Delta V I_{tail}$	$\frac{1}{2}\Delta V I_{tail}$
F	$2+2\gamma+\frac{4\pi\Delta V}{9V_x}\gamma$	$2\varepsilon+2\gamma\frac{\Delta V}{V_x}+\gamma 2\varepsilon A_v\left(1-[1+\varepsilon]^{-2}\right)$
Q	$\approx Q_L$	$\sqrt{\frac{\ln(1+\varepsilon)}{\varepsilon\xi}}$

should be maximized. With an increasing number of stages the quality factor increases and approaches $\sqrt{\ln(2)}$, which is much lower than the quality factor of practical LC oscillators.

By choosing the maximal allowed phase noise, a minimal tail current is obtained. This tail current in combination with the desired voltage swing ΔV

$$\Delta V_{LC} \approx \frac{4}{\pi} I_{tail} Q \omega_o L \tag{4.27}$$

$$\Delta V_{Ring} = \varepsilon I_{tail} \frac{L_p}{\mu_p C_{ox} W_p \left(V_{dd} - |V_{Tp}| - \frac{\Delta V}{2\varepsilon}\right)}, \tag{4.28}$$

is used to determine the required circuit impedance. When I_{tail} is decreased, the load impedance has to be increased. In the case of the LC oscillator, the inductance L has to be increased whereas the $\frac{L_p}{W_p}$ ratio has to increase for the ring oscillator type, see (4.27) and (4.28) respectively. However, an increasing inductance leads to an increase of the parasitic capacitances. At some point the inductance can no longer be increased, because the self-resonance frequency becomes too low. This maximal inductance value depends on the technology used and the practical implementation of the on-chip inductor, such as e.g. layout.

Given the transistor width W_p is minimal, the total area increases with an increase of $\frac{L_p}{W_p}$, which in turn leads to larger parasitic capacitances. At some point the desired oscillation frequency can no longer be obtained, hence the current can not decrease anymore. Again the parasitics and thus the minimal capacitance depends on the technology used.

Besides the phase noise and swing requirements also the oscillation criteria should be met. The gain criteria can be met by scaling the NMOS transistors and the right oscillation frequency can be set by adding additional capacitances to the load. When the parasitic capacitances are larger than the required total capacitance, the tail current should be increased which leads to a more relaxed requirement on the load.

The minimal LC tail current can be obtained by substituting the maximal quality factor Q and inductance L in (4.27). Substituting the tail current in (4.25) yields the minimal power consumption

$$P_{\text{LC, min}} = \frac{V_{dd}\Delta V}{4Q_{\max}L_{max}f_{osc}}.$$

The minimal tail current for the ring oscillator is obtained by substituting the minimal capacitance in (4.24). Using this current, the minimal ring oscillator power consumption is obtained

$$P_{\text{ring, min}} = \frac{2N^2\ln(1+\varepsilon)V_{dd}\Delta V}{\varepsilon}C_{min}f_{osc}.$$

4.2.5 LC vs Ring Oscillators

The ring oscillator consumes less power than the LC type for $\mathscr{L}(\Delta f)$ exceeding a cross-over point $\mathscr{L}_X(\Delta f)$. Assuming $P_{\text{LC, min}} < P_{\text{ring, min}}$, the cross-over point $\mathscr{L}_X$

is obtained by calculating the phase noise of the ring oscillator for $P_{\text{ring}} = P_{\text{LC, min}}$,

$$\begin{aligned} P_{\text{ring}} &= P_{\text{LC, min}} \\ I_{\text{tail, ring}} &= \frac{\Delta V}{4NQ_{\max}L_{max}f_{osc}} \\ \mathscr{L}_X(\Delta f) &= \mathscr{L}_{\text{ring}}(\Delta f)\big|_{I_{\text{tail, ring}}} \\ \mathscr{L}_X(\Delta f) &= F_{ring}\frac{4kTNQ_{\max}L_{max}f_{osc}}{\Delta V^2}\left(\frac{f_{osc}}{Q_{ring}\Delta f}\right)^2. \end{aligned}$$

The condition $P_{\text{ring, min}} < P_{\text{LC, min}}$ is rewritten as an upper bound on the oscillation frequency

$$\begin{aligned} P_{\text{LC, min}} &> P_{\text{ring, min}} \\ \frac{V_{dd}\Delta V}{4Q_{max}L_{max}f_{osc}} &> \frac{2N^2\ln(1+\varepsilon)V_{dd}\Delta V}{\varepsilon}C_{min}f_{osc} \\ f_{osc} &< \frac{1}{2N}\frac{1}{\sqrt{L_{max}C_{min}}}\sqrt{\frac{\varepsilon}{2\ln(1+\varepsilon)Q_{\max}}}. \end{aligned}$$

The power consumptions of both oscillator types are compared with respect to the required phase noise. The parameters used for this comparison and practical values for the used TSMC CMOS 90nm process are given in table 4.3.

Table 4.3: *Parameters used for the comparison of the LC and ring oscillators.*

Parameter	Value
f_{osc}	915 MHz
ΔV	0.35 V
V_{dd}	1 V
N	4

Parameter	Value
L_{max}	20 nH
Q_{max}	11
C_{min}	3 fF

The predicted and simulated power consumption of the ring oscillator are shown in figure 4.12. It can be seen that the model is very close to the simulation results. At low power consumption the error increases, since the transistor sizes decrease and the used mosfet models fit less well for smaller transistors.

Figure 4.13 shows the minimal power consumption as a function of the maximal tolerable phase noise for both the ring and LC oscillators. Additionally, the calculated cross over phase noise point $\mathscr{L}(\Delta f)$ is shown by the dashed line. It is not possible to consume less power for a certain phase noise requirement.

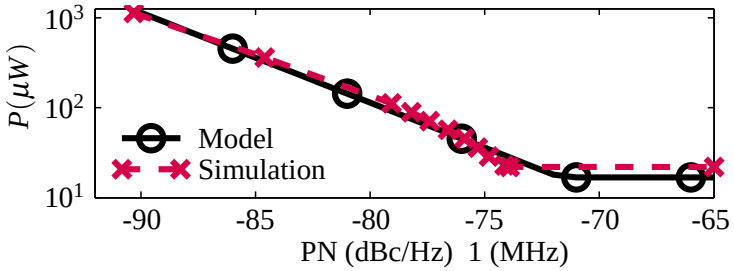


Figure 4.12: *Simulated and predicted power consumption of the ring oscillator as a function of the required phase noise.*

However, it is possible to design a circuit that consumes more power. Hence, the figure shows a lower bound on the energy consumption. The bottom figure gives the required inductance and capacitance for the LC and ring architecture respectively. The two figures show the load impedance has to increase, i.e. higher inductance L and lower capacitance C, as the power consumption decreases.

At low phase noise levels an LC oscillator is more power efficient than a ring oscillator, see figure 4.13, which is expected from theory. However, at higher

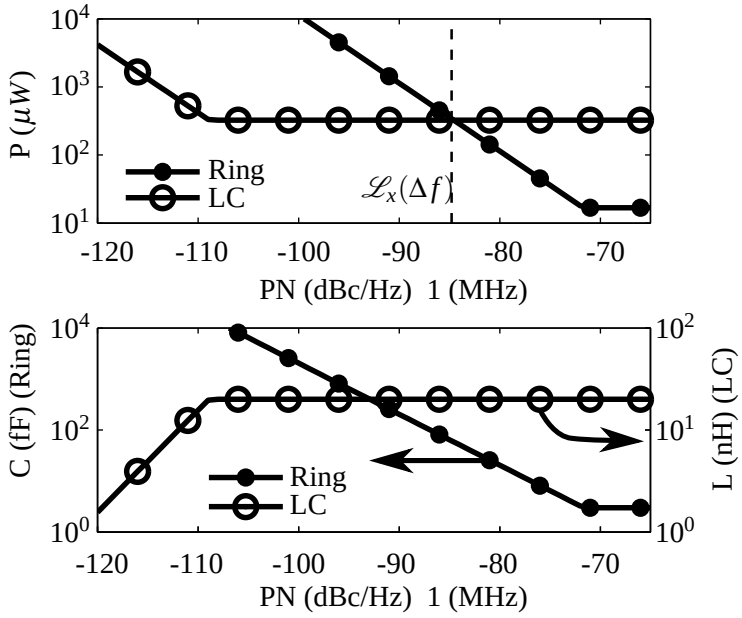


Figure 4.13: *Lower bound on the power consumption and required inductance and capacitance.*

phase noise levels this no longer holds, since at a certain point the impedance of the load can no longer increase because of technological limitations. Thus the technology limits the minimal power consumption.

The parasitic capacitance scales with technology, leading to a lower power consumption of the ring oscillator. This is in contrast with the power consumption of the LC oscillator. However, the downside is that the phase noise will increase at the same time. Additionally, the power consumption of the ring oscillator decreases with a decrease of the oscillation frequency.

The LC performance can be increased by using a different technology that increases the quality factor or the maximal inductance. When the quality factor is increased either the phase noise is decreased with constant power consumption or the power consumption is decreased with constant phase noise.

4.3 FSK Demodulator

Figure 4.14a shows the block diagram of the theoretical FSK demodulator, and figure 4.14b shows the 1-bit implementation. The 1 bit multipliers are implemented by the XOR and NXOR gates and the 1-bit adder by the AND gate.

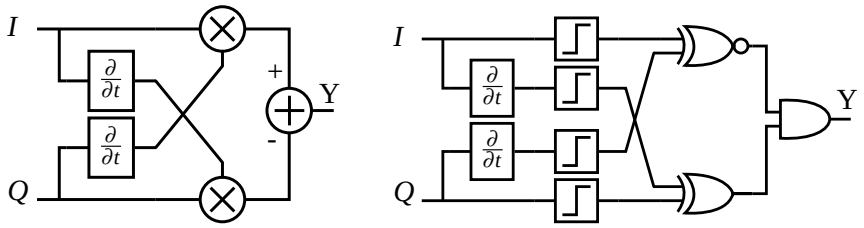


Figure 4.14: *Block diagrams of (a) a mathematical FSK demodulator and (b) a 1-bit FSK demodulator.*

The demodulator is a one-bit implementation of a Digital Cross-Differentiate Multiply (DCDM) demodulator. The in-phase (I) and quadrature-phase (Q) signals are

$$I(t) = A\cos\left([a_n\Delta\omega + \omega_{off}]t\right)$$
$$Q(t) = A\sin\left([a_n\Delta\omega + \omega_{off}]t\right),$$

where A is the signal amplitude, ω_{off} and $\Delta\omega$ are the frequency offset and FSK frequency deviation. The data is given by $a_n = \pm 1$. The derivatives of the input signals are

$$\begin{aligned}\dot{I}(t) &= -A\left[a_n\Delta\omega + \omega_{off}\right]\,\sin\left(\left[a_n\Delta\omega + \omega_{off}\right]t\right)\\ \dot{Q}(t) &= A\left[a_n\Delta\omega + \omega_{off}\right]\,\cos\left(\left[a_n\Delta\omega + \omega_{off}\right]t\right)\,.\end{aligned}$$

Since all the information is contained in the frequency, hard limiters can be used to remove the amplitude noise and improve the performance. The hard limiter operates on the signal envelope and is denoted by $\mathbf{L}\{.\}$. The demodulator output Y is

$$\begin{aligned}Y(t) &= \mathbf{L}\left\{I(t)\dot{Q}(t) - Q(t)\dot{I}(t)\right\}\\ &= \mathbf{L}\{A\}\,\mathbf{L}\left\{A\left[a_n\Delta\omega + \omega_{off}\right]\right\}\,.\end{aligned}$$

Depending on the offset frequency the output can be written as

$$Y(t) = \begin{cases} 1 & \text{if } \omega_{off} \geq \Delta\omega \\ 1 & \text{if } -\Delta\omega < \omega_{off} < \Delta\omega \text{ and } a_n = 1 \\ 0 & \text{if } -\Delta\omega < \omega_{off} < \Delta\omega \text{ and } a_n = -1 \\ 0 & \text{if } \omega_{off} \leq -\Delta\omega \end{cases} \tag{4.29}$$

Note that the output of the demodulator is unipolar while a_n is a bipolar signal. Assuming there is no amplitude noise, the demodulator performance does not deteriorate as long as the frequency offset is less than the frequency deviation.

4.4 Automatic Frequency Control Loop

A free-running ring oscillator is used to achieve low power consumption. However, a ring oscillator is sensitive to power supply and temperature variations. To stabilize the oscillation frequency, a control loop is needed. A non-coherent FSK receiver does not require a phase-locked-loop, a frequency control loop is sufficient. A simplified block diagram of the automatic frequency control loop is shown in figure 4.15. The depicted loop is implemented in the discrete time for ease of digital implementation. However, it is also possible to use a time continuous loop. The mixer and FSK demodulator act as frequency comparator; the mixer is used to obtain the LO frequency offset (ω_{off}), and the demodulator translates the frequency offset to a voltage. The demodulator was modeled in section 4.3 and the demodulator output was given by equation (4.29). The measured

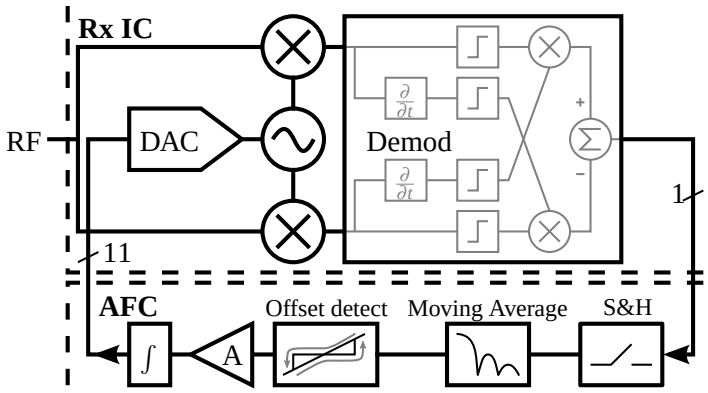


Figure 4.15: *Simplified block diagram of the automatic frequency control loop.*

offset is sampled and filtered using a moving average filter by the off-chip AFC implementation. The discrete time-domain representation of the implemented moving average filter is

$$y_{mavg}[k] = \sum_{n=0}^{N-1} x[k-n]\,,$$

where N is the number of FIR taps. Note that the filter coefficients are 1 instead of $\frac{1}{N}$ for ease of implementation. As a result, the gain of the filter is not 1, but N. The integration time of the moving average filter is $T_{mavg} = NT_s$, where T_s is the sample time.

Besides the frequency offset, the filtered signal also contains the filtered FSK data a_n. The residual FSK data is removed by the threshold detector. For the AFC to discriminate between valid data and frequency offsets the maximal run length of a sequence of either zeros or ones need to be limited. Hysteresis is used in the threshold detector to remove undesired toggling when the error crosses the threshold. Finally, the filtered error is amplified, integrated and fed-back to the on-chip ring oscillator.

4.4.1 Closed Loop Analysis

The AFC loop is linearized, to ease the closed-loop analysis. Additionally, the AFC loop is analyzed without input noise. The threshold detector is removed in the linearized model, assuming the frequency offset is larger than the threshold. When the offset is smaller than the threshold, the gain of the threshold detector is

zero and the loop is disabled. The demodulator can be modeled as a limiter when no data is present or when the frequency offset is larger than the FSK frequency deviation. The gain of the limiter is inversely proportional to the input signal. Since the demodulator only reacts to frequency offsets larger than the frequency deviation $\Delta\omega$, the maximal demodulator gain is $\frac{1}{2\Delta\omega}$.

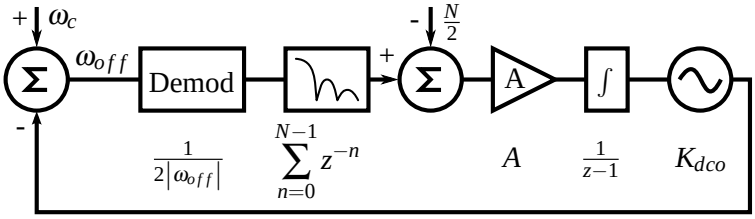


Figure 4.16: *Linearized discrete-time model of the AFC loop, including the linear gain of the blocks.*

The linearized discrete-time AFC loop is depicted in figure 4.16, and the Z-domain closed loop transfer function becomes

$$H_{cl}(z) = \frac{G\sum_{n=0}^{N-1} z^n}{z^N + (G-1)z^{N-1} + G\sum_{n=0}^{N-2} z^n},$$

where the open loop gain is

$$G = \frac{AK_{dco}}{2\left|\omega_{off}\right|}.$$

The AFC loop is stable when all the poles of the closed-loop transfer function lie within the unit circle $|z| = 1$. The poles depend on the open loop gain G. The criteria on G for a stable loop can be checked analytically using the "Jury's stability test". However, the table needed for the test contains $2N-3$ rows, making it very cumbersome to check the stability for moving average filters with many taps. Instead the upper bound on G is numerically found using Matlab. The upper limit on G as a function of filter length N is depicted in figure 4.17. The fitted curve $G = \frac{4.5}{N^2}$ fits well with the numerical Matlab results. Moreover, the fitted curve lies below the upper limit on G for every N and can be used as an upper limit on G. Thus the loop is stable when the gain A satisfies

$$A < \frac{4.5}{N^2}\frac{2\left|\omega_{off}\right|}{K_{dco}}. \tag{4.30}$$

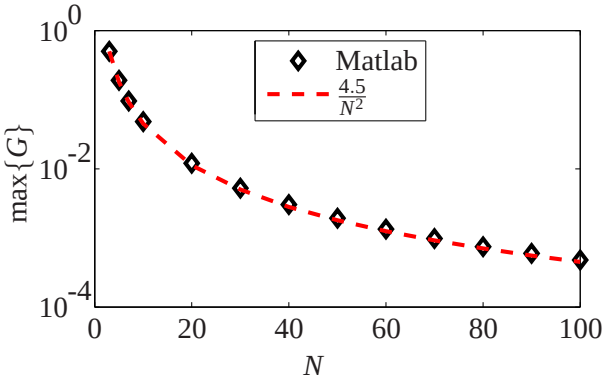


Figure 4.17: *Upper limit of the open loop gain G for stable operation. The red dashed line represents the fitted curve* $G = \frac{4.5}{N^2}$.

Figure 4.18 shows the closed-loop transfer function for three different open loop gain values G. When the loop is on the edge of stability ($G = \frac{4.5}{N^2}$), there is a large peak in the amplitude response. When $\left|H_{cl}\left(e^{j\Omega}\right)\right| > 1$ the loop can over-compensate the frequency error, which is undesired. Therefore, the upper bound of the open loop gain is set as

$$G = \frac{1}{N^2}\,.$$

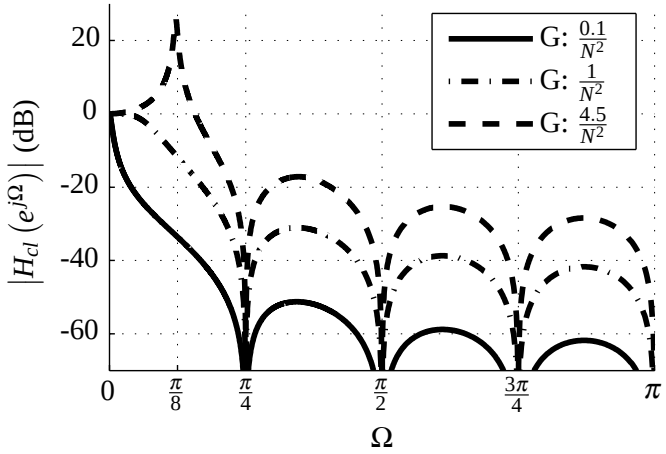


Figure 4.18: *Modulus of the closed loop transfer function for three different open loop gains and* $N = 8$.

Substituting the maximal demodulator gain $\frac{1}{2\Delta\omega}$, A is upper bounded as follows:

$$A < \frac{1}{N^2}\frac{2\Delta\omega}{K_{dco}}.$$

The slew rate, or maximal DCO frequency step per second is obtained by observing that the maximal output of the moving average filter is $\frac{N}{2}$ and the gain per second of the integrator is $\frac{1}{T_s}$. Therefore, the slew rate becomes

$$\mathrm{SR} = AK_{dco}\frac{N}{2T_s}\,(rad/s^2).$$

4.4.2 System Level Implications

The automatic frequency feedback loop uses the received data to calibrate the local free-running oscillator against process, voltage and temperature (PVT) mismatches. This feedback scheme has implications on the system.

When the receiver is started for the first time the free oscillator offset is completely unknown. Therefore, the receiver should scan the spectrum by sweeping its oscillation frequency. Care should be taken not to track interfering signals. Therefore, the digital baseband should first determine whether the received signal is an interferer or not before it starts tracking it.

Once the desired signal is received the receiver knows approximately which DCO code corresponds to the desired frequency band. Since the temperature and temperature only change slowly the receiver does not need to track fast varying error signals. Moreover, once the DCO code is known also the maximal and minimal bounds on the variation can be estimated. Also the supply voltage could be fed forward to the control loop to estimate the first order frequency deviation due to supply voltage variations. This information should be used in the feedback loop to ensure that the loop does not unlock. Additionally when there is no input signal the loop should not track the received noise but should be disabled. This can be achieved by implementing a received signal strength indicator (RSSI) and comparing the received signal strength to a minimal signal threshold.

For the AFC to work it is not required that binary zeros and ones are equiprobable. However, for the AFC to discriminate between valid data and frequency offsets the maximal run length of a sequence of either zeros or ones need to be limited.

4.5 Conclusion

In this chapter closed-form models and optimal design procedures were presented that make use of body area network specific requirements. The short communication distance is exploited by removing the low-noise amplifier (LNA), and generating gain at the low-frequency baseband stage. The reduced isolation from the oscillator to the antenna is not a problem, because the oscillator signal itself is very low power in a WURx. In the mixer-first topology the mixer is matched to the off-chip antenna and its transducer power gain has a large influence on the overall noise figure. As was discussed in section 4.1 the maximal transducer gain is obtained when the overlap current between the I and Q phases is minimized, which means a oscillator duty cycle of 25%. In section 4.1.7 the optimal mixer impedances where given. Furthermore, it was shown that the optimal load and source impedances scale linearly with the switch on-resistance.

Besides the LNA also a stable local frequency reference consumes a lot of power. Given relaxed phase noise requirements and taking into account technology limitations on the parasitic capacitances and on-chip inductor quality factor it was shown that ring-oscillators can be more power efficient than LC oscillators. By exploiting the FSK demodulator as a frequency offset detector the receiver chain is used in an automatic frequency control loop to stabilize the free-running low-power oscillator. The feedback loop should use all the information in the feedback loop for a robust control.

CHAPTER 5

RECEIVER FRONT-END VERSION 1

A mixer-first wideband-FSK architecture has been proposed in the previous chapters to reduce the receiver power consumption at the cost of bandwidth efficiency. In this chapter the feasibility of a low-power mixer-first front-end is studied. Special attention is paid to the passive mixer and first IF amplifier since they determine the noise figure of the complete receiver. Moreover, a lot of design effort is spent on the local oscillator, since it is the most power consuming sub-circuit.

In chapter 4, the theoretical optimal design paradigm of the passive mixer and local oscillator was presented. The transistor implementations of the circuits are presented in section 5.1, after which the measurement results are given in section 5.2. These results are compared against other reported low-power FSK receivers using a radar plot in section 5.3. A radar plot is used since the specific receiver optimization target can be seen immediately, e.g. low-power consumption, high linearity, etc. The chapter ends with conclusions and presents recommendations for future low-power front-end designs.

5.1 Implementation

The mixer-first receiver architecture depicted in figure 5.1 is used for the WURx front-end. The transistor level implementations of the receiver sub-blocks are given in this section. All the circuits are designed with low power consumption

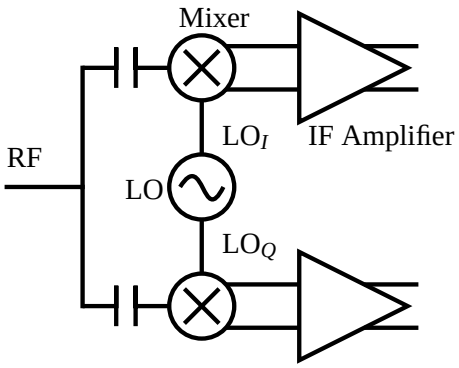


Figure 5.1: *Proposed mixer-first receiver architecture.*

in mind. As was already mentioned the LNA is omitted to reduce power consumption and the passive mixer shown in section 5.1.1 is matched to the external 50Ω signal source. The low-power oscillator and IF amplifier implementations are presented in sections 5.1.2 and 5.1.3. The measurement results of the subcircuits and the complete receiver are given in section 5.2.

5.1.1 Mixer

A passive mixer has been chosen instead of an active mixer, since power consumption is of the utmost importance. Additionally, the passive mixer has lower 1/f noise and usually a larger linearity than an active mixer. Although the bandpass filter reduces the 1/f noise it is still important to keep the 1/f noise low, since the 1/f noise corner frequency can easily be higher than the cut-off frequency of the bandpass filter. The presented passive mixer uses 50% duty-cycling.

Since no LNA is present, the mixer is the first block in the RF front-end. Therefore, the input of the mixer should be matched to 50Ω in order to have the maximal power transfer. The circuit of the mixer is shown in figure 5.2. The load resistance R_L represents the input impedance of the following stage.

To minimize the overall noise figure, the power gain of the passive mixer should be maximized by choosing the optimal load impedance R_L. Actually, the available power gain should be optimized, but the available power gain of the IF amplifier is maximal when its input is also matched. These two optimization goals can both be obtained when the transducer gain is maximized, as was discussed in section 4.1. Additionally, there is a trade-off between the mixer switch resistances and the required LO power needed to drive the switches. Limiting the LO

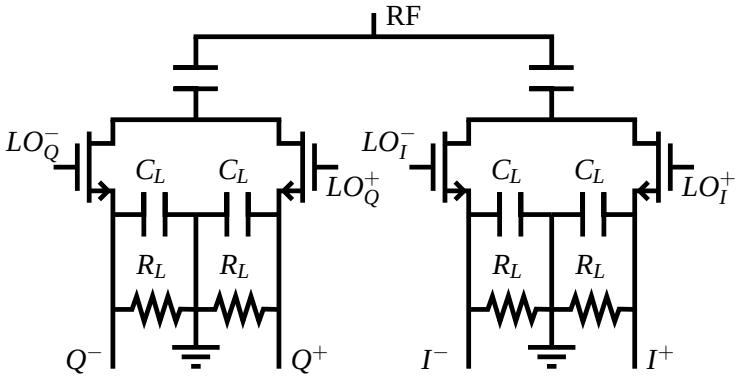


Figure 5.2: *Passive quadrature mixer circuit*

buffer power consumption to 20µW, the switch resistance is limited to approximately 200Ω. Using these choices, figure 5.3 shows the transducer power gain as a function of R_L. The optimal load resistance is approximately 2.3kΩ.

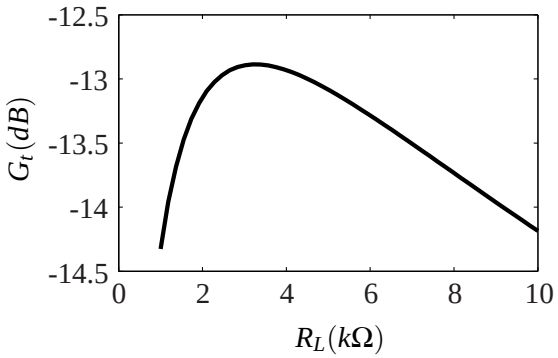


Figure 5.3: *Simulated transducer power gain G_t of the passive quadrature mixer as function of the load impedance R_L.*

5.1.2 Local Oscillator

Because the RF signal frequency is relatively low, only 868MHz/915MHz, a ring oscillator can be less power-consuming than an LC oscillator, see section 4.2. This can be explained by the fact that the energy lost in the on-chip inductor is larger than the energy needed to charge the load capacitance of each ring-oscillator stage. Moreover, with a decrease in technology-node size, the parasitic capacitances and therefore the energy needed to charge each node decrease. However, this also leads to an increased phase noise. Assuming a maximal bit

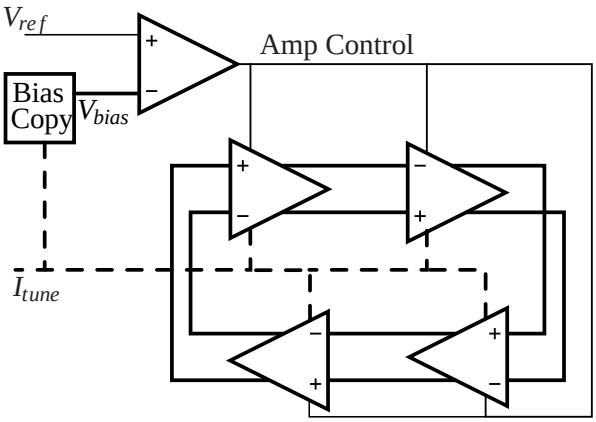


Figure 5.4: *Schematic overview of the four stage ring oscillator, including the amplitude stabilization.*

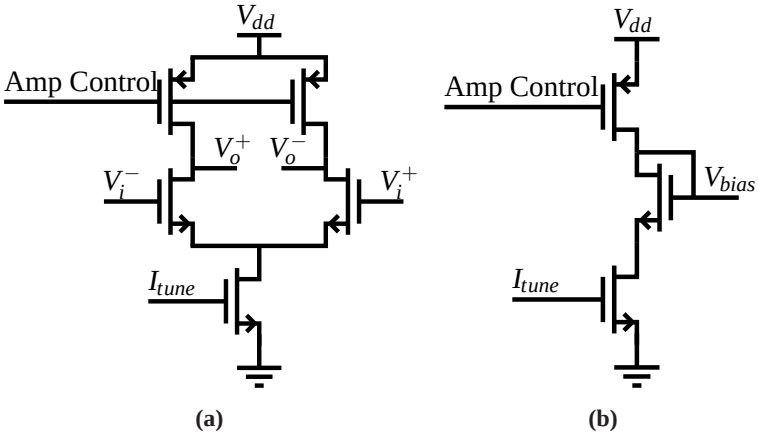


Figure 5.5: *Transistor level ring oscillator circuits. a) Differential amplifier stage used in the ring oscillator b) Bias copy circuit.*

rate of 50kbps and FSK frequency deviation of 250kHz the maximal tolerable phase noise is -70dBc/Hz at a 1MHz offset, see section 3.5. Based on this high phase noise tolerance and the model results presented in section 4.2.5, a ring oscillator is chosen.

The proposed receiver has a zero-IF architecture. Therefore, both an I and Q output are needed. Additionally, differential outputs are needed for the passive mixer. To generate differential quadrature signals, four oscillator stages are used, as is shown in figure 5.4, and a single amplifier stage is depicted in figure 5.5a. The load of the differential amplifier comprises two transistors which are biased

deep in the triode region.

The frequency is tuned by changing the tail current, which enables a very large tuning range. There is a big drawback of this solution: the amplitude changes with the frequency. An amplitude feedback loop is used to counter the amplitude variation, which is also shown in figure 5.4. A scaled bias circuit, equivalent to the amplifier stage, is added. The bias copy circuit depicted in figure 5.5b is used to sense the bias level instead of directly sensing the dc level of the LO itself, because the input of the opamp would load the LO which is very sensitive due to the ultra low power consumption. The external reference is compared with the copied bias and the load is tuned to reduce the amplitude modulation.

5.1.3 IF Amplifier

In section 5.1.1 the optimal load impedance was derived to be 2.3kΩ for this design. This is much lower than the input impedance at the gate of a transistor. Therefore, a common-gate input stage is chosen which is depicted in figure 5.6a. The second stage consists of two single-ended common source stages, one of which is depicted in figure 5.6b. The two stages are connected by a series capacitor, which introduces high pass filtering used to remove DC offset and low frequency 1/f noise as was discussed in section 3.3.

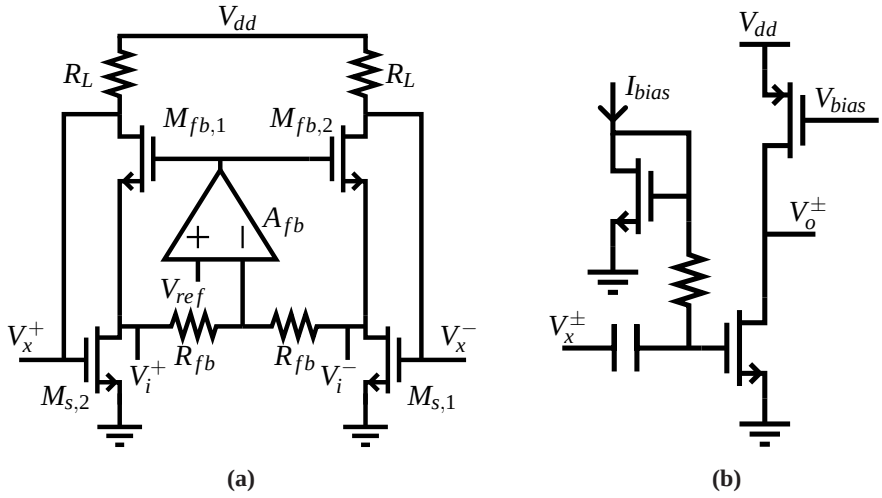


Figure 5.6: *Transistor implementations of the IF amplifier. a) Common gate input stage b) One of the two single-ended common source output stages.*

The common mode feedback loop in the first stage containing the feedback amplifier A_{fb} and both transistors $M_{fb,1}$ and $M_{fb,2}$ stabilizes the biasing with respect to the input port, which is directly connected to the passive mixer. Moreover, it is important that the biasing point is well defined, because this will affect the switching behavior of the transistors in the passive mixer.

Without the voltage to current feedback implemented by transistors $M_{s,1/2}$, the differential input impedance is

$$R_{in} = 2\frac{1+gds_{fb}R_L}{gm_{fb}+gds_{fb}}.$$

The input impedance is highly dependent on the trans-conductance *gm* of the feedback transistor M_{fb}, which dependents linearly on the bias current. To reduce the bias current needed for the 2.3kΩ input impedance a voltage to current feedback loop consisting of $M_{s,1/2}$ is implemented; the feedback reduces the input impedance. Assuming the feedback resistance R_{fb} and the drain-source output impedance of $M_{s,1/2}$ are negligible compared to the input impedance, the differential input impedance becomes

$$R_{in} = 2\frac{1+gds_{fb}R_L}{gm_{fb}+gds_{fb}}\frac{1}{1+gm_sR_L}.$$

The voltage gain of the first stage is equal to

$$G_v = \frac{\left(gm_{fb}+gds_{fb}\right)R_L}{1+gds_{fb}R_L}.$$

Because a wideband-FSK modulation is used, most of the signal power is not concentrated round DC, hence bandpass filtering is implemented by means of AC coupling between the two amplifier stages.

5.2 Measurement Results

The chip was fabricated in 90nm CMOS and packaged in a standard QFN56 package which was placed on a PCB. Figure 5.7 shows the PCB setup including an on-chip measurement buffer capable of driving a 20pF off-chip capacitance and a differential to single-ended converter. The LC matching circuit is placed on the PCB to match the receiver input to a 50Ω source.

The die photo is shown in figure 5.8. Besides the receiver front-end, also stand-alone versions of the IF amplifier and the LO were taped-out. Therefore, the amplifier and oscillator performance could be measured separately.

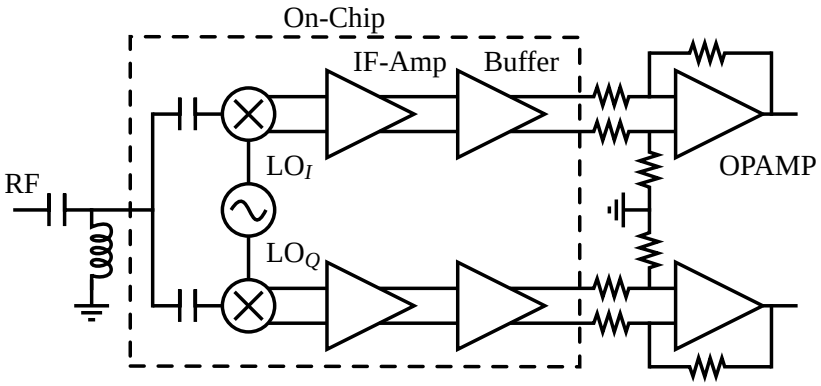


Figure 5.7: *Receiver measurement setup including the on-chip measurement buffer and off-chip opamp measurement circuit.*

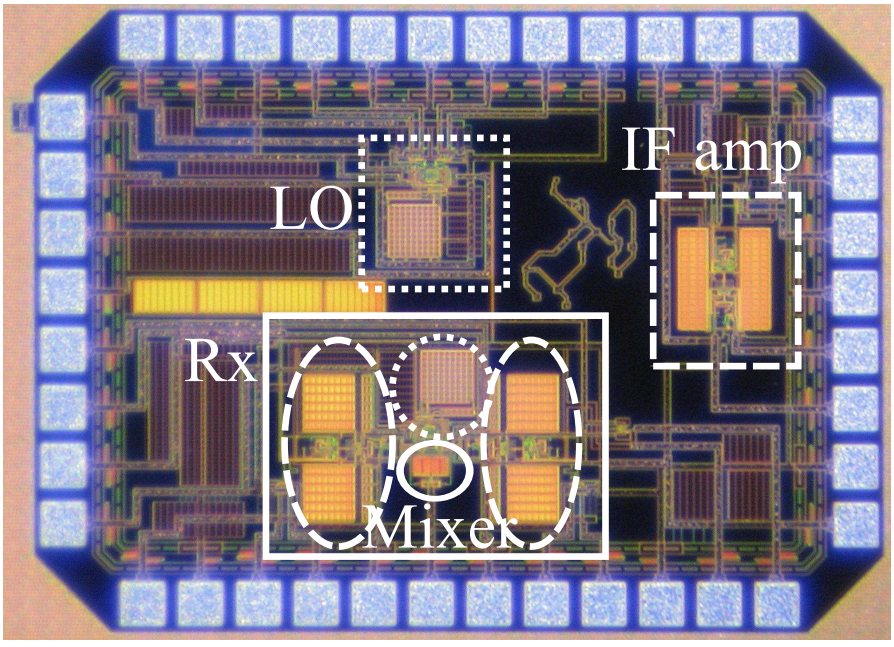


Figure 5.8: *Die photo, with: IF amplifier (dashed line), local oscillator (dotted) and the complete receiver front-end.*

5.2.1 LO Measurements

Figure 5.9 shows the measured LO tuning range and the corresponding power consumption, which includes the LO buffers. The power consumption increases almost linearly with the oscillation frequency. The measured amplitude error between the I and Q outputs is less than 2% between 350MHz and 1100MHz and the phase error is less than 7 degrees.

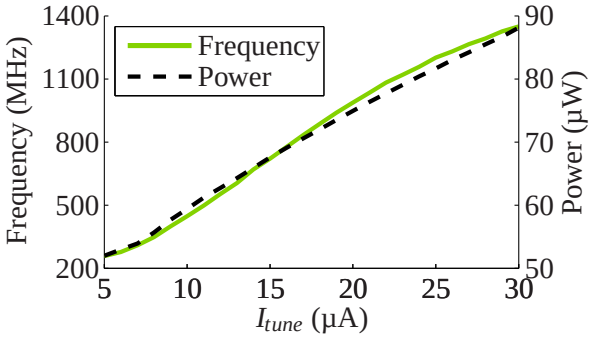


Figure 5.9: *Oscillator tuning range and power consumption of the VCO core including the LO buffers and amplitude control loop.*

The phase noise was estimated by measuring the oscillator jitter using the phase noise and jitter model presented in section 3.4.2. At a frequency offset of 1MHz the phase noise was estimated to be -71dBc/Hz. This is higher than the simulated phase noise of -75dBc/Hz @ 1MHz offset, see figure 5.10. The phase noise model was presented in section 4.2.5. The difference between the simulated and measured phase noise can be caused by incorrect modeling of the transistor 1/f

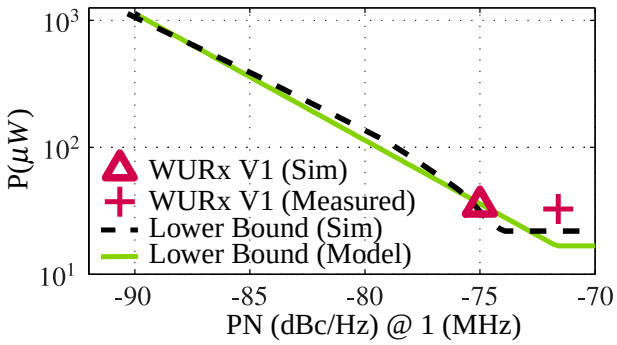


Figure 5.10: *Measured (+) and simulated (triangle) phase noise of the WURx V1 oscillator. Additionally, the modeled and simulated lower bound of the rind oscillator phase noise are depicted.*

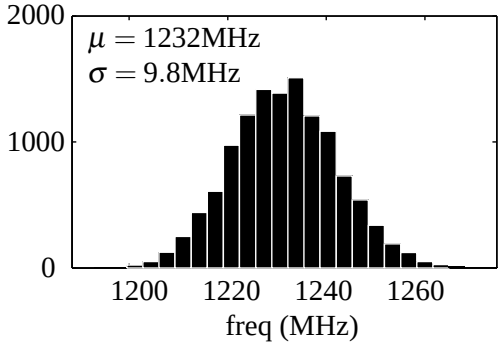


Figure 5.11: *Measured instantaneous oscillator frequency.*

noise or a higher noise contribution of the amplitude feedback loop: the noise produced in the feedback loop is fed into a common-mode node and can appear at the differential output because of mismatches in the differential oscillator core. It should also be noted that the phase noise is estimated using the measured LO jitter, which is less accurate than a direct phase noise measurement.

Figure 5.11 shows a histogram of the measured instantaneous oscillator frequency when it is tuned to 1232MHz. From the plot it is clear that the instantaneous frequency has a Gaussian distribution with standard deviation σ=9.8MHz.

5.2.2 Amplifier Measurements

The measured and simulated transfer function of the IF amplifier are depicted in figure 5.12. The simulated transfer function corresponds well to the measure-

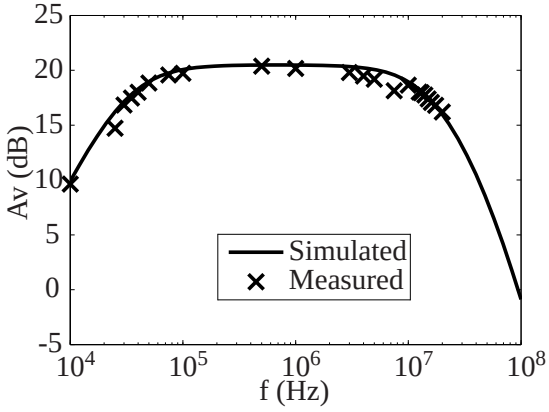


Figure 5.12: *Measured and simulated IF amplifier transfer function.*

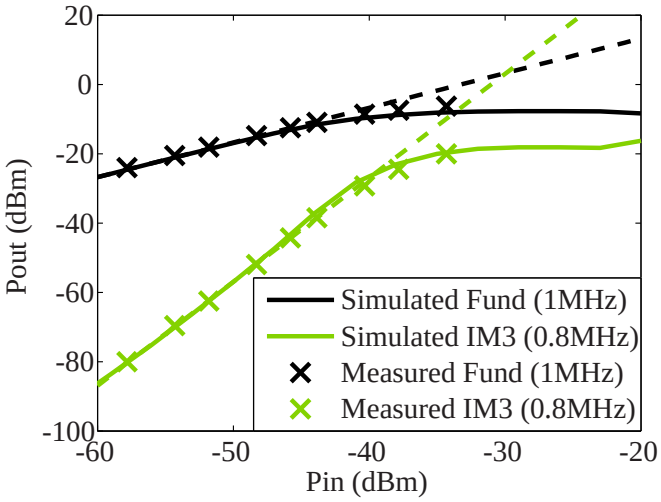


Figure 5.13: *This figure shows the measured and simulated IM3 and fundamental IF amplifier output tones given the two input tones at $f_1 = 1MHz$ and $f_2 = 1.2MHz$. The measured fundamental frequency is 1MHz and the measured IM3 component is located at 800kHz. The measured input referred IIP3 is P_{IIP3} = -29.8dBm.*

ments.

The linearity is measured by measuring both the 1dB input compression point P_{1dBc} and third order input interception point P_{IIP3}. At the input of the amplifier two tones at 1MHz and 1.2MHz are applied. Subsequently the power of both tones is increased and the power of the fundamental output tone at 1MHz and of the third order inter-modulation component at 800kHz are measured and plotted in figure 5.13. From the figure it can be concluded that the measured and simulated IM3 and fundamental components and therefore IIP3 results match closely. The input referred 1dB compression point is P_{1dBc} = -38.9dBm and the input referred third order interception point is approximately P_{IIP3} = -30dBm.

5.2.3 Receiver Front-End Measurements

Figure 5.14 shows the quality of the input match of the receiver front-end. The optimum frequency point is shifted to higher frequencies compared to simulations. This is because of an over-estimation of the parasitic capacitances in the simulations and component mismatches.

A summary of the measured receiver front-end specifications is given in table 5.1. Note that the measured front-end linearity is higher than the linearity of the IF

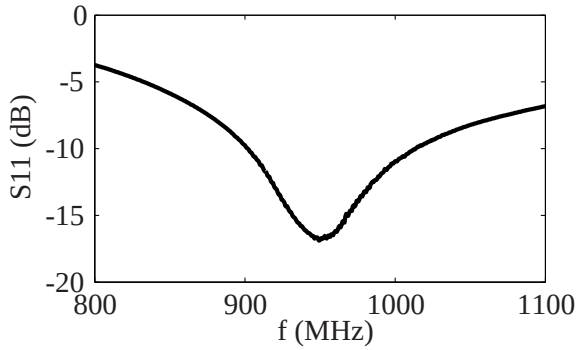


Figure 5.14: *Measured S11 of the mixer-first receiver front-end.*

amplifier, because the first stage is a passive mixer which has a power loss. This is also the reason the noise figure is relatively high. To overcome the phase noise, the frequency deviation was increased to 2.5MHz to obtain a BER of 10^{-3}. Matlab was used to demodulate the received signal and measure the BER.

Table 5.1: *Receiver front-end measurement summary.*

Technology		90nm CMOS
$\boldsymbol{V_{dd}}$ **(V)**		0.75
Power (µW)	WURxV1	126
	IF amplifier	2 x 24
	LO	77 (@ 900MHz)
Freq. (MHz)		700-1000
$\boldsymbol{P_{1dBc}}$ **(dBm)**	WURxV1	-30
	IF amplifier	-38.9
IIP3 (dBm)	WURxV1	-21
	IF amplifier	-29.8
NF (dBm)		25
$\boldsymbol{P_{sens}}$ **(dBm)**		-65
$\boldsymbol{R_b}$ **(kbps)**		50

5.3 Comparison with Literature

The presented front-end is compared against the literature and the key performance parameters are given in table 5.2, where the sensitivity was obtained with a BER of 10^{-3} and the reported power consumption includes the local oscillator. The other front-ends are chosen because they all use FSK modulation and have very low power consumption. It is clear that the presented receiver has a much lower power consumption than the other receivers. The power consumption of the presented oscillator including LO buffers is only 77µW at 900MHz, which is much lower than the oscillators presented in literature. However, the linearity and noise figure of [9, 13, 18] are better, showing a trade-off between power consumption and linearity. Especially [9] has a much higher linearity at the cost of a high power consumption, which makes the receiver better suited for high performance applications. Additionally, it is clear that the low supply voltage of 0.25V used in [16] leads to a low 1dB compression point and low IIP3. The increased noise figure of the reported receiver can be explained by the absence of the LNA and the very low power consumption of the VCO.

Most receivers reported in table 5.2 require only one voltage supply, except for [19]. Having multiple power supplies has the disadvantage that additional DC-DC converters are needed, which decreases the power efficiency of the system.

The reported bit rates roughly range from 50kbps to 300kbps, with the exception of [14]: this receiver has a bit rate of 5Mbps, and has the best energy efficiency (nJ/bit). However, the receiver injects the received RF signal into its local oscillator at the cost of lower linearity, making it a better alternative for low power high bit rate applications operating in a licensed band, where the level of interference is very low.

Table 5.2: *Performance summary and comparison.*

REF	WURx V1	[9]	[12]	[13]	[14]	[15]	[16]	[18]	[19]
CMOS	90nm	130nm	180nm	130nm	180nm	180nm	130nm	180nm	180nm
Power (µW)	126	1920	500	750	420	490	352	11700	1088
V_{dd} (V)	0.75	1.2	1.0	0.4	0.7	0.7	0.25	1.8	0.7 & 1.0
Freq. (MHz)	700-1000	825-983	2400	1950-2380	920	398-408	1500-1650	760-1000	2220-2450
NF (dBm)	25	10	10.1	5.1	-	-	7.2	19	10.1
P_{1dBc} (dBm)	-30	-10	-31	-17.5*	-34†	-	-48	-15	-31
IIP3 (dBm)	-21	-	-	-7.5	-	-	-48	-	-
P_{sens} (dBm)	-65	-83	-	-	-73	-68	-	-	-
R_b (kbps)	50	45-48	100	300	5000	250	-	-	100
$\frac{P_{DC}}{R_b}$ (nJ/bit)	2.5	40	5.0	2.5	0.084	1.96	-	-	10.9

† The linearity is not directly specified in the paper, but estimated after comparing the reported blocker rejection with the second version of the WURx front-end presented in chapter 6.

* The 1dB compression point is not reported. It is estimated by assuming that the 1dB compression point is 10dB lower than the input referred third order interception point.

It is clear that the optimization targets of the reported receivers are different; the design target of the front-end reported within this chapter was low power consumption, whereas [14] was optimized for low energy per bit and [9] was designed to have better linearity. These different design and optimization targets make it difficult to compare the receivers with each other, since multiple performance parameters have to be taken into account. Moreover, some design parameters are related and can be traded. For example, power consumption and linearity are directly linked: two parallel connected amplifiers consume twice as much power as a single amplifier, but at the same time are twice as linear [60]. To ease the comparison, Figure of Merits (FOM) are used. In a FOM different performance parameters are mapped onto a one-dimensional figure, such that the FOM does not change with design parameter scaling. Ideally a FOM is insensitive to these kinds of scaling; once the FOM of a receiver is known, the circuit can be scaled to trade-off between parameters that are taken into account in the FOM. Therefore, different receivers can be compared using FOMs. However, FOMs also have limitations. At a given application scenario, some performance parameters have more stringent specifications than the others. For example, wake-up receivers should be optimized for low power consumption, instead of very high bit rates.

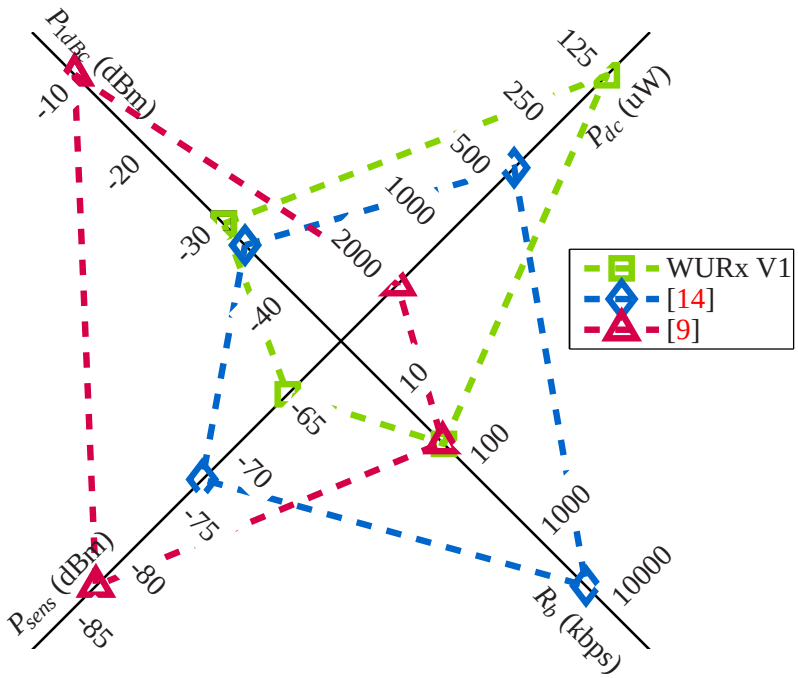


Figure 5.15: *Graphical comparison of reported FSK receivers.*

Another way of comparing receivers is by plotting the performance parameters, like 1dB compression point, power consumption, bit rate and sensitivity, in one radar plot, see figure 5.15. The axes are scaled such that the performance increases when the point moves away from the origin. Moreover the axes are grouped together such that the combination of two neighboring axes give additional information. As was mentioned before there is a clear trade-off between power consumption and linearity; in conventional receivers one is traded for the other. Similarly, the ratio of the power consumption and bit rate ($\frac{P_{DC}}{R_b}$) is a measure of energy efficiency often reported in nJ/bit. The combination of bit rate and sensitivity gives a measure of the noise figure, whereas the combination of the sensitivity and 1dB compression point gives a measure of dynamic range.

By comparing the pointing direction of the "arrow" of different receivers depicted in the same radar-plot their strong points can more easily be compared. For example, the WURx presented in this chapter represented by the green squares in figure 5.15 is pointing in the power consumption direction, i.e. the WURx is geared towards low power consumption at the cost of sensitivity and linearity. Similarly [14] (blue diamond) is optimized for high bit rate and high power efficiency in (nJ/bit) and [9] (red triangle) is optimized for high sensitivity and linearity. Note that the pointing direction can only be compared between different receivers.

5.4 Conclusion

The front-end presented in this chapter uses a mixer-first architecture, and the received signal is amplified at the baseband frequency. Amplification at low frequencies can be performed more power efficiently than amplification at higher frequencies, since the required gain-bandwidth-product at higher frequencies is higher. From the measurement results it is clear that the proposed mixer-first architecture is feasible and reduces the overall power consumption. However, the obtained noise figure was high because a sub-optimal 50% duty cycling was used. Therefore, 25% duty-cycling is used in the second WURx design presented in chapter 6.

The phase noise requirements of the receiver are reduced by means of increasing the FSK modulation index. This is exploited by implementing a low-power ring oscillator; the ring oscillator including the LO buffers only consumes 77µW at an oscillation frequency of 900MHz. The simulated oscillator power consumption is close to the theoretical lower bound presented in section 4.2.1, given the

simulated phase noise. However, the measured phase noise was a few dB higher than expected and limits the minimal BER to 0.1%. If a better BER is required the LO should have a lower phase noise at the cost of higher power consumption.

WURx version 1 was compared against other reported low-power FSK receivers using a radar plot. It gives additional information about the different optimization targets of compared receiver front-ends. By comparing the performance differences the merits of different receivers are observed. Compared to other reported FSK receivers, the power consumption of the proposed WURx was low, at the cost of sensitivity.

CHAPTER 6

RECEIVER FRONT-END VERSION 2

THE goal of the first version of the WURx, described in chapter 5, was to study the mixer-first topology. However, it used a 50% oscillator duty-cycling scheme, while the optimal duty cycle is 25%, see section 4.1. Therefore, in a second version, which is discussed in this chapter, the 25% scheme is implemented. Additionally, an on-chip digital tuning DAC and FSK demodulator are implemented, enabling the implementation of the automatic frequency control loop discussed in section 4.4.

In this chapter the circuit implementation and measurement results of this second version of the WURx are presented. The implementation issues and simulation results are given in section 6.2. In section 6.3 the simulation results are compared to the actual measured data. Additionally, the results are compared to the receivers reported in literature. At the end of the chapter, conclusions are drawn.

6.1 Design Targets

The receiver targets the European 868MHz ISM band and the North-American 915MHz ISM band. Therefore, the DCO should be able to tune to those bands taking into account $\pm 3\sigma$ process variation. On top of that, the receiver should attain a BER lower than 0.1% at a received signal strength of -72dBm and a bit rate of 100kbps, as was discussed in section 3.6.2.

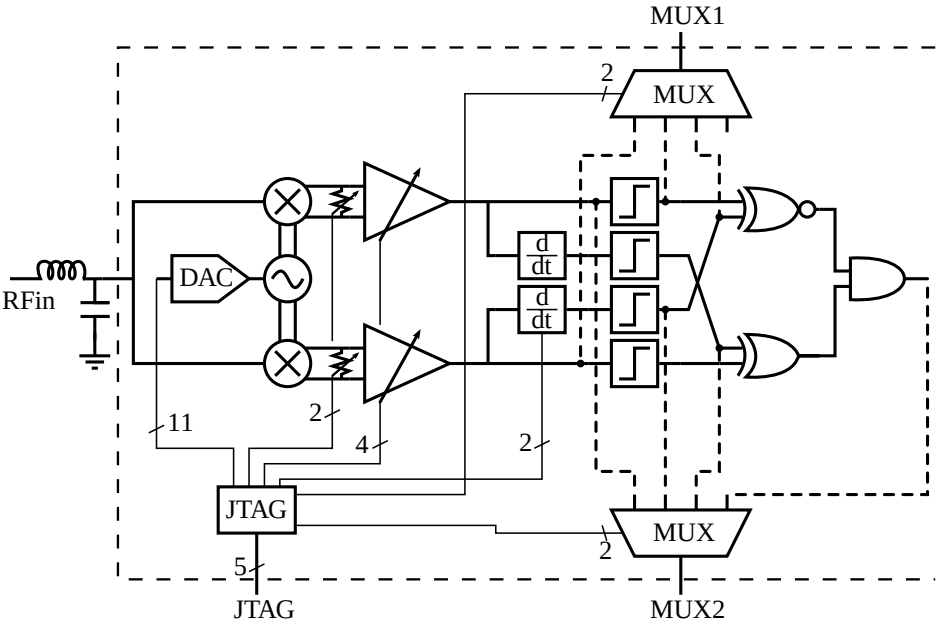


Figure 6.1: *Schematic overview of the WURx architecture. Every block inside the dashed box is implemented on-chip.*

6.2 Implementation

Figure 6.1 shows the block diagram of the WURx architecture. The RF mixer-first front-end is matched to a 50Ω source using an off-chip LC network. The number of required bondpads is minimized by using a serial JTAG interface, which is used for programming the receiver settings. Additionally, two analog multiplexers are placed on the chip to be able to measure the seven different signals listed in table 6.1 using only two bondpads. The analog I and Q signals are digitized using hard-limiters as is discussed in section 3.4.3.

Table 6.1: *Available signals at the output of the on-chip analog multiplexers.*

Code	MUX 1	MUX 2
00	Digital Q	Digital I
01	Digital $\frac{dI}{dt}$	Digital $\frac{dQ}{dt}$
10	-	Demodulator output
11	Analog I	Analog Q

In this section emphasis is placed on the design and simulation of the low-power front-end comprising a passive mixer (section 6.2.1), digital controlled oscillator (section 6.2.2), variable gain amplifier (section 6.2.3), FSK demodulator (section 6.2.4) and Automatic Frequency Control loop (section 6.2.5). The on-chip JTAG interface will not be discussed in detail.

6.2.1 Passive Mixer

Figure 6.2 depicts the transistor implementation of the passive mixer described in section 4.1. The transistors are relatively small to decrease the load and therefore the power consumption of the local oscillator buffer; their W/L is 12µm / 40nm. This is the only circuit where the small 40nm gate length is used. In other

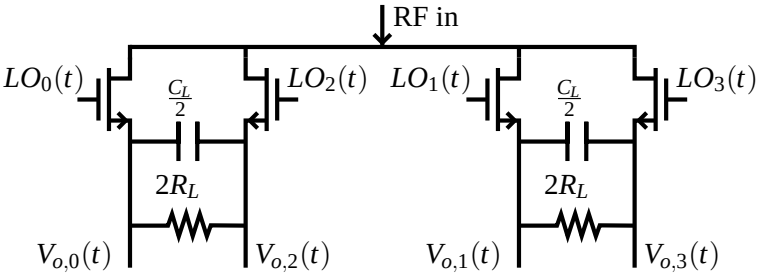


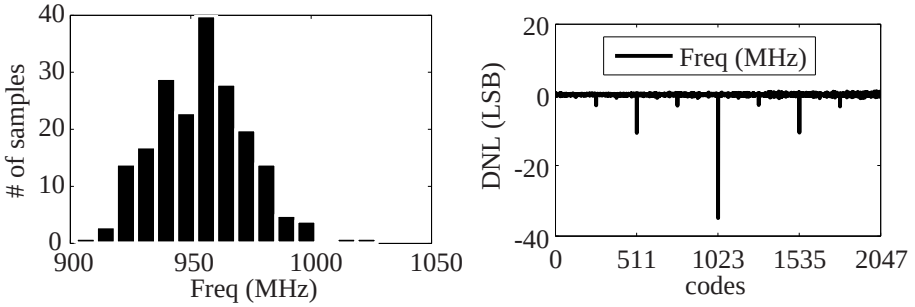
Figure 6.2: *Implementation of the passive mixer.*

subcircuits of the WURx front-end longer devices are used to either decrease the process spread or reduce the flicker noise.

6.2.2 Local Oscillator

Given the power consumption versus phase noise trade-off discussed in section 4.2 a ring oscillator is chosen. The digitally controlled oscillator (DCO) tuning range needs to be large enough to cover both the European 868MHz and North-American 915MHz bands and 3σ process variation. The process variation is simulated using Monte-Carlo analysis and depicted in figure 6.3a. The simulated standard deviation σ of 200 runs is 20MHz. Combining the two frequency bands and 3σ variation the tuning range needs to be between 808MHz and 975MHz.

Figure 6.4 shows the complete DCO. The ring oscillator is digitally controlled by an 11-bit R-2R DAC topology. However, the resistors are replaced by equally-sized transistors, as was proposed by [61]. An R-2R DAC is used, since it needs



(a) *Monte Carlo simulation of the DCO frequency.*

(b) *Post-simulation results of the differential non-linearity (DNL) of the DCO oscillation frequency.*

Figure 6.3

less area than a switched-current source topology. Process variations may lead to 'gaps' in the DCO tuning range, which is solved by designing an overlap [62]. This overlap in the tuning range is not a problem when the tuning algorithm does not compare two consecutive measurement samples. The simulated differential

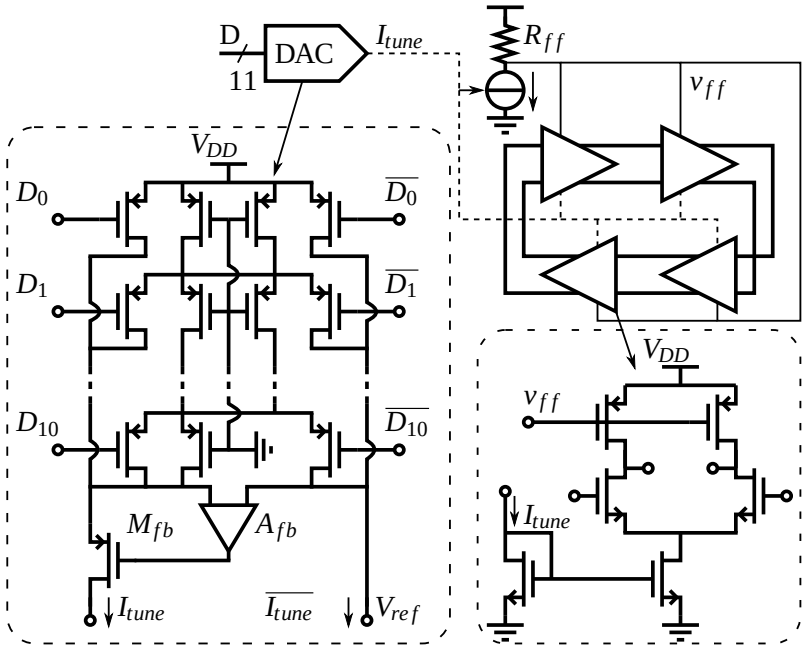


Figure 6.4: *Overview of the complete digitally controlled oscillator (DCO) excluding the output buffer.*

non-linearity (DNL) of the DCO oscillation frequency including the effects of the layout parasitics is depicted in figure 6.3b.

The feedback amplifier A_{fb} together with the output MOST M_{fb} act as a current-conveyer. They match the source voltage of M_{fb} to V_{ref} and increase the output impedance of the current DAC. This leads to a more linear relationship between the DCO tuning code and tuning current, since the tuning current is less dependent on the source drain voltage of the current mirror.

The DAC changes the tail current to tune the oscillation frequency. However, like in version one, the changing tail current also changes the signal amplitude, which is unwanted. To combat the amplitude variation, a feed-forward loop consisting of I_{tune}, R_{ff} and the P-MOST load is used. The post-layout simulation results of the oscillation frequency and amplitude are depicted in figure 6.5a and 6.5d. The tuning range is large enough to cover the simulated 3σ process mismatch. The power consumption increases linearly with the oscillation frequency as is visible

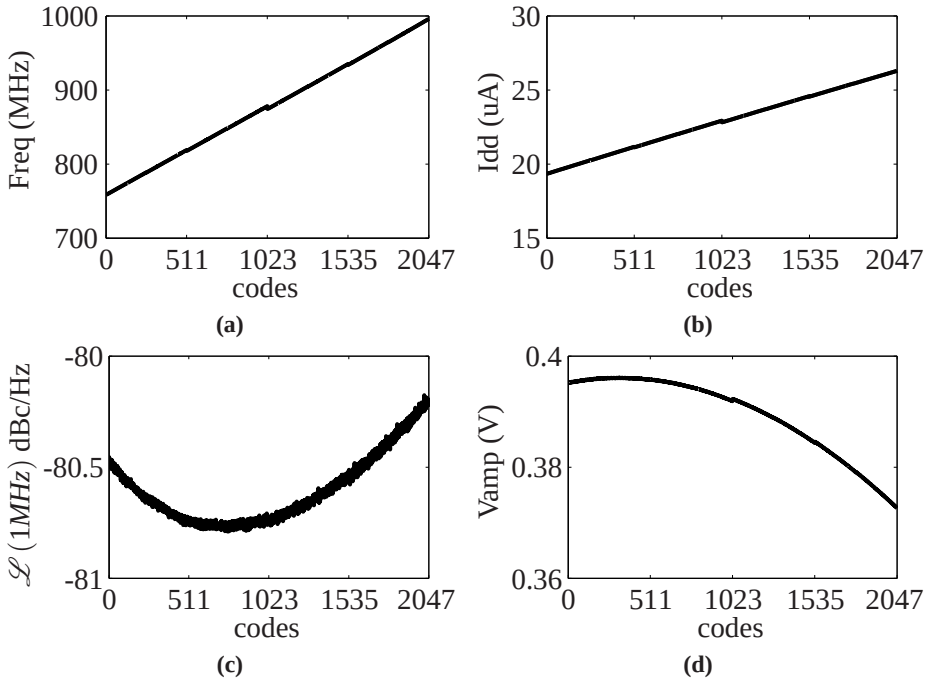


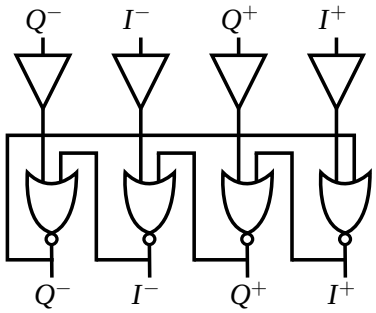
Figure 6.5: *Post-layout simulation results of the complete digitally controlled oscillator as a function of the 11 bit DCO code. The simulated parameters are a) frequency b) current consumption of one oscillator stage c) phase noise d) oscillation amplitude.*

in figure 6.5b. Moreover, the amplitude and phase noise are relatively constant over the tuning range, see figures 6.5c and 6.5d respectively. The phase noise is dependent on the signal amplitude; larger signal amplitude leads to lower phase noise as is expected.

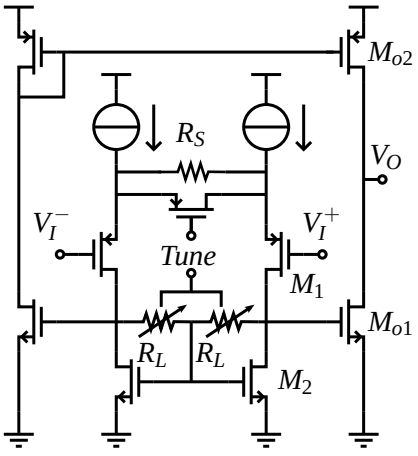
The four stage ring oscillator delivers the in-phase and quadrature-phase signals needed by the mixer. However, the DCO signal still has 50% duty cycle instead of the required 25% duty cycle, see section 4.1.1. This is corrected by the DCO buffer circuit, shown in figure 6.6a. The first stage minimizes the DCO load and frequency pulling, and the second stage is used to ensure a non-overlapping 25% duty cycle output.

6.2.3 Variable Gain Amplifier

The first amplifier stage of the front-end is present at the output of the passive mixer, as is depicted in figure 6.1. Figure 6.6b shows the implementation of the variable gain amplifier (VGA). Its noise performance is important since it is the first gain stage. Moreover, the low frequency 1/f noise needs to be very low since the receiver has a zero-IF architecture. To reduce the 1/f noise the transistors in the differential input stage are large: $\frac{W_1}{L_1} = \frac{38.4\mu m}{1.5\mu m}$ and $\frac{W_2}{L_2} = \frac{19.2\mu m}{4\mu m}$. The inversion



(a) *DCO buffer with 25% duty cycle output.*



(b) *Variable Gain Amplifier circuit, with biasing circuit omitted.*

Figure 6.6

coefficient

$$\mathrm{IC} = \frac{I_D}{2n\mu C_{ox}\left(\frac{W_{eff}}{L_{eff}}\right)V_T^2}$$

of the input transistors M_1 and M_2 is 2.5 and 10 respectively at a bias current of $25\mu A$.

The VGA gain is tuned by switching between three different load impedances R_L, changing the voltage gain between 29dB and 41dB with 6dB steps. As a second step the source degeneration can be turned on to decrease the gain by 6dB and increase its linearity. The benefit of switching the load impedance of the first stage is that the biasing point does not change and the linearity increases as the gain decreases. On the other hand, the noise contribution of the second stage increases as the gain decreases. However, when the low gain mode is selected the noise performance is less important than the linearity since the input power is larger.

Since the VGA is the first amplifier stage in the receiver chain, as depicted in figure 6.1, not only its gain and power consumption are important, but also its noise figure. Especially, the low frequency 1/f noise is a potential problem when the bias current is low. Therefore, the transistor length and area are as large as possible. Furthermore, the gain in the first stage is high to decrease the noise contribution of the second stage.

6.2.4 Demodulator

The implementation of the Digital Cross-Differentiate Multiply (DCDM) demodulator, which was already discussed in section 4.3, is presented in this section. Figure 6.7 shows the block diagram of the FSK demodulator. Note that the absolute phase of the in-phase (I) and quadrature-phase (Q) signals is unknown. However, to demodulate FSK signals not the absolute phase, but the phase change over time (frequency) is of concern. Figure 6.7 also shows the implementations of the analog time differentiator and limiter circuits. Both circuits are AC-coupled to remove low frequency 1/f noise and bias offsets. The limiter is self-biased using a large pseudo-resistor, which is implemented by a large transistor. The large resistance is set by the leakage current of the transistor. Therefore, the resistance is very sensitive to process variation. However, the value of the resistor is less important, as long as the cut-off frequency set by the RC time of the pseudo-resistor and parasitic capacitance is much lower

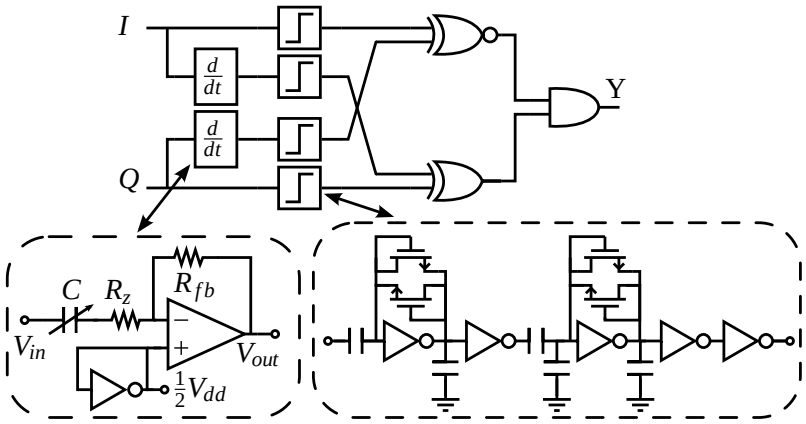


Figure 6.7: *FSK demodulator block diagram together with the circuit implementations of the limiter and time-differentiator.*

than the signal frequency. Additionally, the series resistance R_z is added to the time-differentiator circuit to increase the phase margin and ensure stability.

Alternatively, the most simple zero-IF FSK demodulator consisting of only one D-type flip-flop can be used. It is named the "Vance demodulator" after its inventor [63]. A simplified block diagram of the Vance demodulator placed in parallel to the DCDM demodulator is depicted in figure 6.8. The grayed out blocks show the additional blocks needed for the DCDM demodulator. It is clear that the Vance demodulator is less complex. First the received RF input signal is down-converted to zero-IF, and an in-phase I and quadrature Q signal are ob-

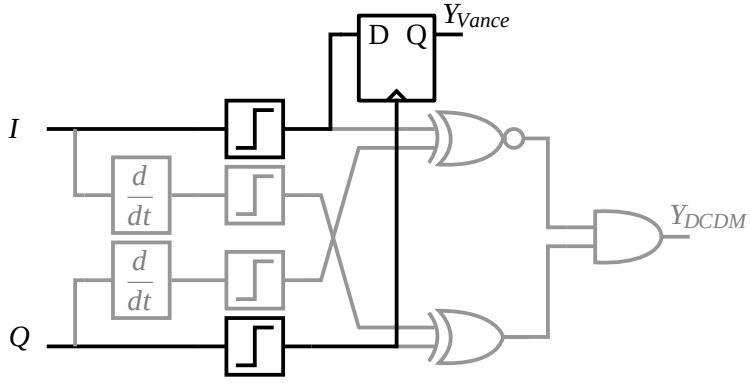


Figure 6.8: *Simplified block diagram of a Vance FSK demodulator placed in parallel to the DCDM demodulator.*

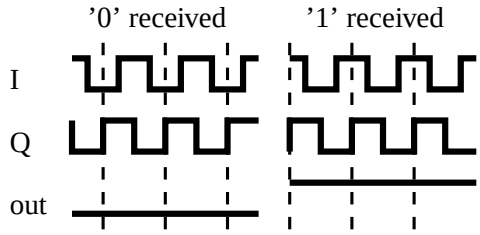


Figure 6.9: *Receiver I, Q and demodulator output signals in case a binary '0' or '1' are received.*

tained. Assuming no noise and no frequency offset are present, the analog I and Q signals for bit n are written as

$$I(t) = A\cos(a_n \Delta\omega t)$$
$$Q(t) = A\sin(-a_n \Delta\omega t)\ ,$$

where $\Delta\omega$ is the frequency deviation and $\pm$ represents a binary '0' ($a_n = -1$) or '1' ($a_n = +1$). The I does not change when the transmitted bit changes, but the Q signal is shifted by 180deg when a_n changes. After the frequency down-conversion both I and Q are hard limited and fed into a D-type flip-flop. I is used as the data signal and Q as the clock. Note that switching them only inverts the demodulated binary bit stream.

The principle of operation can be explained by figure 6.9. The I signal is sampled at the rising edge of Q. In case a binary '0' is received the I signal is low at every rising edge of Q and the output of the demodulator is zero. However, when a binary '1' is received the clock sign changes and the output of the demodulator is one.

The noise is not shaped in the Vance demodulator as it is in the DCDM demodulator. Therefore, the Vance demodulator will perform worse when the modulation index is high. On the other hand the Vance demodulator has the benefit of simplicity.

6.2.5 Automatic Frequency Control Loop

When there is a frequency offset between the transmitter and the local oscillator, bit errors are introduced. When the LO oscillates at a too low (high) frequency the demodulator only produces ones (zeros). This can be used to calibrate the local oscillator and track frequency shifts, as was discussed in section 4.4.

The automatic frequency control loop has been implemented on a Xilinx Spartan 3E FPGA and written in VHDL. In this section the digital circuit implementations are presented which could be used in an ASIC implementation. Moreover the design constraints and design methodology are presented in this section.

Moving Average Filter

The output of the demodulator is sampled and fed into a moving average filter. The integration time T_{mavg} of the moving average filter has to be larger than the bit period T_b, otherwise the loop can not distinguish between data and frequency offset. Furthermore, it is convenient to integrate over an integer number of bits N_{bits}. Taking into account the sample time T_s, the number of moving average filter taps is

$$N = N_{bits}\frac{T_b}{T_s}.$$

Using the demodulator function given by equation (4.29), the output of the moving average filter is computed as follows

$$Y_{mavg}[k] = \frac{N}{2} + \frac{1}{2}\begin{cases} \sum_{n=0}^{N-1} a_{k-n} & \text{if } \left|\omega_{off}\right| < \Delta\omega \\ N\,\text{sign}(\omega_{off}) & \text{if } \left|\omega_{off}\right| \geq \Delta\omega \end{cases}$$

In other words, the output of the moving average filter is equal to the number of '1' samples present in the filter.

The moving average filter implementation is depicted in figure 6.10 and consists of an N-stage shift register, an up-down counter and count logic. The reset signals

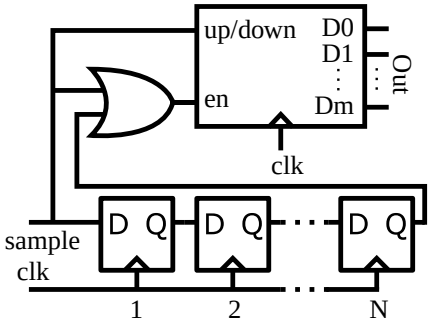


Figure 6.10: *Implementation of the N-tap moving average filter.*

Table 6.2: *Counter logic for the moving average filter. A logic '0' ('1') decreases (increases) the counter.*

new	old	up/down	enable
0	0	X	0
1	1	X	0
0	1	0	1
1	0	1	1

are not shown for readability. A new sample is inserted in the shift-register and is compared with the last sample of the shift register. When the samples are equal nothing happens. On the other hand, when they differ the counter is activated, see table 6.2. Less area, gates and power are needed by the counter approach instead of the straightforward FIR implementation. Additionally, the filter output is present as parallel data.

The system cannot distinguish between N_{bits} consecutive 0's (1's) and a negative (positive) frequency offset. Therefore, a maximal run length N_{max} must be set. The system can distinguish between a long sequence of equal bits and frequency offset, when the filter length is larger than the maximal number of consecutive bits: $N_{bits} \geq N_{max} + 1$. Possible situations for a AFC with $N_{max} = 7$ and $N_{bits} = 8$ are given in table 6.3. The situations (a) and (c) can only appear in case of a frequency offset and/or bit errors. In (a) the receiver LO frequency is lower than the transmitter frequency and the output of the demodulator contains only ones, whereas in (c) the LO frequency is too high and only zeros are present at the output of the demodulator. On the other hand, in situation (b) there either is a frequency offset between the transmitter and receiver in combination with bit errors or valid data is received. In (b) the filter output is bound between 1 and

Table 6.3: *Possible moving average filter outputs and filter memory given $N_{max} = 7$ and $N_{bits} = 8$ and assuming the sample frequency is equal to the bit rate.*

Situation	Y_{mavg}	Filter taps
(a) LO frequency too low	8	11111111
(b) Valid data	7	11111110
	...	...
	1	10000000
(c) LO frequency too high	0	00000000

N_{max}. Thus the LO value should not be changed when the output of the filter is within this range. The detection of the cases (a, b and c) is taken care of by the frequency offset detector discussed in the following section.

Frequency Offset Detector

The frequency offset detector consists of two parallel detectors with hysteresis, one for detecting positive frequency offset and one for detecting the negative frequency offset. The input-output relationship is depicted in figure 6.11a. The

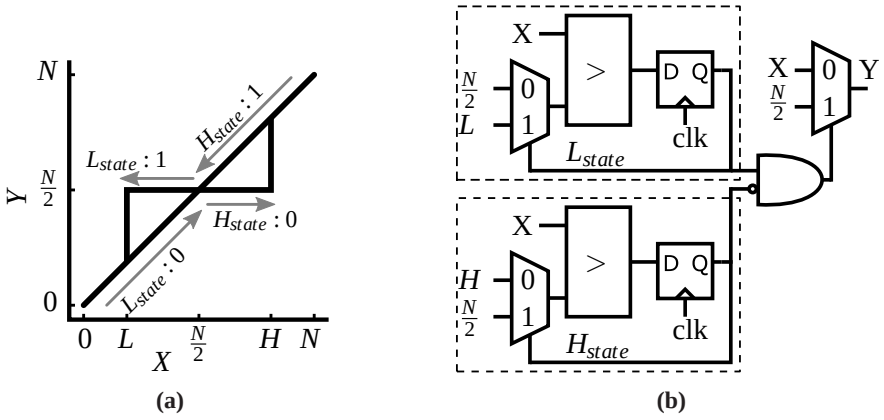


Figure 6.11: *a) Offset detector input-output relationship. b) Frequency offset detector implementation, the circuits within the dashed boxes are the schmitt-triggers.*

arrows give the paths from high to low and low to high input values. Assuming no bit errors occur due to noise, the low threshold should be set to $L = \frac{T_b}{T_s}$ and the high threshold to $H = N - \frac{T_b}{T_s}$, so that the AFC loop does not react on the data stream. However, in the practical case that noise is present, bit errors may occur and the AFC loop should not change the LO value because of them. Therefore, the moving average filter length should be increased and the low L and high threshold H adjusted.

Figure 6.11b shows the frequency offset detector implementation, where the two schmitt-triggers are depicted inside the dashed boxes. The schmitt-trigger stores the signal direction as an internal state. When the input signal X trips over the threshold, the state and threshold value change.

Parameter Values

The AFC loop is implemented off-chip in an FPGA for debugging purposes. Choosing A to be a negative power of 2 leads to an efficient implementation, since the gain can then be implemented by a bit shift instead of a full division operation. Furthermore, the oversampling ratio, i.e. $\frac{T_b}{T_s}$, should be an integer. The on-chip JTAG interface limits the sample rate to 125ksps. Therefore a bit rate of 62.5kbps can be achieved with an oversampling-ratio of 2. The maximal number of consecutive 0's or 1's (N_{max}) is chosen to be 7.

The boundary on the gain was given by (4.30), and is copied below for convenience,

$$A < \frac{4.5}{N^2} \frac{2\Delta\omega}{K_{dco}}$$
$$N \geq (N_{max}+1)\,\frac{T_b}{T_s}.$$

The FSK frequency deviation is $\Delta\omega = 2\pi \times 5\text{MHz}$ and DCO gain $K_{dco} = 2\pi \times 71.1\text{kHz}$. Table 6.4 summarizes the AFC loop parameters and the maximal slew rate in MHz/ms.

Table 6.4: *Parameters used in the FPGA automatic frequency control loop implementation.*

A	**N**	**R$_b$**	**F$_s$**	**max SR**
2^{-2}	32	62.5 kbps	125 ksps	35.55 MHz/ms

6.3 Receiver Front-End Measurements

Two test chips were fabricated in a 40nm CMOS process and packaged in a QFN48 package and mounted on a four layer FR-4 PCB. The first tape-out of the front-end, version WURxV2.0, had an additional DCO buffer to measure the oscillation frequency and phase noise. However, because of area limitations the DCO buffer was only present at one of the four DCO phases, causing a DCO imbalance. Consequently, not every switch in the mixer was fully switching, because of the additional parasitics in the DCO buffer phase. This was partly elevated by increasing the supply voltage of the DCO buffer between the DCO and mixer. The higher supply voltage leads to higher current consumption and

Table 6.5: *Differences between the WURx front-end versions WURxV2.0 and WURxV2.1.*

	WURxV2.0	**WURxV2.1**
DCO measurement buffer	Included	Excluded
Additional Vance demodulator	Excluded	Included
Normalized DCO buffer size	1	4

switching speed. A second version of the WURx front-end without the additional DCO buffer, version WURxV2.1, was taped-out later to verify the performance of the front-end. The differences between the two front-end versions are summarized in table 6.5. The biggest difference in WURxV2.1 was the exclusion of the additional DCO buffer and the added Vance FSK demodulator.

The DCO buffer of WURxV2.0 requires a larger supply voltage (1.2V), than expected (1.0V) due to the added DCO measurement buffer as stated before. The layout mistake added additional parasitic capacitance, decreasing the switching speed. Front-end WURxV2.0 consumes 382.5µW from a 0.8V source, except for the DCO buffer. The total power consumption of WURxV2.1 is only 329.6µW.

Table 6.6: *Measured receiver power consumption and supply voltage divided per sub-block. The values are given in V_{dd} (V) / Power (µW).*

Sub-circuit	Total	DCO	DCO buffer	VGA+Demodulator
WURxV2.0	382.5	0.8 / 116.3	1.2 / 142.2	0.8 / 134.0
WURxV2.1	329.6	0.8 / 119.1	1.0 / 122.5	0.8 / 88.0

Table 6.6 gives the measured power consumption. The VGA and demodulator share the same supply and their power can not be measured separately. Furthermore, the reported power consumption of the DCO was measured at the center of the tuning range. The power consumption of the DCO scales linearly with the oscillation frequency, see sections 4.2.3 and 6.3.2. The power consumption of the off-chip AFC loop was estimated using the Xilinx ISE Design suite to be roughly 10µW.

Besides the power consumption, also the I/Q imbalance is improved in WURxV2.1. Especially the gain imbalance is considerably reduced. Table 6.7 shows the gain and phase imbalance, measured at the baseband outputs, between the I and Q paths for both WURx versions. Although wideband FSK modulation is insensitive for I/Q imbalance as discussed in section 3.5.2, the large gain

Table 6.7: *Measured I/Q imbalance of both WURx versions.*

Sub-circuit	Gain imbalance (dB)	Phase imbalance (deg)
WURxV2.0	17	9
WURxV2.1	1.5	7.8

imbalance in WURxV2.0 will cause a slight increase in the BER.

The measured S11 for both front-end versions is shown in figure 6.12. The S11 is below -10dB between 740MHz and 897MHz for WURxV2.0 and between 745MHz and 950MHz for WURxV2.1. The input matching frequency of WURxV2.0 was lower than targeted (868-915MHz), because the PCB and SMA connector parasitics were wrongly estimated. For the second tape-out the estimation was improved and the input matching was much better. The minimal S11 measured was -67dB. Another difference is that the LO feed-through to the RF input was much larger for WURxV2.0, which explains the irregularity at the DCO frequency of 868MHz. At the RF input the oscillator signal is measured to be -71dBm. In the second version the oscillator signal was not visible in the S11 measurement. The worse isolation in WURxV2.0 is caused by the imbalance between the oscillator phases.

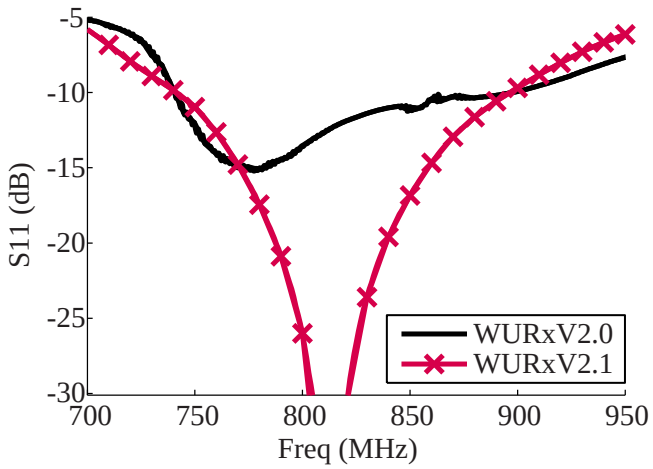
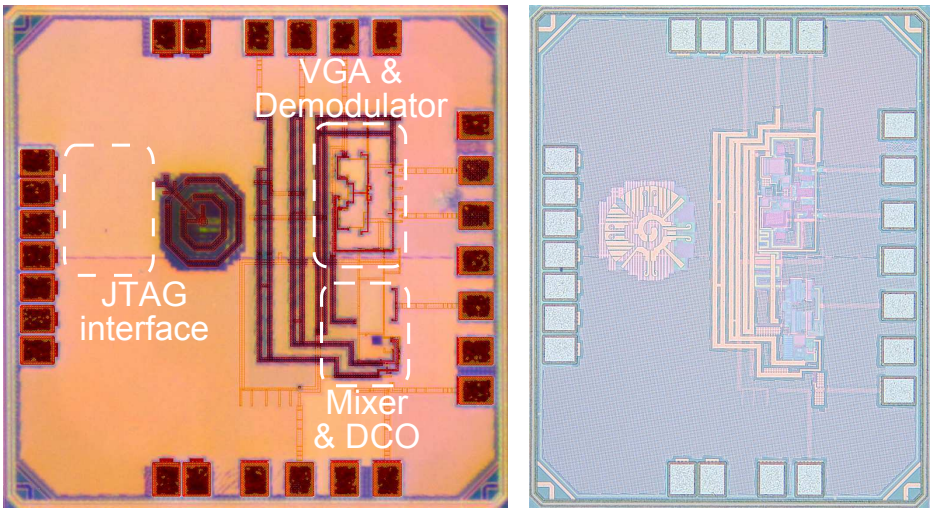


Figure 6.12: *Measured S11 of both WURx versions, including the PCB and off-chip inductor. The irregularity in the WURxV2.0 measurement is located at the DCO frequency (868MHz).*



(a) **(b)**

Figure 6.13: *Die photos of a) WURxV2.0 and b) WURxV2.1, with projected top-level metals.*

Figure 6.13 depicts the die photos of the two WURx versions. The total die area of WURxV2.0 is 0.81mm^2 and of WURxV2.1 is 0.63mm^2. In both versions the analog front-end is approximately 145µm x 415µm. The biasing voltages were generated on the PCB with low noise off-the-shelf voltage regulators. Additionally, an opamp was used as voltage buffer with 50Ω output impedance for the noise figure measurements. The low-frequency analog and digital output signals were sampled with a 60Gsps LeCroy WaveMaster 8 oscilloscope and analyzed using Matlab.

The power consumption of the presented WURxV2.1 is higher than the WURxV1 front-end presented in chapter 5, which is mainly due to the improved linearity in the baseband amplifier stage and the higher power consumption in the local oscillator. The power consumption in the DCO was increased to decrease the oscillator phase noise. The phase noise needed to be reduced to lower the BER floor at higher input power levels. Although the dc power is increased, the energy per bit was reduced from 2.52 to 0.26 by increasing the bit rate. Additionally, the sensitivity of the front-end was improved considerably from WURxV1 to WURxV2.1 by changing the mixer duty cycle from 50% to 25%. The measured NF was 0.3dB higher than simulated and the linearity was 2dB better than expected.

6.3.1 DCDM Demodulator

Since there are on-chip multiplexers for measurement purposes in the second version of the WURx, many internal signals can be measured. A detailed explanation of the signal mapping is given in figure 6.1 and table 6.1. The measurement results of the limiter input and output in the I channel are depicted in figure 6.14a. There is a small phase difference between the input and output terminals. However, this should not be a problem since the limiter is present in every branch of the demodulator see figure 6.7, hence there is no phase shift between branches. The phase difference of the two WURx versions was very similar, because the implemented limiters were the same.

The phase shifts between the input and output of the time-differentiator measured over a few thousand cycles is shown in the histogram shown in figure 6.14b. Ideally, the phase difference between the time-differentiator input and output should be 90 deg at the frequency deviation. However, the measured average phase difference of WURxV2.0 is $\mu = 86.7$ deg and the standard deviation is $\sigma = 9.6$ deg. The average phase shift of WURxV2.1 is 83.6 deg. The average phase shift of both WURx versions is close enough to the ideal 90 deg phase shift for a good performance.

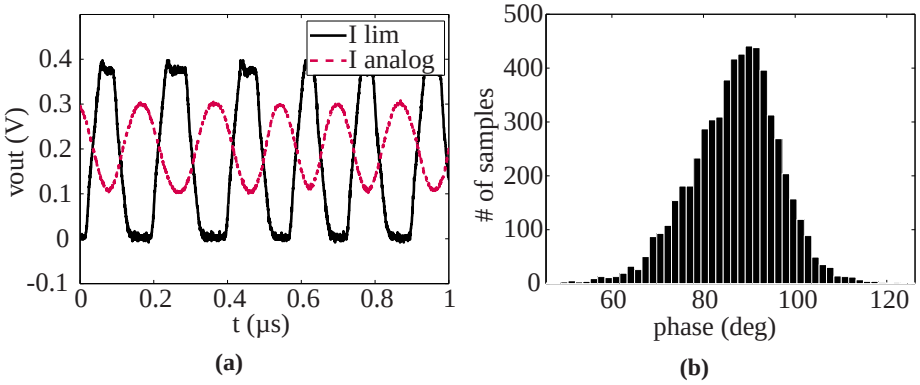


Figure 6.14: *Demodulator sub-block measurements of WURxV2.0 for a) limiter input and output as a function of time and b) time-differentiator phase shift of an input sinusoid.*

6.3.2 DCO

In WURxV2.0 the DCO measurement buffer did not work properly and was removed in WURxV2.1. Therefore it is impossible to measure the tuning range and

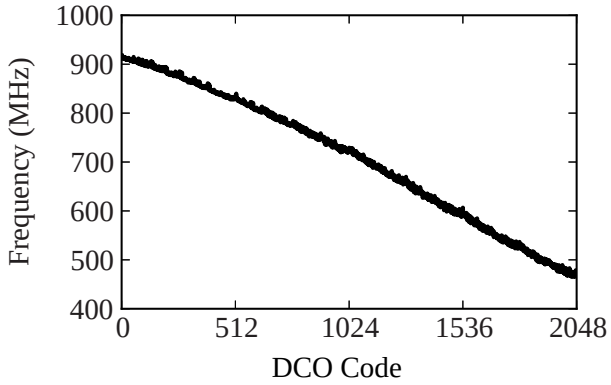


Figure 6.15: *Measured WURXV2.1 DCO tuning range.*

phase noise directly. However, the tuning range can be measured indirectly. To measure the DCO oscillation frequency the digital code is set, the RF input frequency is swept and the power at the baseband output is measured round 5MHz. When the output power is maximal the DCO oscillation frequency is found after taking the measurement frequency of 5MHz into account. The measured tuning range is depicted in figure 6.15. Note that the tuning code is the inverse of the simulated tuning code because of a bit inversion in the JTAG interface.

Instead of the phase noise the jitter of the down-converted baseband output is measured. The measured N-cycle jitter is depicted in figure 6.16a. The DCO frequency was approximately 826MHz. As was discussed in section 3.4.2 equation (3.12), a linear increase of the long-term N-cycle jitter resembles the $\frac{1}{f^2}$ phase-domain behavior of the phase noise caused by thermal noise, which has a flat spectrum in the frequency domain. The 1/f noise leads to the well-known $\frac{1}{f^3}$ phase noise behavior and is visible as the constant part in the N-cycle jitter measurement. From the figure it can be determined that the thermal noise is dominant up to approximately $N = 3 \times 10^3$ cycles. Taking into account the DCO frequency $f_{DCO} \approx 826MHz$ the $\frac{1}{f^3}$ phase noise corner can be estimated

$$f_{\frac{1}{f^3}} \approx \frac{f_{DCO}}{N}, \tag{6.1}$$

leading to a corner frequency of approximately 275kHz. The white phase noise parameter C_{LO} as defined in equation (3.10) is estimated by combining figure 6.16a and equation (3.12). Since the absolute time jitter shown in figure 6.16a is measured at baseband, the average signal frequency at baseband should be sub-

stituted in ω_o used in equation (3.12):

$$\omega_o = 2\pi\,\mu_f\,.$$

In this measurement the frequency ω_o is 38.45Mrad/s. Furthermore, the offset time τ used in the jitter definition is calculated by dividing the number of cycles by the average cycle frequency

$$\tau = \frac{N}{\mu_f}\,.$$

At small time offset the effect of the $\frac{1}{f^3}$ phase noise component is negligible and can be neglected. After rearranging equation (3.12) and neglecting the $\frac{1}{f^3}$ phase noise component at small τ the C_{LO} parameter is estimated as

$$C_{LO} \approx \frac{\omega_o^2}{|\tau|}\sigma_{abs}^2\,.$$

From figure 6.16a it can be read that the jitter at $N = 10$ is approximately $\sigma_{abs} \approx 0.08\mu s$, which gives a $C_{LO} \approx 5.7$Mrad. It should be noted that these are very rough estimations.

The instantaneous DCO frequency statistics can be estimated from the histogram depicted in 6.16b. The average baseband frequency μ_f is the difference between

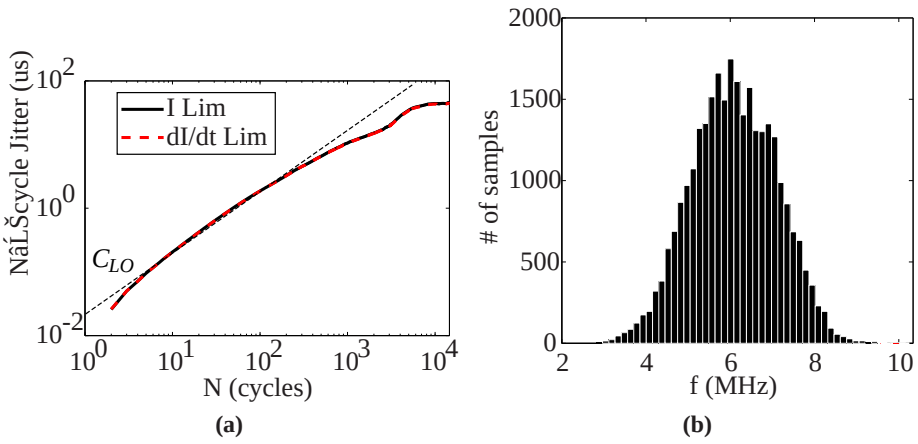


Figure 6.16: *Indirect DCO measurements: a pure 820MHz sine signal was applied to the RF input and the down-converted jitter and instantaneous frequency was observed over 20.000 cycles. a) Plot of N-period jitter measurement σ_{abs} as function of number of cycles N and two lines used to estimate C_{LO} and K_{LO} b) instantaneous baseband frequency measurements $\mu_f = 6.12MHz$, $\sigma_f = 977kHz$.*

the RF input frequency and the local DCO frequency, and the measured standard deviation is $\sigma_f = 977kHz$.

For a low bit error rate the frequency deviation should be high enough to cope with the jitter as was discussed in section 3.5.2. The minimal required SNR for a BER of 0.1% is estimated to be 9.8dB by making use of equation (3.41). The phase noise induced SNR floor at the output of the FSK demodulator is given by equation (3.45) and is copied below for convenience

$$\max\{SNR_{F,IQ,PN}\} \approx \frac{\Delta\omega^2}{R_b C_{LO} + K_{LO}}. \tag{6.2}$$

Combining the SNR floor with the required minimal SNR of 9.8dB, it is calculated that the minimal deviation frequency for a bit rate of 125kbps is approximately 1.12MHz.

6.3.3 Bit Error Rate

The receiver BER performance is measured by transmitting a random bit sequence and sampling the time continuous digital demodulator output. The digital output is filtered and compared to the transmitted bit stream, and the BER is calculated. A simplified diagram of the BER measurement setup is depicted in figure 6.17.

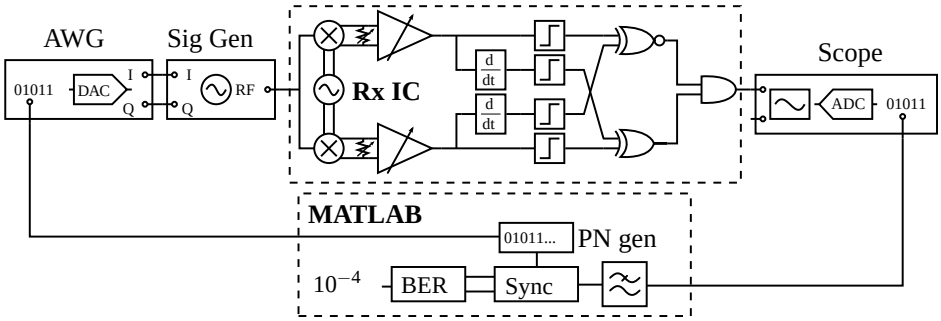


Figure 6.17: *Bit error rate measurement setup using the on-chip FSK demodulator.*

The BER of the DCDM demodulators of both WURx versions for different bit rates are depicted in figure 6.18. For all the different bit rates the frequency deviation is chosen to be 5MHz unless otherwise noted. The sensitivity of the receiver is defined as the input power below which the BER drops below 0.1%. This boundary is given by the dashed horizontal line. The dashed curves represent the

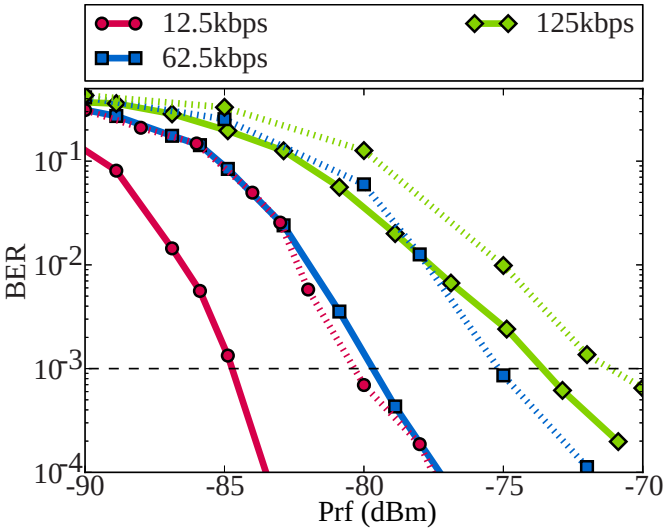


Figure 6.18: *Measured bit error rate (BER) using the on-chip DCDM FSK demodulator, for WURxV2.0 (dotted line) and WURxV2.1 (solid line) as function of the applied input power for different bit rates.*

BER of WURxV2.0 and the solid curves represent the BER of WURxV2.1. The sensitivity of WURxV2.1 is improved by about 6dB with respect to WURxV2.0. However, at higher bit rates the difference is smaller. It is very likely that the sensitivity improved because the gain imbalance between the I and Q paths improved, since all the other parameters are very similar.

In the second version also a Vance FSK demodulator was added on-chip parallel to the DCDM demodulator. According to literature [63] the Vance demodulator should be sub-optimal, which is confirmed by the measurements shown in figure 6.19a. Especially at lower bit rates the DCDM demodulator outperforms the Vance demodulator. However, at higher bit rates the Vance demodulator outperforms the DCDM demodulator. At higher bit rates and constant frequency deviation the FSK modulation gain decreases since the noise is shaped less in the DCDM demodulator, which is discussed in more detail in section 3.5.2. Thus at higher bit rates the advantage of the DCDM demodulator vanishes.

For data rates up to 1.25Mbps the BER measurements are shown in figure 6.19b. The sensitivity scales approximately linear with the bit rate as expected; when the bit rate increases from 6.25kbps to 625kbps the sensitivity increases from -81.7dBm to -72.0dBm. From figure 6.19b it can be seen that the phase noise induced noise floor becomes more prominent at higher bit rates as discussed before.

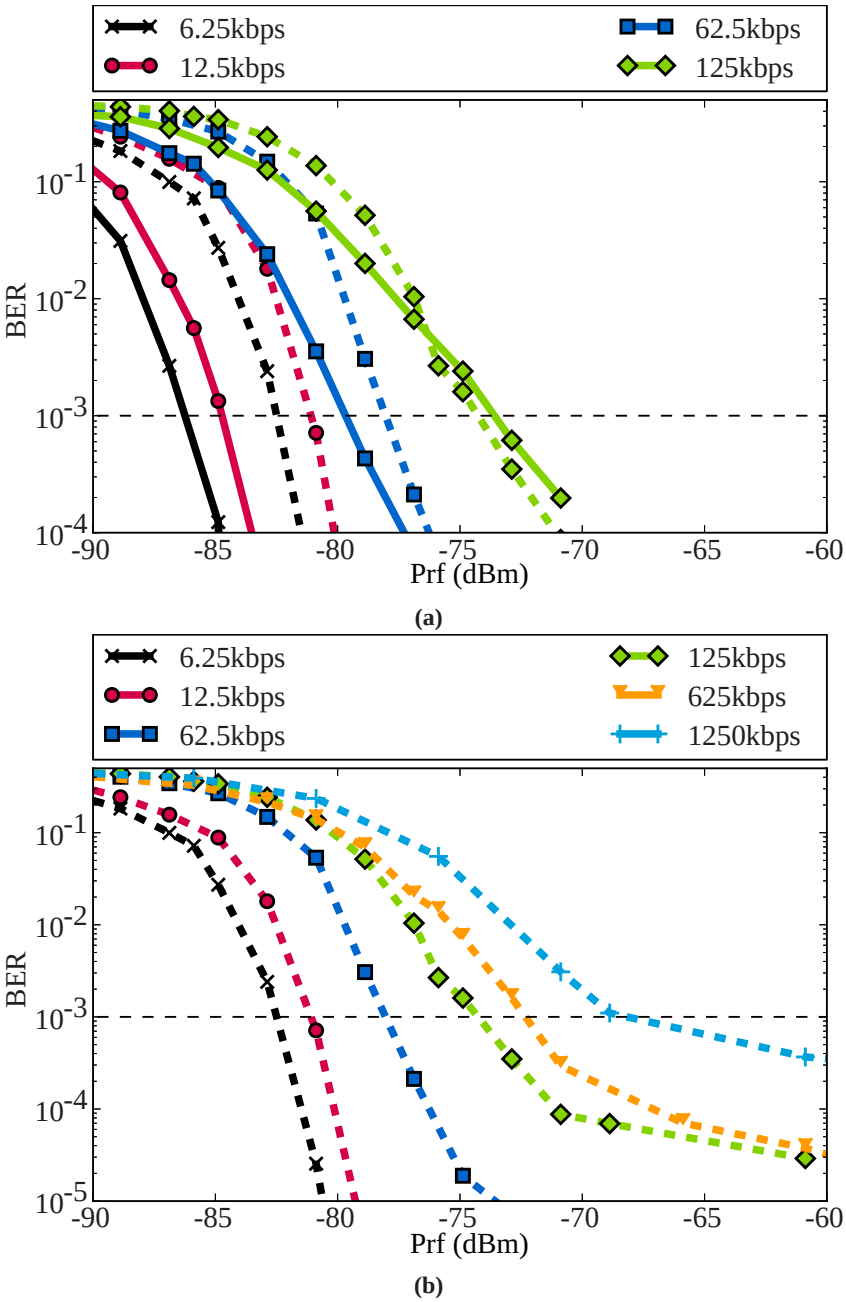


Figure 6.19: *Measured bit error rate using the on-chip DCDM FSK demodulator (solid curves) and Vance demodulator (dashed curves) of the WURxV2.1 front-end as a function of the applied input power for different bit rates. Figure a) depicts the difference between both demodulator types and in b) the BER of the Vance demodulator for a wide range of bit rates are depicted.*

6.3.4 Blocker Rejection

The blocker rejection of the receiver is measured with the on-chip demodulator and a demodulator implemented in Matlab. The measurement setups for the on-chip demodulator and Matlab demodulator are shown in figures 6.17 and 6.20 respectively. The main difference between the two setups is the bandpass filter

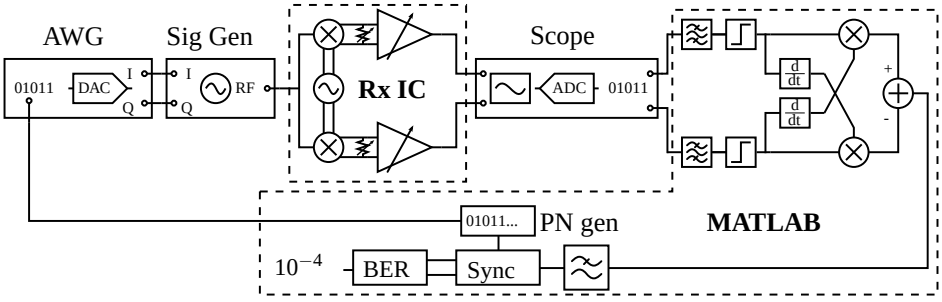


Figure 6.20: *Bit error rate measurement setup using the Matlab demodulator.*

in the analog I and Q channels, which is added in the Matlab demodulator setup. The filter attenuates interferers present in the received signal, hence it improves the blocker rejection.

The blocker rejection is measured by adding a continuous-wave (CW) interferer to a 125kbps FSK modulated desired signal. The frequency of the desired signal is 816.5MHz and the power is set 6dB higher than the sensitivity level. The CW interferer power is increased until the BER drops below 0.1%. The measured

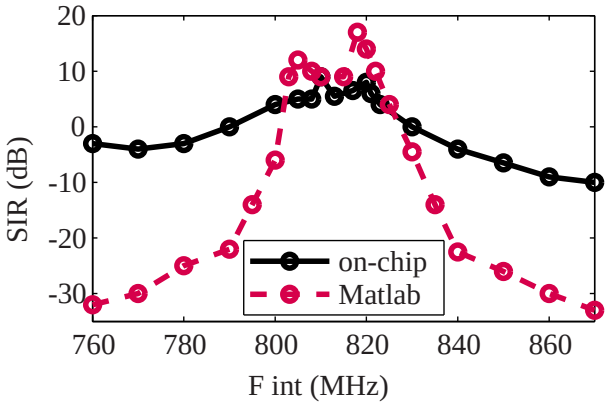


Figure 6.21: *Measured signal-to-interference-ratio for both the on-chip (solid) and ideal (dashed) demodulator, while maintaining BER=10^{-3} for a bit rate of 125kbps as a function of the interferer frequency.*

signal-to-interferer-ratio (SIR) for both the on-chip and ideal demodulator is depicted in figure 6.21. The receiver is most sensitive at the '0' and '1' frequencies, hence the 'peaks' in the measured results.

The out-of-band blocker rejection of the on-chip demodulator can be improved by adding a channel-select filter in front of the demodulator as was done in the Matlab implementation. The on-chip analog multiplexer and measurement buffers limit the in-band blocker rejection of the ideal demodulator. Therefore, the measured in-band blocker rejection of the on-chip demodulator is better than the rejection of the ideal demodulator.

6.3.5 AFC Loop

The automatic frequency control loop discussed in sections 4.4 and 6.2.5 was implemented on a Xilinx Spartan-3E starter kit. The AFC loop analysis did not take into account the receiver noise. To combat the noise, the offset detector thresholds L and H shown in figure 6.11 were adjusted experimentally: the low threshold L was increased by 2 and the high threshold H was decreased by 2.

During the measurement a random bit sequence was sent to the receiver with a bit rate of 62.5kbps. The slew rate was measured by applying a 25MHz step to the carrier frequency and measuring the AFC loop response. The measured results are shown in figure 6.22a. The maximal slew rate was calculated to be 35.55 MHz/ms, and the measured slew rate was 27.1 MHz/ms. The measured slew rate is lower, since noise in the system decreases the error signal present in

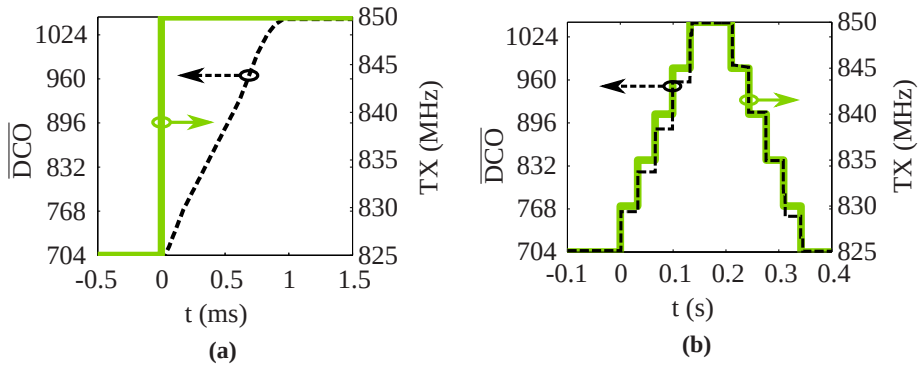


Figure 6.22: *Bit error rate measurement setup. a) Step response of the AFC loop. Receiver noise causes the slight variation in tracking speed. b) Long term AFC loop stability.*

the frequency feedback loop. This can be seen in figure 6.22a: the derivative of the DCO code is not constant.

Figure 6.22b shows the long term stability. The transmitter carrier frequency (TX) is changed, and the fed-back inverse DCO code ($\overline{DCO}$) is observed. From the figure it is clear that the AFC loop tracks the changes very well. Moreover, it is observed that at the same DCO frequency the digital code can settle to two different values. This is caused by the overlap in DAC codes discussed in section 6.2.2.

6.4 Comparison with Literature

The improved FSK receiver WURxV2.1 is compared against reported, low-power FSK receivers, see table 6.8. Not all the parameters are known for all the reported receivers. The presented IIP3 was estimated from IIP3 simulations and input 1dB compression point simulations and measurements.

Compared to the reported FSK receivers, the WURxV2.1 has a low power consumption, especially taken into account that [12, 13, 16] do not have frequency calibration or an on-chip demodulator. Direct comparison in power consumption is difficult since also other parameters are different. However, the presented receiver has similar sensitivity and bit rate as [15], but WURxV2.1 has a 33% lower power consumption. Additionally, the bit rate is higher than most receivers presented in literature, and high enough for most sensor network applications.

By comparing the power consumption, it is evident that the presented AFC loop is a good and power efficient alternative to a PLL. For example in [9], the on-chip PLL consumes 916.5µW.

The WURxV2.1 has a relatively high 1dB compression point, because of the mixer-first architecture. On the other hand, reference [14] has a poor blocker rejection caused by its injection-locked architecture. However [14] has a very low energy per bit of approximately 0.1nJ/bit, which is about 2.5 times lower than the presented receiver.

The reported receiver uses a more advanced technology than the other receivers, which is beneficial for digital signal processing. However, for analog and RF circuits it has little benefit. Firstly, the threshold voltage of the used 40nm technology is higher than that of the 90nm CMOS technology used in the first version of the WURx front-end discussed in chapter 5. This high threshold voltage places a lower bound on the supply voltage and power consumption. Additionally, to

Table 6.8: *Performance summary and comparison.*

REF	WURx V1	WURx V2.0	WURx V2.1	[9]	[12]	[13]	[14]	[15]	[16]
CMOS	90nm	40nm	40nm	130nm	180nm	130nm	180nm	180nm	130nm
Power (µW)	126	382	329	352	500	750	420	490	1920
V_{dd} (V)	0.75	0.8&1.2	0.8&1.0	0.25	1.0	0.4	0.7	0.7	1.2
Freq. (MHz)	782-932	782-932	478-918	1500-1650	2400	1950-2380	920	398-408	825-983
NF (dBm)	25	11.4	12	7.2	10.1	5.1	-	-	10
P_{1dBc} (dBm)	-30	-24	-22	-48	-31	-17.5*	-34†	-	-10
IIP3 (dBm)	-21	-14	-12	-48	-	-7.5	-	-	-
P_{sens} (dBm)	-65	-71 (125kbps)	-74 (125kbps)	-	-	-	-73	-68	-83
R_b (kbps)	50	≤625	≤1250	-	100	300	5000	250	45-48
$\frac{P_{DC}}{R_b}$ (nJ/bit)	2.52	0.61	0.26	-	5.0	2.5	0.08	1.96	40

† The linearity is not directly specified in the paper, but estimated after comparing the reported blocker rejection with the presented second version of the WURx front-end.

* The 1dB compression point is not reported. It is estimated by assuming that the 1dB compression point is 10dB lower than the input referred third order interception point.

decrease the 1/f noise the channel length of the transistors in the receiver chain are increased from their minimal value of 40nm. The only place were the 40nm gate length is used is the switches in the passive mixer. The reduced gate length reduces the required DCO signal power and decrease the switch on resistance.

In figure 6.23 four receivers are compared graphically using the radar plot, that was introduced in section 5.3. Although the WURx reported in chapter 5 has the lowest power consumption, it also has the lowest sensitivity and bit rate, whereas the improved WURxV2.1 has a better balance between DC power consumption and receiver performance. Reference [13] also has a mixer-first architecture, whose linearity is larger at the cost of higher power consumption. The lowest energy per bit was consumed by [14]. However, the blocker rejection was poor due to the injection lock-in architecture.

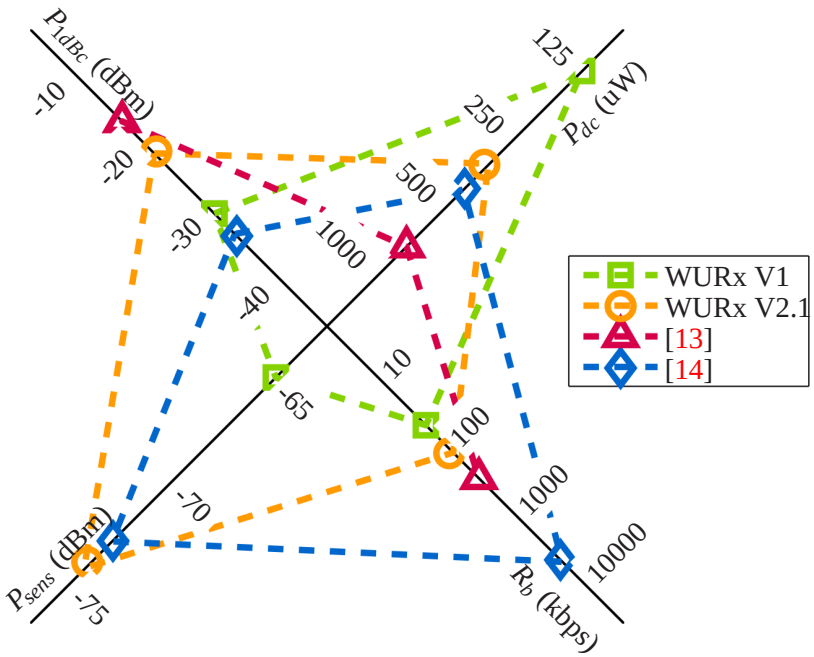


Figure 6.23: *Graphical comparison of reported FSK receivers.*

6.5 Conclusion

The 25% duty-cycle scheme improved the noise figure by about 6dB compared to the 50% duty-cycle scheme that was used in the first WURx tape-out presented in chapter 5. Because of the lower mixer noise figure and higher transducer power gain the sensitivity of the second version also improved, such that it meets the specifications given in section 3.6.2. Additionally the sensitivity scales linearly with the bit rate as was expected.

Because of an asymmetric layout between the DCO buffer and passive mixer in the first tape-out, the mixer did not switch correctly. The effect was alleviated by increasing the DCO buffer supply voltage. However this led to an approximately $50\mu W$ increase in power dissipation. The receiver front-end was later taped-out without the imbalance between the DCO phases. The I/Q imbalance was reduced considerably after the new tape-out, which also led to an 5dB improvement in sensitivity.

Compared to other reported receivers in literature the presented receiver has a good linearity to power dissipation ratio, thanks to the mixer-first design.

From the comparison between the DCDM and Vance FSK demodulators it is seen that the DCDM gives a 3dB improvement in sensitivity at low bit rates, because the DCDM demodulator shapes the noise and thereby reduces the output noise after filtering when the modulation index is high. However, at lower modulation index or higher bit rates the DCDM can not exploit the noise shaping anymore since the data bandwidth is increased. Therefore, the DCDM looses then its advantage and the Vance demodulator outperforms the DCDM demodulator.

After comparing the on-chip demodulator with the ideal demodulator implemented in Matlab it is clear that the out-of-band blocker rejection would be greatly improved by adding a bandpass filter in front of the limiters used in the FSK demodulator.

Additionally, the implemented low-power automatic frequency control loop was demonstrated. The loop was shown to be stable and can track frequency steps of 20MHz, which is a much larger step than is expected in a real environment where the voltage and temperature variations are expected to be slowly varying. The low power AFC loop is shown to be a good alternative to power-hungry phase-locked loops in wideband FSK systems.

CHAPTER 7

CONCLUSIONS

WIRELESS body area networks (WBAN) require low power sensor nodes, since the network needs to operate for prolonged periods on restrained power sources. In this thesis the Wake-up Receiver (WURx) concept has been studied. It is shown that the WBAN energy consumption is reduced by making trade-offs between the network, system and circuit level design phases of the WURx concept.

Small-scale WBANs are asymmetric in nature; they consist of many small, low power sensor nodes and a single high-power data sink or master node. We introduced a closed-form MAC-layer energy consumption model for the synchronization between sensor nodes and master node. Using the model we have shown that for a typical WBAN application the synchronization energy can be reduced by a factor 2 to 3 by using a WURx-enhanced synchronization scheme. How much the average power consumption can be reduced exactly depends on the required packet rate and link-setup latency. It is shown that the exact limits on the packet rate and link latency depend on the main radio and the WURx power consumptions.

In this thesis we focused on FSK receiver front-ends instead of OOK front-ends. While envelope detector based OOK receivers have a lower average power consumption, they require bulky and costly bulk or surface acoustic wave filters. Additionally, envelope detector based receivers are more vulnerable to interferers than FSK receivers which increases their packet error rate and increases the

retransmission power consumption. Therefore, for interferer rich environments such as ISM bands, FSK is a better alternative than OOK.

The small communication distance for body-area-networks allows for a reduced receiver sensitivity. This lower sensitivity requirement has been exploited here by removing the power hungry low noise amplifier from the receiver front-end, leading to a mixer-first architecture.

In this thesis a closed-form analytical model has been presented that describes the relationship of phase noise and I/Q imbalance and the wideband FSK signal-to-noise-ratio (SNR) and bit error rate (BER). This model is used during the cross-layer design of the receiver architecture and its circuit implementation. This model is used to obtain quantitatively how much I/Q imbalance and phase noise the receiver can tolerate as a function of modulation index. It was shown that the phase noise requirement can be relaxed to -80dBc/Hz at 1MHz offset by increasing the modulation index to 6.8. Since the local oscillator phase noise requirement is relaxed, the ring oscillator is a better alternative to LC oscillators. Moreover, technology scaling favors low power ring oscillators to LC oscillators as long as the phase noise requirement is relaxed.

It was shown that the power consumption reduces by exchanging a phase-locked-loop (PLL) for a low power automatic frequency control (AFC) loop. To track PVT variations the AFC loop makes use of the already present FSK demodulator to measure the frequency offset between the transmitter and local oscillator.

We validated the presented theory by implementing two WURx front-ends in 40nm and 90nm CMOS technologies. It is demonstrated that the WURx front-ends designed using the presented theory can compete against state-of-the-art FSK receivers regarding power consumption, bit rate and sensitivity. The sensitivity, defined as the input power at which the BER drops below 0.1%, of the first WURx version was -65dBm at a bit rate of 50kbps while consuming only 126µW. The sensitivity of the second WURx version was improved to -74dBm at a bit rate of 125kbps. The sensitivity was improved by changing the mixer duty cycle from 50% to 25% and decreasing the oscillator phase noise. While the power consumption of the second WURx was increased to 329µW, also the maximal bit rate was increased from 50kbps to 1.25Mbps. The energy per bit between the two WURx versions improved from 2.52nJ/bit to 0.26nJ/bit. Additionally, the AFC was demonstrated to work for frequency steps of 25MHz, which is more than enough to track slowly varying PVT variations.

RECOMMENDATIONS

This thesis covers a wide range of topics from network statistics to transistor-level circuit design, with a main focus on low peak-power consumption. Not all topics are covered in full detail. Possible directions for future research include:

- The effect of retransmission on average power consumption and channel occupation should be studied. This should include channel coding. In this thesis a simple correlation code with a minimum Hamming distance was chosen for its low complexity and power consumption. However, it could be beneficial to implement a more complex code when the retransmission overhead can be reduced significantly. Additionally, excessive retransmission might lead to congestion which reduces the quality of service of the entire network.
- To be able to cope with a larger frequency offset the modulation index can be increased even further than is done in this thesis. To coexist with existing standards and allow for more nodes in a single frequency band a signal could occupy two channels or bins: one for the "0" frequency and one for the "1" frequency. The interference to other channels can be reduced by filtering the signal away from these two bins in the transmitter. However, the effect on inter-symbol interference and efficient wideband demodulation should be studied in more depth.
- The input impedance of the mixer-first receiver depends on the baseband load resistance, which enables adaptive source matching. This could be studied in more detail. Additionally, the input impedance becomes solely dependent on the source resistance when the load resistance is much larger than the switch and source resistances. Thus, the mismatch should be unaffected by source impedance variations.
- An automatic frequency control loop is used as a replacement of the ubiquitous power-hungry phase locked loop. However, it is possible for the

loop to start tracking interferers. Research is needed on baseband algorithms to prevent this. For example, the receiver should only track the received signal when a package header is received correctly.

APPENDIX A

MAC PROTOCOL PACKET STATISTICS

In this appendix the MAC layer packet statistics used in section 2.2 are derived from the parameters: p_{miss}, p_{false} and N^{+}_{WUC}. The appendix starts with the derivation of the asynchronous MAC statistics. At the end of the appendix the synchronous MAC statistics are derived.

A.1 Number of Wake-up Calls

The probability density needs to be known before the expected number of WUC packet transmissions can be obtained. Initially, the limited number of retransmissions will be ignored; this issue is corrected afterward. Table A.1 is used to obtain the probability distribution. The first two columns specify the number of wake-up calls and acknowledgments respectively, and the third column gives the possible scenarios. The last column shows the probability of the given scenario.

Every time the number of WUCs is increased, the probability is multiplied by p_{miss} and the number of possible scenarios increases by 1. Therefore, the probability of n WUC transmissions, specified by $p_{WUC,n}$, is

$$p_{WUC,n} = n\left(1 - p_{miss}\right)^2 p_{miss}^{n-1}. \tag{A.1}$$

Table A.1 is only valid when the maximal number of WUC transmissions is unlimited. However, when a maximum N^{+}_{WUC} exists, an error is made for

Table A.1: *Wake up call retransmission probabilities*

# WUC	# ACK	Scenario	Probability
1	1	WUC OK, ACK OK	$(1-p_{miss})^2$
2	1	WUC MISS	$p_{miss}(1-p_{miss})^2$
		WUC OK, ACK OK	
	2	WUC OK, ACK MISS	
		WUC X, ACK OK	
3	1	WUC MISS 2x	$p_{miss}^2(1-p_{miss})^2$
		WUC OK, ACK OK	
	2	WUC MISS	
		WUC OK, ACK MISS	
		WUC X, ACK OK	
	3	WUC OK, ACK MISS	
		WUC X, ACK MISS	
		WUC X, ACK OK	

$p_{WUC,N^+_{WUC}}$. This error is caused by the fact that after N^+_{WUC} transmissions the transmitter quits, whether the WUC and ACK are correctly received or not. In the table this possibility is not present. The error made can be easily corrected by changing $p_{WUC,N^+_{WUC}}$ to

$$p_{WUC,N^+_{WUC}} = 1 - \sum_{k=1}^{N^+_{WUC}} p_{WUC,k}\,.$$

By definition, the expected value is calculated as

$$\mu_X \stackrel{\text{def}}{=} \sum_{n=1}^{n^+} X_n p_X(X_n)\,. \tag{A.2}$$

Note that in this appendix we will use μ to specify the expected value instead of the expectation operator $E[.]$ to avoid confusion with energy. Again, we assume that the number of retransmissions is unlimited, and we will show that the approximation error is negligible when $N^+_{WUC} > 1$. Substituting the probability given by (A.1) in (A.2) gives

$$\mu_{WUC} = \frac{(1-p_{miss})^2}{p_{miss}} \sum_{k=1}^{N^+_{WUC}} k^2 p_{miss}^k\,.$$

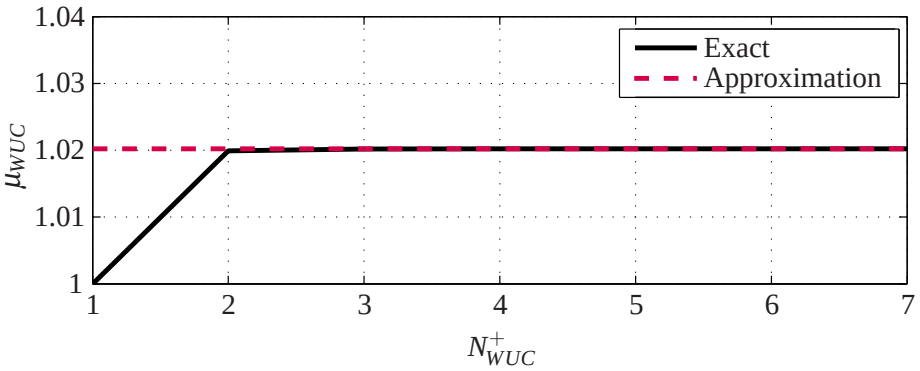


Figure A.1: *Exact(solid line) and approximated (dashed line) expected number of WUC transmissions using* $p_{miss} = 1\%$.

This equation can be approximated by

$$\mu_{WUC} \approx \frac{1 + p_{miss}}{1 - p_{miss}}.$$

Figure A.1 shows the actual and expected number of WUC transmissions for $p_{miss} = 1\%$. It is clear that the approximation error is very small when $N^{+}_{WUC} > 1$. The maximal error is $2p_{miss}$ when $N^{+}_{WUC} = 1$.

A.2 Number of Acknowledgments

Similar to the expected number of wake-up calls, the expected number of acknowledgments μ_{ACK} is obtained by first calculating the probability distribution. The probability of n acknowledgments per link setup is given by $p_{ACK,\,n}$, and is calculated using table A.1:

$$p_{ACK,\,n} = (1 - p_{miss})^2 \sum_{k=n-1}^{N^{+}_{WUC}-1} p^{k}_{miss}. \tag{A.3}$$

The given probability is only valid when there is no maximum on the number of WUC transmissions. When the number of transmissions is limited, the approximation error is

$$p_{error} = (1 - p_{miss})\, p^{N^{+}_{WUC}}_{miss}.$$

After correcting this approximation error from from (A.3), the probability is given by

$$p_{ACK,\,n} = (1-p_{miss})^2 \sum_{k=n-1}^{N^+_{WUC}-1} p^k_{miss} + (1-p_{miss})\, p^{N^+_{WUC}}_{miss}\,.$$

Using the well-known summation of geometric series

$$\sum_{k=0}^{n} p^k = \frac{1-p^{n+1}}{1-p}$$

the $p_{ACK,n}$ probability can be simplified to

$$p_{ACK,\,n} = (1-p_{miss})\, p^{n-1}_{miss}\,. \tag{A.4}$$

The expected number of acknowledgments is calculated by substituting equation (A.4) in definition (A.2):

$$\mu_{ACK} = \frac{1-p^{N^+_{WUC}}_{miss}}{1-p_{miss}} - N^+_{WUC}\, p^{N^+_{WUC}}_{miss}\,.$$

The second term is small compared to the first term and can be neglected,

$$\mu_{ACK} \approx \frac{1-p^{N^+_{WUC}}_{miss}}{1-p_{miss}}\,.$$

The approximation error is maximally p_{miss} when $N^+_{WUC} = 1$, and decreases rapidly for increasing number of retransmissions.

The energy consumption of retransmitting an acknowledgment can be different from the energy consumption of the first transmission, because the transceiver is already in transmit mode. Therefore the expected number of retransmissions μ_{ACKx} and the probability that at least the initial ACK packet is transmitted $p_{ACK\geq 1}$ need to be specified. The latter one is

$$p_{ACK\geq 1} = \sum_{n=1}^{N^+_{WUC}} p_{ACK,\,n}\,,$$

which simplifies to

$$p_{ACK\geq 1} = 1 - p^{N^+_{WUC}}_{miss}\,. \tag{A.5}$$

The expected number of retransmissions given by μ_{ACKx} is

$$\begin{aligned}\mu_{ACKx} &= \mu_{ACK} - p_{ACK\geq 1} \\ &= \frac{p_{miss}}{1-p_{miss}} - p_{miss}^{N^+_{WUC}} \left(N^+_{WUC} + \frac{p_{miss}}{1-p_{miss}} \right),\end{aligned}$$

neglecting the second term the expected number of retransmissions is approximated by

$$\mu_{ACKx} \approx \frac{p_{miss}}{1-p_{miss}}. \tag{A.6}$$

A.3 False Wake-up Statistics

When a node receives a wake-up call meant for another node, and falsely assumes that it is the destination, it starts transmitting false acknowledgments (FACK). The node will transmit the maximum number of acknowledgments. This will consume a lot of power and congests the channel. In this section the expected number of false acknowledgments per received packet per 'other node' is calculated, assuming the number of false wake-ups increases as the network size increases.

Table A.2 is used to calculate the probability that n false ACK are transmitted, given by $p_{FACK,\,n}$. The first column specifies the number of wake-up calls. Furthermore, the third column gives the scenario, where 'false' means a falsely decoded packet, 'OK' means that the packet is ignored as it should be and 'X' specifies a don't care. Using the table the probability of n falsely transmitted

Table A.2: *Probability distribution of false acknowledgments*

# WUC	# False ACK	Scenario	Probability
1	N^+_{WUC}	false	$p_{false}\ p_{WUC,\,1}$
2	N^+_{WUC}	false, X	$p_{false}\ p_{WUC,\,2}$
	$N^+_{WUC}-1$	OK, false	$p_{false}\left(1-p_{false}\right)\ p_{WUC,\,2}$
3	N^+_{WUC}	false, X, X	$p_{false}\ p_{WUC,\,3}$
	$N^+_{WUC}-1$	OK, false, X	$p_{false}\left(1-p_{false}\right)\ p_{WUC,\,3}$
	$N^+_{WUC}-2$	OK, OK, false	$p_{false}\left(1-p_{false}\right)^2\ p_{WUC,\,3}$

acknowledgments is

$$p_{FACK,\,n} = p_{false}\left(1-p_{false}\right)^{N^{+}_{WUC}-n} \sum_{k=N^{+}_{WUC}+1-n}^{N^{+}_{WUC}} p_{WUC,\,k}\,.$$

After substituting $p_{WUC,\,k}$ in the equation above, the probability of exactly n falsely transmitted ACK packets is

$$p_{FACK,\,n} = p_{false}\left(1-p_{false}\right)^{N^{+}_{WUC}-n} \frac{\left(1-p_{miss}\right)^{2}}{p_{miss}} \sum_{k=N^{+}_{WUC}+1-n}^{N^{+}_{WUC}} k p_{miss}^{k}\,. \tag{A.7}$$

The equation becomes cumbersome when the sum is computed. However, it can be noticed that the probability is maximal for $n = N^{+}_{WUC}$

$$p_{FACK,N^{+}_{WUC}} \approx p_{false}\,,$$

and the probability decreases rapidly with decreasing n when $p_{miss} \ll 1$.

Using definition (A.2) the expected number of falsly transmitted acknowledgments per 'other node' in the network is

$$\mu_{FACK} = \sum_{k=1}^{N^{+}_{WUC}} k\, p_{FACK,\,k}\,.$$

Since $p_{FACK,\,n}$ is negligible except for $n = N^{+}_{WUC}$ it can be approximated by

$$\mu_{FACK} \approx N^{+}_{WUC} p_{false}\,. \tag{A.8}$$

Figure A.2 depicts the exact and approximated values of μ_{FACK} for two different values of p_{miss}, namely 1% and 10%. As the figure shows, the approximation error increases when the packet miss probability increases. However, for practical systems, $p_{miss} \leq 1\%$, the approximation can be used.

The probability that at least one false acknowledgment is transmitted, given by $p_{FACK\geq 1}$, is equal to

$$p_{FACK\geq 1} = \sum_{k=1}^{N^{+}_{WUC}} p_{FACK,k}\,.$$

As was commented before, $p_{FACK,n}$ is maximal for $n = N^{+}_{WUC}$ and decreases quickly for decreasing n. Therefore $p_{FACK\geq 1}$ is approximately equal to

$$\begin{aligned} p_{FACK\geq 1} &\approx p_{FACK,N^{+}_{WUC}} \\ &\approx p_{false}\,. \end{aligned}$$

The expected number of false acknowledgment retransmissions per 'other node' in the network is

$$\mu_{FACKx} = (\mu_{FACK} - \mu_{FACK1}) .$$

As was already stated the probability of N^{+}_{WUC} false acknowledgments is much larger than the probability of 1 false acknowledgment transmission. Therefore $\mu_{FACKx} \approx \mu_{FACK}$ and

$$\mu_{FACKx} \approx N^{+}_{WUC}\, p_{false} . \tag{A.9}$$

A.4 Synchronized Transceiver Packet Statistics

In this section the expected number of TDMA slots per received packet given by μ_{slot} is derived, which is very similar to the expected number of wake up

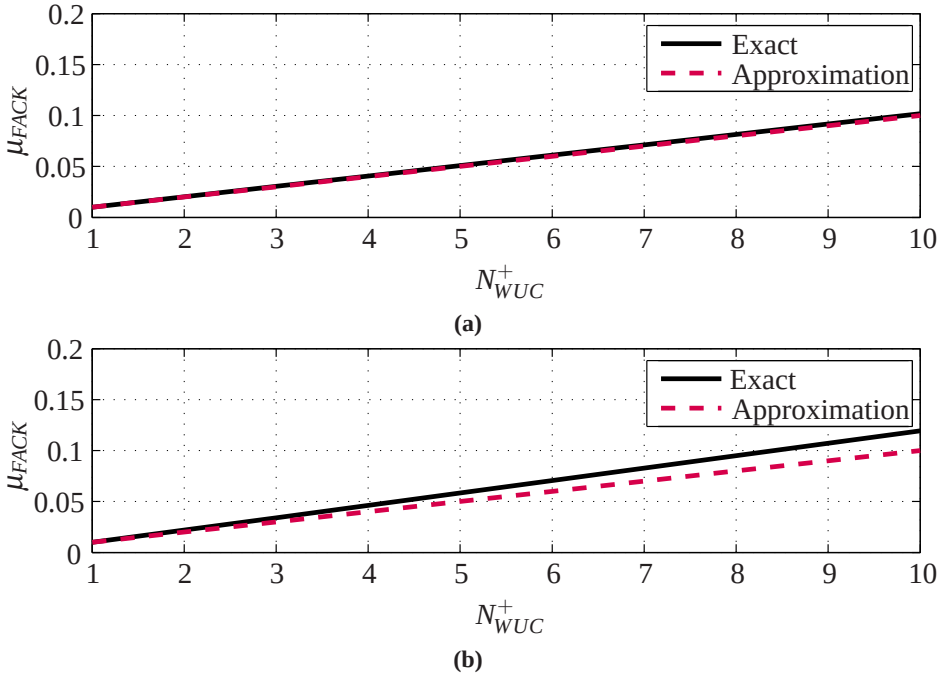


Figure A.2: *Exact and approximated expected number of false ACK transmissions μ_{FACK} as function of the maximal number of attempts. Using the packet miss and false wake-up probabilities: a) $p_{miss} = 1\%$ and $p_{false} = 1\%$ b) $p_{miss} = 10\%$ and $p_{false} = 1\%$.*

calls given in section A.1. The difference is that the initial WUC is not transmitted. In case the first ACK transmission is successful only one needs to be transmitted, the probability on this occurrence is $(1-p_{miss})$. One extra ACK needs to be transmitted when the first one is unsuccessful, the probability of this is $p_{miss}(1-p_{miss})$. For every extra ACK transmission the previous probability needs to be multiplied by p_{miss}. Therefore, the probability that n ACK transmissions are needed is

$$p_{slot,n} = (1-p_{miss})\, p_{miss}^{n-1}.$$

The same approximation error is made as was done with the μ_{WUC} analysis; the number of ACK transmissions is limited by N^{+}_{WUC} times, when the ACK is not correctly received within this number of attempts the packet is lost. Taking into account the retransmission limit, the probability that n acknowledgments are send becomes

$$p_{slot,N^{+}_{WUC}} = \sum_{k=N_{WUC}}^{\infty} p_{slot,k}$$

$$p_{slot,N^{+}_{WUC}} = 1 - \sum_{k=1}^{N^{+}_{WUC}-1} p_{slot,k}\,.$$

Using the definition given by (A.2), the expected number is approximated by

$$\mu_{slot} \approx \frac{1-p_{miss}^{N^{+}_{WUC}}}{1-p_{miss}},$$

assuming $N^{+}_{WUC} > 1$ and $p_{miss} \lesssim 1\%$.

APPENDIX B

NORDIC RADIO PARAMETERS

The Nordic nRF24L01 radio chip is often used, since it is a low-power high bit rate transceiver. The parameters of this chip are summarized in table B.1. The

Parameter	Explanation	Value
T_{wake}	Switching: Sleep → Standby	1.5ms
T_{set}	Switching: Standby → Rx or Tx	130µs
T_{set}	Switching: Settling period when switching between Rx and Tx.	130µs
P_{sleep}	Power consumption in sleep (power down) mode.	2.7µW
$P_{standby}$	Power consumption in standby mode 1.	66µW
P_R	Power consumption in Rx mode. (2 Mbps)	36.9mW
P_T	Power consumption in Tx mode. (0dBm)	33.9mW
P_{Rset}	Power consumption when switching to Rx mode.	25.2mW
P_{Tset}	Power consumption when switching to Tx mode.	24mW
P_{wake}	Power consumption when switching between sleep and standby mode.	855µW
k	Length of minimal packet in bits. Used for: sync, ACK, WUC	34bits
R_b	Bit rate of main radio	2Mbps

Table B.1: *nRF24L01 parameters*

Nordic chip can operate in different power down modes. In this document the "Power down mode" and the "Standby 1 mode" are used in the analysis. In the energy consumption analysis the differences between the power consumption of different regimes and the sleep/standby mode are used. When the mode is not specified the node uses the sleep mode. The used power differences are

$$\Delta P_x = P_x - P_{sleep}\,.$$

When the "Power down mode" is not used the power difference is

$$\Delta P_x = P_x - P_{standby}\,,$$

this is the normal way of operation of the Holst node. It is specifically mentioned when this equation is used.

APPENDIX C

SIMULATION SCRIPT

This appendix gives simplified pseudo-Matlab code for script used for the simulation of the output SNR and BER, all the variables correspond to the ones in section 3.4. To increase the simulation speed the phase noise θ is incorporated in the received signal r instead of the matrix Mrx. To obtain accurate BER results at least 100 bit errors need to be simulated, which means that for very low bit error rates the simulation time becomes very long.

```
function SNR_BER_sim(Rb,dw,Grf,PN,g,e)
  % Generate phase noise
  % PN dBc/Hz @ 1MHz
  clo = (2*pi*1e6)^2 * 10^(PN/10);
  theta = sqrt(clo)*cumsum(randn*sqrt(dt));

  % Generate bits
  an = 2*(randn > 0) - 1;
  % Generate signal
  phi = t.*an*dw;
  I = A * cos(phi + theta);
  Q = A * sin(phi + theta);
  r = [I ; Q];

  % Generate bandwidth limited noise
  nrf = filter([randn ; randn]*sigma_rf);
  nbb = filter([randn ; randn]*sigma_bb);

  % Receiver
  Mrx = Grf/2 * [1 0; -g*sin(e) g*cos(e)];
```

```
  sr = Mrx * r;
  sn = Mrx * nrf + nbb;
  s = sr + sn;

  % Hard limit
  R = sqrt(s(1, :).^2 + s(2, :).^2);
  Ilim = s(1, :)./R;
  Qlim = s(2, :)./R;

  % differentiate
  Ilimdot = [0 diff(Ilim)] ./ dt;
  Qlimdot = [0 diff(Qlim)] ./ dt;
  ydemod = (Qlim.*Ilimdot - Ilim.*Qlimdot);

  % Integrate and dump filter
  ydemod_iad = filter(ydemod(2:end));

  % Sample bits and obtain the BER
  ybits_smp = 2*(sample(ydemod_iad)<0)-1;

  % Calc BER
  Nerr = sum(ybits_smp ~= an);
  BER = Nerr / Nbits;

  % Calculate output SNR
  Psout = 10*log10( mean(ydemod_iad.^2) );
  Pnout = 10*log10( var (ydemod_iad)    );
  SNRout = Psout - Pnout;
end
```

APPENDIX D

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APPENDIX E

LIST OF PUBLICATIONS

Journal Publications

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, “Mixer-first FSK Receiver with Automatic Frequency Control for Body Area Networks," *IEEE Trans. Circuits Syst. I, vol 60*, #8, 2051-2063, 2013, doi: 10.1109/TCSI.2013.2239179.

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, “Implications of I/Q Imbalance, Phase Noise and Noise Figure for SNR and BER of FSK Receivers," *IEEE Trans. Circuits Syst. I, vol 60*, #8, 2187-2198, 2013, doi: 10.1109/TCSI.2013.2239151.

Invited Paper

M. Lont, N. F. Kiyani, and G. Dolmans, “System Considerations for Low Power Design in Wireless Body Area Networks," *Communications and Vehicular Technology in the Benelux (SCVT), 2012 19th IEEE Symposium on*, pp. 1-4, Nov 2012, Eindhoven, The Netherlands, doi: 10.1109/SCVT.2012.6399411.

Conference Publications

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, “Ultra-low power FSK receiver for body area networks with automatic frequency control,” *Proceedings of the 42nd European Solid-State Circuits Conference (ES-*

SCIRC 2012), pp. 430-433, 17-21 September 2012, Bordeaux, France, doi: 10.1109/ESSCIRC.2012.6341347.

B. van Liempd, M. Vidoikovic, M. Lont, C. Zhou, P. Harpe, D. Milosevic, and G. Dolmans, "A 3µW fully-differential RF envelope detector for ultra-low power receivers," *Proceedings of the IEEE International Symposium on Circuits and systems (ISCAS)*, pp. 1-4, 20-23 May 2012, Seoul, Korea, doi: 10.1109/ISCAS.2012.6271532.

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, "Ultra-Low power FSK wake-up receiver front-end for body area networks," *Proceedings of the 2011 IEEE Radio Frequency Integrated Circuits Symposium (RFIC 2011)*, pp. 1-4, 5-7 June 2011, Baltimore, MD, USA, doi: 10.1109/RFIC.2011.5940697.

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, "Requirement driven low-power LC and ring oscillator design," *Proceedings of the 2011 IEEE International Symposium on Circuits and Systems (ISCAS 2011)*, pp. 1129-1132, 15-18 May 2011, Rio de Janeiro, Brazil, doi: 10.1109/ISCAS.2011.5937769.

M. Lont, D. Milosevic, G. Dolmans, and A.H.M. van Roermund, "Analytical passive mxer power gain models," *Proceedings of the Annual Workshop on Circuits, Systems and Signal Processing (ProRISC 2010)*, 18-19 November 2010, Veldhoven, The Netherlands.

M. Lont, D. Milosevic, P. G. M. Baltus, G. Dolmans, and A.H.M. van Roermund, "Analytical passive mixer power gain models," *Proceeding of 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010)*, pp. 2386-2389, May 30-June 2 2010, Paris, France, doi: 10.1109/ISCAS.2010.5537183.

M. Lont, D. Milosevic, P. G. M. Baltus, G. Dolmans, and A.H.M. van Roermund, "Analytical models for the wake-up receiver power budget for wireless sensor networks," *Proceeding of the IEEE Global Telecommunications Conference, GLOBECOM 2009*, pp. 1-6, November 30-December 4 2009, Honolulu, Hawai, USA, doi: 10.1109/GLOCOM.2009.5425470.

M. Lont, D. Milosevic, P. G. M. Baltus, G. Dolmans, and A.H.M. van Roermund, "Wake-up receiver for wireless sensor networks," *Proceedings of ProRISC 2009, 20th Annual Workshop on Circuits Systems and Signal Processing*, pp. 484-487, November 26-27, 2009, Veldhoven, The Netherlands.

APPENDIX F

SUMMARY

Wake-up Receiver Based Ultra-Low-Power WBAN

SENSOR nodes used in wireless body area networks operate on energy scavenging devices or small batteries. Moreover, it is often impractical or even impossible to replace or recharge the batteries regularly. Therefore, the main design goal is to reduce their power consumption as much as possible. To reduce the average power consumption the sensor nodes are placed in deep sleep mode as often and as long as possible, making the network synchronization challenging. Combining the fact that the average packet rate is very low and the link to link setup-latency requirement is relaxed a wake-up receiver (WURx) enhanced synchronization scheme is beneficial. This thesis focuses on power reduction strategies for WURx making use of network, system and circuit level requirements.

In chapter 2 Wireless Body Area Network (WBAN) properties are studied. It is shown that the maximal transmission distance is approximately 10m, making a single hop network topology a good fit. Additionally, it is shown that network symmetry and synchronization has a big influence on the average power consumption of wireless sensor nodes. Because of the asymmetric nature of WBANs, the synchronization power is reduced by adding a WURx to the sensor node.

The impact of system level design considerations on WURx design is presented in chapter 3. The chapter starts with a survey on modulation complexity, and

it is shown that low-power receivers reported in literature either use envelope-detector based OOK modulation or FSK modulation. While the reported OOK receivers have lower power consumption, their inherent non-linear nature makes them susceptible to interferers and blockers. It is proven that by increasing the modulation index of FSK modulation the receiver becomes less susceptible for phase noise, I/Q imbalance, LO feed-through and 1/f noise. Therefore, a zero-IF receiver using wideband FSK is proposed.

Subsequently, chapter 4 shows architecture design trade-offs for zero-IF WURx receivers. The mixer-first architecture is studied in depth and shown to be a viable alternative for low-power WURx design, since the noise figure requirement is relaxed. Moreover, power consumption is reduced by exploiting the reduced wideband FSK receiver phase noise requirement. Combined with technology scaling the reduced phase noise requirement favors ring oscillators above LC oscillators. At the end of the chapter an automatic frequency control (AFC) loop is introduced. The low-power AFC loop replaces the power consuming phase locked loop.

Chapter 5 validates the viability of the low-power mixer-first architecture introduced in earlier chapters. A first version of the WURx front-end is fabricated in 90nm CMOS technology. Its functionality is confirmed by measurements. The receiver consumes only 126µW and achieves a sensitivity of -65dBm at 50kbps. Additionally, a graphical method is used to compare the WURx front-end with literature.

In chapter 6 an improved version of the WURx front-end is presented. To increase the receiver sensitivity compared to the first WURx version, the mixer duty cycle is reduced from 50% to 25%. Besides the circuit level improvements also a FSK modulator and AFC loop are implemented on chip. The second WURx receiver is fabricated in 40nm CMOS instead of 90nm, which is only fully utilized in the switching transistors in the passive mixer. The smaller switch size reduces the LO power needed to drive them. The power consumption of the second version is increased to 329µW. However, its sensitivity is improved to -74dBm at 125kbps. Moreover, bit rates up to 1.25Mbps are supported leading to a energy efficiency of 0.26nJ/bit.

At the end of the thesis conclusions are drawn in chapter 7.

APPENDIX G

SAMENVATTING

Wake-up Receiver Based Ultra-Low-Power WBAN

SENSOR nodes die gebruikt worden in draadloze body-area netwerken (WBAN) maken meestal gebruik van energie-harvesters of kleine batterijen. Bovendien is het vaak niet praktisch of zelfs onmogelijk om de batterijen regelmatig te vervangen of op te laden. Daarom is het belangrijk om het energieverbruik van de nodes te minimaliseren. Om het gemiddelde energieverbruik van de sensor nodes te minimaliseren worden de nodes zo vaak en lang mogelijk in de energiezuinige slaapstand gehouden, wat de netwerksynchronisatie bemoeilijkt. Aangezien de gemiddelde packetrate laag is, en een lange link-setup latency is toegestaan, is het gunstig om een wake-up-receiver (WURx) te gebruiken voor de netwerk synchronisatie. Dit proefschrift richt zich op strategieën om op netwerk-, systeem- en circuitniveau het energieverbruik van de WURx te minimaliseren.

In hoofdstuk 2 worden WBAN eigenschappen bestudeerd. Een singlehop netwerktopologie wordt gebruikt, omdat de maximale afstand tussen zender en ontvanger oangeveer 10 meter is. Verder is aangetoond dat netwerksymmetrie en synchronisatie een grote invloed heeft op het gemiddelde energieverbruik van draadloze sensor nodes. Het energieverbruik dat nodig is voor de synchronisatie kan worden verminderd door toevoeging van een WURx aan de sensor node, omdat WBAN asymmetrische netwerken zijn.

De impact van systeemniveaukeuzes op het ontwerp van WURx worden nader bestudeerd in hoofdstuk 3. Het hoofdstuk begint met een overzicht van de com-

plexiteit van verschillende modulatie types. Uit eerder gepubliceerd werk blijkt dat de meeste energiezuinige ontvangers gebruik maken van niet-coherente OOK of FSK modulatie. De gepubliceerde OOK ontvangers hebben vaak een lager stroomverbruik, maar hebben als nadeel dat ze gevoeliger zijn voor stoorzenders doordat ze gebruik maken van niet-lineaire omhullende detectoren. Verder wordt bewezen dat FSK ontvangers minder gevoelig worden voor I/Q onbalans, 1/f ruis, faseruis en LO feed-through als de FSK modulatie index verhoogd wordt. Daarom wordt gekozen voor een zero-IF ontvanger met wideband FSK modulatie.

Vervolgens worden in hoofdstuk 4 verschillende zero-IF WURx ontwerp keuzes besproken, en wordt de “mixer-eerst” architectuur gepresenteerd en geanalyseerd. In deze architectuur is de LNA verwijderd en is de mixer het eerste circuit in de ontvangerketen. Met deze architectuur kan het energieverbruik verlaagd worden omdat het ontvangen signaal niet versterkt wordt op RF frequenties, maar in de basisband. Doordat de LNA ontbreekt, is het ruisgetal groter dan in conventionele ontvangers. Aangezien de afstand tussen zender en ontvanger klein is, kan het verhoogde ruisgetal worden toegelaten. Bovendien is het stroomverbruik verminderd door gebruik te maken van de gereduceerde eisen aan de faseruis. Door hogere faseruis toe te staan en gebruik te maken van technologie schaling zijn ringoscillatoren een beter alternatief dan LC oscillatoren. Aan het einde van het hoofdstuk wordt de energiezuinige automatische frequentieregeling terugkoppellus (AFC) als alternatief voor de PLL gepresenteerd.

In hoofdstuk 5 wordt de “mixer-eerst” architectuur gevalideerd door een 90nm CMOS implementatie. De functionaliteit is bevestigd door metingen. De ontvanger verbruikt slechts 126µW en heeft een gevoeligheid van -65dBm bij een bitrate van 50kbps. Daarnaast wordt op grafische wijze het WURx front-end vergeleken met de literatuur. In hoofdstuk 6 wordt een verbeterde versie van het WURx front-end gepresenteerd. Om de gevoeligheid van de ontvanger te verhogen ten opzichte van de eerste WURx versie, is de mixer duty cycle verlaagd van 50% tot 25%. Naast de aangepaste duty cycle, is ook een FSK modulator en AFC lus toegevoegd op de chip. De tweede WURx ontvanger is gefabriceerd in 40nm CMOS in plaats van de eerder gebruikte 90nm, die slechts ten volle wordt benut in de schakeltransistoren in de passieve mixer. De kleinere switch vermindert het benodigde LO vermogen dat nodig is om ze te schakelen. Het energieverbruik van de tweede versie is verhoogd tot 329µW, de gevoeligheid is echter verbeterd naar -74dBm bij 125kbps. Bovendien worden bitrates tot 1.25Mbps ondersteund en is het minimale energieverbruik per bit slechts 0.26nJ/bit.

APPENDIX H

INDEX

APPENDIX I

ACKNOWLEDGMENT

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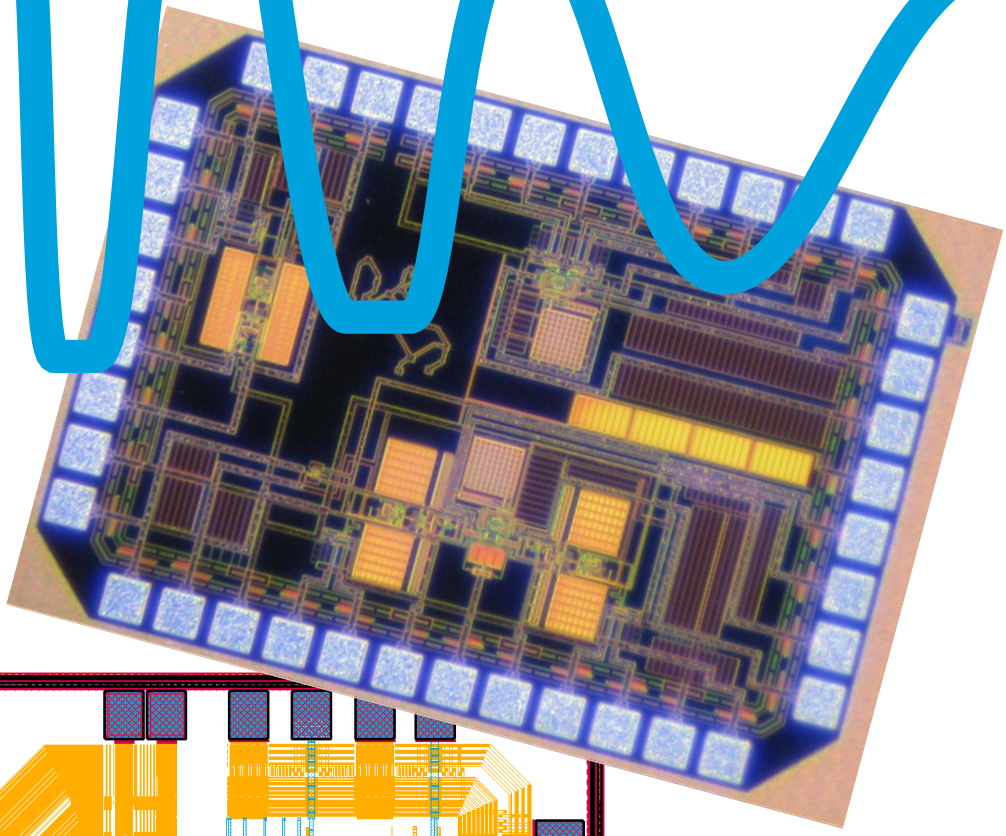
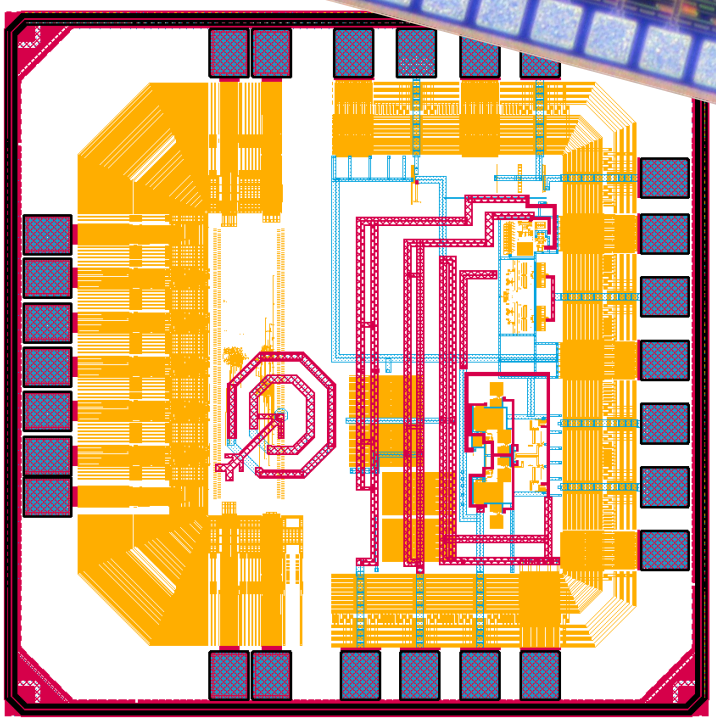
APPENDIX J

BIOGRAPHY

Maarten Lont was born Steinheim, Germany, in 1983. After finishing high school "VWO" at the "Merewade College" in Gorinchem, The Netherlands, he started the Bachelor Electrical Engineering at the Eindhoven University of Technology, The Netherlands, in 2002. He received his Bachelor and Master of science in Electrical Engineering in 2005 and 2008 respectively. For his Master thesis project he designed, implemented and evaluated a 60GHz VCO at NXP research in Eindhoven.

In 2008 he started pursuing a PhD degree on the design of low-power Wake-up Receivers at Eindhoven University of Technology with close cooperation with IMEC-NL. After his PhD study he joined IMEC-NL in the wireless group as a full-time researcher in 2012, where he is working on low-power transceiver architectures.





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