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Citation for published version (APA):
Verhoeven, A. (2004). Digital linear control theory for automatic stepsize control. In *The 5th International Workshop Scientific Computing in Electrical Engineering (SCEE), Capo d'Orlando, 5-9 September 2004 : book of abstracts* (pp. 60-62). University of Catania.

Document status and date:
Published: 01/01/2004

Document Version:
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
• The final author version and the galley proof are versions of the publication after peer review.
• The final published version features the final layout of the paper including the volume, issue and page numbers.

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Download date: 17. Nov. 2023

Digital linear control theory for automatic stepsize control

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Abstract. Numerical integration methods are used to find the numerical solution of the transient analysis of electrical circuits. Because the electrical circuits are modelled by stiff differential algebraic equations, the BDF-methods are very popular in circuit simulation. Error control is used to handle with the trade-off between efficiency and accuracy. For optimization purposes smooth behaviour of the errors and the stepsizes is wanted.

Application of digital linear control theory

Error control can also be considered from a control-theoretic approach. For onestep methods, the local error estimate $\hat{r}_n$ satisfies the following asymptotical model, which only depends on the last stepsize

$$\hat{r}_n = \hat{\phi}_n h_n^P.$$

In logarithmic form, we get the next linear model.

$$\log \hat{r}_n = P \log h_n + \log \hat{\phi}_n. \tag{1}$$

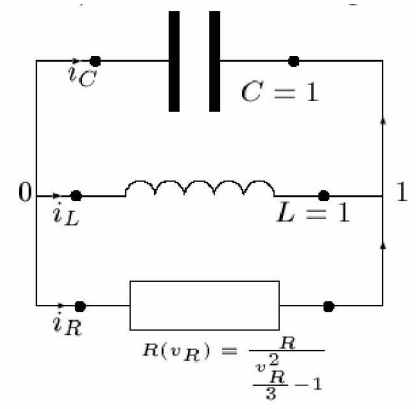
Here $\log \hat{r}_n$ is viewed as the output of this system, which depends on the input $\log h_n$ and an unknown disturbance $\log \hat{\phi}_n$. The goal is to keep the output close to a reference level $\log \varepsilon$ means of the input. A simple controller with this task is

$$h_n = \left(\frac{\varepsilon}{\hat{r}_{n-1}} \right)^{\frac{1}{P}} h_{n-1} \qquad or \qquad \log h_n - \log h_{n-1} = \frac{1}{P(\log \varepsilon - \log \hat{r}_{n-1})}. \tag{2}$$

For multistep methods, the error estimate also depends on the previous stepsizes. It is still possible to use the onestep model (1) or to apply linearization techniques. If the stepsize control process is correctly modelled, a finite order digital linear controller can be designed. The closed loop dynamics of the error model and the used controller are determined by the roots of the characteristic equation. For stability, it is necessary that these roots must be situated within the complex unity circle. If the disturbance $\log \hat{\phi}_n$ is a polynomial of degree $p_A - 1$ and the errors $\hat{r}_n$ are equal to the reference level ε, the controller has adaptivity order p_A. If $p_A \geq 1$ and the closed loop dynamics are stable, the output $\log \hat{r}_n$ will converge to the wanted reference level $\log \varepsilon$. The controller can also have filter properties with respect to the output $\log \hat{r}_n$ or the input $\log h_n$.
In the presentation, I will discuss the application of digital linear control theory for the transient simulation of electrical simulation more profoundly. From numerical experiments, it appears possible to get smooth results while the computational workload remains about the same or even decreases.

Example of adaptivity

Consider the initial value problem (VandePol equation) for the following electrical circuit:



$$\frac{dV_1}{dt} + i_L + 30V_1\left(\frac{V_1^2}{3} - 1\right) = 0 \quad V_1(0) = 0$$

$$\frac{di_L}{dt} - V_1 = 0 \qquad i_L(0) = 1$$

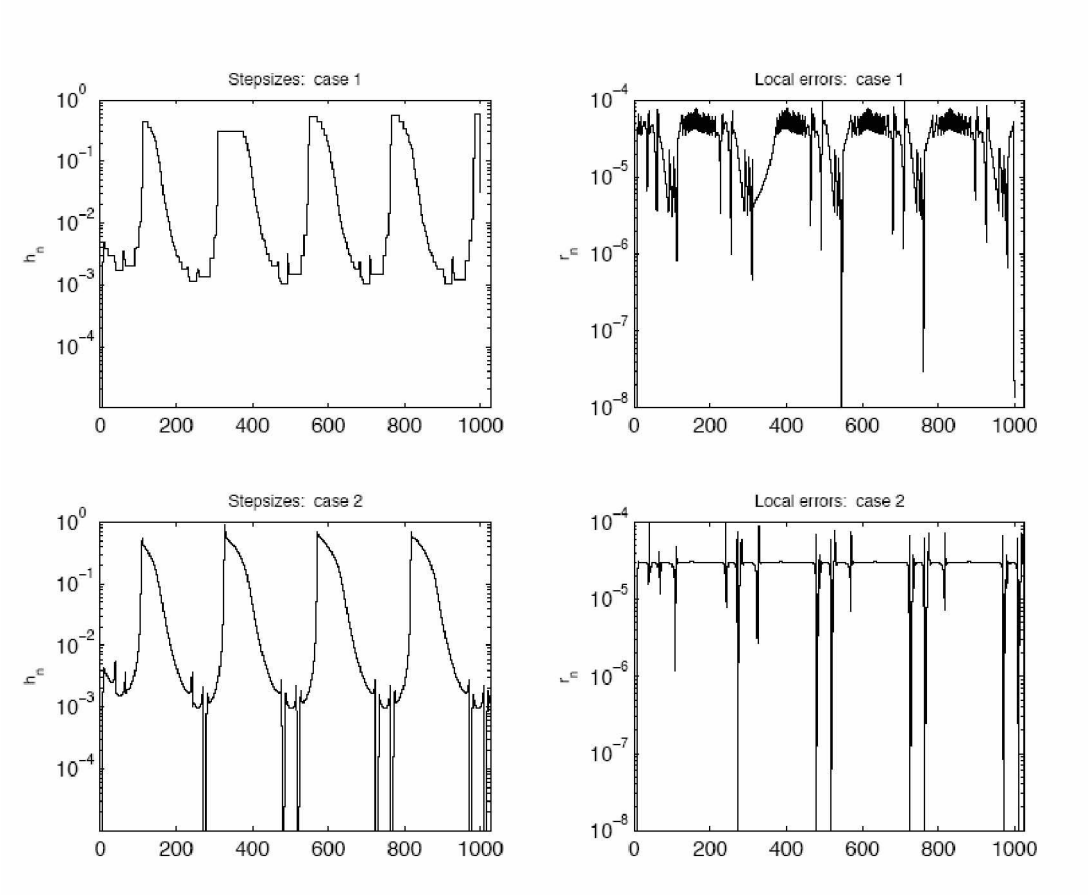


Figure 1: Stepsize and error sequences for the two tested controllers.

This IVP is solved by means of the BDF2 method with tolerance level TOL = 1e-4 and reference level ε = 0.3TOL. A frequently used controller is (2) with $p_A = 1$ and which pole is equal to zero.

$$I \quad h_n = \left(\frac{\varepsilon}{\hat{r}_{n-1}}\right)^{\frac{1}{3}} h_{n-1} \qquad (p_A = 1)$$

Often, this controller is used in combination with a buffer, e.g.

$$\frac{h_n}{h_{n-1}} \in [0.8, 2] \Rightarrow h_n = h_{n-1}.$$

Consider the next second order adaptive stepsize controller, which poles are equal to 0.2. This means that it is able to predict linear trends of the disturbance $\log\hat{\phi}$.

$$II \quad \frac{h_n}{h_{n-1}} = \left(\frac{\varepsilon}{\hat{r}_{n-1}}\right)^{\frac{8}{15}} \left(\frac{\hat{r}_{n-2}}{\hat{r}_{n-1}}\right)^{-\frac{8}{25}} \frac{h_{n-1}}{h_{n-2}} \qquad (p_A = 2)$$

For the next two cases, the IVP has been solved.

case 1 Controller I with buffer.
case 2 Controller II.

For these cases, 1686 and 2054 Newton iterations are required, respectively. In Figure 1, the resulting stepsizes and errors are shown. The best results are obtained in case 2, because of the better adaptivity at the cost of a slight increase of Newton iterations. Because of the higher smoothness of case 2, the safety factor could be increased for case 2. Indeed, for ε = 0.6TOL, the cases need 1847 and 1667 Newton iterations, respectively.

References

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Towards One-Step Multirate-Methods In Full Chip Design

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Abstract. In full chip design the behaviour of electrical circuits with thousands or even millions of nodes and transistors has to be analysed by numerical simulation before a circuit is build physically.
Modified nodal analysis (MNA) is applied to get equations describing the lumped electrical network. These differential algebraic equations (DAEs) are generated automatically from the circuit's topology and element models. To solve the occuring DAE system numerically common integrators treat the system as one unit and use just one overall stepsize for each step.
In most applications different parts of large integrated electrical circuits com- prise different functionality and therefore show different transient behaviour at every instant of time. To save computational costs this physical property can be brought forward to the numerical integration of the network-DAE by applying a multirate method that uses different stepsizes for the different parts of the circuit. This prevents parts to be computed more often, i. e. on a finer grid, than necessary to guarantee given error tolerances.
To get an appropriate partitioning of the network, we divide the circuit into several subcircuits, duplicate the boundary nodes and connect them by virtual voltage sources. This causes branch currents u through the coupling voltage sources as additional unknowns and the constraint that the node potentials of the connected subsystems have to coincide at the boundaries yields an additional algebraic equation.
If the considered electrical circuit is decomposed into r subcircuits, charge oriented MNA [1] thus produces for each of them (i = 1, . . . , r)