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Controlled coupling of semiconductor quantum dots to optical micro-cavities

PROEFSCHRIFT

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof.dr.ir. F.P.T. Baaijens, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op woensdag 6 mei 2015 om 16:00 uur

door

Tian Xia

geboren te Nanjing, China

Dit proefschrift is goedgekeurd door de promotoren en de samenstelling van de promotiecommissie is als volgt:

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dr. E. Pelucchi (University College Cork)
prof.dr. P.M. Koenraad
dr. R.W. van der Heijden

To my family…

Abstract

Quantum photonic integrated circuits (QPIC), which allow the generation, transmission, manipulation and detection of single photons on a semiconductor chip, are a strong candidate for solid-state quantum information processing and communication systems. Taking advantage of the epitaxial growth techniques of semiconductor materials and the semiconductor processing technology, components of the QPIC systems can be fabricated and integrated together: epitaxial quantum dots (QDs), serving as single-photon sources, can be easily embedded into the device structure during the epitaxial growth; photonic crystal cavities (PCCs) can be fabricated by using advanced lithography and etching techniques around the QDs to control their spontaneous emission process; waveguides and superconducting single photon detectors (SSPDs) can be fabricated on the same chip to form interconnection channels for single-photon transmission between different elements of the QPIC system and to detect single photons with ultrahigh sensitivity.

This thesis focuses on the controlled generation of single photons by coupling the epitaxial QDs to photonic crystal optical micro-cavities. In the first part of the thesis, the spatial alignment of the QDs with the cavity is studied. The growth optimization of self-assembled QDs on planar substrates and the growth of position-controlled low-density QDs on patterned substrates with pre-defined nanoholes are investigated. Arrays of site-controlled multiple QDs can be grown with various site-to-site distances without the formation of interstitials. To optimize the desorption procedure of the native oxide on the patterned substrates, the In-assisted deoxidation method is systematically investigated and optimized.

In the second part of the thesis, the spectral alignment of the QDs and the PCCs is studied. A novel nano-opto-electromechanical system (NOEMS) device is demonstrated. This device allows an independent control of the exciton energy of QDs via the Stark effect and the electromechanical tuning of the cavity mode wavelength of a double-slab PCC. At 10 K, tuning of the mode wavelength over 3 nm as well as a ~ 6 nm/V tunability of the emission wavelength of QDs has been achieved. This device enables the in-situ alignment of the cavity mode to a single excitonic line of the QDs with two degrees of freedom and the enhancement of the spontaneous emission rate of the QDs due to the Purcell effect. This device facilitates the realization of two-photon bunching experiments on chip and is therefore a step towards a complete QPIC system. In addition, a novel mechanical-stress-free vertically-aligned double-nanobeam structure has been designed and fabricated, and optomechanical coupling effects have been demonstrated.

Contents

CHAPTER 1

Introduction

In this chapter, the author first briefly reviews the applications of quantum information, processing and communications. After that, the necessity of establishing a solid-state quantum-photonic integrated-circuit (QPIC) will be explained together with the approach of our group at TU/e. Then, the author will discuss in more detail the methods and related physics to realize on-chip controllable single-photon sources in solid-state QPIC.

1.1 Quantum information processing and communication (QIPC)

1.1.1 Strategic motivations behind the development of QIPC

Nowadays, the young scientific discipline of quantum information processing and communication (QIPC) has become one of the most exciting scientific frontiers. [1] However, the driving force behind the development of this field should not only be seen as science or technology itself. The strategic importance of the QIPC in national defense and economy for countries in the 21century has even been compared with the 'atomic bombs' in war times. [2]

From the national defense point of view, on one hand, the expected computing power of quantum computers exceeds any classical computers. [3] This means that they may solve problems that classical computers cannot or will take a very long time to solve. On the other hand, quantum communication guarantees an absolutely secure way of communication, thanks to the quantum key distribution (QKD) technique. [4]

From the economy point of view, the QIPC technology is considered to be the footstones of the information technology in the 'post Moore's-law time' [5] and is expected to open up a new quantum information technology industry [6] based on it. In the past 50 years, the development of the semiconductor industry has followed the Intel co-founder Gordon Moore's forecast that 'The number of transistors incorporated in a chip will approximately double every 24 months' (known as the 'Moore's law'). However, it can be extrapolated from the Moore's law that around 2020, the size of the elementary devices will be so small that the number of electrons per device will decrease down to 1 electron/device. At the atomic scale, quantum effects will appear. It has been predicted that the breakdown of the Moore's law is inevitable due to heat and leakage issues. [7] Although the information technology (IT) industry (such as Intel) is still putting much efforts to follow or prolong Moore's law by minimizing the size of transistors to the nanometer level[8],[9], in fact the cost in the fabrication has increased so much that the long-lasting growth of economic interests will be difficult to sustain. Therefore, heading for a new QIPC industry is expected to be an inevitable trend in the future. [6]

1.1.2 Quantum key distribution (QKD) technology
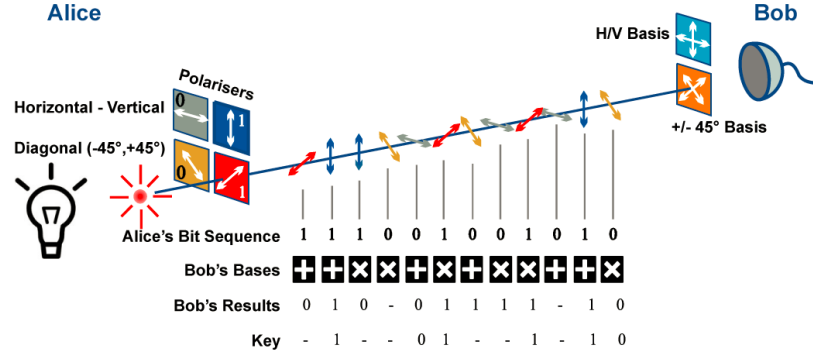
Fig.1.1 Schematic illustration of the basic working principle of QKD [11]: The value of a bit is encoded to the polarization state of a photon. Two bases (horizontal-vertical basis and diagonal basis) can be chosen to set the state of the photon. The sender Alice sends the sequence of bits with randomly chosen bases and the receiver Bob measures the bit sequence with random bases as well. If the basis that Bob uses in decoding does not match the one that Alice uses in encoding, Bob will have a 50% chance of failure in detecting the information due to the quantum nature of the states. Alice and Bob discuss in public channels the bases that they have used. They discard the bits for which their bases do not match, leaving the remaining bit string as a confidential key. In case of the presence of an eavesdropper, errors will be introduced in Bob's measurement and will be discovered when Alice and Bob compare a part of the remaining bit string.

Using the nature of quantum mechanics, the QKD technology guarantees a secure way of transmitting confidential information and establishes the bases for quantum communication networks. [1], [2], [4], [10] It allows different parties in the communication network to generate and distribute random secret keys in the quantum channels; and to evaluate and decide the credibility of the exchanged information and confidentiality of the quantum channel in classical public telecommunication channels.

Up to now, it is widely believed that the photon, known as 'flying qubit', is the only form of qubit which is suitable for coding and carrying quantum information in existing medium-long distance (100 to 1000 km) optical-fiber-based telecommunication systems and the ultra-long-distance free-space communication systems. [1], [10] In 1984, Charles Bennett and Gilles Brassard proposed the first protocol (known as 'BB84' protocol) to illustrate the way of quantum communication via the polarized states of photons. [12], [13] The basic working principle of QKD is illustrated in Fig. 1.1. [11]

Photons are ideal quantum information carriers for telecommunication at long distances based on the following facts:

(a) Photons couple weakly with the surrounding environment so that quantum coherence of superposition states can be maintained even long distances. [13] (b) photons can be detected efficiently and precisely by using existing single photon detectors[14], such as nanowire

superconducting single photon detectors (SSPDs) [15]-[20], avalanche photodiodes (APDs) [21]-[23] , photomultipliers (PMTs) [24] , etc.

1.1.3 Quantum computing and its possible platforms

In classical computing, information is encoded in to a series of 'bits', with the state of each bit being either 0 or 1. For example, the conventional form of 'bit' in a classical computer is an electrical voltage, with a low value for coding 0 and a high value in coding 1. The information processing is carried out by gate operations performed by transistors in circuits of classical computers.

In quantum computing, information is encoded into a 'qubit', which is a linear superposition of the $|0\rangle$ and $|1\rangle$ states of a quantum system:

$$|\psi\rangle = \alpha|0\rangle + \beta|1\rangle, \tag{1.1}$$

where α and β are probability amplitudes and satisfy $|\alpha|^2 + |\beta|^2 = 1$. Unlike the two definite states of classical bit, a qubit represents all the possible linear combinations of $|0\rangle$ and $|1\rangle$. This can be a geometrically represented by the Bloch sphere (Fig 1.2): [25]
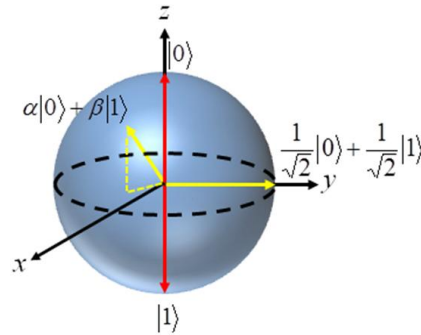
Fig 1.2 Illustration of Bloch sphere. The states $|0\rangle$ and $|1\rangle$ are represented by the two poles and a general qubit by a point on the surface of the sphere.

Similar to classical computers, qubits information can be processed in parallel via controlled-NOT (CNOT) gates. Therefore, due to the strong parallelism in the data processing, a quantum computer is expected to beat the classical computers and have immensely powerful data processing capability in a number of relevant computation and processing tasks. [1], [3], [25]

A number of potential physical platforms are under investigation for the implementation of quantum computers: trapped ions [26]; neutral atoms [27], molecules and cavity QED [28], [29] ; solid state superconducting circuits [30]; semiconductor quantum dots [31]; photons [32]; impurity spins in solids [33] and single molecular clusters [34]. However, none of the above mentioned technologies provides a perfect solution for quantum computing. The most realistic platform for quantum

computation is a hybrid system, which integrates the transmission of quantum information via the photons and the storage and processing of quantum states via neutral atoms, ions, quantum dots, etc. [1], [3]

1.1.4 Quantum simulation

A quantum simulator (such as boson-sampling circuit [35]) is expected to simulate the behavior of complex quantum systems and model complex quantum mechanics problems, which are difficult to be investigated by experiments or classical computation, by using a controlled quantum system. The idea of quantum simulation was proposed by Richard Feynman in 1982. [36] Till now, several platforms (e.g., based on trapped ions, atoms, superconducting circuits and linear optics) have been proposed to realize quantum simulators. [37]

1.1.5 Quantum photonic integration

The objective of the thesis is the investigation of some of the key building blocks for the realization of a solid-state QPIC. The QPIC is expected to provide feasible solutions for quantum communication and quantum computation by implementing single-photon generation, transmission, manipulation and detection on a micro-chip. A sketch of the structure of QPIC is presented in Fig .1.3.
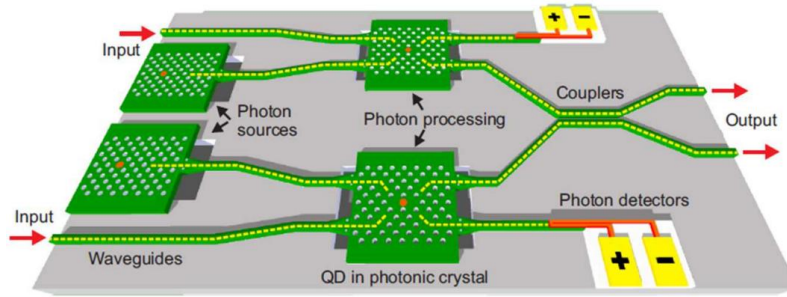
Fig. 1.3 Sketch of a QPIC. Drawn by Dr. R. Johne.

Several building blocks of the QPIC are:

- **Quantum dots as single-photon emitters**: An ideal single-photon emitter emits light with the photon number distribution corresponding to the Fock state (n=1). Every time it is triggered, it emits one and just one photon. Epitaxial quantum dots (EQDs), which have atomic-like discrete energy states, are chosen as single photon sources in solid-state QPICs. Details about the EQDs will be explained in Section 1.2.

- **Waveguides:** Waveguides (photonic crystal waveguides and ridge waveguides) are used to form interconnections between different elements on chip. Photonic crystal waveguides (PCWG) [38] (Fig 1.7) are line-defects of photonic crystals in which light is guided and propagates along the defect and is vertically confined in the PhC due to total internal reflection. [38] The ridge waveguide [40] (RWG) is another kind of more common waveguide for light transmission. It is widely used in photonic integrated circuits. [41]

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- **Single-photon processors:** Single-photon processors carry out tasks such as the storage (quantum memory [42]) and the nonlinear processing of quantum information (single photon transistor [42]). In QPIC, a single-photon processor is expected to be realized by waveguide-coupled QD-PCC devices.

- **Photon couplers:** Photon couplers implement the task of a beam splitter. When a single photon incidents on the input of the coupler, the probability for the output of the photon splits equally among the two output ends. When two identical photons are simultaneously incident on the two inputs of the coupler, they are always channeled into the same output port of the coupler. [43]

- **Single photon detectors (SPDs):** QPIC need SPDs working at telecommunication wavelength to detect single photons. The existing telecom-wavelength SPDs include [14]: PMTs, InGaAs APDs, transition edge sensors (TES) and superconducting single photon detectors (SSPD). We employ nanowire superconducting single photon detectors (SSPD) as SPDs in our integration system, since they provide the best performance among the existing SPDs working at telecommunication wavelength, in terms of high quantum efficiency (93%), low dark counts (~ 1 Hz), small timing jitter (< 50 ps) and short dead time (~ ns), etc. [45]

- **Input/output optical couplers:** Input/output couplers are interfaces between the QPIC and outside environment. Light input/output can be achieved by coupling light to the side facet or the top of the chip.

The thesis focuses on the fabrication of spatially and spectrally controlled single photon sources. In Section 1.2, III/V semiconductor epitaxial QDs, position-control of III-V QDs, Stark tuning of QDs' exciton energy, double slab-PCCs are discussed in more details.

1.2 Controlled single photon sources

1.2.1 Epitaxial quantum dots

Quantum dots (QDs) are zero-dimensional semiconductor nanocrystals which provide three-dimensional tight confinement of carriers in a semiconductor material. When the scale of the confinement region is comparable to the de Broglie wavelength of the carriers, the quantization effect will appear, leading to sets of discrete atomic-like electronic energy levels in QDs as a result. [46]

QDs can be created with many approaches: (a) top down approach: by etching of quantum wells, ion implantation or locally annealing of QWs; (b) by infilling low bandgap energy materials in corrugated layers with high band-gap energy material (c) by embedding low band-gap energy material into higher energy sections in nanowires (d) by colloidal synthesis, etc. [47]

Epitaxial quantum dots (EQDs) are fabricated by epitaxially embedding 3-dimensional nanostructures with lower bandgap into semiconductor material with higher bandgap. Due to their

atomic-like discrete energy states, EQDs are often referred to as 'artificial atoms' (Fig. 1.4). The reason for choosing EQDs as the single photon sources in the QPIC is based on the following facts:

(1) EQDs can be easily embedded in a semiconductor waveguide during epitaxial growth and subsequent processing; (2) EQDs can be isolated from each other either by epitaxially tuning the density of QDs (i.e. growth of ultra-low density QDs [36]) or by ex-situ processing (e.g., by plasma etching) (3) EQDs are suitable for the large-scale fabrication of multiple single-photon sources; (4) solid-state cavity quantum electrodynamics (CQED) effects (to be discussed in 1.2.4) between EQDs and optical-cavities can be used to control the spontaneous emission rate.
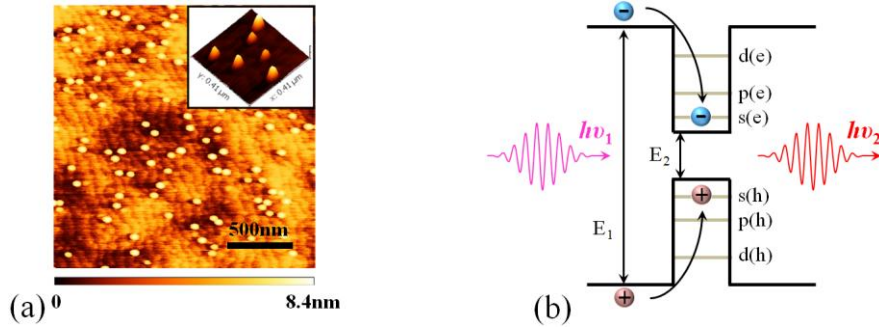
Fig 1.4 (a) 2×2 μm^2 atomic force microscopy (AFM) micrographs of low-density InAs/GaAs epitaxial quantum dots grown with molecular beam epitaxy at TU/e. The inset shows a 3D view of the quantum dots. (b) Schematic illustration and a simplified energy diagram to explain the photoluminescence process of a QD under non-resonant pumping, including the generation of an electron-hole pair upon absorption of a photon with energy of $h\nu_1$, the relaxation of carriers from the barrier into the ground state of the QD, and the emission of a photon with energy of $h\nu_2$ (with $\nu_2 < \nu_1$) from the electron-hole recombination.

Molecular beam epitaxy (MBE) [48] is an ultrahigh-vacuum deposition technique used to produce epitaxial quantum dots in QPIC. There are basically two approaches to produce QDs with MBE. One approach is the so-called **'Droplet epitaxy'** method [49]: To grow QDs, first, metal droplets are formed by a metal flux (e.g., Ga, Al, In) impinging on the sample surface in the absence of As. Then, As flux is supplied to crystallize the metal droplets into compound nanocrystals. (Fig 1.5)
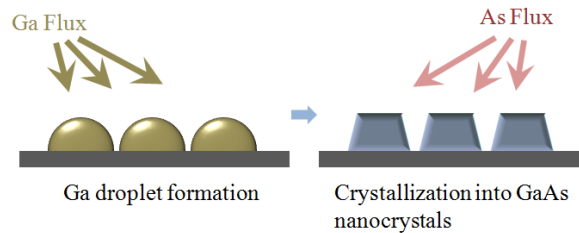
Fig 1.5 Schematic illustration of the formation of QDs (GaAs QDs on AlGaAs surface) with the droplet epitaxy method.

The advantages of this method are: (a) it provides a way to produce strain-free quantum dots, which means it has a higher degree of freedom in choosing the material of substrate and QDs

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(e.g., GaAs dots on AlGaAs, GaAs or AlGaAs on Si); [49], [50] (b) it allows the production of nanostructures with variable density, dimension and shapes (e.g., QDs, quantum rings). [46], [51] (c) it provides a way to in-situ etch the substrates with metal droplets. [52] The major disadvantage with the method is that due to the low crystallization temperature during the QDs formation, the chance of incorporating impurities is increased. This usually leads to a degradation of the optical efficiency of QDs.

The other way is the 'Stranski-Krastranow' (SK) method, which is the most widely used method to create high-optical-quality QDs. [53] To grow SK QD, the substrate material is required to have higher band-gap energy and slightly smaller lattice constants than the QD material. Take the common InAs/GaAs QDs as an example. InAs and GaAs materials have the same lattice structures (zincblende) but are characterized by a lattice mismatch of 7%. In the SK growth mode, after depositing InAs on GaAs surface, 2D InAs layers will be formed first. The lattice constant of InAs initially follows that of GaAs in the first several 2D layers. As a result of the lattice mismatch, strain is gradually accumulated at the interface and the InAs layer. When the InAs layer thickness reaches a certain critical value (named 'critical thickness', $\Theta_{critical}$), 3D nanocrystals, with lattice constant closer to the bulk InAs, will form to partially relax the strain. (Fig. 1.6)
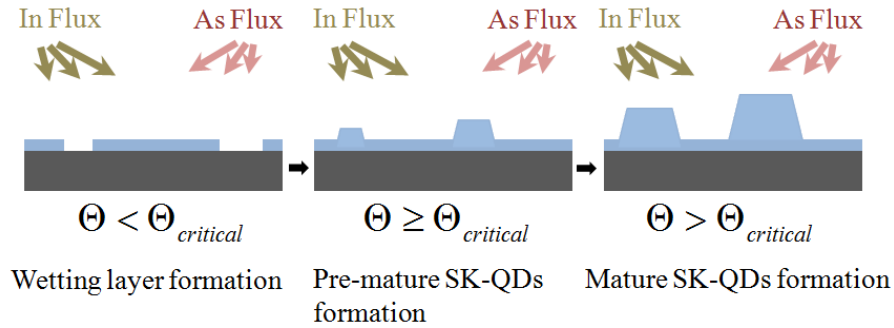
Fig. 1.6 Schematic illustration of InAs/GaAs QDs formation in S-K mode.

In QPIC studied in this thesis, the InAs/GaAs SK QDs, are chosen as single-photon emitters. Other III-V materials can also be used as QDs or substrate material: InAs/InP, GaAs/AlGaAs, InP/GaInP, CdSe/ZnSe, InN/GaN, InGaN/GaN, etc. Fig 1.7 shows a schematic representation of wavelength ranges accessible with different SK QDs. [54]
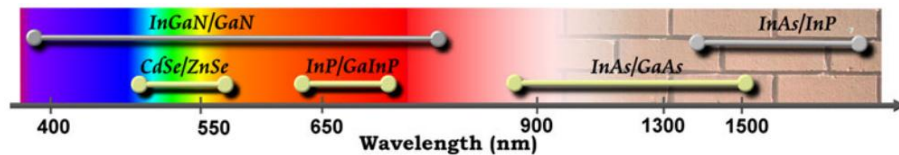
Fig. 1.7 Schematic representation of wavelength ranges with different SK QDs. The region inaccessible for Si detector is indicated in brick. [54]

Fig. 1.8 shows the spectral attenuation in a silica fiber versus wavelength and the three transmission windows. Putting Fig. 1.7 and Fig. 1.8 together, it is clearly that both InAs/GaAs and InAs/InP quantum dots emit light in the near-IR telecommunication window.
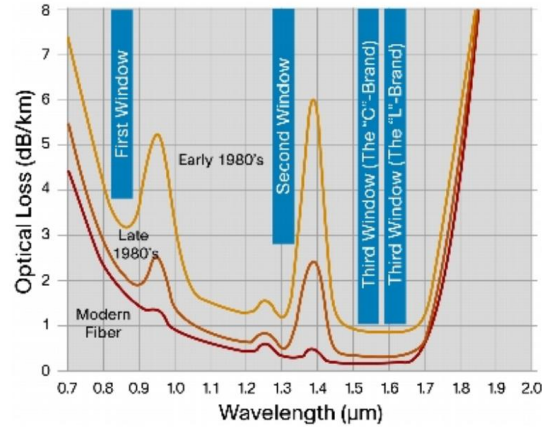
Fig. 1.8 Spectral attenuation in a silica fiber versus wavelength and transmission windows. [55]

1.2.2 Position-control of III-V quantum dots

QDs described in Section 1.2.1 are self-assembled (or self-organized) QDs which form randomly on a substrate surfaces. To achieve a controllable spatial alignment between QDs and nano-photonic devices (e.g., photonic crystal cavities, nano-pillars, optical microdisks), the fabrication of site-controlled quantum dots (SCQDs) with high precision in position is needed.

SCQDs can be fabricated with several different approaches:

1. SCQDs grown on truncated nano-pyramids

SCQDs can be created by growing QDs on top of position-controlled truncated nano-pyramids. For example, in the work of the group of Dr. Richard Nötzel at TU/e (before 2011), first, lithography and chemical techniques are used to define openings on dielectric hard masks (e.g., SiN, SiO$_2$) on the substrate. Then selective area growth is performed to create truncated nano-pyramids. After that, QDs are grown on the top of the pyramids. Fig. 1.9 shows the result of formation of site-controlled InAs QDs on InP pyramids grown by MOVPE with different shapes. [56]
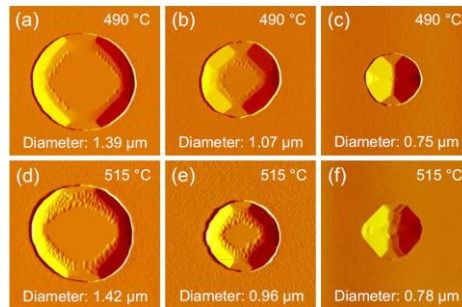
Fig. 1.9 InAs QDs grown on truncated InP nano-pyramids created with MOVPE. [56]

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2.   SCQDs grown in inverted pyramids

Formation of QDs in inverted pyramids is another approach to fabricate SCQDs [57], [58]. This approach is pursued by the groups of Dr. E. Pelucchi's group at Tyndall University (Ireland) and Prof. E. Kapon's group at EPFL (Switzerland). In the work of the Tyndall group, first, a GaAs (111)B substrate is patterned, by lithography and wet chemical etching, with arrays of inverted pyramids which have three (111)A facets. Then, a multilayer structure consisting of AlGaAs/GaAs is grown inside the inverted pyramids by MOVPE. Due to a higher growth rate on the side facets (111)A than on the bottom facets (111)B, the width of the bottom facets keeps shrinking until the system reaches a self-limited profile. [46] Then the growth rates becomes equal on (111)A side facets and (111)B facets due to capillary effects. [57] After the system has reached a self-limited profile, the growth of an (In)GaAs layer is carried out with a thickening at the bottom. A lens-shaped QD is formed at the bottom of the inverted pyramid as a result of the combination of the growth rate anisotropy and the capillary effect. (Fig. 1.10)
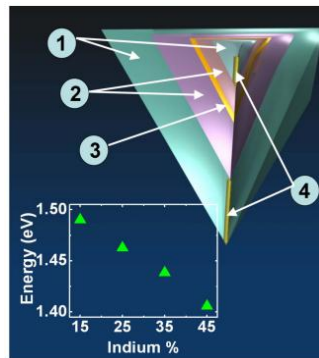
Fig. 1.10 InGaAs QDs grown with MOVPE in inverted pyramids. [57]

3.   SCQDs grown in nanoholes

Growing QDs in pre-patterned substrates with nano-holes is another way to fabricate SCQDs. It is also the method which is adopted in the work presented in this thesis. This approach is pursued, among others, by the groups of Prof. O. Schmidt and A. Rastelli in Dresden (Germany), Prof. S. Höfling, M. Kamp and A. Forchel in Würzburg (Germany), and Prof. D. Ritchie in Cambridge (UK). [59] - [64] The general procedures to create SCQDs are:

- Surface patterning: Using the combination of e-beam lithography (or nano-imprint) and wet (or dry) etching techniques to fabricate nano-hole arrays on epitaxial GaAs substrates (~ 100nm in diameter).

- Surface cleaning: Contaminants (organic & inorganic) are chemically removed from substrates. Combinations of chemicals (such as acetone, isopropanol, H_2SO_4, HCl, Dimethyl sulfoxide (DMSO), N-methylpyrrolidon (NMP)), oxygen plasma, and UV ozone ashing are used for surface cleaning.

- Buffer layer growth: The purpose of this step is to grow a thin layer to smoothen the surface and to separate the growth interface of QDs from the contaminated GaAs surface, without

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damaging the patterned nanostructures. Typically, a thin (≤ 15 nm) GaAs layer is used as buffer. In the recent publication of the Dresden group, they report the use of a 5 nm $Al_{0.75}Ga_{0.25}As$/5nm GaAs to build an interface-carrier blocking barrier to enhance the brightness of the active QDs grown on top. [63]

- Formation of SCQDs: After the deposition of the buffer layer, InAs is deposited to form SCQDs. Due to the fact that the concave nanoholes have lower surface chemical potential and that the density of atomic-steps are higher on the sidewall of holes than on the planar area, adatoms tend to migrate toward the holes and form QDs there first. [59] Therefore, when the substrate temperature is high enough to provide a large enough diffusion length for the adatoms and the amount of InAs material is set below the critical thickness of the planar area, site-controlled InAs quantum dots will be formed on patterned sites without interstitials.

To our knowledge, by now, the Cambridge group has reported the best optical quality of a single layer of SCQDs grown on patterned GaAs (100) and separated by a 15 nm GaAs buffer from the re-growth interface. [65] The average linewidth they achieved from single SCQDs is 132 ± 26 μeV and the narrowest linewidth they have obtained is 80 μeV (Fig. 1.11).
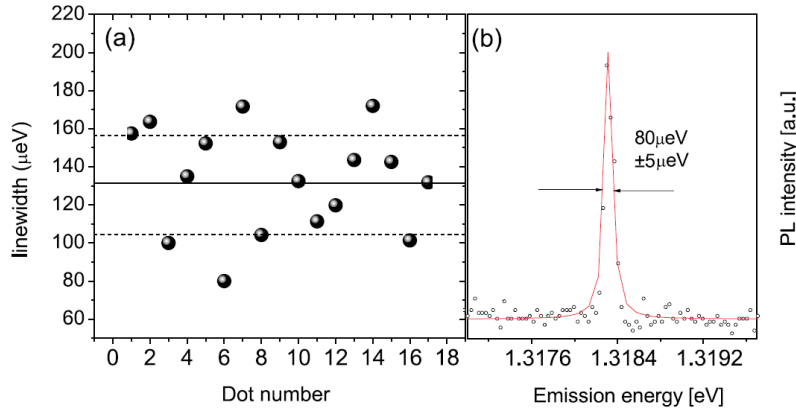
Fig. 1.11 Record linewidth obtained from single-layer SCQDs. [65] (a) Spectral linewidth over 17 chosen SCQDs. The mean linewidth is 132 ± 26 μeV. (b) Spectral line of from a SCQDs with linewidth of 80 μeV.
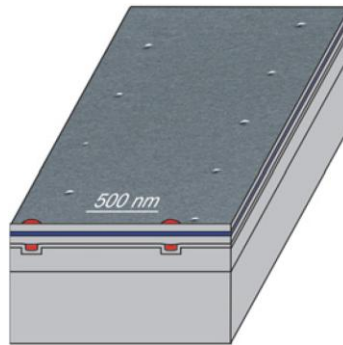
Fig. 1.12 Schematic illustration of vertically aligned two-layer stacked SCQDS. [61]

Compared to the linewidth of self-assembled QDs grown with SK mode on thick buffer layer, [66] this linewidth is still much wider. The spectral linewidth of the SCQDs is broadened due to the spectral diffusion induced by contaminants at the patterning interface.

To overcome this issue, the QD-stacking technique is used to further reduce the linewidth of SCQDs by increasing the distance between the optically-active SCQDs (on the top layer) and the contaminated re-growth interface. For example, to grow a 2-layer-stacked SCQD structures, first, a GaAs spacer layer is deposited on the capped 1st layer of SCQDs. Driven by the lower local strain field between the InAs and GaAs above the 1st layer of SCQDs, the deposition of InAs on the spacer layer will result in the nucleation of the 2nd layer of SCQDs. [61] Both the Würzburg group (Fig. 1.12) and the Dresden group have adopted this method.

In 2012, the Würzburg group has reported the observation of SCQDs with a average linewidth of 133 μeV and the narrowest observed linewidth of 25 μeV. (Fig 1.13 (a)-(b)) In 2012, the Dresden group has reported growth of SCQDs with a median value of 13 μeV for the linewidth and with 7 μeV for the narrowest linewidth (Fig 1.13 (c)), which is close to the best result reported for self-assembled QDs.
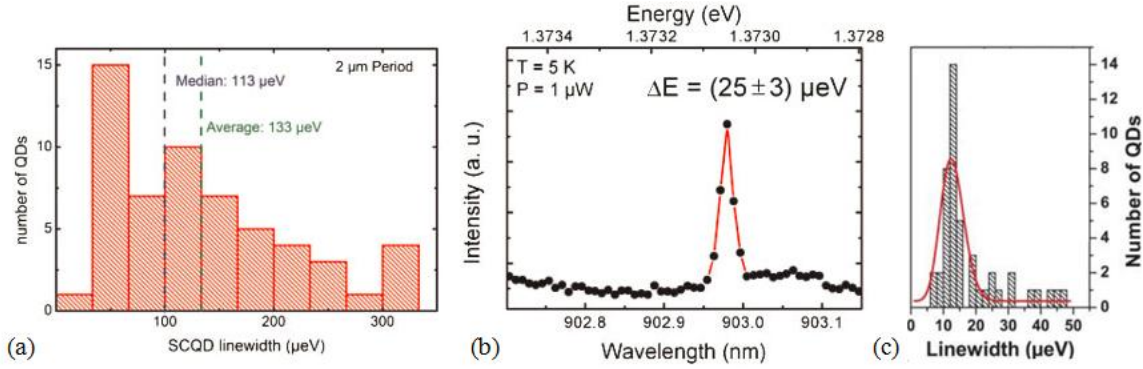
Fig. 1.13 (a)-(b) Results of record linewidth from SCQDs of Würzburg group: [62] Emission from a single SCQD with linewidth of 25 μeV. (c) Results of record linewidth from SCQDs of Dresden group. [63]

1.2.3 Stark tuning of exciton energy of QDs

Different single-photon sources in the QPIC must have the same spectrum to provide the quantum interference effect. Because the capability of controlling the structural properties of QDs during growth is limited, active tuning methods after growth are necessary to obtain sources with the same spectral features. The excitonic transition energy of QDs can be electrically tuned taking advantage of the Quantum Confined Stark Effect (QCSE): when an electric field is applied along the growth direction of the QDs, the electric field will push the electron and hole wavefunction in the opposite direction, and their relative distance will increase or decrease, depending on their relative position within the QD. [67], [68], [69]

Let us consider the self-assembled InAs/GaAs QDs, which have a graded $Ga_xIn_{1-x}As$ composition with x decreasing from base to apex, as an example. [68] When a reverse bias voltage V is applied to the QDs, which are embedded in a p-i-n structure (Fig. 1.14 (a)), the transition energy of the QDs is shifted with the change of the field (Fig. 1.14 (b)). The electric field F_e dependence of the transition energies E satisfies a parabolic expression:

$$E = E_0 + pF_e + \beta F_e^2 \tag{1.2}$$

The first term E_0 is the transition energy in absence of external field ($F_e = 0$). The second term pF_e expresses the linear shift of the transition energy with external electric field. p is the permanent dipole moment inside the QD, coming from the electron-hole wavefunction separation in the z-direction due to the asymmetric QD-shape, compositional gradients and piezoelectricity. The third term shows the quadratic shift in the exciton energy under the electric field F_e, resulting from the polarizability of the dot, which reflects the response of the electron-hole separation to the field. [68]

Fig. 1.15 shows examples of the calculated electron-hole wavefunction under different external fields for truncated InAs/GaAs QDs. Under zero-field (0 kV/cm), the center of the hole-wavefunction is located above the electrons'; under reverse bias, the electron and hole wavefunctions are pulled apart.
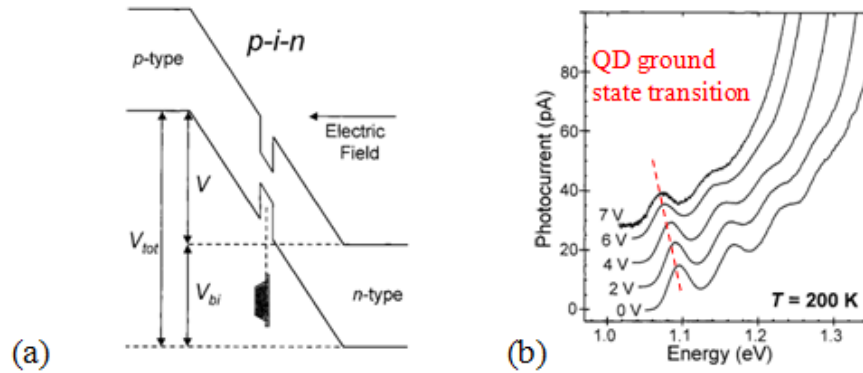
Fig.1.14 (a) Band diagram of a p-i-n device under reverse bias V. [68] (b) Photocurrent spectra of a sample for different applied voltages at the temperature of 200 K. [68]
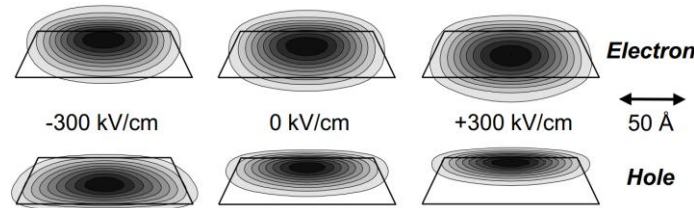
Fig. 1.15 Calculated electron-hole probability densities in an InGaAs QD under different electric fields. [68]

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The Stark tuning range of QDs' transition energy is limited by the process of carrier tunneling. When the tunneling rate is comparable to the radiative recombination rate, the emission efficiency of QDs decreases and the transition broadens. To suppress the carrier tunneling process, an effective method is to embed QDs into carrier-confinement-barriers (layers with large band-gap energies). In this case, the height of the triangular barrier can be extended, resulting in a decreased tunneling rate.[69] Fig. 1.16 shows the qualitative illustration of the band diagram of an InAs QD embedded in GaAs with AlGaAs claddings.
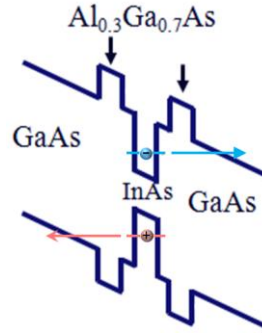
Fig. 1.16 Schematic band diagram of a biased InAs/GaAs QD embedded in AlGaAs carrier confinement layers. The arrows illustrate the tunneling of carriers in the QD to the barriers.

1.2.4 Photonic Crystal Cavities

According to the Purcell effect, the spontaneous emission rate of atoms can be enhanced by controlling the atoms' boundary conditions of the electromagnetic field with a cavity. [71] The Photonic Crystal Cavities (PCCs) are dielectric cavities with periodically modulated dielectric constants. Due to the fact that PCCs provide a high quality factor/mode volume ratio among different approaches to optical micro-cavities, we fabricate PCCs around QD emitters in QPIC to control their spontaneous emission rate taking advantage of the Purcell effect. The normal forms of PCCs are planar 1D nanobeams, planar 2D hole arrays, and 3D pile structures (Fig. 1.17).
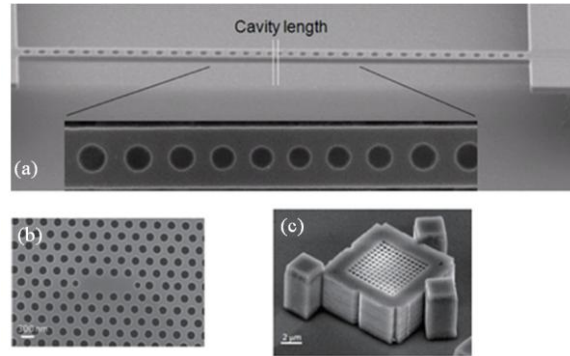
Fig. 1.17 Examples of PCCs: 1D nanobeams (a), [72] 2D planar hole arrays (b), [73] 3D woodpile PCC (c). [74]

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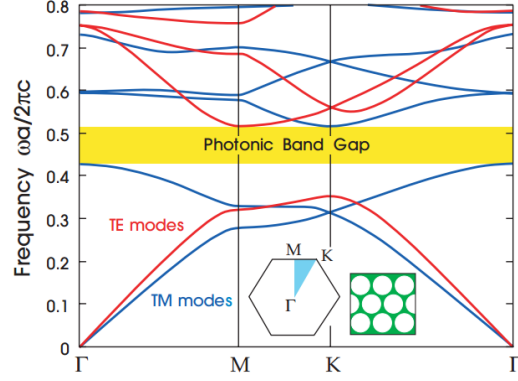
Fig. 1.18 The photonic band structure of modes of a PCC with a triangular array of holes. [75]

The PCCs we use in QPICs are 2D PCCs. In analogy to the concept of the bandgap of the semiconductor material, due to the periodic structure of the PCC, the interference of light in the 2D PCCs creates a range of wavelengths which cannot propagate in the PCCs, known as the 'photonic band gap'. (Fig. 1.18) By creating a defect in the structure of a 2D PCC, the localization of modes within the photonic band gap will happen and light will be confined in the defect. [75]

1.2.5 Spontaneous emission rate control of single QDs by tunable PCCs

By adding an optical micro-cavity around a QD emitter, the spontaneous emission rate of the QD can be enhanced, allowing the increase of the number of photons emitted from the cavity per unit time. To control the spontaneous emission rate of the QD embedded in the PCC cavity, the wavelength of the PCC should be spectrally aligned to the emission energy of the QD. In experiments, due to technical limitations (e.g., structural defects created in processing, aging/oxidation of material in air), it is difficult to create a PCC with mode exactly at a desired wavelength. Therefore, a novel technology is needed for the real-time control of the PCC mode wavelength.
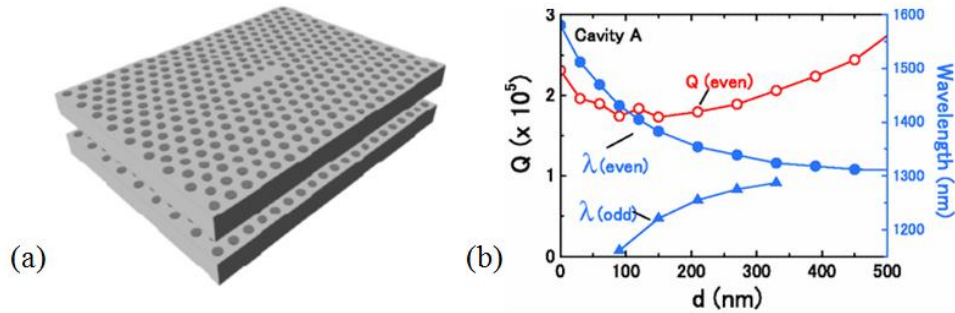
Fig 1.19 Proposal of double-slab PCCs in Notomi's paper. [76] (a) Schematic drawing of a double-slab PCC. (b) Resonant wavelength and quality factor of the double-slab PCC as a function of the inter-membrane distance.

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In 2006, Notomi et al.[76] theoretically proposed a novel solution. They predicted that when two identical PCCs-membranes are brought closely to each other, the evanescent tail of guided modes from each PCC will penetrate to the slab of the other to form two coupled modes, and the modes' wavelength can be tuned by modifying the inter-membrane distance without degrading the Q factor. The electric field amplitude of the two modes have the same in-plane symmetry and opposite out-of-plane symmetry. Therefore, they are defined as even (symmetric) and odd (or anti-symmetric) mode, respectively. [76] (Fig. 1.19)

For QPICs, the proposal of Notomi provides a feasible solution to the real-time control of PCCs: (a) Creating two vertically-aligned suspended PCC membranes is possible and the approach is fully compatible with the whole fabrication flow of the QPIC: sacrificial layers, which can be selectively etched away, can be epitaxially grown below the bottom membrane and inserted between two active layers of PCC-slabs. (b) QDs can be easily embedded in double-membrane PCCs since they can be epitaxially grown within the upper (or lower) membrane. (c) The controlled modification of the inter-slab distance can be achieved in an electromechanical way, which will be discussed in detail below.

When two doped-layers (n-doped and p-doped) are epitaxially integrated in the bottom of the upper–slab and the top of the bottom-slab, the n-doped-layer, the sacrificial layer, and the p-doped-layer form a p-i-n diode. (Fig. 1.20) When a reverse bias voltage is applied on the diode, the amount of fixed charge in the two sides of the junction will change. Then, the p-i-n structure resembles to a parallel-plate capacitor with two plates separated by a dielectric layer. Under reverse bias V, the inter-slab distance $d_g(V)$ shrinks due to the attractive force F between the two plates.
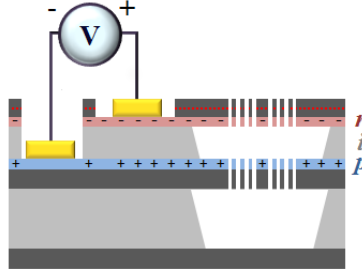
Fig. 1.20 Schematic illustration of a p-i-n structure under reverse bias. The p-i-n structure consists of two doped layers (n-doped and p-doped) and one dielectric layer between them. Metal contacts are made on the doped layers and are connected with a voltage source. The device is partially released by chemical etching through holes in the PCC. Under reverse bias, the electrostatic force between the two slabs is increased.

The vertical displacement of the membrane layer(s) $d_g(V)$ can be reversible. Due to the elasticity of the membrane material, the deformation of the membrane is reversible if the vertical displacement of the membrane is within 1/3 of the initial inter-membrane distance $d_g(0)$. Beyond that range, the system undergoes an electromechanical instability and collapses due to the so called 'pull-in' effect. The process can be understood by modeling the double-slab p-i-n structure as a capacitor with one plate fixed and another plate attached to a spring with an elastic constant k.

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(Fig. 1.21) Since the vertical deformation of the movable plate is always tiny as compared to its area, the curvature of the plate can be ignored.
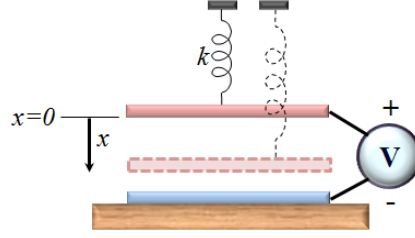
Fig. 1.21 Schematic illustration of simplified capacitor model.

The net force exerted on the upper slab is:

$$F = \frac{\varepsilon_a A V^2}{2(d_g - x)^2} - kx \tag{1.2.3}$$

where ε_a is the permittivity of air, A is the area of each plate, d_g is the gap initial distance between the two plates. The composite stiffness k_{comp} of the upper slab can be obtained by deriving eq. 1.2.3:

$$k_{comp} = -\frac{\partial F}{\partial x} = -\frac{\varepsilon_a A V^2}{(d_g - x)^3} + k \tag{1.2.4}$$

At the equilibrium point where $F=0$,

$$\frac{\varepsilon_a A V^2}{2(d_g - x)^2} = kx \tag{1.2.5}$$

Thus,

$$k_{comp} = -\frac{\partial F}{\partial x} = -\frac{2kx}{(d_g - x)} + k$$
$$= k(1 - \frac{2(x/d_g)}{(1 - x/d_g)}) \tag{1.2.6}$$

A plot of k_{comp}/k as a function of x/d_g (Fig 1.22) shows:

1. When $x = 0$, $k_{comp} = k$. This means when no voltage is applied ($V = 0$), the system can be modeled as the common spring with restoration force $F = -kx$.

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2. When $0 < x/d_g < 1/3, |k_{comp}/k| < 1$. This means that the restoring force is reduced by the electrostatic force.

3. When $x/d_g = 1/3, k_{comp}/k = 0$. In this case, when the composite stiffness $k_{comp} = 0$, the electrostatic force equals the spring force. Thus, the system becomes unstable.

4. When $x/d_g > 1/3, k_{comp}/k < 0$. This means a positive displacement x will result in a positive force to increase x. In this case, the electrostatic force overwhelms the restoring spring force, resulting in the snapping of two layers. This is the so-called "pull-in effect", which limits the electromechanical tuning range of the device.
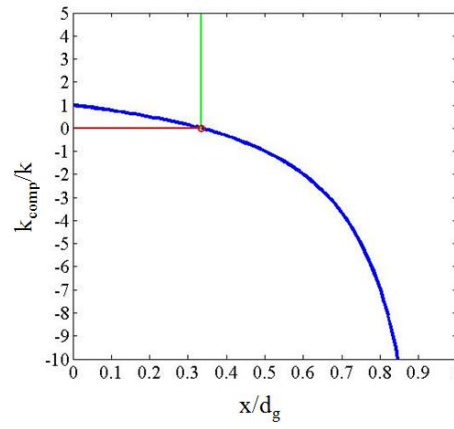
Fig. 1.22 k_{comp}/k as a function of x/d_g

In 2012, *L. Midolo et.al* from our group have experimentally realized the electromechanical tuning of GaAs based double-slab PCCs (L3 PCC-cavities). At 8 K, a maximum tuning range of 13 nm of the cavity mode has been achieved as shown in Fig 1.23. The Purcell enhancement of the QD excitonic emission when the cavity mode is in resonance has been observed as well. [77]-[79]
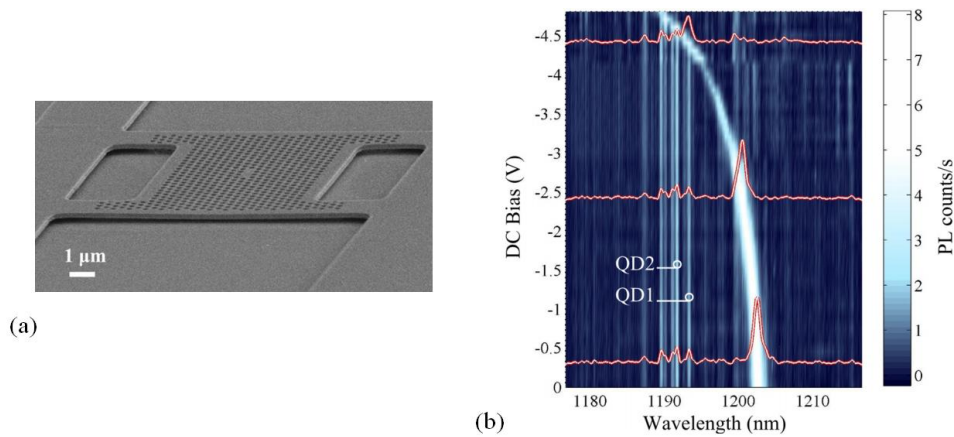
Fig. 1.23 SEM image of a double-slab PCC (a) and PL (8 K) of an anti-symmetric L3 mode as a function of the DC bias using an average pump power of 40 nW (b). [77]

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In order to realize a two-photon bunching experiment in the future, it is necessary to achieve the simultaneous tuning of the QD and PCC in an individual device to bring the two cavities/QDs in resonance with each other.

1.3 General overview of the thesis

This thesis focuses on the spatial and spectral alignment of epitaxial InAs/GaAs QDs with wavelength-tunable photonic crystal micro-cavities. Two main related challenges are studied.

On one hand, the growth of site-controlled QDs with high radiative quality is investigated, in order to obtain the spatial alignment. On the other hand, the combination of Stark tuning and cavity tuning in a single device is investigated.

Chapter 2 describes the general experimental methods employed in the work.

Chapter 3 describes the MBE growth condition optimization for achieving the growth of low density InAs/GaAs quantum dots emitting at telecommunication wavelength.

Chapter 4 shows the investigation and preliminary results in the growth of site-controlled InAs quantum dots on pre-patterned GaAs substrate with nanoholes.

Chapter 5 deals with the indium-assisted deoxidation (IAD) method of an air-exposed planar GaAs substrate, essential for obtaining high quality site-controlled QDs. Preliminary results on the IAD process and related local-droplet etching effect on patterned GaAs substrate are also reported.

Chapter 6 describes the design, fabrication and optical demonstration of buckling-free vertically aligned nanobeam nano-opto-mechanical (NOMS) system devices with novel stress releasing structures.

Chapter 7 demonstrates the result of a novel nano-opto-electromechanical system (NOEMS) device which integrates the Stark tuning of QDs' exciton energy with double-slab PCC NOEMS.

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CHAPTER 2

Experimental Methods

In this chapter, the experimental methods applied in this work are presented. The first part (Section 2.1) describes the molecular beam epitaxy growth technique. The second part (Section 2.2) discusses the details of the nanofabrication techniques used in realizing nano-patterned substrates for the growth of site-controlled quantum dots (SCQDs), and integrated tunable devices. The last part (Section 2.3) explains the setups and devices used for the characterization of MBE as-grown samples and the electrical and spectroscopic properties of the integrated tunable devices.

2.1 Molecular beam epitaxy (MBE)

MBE history

MBE is the method that was used to perform all the thin-film growth (including the growth of low density QDs, SCQDs, device structures for nano-photonic devices, etc) in the work discussed in the thesis. The word 'epitaxy' is a combination of two ancient Greek words *'epi'* (which means 'above') and *'taxis'* (which means 'ordered manner'). [1] Molecular beam epitaxy therefore indicates a method for building ordered layers of material with molecular/atoms from provided molecular/atom beams of different elements. J. R. Arthur Jr. and Alfred Y. Cho (Fig. 2.1), who is known as the 'father of MBE ', are considered having invented this technique in the late 1960s at the Bell Labs in the USA. [2]
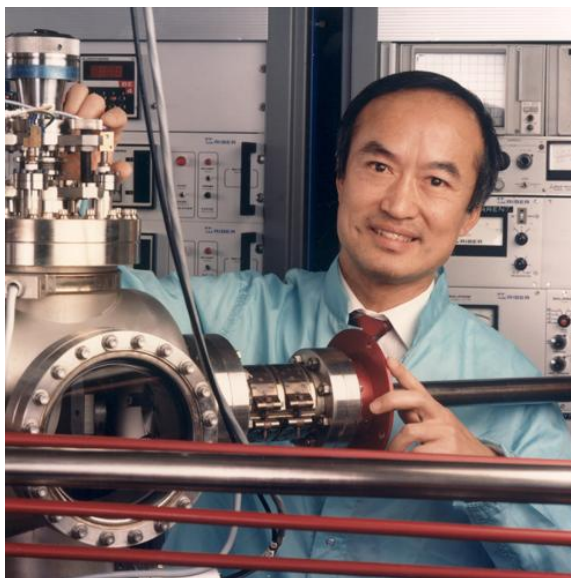

Fig. 2.1 Alfred. Y. Cho at work. [3]

MBE reactor

MBE allows creating new materials and nanostructures in an ultra-high vacuum environment and has played a very important role in the development of nanotechnology and material science. [4] A schematic illustration of the growth chamber of a typical solid-source MBE machine is shown in Fig. 2.2:
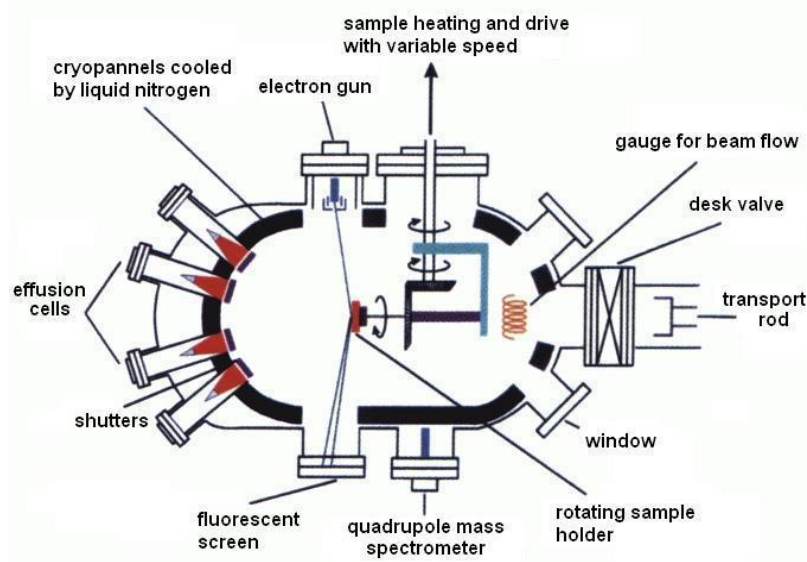

Fig. 2.2 Schematic illustration of the growth chamber of MBE. [5]

The Createc SY022 MBE system at TU/e Nanolab has a similar chamber configuration as the one in Fig. 2.2. Eight cells are installed in the MBE system: $1 \times$ Ga, $2 \times$ In, $2 \times$ Al, $1 \times$ Be, $1 \times$ Si, $1 \times$ As cracker. During growth, molecular beams are generated by heating up materials in the crucibles of effusion cells. An ion gauge is mounted to measure the beam equivalent pressure (BEP) of the molecular beams of the material. The sample is mounted on a molybdenum (Mo) holder and fixed to an adapter connected to a rotation mechanism. In order to achieve a homogeneous deposition of material over a wafer, the substrate is rotated during growth. During the growth, the molecular beams can be easily switched on and off by opening or closing the shutters. The rapid mechanical motion speed of the shutter enables a rapid switching of different materials in the growth and therefore guarantees the growth of layered materials with atomically abrupt interface. The sublimated elements condense on the surface of the substrate and form atomic bonds with each other. The substrate temperature plays a crucial role in the growth of the material by influencing the mobility and desorption rate of adatoms on the surface. Due to the ultra-high vacuum level of the growth chamber (with a background pressure of $\sim 10^{-10}$ mbar) and the precisely controlled beam flux, materials with ultra-high purity can be grown on the sample surface with sub-single-monolayer level deposition rate.

RHEED

A reflection-high-energy-electron-diffraction (RHEED) [6] system, consisting of a high energy electron gun (0 ~ 20 keV) and a phosphor fluorescence screen, is used for the in-situ diagnostics

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of the sample surface during growth. Fig. 2.3 shows a schematic illustration of the basic principle of the RHEED. The high energy electron beam is directed to the sample with a small incident angle (< 3°). The electrons are reflected and diffracted by atoms in the top layers of the surface. The diffracted electrons impinge on the phosphor screen and the fluorescence patterns are detected with a camera which is connected to a computer. The RHEED patterns carry information about the atomic arrangement on the top layers of the specimen. Fig. 2.4 shows the RHEED pattern of a typical 2×4 surface reconstruction. [7] The intensity of the specular spot in the RHEED pattern also shows the overall roughness of the surface [6] and carries information about the growth rate of certain layer since each intensity fluctuation cycle corresponds to the growth of one monolayer of material. To analyze the specular spot intensity, the author built a Labview program to deal with data collected by a Thorlabs DCx camera by referring to a program written by Carl Zinoni (EPFL). Fig. 2.5 shows an example of the front panel of the Labview program.
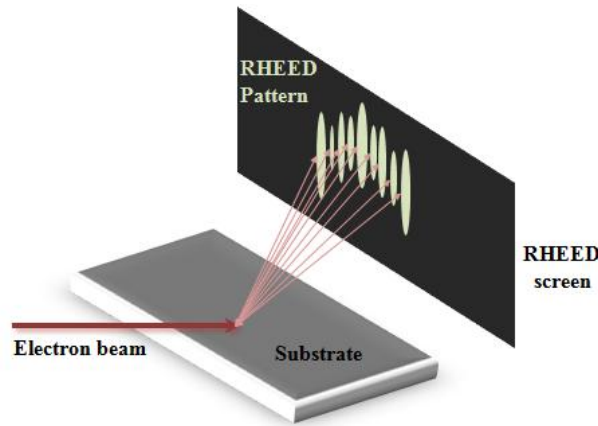
Fig. 2.3 Schematic illustration of the principle RHEED measurement.
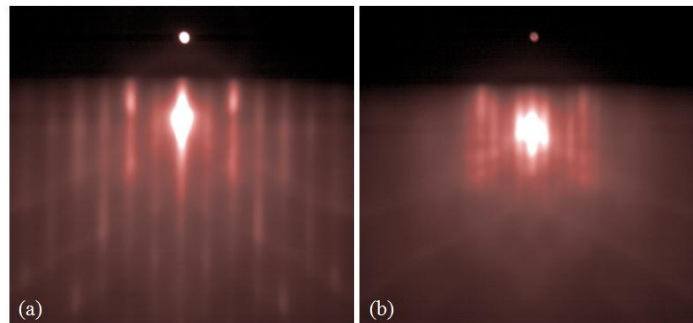
Fig. 2.4 RHEED pattern of the 2 fold (a) and 4 fold (b) of the 2×4 surface reconstruction pattern.

A region of interest (ROI) area can be selected by the square tool to manually define the region in the specular spot to be processed. The Labview program integrates the total counts in the ROI and displays the integrated intensity vs time in the 'ROI Intensity' panel. Settings of the camera can be modified in the 'Camera Settings' panel. By pressing the 'Record Video' button, the video of the RHEED pattern on screen can be saved. The period of the RHEED oscillations (in sec) can be calculated in the 'Oscillation Period Analysis' panel. Fig. 2.6 shows an example of the specular

spot intensity oscillation. Each period of oscillation corresponds to the process of the formation of one monolayer of atoms on the surface.
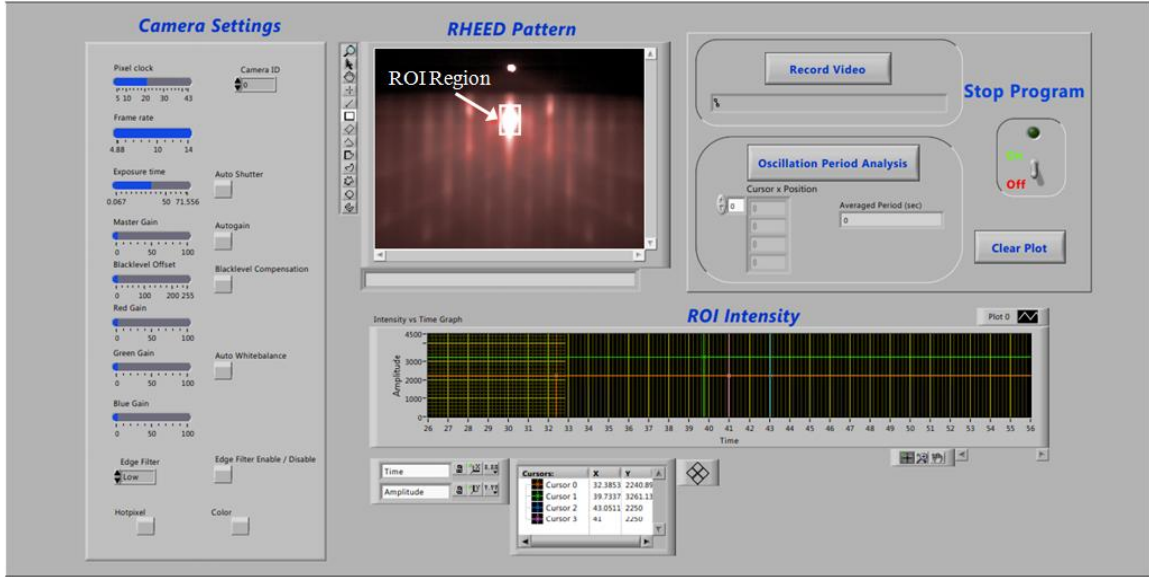
Fig. 2.5 View of the front panel of the RHEED analysis Labview program.
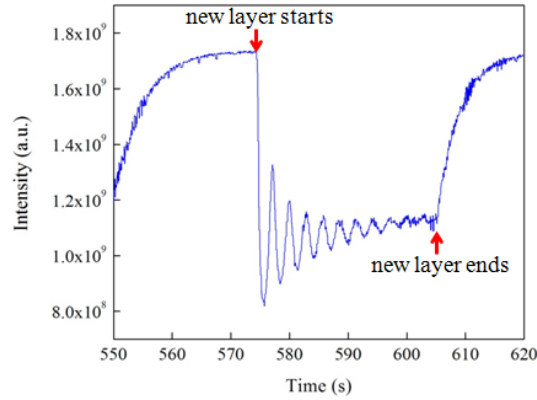
Fig. 2.6 Example of RHEED specular spot intensity oscillation as a function of time.

Temperature monitoring

The substrate temperature can be measured by a thermocouple placed behind the sample holder adapter. However, this is not precise enough, due to the absence of physical contact between the thermocouple and the substrate. Since the substrate temperature is essential for the epitaxy process, especially for the growth of low-density QDs, a more precise substrate temperature monitoring method is needed. We use a calibrated kSA BandiT system (kSA BandiT NIR-range temperature monitor for MBE) to measure the temperature on the substrate.[8] (Fig. 2.7) The BandiT system determines the temperature of a semiconductor substrate by monitoring the change of the absorption edge of the material which is proportional to the temperature-dependent

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bandgap energy of the material. For example, in the case of GaAs, the bandgap energy is expressed by:

$$E_{g,GaAs}(T) = 1.519 - \frac{5.5 \times 10^{-4}}{225+T} T^2 [eV] \tag{2.1}$$

The hardware of the BandiT system consists of a broad-band light source (gold coated Halogen lamp), a laser diode, a spectrometer, and a system controller (Detector + Controller in Fig 2.7), optical fibers, and optics sets for alignment.

In the measurement, the light from the halogen lamp is shined to the substrate surface. Part of the diffusively scattered light will be collected by a multimode fiber and spectrally dispersed and detected by an InGaAs detector. The region on the sample where the temperature is detected can be determined beforehand by sending an alignment laser beam to the sample.
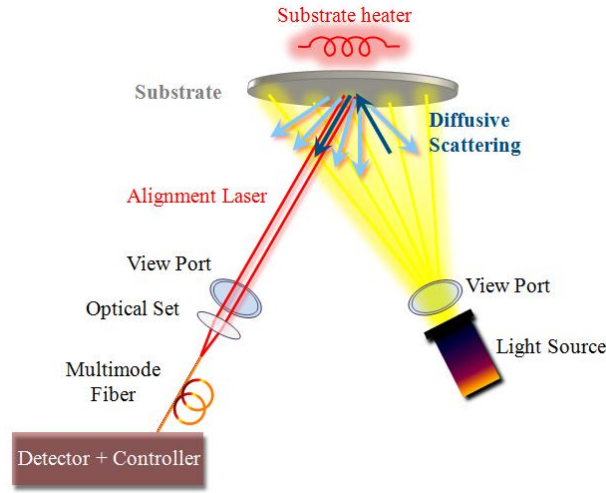
Fig. 2.7 Schematic illustration of BandiT system

2.2 Fabrication

2.2.1 Plasma enhanced chemical vapor deposition (PECVD)

The deposition of hard masks on the sample surface is very important in nanofabrication. In the case of dry etching, a hard mask blocks the plasma bombardment on the covered area and therefore allows a local plasma etching only through the opened area on the mask. In the case of wet etching, a hard mask, which has very good adhesion to the substrate surface, guarantees a smooth etched profile of the pattern on the substrate through openings on the mask. Moreover, as a dielectric layer, a hard mask can be deposited on a sample surface to provide electrical isolation.

The hard mask chosen in this work is Si_3N_4. The deposition of Si_3N_4 is done by a plasma enhanced chemical vapor deposition (PECVD) machine (Oxford Plasmalab System 100) in the Nanolab @ TU/e cleanroom. The schematic illustration of the PECVD processing chamber is

shown in Fig. 2.8. During the process, the substrate is heated up to 300 ℃ on the heated table. The two precursor gasses of Silane (SiH_4) and ammonia (NH_3) (with a flow rate of ~ 17 sccm and ~ 13 sccm, respectively) together with N_2 flow which is a carrier gas (with a flow rate of ~ 980 sccm) are injected into the process chamber via the "shower head" gas inlet from the top. SiH_4 and NH_3 react on the hot sample surface and form Si_3N_4 based on the chemical reaction[9]:

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \qquad (2.2)$$
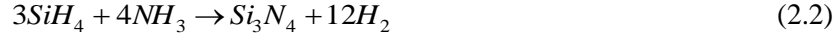
The RF-controlled top electrode ionizes the gasses, controls the bombardment rate of ions on the growing film, and therefore controls the stress in the film. The nominal growth rate of Si_3N_4 with the PECVD machine in the Nanolab is about 15 nm/s.
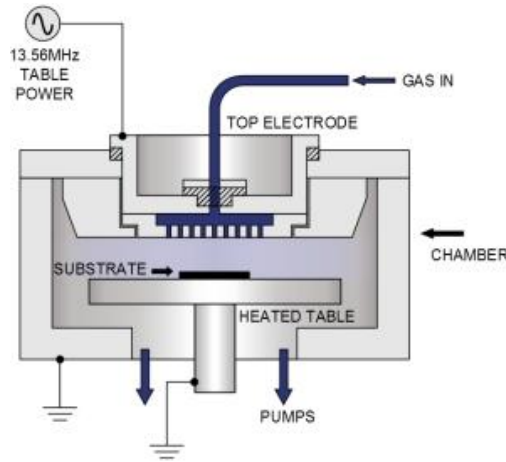

Fig. 2.8 Schematic illustration of PECVD machine (Oxford Plasmalab System 100). [10]

2.2.2 Optical lithography

Optical lithography is used to transfer the pattern from a (quartz plate) optical lithography mask to the sample. The Karl Süss Mask Aligner 'MA6' is used as the optical lithography machine in the Nanolab @ TU/e cleanroom. A mercury arc UV-lamp (with UV-light wavelength in the range of 365 nm to 405 nm) is used for the exposure. The optical lithography mask is a Cr-coated square quartz mask (6×6 inch^2). The mask is designed at TU/e and fabricated at TU Delft. In this work, both the positive resist HPR 504 and the negative resist ma-N 440 are used.

In the process of optical lithography, first, the sample is cleaned by acetone flow and isopropanol flow to remove any organic contaminants on the surface. Then, after blowing dry the sample with N_2 gas, the photoresist (PR) is spin-coated on the surface (for HPR 504, spinning at speed of 3000 rpm for 30 sec with an acceleration rate of 5000 rpm/s, results in a ~ 750 nm thick PR). After pre-baking, the resist is exposed to the UV-light which comes through openings in the Cr-quartz mask (see Fig. 2.9). After post-baking, the resist is developed in developer solvents removing the exposed part of the positive PR and the un-exposed part of the negative PR. The resist developing solvents of HPR 504 are PLSI: H_2O (1:1) or OCG: H_2O (1:2). The finest structure that can be realized with the MA6 system has sizes of the order of ~ 0.6 μm.
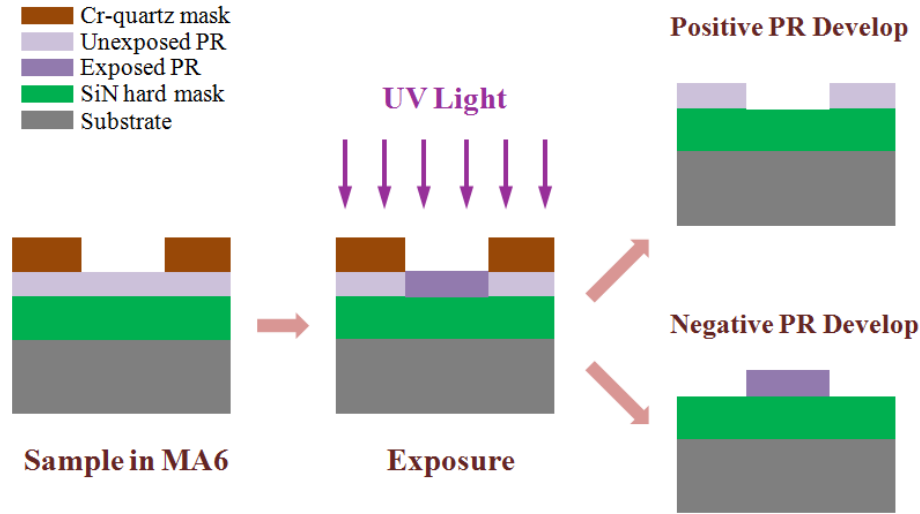
Fig. 2.9 Schematic illustration of exposure and development process of positive and negative PR

2.2.3 Electron-beam lithography (EBL)

Electron-beam lithography (EBL) is another way to define patterns on a sample. It uses collimated high-energy electron beams to 'write' directly on a resist according to the designed mask file (GDSII design file). Compared to optical lithography, EBL provides higher resolution but requires longer pattern writing time (or exposure time). The EBL in the Nanolab @ TU/e is a 'Raith 150 Two' machine. The system consists of a scanning electron microscope (SEM) integrated with a beam blanker, apertures, alignment coils, stigmator, Zeiss Gemini objective lens, x-y-stage controller, etc. The highest acceleration voltage of the column is 30 kV. Fig. 2.10 gives an illustration of the structure of the EBL system.

Two types of Electron-beam resists, ZEP-520A and PMMA-950k, are used in the work described in this thesis. They are both positive resists. ZEP-520A has better plasma etch resistance than PMMA-950k, while PMMA-950k provides a better resolution in defining small structures than ZEP-520A. In the process of EBL, first, the sample is spin coated with the resist (for ZEP-520A, with a spin speed of 4000 rpm, the thickness of the resist is ~ 360-380 nm; for PMMA-950k, with a spin speed of 9000 rpm, the thickness of the resist is ~ 140 nm). After pre-baking, the sample is first transferred to the Load-Lock chamber of the EBL machine and then loaded to the motorized x-y-z stage in the main chamber. Nano-meter precision of sample movement can be guaranteed.

A manual alignment is needed in order to have a rough match of the x-y-z stage coordinate with the sample's physical coordinate system, to make a good focus of the electron beam on the sample /surface, to adjust the aperture to minimize the focus wobble, to minimize the stigmation and to optimize the stitching of each write field. It is worth mentioning that the EBL mask design is divided into squares with the same size (for example, $100 \times 100 \ \mu m^2$ square). Each square is called a 'write field'. (Fig. 2.11) The write fields are exposed one by one and stitched together to form the final pattern. For example, when the sample is at position a on the x-y-z stage, the e-beam deflects to write all the patterns within the write field A. Then, the stage is moved, and the

e-beam writes in the write field B. After exposure, the sample is unloaded from the EBL machine and the patterns are developed with developer solvents. ZEP-520A is developed with n-amyl-acetate for 1 min and rinsed in the stopper solvent of methy isobutyl ketone (MIBK)-IPA solution for ~ 40 sec. PMMA-950A4 is developed with MIBK: IPA (1:3) for ~ 70 sec and rinsed in IPA for 1 min. To open a structure of similar size, the EBL dose (in $\mu C/cm^2$) of PMMA is about 10 times higher than that of the ZEP 520A.
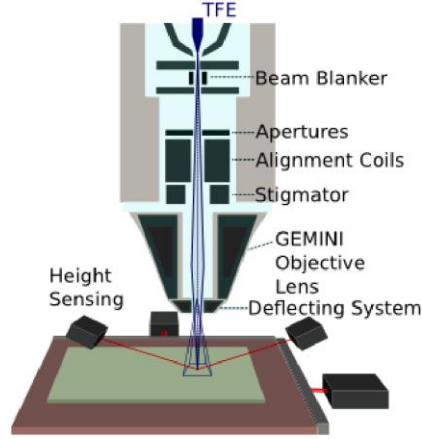
Fig. 2.10 Schematic illustration of the Raith 150 Two EBL system. [11]
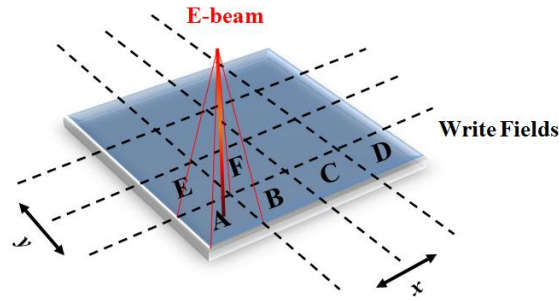
Fig. 2.11 Schematic illustration of write fields.

When closely separated patterns are exposed, due to the influence of the scattering of electrons in the resist during exposure, the effective dose on certain pattern is changed. The forward and back scattering of electrons determines the smallest structure (or the effective beam diameter) d_f (in nm) that can be defined in the resist [12]:

$$d_f = 0.9 \times (\frac{t}{V})^{1.5}$$
(2.3)

where t is the thickness of the resist with the unit of nm and V is the value of acceleration voltage in kV. The back scattered electrons have a larger area of influence than the forward scattered electrons. Therefore, the back scattered electrons from neighboring patterns can influence the local doses. This effect is called the 'Proximity Effect'. This effect can be corrected by changing the dose of each pattern in the design.

2.2.4 Dry etching

Dry etching method provides a way to transfer patterns from masks to samples. Usually, dry etching is realized with the help of plasma. Dependent on the working condition, dry etching can result in isotropically or anisotropically etched profiles (Fig. 2.12).
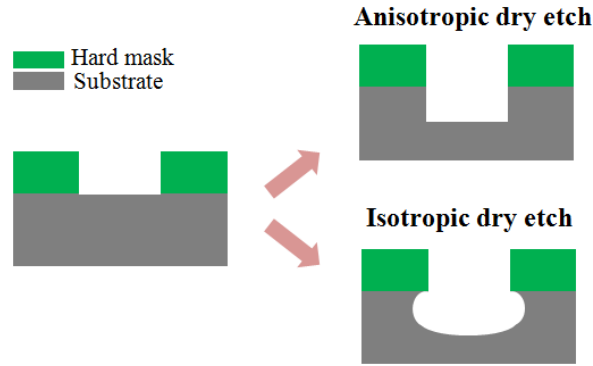
Fig. 2.12 Illustration of anisotropic and isotropic dry etching.

In the work described in this thesis, three types of plasma etching are adopted: plasma etching (PE) (TePla 100 barrel etcher), reactive-ion etching (RIE) (Oxford Instrument Plasmalab 100), inductively coupled plasma etching (ICP) (Oxford Instrument Plasmalab 100).

Plasma etching (PE):

In some parts of this work, the PE is used to remove Si_xN_y hard mask in an isotropic way. Fig. 2.13 gives a schematic illustration of the principle of PE. The gas (in our case is CF_4 gas) is injected to the process chamber through the inlet on top and is ionized by the RF field generated in the top electrode. The sample is placed on the bottom electrode which is grounded. The ions move randomly in the chamber, reach the surface of the target substrate and chemically react with the surface of the substrate. Due to the randomness in the movement of the ions, PE is highly isotropic.

Fig. 2.13 Schematic illustration of the PE. [13]

RIE:

In this work, RIE is used to etch the Si_xN_y hard mask and large structures on GaAs substrate. Fig. 2.14 shows a schematic illustration of the structure of the process chamber of a RIE machine. [13] RIE is a modified t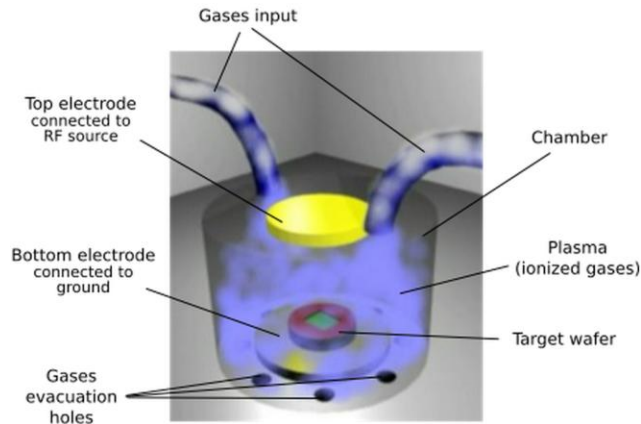ype of PE. In the process, the sample is placed on a quartz or graphite plate on the bottom electrode. Gases (for Si_xN_y etch, CHF_3 or CHF_3+O_2 are gas etchants; for GaAs etch, $SiCl_4$ + Ar are gas etchants) are injected to the process chamber through a 'showerhead' gas inlet of the top electrode. Different from the configuration of PE, the top electrode of RIE is grounded whereas the bottom electrode is connected with a RF-controller. When a 13.5 MHz RF field is present, the gas in the chamber will be partially ionized due to the electromagnetic excitation and ion-electron pairs will be generated. Due to the lower mass of the electrons as compared to the ions and the fact that the substrate is connected to the RF field, electrons follows well the RF field and get easily adsorbed by the substrate. Due to the loss of electrons in the ionized gasses and the accumulation of negative charges on the bottom electrode, an electric field is generated between the ion cloud (positively charged) and the wafer (negatively charged). Driven by the field, ions are accelerated toward the wafer with a good directionality, collide (physical bombardment) and react (chemical reaction) with the material on the wafer surface.
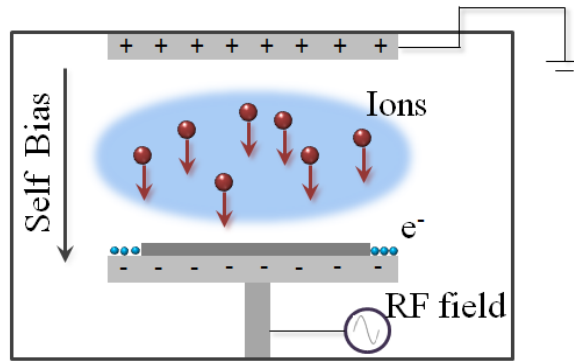
Fig. 2.14 Schematic illustration of the RIE working principle. [12]

ICP-RIE:

In this work, ICP-RIE (Oxford Instrument Plasmalab 100) (Fig. 2.15) is used to deeply etch holes of photonic crystal cavities (PCCs) in GaAs with excellent aspect ratio. In ICP-RIE, the target sample is placed at the bottom electrode which is connected to a RF controller. Gases are injected from the top of the processing chamber and ionized under a strong magnetic field created by a coil close to the gas inlet. In ICP-RIE, the ion energy and ion density are controlled by the RF generator and the ICP power generator, respectively. A high etch rate and a good verticality of etched sidewalls can be achieved by accelerating high density ions under high electric field. In the etching of GaAs PCCs, Cl_2+N_2 gases are used as etchants and the process temperature of the GaAs substrate is set at 200 ℃.

Fig. 2.15 Illustration of ICP-RIE (Oxford Instruments Plasmalab 100). [14]

2.2.5 Wet etching

Wet etching employs chemical solutions to erode the substrate. Compared with the dry etching, wet etching has several advantages and disadvantages. Advantages are: (a) wet etching induces no plasma induced defects 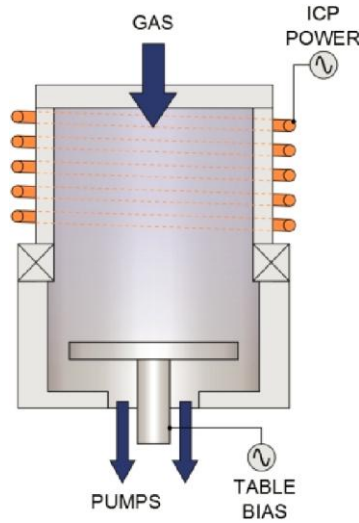in the material; (b) wet etching can be selective to different types of material. The major disadvantages are: (a) it is difficult to produce vertical side walls with high aspect ratio with wet etching; (b) undercut will be created with wet etching. Table 2.1 summarizes the wet etching recipes used in this work and the corresponding etching rates.

Table 2.1 Wet etching rate of chemicals

Chemical	Etched Material	Etch Rate	Stop on
CA^*:H_2O_2 (40:1)	GaAs	~ 1.34 nm/s	$Al_{0.79}Ga_{0.21}As$, Si_xN_y
HF 10%	$Al_{0.79}Ga_{0.21}As$	~ 75 nm/s	GaAs
HF 1%	$Al_{0.79}Ga_{0.21}As$	~ 6 nm/s	GaAs
HF 10%	Si_xN_y	~ 4 nm/s	GaAs
H_2SO_4: H_2O_2: H_2O (8: 16: 200)	GaAs	~ 25 nm/s	Si_xN_y
H_2SO_4: H_2O_2: H_2O (0.5: 4: 600)	GaAs	~ 0.5 nm/s	Si_xN_y

* CA is $C_6H_8O_7$:H_2O (1:1 in weight)

2.2.6 Contact evaporation

Two types of metal evaporators are used for evaporating metals to form contacts on devices.

Electron beam evaporator:

In this work, the Temescal FC2000 electron-beam evaporator (Fig. 2.16 (a)) is used for evaporating Ti/Au contacts. In the process, the metals are heated and melted by the bombardment of a high energy electron beam in a high vacuum chamber. When the metals evaporate, the atoms travel through the chamber and condensate on the sample, forming a metallic layer on the sample surface. As compared to thermal evaporators, the electron beam evaporator allows working with metals with high melting temperature. The deposition thickness of the deposited film is monitored by evaluating the resonance frequency of a quartz crystal.

Resistance heating evaporator:

In this work, thermal evaporators (Edwards Coating Systems E305A & Edwards Auto 306) (Fig. 2.16 (b)) are used for evaporating Ni-Zn-Au contact (p-contact) and Ni-Ge-Au contact (n-contact). In the process, metals are melted by a Joule heating of a metal plate. The thermal evaporators are suitable for working with metals with low melting temperature.
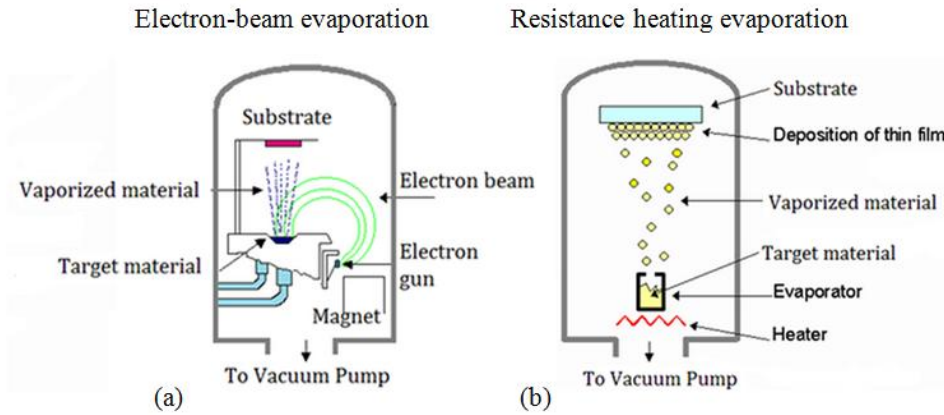
Fig. 2.16 Schematic illustration of thermal evaporator and e-beam evaporator. [15]

2.3 Characterization setups

2.3.1 Atomic Force Microscopy (AFM)

In this work, the surface morphology of MBE grown samples is characterized with an AFM (Veeco Dimension 3100) working in the tapping mode. The schematic illustration of the structure of the AFM is presented in Fig. 2.17.

AFM provides an atomic level height-resolution of the structure. In the measurement, the sample can be moved in the x-y-z directions. The AFM tip is mounted to an AFM tip holder and fixed to the AFM head with the movement controlled by a piezo. A laser beam is focused to the backside of the AFM tip and is reflected to a position sensitive detector (split photodiode detector). Before scanning, the tip is brought close to the sample surface where the force between the sample and the tip is strong. During scanning, the cantilever of the AFM tip oscillates. The amplitude and the

frequency of the oscillation are kept constant during the scan by using a feedback loop to analyze the laser spot detected by the PSD and control the piezo actuator in the z direction.

The AFM tips used are NT-MDT NSG10 series noncontact single crystal silicon SPM tips with Pt conductive coating and with the resonant frequency in the range of 140-390 kHz, force constant of 3.1-37.6 N/m. (Fig. 2.18) The cantilever length, width and thickness are 95 ± 5 μm, 30 ± 3 μm and 2 ± 0.5 μm respectively. [17]
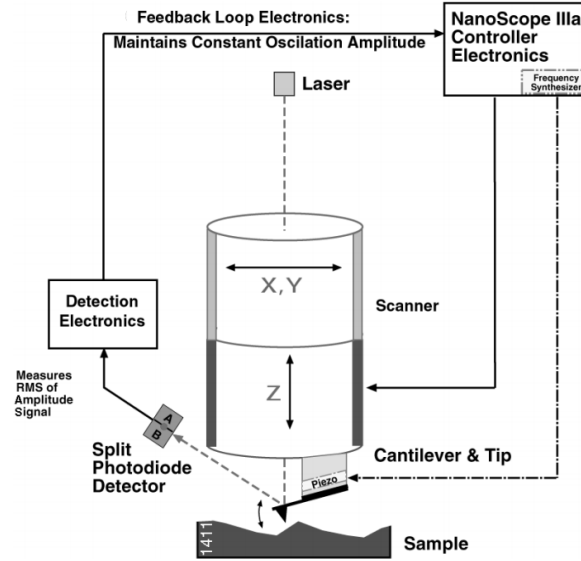
Fig. 2.17 Illustration of the AFM feedback loop [16]

For the AFM at TU/e lab, the z piezoelectric actuator has a good precision whilst the x and y actuator always have a drift which deforms the images. Calibration of the x and y actuator can be done by using samples which have patterns with known/calibrated size. The AFM images are analyzed by Gwyddion, open source SPM software which can perform many data visualization and data processing tasks. [18]

Fig. 2.18 SEM images and illustrations of parameters of AFM tips [17]

2.3.2 Scanning Electron Microscopy (SEM)

The high resolution SEM JEOL 7500FA in the Nanolab @ TU/e cleanroom is used for device morphology characterization in this work. The acceleration voltage range is between 0.1-30 kV.

The magnification is from $\times 25$ to $\times 1000000$ times. [19] For measuring devices of this work, 2 kV and 5 kV are two commonly used acceleration voltages to get good pictures.

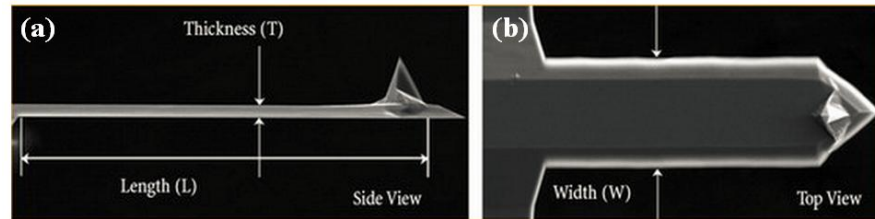### 2.3.3 The general 'Grower PL' micro-PL setup

A general micro-PL setup, which is able to work at both room temperature and low temperature, is used in this work for having a quick measurement of the photoluminescence of the as-grown QD samples and cavity modes of fabricated devices. A sketch of the structure of the setup is shown in Fig. 2.19. A continuous-wave (cw) diode laser operating at 635 nm with a maximum output power of 2.8 mW is used as the excitation source. An objective (Numerical Aperture (N.A.) = 0.5, Magnification = $\times 100$) is used to focus the laser beam on the sample and collect the PL signal which is then focused into a multimode fiber. A green light LED is used to illuminate the surface. The position of the sample is controlled by a Thorlabs x-y-z stage controlled by step motors. An InGaAs detector array working at -100 ℃ is used to detect the PL in the 800 to 1600 nm wavelength range.
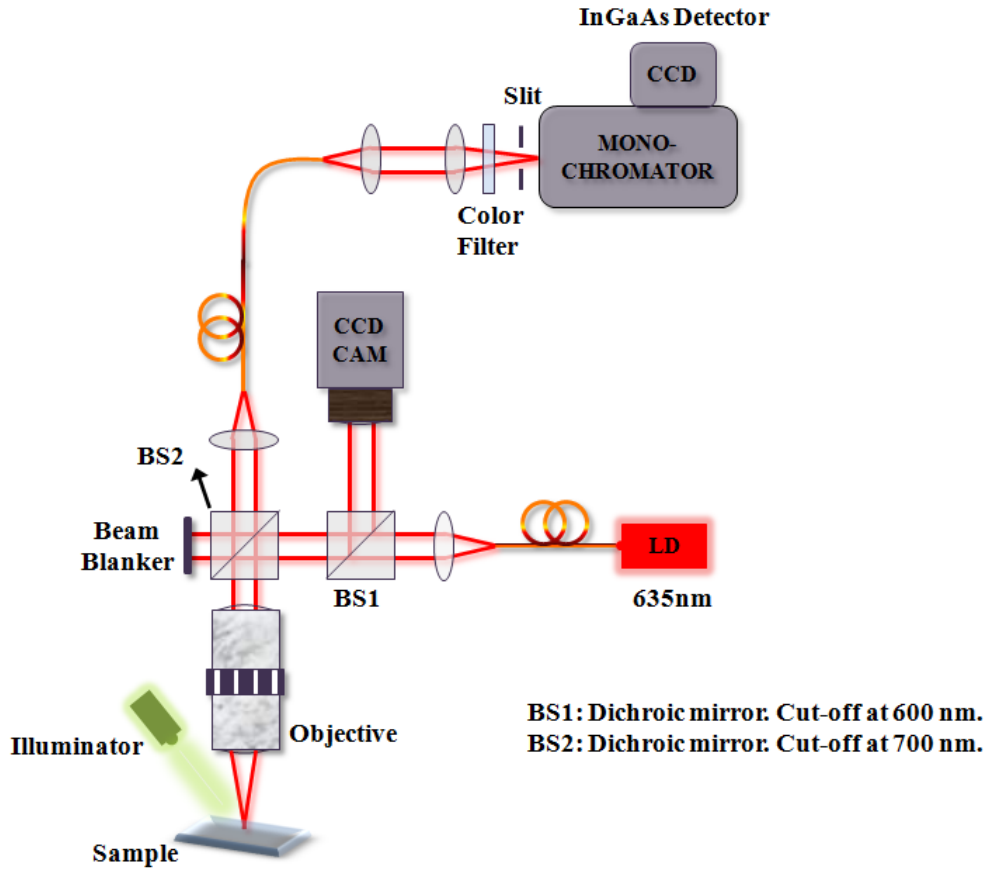

Fig. 2.19 Schematic Illustration of the 'Grower PL' setup.

2.3.4 'Single-photon' (SP) micro-PL setup

High resolution spectra of MBE grown QD samples are measured with another micro-PL setup (named as 'SP-PL'). The system was designed and built by C. Zinoni [20]. The structure of the setup is shown in Fig. 2.20. A cw diode laser operating at 780 nm is used as the excitation source. The focusing objective has an N.A. of 0.6 and magnification of $\times$ 100. The collected PL signal enters into the monochromator (Horiba-Jobin-Yvon FHR 1000) from its lateral entrance, leaves it from its axial exit and impinges on the Jobin-Yvon InGaAs array detector. The spectral resolution of the micro-PL system is better than 0.04 nm and the spatial resolution is about 2 μm in diameter. A fiber-coupled white light source is used to illuminate the surface of the sample. A Si CCD camera and an infrared CCD camera can be used to monitoring the spot and the sample surface. The sample can be placed in a cryostat which can be cooled down to 5 K with a continuous He-flow. The position of the sample can be modified by a joy-stick controlled x-y-z stage, driven by step motors.
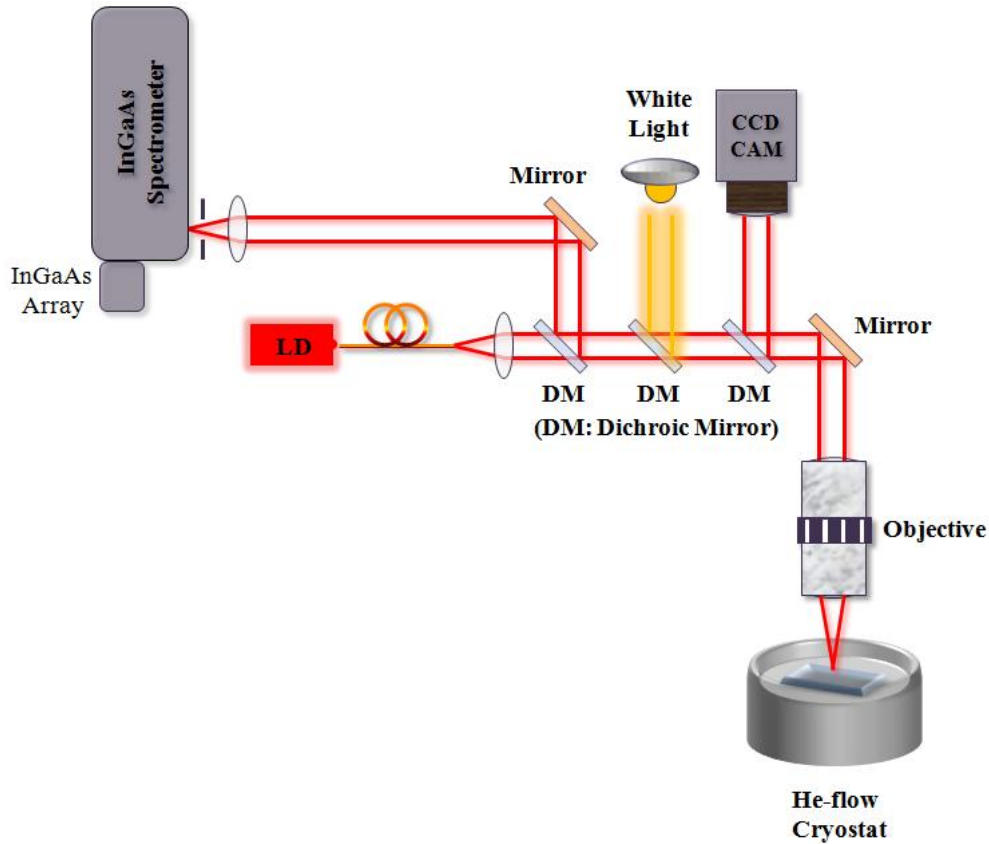

Fig. 2.20 Schematic Illustration of the 'SP-PL' setup

2.3.5 Time-resolved PL set-up

The time-resolved PL signal of MBE-grown QD samples is measured by a modified 'SP-PL' setup. The purpose of the TRPL signal measurement is to explore the decay dynamics of excitons in QDs. The sketch of the system is presented in Fig. 2.21. In the TRPL measurement, a 757 nm

pulsed diode laser (pulse width ~ 70 ps, repetition rate = 40 MHz) is used as the excitation source. A Scontel commercial SSPD is used to detect the collected PL signal. The TTL sync-output of the PDL 800 laser controller is sent to the channel '0' of a PicoHarp 300 correlation card as the 'start signal' and is sent to the 'Trigger' input of the controller of the SSPD. The electrical pulse output of the SSPD is sent to the channel '1' of the correlation card as the 'stop signal'. The correlation card builds up statistical histograms showing the time delays between the 'start' and 'stop' signal and the corresponding photon counts.
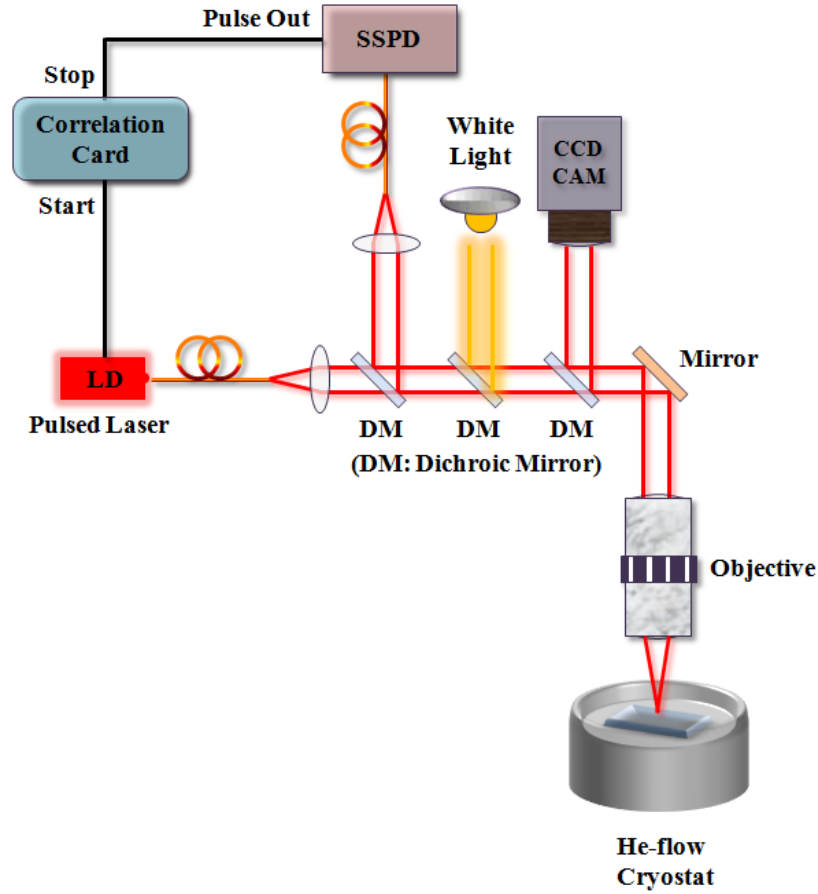
Fig. 2.21 Schematic Illustration of the TRPL measurement setup.

2.3.6 micro-PL+ probe station setup

2.3.6.1 The general probe station

To quickly measure the optical properties as well as the electrical properties of the NOEMS devices, a general purpose probe station was built by Tian Xia and Zili Zhou based on the 'Grower PL' setup. In the modified probe station, an easy-to-mount 'probe set' is added to the system. (Fig. 2.22) The 'probe set' mainly consists of a probe mounted on a home-assembled

position controller which is able to perform fine adjustment of the position of the probe in the x-y-z directions.

Fig. 2.22 Picture of the general probe station.

Fig. 2.23 Schematic Illustration of the 'General' probe station

During the measurement, the probe (with the tips in a Ground-Signal-Ground configuration) is connected to the gold pads on the device and the connecting cable is connected to a voltage source via a 10 Ω resistor (Fig. 2.23) By measuring the voltage drop on the r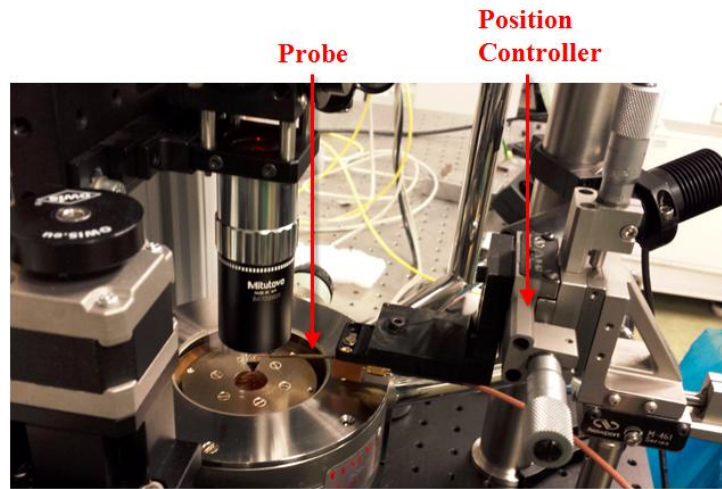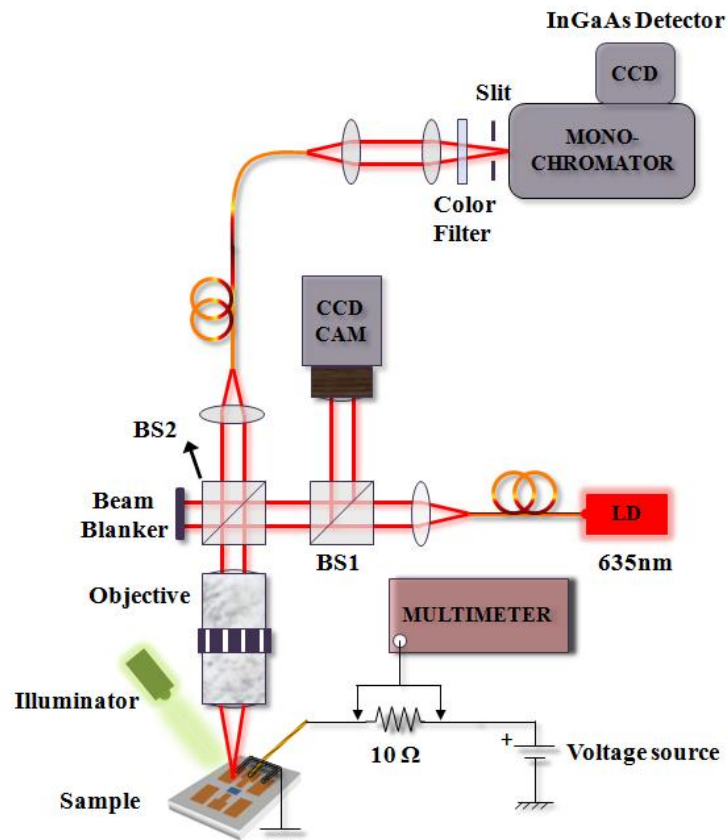esistor with a multimeter, the current flowing in the probe can be calculated. Therefore, the I-V of the device can be deduced. The PL of the device can be measured at the same time. Fig. 2.23 shows a sketch of the complete general probe station system. This probe station is very flexible and easy to use, however it has several problems: (a) limited mechanical stability of the system (b) drifting of sample due to the absence of a sample clamp (c) incapability to measure samples at low temperatures.

2.3.6.2 The 'mPL+PS' probe station

To overcome the above mentioned problems of the 'General probe station' setup, in the characterization of delicate devices, the 'mPL+PS' setup, built by Francesco Pagliano, is used. The sketch of the setup is shown in Fig. 2.24. In this system, two probes can be mounted inside the cryostat. A set of x-y-z Attocube piezo is used to adjust the position of the sample. In addition, the temperature of the sample is controlled by a temperature controller and is connected to a heater. This guarantees that no water condensation will take place on the device during warming up the systems. Since the temperature of the sample can always be kept at a higher value than the environment in the cryostat.
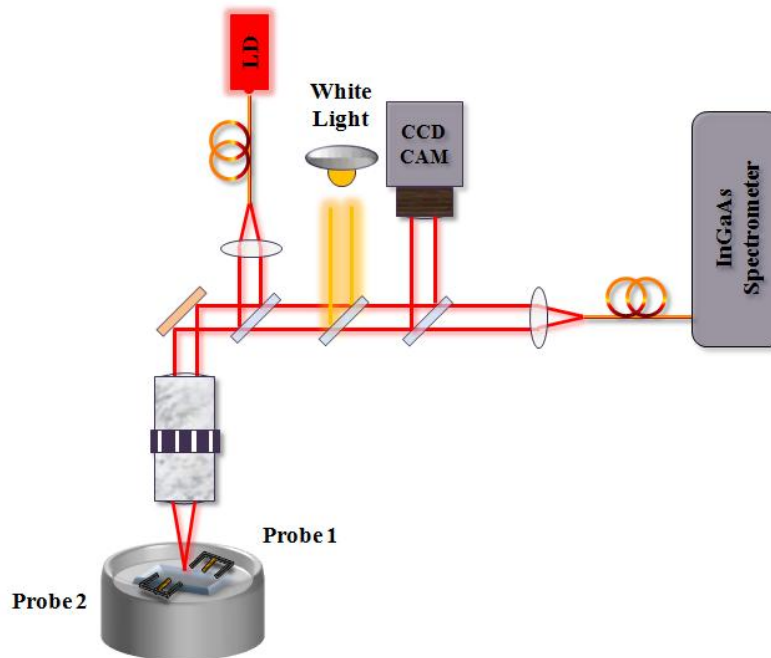

Fig. 2.24 Schematic Illustration of the 'mPL+PS' probe station.

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CHAPTER 3

Growth condition optimization of low-density InAs/GaAs QDs

In this chapter, the author discusses the methods used to produce low-density InAs/GaAs QDs on planar GaAs substrates. This also establishes the basis for the growth of nano-photonic device structures with low-density quantum dots (LDQDs) and has directly contributed to three publications. [1] - [3] This work is a preparation for the growth of low-density site-controlled on quantum dots (SCQDs).

3.1 Characterization of substrate holders

The substrate temperature is an essential parameter that influences the growth of LDQDs. Uniform growth of LDQDs with emission wavelength ~ 1300 nm can be obtained by using high substrate temperature and low material deposition rate, resulting in a long adatom migration length. [4] In these conditions, the growth of LDQDs is very sensitive to the substrate temperature variation since, at high temperature, the In adatom desorption rate is comparable to the deposition rate.

To get a homogeneous distribution of QDs, a good uniformity of the temperature on the substrate needs to be guaranteed. In MBE growth, the substrate is heated by a filament heater and the temperature distribution on the substrate is influenced by the substrate holder. As shown in Fig. 3.1, three types of substrate holders were used in this work: the In-free mounting holder (Fig. 3.1 (a)), the In mounting holder (Fig. 3.1 (b)) and the 2-inch In-free mounting holder (Fig. 3.1 (c)). The work started with the sample growth on the In-free holders. However, as it will be shown in more detail in Section 3.2, a large dot density inhomogeneity is found for LDQDs grown with In-free holders. Then, the In mounting holders are used as an alternative solution and proved to be able to produce a better dot density uniformity. The 2-inch In-free sample holders are used to grow production samples which undergo further processing.
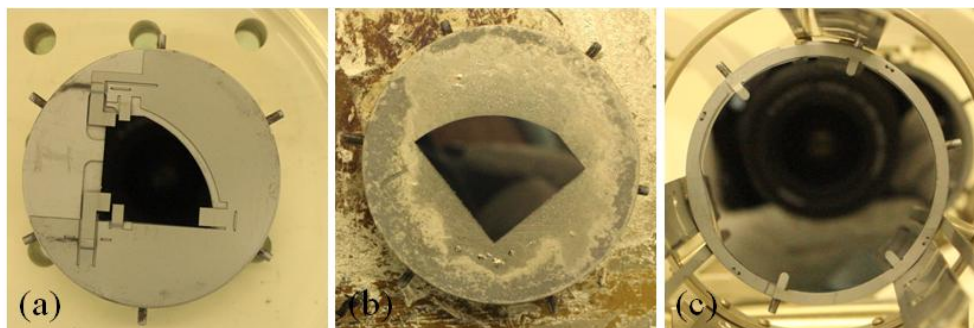

Fig. 3.1 Pictures of samples mounted on (a) In-free mounting holder (b) In mounting holder (c) 2-inch In-free mounting holder.

The BandiT temperature measurement system (Fig 2.7) mounted on the Createc SY022 MBE allows characterizing the temperature uniformity of substrates. The author characterized, together

with Zili Zhou, the substrate temperature distribution on an In-free mounting holder and an In-mounting holder by using the BandiT system. As it is explained in Chapter 2, the region of interest on the sample where the temperature is measured by BandiT can be pre-determined by sending an alignment laser to the sample and observing the position of the laser spot on the sample. By manipulating the optical set of the BandiT system, the laser spot position can be modified along the radial direction. (Fig. 3.2)
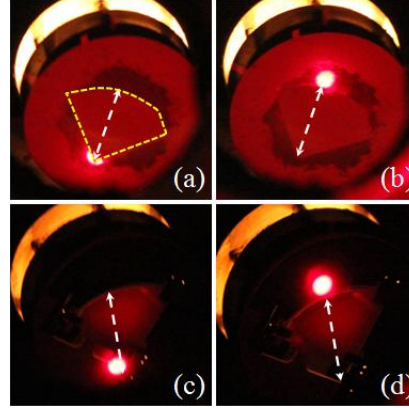
Fig. 3.2 Pictures of the laser spot impinging on samples mounted on an In mounting holder (a)-(b) and an In-free mounting holder (c)-(d) .The arrow shows the direction of the movement of the laser spot.

The laser spot was first adjusted to the rectangular corner (the position denoted by R_0) of the ¼-substrate (Fig. 3.2 (a)). When the sample is rotated, the laser spot impinges on different positions on the sample. Fig. 3.3 shows pictures of the position of a laser spot during the rotation of an In mounting holder. The angular variation step $\Delta\theta$ of the sample is 20 °.

Fig. 3.3 Pictures of the positions of a laser spot on a ¼ GaAs substrate mounted on an In mounting holder during rotation. The angular rotation step is 20 ° between each sub-figure. After 18 rotation steps, the laser spot returns to its original position.

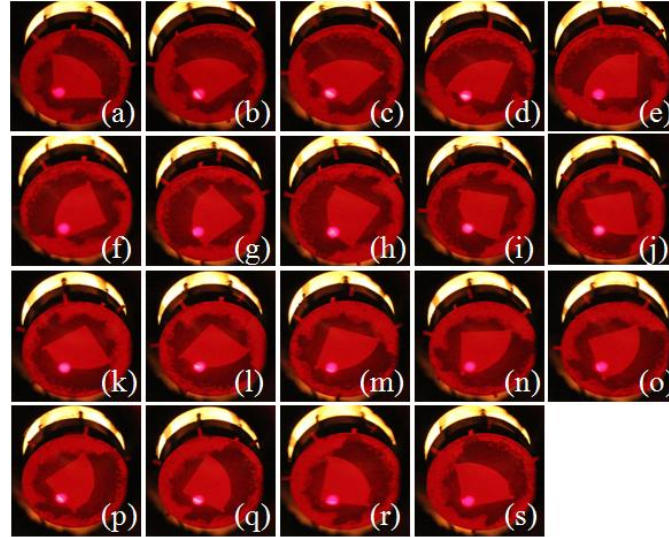Then, the laser was turned down and the temperature measurement started. The rotation of the substrate was carried out by manually adjusting the rotation mechanism based on the scale marks of the precision screws on it. Two complete turns of rotation (720°) of the rotation mechanism corresponds to one complete turn of the rotation of sample (360°). The temperature of the substrate was measured every 20° (according to a 40° angular variation of the rotation mechanism) till the sample returned to its original position.

Afterwards, the laser was turned on again. The position of the laser spot was adjusted along the radius axis to the next position R_2, which is one step toward the edge of the substrate along the radius of the sample. Each step equals to $R/(N-1)$, where R is the radius of the sample, N is the number of points to be measured along the axis (N determines the spatial resolution of the measurement). For every R_x, eighteen temperature measurements were taken every 20° during a 360° rotation of the sample. Then, the laser spot was moved to the next radius position and the temperature procedure was repeated till the spot completely fell out of the sample. (Fig. 3.4)
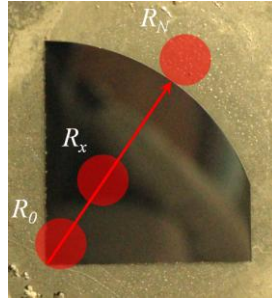

Fig. 3.4 Schematic illustration of the radius positions of a laser spot (red spots in figure) on sample and its movement direction (arrow in figure).

The coordinate of each data point on the sample was rebuilt by ex-situ geometric calculations. Fig. 3.5 (a) shows a reconstructed position map of the data points collected from a sample mounted on an In-mounting holder when the reading from thermocouple is $T_c = 950$ °C. The In mounting holder provides better temperature uniformity than the In-free mounting holder. Samples mounted on them have temperatures of 623.4 ± 3.4 °C and 563.1 ± 26.3 °C, respectively. Fig. 3.5 (b) and (c) shows the 2D color temperature maps of substrates mounted on the In and In-free mounting holders, respectively. It is worth noticing that the center of the substrate mounted on the In-free holder has a much higher temperature (in this case ≈ 30 °C) than the other region of the sample. The 2D temperature map (Fig. 3.5 (b)) of the In mounting holder falls all into the physical profile of the substrate. It can be observed that the data points around the edge of the sample are missing. The reason comes from the detection and calculation mechanism of the BandiT system. The system only outputs correct substrate temperature at positions where > ½ of the alignment laser spot (diameter ~ 7 mm) falls inside the substrate. In Fig. 3.5 (c), the reason why some data points are out of the area of a standard ¼ wafer is not clear yet. Tentatively, it can be attributed to the influence of the leakage of the blackbody radiation from the hot filament heater through the gap between the mounting slot on the holder and the edge of the sample. The reason why the temperature uniformity on the sample is better with In mounting is due to the better thermal conductivity of In than the vacuum in heat distribution: In the case of the In mounting holder,

heat is absorbed by the underlying metallic substrate holder and diffuses into the GaAs substrate through the In-layer. Since the sample size is small compared to that of the holder the heater underneath, the temperature is quite homogeneous across the substrate. In the case of the In-free mounting holder, heat is absorbed both by the GaAs substrate and the metallic holder. In this case, the temperature homogeneity on the GaAs substrate is sensitively influenced by the thermal contact between the substrate and the holder and is very sensitive to the temperature inhomogeneity of the heater. The higher substrate temperature in the center of the In-free mounted sample than that on the corner can be due to the heat loss resulting from the contact of the sample clamp with the corners of the sample. The reason for the slightly lower temperature in the center of the In-mounted sample than the corners and edges is not completely clear yet.
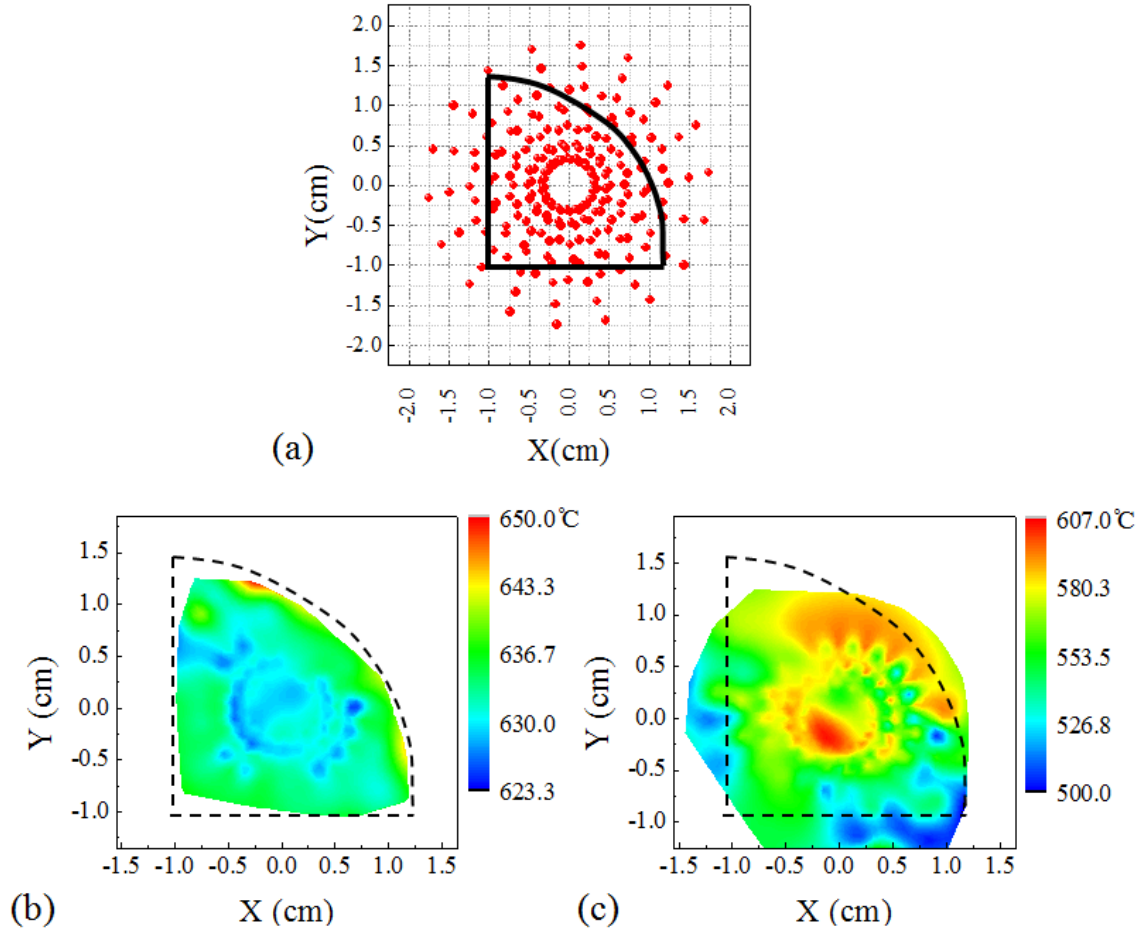

Fig. 3.5 (a) Reconstructed 2D coordinate maps of measured positions on an In mounting holder. 2D color temperature maps of substrates mounted on an In mounting (b) and an In-free mounting (c) holder. The dashed lines in each figure show the physical profile of the substrate.

3.2 Growth optimization

The growth optimization of low density, long-wavelength SCQDs on GaAs is studied, following the low-growth rate approach first proposed by Alloing et al. [4], [5]

3.2.1 Selection of appropriate substrate holder

(Note: The work described in this section was done before the BandiT system was mounted on the MBE. The substrate temperature T_{sub} when the reading of the thermocouple equaled to T_C was evaluated with the function: $T_{sub}/580 = T_C/T_{OR}$, where T_{OR} is the reading of the thermal couple when the oxide on the surface is decomposed. The absolute substrate temperature in this condition is considered to be 580 ℃).

As it has been discussed in Section 3.1, different types of substrate holders provide different temperature uniformity across the substrates. To verify the sensitivity of the growth of LDQDs on the substrate holder and the growth temperature, four samples (Sample A, B, C and D) were grown.

In all the samples, the InAs layers were deposited on a 350 nm-thick GaAs buffer layer. The GaAs buffer layer was grown at $T_{sub} = 580$ ℃ with a growth rate (GR) of ~ 10 nm/min under an As$_4$ background pressure of ~10^{-6} mbar. The growth conditions and sample structures of the four samples are summarized in Table. 3.1. Samples A and B (C and D) are grown for AFM (PL) investigation.

Table 3.1 Growth condition and sample structure of sample A, B, C and D

	Sample A	Sample B	Sample C	Sample D
Holder	In-free mounting	In mounting	In-free mounting	In mounting
InAs Thickness	1.9 ML	1.9 ML	1.8 ML	2.4 ML
GaAs Capping Layer Thickness	0	0	100 nm	100 nm
T_g*	505 ±5 ℃ **	505 ±5 ℃	505 ±5 ℃	515 ±5 ℃
In-flux BEP	7.6×10^{-9} mbar	5.7×10^{-9} mbar	1.1×10^{-8} mbar	4.3×10^{-9} mbar
InAs GR	0.0052 ML/s	0.0023 ML/s	0.0055 ML/s	0.0021 ML/s

* T_g: Substrate temperature during InAs (and GaAs capping layer) growth

** ± 5 ℃: Due to the possible human errors in the evaluation of the oxide removal temperature, a ± 5 ℃ error is estimated.

Compared with sample A, the QD density of sample B is observed to have a much better homogeneity (Fig. 3.6). The standard deviation/mean value of the QD density for sample A and B are ~ 1.2 and ~ 0.67, respectively. In sample A, the trend of having the lowest dot density in the center region (point 6, 7, 10) of the wafer is consistent with the observation in the 2D temperature

distribution map shown in Fig. 3.5 (c). A large PL intensity variation exists across sample C. (Fig. 3.7 (a)). The intensity in the center region is weak as well, corresponding to the observed lower dot density in this region. In contrast to sample C, the PL intensity homogeneity of sample D is much better across a line through the center of the wafer. (Fig. 3.7 (b))

This series of tests, together with the results of the temperature characterization works discussed in Section 3.1, proves the better suitability of the In-mounting holders than the In-free mounting holders in the growth of LDQDs. Therefore, we chose the In mounting holders to investigate the optimal growth condition of LDQDs.
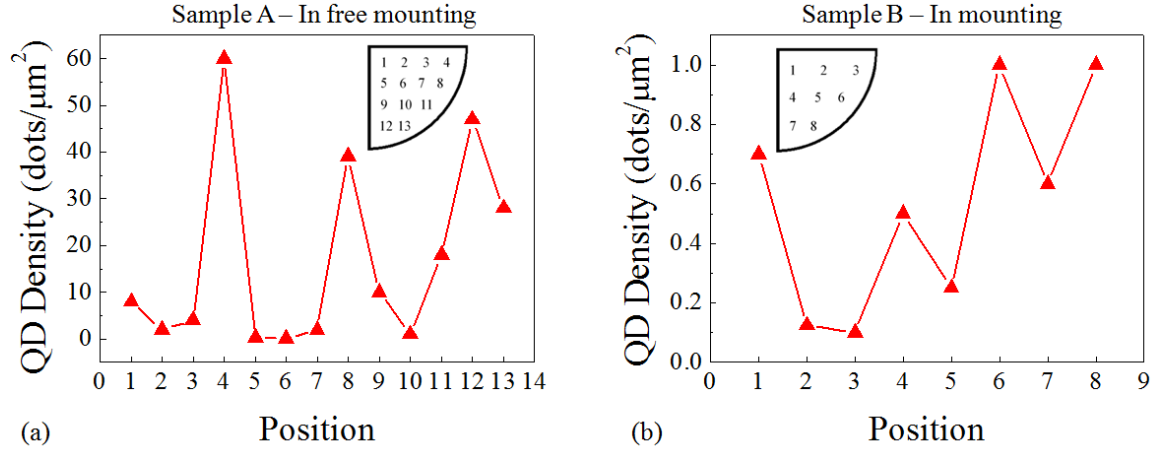

(a)

(b)

Fig. 3.6 Dot density as a function of the position of sample A (a) and sample B (b). The insets show the wafer map indicating the positions of the measured points on each wafer.

(a)

(b)
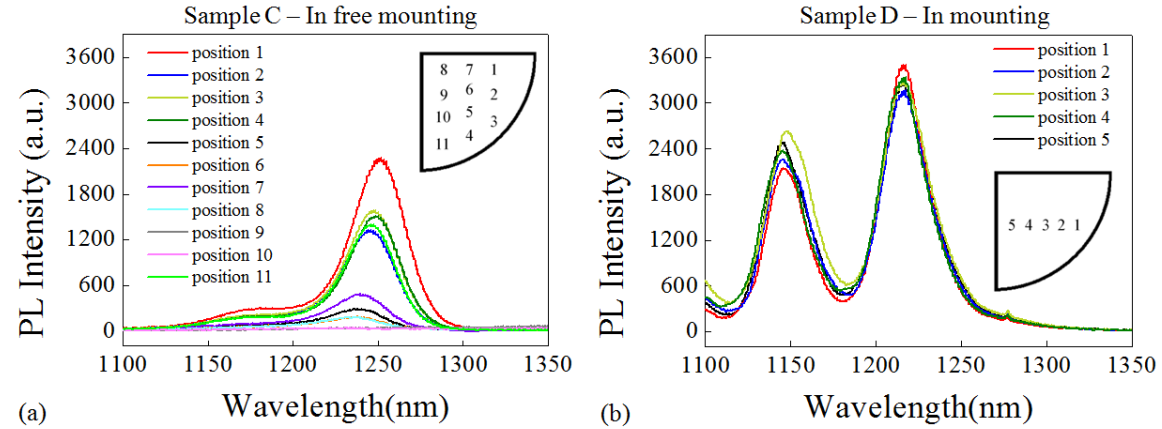
Fig. 3.7 PL spectra taken at different positions of sample C (a) and D (b). The insets show the wafer map indicating the positions of the measured points on each wafer.

3.2.2 Growth parameter optimization

From Ref. [4], we know that in order to form InAs LDQDs, an ultralow growth rate is required. Therefore, the working window of producing LDQDs becomes rather narrow. First, a high substrate temperature and a low In flux are needed to enhance the migration length of the adatoms

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on the substrate surface. In growth conditions like this, the desorption rate of adatoms is comparable to the low InAs deposition rate. As the deposition rate strongly depends on temperature, the dot density can vary significantly when the growth temperature changes. Second, the deposition amount of InAs material needs to be precisely controlled since the dot density scales with the thickness of InAs. The optimized conditions for producing LDQDs have already been given in Ref. [4]. However, due to the differences in growth systems, the author needed to optimize the growth conditions on the Createc SY022 MBE system at the Nanolab @ TU/e cleanroom. This is the background and the reason for this work described in this chapter.

Based on Ref. [4], we chose to work at the two growth temperatures $T_g = 505$ ℃ and 515 ℃. The GR of InAs at these two temperatures as a function of the In-flux beam equivalent pressure (BEP) are compared in Fig. 3.8. The growth rate was estimated by dividing the critical thickness for the formation of QDs (i.e. 1.7 ML) with the 2D-to-3D transition time of the RHEED pattern. The lower InAs GR at $T_g = 515$ ℃ is a result of the larger InAs desorption rate.
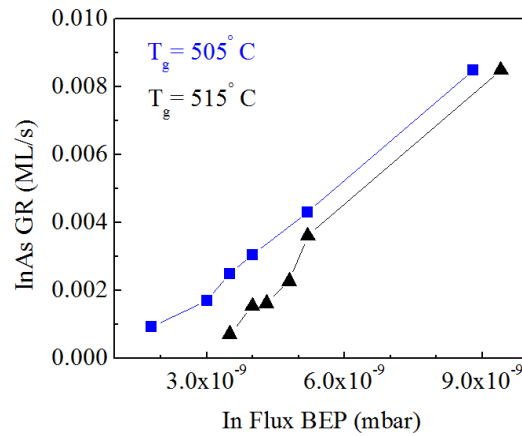

Fig. 3.8 InAs GR as a function of the In flux BEP at growth temperatures of 505 ℃ and 515 ℃.

At $T_g = 515$ ℃, by depositing 1.9 ML InAs with a growth rate of ~ 0.0023 ML/s, the average InAs QD density can be reduced down to ~ 0.6 dots/μm^2 (Fig. 3.9 (a)) . The dots are capped with 5 nm GaAs at the same temperature as the QD growth. At 10 K, with low excitation power, the LDQDs emit in the range of 1000 to 1120nm. (Fig. 3.9 (b)) Discrete excitonic emission lines can be resolved. Typical single emission lines shown in the inset of Fig. 3.9 (b) have linewidths in the 80 μeV – 100 μeV range.

When the deposition amount of InAs increases to 2.4 ML, the 10 K PL emission red shifts by > 100 nm. The number of discrete emission lines has also increased, indicating an increase in the dot density. A typical excitonic line has a linewidth of ~ 60 μeV (Fig. 3.10 (a)). Fig. 3.10 (b) shows the RT and 10 K ensemble PL spectra of this sample. The ground state (GS), 1st excited state (1 ES), and 2nd excited state (2 ES) peaks are marked in the figure. From RT to 10K, the ground state peak blue shifts by ~ 80 nm and the FWHM is reduced from 40.5 meV to 29.5 meV.
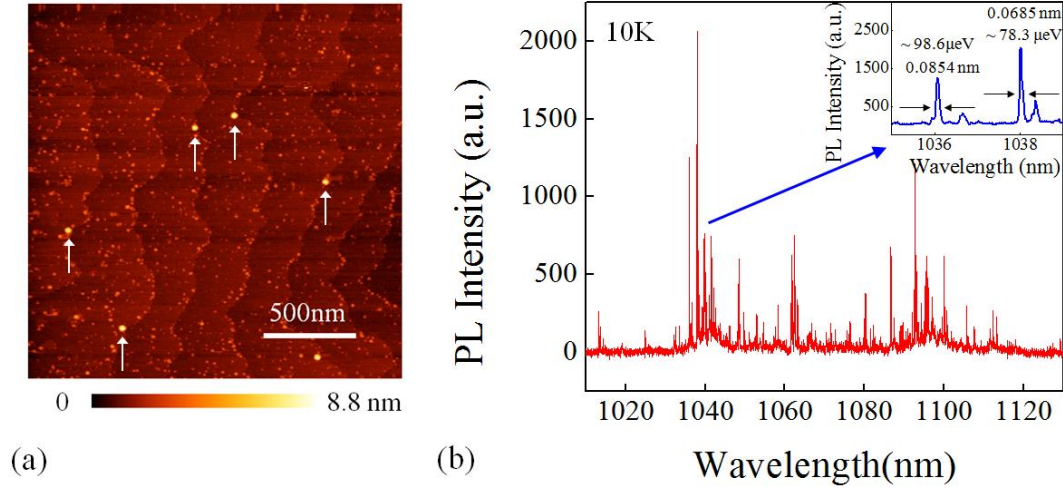
Fig. 3.9 AFM image (a) and 10 K μ-PL spectrum. The arrows indicate the position of QDs. (b) of a sample grown with 1.9 ML InAs deposited with a GR of 0.0023 ML/s at a substrate temperature of 515 ℃. The inset of (b) shows two zoomed excitonic lines from the spectrum. The FWHM of the two lines is ~ 98 μeV and ~ 78 μeV.

At RT, the wavelength of the GS peak is similar to what has been reported in Ref. [4] for samples grown at similar conditions. The FWHM of the RT GS PL peak is ~ 15 meV wider than what has been reported in Ref. [4], indicating a slightly wider distribution of the dot shape. A sample grown in the similar condition but without GaAs capping has a density of ~ 20 dots/μm^2.
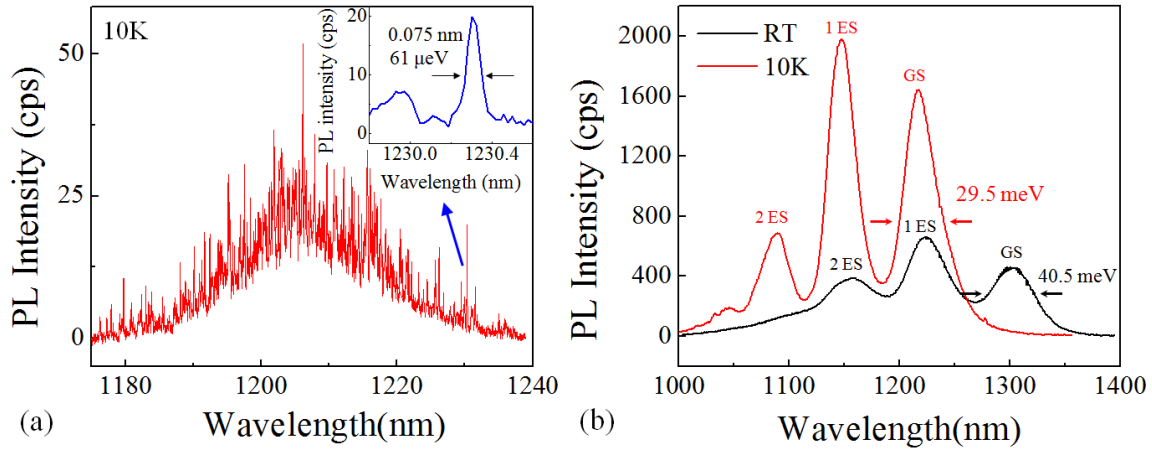

Fig. 3.10 10 K high resolution μ-PL spectrum (a) and the comparison of the RT and 10K ensemble PL of a sample grown with 2.4 ML InAs deposited with a GR of 0.0023 ML/s at a substrate temperature of 515 ℃. The inset of (a) shows a zoomed excitonic line from the spectrum. The FWHM is ~ 61 μeV.

It was important to grow QDs with GS wavelength close to 1300 nm at LT. First, this wavelength range is within the transmission window of the optical fibers. Second, this wavelength range was within the range of tunability of the available optical filters in the lab. Intuitively, one direct way to extend the QDs emission wavelength is to increase the InAs deposition amount to form bigger dots. Indeed, this method allows extending the emission wavelength. However, as the deposition

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amount increases, the QDs density increases as well. For example, when the deposition amount of InAs increases from 2.3 to 2.5 ML, the GS emission wavelength increases by ~ 10 nm whilst the integrated wetting layer (WL) peak intensity to the integrated GS peak intensity decreases for 6 times. (Fig. 3.11) As it has been discussed in Ref. [4], under the same excitation power, the WL/GS ratio is an indication of the dot density and the WL emission is more intense for low density samples. Therefore, simply increasing the InAs deposition amount is not a proper way to achieve LDQDs with long emission wavelength.
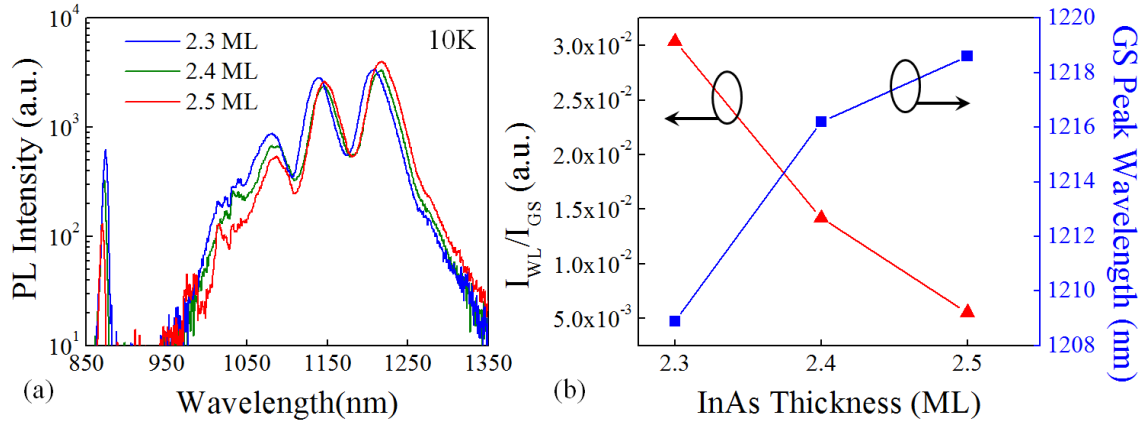

Fig. 3.11 (a) 10 K μ-PL spectra of samples grown with 2.3, 2.4 and 2.5 ML InAs capped by 100 nm GaAs. The growth temperature and growth rate for all the samples were ~ 0.0023 ML/s. (b) The I_{WL}/I_{GS} and the GS peak emission wavelength as a function of the InAs thickness.

Fig. 3.12 summarizes the dot density obtained in different growth conditions (In flux, temperature, InAs thickness). It is clear that at fixed growth temperature and amount of InAs deposited, the dot density increases with the In flux BEP (i.e. the growth rate). In addition, at the fixed growth temperature and growth rate, the dot density increases with the deposition amount. Moreover, at fixed deposition amount and growth rate, the dot density increases for lower growth temperature.
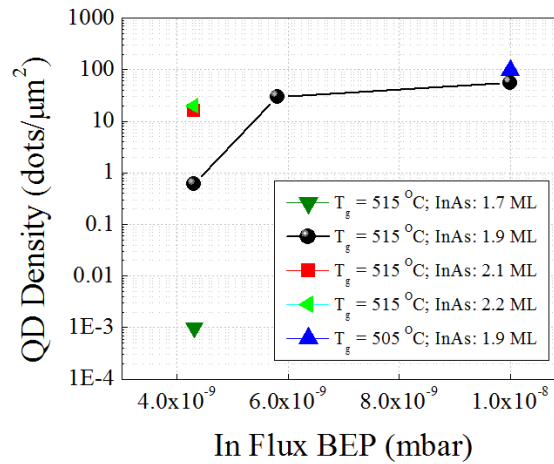

Fig. 3.12 Conclusion of the dot density achieved at several typical growth conditions.

In the experiment, a 5 nm InGaAs partial capping layer was grown on top of the QDs before the deposition of the 100 nm GaAs capping layer. To do this, a second In effusion cell was mounted to facilitate the quick switching from the low cell-temperature for QDs growth and the high cell-temperature for the capping layer growth. To determine the optimum In concentration in the InGaAs capping layer, a series of samples were grown. In all the samples, 2.1 ML InAs was deposited with a growth rate of 0.0023ML/s at T_g= 515 ℃, followed by a 30 sec annealing at the same substrate temperature. The In concentration in the InGaAs capping layer was varied from 0% to 25%. A strong dependence of the PL emission wavelength on the In concentration of the InGaAs capping layer can be observed. The FWHM of the GS peak reaches a minimum when the In concentration equals 10% (Fig. 3.13 (a)). Fig. 3.13 (b) shows the RT PL spectra of two samples capped with GaAs and $In_{0.25}Ga_{0.75}As$. A strong red shifting of ~ 85 nm in the GS emission wavelength is observed. In Ref. [4], it was reported that by increasing In concentration in the InGaAs capping layer from 0% to 15%, the GS emission peak can be red shifted by ~ 150 nm. The discrepancy could be from the differences (or errors) in the growth rate calibration.
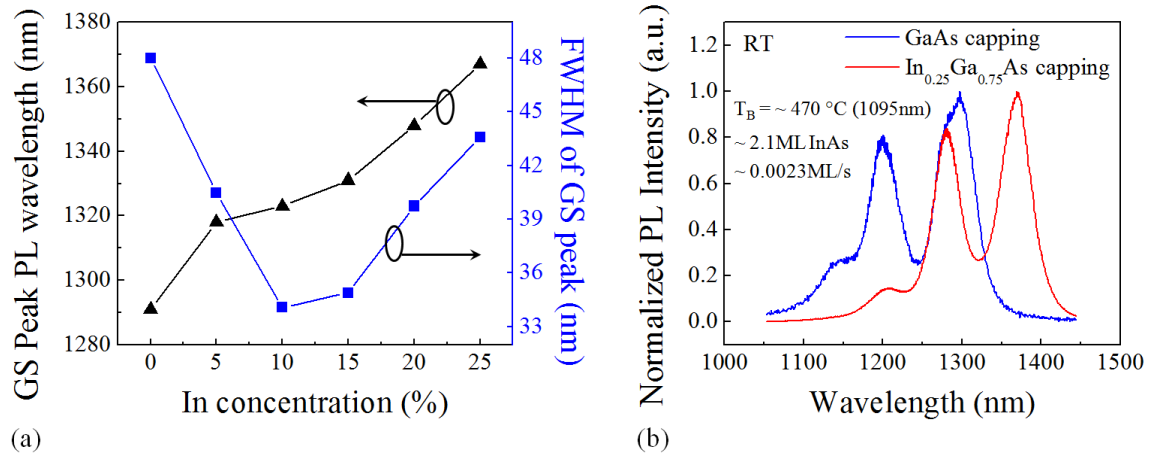

Fig. 3.13 (a) RT PL emission wavelength and FWHM width of GS peak as a function of the In concentration in the InGaAs capping layer. (b) The RT ensemble PL spectra of two LDQDs samples capped with GaAs and $In_{0.25}Ga_{0.75}As$ respectively.

The optimal growth recipe of producing low-density InAs QDs emitting at telecommunication wavelength in the Createc SY022 MBE system is given in Table 3.2.

Table 3.2 Optimized growth condition for producing low density InAs QDs at TU/e

	Layer	Thickness	GR	T_{sub}*	Background Pressure
1	GaAs buffer	350 nm	~14 nm/min	580 ℃	10^{-6} mbar
2	InAs QDs	2.1 ML	~ 0.0023 ML/s	515 ℃	10^{-6} mbar
3	$In_{0.2}Ga_{0.8}As$	5 nm	~ 14 nm/min	515 ℃	10^{-6} mbar
4	GaAs capping	100 nm	~ 14 nm/min	515 ℃	10^{-6} mbar
Air					

* T_{sub}: In the experiments, the growth temperature was estimated by using $T_{sub}/580 = T_C/T_{OR}$. In the device production, we used the temperature corresponding to the transition edge wavelength of ~ 1095 nm detected by the BandiT system.

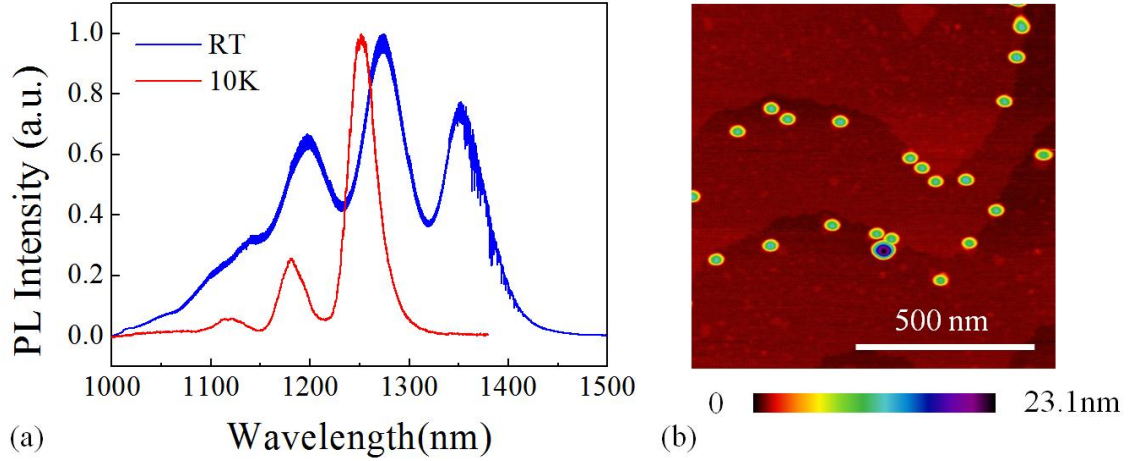Fig. 3.14 shows the PL emission and AFM image of samples grown in the optimal condition.

(a)   (b)

Fig. 3.14 RT and LT ensemble PL spectra (a) and AFM image (b) of samples grown in the optimal growth condition described in Table 3.2.

3.2.3 Growth condition optimization for production samples

The In mounting substrate holder is not suitable for producing 2-inch samples for further processing due to the limited size of the holder surface and the residue In on the backside of the sample after growth. Therefore, the 2-inch In-free holder was used.

In order to produce production samples with low-density InAs QDs on the 2-inch holder, a growth condition optimization with this holder is required. The temperature homogeneity problem on the 2-inch holder must be solved first. Similar to the ¼-In-free mounting holder, the temperature distribution provided by the 2-inch holder is also not homogeneous. Under the nominal LDQDs growth conditions of table 3.2, the dots only form close to the edge of the wafer. (Fig. 3.15)
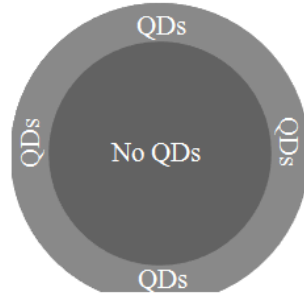

Fig. 3.15 Schematic illustration of LDQDs distribution on a 2-inch wafer.

To improve the temperature homogeneity of the holder, we modified the structure of the 2-inch holder by inserting a 2-inch pyrolytic boron nitride (PBN) diffuser plate between the holder chunk and the 1st cover ring. (Fig. 3.16) The PBN diffuser plate is able to improve the heating uniformity on the substrate by conducting heat laterally. [6] Frank van Otten performed the hand-on assembling work. As expected, the new holder with the PBN plate has shown better temperature homogeneity.

Filament Heater
Cover ring
Substrate
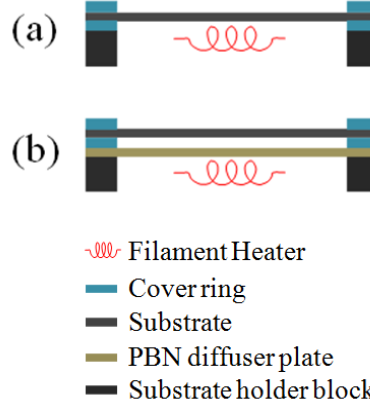*PBN diffuser plate*
Substrate holder block

Fig. 3.16 Schematic illustration of the side view of a typical 2-inch holder (a) and a modified 2-inch holder with a PBN diffuser plate inserted.

With the help of the BandiT system, it is easy to optimize the growth condition for the 2-inch holder based on the previous investigation on In mounting holders as described in Section 3.2.2. The major task is to reproduce the same growth temperature as that on the In mounting holders. Taking the advantage that BandiT calculates the temperature based on the 'transition edge' of the collected diffusive reflection spectra, the wavelength of the 'transition edge' can be used to precisely compare the absolute growth temperature on different systems. At thermocouple read T_c ≈ 660 °C, the 'edge' wavelength (denote as 'λ_T') of the substrate on 2-inch holder with PBN plate equals ~ 1097 nm. This wavelength reproduces the 'edge' wavelength of a substrate on the In mounting holders at the optimal QD growth temperature (515 °C according to Section 3.2.2). Fig. 3.17 shows the calibration data of the transition edge wavelength of a substrate mounted on the 2-inch PBN holder as a function of the thermocouple temperature T_c.

By depositing 2 ML InAs capped with 100 nm GaAs under a In-flux BEP of 4.1×10^{-9} mbar at a substrate temperature for which $\lambda_T \approx 1097$ nm, QDs were grown on a 2'' substrate with dot density in a range of 10 ~ 30 dots/μm^2, as observed at various positions on the substrate. The RT μ-PL spectra taken at different positions of the sample are shown in Fig. 3.18.

3.3 Conclusion

In this chapter, first, the temperature homogeneity of substrates mounted on different types of sample holders has been studied and optimized. In addition, the growth conditions of low density, long-wavelength QDs on GaAs have been optimized. Under the optimized growth conditions,

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LDQDs with homogeneous density distribution across 2'' wafers can be produced. The QDs produced with this method have been used in the experiments of:

(a) Electromechanical tuning of double-slab photonic crystal cavities [1]

(b) Electromechanical tuning of vertically coupled photonic crystal nanobeams [2]

(c) Independent control of the exciton energy and of cavity mode wavelength in a photonic crystal cavity [3]

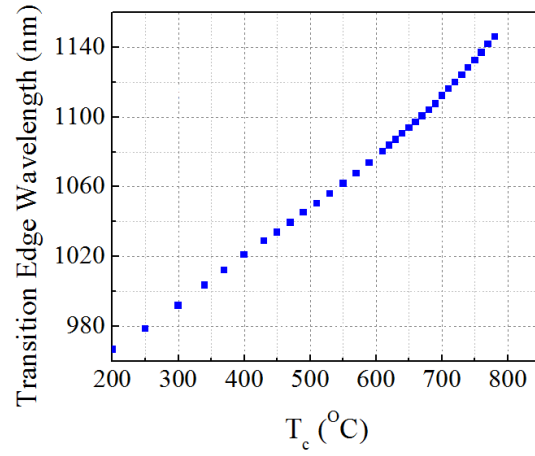(d) Cavity optomechanics in vertically-coupled photonic crystal nanobeams [7]

Fig. 3.17 The transition edge wavelength as a function of thermocouple reading 'T_c' for a substrate mounted on a 2-inch In-free holder with PBN plate.
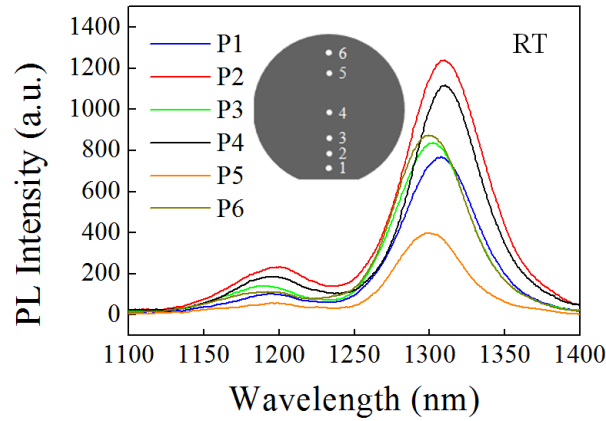

Fig. 3.18 PL spectra taken at different positions on a 2-inch sample. The insets show the wafer map indicating the positions of the measured points on each wafer.

Reference

[1] L. Midolo, F. Pagliano, T. B. Hoang, T. Xia, F. W. M. van Otten, L. H. Li, E. H. Linfield, M. Lermer, S. Höfling, and A. Fiore, "Spontaneous emission control of single quantum dots by electromechanical tuning of a photonic crystal cavity", *Applied Physics Letters*, vol. 101, p 091106 (2012).

[2] L. Midolo, S. N. Yoon, F. Pagliano, T. Xia, F. W. M. van Otten, M. Lermer, S. Höfling, and A. Fiore, "Electromechanical tuning of vertically-coupled photonic crystal nanobeams", *Optics Express*, vol. 20, p 19255 (2012).

[3] F. Pagliano, Y. J. Cho, T. Xia, F. W. M. van Otten, R. Johne and A. Fiore, "Dynamic controlling the emission of single excitons in photonic crystal cavities", accepted by *Nature Communication* (2014) .

[4] B. Alloing, PhD thesis, "Growth and characterization of single quantum dot devices for fiber-based quantum communications" (2006).

[5] B. Alloing, C. Zinoni, V. Zwiller, L. H. Li, C. Monat, M. Gobet, G. Buchs, A. Fiore, E. Pelucchi, and E. Kapon, "Growth and characterization of single quantum dots emitting at 1300 nm", *Applied Physics Letters*, vol. 86, 101908 (2005).

[6] http://www.google.com.ar/patents/US5388909

[7] S. Westerndorp, Master thesis, "Cavity optomechanics in vertically-coupled photonic crystal nanobeams and membranes", Eindhoven University of Technology (2014).

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CHAPTER 4

Growth of site-controlled InAs/GaAs QDs

In this chapter[*], the author discusses the preliminary results on the growth of site-controlled InAs/GaAs QDs on nano-patterned substrates. In Section 4.1, the fabrication procedures of nano-patterned substrates are introduced. Then, experimental details and results of the growth of site-controlled InAs/GaAs QDs are shown in Section 4.2. In Section 4.3, the applicability of two deoxidation methods for the oxide removal on patterned substrates is compared.

4.1 Fabrication of nano-patterned substrates for SCQDs growth

In August 2011, the author spent one week to study the technique of substrate fabrication and the growth of SCQDs in the Nanophotonics group of the Department of Applied Physics at the Universität Würzburg. After coming back, the author developed the processing recipe at the Nanolab @ TU/e cleanroom based on the experience and knowledge transferred from Würzburg.

4.1.1 General process flow for the fabrication of nano-patterned substrates

Generally speaking, the size of the nanoholes needed for the growth of SCQDs is 100 ~ 150 nm in diameter and 15 ~ 20 nm in depth. In the experiment, nanohole arrays were patterned in the center of square mesas in order to facilitate the characterization of the nanoholes. Alignment markers were patterned on the substrate as well to provide references for the alignment between optical and e-beam lithography masks. The major processing steps for producing nano-patterned substrates are illustrated as follows:
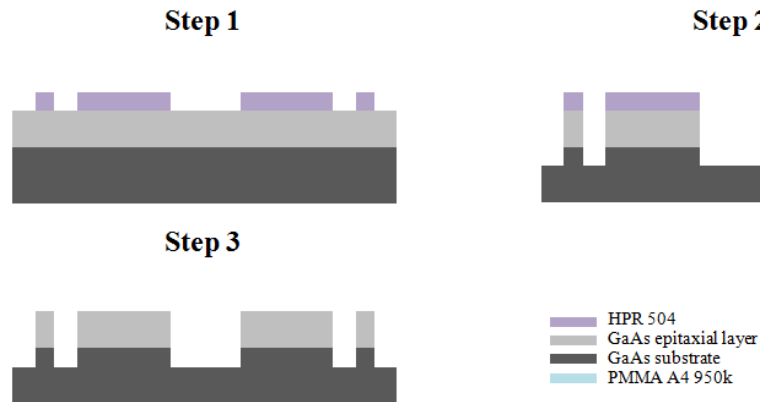
➢ **Etching of mesas and alignment markers** (Fig 4.1)

Fig. 4.1 Schematic illustration of the etching of mesas and alignment markers. （Step 1–3）

_____

- Step 1: Definition of square mesas and alignment markers by optical lithography. (Details of the design of the optical lithography mask will be introduced in Section 4.1.2.)
- Step 2: Etching of the GaAs epitaxial substrate (GaAs epi-ready substrate with thick GaAs buffer layer grown on top) with the solution of H_2SO_4: H_2O_2: H_2O (8: 16: 200) (with etch rate of ~ 25 nm/s) for 40 seconds to get an etch depth of ~ 1 μm.
- Step 3: Removal of PR with acetone (5min + 5min + 5min) ultrasonic bath. Rinse the sample in isopropanol for 3 min.
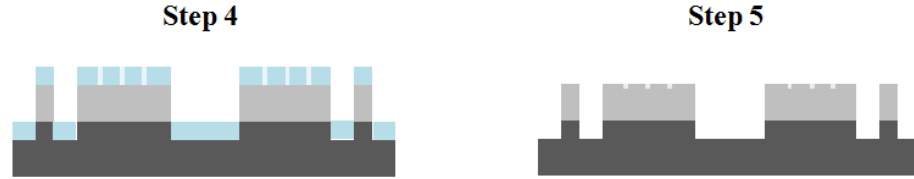
➢ **Etch of nanoholes**

Fig. 4.2 Schematic illustration of mesas and alignment markers etch. （Step 4–5）

- Step 4: Definition of nanoholes in the central area of mesas with EBL on a PMMA resist.
- Step 5: Etching of nanoholes into GaAs with the solution of H_2SO_4: H_2O_2: H_2O (0.5: 4: 600) (with etch rate of ~ 0.5 nm/s) for ~ 15nm in depth. Remove PMMA resist with acetone ultrasonic bath and isopropanol (similar to Step 3).

Before mounting the substrate to sample holders for MBE overgrowth, the substrate is cleaned first by rinsing in concentrated H_2SO_4 (96%) for 100 sec followed by 5 min distilled water rinse, then by rinsing in HCl (36%): H_2O (1:1) for 1 min followed by another > 5 min distilled water rinse.
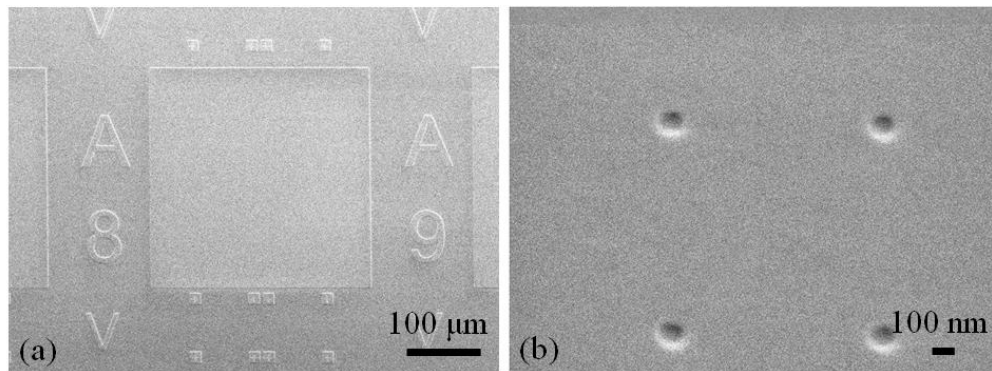

Fig. 4.3 SEM image of a GaAs substrate after Step 3 (a) and Step 5 (b). In (a), square mesas, local alignment markers, and character markers for the mesas can be seen. In (b), nanoholes fabricated in the center of a mesa can be observed. The holes are approximately 100 nm in diameter.

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4.1.2 Fabrication process optimization

Design of optical lithography mask

The optical lithography mask is designed by the author for working with 2-inch wafers. In total, 32 square blocks exist in the design. There are 8 blocks for each one quarter of a 2-inch wafer. As shown in Fig. 4.4, each block consists of a 10×10 array of mesas. 10 rows of character makers (from 'A' to 'J') and 10 columns of number makers (from '1' to '10') serve as coordinate markers for the mesas. The size of each mesa is 300×300 μm^2. The local alignment makers are designed for possible needs in the future to align the photonic devices with the SCQDs. The number characters, such as '011', mark the crystal direction for each block. The markers help to identify the crystal direction after the sample is cleaved into small pieces.
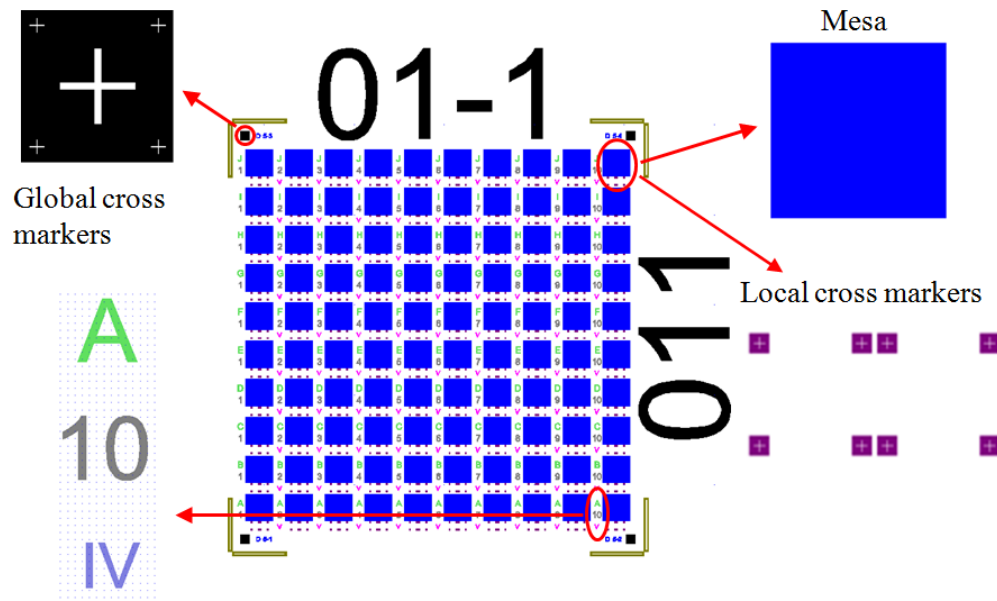

Fig. 4.4 Outlook of one block (a) and zoomed views of major components of the block.

Fabrication of nanoholes - EBL dose calibration

As mentioned in Chapter 2, the PMMA A4 950k resist was used to define nanoholes with EBL. The reason of using this resist instead of the more commonly used ZEP 520A resist in the Nanolab @ TU/e cleanroom is due to the smaller thickness after spin coating that the PMMA can reach. As a direct consequence, a smaller front scattering range of the electrons (i.e. smaller feature size) can be achieved. The author performed a series of EBL dose calibration tests on the PMMA resist and developed the recipe to generate nanoholes with ~ 100 nm size of diameter.

The PMMA was spin-coated by the Convac-Spinner with at a spin speed of 9000 rpm for 60 sec. The resulting thickness of the resist is approximately 140 nm. It is worth noting that 9000 rpm is the upper limit of the rotation speed of the Spinner and the spin speed can be not very stable each time. As a result, the coated resist thickness can vary slightly case by case.

To produce the nano-patterned substrates for SCQDs growth, the required feature size developed by EBL is about 50 ~ 60 nm. The size is very close to the size limit that the 30 kV Raith 150 Two EBL system can develop on the 140 nm PMMA resist. In our case, the patterning of the tiny structures is very sensitive to the thickness of the resist since the dose for opening certain features on a resist is critically dependent on its thickness. In all the EBL dose calibration tests, to exclude the influence of the thickness variation of the resist on the opening of structures, nanoholes with various sizes and doses are included in the EBL digital mask design. The design parameters which guarantee the reproducible opening of the tiny features on the resist spinned in different cases were chosen as the patterning parameters for further experiments.

Due to the tiny opening size and the shallow depth of the features on the resist and the charging effect, it is difficult to check the opening of the feature with equipment, inside the cleanroom, such as SEM and TENCOR Step Height Analyzer. Actually, locating the position of the EBL exposed nanoholes on the resist can already be very difficult without observable markers close by. Considering the fact that only the size of features on GaAs after the wet chemical etching is interesting to the experiment, the author used a solution to speed up and simplify the dose calibration test. First, the H_2SO_4: H_2O_2: H_2O (0.5: 4: 600) etchant was used to etch the GaAs substrate after the development of the resist. Then, the resist was removed by the O_2 plasma stripping. By checking the opening of the features on the GaAs surface with optical microscope, SEM or AFM, the opening of the features in the resist by EBL can be determined. (If the feature in the resist is not completely opened, the etchant will not be able to etch the GaAs substrate through the openings in the resist. If the shape/profile of the etched patterns on the GaAs substrate is irregular, it means the dose for opening the structures in the resist is lower than needed.)

Fig. 4.5 shows the statistical analysis of the diameter of holes in the GaAs substrate as a function of the hole diameter in the EBL mask design. The EBL dose for the holes in this case is 600 μC / cm^2. In this case, when the hole diameters in the mask design is in the range from 20 to 35 nm, the hole diameters in the GaAs substrate after chemical etching are no larger than 100 nm.
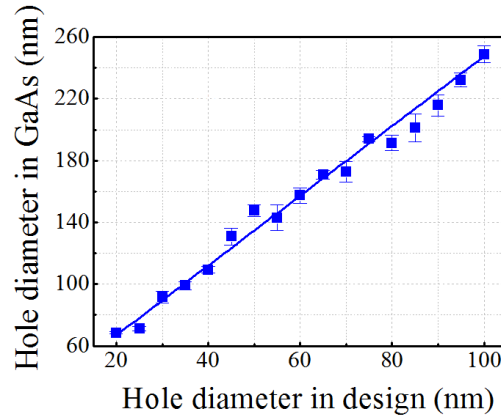

Fig. 4.5 Hole diameters in GaAs after chemical etching as a function of the hole diameter in the EBL mask design. The dose factor of the holes is 600 μC/cm^2 in design. The wet etching time of the GaAs substrate is 35 s.

Since it is not practical to make dose calibration test for every spin-coated wafer, in all the EBL designs for producing nano-patterned substrates, several different hole diameters and dose factors close to the optimized patterning parameters in the dose calibration tests were included.

4.2 Growth of site-controlled InAs/GaAs QDs

The time required for producing a 2-inch nano-patterned substrate for SCQDs growth in the Nanolab @ TU/e cleanroom is ≥ 3 days. The length of the processing period is mainly limited by the regular waiting time in the machine reservation system and the EBL exposure time. In addition, the EBL sample holder plate of the Raith 150 Two system only allows loading ≤ ½-2-inch wafer each time. This also limits the general processing speed. To shorten the time spent on processing and to make a better use of the patterned wafer, one part of the wafer was cleaved and used in each growth. Basically, a patterned 2-inch wafer can be used for 32 growth tests.

Considering the size of the wafer and the temperature homogeneity provided by different holders (Section 3.1), the In mounting holders were chosen to be used for the growth of SCQDs. The Bandit system was used to determine the temperature on the substrate.

4.2.1 Native Oxide Removal (Atomic-hydrogen assisted deoxidation)

Before being loaded into the MBE system, the patterned substrate undergoes an HCl (36%): H_2O (1:1) rinse to remove the oxide layers on top. However, during mounting the wafer with melted In on the Molybdenum holder, a layer of oxide (Fig. 4.6) is formed on the surface due to its air exposure at elevated temperatures (between 170 ℃ and 200 ℃) of the hot plate.

To perform a defect-free epitaxial growth on the patterned substrate, the native oxide needs to be removed in a gentle way.[1] According to the literature [2]-[6], the atomic-hydrogen assisted deoxidation (HAD) method is a suitable method to provide oxide-free substrate surfaces without damaging the fragile nano-patterns. Therefore, the author chose to work with the HAD method in the beginning of this work.
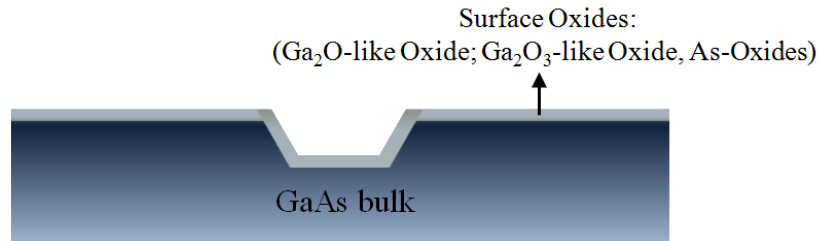

Fig. 4.6 Schematic illustration of an oxide layer formed on a nano-patterned substrate.

There are mainly three types of oxides on the GaAs surface: Ga_2O-like oxide, Ga_2O_3-like oxide, and As-oxides. The Ga_2O-like oxide and the As-oxides desorb from the GaAs surface at moderate substrate temperature of ~ 400 ℃. [5] The Ga_2O_3-like oxide is more thermally stable and therefore is considered to be the major type of oxide to be dealt with.

The HAD method is based on the chemical reaction between the atomic hydrogen and the Ga_2O_3:

$$Ga_2O_3 + 4H \rightarrow Ga_2O\uparrow + 2H_2O\uparrow \qquad\qquad (4.1)$$
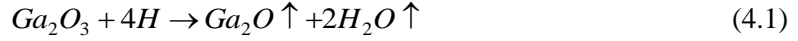
In the reaction, the solid-phase Ga_2O_3 is converted to the more volatile Ga_2O, which starts to decompose at substrate temperatures of 350 - 400 ℃.[4] In the Createc SY022 MBE system, it is possible to perform the HAD procedure in both the load-lock chamber and the growth chamber. We executed it in the load-lock chamber to prevent any possible contaminations to the growth chamber. The background pressure of the load-lock chamber was at the level of 1.0×10^{-8} mbar.
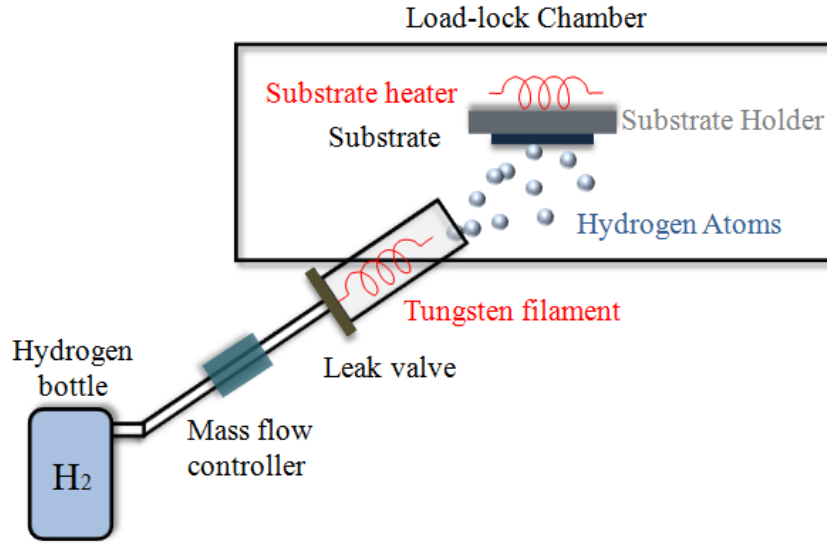

Fig. 4.7 Schematic illustration of hardware components used in the HAD and the basic experimental configuration in the load-lock chamber.

As shown in Fig. 4.7, the substrate was mounted on the heating stage of the load-lock chamber and was heated up by a W-filament heater. The temperature of the substrate was monitored by a thermocouple. The hydrogen gas was guided from the hydrogen bottle to the load-lock chamber via a pipe transfer line. The gas flow was adjusted to 2 sccm and monitored by a mass flow controller (MFC). To perform the HAD procedure, the leak valve was manually opened to introduce the hydrogen gas to the load-lock chamber to reach a background pressure of 3.2×10^{-5} mbar. The W-filament was heated up to a 1250 ℃ to crack the hydrogen molecules into the hydrogen atoms. The hydrogen atoms impinged on the heated substrate and reacted with the oxide layer on the surface.

The influence of the substrate temperature on the surface morphology of the patterned substrate was investigated. Three samples were cleaned with atomic hydrogen for 30 min at substrate temperatures of 350 ℃ (sample A), 450 ℃ (sample B) and 550 ℃ (sample C). After the HAD cleaning, the samples were unloaded for AFM investigation. Fig. 4.8 (a) and (b) show AFM images of sample B and the comparison of the averaged hole profiles along the [01-1] directions through the center of the holes of the three samples. The hole pitch in all the samples is 500 nm in design. A slight deviation of the hole pitches in the AFM image (and the cross section profile) from the design is due to the calibration error of the piezo of the AFM. The surface morphology

of the three substrates does not show differences from each other (the difference between the three samples in surface roughness is within the experimental uncertainty). (Fig. 4.8 (c)) In the end, 450 ℃, as the median, was chosen as the substrate temperature in the HAD process for future samples. A RHEED image of sample B after the HAD process is shown in Fig. 4.9. The bright specular spot indicates an oxide free surface.
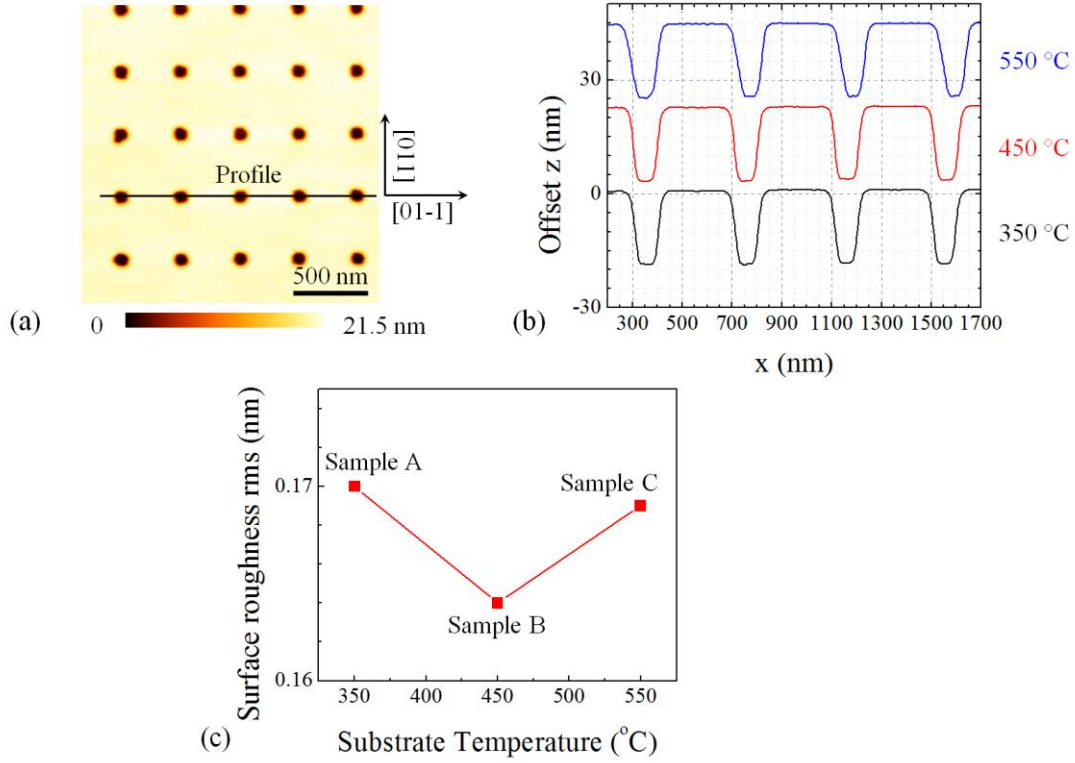

Fig. 4.8 (a) An AFM image of sample B. (b) Line profiles of the holes along the [01-1] direction (illustrated in (a)) through the center of the holes of sample A, B and C. (c) Comparison of the surface roughness rms value of sample A, B and C in 5×5 μm^2 planar areas without nanoholes as a function of the substrate temperature during the HAD process. The difference between the three samples in surface roughness is within the experimental uncertainty.
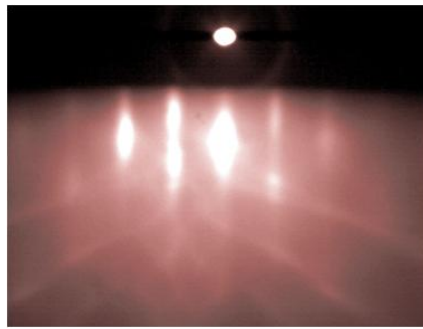

Fig. 4.9 RHEED image of sample B after the HAD process at the substrate temperature of 100 ℃ with the absence of Arsenic.

4.2.2 GaAs buffer layer growth

According to Ref. [6]-[9], a thin GaAs buffer layer deposited on the patterned substrate can help to smoothen the surface, separate the optically active QDs from the patterned interface and thus improve the optical quality of the QDs. One important criterion for choosing the thickness of the buffer layer is to have the nano-patterns preserved after the buffer layer growth.

A series of four samples (D, E, F, and G) were grown to explore the suitable buffer layer thickness. The four substrates were processed and cleaned with the HAD procedure under the same conditions. Afterwards, the samples were transferred to the growth chamber and heated up in an Arsenic background with a pressure of $\sim 1 \times 10^{-6}$ mbar to the substrate temperature for which $\lambda_T = 1115$ nm. Then, GaAs buffer layers with thicknesses of 4 nm, 9.3 nm, 12 nm, 24 nm were deposited with a growth rate of ~ 10 nm/min. The samples were cooled down immediately after growth, unloaded from the MBE system and measured with the AFM.
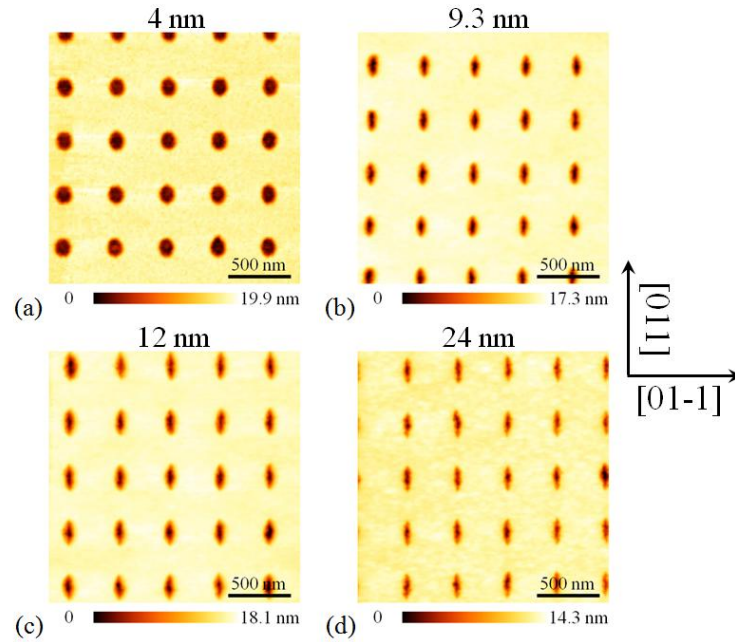

Fig. 4.10 (a) (b) (c) (d) AFM images of sample D, E, F, G with the deposition of 4 nm, 9.3 nm, 12 nm and 24 nm GaAs buffer layer on the patterned substrate, respectively.

Fig. 4.10 shows the AFM images of the four samples. Fig. 4.11 (a) shows the averaged line profiles along the [01-1] direction through the center of the holes for each sample. It is easy to see that the hole profile dramatically changes as the buffer layer thickness increases from 4 to 9.3 nm. The holes evolve towards a conic shape with increasing GaAs thickness. No significant differences are observed for the hole shape between sample E and F while the hole depth decreases by 1 nm in sample F as compared to sample E (Fig. 4.11 (b)). As the thickness of the buffer layer increases to 24 nm (sample G), the hole depth decreases down to ~ 10 nm and the hole volume decreases as well, indicating the filling of the holes by the deposited GaAs.

The length/width ratios of the holes in samples D to G are shown in (Fig.4.11 (c)) When the buffer layer thickness increases, the width/length ratio of the holes in the sample increases by a factor of 3, indicating a strong tendency of elongation of the hole shape. The reason can be explained with the directional migration of Ga adatoms towards the more Arsenic-rich side facets in the [01-1] direction[10]. It can be seen that the length/width ratio of the holes with no buffer layer deposited is less than one (the ratio in ideal case). The reason comes from the influence of the error in the AFM calibration with piezos moving in the x and y directions.
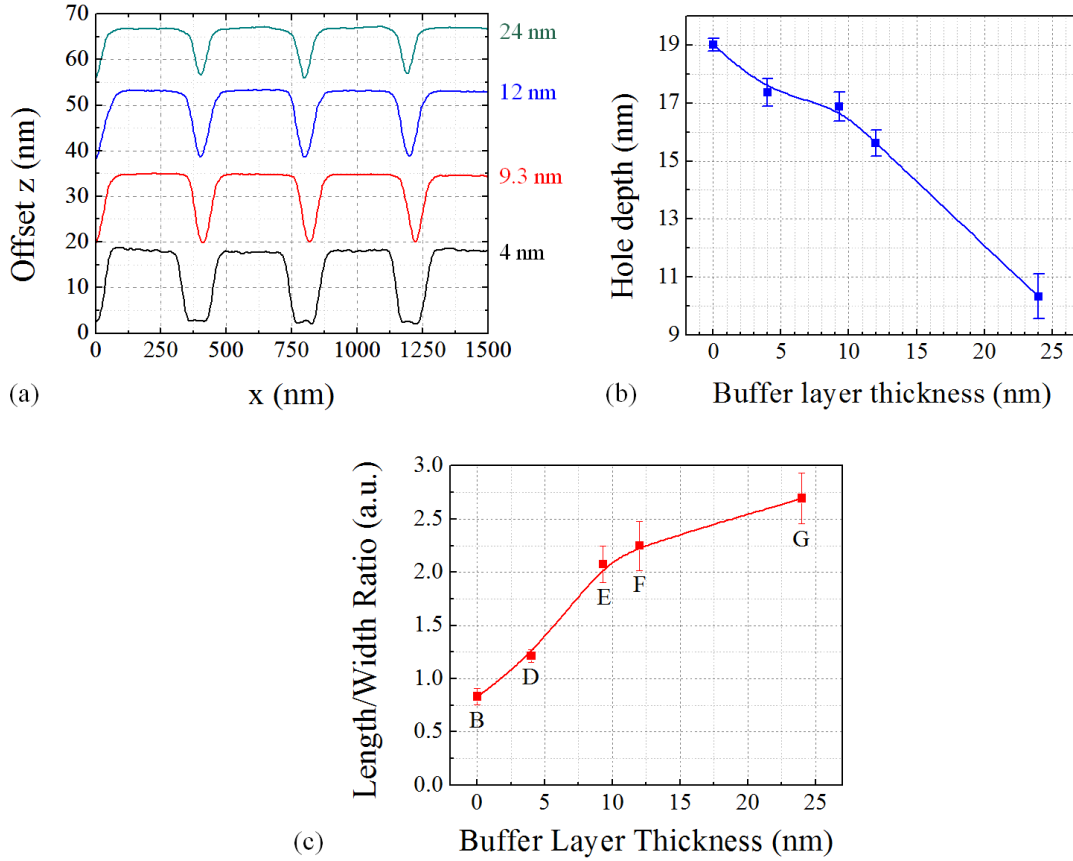

Fig. 4.11 (a) Averaged line profiles of sample D, E, F, G. Each profile was averaged over four line scans. (b) Nanohole depth as a function of the buffer layer thickness. (c) Length/width ratio of nanoholes as a function of the buffer layer thickness. The solid line in (b) and (c) are to guide the eye.

In the growth of subsequent samples, 8 nm buffer layer was grown at the substrate temperature for which $\lambda_T = 1100$ nm (same as the temperature for the growth of seeding layer). The purpose of keeping the same temperature was to minimize the time of keeping the patterned substrate at high temperature since annealing the patterned substrate can cause a pattern deformation due to the migration of GaAs material.

4.2.3 InAs seeding layer growth

After the GaAs buffer layer growth, a layer of InAs is deposited to (partially) fill the holes on the buffer layer. As explained in Ref. [7], the InAs layer is acting as a seeding layer which will guide the formation of the second layer of SCQDs in the 2-layer-stacked structures (Fig. 4.12).
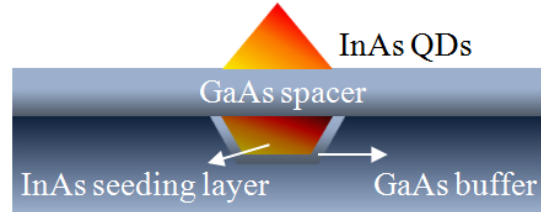

Fig. 4.12 Schematic illustration of the 2-layer-stacked SCQD structure.

As explained in Section 1.2.2, when InAs is deposited on the patterned substrate, QD structures tend to form first in the nanoholes and therefore the critical thickness for the formation of QDs in the nanoholes is smaller than that on planar substrates. In order to prevent forming unwanted QDs on the planar area of the substrates, the amount of the InAs material needs to be controlled precisely.

To investigate the optimal thickness for the seeding layer, five samples (H, I, J, K, L) were grown with the thickness of the InAs layer equal to 1.1, 1.2, 1.4, 1.7, 2.0 ML, respectively. All the samples were cleaned with the standard HAD procedure at $T_{sub} = 450$ ℃. After the growth of a 8 nm GaAs buffer layer at a temperature for which $\lambda_T = 1100$ nm, the InAs seeding layer was deposited with a growth rate of ~ 0.0023 ML/s.
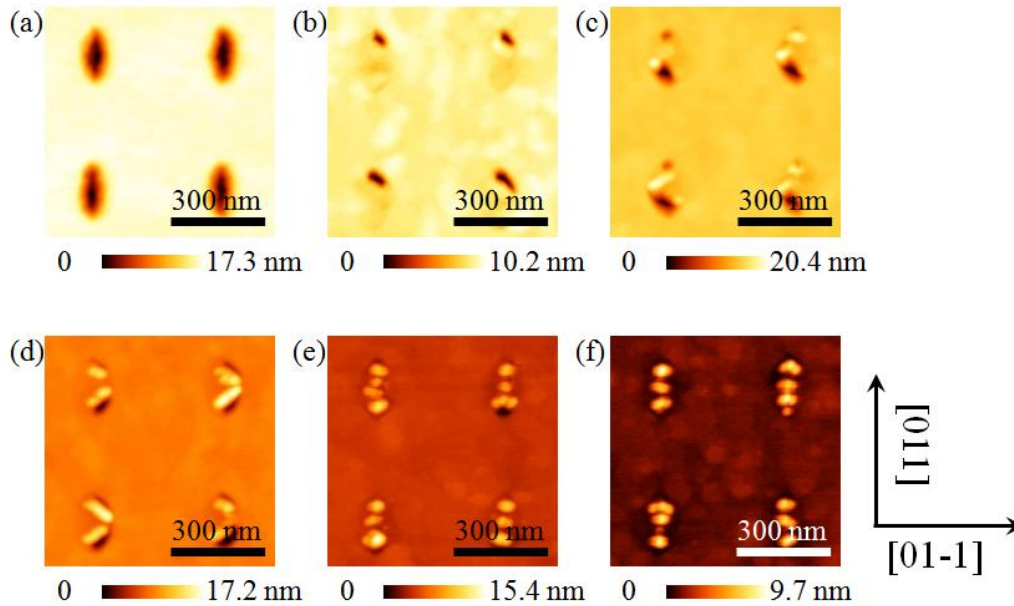

Fig. 4.13 AFM images of sample E (a) (reference, holes before regrowth), H (b), I (c), J (d), K (e), L (f) after the deposition of 1.1, 1.2, 1.4, 1.7, 2.0 ML of InAs on 8 nm GaAs buffer layer as the seeding layer, respectively.

The substrate temperature for the seeding layer growth and the growth rate of InAs was chosen to be equal to the optimal substrate temperature for the growth of LDQDs in Chapter 3. The purpose is to provide enough adatom migration length for the growth of the dilute array of SCQDs.

AFM images of sample H to L are shown in Fig. 4.13 (b) to (f). The AFM image of sample E is added to Fig. 4.13 (a) as well to show the hole shape after the buffer layer growth. As it can be seen with 1.1 ML InAs, the holes are partially filled and no clear 3D structures are observed in the holes. With the InAs amount increasing to 1.2 and 1.4 ML, 3D mounds start to form in the holes although part of the holes stays unfilled with InAs. The number density of the 3D mounds in sample I and J are 1.5 mounds/hole and 2 mounds/hole. As the InAs amount increases to 1.7 and 2.0 ML, the holes are almost filled and the number of 3D mounds per hole increases. In the meanwhile, the alignment of the 3D mounds in the holes is also changed. The reason is not clear to the author yet.

The criterion for choosing the optimal InAs amount for the seeding layer is to fill in the holes as much as possible without forming 3D structures. Based on this, 1.1 ML was initially chosen as the optimal amount. However, results similar to Fig. 4.13 (b) were not very reproducible in following tests. Therefore, 1.2 ML was chosen as the optimal amount for the InAs seeding layer of future samples.

4.2.4 Growth of the 2nd layer of InAs QDs

Similar to Ref. [7], after the growth of the InAs seeding layer, a 10 nm GaAs spacer layer was deposited with a growth rate of 10 nm/min at the same substrate temperature as the seeding layer growth. A 1 minute growth interruption was introduced to smoothen the surface of the spacer layer. Then, the second layer of InAs was deposited to form QDs. Due to the difference in the lattice constant in the GaAs spacer layer above the 2D or 3D mounds which are buried underneath, the 2nd layer of InAs QDs will form first above the patterned sites. As a result, the critical layer thickness of the 2nd layer of InAs QDs is thinner than the nominal thickness for InAs QDs formed on the planar GaAs substrates.

To investigate the growth of the 2nd layer of InAs QDs, a series of three samples (M, N, O) were grown with 1.2, 1.6 and 2.0 ML chosen as the amount of the deposited InAs. For all the samples, the 2nd layer of InAs was grown at the same growth condition as the InAs seeding layer. After growth, the sample was cooled down immediately and unloaded for AFM measurements. In all the samples, nanoholes arrays with pitches of 250 nm, 500 nm, 1 μm, and 2 μm were patterned on different mesas.

The AFM images of sample M, in which 1.2 ML InAs was deposited on the 2nd layer, are shown in Fig. 4.14 (a) - (d). No nanostructure arrays can be observed from Fig. 4.14 (a) for mesas with the hole pitch of 250 nm. As the hole pitch on the mesa increases to 500 nm (Fig. 4.14 (b)), nanostructure arrays start to appear on the surface. The size of the nanostructures increases as the hole pitches enlarges (Fig. 4.14 (b) – (d)). Fig. 4.14 (e) shows the averaged line profiles of the nanostructures along the [011] direction through the center of the nanostructures. From the chart, the gradual appearance of the periodical nanostructures and the increase of the height with the

hole-to-hole distance can be clearly observed. When the hole pitch equals 2 μm, the height of nanostructures ("nanopads") is still less than 1 nm.
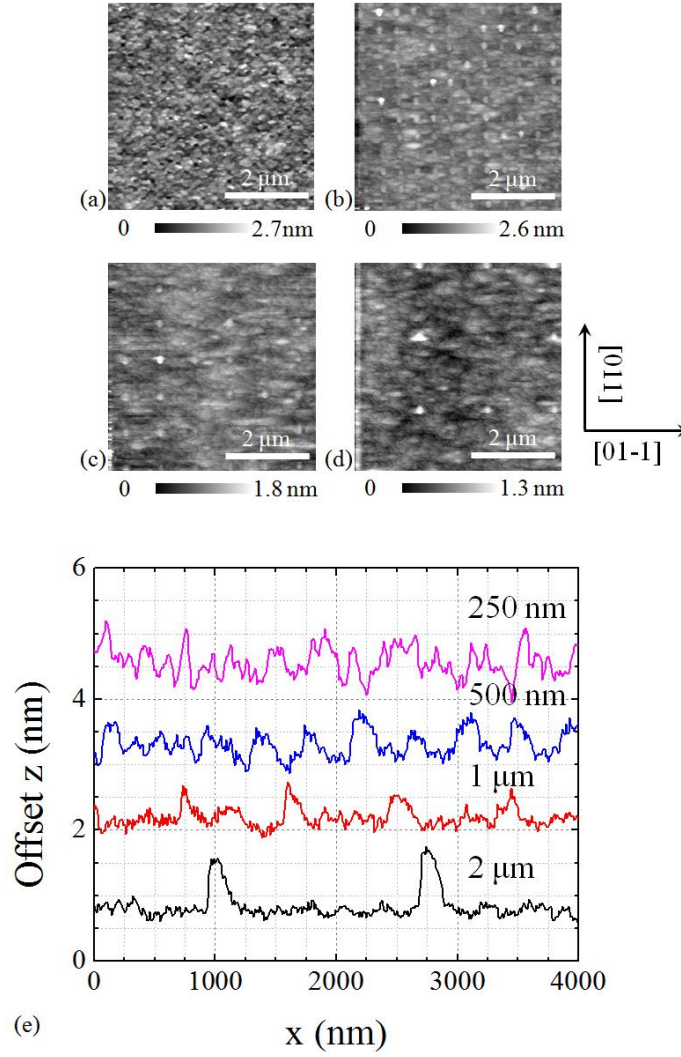

Fig. 4.14 (a)-(d) AFM images of nanostructures grown on patterned mesas with hole pitches of 250nm (a), 500 nm (b), 1 μm (c) and 2 μm (d) of sample M. (e) is the averaged line profiles of the nanostructures in the four mesas.

The AFM images of sample N, in which 1.6 ML InAs was deposited on the 2nd layer, are shown in Fig. 4.15 (a) – (d). Similar to the case of sample M, no periodic nanostructure arrays can be observed from Fig. 4.15 (a) for mesas with hole pitch of 250 nm. For mesas with hole pitches from 500 nm to 2 μm (Fig. 4.15 (b)-(d)), arrays of prominent nanostructures appear on the surface. Fig. 4.15 (e) shows the averaged line profiles of the nanostructures. According to the theory of the re-distribution of materials over arrays with different density, a gradual increase of the size of nanostructures with the hole pitches is expected. However, the nanostructures with the hole pitch of 500 nm are observed to have the largest size.
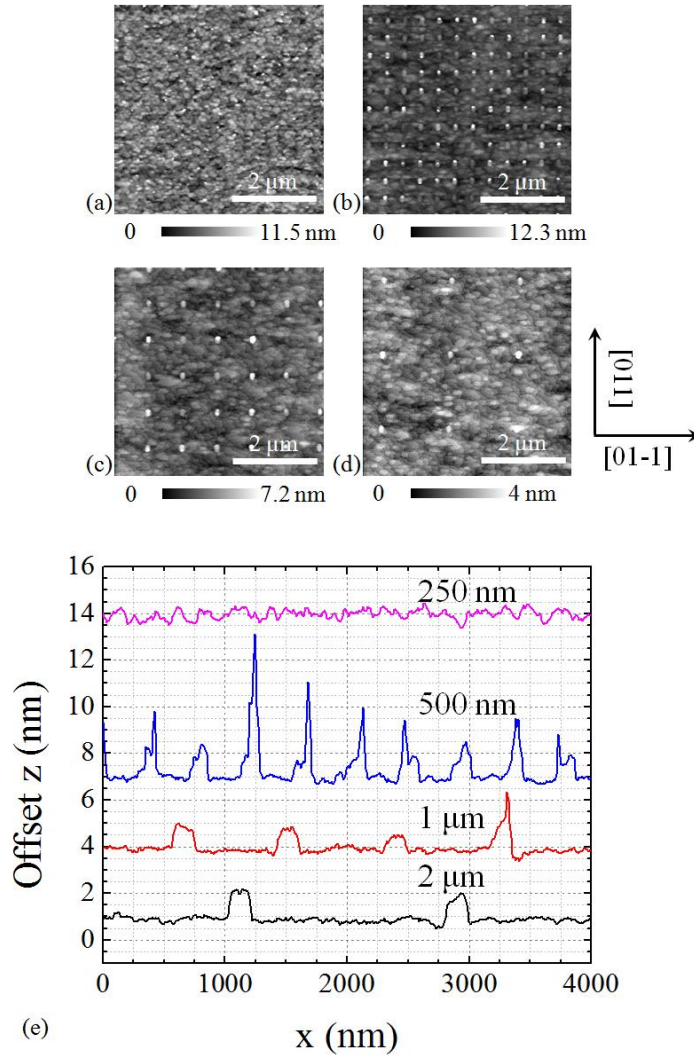
Fig. 4.15 (a)-(d) AFM images of nanostructures grown on patterned mesas with hole pitches of 250 nm (a), 500 nm (b), 1 μm (c) and 2 μm (d) of sample N. (e) is the averaged line profiles of the nanostructures in the four mesas.

As the InAs deposition amount increases to 2 ML (sample O) which is larger than the standard critical thickness for InAs QDs formation on planar GaAs, arrays of clutters of big dots appear on the surface (Fig. 4.16 (a) – (f)). No dot interstitials are observed on mesas with hole pitch of 250 nm. The densities of dot interstitials for mesas with pitches of 500 nm, 1 μm and 2 μm are 0.64 dots/μm², 2.6 dots/μm², 3.68 dots/μm², respectively. In all the samples, the occupation of each position with multiple dots (2 or 3) are observed. The reason could be from the incompletely infilled nanoholes or the formation of multiple protruded structures formed in the nanoholes during the seeding layer growth, showing that a further growth optimization of the seeding layer is necessary.

250 nm

500 nm

(a)

(b)

0 ▬ 37.2 nm

0 ▬ 31.5 nm

1 μm

2 μm

(c)

(d)

0 ▬ 25.2 nm

0 ▬ 29 nm

1 μm

2 μm

(e)
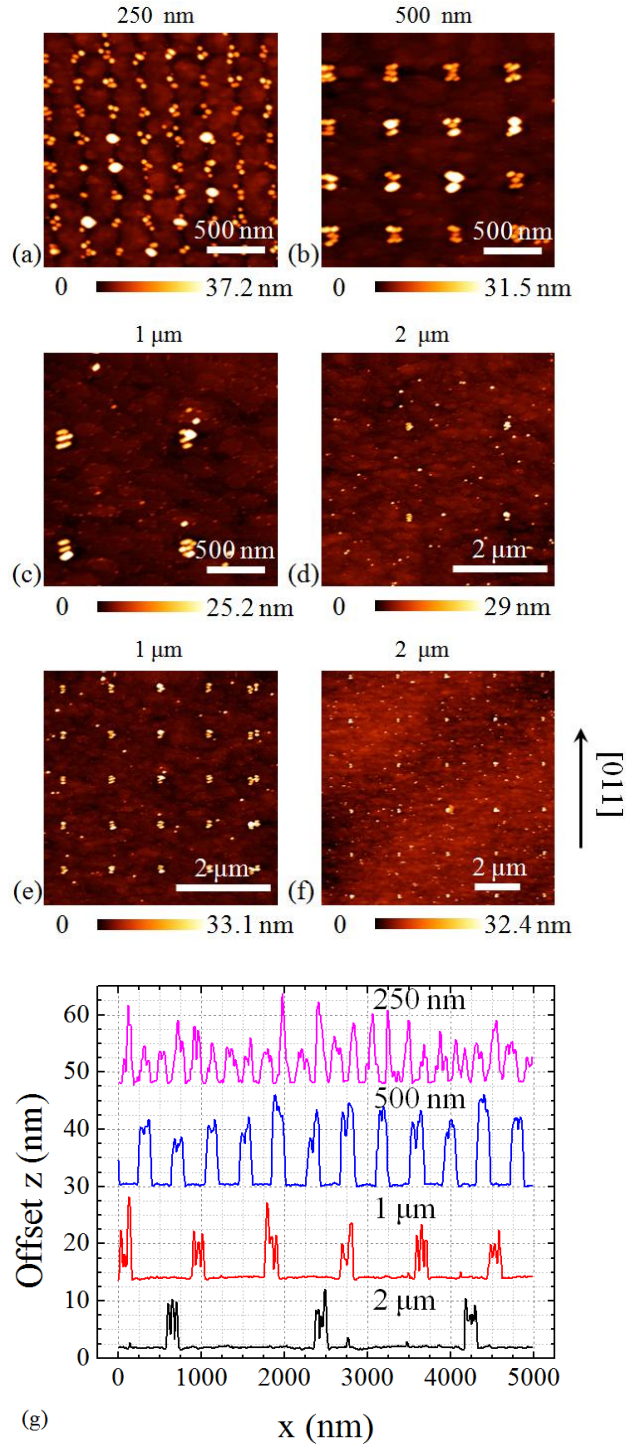
(f)

[1̄10]

0 ▬ 33.1 nm

0 ▬ 32.4 nm

(g)

Fig. 4.16 (a)-(d) AFM images of nanostructures grown on patterned mesas with hole pitches of 250 nm (a), 500 nm (b), 1 μm (c) and 2 μm (d) of sample O. Sample (e) and (f) shows the longer range scan of (c) and (d). (g) is the averaged line profiles of the nanostructures in the four mesas.

4.3 Preliminary investigation on two surface oxide desorption methods

Several samples were grown with the 2nd layer of site-controlled InAs capped by GaAs. However, the PL signal from SCQDs was not observed from those samples during the measurement. Unfortunately, only a few tests were done, due to a long-term instability of the MBE system. Therefore, no conclusive summary could be made.

Two reasons could lead to the degradation of QD PL efficiency: the patterning of the substrate and the HAD process. The first one is well-known to create defects and introduce contaminations at the growth interface. In this work, more effort was dedicated to investigating the influence of the HAD process on the optical quality of the QDs.

Two pieces of samples patterned with mesas were used for the growth. The two samples went through the same processing and chemical cleaning steps. After being loaded to the MBE system, one sample (sample P) was deoxidized with the standard thermal deoxidation (TD) method (T_{sub} = 580 ℃, As background pressure = 1×10^{-6} mbar) in the growth chamber and the other one (sample Q) was deoxidized with the optimized HAD method in the load-lock chamber. Then, 20 nm GaAs was deposited on both samples, followed by a 2.2 ML InAs deposition at the temperature for which $\lambda_T = 1100$ nm. A 30 sec growth interruption carried out at the same substrate temperature was introduced to anneal the dots. After that, a 100 nm-thick GaAs layer was grown to cap the dots. The RT ensemble μ-PL spectra of the two samples are shown in Fig. 4.17. The PL peak intensity of sample P is about one order of magnitude higher than that of the sample Q. This result indicates that some contamination was included during the HAD process.

From the PL point of view, indeed, the TD method provides better PL efficiency of the QDs. However, compared to the smooth surface achieved after the HAD process (Fig. 4.18 (a)), the TD method ends up with a rough surface (Fig. 4.18 (b)) with big pits, due to the consumption of the bulk GaAs material in the chemical reaction which removes the oxide:

$$Ga_2O_3 + 4GaAs \rightarrow 3Ga_2O\uparrow + 2As_2\uparrow \tag{4.2}$$
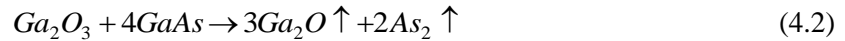
In standard epitaxial growth, the planarity of the surface is recovered by growing a thick (~ 500 nm) GaAs buffer layer. However, this is not applicable in the case of SCQDs growth. Therefore, the TD method is not suitable for being applied to remove the oxide layers on the patterned substrate.

The indium-assisted deoxidation method which will be introduced in Chapter 5 is a suitable method which preserves well the surface and guarantees a good optical quality of QDs.
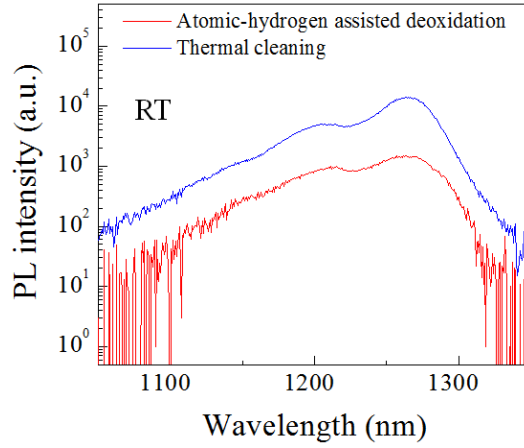
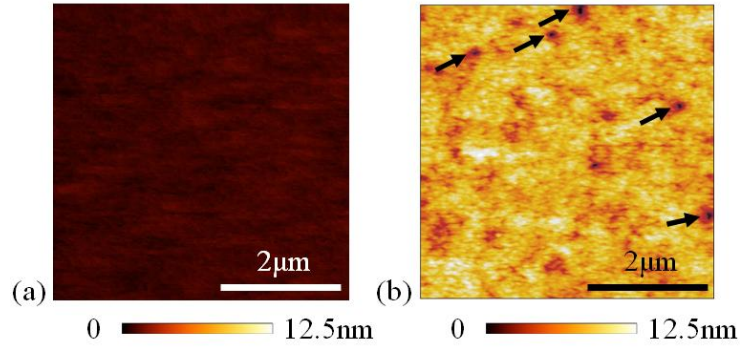Fig. 4.17 The RT ensemble μ-PL spectra of sample P and Q.

Fig. 4.18 AFM images of GaAs epitaxial substrate with native oxide removed by the HAD method (a) and the TD method (b). The black arrows in (b) highlight big pits formed on the GaAs surface after the TD process. The surface roughness rms values of (a) and (b) are 0.17 nm and 1.1 nm, respectively.

4.4 Conclusion

In this chapter, a preliminary study on the growth of low-density site-controlled InAs/GaAs QDs has been done. By optimizing the process flow, nano-holes with sub-100 nm diameter can be patterned on square mesas of GaAs substrates. PL (similar to Fig. 4.17) would have provided for instance additional information. The growth conditions for the deposition of the thin GaAs buffer layer, the InAs seeding layer, and the 2nd layer of InAs QDs have been partially optimized. Based on this, the growth of SCQDs, with multiple dots occupying the same site, has been achieved. However, the PL emission from the SCQDs could not be observed in the measurements. One possible reason could be the possible contamination introduced to GaAs surface during the HAD process. This motivated the investigation of another surface deoxidation method.

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CHAPTER 5

In-assisted deoxidation of GaAs substrates for the growth of single InAs/GaAs quantum dot emitters

In this chapter[*], a systematic study on the method of In-assisted deoxidation (IAD) of planar epitaxial GaAs (100) substrates is reported. In Section 5.1, a preliminary study on the general growth conditions of the IAD method and the general IAD procedures are discussed. In Section 5.2, the investigation of the optimal IAD condition which results in pit-free and smooth GaAs surface is presented. In addition, the results of the PL emission measurements of low-density InAs QDs grown in close proximity to a GaAs surface deoxidized with the IAD method under an optimized condition are discussed.

5.1 Preliminary investigation of the IAD method

As it has been discussed in Chapter 4, the selective removal of surface oxide while preserving delicate nano-patterns on the substrate is essential for the MBE regrowth on nano-patterned GaAs substrate. The conventional thermal deoxidation (TD) method (Fig. 5.1 (a)) results in a rough surface with big pits (Fig. 4.19) and causes damage to the patterned structures. [1] The atomic-hydrogen-assisted deoxidation (HAD) method (Fig. 5.1 (b)), [2],[3] while effective in achieving a pit-free surface, has sets additional hardware requirements on III-V MBE systems and can induce unwanted hydrogen-induced contamination.[4] (Sec. 4.3) The Ga-assisted deoxidation (GAD) method (Fig. 5.1 (c)) [5],[6] enables a thorough native oxide removal with Ga. However, the removal of residual Ga atoms on the surface is difficult due to the high desorption temperature.
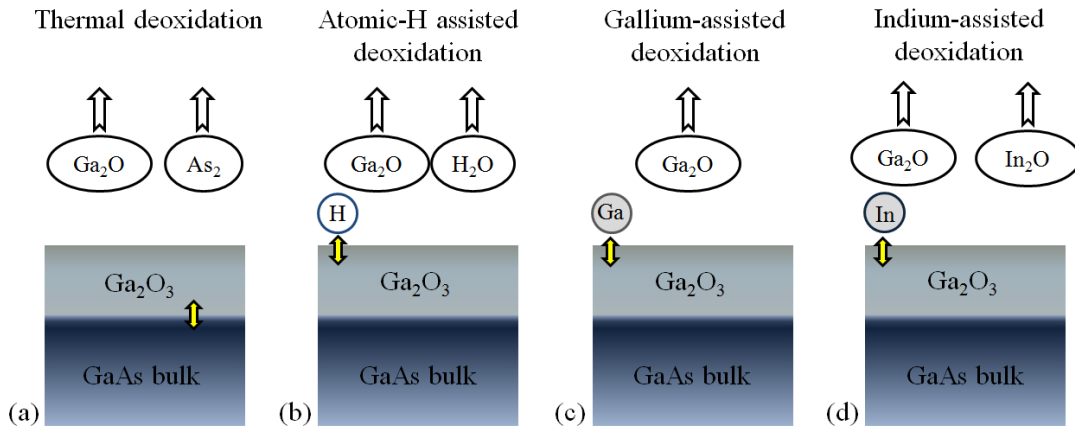

Fig.5.1 Schematic illustration of the principle of the methods of thermal deoxidation (a), atomic-hydrogen assisted deoxidation method, gallium-assisted deoxidation (c), and indium-assisted deoxidation (d).

The In-assisted deoxidation (IAD) method (Fig. 5.1 (d)), recently proposed by Li et al. [7], provides a way to prevent from problems mentioned above. Due to the similar group III nature of In and Ga and lower desorption/decomposition temperature of In/InAs, an In-assisted oxide desorption method can allow removing the native oxide as well as the residual In on the surface.

The principle of the IAD method is based on the chemical reaction: [7]

$$Ga_2O_3 + 4In \rightarrow Ga_2O \uparrow + 2In_2O \uparrow \tag{4.1}$$
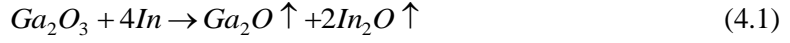
In the first stage of this work, the author investigated the general working condition for the IAD method carried out in the Createc SY022 MBE system.

For the sample preparation, a 500 nm GaAs epitaxial layer was grown on a 2" substrate after the thermal desorption of the oxide layer at 580 ℃. A constant growth rate of ~ 14.3 nm/min was kept and a constant As_4/Ga V/III flux ratio of 12 during the GaAs layer growth. Once unloaded after growth, the epitaxial substrate was exposed to air for 2 days, cleaved into small pieces, which were then stored in a vacuum jar with the pressure below 1×10^{-3} mbar. For individual experiments, a substrate piece was taken out from the vacuum jar and then In-bonded to a sample holder at ~ 200 ℃ and loaded into the MBE system. During these steps fresh oxide films are formed on the GaAs surface.

According to Ref. [7], the IAD method consists of steps of indium flux irradiation, excessive indium desorption and substrate annealing under arsenic overpressure. In the first stage of the experiment, the indium flux irradiation was performed at the substrate temperature of 500℃ with an indium flux (Φ_{In}) of 1.3×10^{-13} cm^{-2}s^{-1}. First, the substrate was gradually heated up to $T_{sub} = 500$ ℃ with a ramping rate of ~ 25 ℃/min under an arsenic background pressure of ~ 1×10^{-9} mbar. Then, the In flux was irradiated to the substrate. In Fig. 5.2, examples of the RHEED patterns of the GaAs surface during indium flux irradiation are given. The gradual increase of the specular spot intensity and the appearance of the diffraction spots with time correspond to the desorption process of the surface oxide.
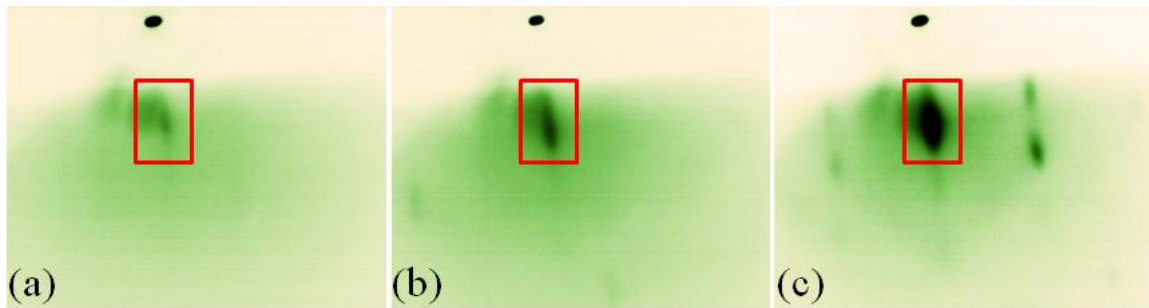

Fig. 5.2 Images of the RHEED patterns of the GaAs surface during the step of the 'indium flux irradiation'. (a) was taken in the beginning of the process. (b) and (c) were taken 1 min and 3 min afterwards. The red square highlights the specular spot. The darkness of the RHEED pattern in the images corresponds to the intensity of the RHEED pattern.

Since it is not possible to evaluate the absolute amount of surface oxide beforehand, an excessive amount of In was provided to the surface. In this case, the RHEED pattern showed an In-rich (4×2) surface reconstruction in the [110] azimuth (Fig. 5.3 (a)). To get rid of the excessive In, the substrate was heated up to a higher temperature (in this case, 20 °C higher than the IAD working temperature) and annealed at this temperature to break the atomic bonds between In and As atoms on the surface. In the RHEED pattern, this process is represented by the gradual disappearance of the non-integral patterns with time. (Fig. 5.3 (b), (c))
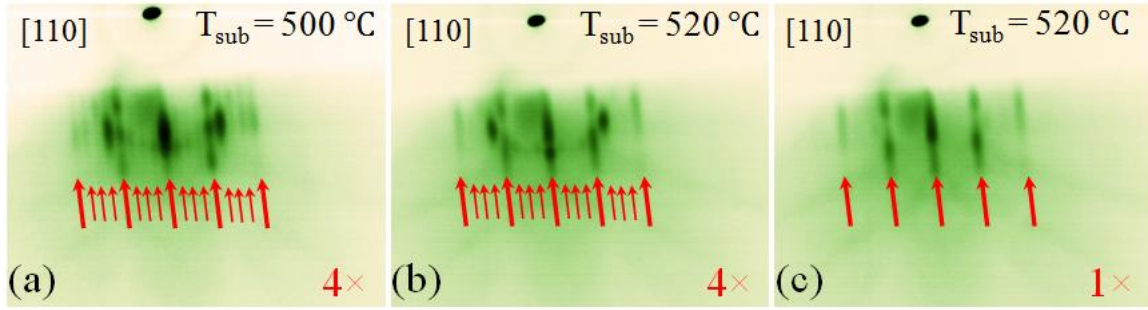
Fig. 5.3 Images of RHEED patterns of the GaAs surface in the [110] azimuth during the step of 'excessive indium desorption'. (a) was taken at T_{sub}=500 °C. (b) and (c) was taken 1 and 3 minutes afterwards at T_{sub}=520 °C. Bold (narrow) arrows indicate the position of integral (non-integral) RHEED patterns. The darkness of the RHEED patterns in the images corresponds to the intensity of the RHEED pattern.

To recover an arsenic rich surface, As_4 was provided to reach a background pressure of ~ 1×10^{-6} mbar. Under this condition, developed $2 \times$ and $4 \times$ surface reconstruction RHEED patterns appeared in the [110] and [1-10] azimuth. (Fig. 5.4) The sample (denoted as sample C) was cooled down immediately and unloaded for AFM investigation. No big pits were found on the GaAs surface after IAD. (Fig, 5.5 (a)) The averaged surface roughness root mean square (RMS) value of a 5×5 area on the surface is ~ 0.58 nm, which is about half of the value of the surface treated with the TD method (RMS ~ 1.12 nm). (Fig. 5.5 (b))
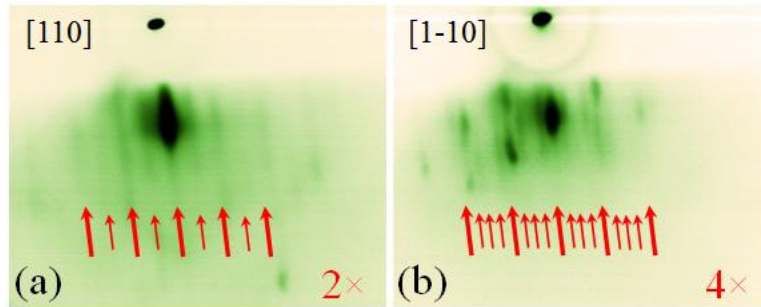

Fig. 5.4 Images of RHEED patterns of the GaAs surface in the [110] (a) and [1-10] (b) azimuth during the step of substrate annealing under arsenic overpressure at T_{sub}= 520 °C. Bold (narrow) arrows indicate the position of integral (non-integral) RHEED patterns. The darkness of the RHEED patterns in the images corresponds to the intensity of the RHEED pattern.

In addition, it was found during the experiment that applying an HCl treatment to the substrate prior to mounting it to the Molybdenum holder helped to improve the surface smoothness after the oxide desorption process. (Fig. 5.5 (b)) Tentatively, the reason comes from the reduction of the amount of native oxide to be removed in the growth chamber. Therefore, in the growth of subsequent samples, the steps of dipping the substrate for 1 min in the HCl (30%): H_2O (1:1) solution, followed by a 5 min rinse in distilled water, were added.
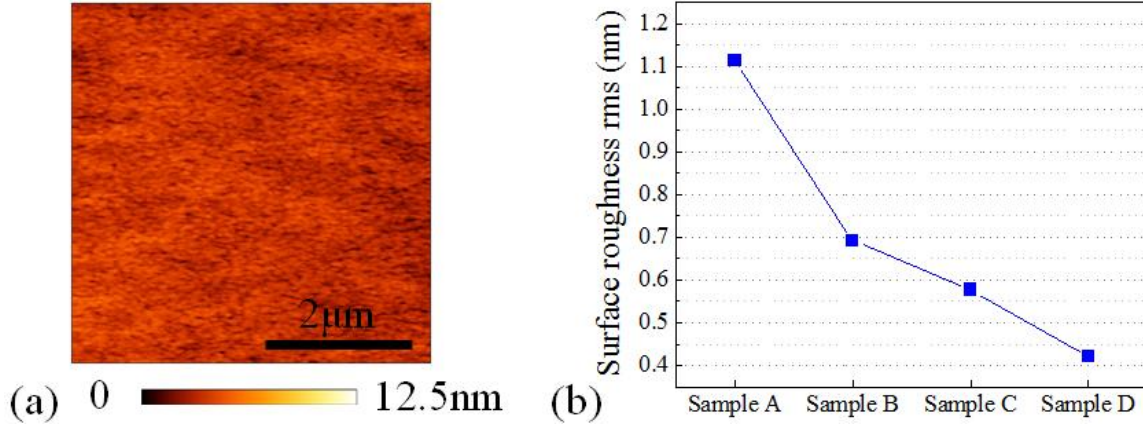
Fig. 5.5 (a) AFM image of the GaAs surface of sample C after the IAD process. (b) Comparison of the surface roughness RMS values of samples after different oxide desorption processes. Samples A and B are deoxidized with the TD method, while for samples C and D, the IAD method was used. For sample B and D, the steps of dipping the sample for 1 min in the HCl: H_2O (1:1) solution, followed by a 5 min rinse in the distilled water, were carried out before mounting them to the holders with In.

5.2 Growth condition optimization of the IAD method

The surface roughness is a key parameter for the growth of low-density and site-controlled QDs because in these cases a large diffusion length of the adatoms is typically needed. Since a residue RMS surface roughness of ~ 0.4 nm (similar to the best reported result) still exists after the IAD process, and very few applications of this method have been reported so far, the author performed a systematic study on the IAD method in collaboration with Dr. Yongjin Cho.

After the work described in Section 5.1 was carried out, the MBE system went through a long period of maintenance and the condition of the MBE growth chamber was changed as a result. Therefore, for the work described in this section, the author started from slightly different working situations for the IAD process.

5.2.1 Experimental Approach

The sample preparation process was the same as what has been described in Section 5.1. In order to study the effects of substrate temperature (T_S) and impinging In flux Φ_{In} on the In-assisted oxide desorption of the GaAs substrate, two groups of samples were prepared. For group A, the surface oxide was desorbed under a constant Φ_{In} of 8×10^{12} $cm^{-2}s^{-1}$ at three different T_S. For group B, T_S was maintained at 525 °C and Φ_{In} was varied from 8×10^{12} to 3.7×10^{13} $cm^{-2}s^{-1}$.

Due to a block of one MBE viewport from which the light from the wide-band lamp can shine in, the Bandit system was not able to work in its regular mode to determine the substrate temperature from the absorption edge in the spectra of the diffusively scattered light. The substrate temperature was therefore measured by the Bandit system working in the pyrometer mode. The GaAs surface change during the oxide desorption process was monitored by the RHEED. The In flux was continuously provided to the surface until the appearance of the In-rich (4×2) surface reconstruction [7]. Different from the way of thermal desorption at high temperature (Section 5.1), the excessive In on the surface was immediately converted into InAs by exposing the surface to As_4 with a beam equivalent pressure (BEP) of 6×10^{-6} mbar, and then the InAs was decomposed while increasing T_S to 580 ℃ with a ramp rate of 30 ℃/min under the As pressure.

The sample was either unloaded for studying the surface morphology by atomic force microscopy (AFM) or kept at 580 ℃ for further growth. In the latter case, a 10 nm-thick GaAs buffer layer was grown. The thickness was chosen to be similar to that of the buffer layer typically used in the SCQDs growth.[8] Then, the sample was cooled down to 505 ℃ and two monolayers (MLs) of InAs were deposited at a growth rate of 0.0014 ML/min to form low-density InAs QDs[9]. Following a 30 s annealing, the sample was either cooled down immediately for AFM study, or capped by 5 nm $In_{0.2}Ga_{0.8}As$ followed by 100 nm GaAs for photoluminescence (PL) study.

In order to compare the PL properties of these QDs with those of InAs QDs grown in a conventional way, a control sample was grown, containing 2.0 ML InAs low-density QDs capped by a 100 nm GaAs layer grown on 500 nm GaAs buffer deposited onto GaAs substrate deoxidized by conventional thermal desorption. The PL measurements were carried out in a μ-PL system with a microscope objective (N.A. = 0.5) and dispersed by a 1 m monochromator to an InGaAs photodiode array (IGA300 HORIBA Jobin-Ynvon) with a spectral resolution better than 0.04 nm. A 780 nm cw diode laser was used as the excitation source. In order to explore the decay dynamics of excitons confined in the QDs, time-resolved PL measurements were performed using a pulsed diode laser as an excitation source (λ = 757 nm, pulse width $\approx$ 70 ps, repetition rate = 40 MHz, spot diameter $\approx$ 4 μm), a commercial SCONTEL superconducting single-photon detector (SSPD) and a correlation card.

5.2.2 Influence of T_S during IAD on surface morphology

Figure 5.6 shows the AFM results of three samples for which the surface oxide was removed under a constant Φ_{In} of 8×10^{12} cm^{-2}s^{-1} at T_S = 500, 525, and 545 ℃ (group A). Each RMS roughness was calculated based on the average of three RMS values taken at three different positions on the sample [Fig. 5.6 (a)]. At T_S = 525 ℃, the surface RMS roughness has the lowest value of ~ 0.26 nm , which is about 1.5 times lower than the previous result achieved by Li et al.[7] and is close to the RMS roughness value (~ 0.2 nm) of epitaxial GaAs surfaces. The RMS roughness is increased to ~ 0.35 nm, and ~ 0.4 nm for T_S = 500 and 545 ℃, respectively. For the case of T_S = 500 ℃, the difference between the two RMS roughness values in 2×2 μm^2 and 5×5 μm^2 areas is relatively larger compared to the cases of the other two samples, which implies that the T_S = 500 ℃ sample has relatively inhomogeneous surface morphology. In addition, compared to the T_S = 525 ℃ sample, the T_S = 500 and 545 ℃ samples are characterized by pronounced surface pits [Fig. 5.6 (b)]. Although these surface pits observed for T_S = 500 and

545 ℃ look similar, their origins are believed to be different. For the case of T_S = 500 ℃, the surface activation energy [7] for the oxide desorption reaction by In is so high that the complete oxide desorption process takes a long time. As a result, significant amounts of extra In atoms accumulate and form local In droplets on the surface. The pits formed at T_S = 500 ℃ are therefore believed to be due to local In droplet etching [10]-[12]. The origin of this effect will be discussed in detail in 5.2.3 below. For the case of T_S = 545 ℃, on the other hand, the substrate temperature is high enough to initiate the thermal desorption process, and both In-assisted and thermal desorption processes contribute to the oxide removal process at this temperature. Thus, the formation of the pits at this temperature is due to the thermal-desorption-induced roughening effect.
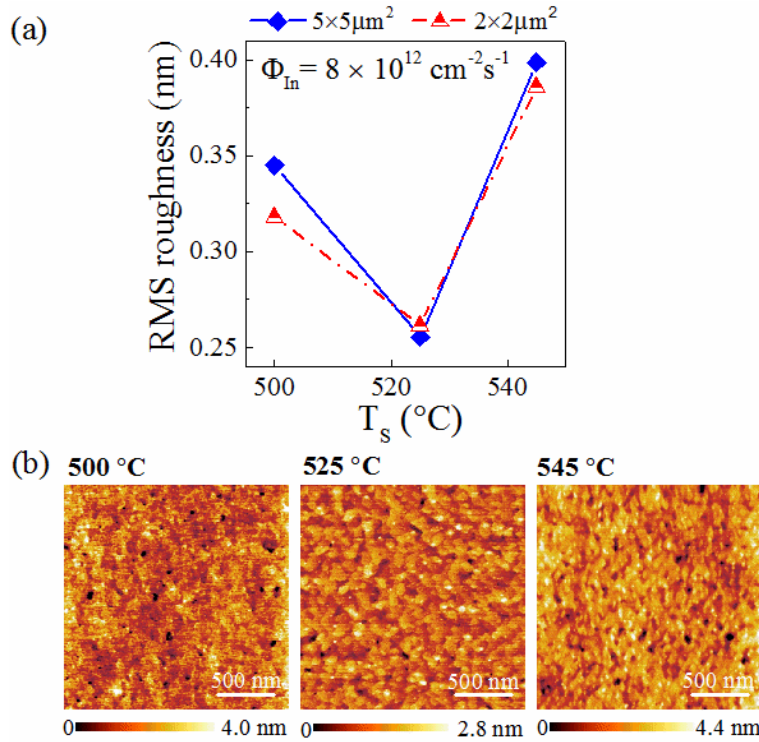
Fig. 5.6 (a) Root-mean-square roughness and (b) 2×2 μm^2 AFM micrographs of GaAs surface deoxidized by a constant In flux of 8×10^{12} $cm^{-2}s^{-1}$ at different substrate temperatures.

5.2.3 Influence of Φ_{In} on surface morphology

Fig. 5.7(a) shows the RMS roughness of GaAs substrates where surface oxides were removed under different Φ_{In} at T_S = 525 ℃ (group B). In IAD conditions with Φ_{In} varying from 8×10^{12} to 2.5×10^{13} $cm^{-2}s^{-1}$, the average RMS roughness amounts to $0.21 - 0.3$ nm. For $\Phi_{In} = 3.7 \times 10^{13}$ $cm^{-2}s^{-1}$, on the other hand, the RMS roughness value measured on 2×2 μm^2 and 5×5 μm^2 areas show a sharp contrast: an AFM image measured on a 5×5 μm^2 area reveals big holes with a density of 0.12 holes/μm^2 [Fig. 5.7(b)]. However, the RMS value measured on a 2×2 μm^2 area

that does not contain such a big hole remains at ~ 0.21 nm which is close to the RMS values of the samples deoxidized with lower Φ_{In}.
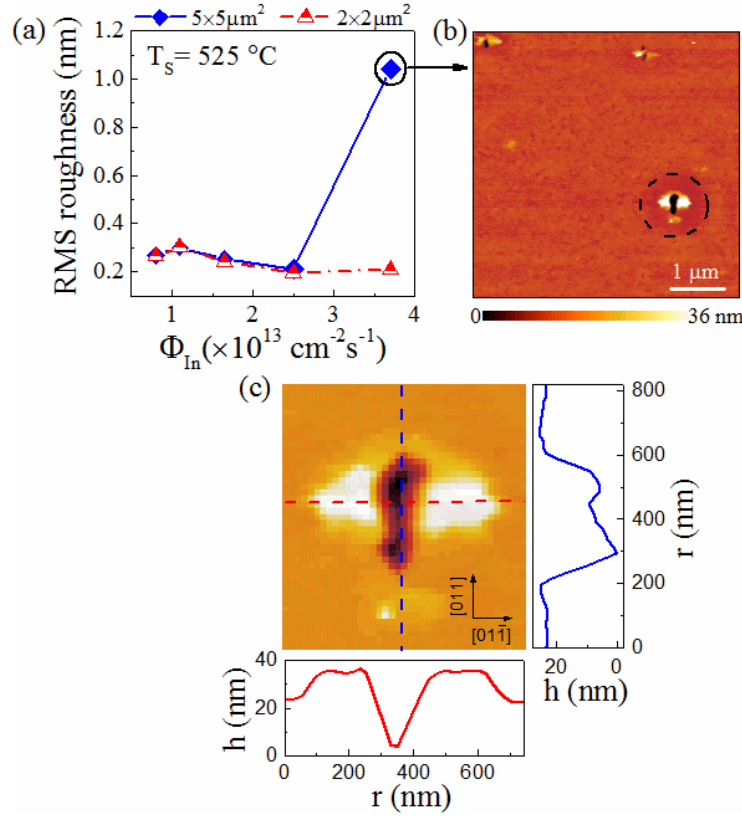

Fig. 5.7 (a) Root-mean-square roughness of GaAs surface deoxidized by different In fluxes at a substrate temperature of 525 °C. (b) 5 × 5 µm² AFM micrograph of the GaAs surface deoxidized by an In flux of 3.7 × 10^{13} cm⁻²s⁻¹. The dashed-circle area in (b) is magnified in (c), where two surface line profiles (surface height h with respect to position r) in the [011] and [01-1] directions are also plotted.

Interestingly, the defects are seen to have a uniform shape: the holes are elongated along the [011] direction and mounds are formed on both sides of the holes along the [01-1] direction. [e.g., see Fig. 5.7 (c)] The origin of the formation of nanoholes is attributed to the local In droplet etching effect[10]-[12] that takes place during the IAD process: At high Φ_{In} and moderate T_S = 525 °C, the deposition rate of In is much higher than the sum of the evaporation and consumption rate in the oxide desorption process. Under this condition, excessive In atoms are accumulated and eventually large In droplets are formed on the surface. Since GaAs is unstable against In droplets under As-free conditions, local droplet etching is expected in this case. And indeed, the characteristic shape of the nano holes is consistent with the typical shape observed in the presence of local droplet etching. [10]-[12] This consideration was the reason for our choice to provide an As overpressure to convert the excessive In into InAs, and then decompose the InAs at elevated temperature.

5.2.4 QDs grown in close proximity to IAD-cleaned GaAs surface

From the systematic study on the In-assisted oxide desorption mentioned in the previous section, it can be concluded that in order to get a smooth surface the In-assisted desorption should be performed with a minimum In flux (to avoid the formation of In droplets) and at a relatively low substrate temperature (not to activate thermal desorption).

Using an optimal IAD condition (T_S = 525 °C and Φ_{In} = 2.5 × 10^{13} $cm^{-2}s^{-1}$), low-density InAs QDs were grown. Fig. 5.8 (a) displays the RHEED pattern of a 10 nm thick GaAs buffer layer along the [01-1] azimuth just before the growth of the InAs QDs. A very clear c(4 × 4) surface reconstruction of As-rich GaAs surface is observed on the perimeters of Laue circles, which implies that the GaAs surface is very flat and smooth in a wide range.
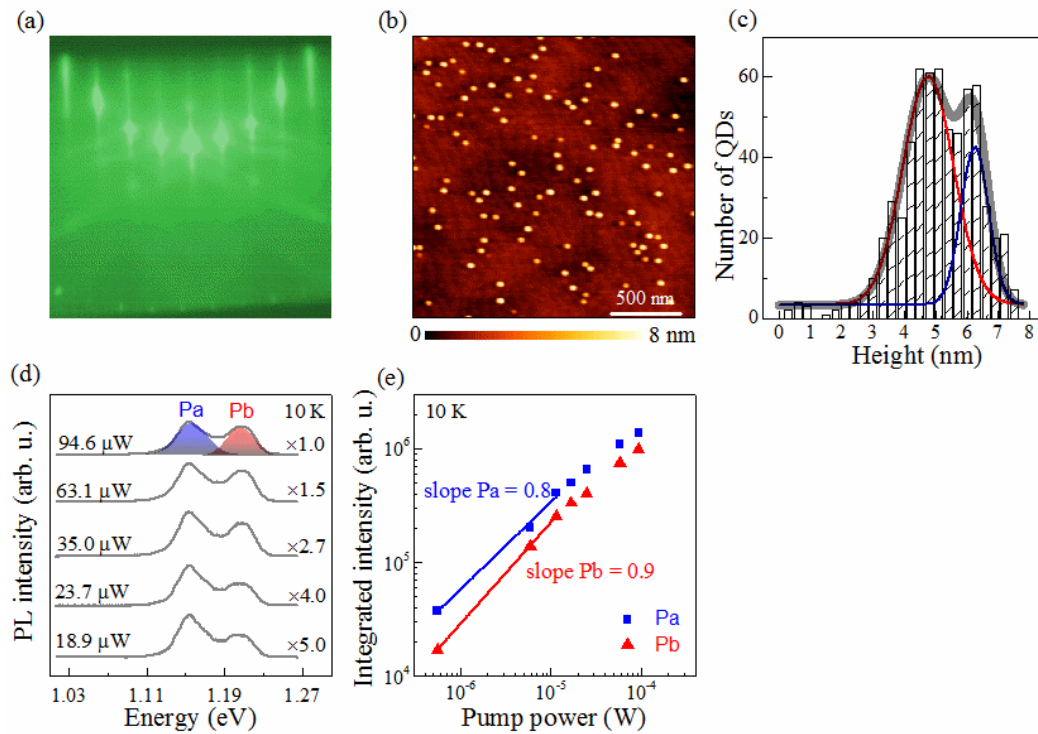
Fig. 5.8 (a) RHEED pattern of a 10 nm thick GaAs buffer grown on GaAs surface deoxidized by In. (b) 2 × 2 μm² AFM micrograph of low-density InAs QDs grown on top. (c) Height distribution of the InAs QDs fitted with two Gaussian peaks. (d) PL spectra of capped InAs QDs at different excitation powers taken at 10 K. (e) Integrated PL intensities of the peaks *Pa* and *Pb* in (d) as a function of average excitation power.

Fig. 5.8 (b) shows an AFM image of uncapped low-density InAs QDs grown 10 nm above the IAD cleaned GaAs surface. QDs with a density of 4 × 10^9/cm² distribute uniformly along the step edges. The statistical analysis on the QDs size suggests a bimodal distribution [Fig. 5.8 (c)]. QD samples grown under similar conditions on standard thermally-deoxidized substrates with thick buffer layers do not show this bimodal distribution, which was instead observed in all IAD-cleaned samples with thin GaAs buffer layers.

Although the reason for the bimodal distribution is currently unclear, the origin is not likely to be related to the cleaning method itself, but rather to the kinetics of the adatoms forming the QDs. As the GaAs buffer layer gets thinner, the QDs are more vulnerable to impurities on the surface of the substrate. For the case of the IAD samples with thin buffer layers, the adatom kinetics in the mass exchange between the QDs is presumably affected by the contaminants on the substrate surface and therefore the formation of a uniform QD size distribution is likely kinetically hindered by these impurities.

The PL from capped InAs QDs as a function of the excitation power was then investigated. The PL spectra obtained at 10 K are shown in Fig. 5.8 (d). All the spectra can be fitted with two Gaussian peaks located at 1.18 eV (denoted by peak Pa) and 1.22 eV (denoted by Pb). The energy difference between the two peaks is ~ 40 meV, which is about half of the typical energy separation between the ground state and the first excited state of single QDs grown in these conditions on the thermally-deoxidized substrate with thick buffer layers.[9] In addition, both peaks grow linearly with the increasing excitation power. Fig. 5.8 (e) shows the integrated PL intensities of the peaks Pa and Pb as a function of the excitation power on a log-log scale. A linear fit of the data in the low pumping power regime (far from being saturated) gives slopes close to 1 for the both peaks. [see Fig. 5.8(c)] Thus, we attribute the two peaks to the ground-state excitonic emissions of the two families of the QDs. [13], [14]

Time-resolved PL measurements were also performed at 10 K to study the dynamics of the exciton relaxation in the QDs. [Fig. 5.9 (a)] A long-pass filter with a cut-off at 1.18 eV was used to filter out the emission from the ground state of the bigger dots. The decay time of the bigger dot ensemble is ~ 0.8 ns. For comparison, we also measured the time-resolved PL from the control sample. The decay time of the control sample is ≈ 0.9 ns. The difference between the two decay times is within the jitter of the setup and the fitting error. The fact that QDs grown at 10 nm distance from an IAD cleaned surface have similar lifetime as the control QDs indicates the absence of nonradiative defects inside the QDs and therefore the high crystalline quality.

Figure 5.9 (b) shows μ-PL spectra taken on the IAD sample at lower excitation power (780 nm laser, 1.91 μW) at 10 K, featuring sharp single QD PL lines. This suggests the first observation of single-QD PL from QDs grown in close proximity to surfaces deoxidized with the IAD method. It is therefore an important indication of IAD for application to SCQDs growth. Linewidths in the range of 250−400 μeV are typically observed [see the inset of Fig. 5.9 (b)], ~ 4 times broader than that of the control sample. Although the origin of the relatively broader PL line is currently not clear, this might be due to the spectral diffusion [15] induced by contaminants such as carbon at the air-exposed surface. Similar to the case of SCQD growth, the QD-stacking technique can be used to further reduce the linewidth of QDs by increasing the distance between the contaminated interface and the optically-active QDs. [8]
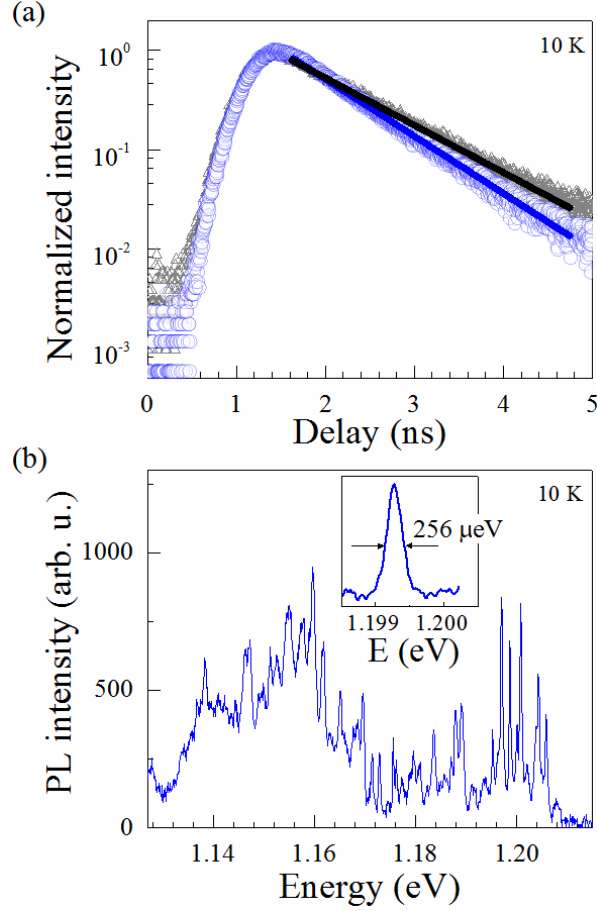
Fig. 5.9 (a) Time-resolved PL of low-density InAs QDs samples, whose substrate surface oxides were removed by In-assisted (blue circles) and thermal deoxidation (grey triangles). Their decay times were estimated with fits (solid lines). (b) 10 K micro-PL spectrum of single quantum dots grown at 10 nm from GaAs surface deoxidized with the IAD method. The inset shows a zoom of a typical single QD PL emission of the main panel with a linewidth of 0.22 nm (256 μeV).

5.3 Conclusion

In this chapter, the In-assisted deoxidation of GaAs surfaces has been systematically studied, and its application to producing low-density InAs QDs with good optical qualities has been demonstrated. Within a large parameter window, thermal desorption and the formation of In droplets can be avoided, resulting in atomically smooth oxide-free GaAs surface. Sharp excitonic PL lines are observed from InAs QDs grown in close proximity (10 nm) to a GaAs surface from which the oxide layer was removed with In. The decay time of the QD ensemble PL is similar to that of regular QDs grown on thick GaAs buffer layers. The IAD method has a very promising application in circumstances which require the growth of nanostructures close to a patterned GaAs surface, and particularly for the realization of high-quality SCQDs.

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CHAPTER 6

Fabrication of vertically-coupled photonic crystal nanobeams

The research field of optomechanics investigates the interaction between the light field and the mechanical motion of objects. The nano-opto-mechanical system (NOMS) device with the double-slab structure is expected to show a very strong optomechanical coupling because of its small mass, small dimensions, and high mechanical and optical quality factors. In this chapter, the fabrication of a NOMS device with vertically-aligned double photonic crystal nanobeams is presented. In Section 6.1, the sample structure and the general fabrication process of the device is introduced. In Section 6.2, the buckling problem of the device will be discussed and analyzed by simulation. In Section 6.3, the experimental demonstration of the NOMS device with stress releasing structures is shown.

6.1 Fabrication of the NOMS devices

In Chapter 5 of Ref. [1], a method of fabricating the vertically-aligned nanobeams has already been presented. The work described in this section followed a similar approach in the fabrication of the device. However, due to the problem related to the etching of the $Al_{0.7}Ga_{0.3}As$ sacrificial layer (to be discussed in more detail in Chapter 7), the Al concentration in the AlGasAs sacrificial layer was increased from 70% to 79%. Therefore, the whole fabrication process of the device had to be changed and re-optimized.

6.1.1 Sample structure

The sample used in the fabrication was grown at Nanolab @ TU/e by Yongjin Cho, Frank van Otten, and Tian Xia. The structure of the sample is shown in Table 6.1.

Table 6.1 Sample structure for fabricating the NOMS device

Material	Thickness	Doping (cm^{-3})	*Comments*
Air			
GaAs	90 nm	undoped	*Upper Slab*
$In_{0.2}Ga_{0.8}As$	5nm	undoped	
InAs QDs	~ 2 ML InAs	undoped	
GaAs	90 nm	undoped	
$Al_{0.79}Ga_{0.21}As$	240 nm	undoped	*Sacrificial Layer 2*
GaAs	170 nm	undoped	*Lower Slab*
$Al_{0.79}Ga_{0.21}As$	1500 nm	undoped	*Sacrificial Layer 1*
GaAs epitaxial layer	500 nm	undoped	*Buffer Layer*
GaAs (100) SI substrate	350 μm		

The room temperature (RT) μ-PL spectrum of the sample is shown in Fig. 6.1, featuring the usual structure with several peaks coming from the different electronic transitions in the QDs, WL and bulk GaAs.
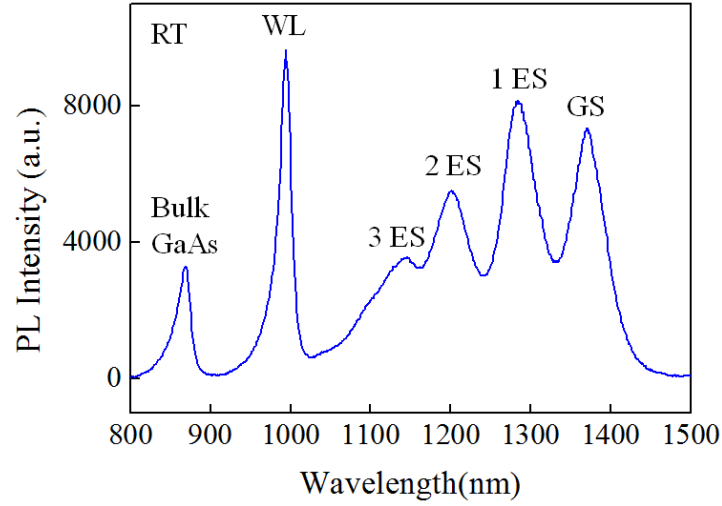
Fig. 6.1 RT μ-PL spectra of the sample used for the fabrication of the double nanobeams NOMS device.

6.1.2 Design and general process flow of the NOMS device

In this work, the NOMS device was designed by Leonardo Midolo and Tian Xia. Fig. 6.2 shows the design of the device with the parameters illustrated in Table 6.2. The PCC cavity is created by shifting two holes in a 1D periodic array. In the EBL mask, an array of the NOMS devices with different lattice parameters (from 360 nm to 530 nm), nanobeam lengths (from L_1 to L_6), and nanobeam widths (from W_1 to W_3) are included (with fixed number of holes).
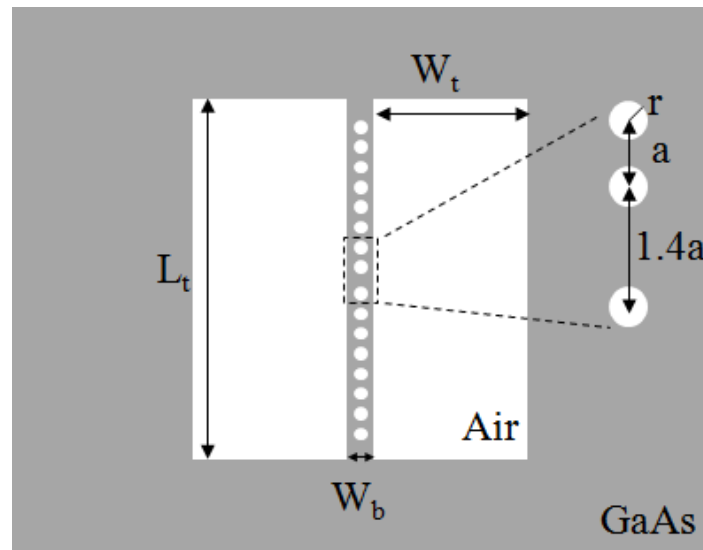
Fig. 6.2 Schematic illustration of the initial design of the nanobeams.

Table 6.2 Illustration of parameters in Fig. 6.2

Symbol	Parameter	Comments
a	Lattice constant	From 360 nm to 530 nm in step of 5 nm
r	Hole radius	0.28a
s	Cavity spacing	1.4a
L_t	Trench length	$L_1=((7a+r)*2+1.4a)+a$; $L_2=L_1+a$; $L_3=L_1+2a$; …; $L_6=L_1+5a$
W_b	Nanobeam width	$W_1=1.19a$, $W_2=1.43a$, $W_3=1.55a$
W_t	Trench width	3.75 μm

The major steps for the fabrication of the device are shown as follows:

➢ Etching of the PCCs and trenches (Fig. 6.3)
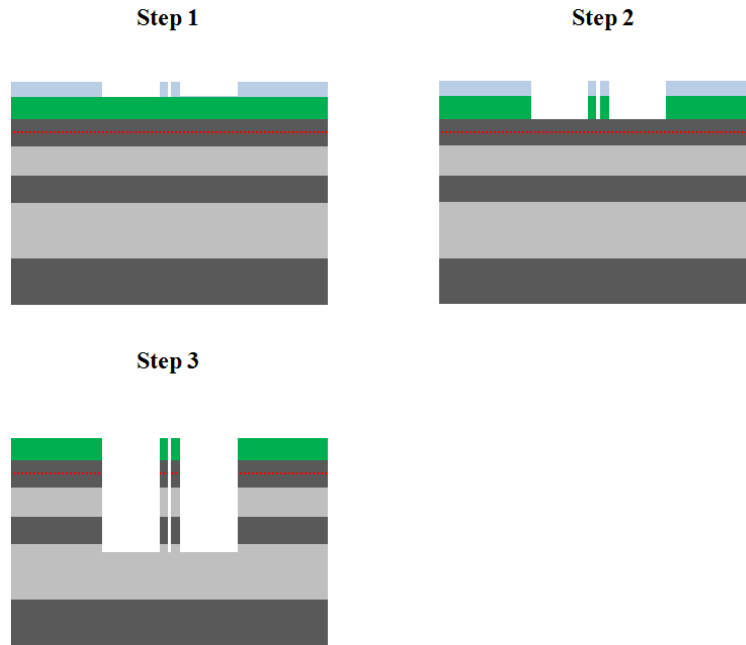
Fig. 6.3 Schematic illustration of the etching of PCCs and trenches. (Step 1-3)

Step 1: Definition of the PCCs and trenches with EBL.

Step 2: Etching of the ~ 400 nm thick SiN hard mask by the CHF_3 RIE. After this step, the ZEP 520A resist was removed by O_2 plasma stripping.

Step 3: Transferring of patterns from the SiN hard mask to the substrate with the Cl_2/N_2 ICP-RIE @ 200 ℃.

➢ Releasing of vertically-aligned double nanobeams (Fig. 6.4)

Step 4

Step 5

Step 6

Step 7
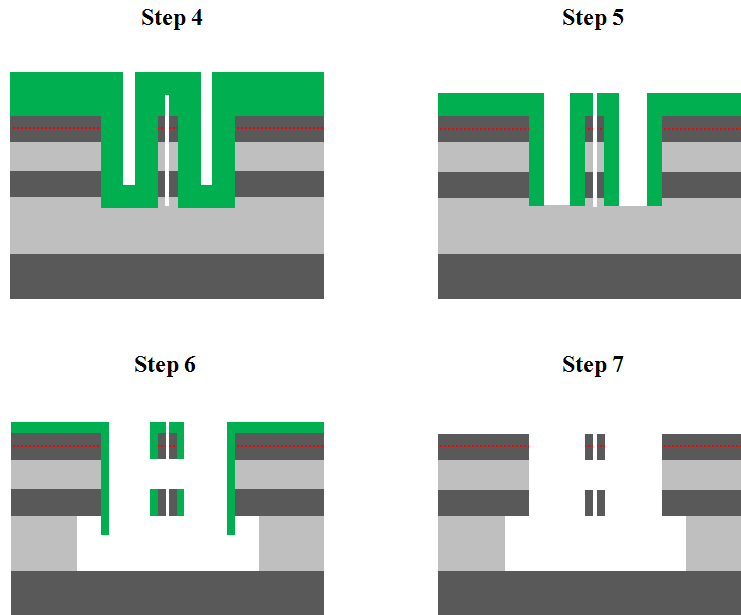
Fig. 6.4 Schematic illustration of the releasing of the vertically aligned nanobeams. (Step 4-7)

Step 4: Growth of a 600 nm thick SiN on the sample with PECVD. [1]

Step 5: Partially etching of the SiN by CHF_3/O_2 RIE to expose the holes on the original SiN hard mask and the surface of the bottom sacrificial layer in the trench area.

Step 6: Releasing of the vertically-aligned nanobeams by etching with HF 10% for 20 sec, followed by a 1 minute IPA hot bath @ 85 ℃. The HF 10% solution etches the inter-membrane and the bottom AlGaAs sacrificial layers through the openings of PCC-holes in the SiN mask and the openings in the trench areas. HF 10% also removes partially the SiN hard mask with an etching rate of 4 nm/s.

Step 7: Removal of the SiN hard mask in the barrel etcher with the recipe of O_2 plasma stripping for 10 minute followed by 3 minute CF_4 plasma etch. The 3 inch metal cage was used to hold the sample in the barrel etcher. The purpose of the O_2 plasma stripping process is to increase the substrate temperature to facilitate the reaction between the CF_4 plasma and the SiN.

6.2 Problems with the buckling and solutions

6.2.1 Problems with buckling of the nanobeams

Fig. 6.5 gives an SEM image as an example of NOEMS devices fabricated following the procedures described in Section 6.1. Both the upper and lower beams buckled heavily after the processing.
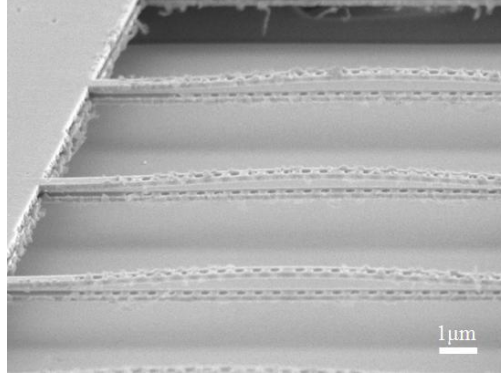
Fig. 6.5 SEM image of as-processed buckled nanobeams.

Actually, the case of the buckling of the long and thin nanobeams is very similar to the case of the buckling of an elastic stick with two ends subject to a compressive force and applied to it from the ends. (Fig. 6.6)
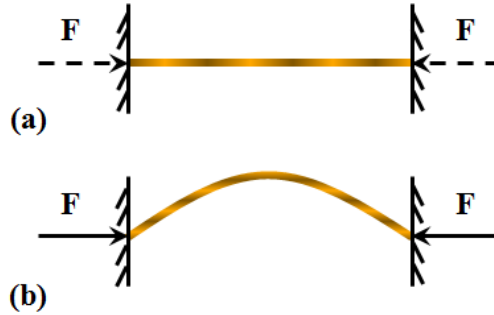
Fig. 6.6 Schematic illustration of the buckling of an elastic stick with two ends fixed subject to a force F.

In Ref. [2], similar examples of buckling of suspended micromembranes due to the internal stress in the material after the releasing of the suspended membranes are reported. The proposed solution is to introduce additional structures to release the stress.

According to Ref. [2], the nanobeams buckle when the stress σ_0 is larger than the critical buckling stress $\sigma_c = \frac{\pi}{3} E (\frac{t}{l})^2$, or equivalently the length of the beam l is longer than the critical buckling length $l_c = t \sqrt{\frac{\pi E}{3\sigma_0}}$, where E is the Young's modulus of the material (i.e. GaAs, with E = 85.5 GPa), t is the thickness of the beam (i.e. the thickness of the upper/lower membrane).

6.2.2 Solutions to the bucking problem

To solve the problem with buckling, first, the value of the residue internal stress needs to be estimated. To do this, a sample was fabricated, containing nanobeams (without PCCs) with gradually changed beam length. By checking the length of the beam from which the buckling

starts to happen, the critical buckling length l_c and the critical buckling stress σ_c can be determined. Fig. 6.7 shows an SEM image of a series of nanobeams, with lengths of 6, 7, 8, 9, 10, 12 μm. It is clear to see that from 9 μm the nanobeam starts to buckle. Therefore, 8 μm was taken as the critical buckling length l_c of the nanobeams. Accordingly, the estimated critical buckling stress σ_c is 140 MPa.

Then, the value of σ_c was taken to the finite element method (FEM) modeling (with Comsol Multiphysics 4.3a) to simulate and to analyze the structure mechanics problems of the NOMS device. With the Comsol software, the geometry of the nanobeams structure can be reconstructed. By defining the surface from which the stress is applied (defined as positive in the case of tensile stress and negative in the case of compressive stress) and the sign and value of the internal stress ('+' corresponds to tensile stress, '-' corresponds to compressive stress), the likeliness of buckling of the device structure under certain internal stress σ_c can be predicted.
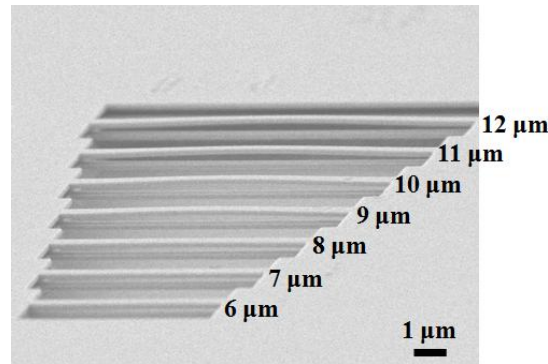
Fig. 6.7 Nanobeams with no PCCs with length varied from 6 to 12 μm.

The occurrence of buckling is indicated by the value of the buckling 'critical load factor' [5] (denoted as BLF) given as an output of the Comsol Simulation. BLF is the ratio of the buckling loads to the currently applied loads (i.e. the internal stress σ_c). The interpretation of BLF is given in Table 6.3.

Table 6.3 Interpretation of BLF [5]

BLF Value	Buckling Status	Remarks
>1	Buckling not predicted	The applied loads are less than the estimated critical loads.
= 1	Buckling predicted	The applied loads are exactly equal to the critical loads. Buckling is expected.
< 1	Buckling predicted	The applied loads exceed the estimated critical loads. Buckling will occur.
-1 < BLF < 0	Bucklin possible	Buckling is predicted if you reverse the load directions.
-1	Buckling possible	Buckling is expected if you reverse the load directions.
< -1	Buckling not predicted	The applied loads are less than the estimated critical loads, even if you reverse their directions.

With Comsol, it is convenient to design devices with different geometries and perform simulations to calculate the BLF value of the device for a certain geometry. In order to release the

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stress in the nanobeams, two supporting beams were added to the design to 'guide' the stress from directly exerting from the two ends of the nanobeams to exerting only from the fixed ends of the supporting beams. (Fig. 6.8) In this case, buckling will only happen on the supporting beams rather than the major nanobeams.

By manipulating the length and the width of the supporting beam, comparing the resulting BLF value for each geometry and the geometry of each buckled mode, the length of 5 to 6 μm and width of 0.4 μm was obtained as the optimized size for the major nanobeams with the length of 12 μm.

Fig. 6.8 Schematic illustration of the force exerted from the fixed ends of the supporting beams to the structure.

Fig. 6.9 shows the calculation result of the Comsol simulation, including the BLF value of 3.41 for this structure, and the geometrical illustration of the first buckled mode.
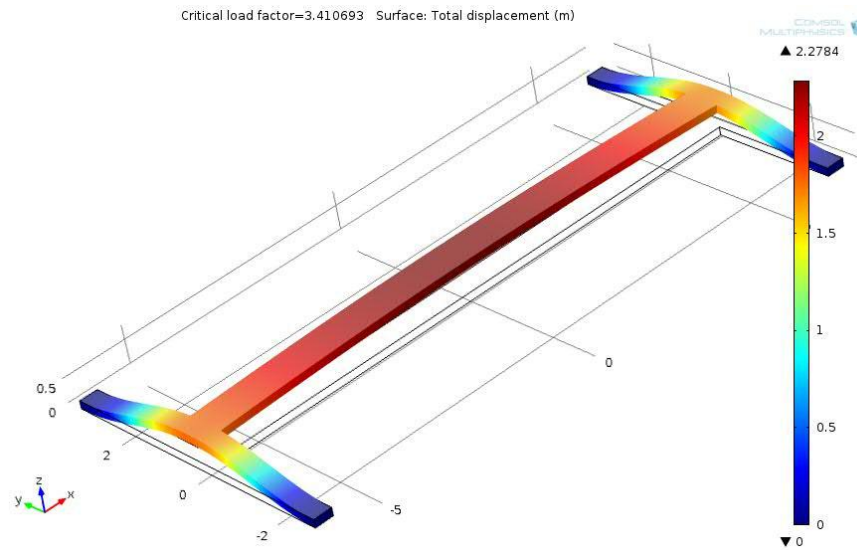
Fig. 6.9 Results of Comsol simulation for the structure with supporting beam length of 6 μm, supporting beam width of 0.4 μm, major beam length of 12 μm, and the thickness of the beams of 0.17 μm. The shape of the structure corresponds to the geometry of the device under the 1st buckled mode. The color bar indicates the deformation of the structures in the vertical direction. The unit of the values in the scale bar equals 0.1 μm.

The Comsol design was realized in the fabrication of new devices. After processing, all the nanobeams stay unbuckled for designed beam lengths from 7.54 to 13.35 µm. (Fig. 6.10) This means the stress-releasing structure works.
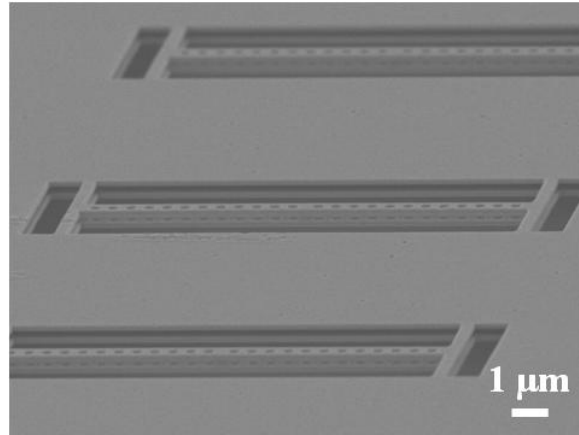
Fig. 6.10 SEM image of as-fabricated nanobeams with stress-releasing structures. The length of the major nanobeams is 13.35 µm.

As it is shown in Fig. 6.11 some defects exist on the sample surface.
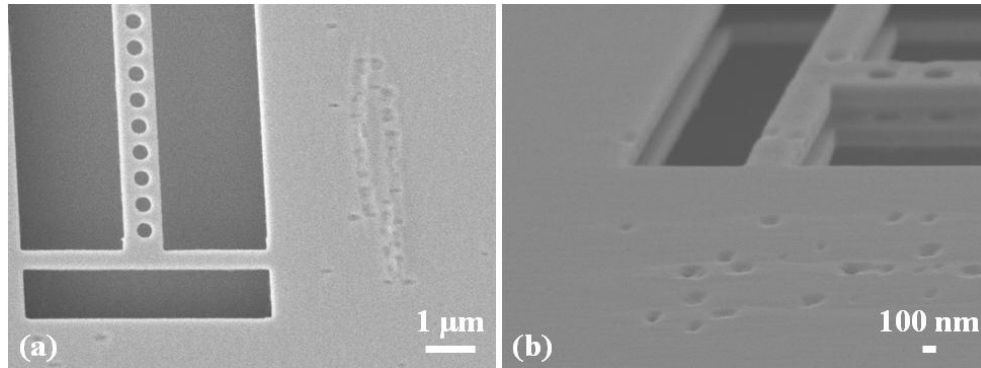
Fig. 6.11 SEM images of defects found on the surface of the as-fabricated samples.

The author also investigated the integration of stress-releasing structures at the ends of the four arms of the double-slab nano-opto-electromechanical system (NOEMS) devices, which will be discussed in Chapter 7. The stress-releasing structures are expected to solve the buckling problem of the device. Fig. 6.12 shows the results of the Comsol simulation of the upper membrane with four supporting beams under internal stress (Fig. 6.12 (b)). The BLF value of this structure is ~ 4.48. In comparison, the BLF value for the standard structure is 0.48 (Fig. 6.12 (a)). The geometry of the devices illustrates the shape of their 1st buckled mode. It can be seen from Fig. 6.12 (b) that for the device with stress-releasing structures, the internal stress has been transferred to the four supporting beams since the center of the device stays unbuckled whilst the supporting beams are buckled under the buckling loads.
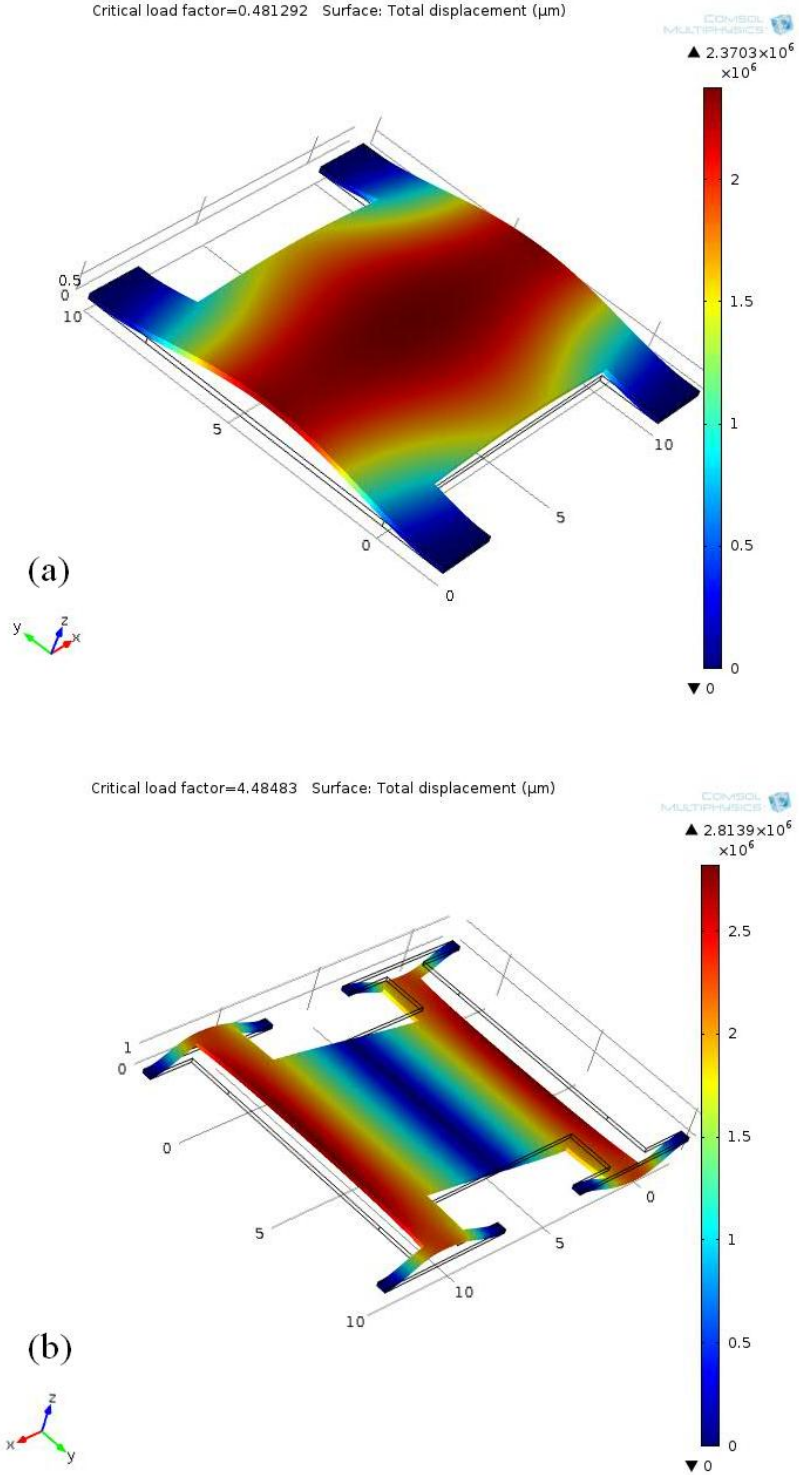
Fig. 6.12 Results of Comsol simulation for the standard structure of the 4-arm upper membrane of the NOEMS devices (a) and the modified structure with stress-releasing structures (b). The length and width of the supporting beams are 6 μm and 0.4 μm respectively. The thickness of structures used in the simulation is set to 180 nm. The shape of the structures corresponds to the geometry of the devices under the 1st buckled mode. The color bar indicates the deformation of the structures in the vertical direction.

6.3 Optical and mechanical property characterization of the NOMS devices

The optical characterization of the cavity mode photoluminescence of the NOMS device was done by Sybren Westerndorp and Tian Xia at TU/e. The opto-mechanical study of the NOMS devices was performed by Rick Leijssen and Sybren Westerndorp at the AMOLF Institute. Part of the contents of this Section has been included in Sybren Westerndorp's Master thesis. [6]

Fig. 6.13 shows the design of the device with stress releasing structures. The major parameters in the design are illustrated in Table 6.4.
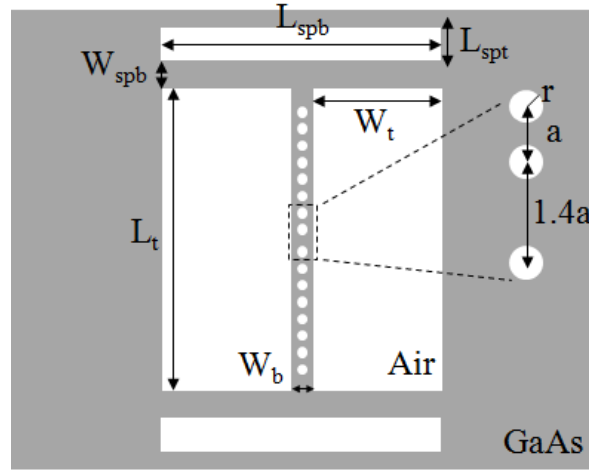
Fig. 6.13 Schematic illustration of the design of the nanobeams with supporting beams.

Table 6.4 Illustration of parameters in Fig. 6.12

Symbol	Parameter	Comments
a	Lattice constant	From 360 nm to 530 nm in step of 5 nm
r	Hole radius	0.28a
s	Cavity spacing	1.4a
L_t	Major Trench length	L_1=20.96a ; L_2= 22.96 a; L_3= 24.96a;
W_b	Nanobeam width	W_1=1.31a, W_2=1.48a, W_3=1.55a
W_t	Major Trench width	2.5 μm - W_b/2
L_{spb}	Length of supporting beams	5 μm
L_{spt}	Length of trench for supporting beams	1 μm
W_{spb}	Width of supporting beams	0.4 μm
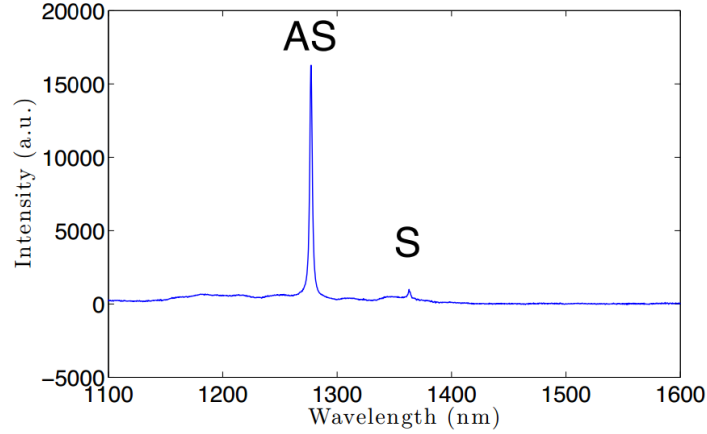
Fig. 6.14 RT μ-PL spectrum of a vertically-aligned double nanobeams device with L_t = 9.6 μm, beam width W_b = 570 nm, lattice constant a = 385 nm, and hole radius r = 108 nm.

Fig. 6.14 shows a typical PL spectrum of the vertically-coupled nanobeams with beam length L_t = 9.6 μm, beam width W_b = 570 nm, lattice constant a = 385 nm, hole radius r = 108 nm. The anti-symmetric (AS) mode and symmetric mode (S) [1], [7], [8] can be recognized. The quality factor Q for the AS mode is 826. Fig. 6.15 shows the wavelength of the AS mode as a function of the lattice constant for nanobeams with the same width W_2 = 1.48 a, and the same length of L_3 = 24.96 a. The linear fit of the cavity mode wavelength gives $\lambda_{cav} = 494 nm + 2.04a$.
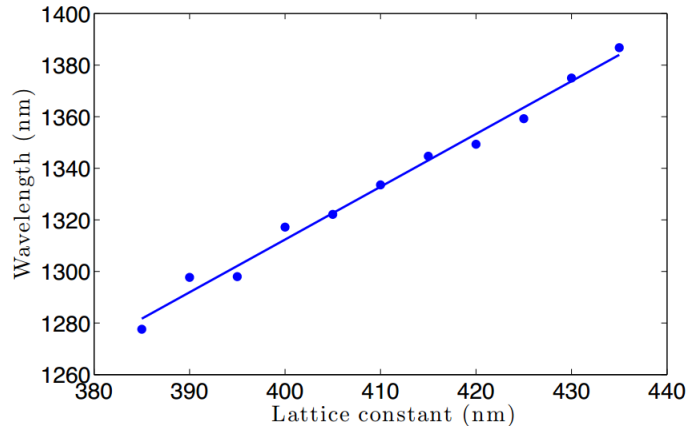
Fig. 6.15 Wavelength of the AS mode as a function of the lattice constant for nanobeams with the same width W_2 = 1.48 a, and the same length of L_3 = 24.96 a.

In a series of optical measurements taken by Rick Leijssen in the group of E. Verhagen at AMOLF, the mechanical spectrum for the lowest order mechanical mode of a vertically-coupled double nanobeams device with a = 535 nm, L_t =13.35 μm, W_b =0.8 μm was measured by recording the noise spectrum of the light scattered by the nanobeams as a function of the incident wavelength. (Fig. 6.16) The change of the mechanical frequency of the device for varying optical frequency, indicates the occurrence of the optical spring effect. The details of the experiment can

be found in Ref. [6]. This represents the first demonstration of optomechanical coupling in a vertically-stacked double-nanobeam structure.
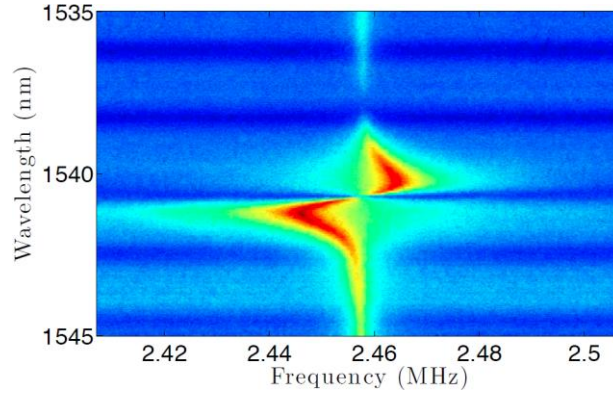
Fig. 6.16 The Mechanical spectrum for the first mechanical mode of a double nanobeams device with L_t = 13.1 µm, beam width W_b = 780 nm, lattice constant a = 525 nm, and hole radius r = 147nm.. The mechanical quality factor of the mode is 1500±100.

6.4 Conclusion

In this chapter, the optimization in the fabrication and the design of the vertically-aligned double nanobeam NOMS devices has been discussed. By increasing the Al concentration in the AlGaAs sacrificial layer from 70% to 79% and etching the $Al_{0.79}Ga_{0.21}As$ layer with HF 10% etchant, the NOMS device was fabricated. Supporting beams were added to the NOMS devices to improve the mechanical susceptibility of the device structure under internal stress. AS and S modes in the PL spectra and the optical spring effect were observed from the device.

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CHAPTER 7

Independent control of the exciton energy and of cavity mode wavelength in a photonic crystal cavity

In this chapter, the study of the independent control of the exciton energy of QDs and the cavity mode wavelength of a photonic crystal cavity is discussed. First, problems with the fabrication of the NOEMS device and corresponding solutions are introduced (Section 7.1). Then, methods used to upgrade the metallization process are discussed (Section 7.2). In Section 7.3, the optimized general processing flow of the device is described. In Section 7.4, the preliminary results of the tuning of a NOEMS device are presented. In Section 7.5, the results of the demonstration of a NOEMS device, which allows an independent control of the exciton energy and cavity wavelength of a double-membrane PCCs, are discussed and analyzed.

7.1 Problems with the fabrication of the NOEMS device and solutions

From May 2013, the author started the work described in this chapter. It is a continuation of the work of L. Midolo [1], [2]. Based on the standard double-slab NOEMS device configuration, by adding one pair of contacts on the top membrane and applying an electric field along the growth direction of the QDs, the exciton energy of the QDs can be tuned independently, via the Stark effect, from the electromechanical tuning of the cavity wavelength of the double-membrane photonic crystal cavity (Fig.7.1).
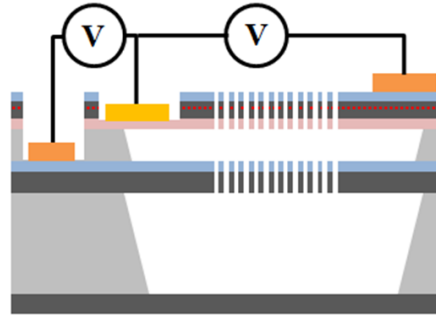
Fig. 7.1 Schematic illustration of the device structure and the working scheme of the device with two pairs of contacts under DC bias.

The sample structure of the device is introduced in Table.7.1. In the beginning of this work, the author followed the process flow described in Ref. [1]. However, several problems were encountered. The first problem came from the etching of the $Al_{0.7}Ga_{0.3}As$ sacrificial layers during the releasing of the double-slab structures. The second problem came from the removal of the Si_xN_y hard mask in the last step of the processing.

Table 7.1 Sample structure for fabricating a complete device

Material	Thickness	Doping (cm^{-3})	Comments
Air			
GaAs	30nm	undoped	*Upper Slab*
$Al_{0.7}Ga_{0.3}As$	30nm	undoped	
GaAs	50nm	$p=1.5\times10^8$	
GaAs	35nm	undoped	
$In_{0.2}Ga_{0.8}As$	5nm	undoped	
InAs QDs	~ 2ML InAs	undoped	
GaAs	40nm	undoped	
GaAs	50nm	$n=2\times10^8$	
$Al_{0.7}Ga_{0.3}As$	240nm	undoped	*Sacrificial Layer 2*
GaAs	50nm	$p=2\times10^8$	*Lower Slab*
GaAs	120nm	undoped	
$Al_{0.7}Ga_{0.3}As$	1500nm	undoped	*Sacrificial Layer 1*
GaAs	500nm	undoped	*Buffer Layer*
GaAs (100) SI substrate	350μm		

7.1.1. Problems with the etching of the $Al_{0.7}Ga_{0.3}As$ sacrificial layers

Problems

According to the standard process flow for the fabrication of the double-slab NOEMS device, the $Al_{0.7}Ga_{0.3}As$ sacrificial layers were removed by etching with the HF 1% solution for 45 sec and with the HCl (36%) solution at 1 ℃ for 8 min. The purpose for etching the sample at 1 ℃ is to improve the selectivity of the HCl between $Al_{0.7}Ga_{0.3}As$ and GaAs. However, devices fabricated on the sample (denoted as sample 'P', sample growth series number: Z607) with this recipe were found to have $Al_{0.7}Ga_{0.3}As$ residue left between the two membranes after etching. (Fig. 7.1)

To understand the origin of this problem, the author first considered the possibility of the blocking of the etchant by polymers formed on the sidewall of the device during ICP etching. Experiments were performed on an old sample grown at Würzburg (denoted as sample 'O', sample growth series number: C 3760) for which the etching problems were not observed before. The fabrication of sample O followed exactly the same procedure as sample P. However, no wet etching problems were observed for sample O. (Fig. 7.2) It indicates that the ICP-etching is not the cause for the problem. The result also drove the author to formulate the hypothesis that the etching problem could be a material – related problem.
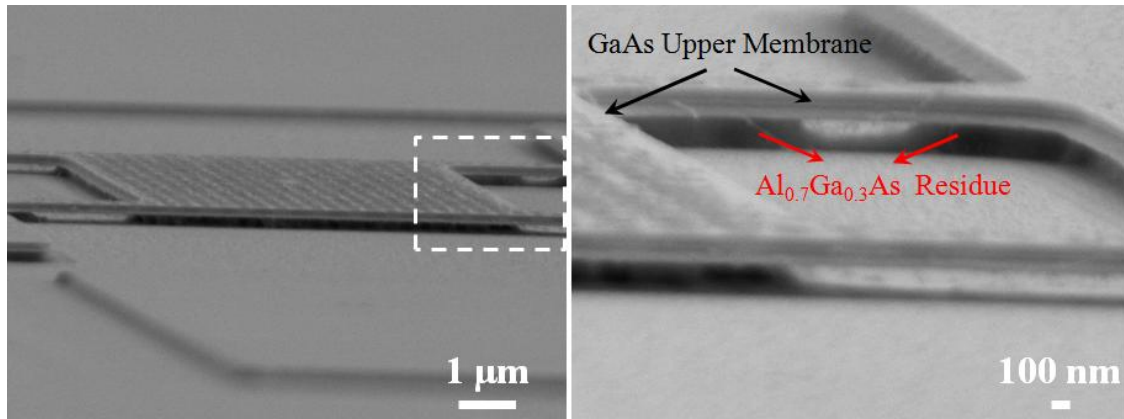
Fig. 7.1 (a) SEM image of a device fabricated on sample P and etched with the standard recipe. The device has $Al_{0.7}Ga_{0.3}As$ residue left between the two membranes after etching. (b) Enlarged SEM image of the area of the device in the dashed square of (a).
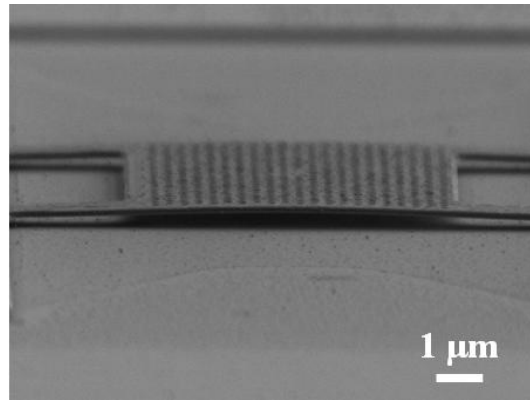
Fig. 7.2 SEM image of a device fabricated on sample O. No $Al_{0.7}Ga_{0.3}As$ residue was observed to be left between the two membranes after etching.

Another series of etching tests was performed to further investigate the etching problem. First, one piece of sample P with freshly cleaved edges was etched with the HF 5% solution for 30 sec. After etching, the two $Al_{0.7}Ga_{0.3}As$ sacrificial layers were found to be not homogeneously etched away. (Fig. 7.3 (a)) The same etching behavior was not observed in etched sample O.

Secondly, trenches were fabricated on sample P by using ICP etching. The pieces were then wet etched with the HF 1% solution for 1 min and HF 5% solution for 30 sec. Fig. 7.3 (b) and (c) present SEM images of two etched trenches on the same piece which were etched down to the inter-membrane layer by ICP. Different etching rates to the inter-membrane $Al_{0.7}Ga_{0.3}As$ layer at different positions of the piece were observed. The etched $Al_{0.7}Ga_{0.3}As$ layer shows similar characteristics as what has been shown in Fig. 7.3 (a). Fig. 7.3 (d) shows the SEM image of another piece of sample P with trenches etched into the bottom $Al_{0.7}Ga_{0.3}As$ sacrificial layer and then etched with the HF 1% solution for 1 min and the HF 5% solution for 30 sec. The inhomogeneous etching of the inter-membrane $Al_{0.7}Ga_{0.3}As$ layer was also observed.
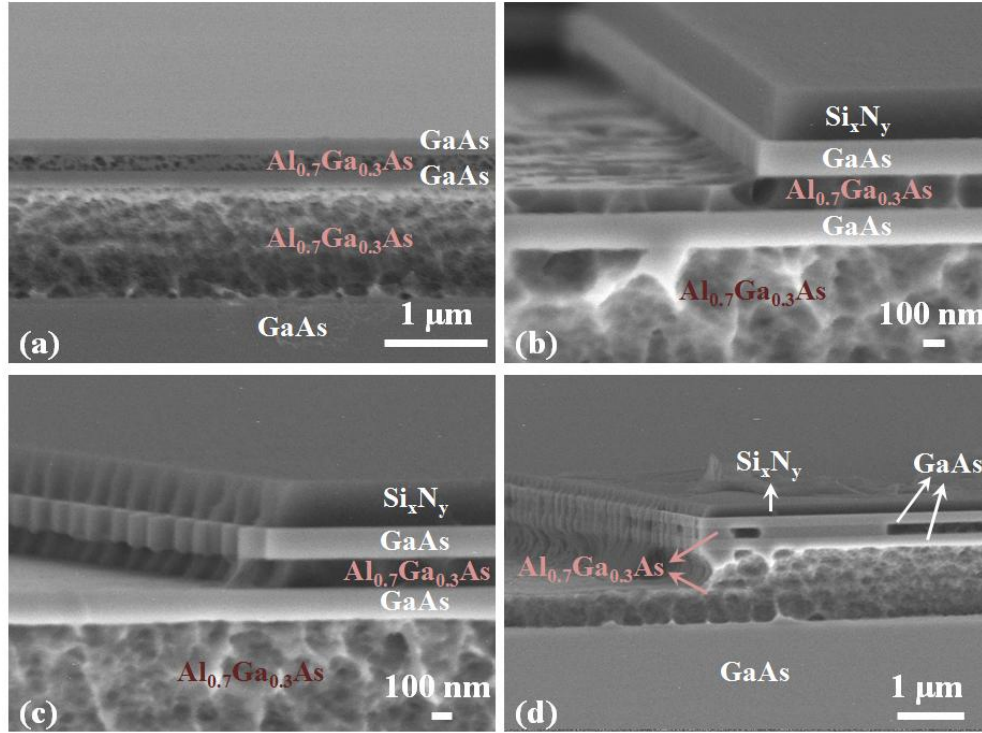
Fig. 7.3 SEM images of etched samples. (a) SEM image of one piece of sample P with freshly cleaved edges etched with the HF 5% solution for 30 sec. (b) and (c): SEM images of two etched trenches on sample P dry-etched with ICP into the inter-membrane layer and wet-etched with HF 1% solution for 1 min (b) and HF 5% solution for 30 sec (c). (d): SEM image of another piece of sample P with trenches dry-etched with ICP into the bottom $Al_{0.7}Ga_{0.3}As$ sacrificial layer and then etched with the HF 1% solution for 1 min and the HF 5% solution for 30 sec.

The abnormal as-etched $Al_{0.7}Ga_{0.3}As$ layer had never been observed before for the samples grown at Nanolab @ TU/e cleanroom and had not been reported in any literature to the knowledge of the author. In the meanwhile, Francesco Pagliano also met similar etching problems in the fabrication of single membrane nano-photonic devices on the samples grown at TU/e.

The author attributed the cause of the problem to possible contaminations in the $Al_{0.7}Ga_{0.3}As$ layers during MBE growth. Later on, a crack on the MBE cooling shroud was discovered since a relatively large amount of N_2 gas was detected in the MBE growth chamber with a mass-spectrometer. Tentatively, the author assumed Nitrogen to be incorporated into the $Al_{0.7}Ga_{0.3}As$ layers during growth and to cause the etching problems. Although no further research was done to find out the composition of material of the problematic $Al_{0.7}Ga_{0.3}As$, several month later, after having solved the problem with the LN_2 leakage, samples grown with the same recipe as sample P did not show the wet etching problems anymore. This fact confirmed the author's assumption about the causality relationship between the presence of nitrogen gas in the chamber and the etching problem.

Solutions

Before having noticed and solved the problem with the cracked shroud, the author collaborated with Francesco Pagliano, Yongjin Cho and Frank van Otten to investigate possible new growth

recipes to improve the quality of the $Al_{0.7}Ga_{0.3}As$ layers. A sample (denoted as sample 'T') with layered $Al_xGa_{1-x}As$/GaAs structures with x varied from 70% to 79% was grown. The layers of $Al_{0.7}Ga_{0.3}As$, $Al_{0.73}Ga_{0.27}As$, $Al_{0.75}Ga_{0.25}As$ and $Al_{0.77}Ga_{0.23}As$ were not homogeneously etched away across the sample. Only the etched $Al_{0.79}Ga_{0.21}As$ layer was residue-free all over the sample. Therefore, $Al_{0.79}Ga_{0.21}As$ was used to substitute $Al_{0.7}Ga_{0.3}As$ in the growth of production samples for device fabrication. A simple etching test similar to the one performed on sample T (etch in HF 5% for 30 sec) was conducted on another production sample with $Al_{0.79}Ga_{0.21}As$ as the sacrificial layers. No residues were observed on the as-etched sample. (Fig. 7.4)
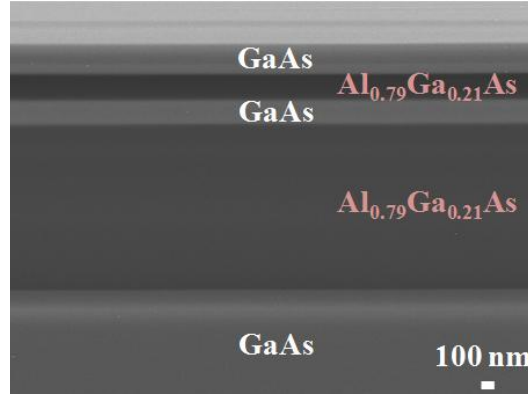
Fig. 7.4 SEM image of an as-etched sample with $Al_{0.79}Ga_{0.21}As$ as the material in the sacrificial layer, etched from the cleaved facet.

To test the etching of new $Al_{0.79}Ga_{0.21}As$ layers with the standard recipe of HF 1% + HCl (36%) @ 1°C, trenches were made on the sample (denoted as sample 'L') by etching with ICP into the bottom $Al_{0.79}Ga_{0.21}As$ layer. After wet etching, fluffy layers were found hanging between suspended GaAs layers (Fig. 7.5 (a)-(c)). The origin of the layer was not completely clear. It had never been observed on standard production samples, such as sample O. Immersing the as-etched sample into the methanol: Br_2 solution for 5 s resulted in the detachment of part of the fluffy layers from the sidewall of the etched trenches. However, the sidewall was not completely clean and fluffy layers were found on the bottom GaAs layer (Fig. 7.5 (d)).

The author tried several other different etching recipes to find a better method which provides both a good etching profile and a clean interface to sample L. The HF 5% solution and the HF 10% solution were both used in the test. After a 20 sec etching in the HF 5% solution, the bottom $Al_{0.79}Ga_{0.21}As$ layer remained slightly under-etched (Fig. 7.6 (a)). Once in a while, fluffy layers were observed hanging on the sidewalls of the etched structures (Fig. 7.6 (b)). In comparison, the sample after 20 sec etching in the HF 10% solution was nicely etched (Fig. 7.6 (c)) and no fluffy layers were observed on the sample (Fig. 7.6 (d)). Therefore, the recipe of etching the sample in HF 10% solution for 20 sec was adopted as the optimized etching recipe for samples with $Al_{0.79}Ga_{0.21}As$ sacrificial layers.
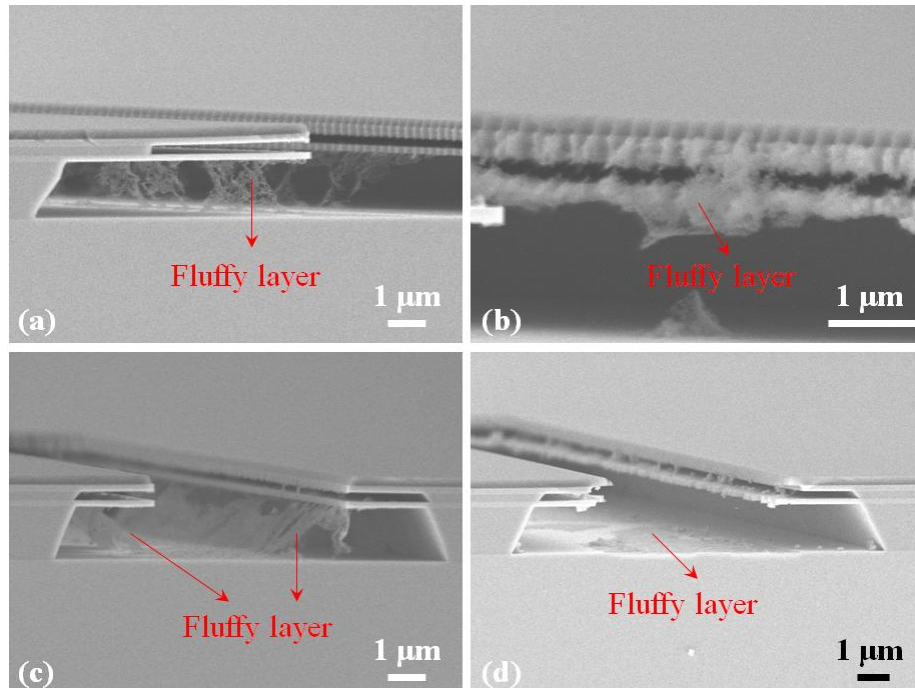
Fig. 7.5 (a) – (c) SEM images of sample L etched with HF 1% solution for 45 sec and HCl (36%) solution for 4 min @ 1 ℃. (d) SEM image of as-etched sample L after being immersed in the methanol: Br$_2$ solution for 5s.
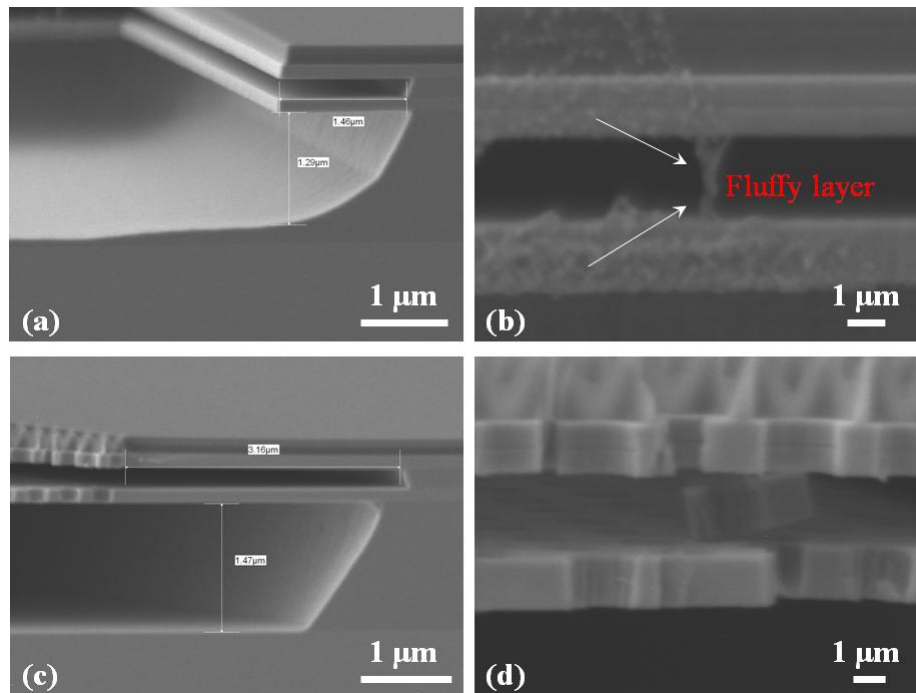

Fig. 7.6 (a)-(b): SEM images of sample L etched with the HF 5% solution for 20 sec. (c)-(d): SEM images of sample L etched with the HF 10% solution for 20 sec.

7.1.2. Optimization of the bottom p-GaAs (p-via) etching procedures of samples with Al$_{0.79}$Ga$_{0.21}$As sacrificial layers

Firstly, due to the high reactivity of the Al$_{0.79}$Ga$_{0.21}$As layer with HCl, the previous recipe described in Ref. [1] to remove the surface oxide by immersing the sample to 1 HCl (36%): 1 H$_2$O solution for 2 min was not applicable anymore. The old recipe was modified by immersing the sample in the solution of 1 NH$_4$OH (30%): 10 H$_2$O for 2 min.

Secondly, in the previous fabrication recipe [1], the p-via was etched by the following procedures (Fig. 7.7):

1. Wet etching of the GaAs top-membrane by a 40 Citric acid: 1 H$_2$O$_2$ solution for about 1.5 min through openings defined in the Si$_x$N$_y$ hard mask. (Step 1 in Fig. 7.7)
2. Removal of photoresist (HPR 504) by O$_2$ plasma stripping. (Step 2 in Fig. 7.7)
3. Wet etching of the Al$_{0.7}$Ga$_{0.3}$As layer through the openings on the GaAs with the solution of HF 1% for ~ 2.5 min. This solution also removes the Si$_x$N$_y$ hard mask at the same time. (Step 3 in Fig. 7.7)
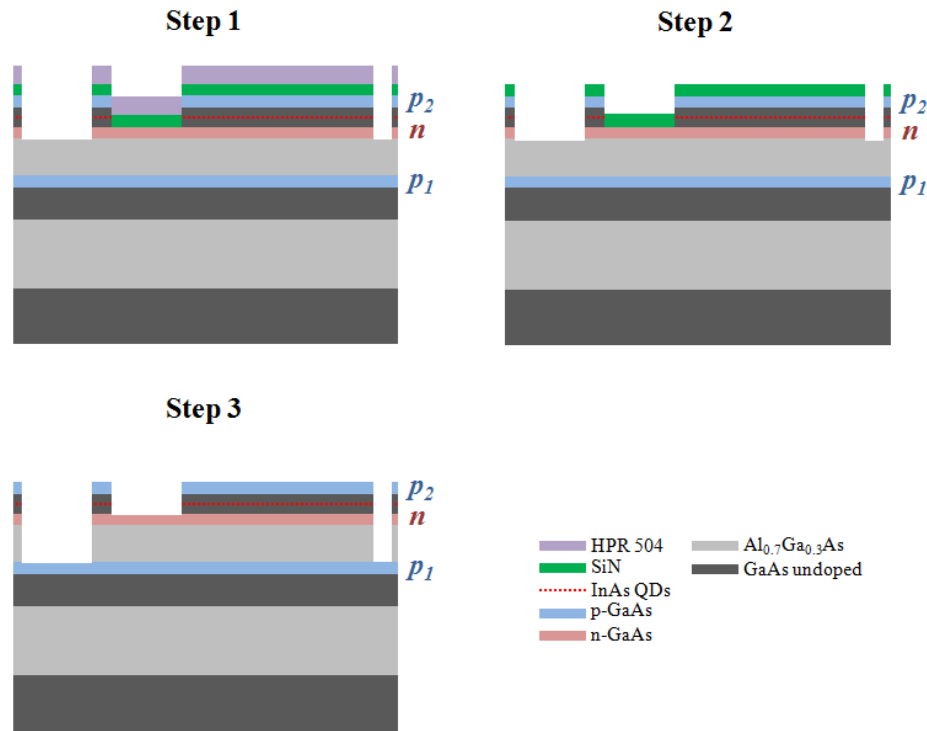
Fig. 7.7 Schematic illustration of the fabrication procedures to etch the p-via described in Ref. [1].

However, due to the change of the Al concentration from 70% to 79%, this etching recipe did not work anymore due to the faster etching rate of the Al$_{0.79}$Ga$_{0.21}$As as compared to Al$_{0.7}$Ga$_{0.3}$As. The etching rates of the HF 1% solution on Al$_{0.79}$Ga$_{0.21}$As and Si$_x$N$_y$ are ~ 6 nm/s and ~ 0.3 nm/s, respectively. That is to say, when the 50 nm Si$_x$N$_y$ hard mask gets completely etched away, the 240 nm thick Al$_{0.79}$Ga$_{0.21}$As layer has already been severely over-etched. In this case, the four bridges (2 nm in width) of the top membrane will be completely released and therefore degrade

the mechanical robustness of the upper membrane in the processing steps afterwards. The recipe optimized by the author uses a photoresist mask instead of Si_xN_y and a combination of dry and wet etching. It proceeds as follows: (Fig. 7.8):

Step 1: Spin-coating of the HPR 504 photoresist directly on the sample after n-via etching. Exposure and developing of the pattern of p-via on the resist.

Step 2: GP-RIE etching of the sample through the openings in the photoresist with $SiCl_4$/Ar plasma. The general plasma etching recipe was optimized by Francesco Pagliano. The etching should be stopped in the inter-membrane $Al_{0.79}Ga_{0.21}As$ layer.

Step 3: Removal of the photoresist by putting the etched sample into acetone ultrasonic bath for 3 min followed by a 1.5 min IPA flow wash. Measuring of the etched depth in the $Al_{0.79}Ga_{0.21}As$ layer with the 'TENCOR'.

Step 4: Wet etching of the remaining $Al_{0.79}Ga_{0.21}As$ layer with HF 1%. The etching time can be calculated based on the profile measurement in Step 3.
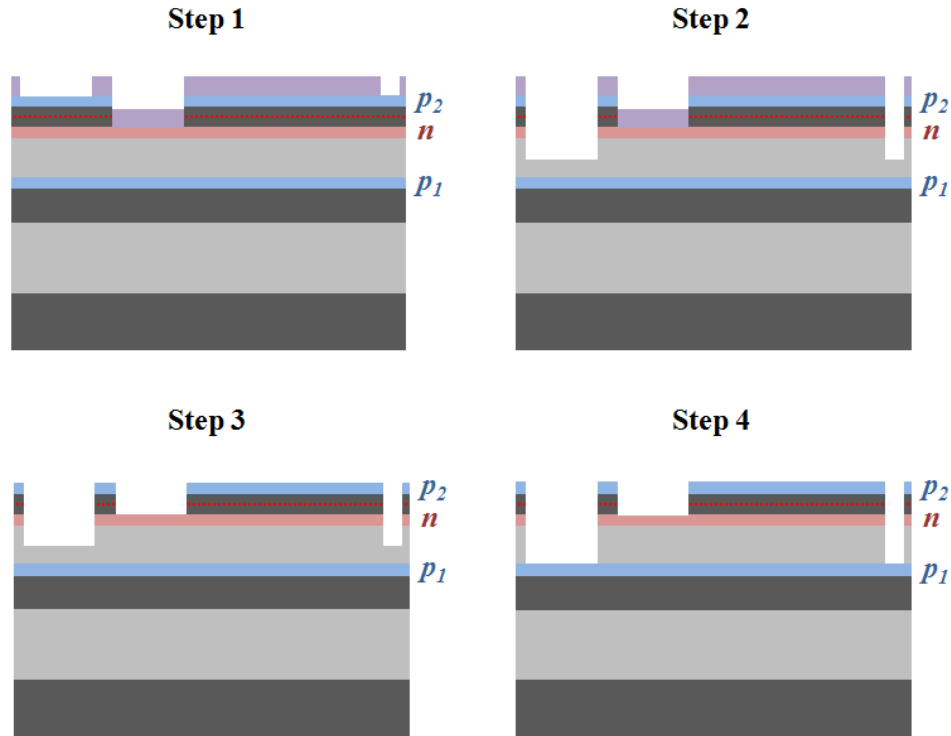
Fig. 7.8 Schematic illustration of the optimized recipe to etch the p-via in samples with $Al_{0.79}Ga_{0.21}As$ sacrificial layers.

7.1.3 Solution to the problem with the removal of the Si_xN_y hard mask after the releasing of the double-slab photonic crystal structure

A problem was encountered in the last step of the processing after the releasing of the double-slab crystal structure. Previously [1], this step was performed in the Barrel etcher with the CF_4 plasma following the O_2 plasma stripping for 10 min at 300 W in the same chamber. Due to the malfunctioning of the mass flow controller of the Barrel etcher and some possible contaminations in the gas line, the previous recipe was not able to thoroughly remove the Si_xN_y without damaging the contact layers.

To optimize the process, the CF_4 plasma anisotropic etching in the GP-RIE system was used to remove the Si_xN_y mask in the last step of the processing flow. The general recipe was optimized by Francesco Pagliano. It is worth noticing that the etching rate of the CF_4 plasma is sensitively influenced by the size of the sample. In all the tests, to improve the reproducibility, as-fabricated samples with the size of 1/36 of a 2-inch wafer were used.

Fig. 7.9 shows the thickness of the Si_xN_y hard mask after different processing steps. The four data points on the left side of the orange dashed line show the thickness of Si_xN_y after depositing Si_xN_y with PECVD deposition for 28 min 50 sec, after ICP etching for 3 min 40 sec, after an additional etching in the HF 1% solution for 45 sec, and after an additional etching for 5 sec in the HF 5% solution. These steps are the ones needed for the etching of the PCCs and the selective etching of the $Al_{0.79}Ga_{0.21}As$ (see general process flow in Section 7.3). The x-coordinates of the four data points do not have any physical meanings. On the right side of the dashed line, the thicknesses of Si_xN_y after CF_4 plasma etching for different time are shown by the black points. The plasma etching rates in the first 4 min and the second 4 min were estimated to be 13.4 nm/min and 24.8 nm/min, respectively.
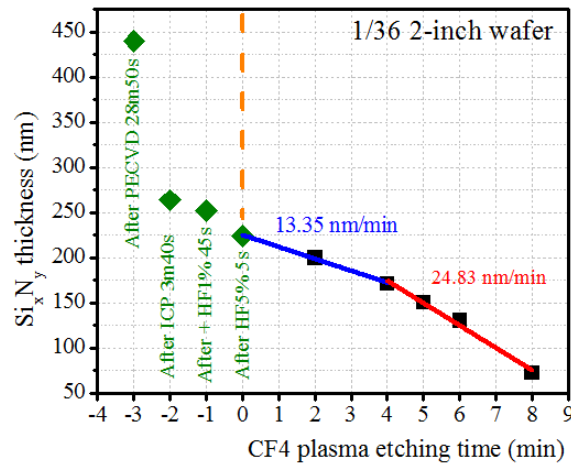
Fig. 7.9 Conclusion of the thickness of the Si_xN_y hard mask after different processing steps.

However, in the period when the author worked on the GP-RIE, the etching rate of the system degraded gradually due to unknown reasons. As a result, the calibrated etching rates shown in Fig. 7.9 were only valid temporarily.

Then, a sample with diode structures fabricated on top went through steps of 3 min 40 sec ICP etching to create holes on PCCs, 15 sec wet etching in HF 10% to release the double-membrane structure, 1 min hot IPA bath, and CF_4 plasma etching in GP-RIE for various length of times. Fig. 7.10 shows the SEM images of one device etched for 6.5 min with the CF_4 plasma. The Si_xN_y residue layer can be observed in the defect areas of the L3 cavity (Fig. 7.10 (a)) and the planar areas of the sample (Fig. 7.10 (b) – (d)).
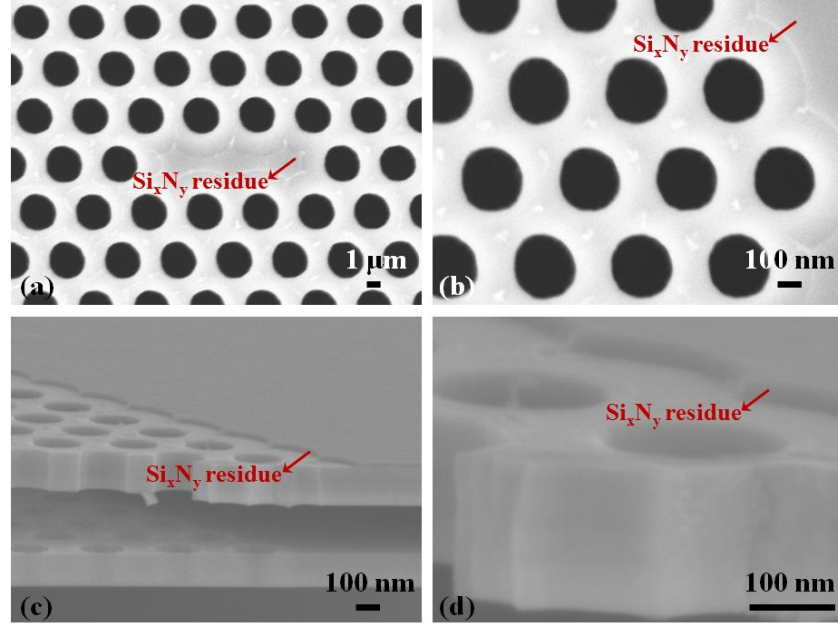
Fig. 7.10 SEM image of a sample which have gone through steps of: 3 min 40 sec ICP etching, 15 sec wet etching in HF 10%, 1 min hot IPA bath, and CF_4 plasma etching in GP-RIE for 6.5 min.

By increasing the CF_4 plasma etching time to 8 min 15 sec, the Si_xN_y mask was completely removed. (Fig. 7.11) The RT current-voltage (I-V) curves of the Membrane diode and the QD diode on the as-etched device are shown in Fig. 7.12. The contact material in this sample is Ti/Au (50 nm/ 200 nm). Both diodes turned on at the voltage of approximately 1 V. The QDs diode started to break to break down from - 4.9 V. No break-down was observed for the Membrane diode till - 5V.
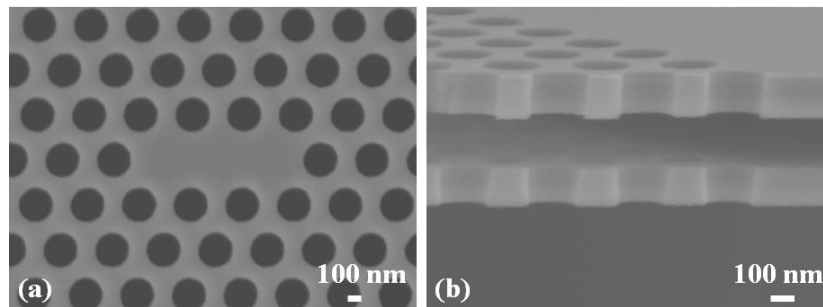
Fig. 7.11 SEM image of a sample which has gone through steps of: 3 min 40 sec ICP etching, 15 sec wet etching in HF 10%, 1 min hot IPA bath, and CF_4 plasma etching in GP-RIE for 8 min 15 sec.

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When the CF$_4$ plasma etching time increased to 8 min 30 sec, the I-V of the QD diode deteriorated (Fig. 7.13 (b)), indicating the creation of plasma induced damages in the top p-GaAs layer.[3] Therefore, 8 min 15 sec was used as the optimized CF$_4$ plasma etching time.
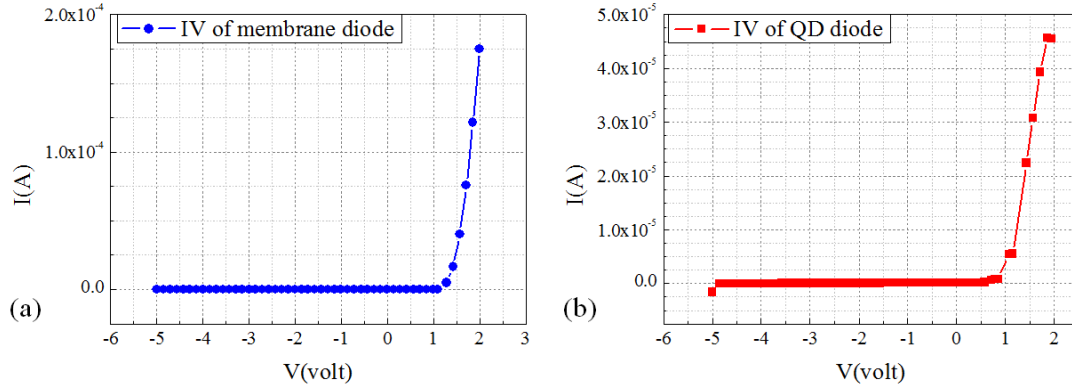
Fig. 7.12 Room temperature current-voltage (I-V) curves of the Membrane diode (a) and the QD diode (b) on a device etched with CF$_4$ plasma for 8 min 15 sec.
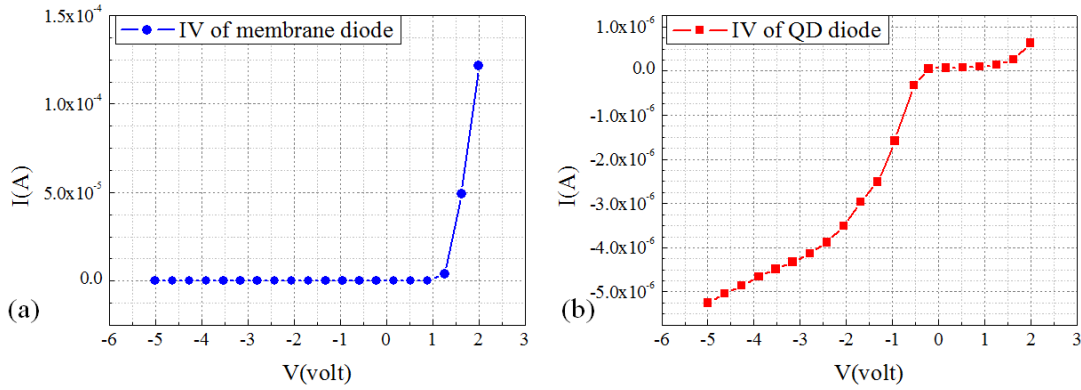
Fig. 7.13 Room temperature current-voltage (I-V) curves of the Membrane diode (a) and the QD diode (b) on the device etched with CF4 plasma for 8 min 30 sec.

7.2 Changing from Schottky contact to ohmic contact

As described in Ref. [1], the use of Ti/Au on the n-GaAs layer results in a Schottky contact. In addition, the p-contact is not completely ohmic either. The Schottky nature of the contact limits the dynamic tuning speed of the NOEMS device at high frequency. The work described in this Section was done by the author in collaboration with Francesco Pagliano. By adopting the optimized metallization recipe for producing ohmic contacts which is described in the Section 4.3 of Ref. [4], the author optimized the fabrication procedures of ohmic contacts on the NOEMS devices.

n-contact metallization Optimization

The contact metal materials used for the p-contacts and n-contacts were Ni/Zn/Au (5 nm/ 20 nm/ 150 nm) and Ge/Ni/Au (20nm/ 10nm/ 150nm), respectively. In the process flow, after the p-via

etching (Fig. 7.8), the n-contacts were first fabricated. Right after the metal evaporation, the n-contact was annealed at 380 ℃ for 1 min in an N_2 ambient with the rapid thermal annealing (RTA) system. Fig. 7.14 (b) and (c) compare the I-V curves measured on the TLM pads on the n-GaAs layer (Fig. 7.14 (a)) before and after the RTA of the n-contacts. After RTA, the n-contact becomes perfectly Ohmic. (Fig. 7.14 (d)) The sheet resistance R_{s-n} of the n-GaAs layer and the n-contact resistivity per unit area ρ_{c-n} are estimated to be 1125Ω/□ and 3.9×10^4 Ωμm^2, respectively.
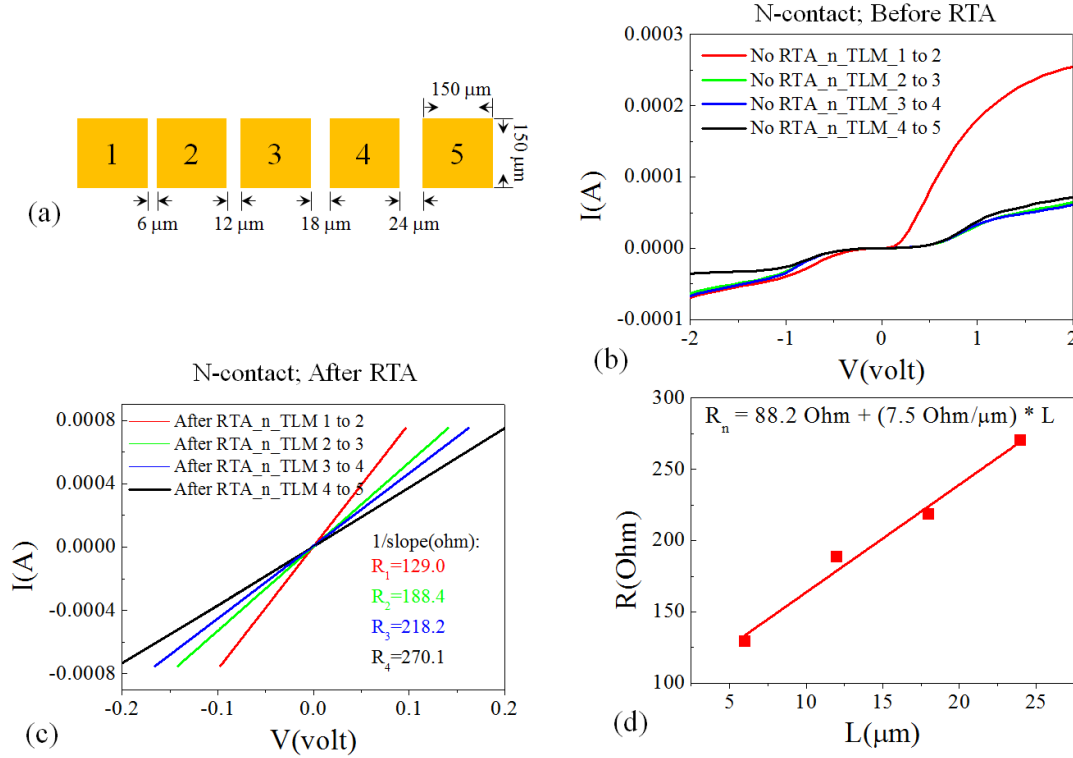
Fig. 7.14 (a) Schematic illustration of the configuration of the TLM pads. (b) and (c): I-V curves of adjacent n-TLM pads before (b) and after (c) the RTA process to the n-contacts. (d): TLM measurement result of the n-contacts.

p-contact metallization optimization

After the n-contact RTA process, the p-contacts were fabricated. The I-V curves of the as-fabricated p-contacts already showed the characteristics of ohmic contacts. (Fig. 7.15 (a)) After annealing with RTA at 350 ℃ for 1 min, the ohmic property of the contact is preserved. (Fig. 7.15 (b)) However, the contact resistance increased after annealing (Fig. 7.15 (c)). Before (after) RTA, the sheet resistance R_{s-p} and the contact resistance per unit area ρ_{c-p} are 3090 Ω/□ (3000 Ω/□) and 9.66×10^4 Ωμm^2 (1.9×10^5 Ωμm^2).

The I-V curves of the membrane diode and QD diode before and after the RTA process of the p-contact were compared in Fig 7.16 (a) and (b). No big change in the I-V property of the membrane diode was observed. However, after the RTA, the I-V curves of the QD diode broke down at a smaller reverse bias voltage.
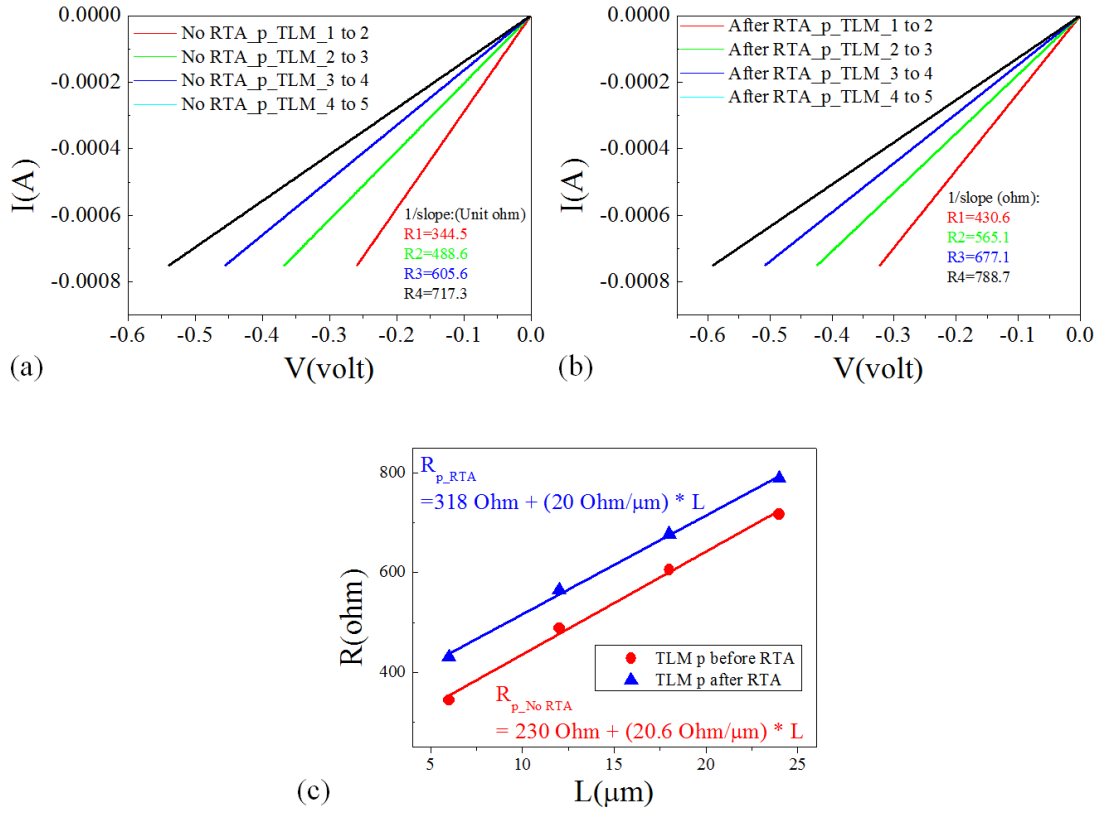
Fig. 7.15 (a) and (b): I-V curves of adjacent p-TLM pads before (a) and after (b) the RTA process to the p-contacts. (c): TLM measurement result of the p-contacts before and after the RTA process.
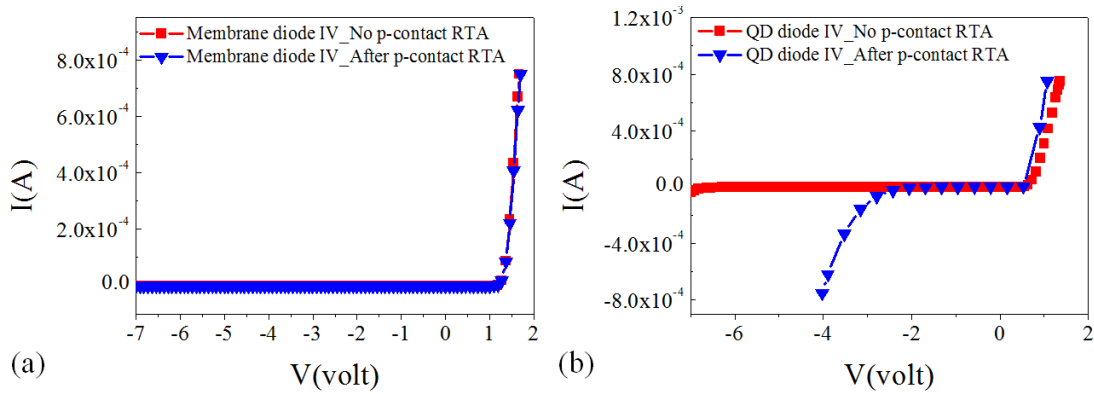
Fig. 7.16 I-V curves of the Membrane diode (a) and QD diode (b) before and after the RTA process of the p-contact.

As a short conclusion to this Section, the optimized recipe for fabricating ohmic contacts is:

➢   Step a: n-contact deposition (Ge/Ni/Au (20nm/ 10nm/ 150nm)) + 1 min RTA at 380 ℃.
➢   Step b: p-contact deposition (Ni/Zn/Au (5 nm/ 20 nm/ 150 nm)). No RTA is required.

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7.3 General process flow of the double-slab NOEMS device

The optimized fabrication process flow of the double-slab NOEMS device can be summarized in the following major steps:

> **n-via etch:**

Step 1: Deposit the SiN hard mask by PECVD and define the n-via with optical lithography and etch the SiN hard mask with CF_3 RIE.

Step 2: Etch GaAs with Citric acid: H_2O_2 (40:1) solution till the top of n-layer.
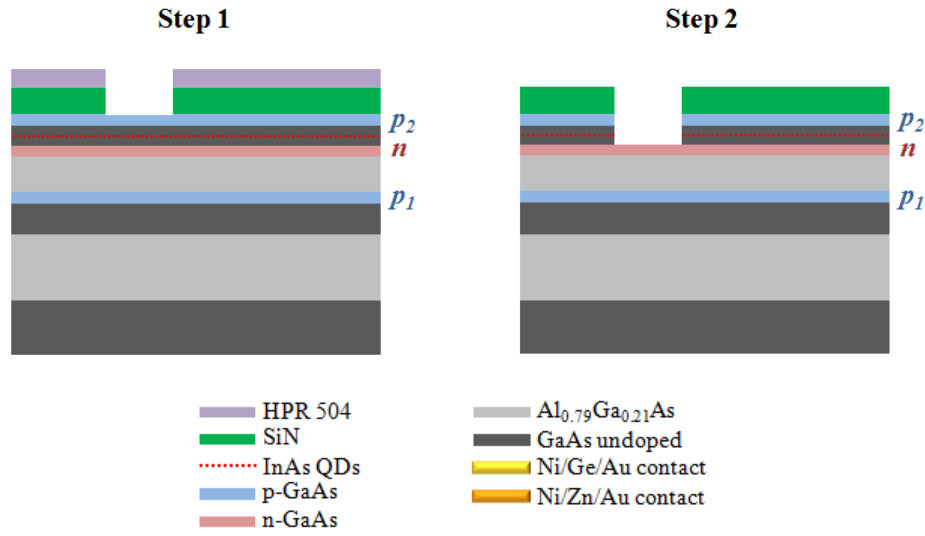
Fig. 7.17 Schematic illustration of the NOEMS device process flow.（Steps 1–2）

> **p-via etch**:

Step 3: Define the p-via with optical lithography and dry etch GaAs with $SiCl_4$/Ar RIE into the middle of the Al $_{0.79}$Ga $_{0.21}$As As sacrificial layer.

Step 4: Etch remaining $Al_{0.79}$Ga $_{0.21}$As layer with HF 1% and stop at the top of p_1 layer.
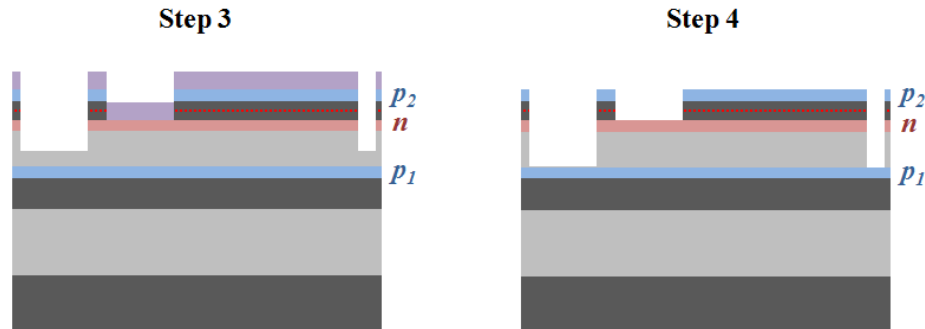
Fig. 7.18 Schematic illustration of the NOEMS device process flow.（Steps 3–4）

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➢ **Contact evaporation**:

Step 5: Define the n-contact with optical lithography, evaporate Ge/Ni/Au (20 nm/ 10 nm/ 150 nm) metal layers, lift off and anneal the contact with RTA at 380 ℃ for 1 min.

Step 6: Define p-contacts with optical lithography, evaporate Ni/Zn/Au (5 nm/ 20 nm/ 150 nm) metal layers and lift off.
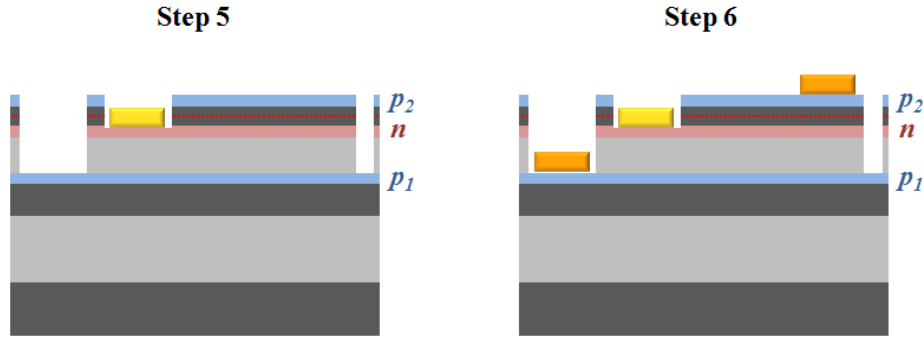
Fig. 7.19 Schematic illustration of the NOEMS device process flow.（Steps 5–6）

➢ **Photonic crystal cavity etching**

Step 7: Define PCCs with EBL, etch ~ 400 nm thick SiN hard mask with CHF_3/O_2 RIE.

Step 8: Transfer PCCs pattern from SiN hard mask to sample with Cl_2/N_2 ICP-RIE @ 200 ℃.
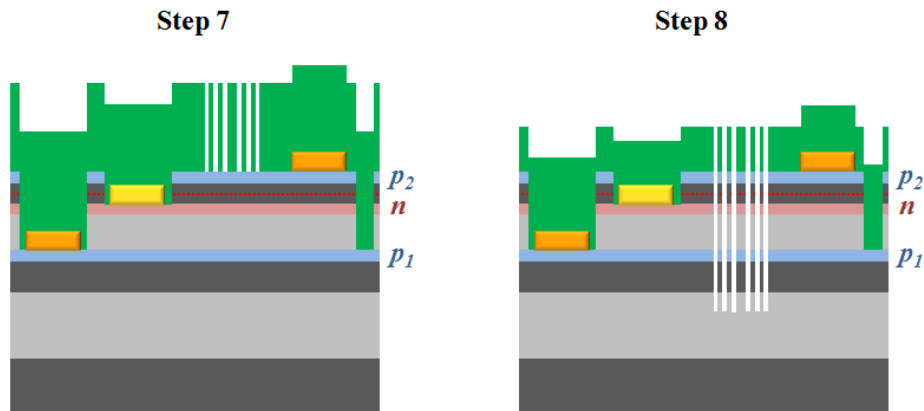
Fig. 7.20 Schematic illustration of the NOEMS device process flow.（Steps 7–8）

➢ **Releasing of double-slab PCC**

Step 9: Release the double-slab PCCs with HF 10% solution for ~ 20sec, followed by a 1 minute 85 ℃ hot isopropanol bath.

Step 10: Remove the SiN hard mask with CF_4 RIE (GP-RIE).
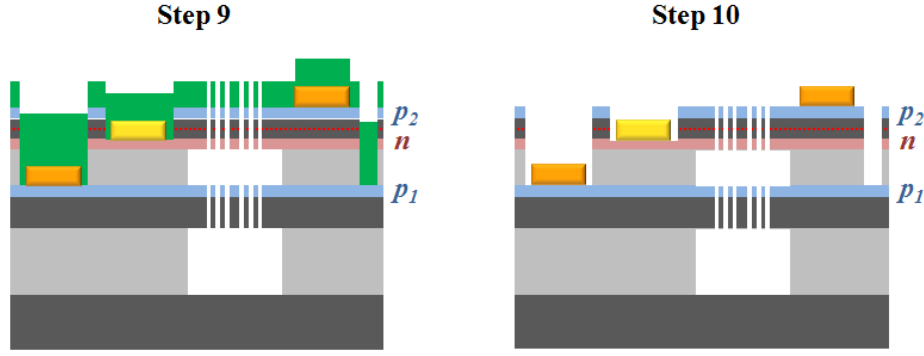
Fig. 7.21 Schematic illustration of the NOEMS + Stark Tuning device process flow.（Step 9–10）

7.4 Preliminary results of the tuning of a double-slab NOEMS device

In the first stage of this work, one NOEMS device was found to provide a 20 nm tuning range in the electromechanical tuning of the double-slab PCC at room temperature. Fig. 7.22 shows SEM images of the device (denoted as device 'M'). Two pairs of contacts were fabricated to enable the electromechanical tuning of the double-slab L3 PCCs and the Stark tuning of the excitonic energy of the QDs (Fig. 7.22 (a)). In the center of the device, the double-slab PCC with the same design as described in Ref. [1] was fabricated (Fig. 7.22 (b)).
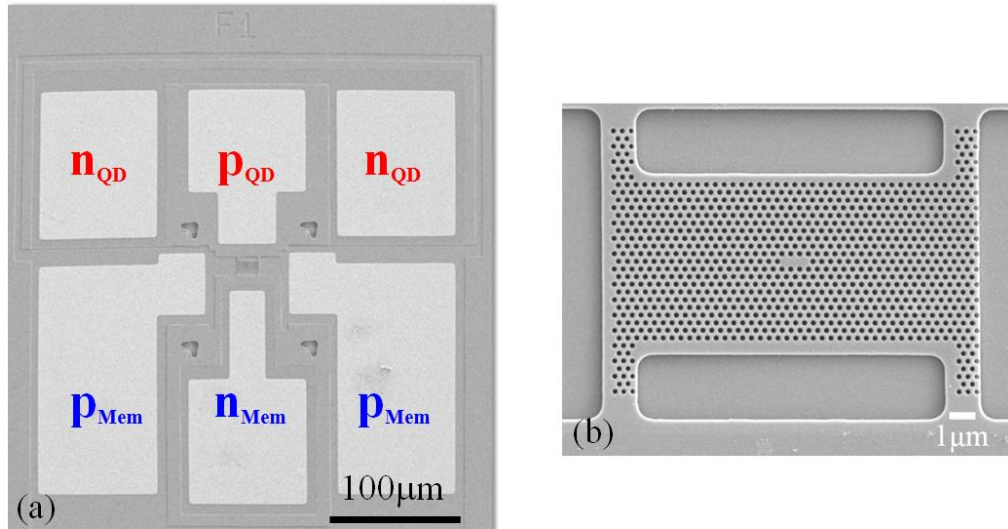
Fig. 7.22 SEM images of device M. (a) Outlook of the whole device. The letters indicate the type (n or p) of the contact and denote the belongingness of the contacts to the according diodes (Membrane diode or QD diode). (b) Zoomed view of the L3 cavity on the top membrane.

The electromechanical tuning of the device was performed in the 'General' probe station described in Section 2.3.6.1. A reverse bias voltage (denoted as U_{RM}, $U_{RM} = U_{N\text{-Mem}} - U_{P\text{-Mem}}$) was added to the Membrane diode (Fig. 7.23 (a)).
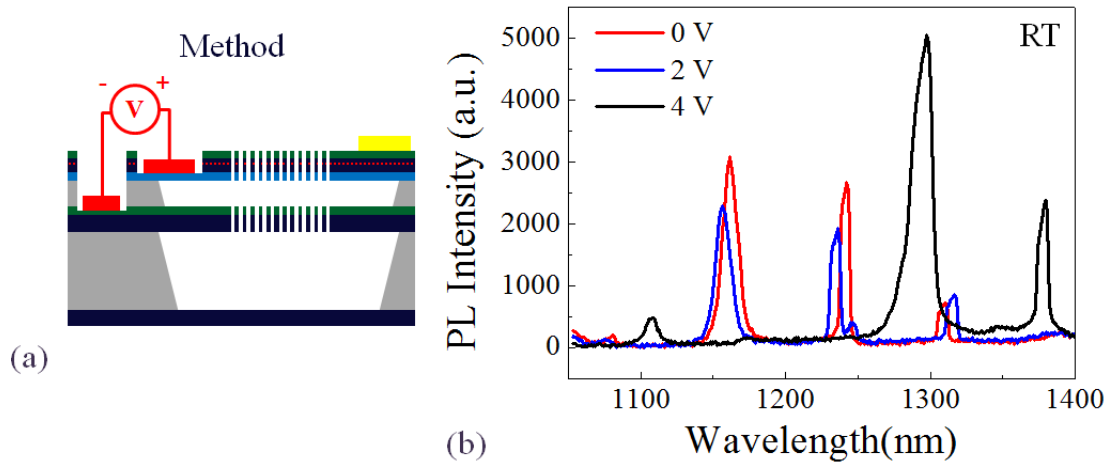
Fig. 7.23 (a) Schematic illustration of the experimental configuration when reverse bias is applied to the membrane diode. (b) RT PL spectra of the cavity modes from the double-slab PCCs of the device measured at different DC bias voltage of the membrane diode.

When U_{RM} was increased from 0 V to 2 V, the blue shift of two asymmetric (AS) modes (by ~ 5 to 6 nm) and the red shift of one symmetric mode (by ~ 6 nm) were observed. Further increasing of the U_{RM} to 4 V irreversibly changed the mode profile in the spectrum. (Fig. 7.23 (b))

As shown in Fig. 7.24 (a), in the device M, the upper membrane buckled upwards. After the electromechanical tuning at U_{RM} = 4V, the configuration of the upper membrane was found to change from buckling upward to downward without being collapsed (Fig. 7.24 (b), (c)) This observation corresponds well with the sudden change in the spectrum.
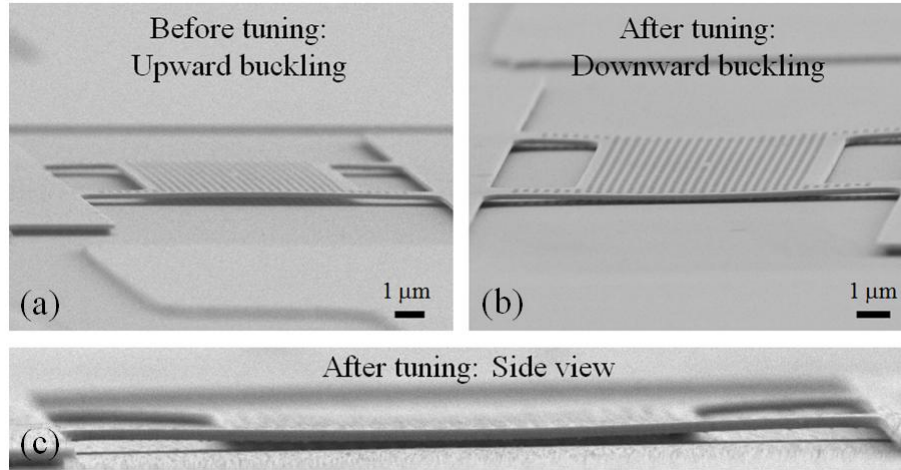
Fig. 7.24 SEM images of device M before (a) and after (b) & (c) the electromechanical tuning.

Interestingly, the downward-buckled device M was still electromechanically tunable under reverse bias. By varying U_{RM} from 0.2 V to 1.8 V, the reproducible blue shifting of two AS modes and the red shifting of two S modes were clearly observable in the spectra. In addition, the wavelength of one S mode shifted by 20 nm from 1351 nm to 1371 nm, which was a record range for the electromechanical tuning ever reported on similar devices before. (Fig. 7.25) The reason

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for the large tuning range without collapsing was not clear yet. It may be related to the internal stress induced buckling effect. (Section 6.2)
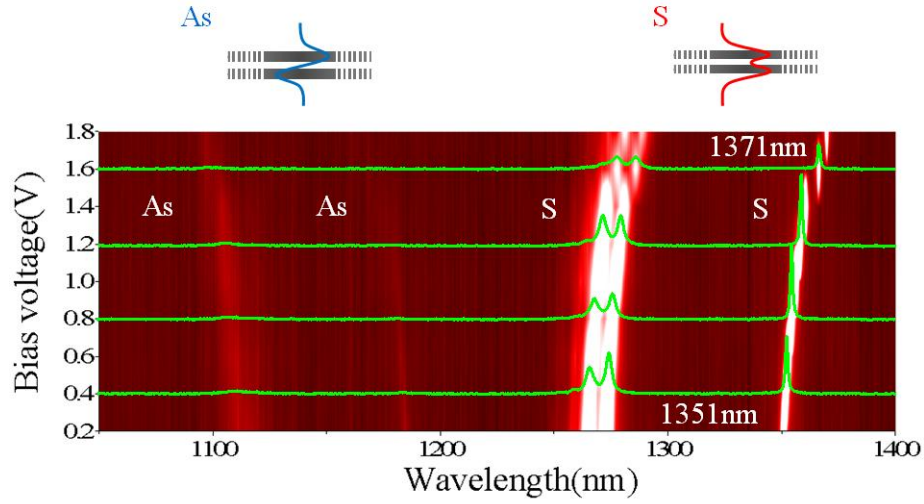
Fig.7.25 RT electromechanical tuning of device M when the reverse bias voltage U_{RM} was changed from 0.2 V to 1.8 V. The type of mode (AS or S) is indicated.

The 'mPL+PS' experimental setup (Section 2.3.6.2) was not available when device M was fabricated. The sample was always measured in air and exposed to air for > 2 months in storage. Probably due to the moisture and temperature variation in the environment, device M got contaminated and collapsed. (Fig. 7.26)
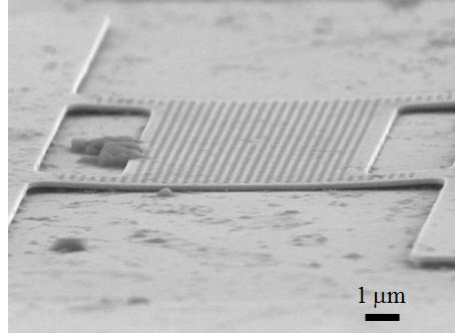
Fig.7.26 SEM image device M after collapsing due to environment reasons.

When the 'mPL+PS' setup became available, low-temperature measurements were performed on device M to characterize the Stark tuning behavior. At 10 K, when the voltage U_{QD} ($U_{QD} = U_{P\text{-}contact\_QD} - U_{N\text{-}contact\_QD}$) across the QD diode increased from - 0.9 V to 0.6 V, the excitonic emission lines of the QDs blue shifted by about 10 nm (corresponding to ~ 6.7 nm/V tunability). (Fig. 7.27) This result shows similar Stark tuning characteristics as it has been described in Ref. [5], indicating a decreasing In concentration from the top to the bottom of the QDs grown at TU/e.

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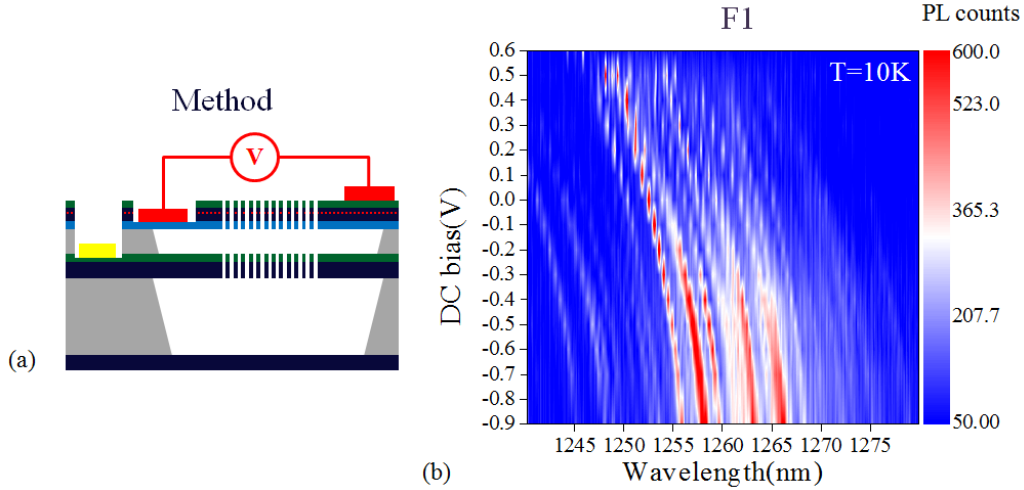
Fig. 7.27 Schematic illustration of the experimental configuration when Stark tuning was performed to the QD diode. (b) LT μPL spectra for the Stark tuning of excitonic lines of QDs at different DC bias voltages on the QD diode.

7.5 Independent control of the exciton energy and of cavity mode wavelength in a photonic crystal

In this section, the result of independent control of the QD exciton energy via the Stark effect and the electromechanical tuning of the cavity wavelength of a double PCC is discussed. The measurements described in section were performed in the 'mPL+PS' setup with the collaboration of Francesco Pagliano.

The sample for the fabrication is denoted as sample 'F' (sample growth series number: Z763). It was grown at TU/e by Yongjin Cho, Frank van Otten and Tian Xia. The sample has growth-related oval defects with a number density of ~ 3 defects/device. The defects were tentatively assumed to be threading dislocations. During the wet chemical etching, the defects acted as tubes, which guided the flow of etchants from the top p-GaAs layer to the GaAs buffer layer in the bottom of the sample. Fig. 7.28 shows an SEM image of a cleaved defect on the device before etching of the PCCs with ICP. It can be seen that contact metals cover the sidewalls and may short-circuit different doped layers. This produces problems in the electrical contacting of the devices, as discussed below.
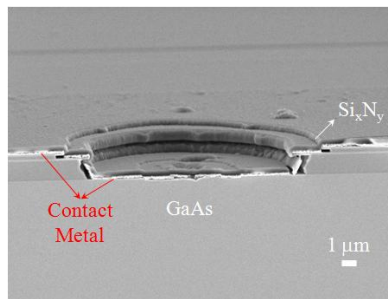
Fig. 7.28 SEM image of a cleaved defect on the device before etching of the PCCs with ICP.

7.5.1 Electrical probing of the devices

Probe configurations

To apply DC bias voltages on the two diodes of the device, initially, two standard GGB RF (up to 40 GHz) Picoprobes (model number: P-14-5172-56) were used. The probe have a G-S-G 3-finger configuration and the lateral pitch between two adjacent fingers is 100 μm. Due to the 'p-i-n-i-p' vertical configuration of the device structure, the device structure can be simplified as two p-i-n diodes with a shared n-layer. We cannot use the normal configuration (Fig. 7.29 (a)) when measuring with two probes, because the external circuit will short-circuit the two grounds of the probes. Instead, as a solution, a shifted probe configuration (Fig. 7.29 (b)) for the Probe$_M$ can be used. In this case, one G-finger of the Probe$_M$ was manually bended upwards and used as a G-S 2-finger probe. Francesco Pagliano performed the handwork of the 'finger' bending. The G-finger of the Probe$_M$ was placed on the n-contact of the membrane diode by shifting the lateral position of the probe.
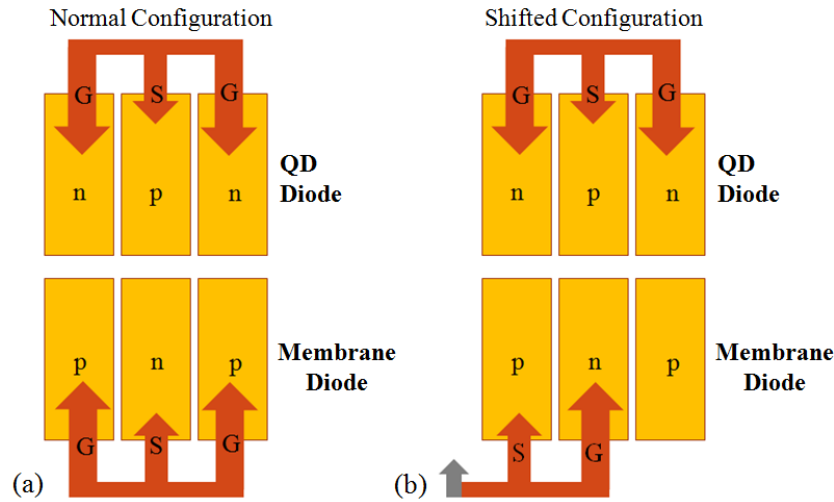
Fig. 7.29 Schematic illustrations of the normal probe configuration (a) and the measurement configuration (b) of the two G-S-G probes. The grey finger in (b) denotes the bended G-finger of the probe.

Defect induced current leakage problem

However, abnormal I-V characteristics were observed in the shifted configuration. In the measurement, the Probe$_{QD}$ was not contacting the QD diode. A difference in the I-V curves of the membrane diode when the Probe$_M$ was placed in the 'normal configuration' and the 'shifted configuration' was found (Fig. 7.30 (a)). The I-V curve of the membrane diode in the 'shifted configuration' and the semi-log plot of it (Fig. 7.30 (b), black curve) resembled well with that of a standard diode with a parallel resistance (Fig. 7.31 (d), solid curve).

By subtracting the I-V curve of the 'normal configuration' from that of the 'shifted configuration' and extracting the slope of the resulting curve, the resistance of the parallel resistor was estimated. Its value (denoted as R$_D$) was calculated to be in the range of 50 kΩ to 80 kΩ.
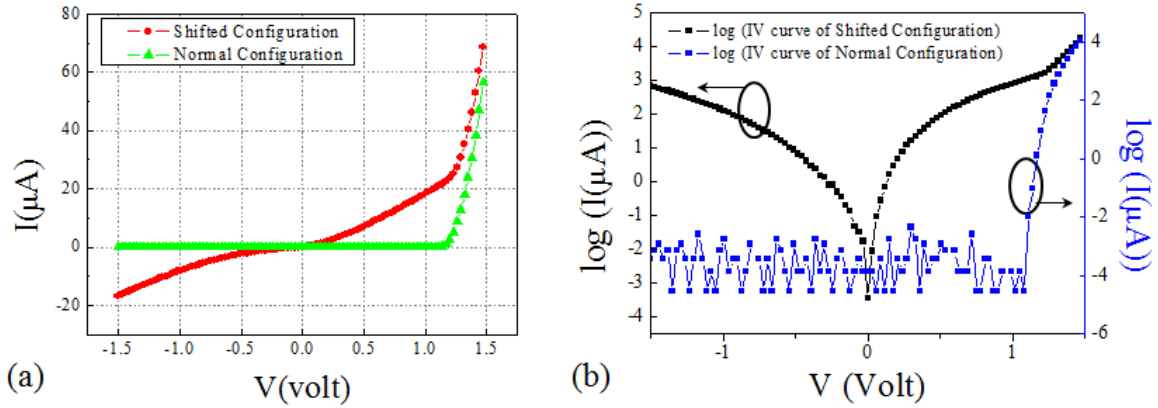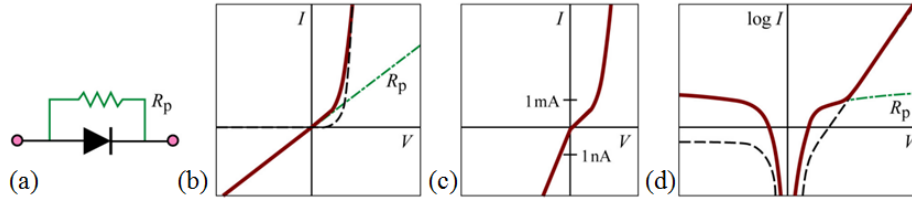
Fig. 7.30 (a) I-V curves of the Membrane diode when the Probe$_M$ was placed in the 'normal configuration' and the 'shifted configuration'. (b) Semi-log plot of the I-V curves in (a).

Diode with parallel resistance (shunt): According to Kirchhoff's current law, the currents through diode and resistor add up. Note that the forward "hump" seen on the semi-logarithmic plot has about the same level as the reverse saturation current. This is a characteristic by which a shunt can be identified.

Fig. 7.31 (a) Schematic illustration of a diode with parallel resistance. (b) I-V curves of the composite device (solid line), the ideal diode (dashed line), and the resistor (dot-dashed line). (c) I-V curve of the composite device (solid line). (d) Semi-log plot of the I-V curves of the composite device (solid line), the ideal diode (dashed line), and the resistor (dot-dashed line). [6]

The reason for observing the difference of the I-V curve at different probe configuration was tentatively attributed to the contact of the sample with two metallic sample clamps of the 'mPL+PS' setup. In the setup, the two grounded sample clamps were used to fix the sample to the sample holder by clamping the sample from the surface (in our case, the top p-GaAs). When the Probe$_M$ was in the 'normal configuration', the bottom p-GaAs layer was grounded and was at the same electrical potential as the top p-GaAs layer. When the Probe$_M$ was in the 'shifted configuration', the bottom p-GaAs layer was connected to the S-finger of Probe$_M$. If there was a resistance connecting the bottom p-GaAs layer and the top p-GaAs layer (which was grounded by the sample clamp), the I-V curve of the Membrane diode would be influenced and modified.

To verify this assumption, the author used a special electrical isolating tape (Kapton Tape [7], [8]) to electrically isolate the contact between the metallic clamp and the top p-GaAs layer of the sample. The handwork of coating the Kapton tape to the two sample clamps was performed by Francesco Pagliano. Then, similar I-V measurements in different probe configurations on the same device were performed with the tape-coated clamps on the sample surface. The I-V curve measured in the 'shifted configuration' showed the same shapes as the one measured in the 'normal configuration'. It proves the validity of the assumption of the electrical influence from the sample clamp and the existence of the parallel resistor between the top and the bottom p-

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GaAs layers. The origin for the parallel resistor may be related to connection of different contact layers on the side walls of defects. It is worth noting that the Kapton tape (with silicon adhesion) is able to work at cryogenic temperature without cracking and losing its adhesion. The Kapton tape was kept on the clamp to perform the following experiments at low temperature.

7.5.2 DC stark tuning of the QD exciton energy

At 10 K, the first series of experiments was performed to characterize the DC stark tuning of the excitonic lines of the QDs. A 780 nm CW diode laser with output power of 2.8 mW (measured on the input part of the attenuator) was used as the excitation source. An analog attenuator was used to attenuate the intensity of the input laser. As it is shown in Fig. 7.32, when the voltage U_M on the membrane diode was set to - 4V in the shifted probe configuration ($U_M = - U_{RM} = U_{P-Mem} - U_{N-Mem}$), by varying the voltage U_{QD} from 1.4 V to 0.65 V, the wavelength of the excitonic emission lines in the spectra red shifted by ~ 3 nm (Fig. 7.32 (a)). When the excitonic line passed through the cavity mode, the Purcell enhancement of the excitonic emission intensity was clearly observed, indicating a good QD-PCC coupling (Fig. 7.32 (b)). By fitting the curve of the emission energy of the QD excitonic lines as a function of the DC bias field on the QDs with the function of $E = E_0 + pF + \beta F^2$, the permanent dipole moment p and the polarizability β were estimated to be p ~ 3.68×10^{-25} C m and β ~ - 1.2×10^{-35} Cm^2(kV)$^{-1}$. (Fig. 7.33 (c))
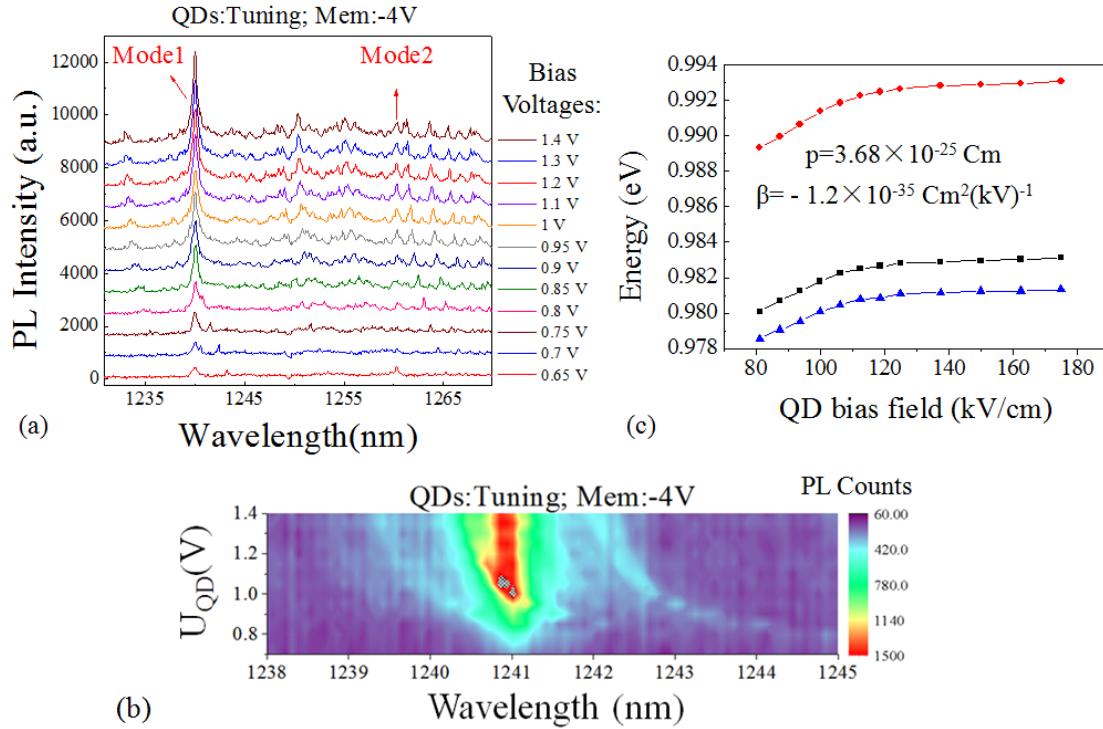
Fig. 7.32 Stark tuning results of the device at 10 K with the excitation power of 9.3 μW. (a) Stacked μPL spectra of the device when the bias voltage on the QD diode changed from 0.65 to 1.4 V. (b) Color map plot of the Stark tuning results of QD emission lines close to mode 1. (c) Emission energy of the QD excitonic lines as a function of the DC bias field on the QDs.

7.5.3 Electromechanical tuning of the double-slab PCCs

A second series of experiments was performed to characterize the electromechanical tuning of the device. Fig. 7.33 (a) shows the µPL spectrum of the two cavity modes of the device under no DC bias. In the experiment, the voltage U_{QD} on the QD-diode was set to 1.4 V. When the voltage U_M on the membrane diode changed from - 1V to - 8V, mode1 (AS mode) blue-shifted by about 3 nm and mode 2 (S mode) red-shifted by 2 to 3 nm (Fig. 7.33 (b)). In the meanwhile, the unexpected red-shifting of the QD excitonic lines was also observed. At the emission energies when the crossing of the cavity mode and the excitonic lines occurred, the enhancement of the emission intensity was observed (Fig. 7.33 (c)).
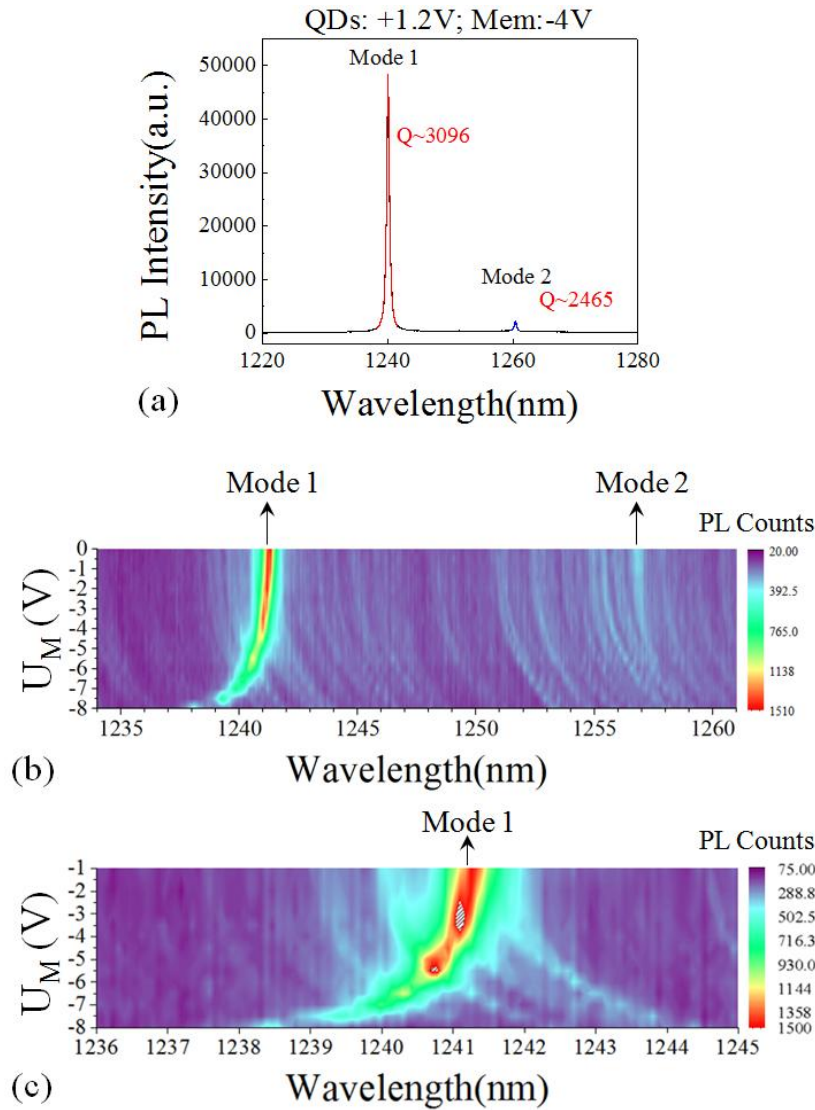
Fig. 7.33 (a) µPL spectrum of the two cavity modes of the device under no DC bias at 10 K. (b) Color map plot of the PL spectra during the electromechanical tuning of the cavity modes when U_{QD} was kept at 1.4 V. (c) Enlarged color map plot of the electromechanical tuning result of Mode 1.

7.6 Conclusion

In this chapter, the first result of the simultaneous tuning of the QD excitonic energy via Stark tuning and the cavity mode wavelength of double-slab PCCs via electromechanical tuning is shown. At 10 K, the tuning of the mode wavelength over 3 nm as well as a ~ 6 nm/V tunability of the emission wavelength of QDs are achieved and the enhancement of the excitonic emission is also observed. The full spectral tuning of the QD-cavity system opens the possibility of bringing two cavities in resonance. The optimization of the growth and fabrication recipe to achieve the fabrication of the device with limited MBE growth conditions has been introduced. The analysis of the unique static tuning phenomenon of the device has been analyzed.

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[1] L. Midolo, PhD thesis, "Electromechanical tuning of photonic crystal cavities", ISBN 978-94-6191-693-8, Eindhoven University of Technology (2013).

[2] L. Midolo, F. Pagliano, T. B. Hoang, T. Xia, F. W. M. van Otten, L. H. Li, E. Linfield, M. Lermer, S. Höfling, A. Fiore, "Spontaneous emission control of single quantum dots by electromechanical tuning of a photonic crystal cavity", *Applied Physics Letters*, vol. 101, p 091106 (2012).

[3]http://www.skyworksinc.com/downloads/press_room/published_articles/gaas_mantech_052011.pdf

[4] F. Pagliano, PhD thesis, "Dynamic control of the spontaneous emission of single quantum dots in photonic crystal cavities", ISBN 978-90-386-3713-6, Eindhoven University of Technology (2014).

[5] P. W. Fry, I. E. Itskevich, D. J. Mowbray, M. S. Skolnick, J. Barker, E. P. O'Reilly, M. Hopkinson, M Al-Khafaji, A. G. Cullis, G. Hill, and J. C. Clark, "Quantum confined stark effect and permanent dipole moment of InAs-GaAs self-assembled quantum dots", *Physica Status Solidi (a)*, vol. 178, p 269 (2000).

[6] http://www.docstoc.com/docs/75317898/Diode-tor-Inspection-of-the-diode-characteristic

Conclusions

Quantum photonic integrated circuits (QPIC), discussed in Chapter 1, enable the generation and detection of single photons in one chip and have a strong application potential in quantum information processing and communication. In QPICs, taking advantage of the atomic-like electronic states in quantum dots (QDs) and of cavity quantum electrodynamic (CQED) effects, singe-photon sources can be built and photonic crystal cavities (PCCs) can be fabricated around the QDs to control their spontaneous emission rate and increase their efficiency. Since the coupling rate between QDs and cavities is critically dependent on their relative spatial and spectral alignment, the precise control of the absolute position of QDs, of the QDs' emission energy and of the cavity mode wavelength have become critical issues for the realization of QPICs.

The work described in this thesis is dedicated to achieve the controlled coupling of semiconductor epitaxial QDs to PCC optical micro-cavities. The main achievements discussed in the thesis can be summarized as follows:

1. The optimization of epitaxial structures which can be used to produce complex nano-photonic devices structures with self-assembled low-density InAs/GaAs QDs emitting at telecommunication wavelengths. The QDs can be produced controllably and homogeneously with density in the range of $10\sim50/\mu m^2$. At low temperature (LT), the typical linewidth of single QDs emission lines was measured to be ~ 60 μeV. The emission wavelength of the QDs can be tuned from 1200 to 1270 nm (at LT).

2. The establishment of a method to create nano-patterned substrates with sub-100 nm-wide nanoholes for the growth of site-controlled quantum dots (SCQDs). The growth of site-controlled multiple InAs/GaAs QDs on pre-patterned GaAs substrates with nanohole arrays with variable hole-to-hole pitches has also been achieved as a preliminary result of the project.

3. The investigation of several native oxide desorption methods and the optimization of the In-assisted deoxidation (IAD) method, which provides pit-free and smooth GaAs surface. Single QD PL lines with a typical linewidth of ~ 0.2 nm can be observed from QDs grown at 10 nm distance from a GaAs surface with surface oxide removed under optimized IAD conditions.

4. The optimization of the design and the fabrication of a mechanical-stress-free vertically aligned double-nanobeam device. The asymmetric and symmetric modes in the PL spectra of the device and the optical spring effect were observed from the device.

5. The first experimental demonstration of the independent tuning of the QD exciton energy with a tunablility of ~ 6 nm/V and of the cavity mode wavelength in a double-slab PCC for more than 3 nm at 10 K. The enhancement of the excitonic emission when QD lines are tuned to be in resonance with cavity modes was observed.

Several subsequent steps are possible along this research line:

1. Further optimization of the growth conditions to produce single SCQDs is needed. According to the author, optimizing the growth condition of the seeding layer can be a good starting point.

2. The influence of the hydrogen assisted deoxidation (HAD) method on the optical efficiency of the QDs grown in proximity to the treated interface is worth to be investigated thoroughly as well.

3. A further optimization of the surface cleaning method needs to be done.

4. The application of the IAD method on the patterned substrate for the growth of SCQDs should be investigated.

5. Creating SCQDs on the patterned substrate by using the droplet epitaxy method can be an interesting topic for investigation.

6. The creation of site-controlled metallic nanocrystal arrays on the patterned substrate by MBE growth can be an interesting research topic, from the point of view of the author.

7. The integration of the SCQDs to nano-photonic devices, such as the NOEMS device that the author has worked on, is an important step for the scalable QPIC.

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List of Publications

JOURNAL PUBLICAITONS:

- **T. Xia**, Y. J. Cho, M. Cotrufo, I. Agafonov, F. W. M. van Otten and A. Fiore, "In-assisted deoxidation of GaAs substrates for the growth of single InAs/GaAs quantum dot emitters", accepted by *Semiconductor Science and Technology*.

- F. Pagliano, Y. J. Cho, **T. Xia**, F. W. M. van Otten, R. Johne and A. Fiore, "Dynamic controlling the emission of single excitons in photonic crystal cavities", *Nature Communications*, vol 5, p 5786 (2014).

- S. Fattah poor, T. B. Hoang, L. Midolo, L. H. Li, E. H. Linfield, J. Schouwenberg, **T. Xia**, F.W.M. van Otten and A. Fiore, "Efficient coupling of single photons to ridge-waveguide photonic integrated circuits", *Applied Physics Letters*, vol.102, p 131105 (2013).

- J. Y. Yuan, C. Y. Jin, M. Skacel, A. Urbańczyk, **T. Xia**, P. J. van Veldhoven, and R. Nötzel, "Coupling of InAs/InP quantum dots to the plasmon resonance of In nanoparticles grown by metal-organic vapor phase epitaxy", *Applied Physics Letters*, vol.102, p 191111 (2013).

- L. Midolo, S. N. Yoon, F. Pagliano, **T. Xia**, F. W. M. van Otten, M. Lermer, S. Höfling, and A. Fiore, "Electromechanical tuning of vertically-coupled photonic crystal nanobeams", *Optics Express*, vol. 20, p 19255 (2012).

- L. Midolo, F. Pagliano, T. B. Hoang, **T. Xia**, F. W. M. van Otten, L. H. Li, E. H. Linfield, M. Lermer, S. Höfling, and A. Fiore, "Spontaneous emission control of single quantum dots by electromechanical tuning of a photonic crystal cavity", *Applied Physics Letters*, vol. 101, p 091106 (2012).

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- M. Petruzzella, **T. Xia,** F.M. Pagliano, S. Birindelli, L. Midolo, Ž. Zobenica, L.H. Li, E. H. Linfield, A. Fiore, "Fully-tunable, Purcell-enhanced on-chip quantum emitters", oral presentation*, CLEO 2015, San Jose*, USA (2015).

- **T. Xia**, F. Pagliano, Y. J. Cho, L. Midolo, M. Petruzzella, F. W. M. van Otten, Z. Zhou, L. Li, E. Linfield, M. Swinkels, R. van der Heijden, and A. Fiore, "Independent control of the exciton energy and of cavity mode wavelength in a photonic crystal cavity", poster, *Physics @ FOM Veldhoven 2015* , Veldhoven, The Netherlands (2015).

- A. Fiore, S. Fattah poor, T. Hoang, L. Midolo, F. W. M. van Otten, F. Pagliano, D. Sahin, **T. Xia**, J. Beetz, M. Lermer, S. Höfling, M. Kamp, A. Gaggero, F. Mattioli and R. Leoni, "Quantum photonic integrated circuits", invited talk, *IEEE Photonics Conference*, San Diego, USA (2014).

- M. Petruzzella, **T. Xia**, S. Fattah poor, L. Midolo, F. Pagliano, Y. Cho and A. Fiore, "Towards on-chip electro-mechanically tunable single-photon sources", poster, *Scientific School in integrated photonic manipulation*, Varenna, Italy (2014).

- M. Cotrufo, **T. Xia** and A. Fiore, "Cavity QED with plasmonic-semiconductor nanostructures", poster,

Physics @ FOM Veldhoven 2014 , Veldhoven, The Netherlands (2014).

- L. Midolo, F. Pagliano, T. B. Hoang, **T. Xia**, F. W. M. van Otten, L. H. Li, E. H. Linfield, M. Lermer, S. Höfling and A. Fiore, "Controlling the emission from single quantum dots with electro-opto-mechanical photonic crystal cavities", oral presentation, *ICTON13 conference*, Cartagena, Spain (2013).

- **T. Xia**, Y. Cho, F. W. M. van Otten and A. Fiore, "Indium-assisted deoxidation of GaAs substrate towards MBE growth of site-controlled InAs quantum dots", poster, *EuroMBE conference 2013*, Levi, Finland (2013).

- S. Fattah poor, L. Midolo, T.B. Hoang, L.H. Li, E.H. Linfield, J. Schouwenberg, **Tian Xia**, F.W.M. van Otten, A. Fiore, "Funneling single photons into ridge-waveguide photonic integrated circuits", oral presentation, *Proceedings of SPIE 2013*, San Francisco, USA (2013).

- L. Midolo, F. Pagliano, T. B. Hoang, **T. Xia**, F. W.M. van Otten, L. H. Li, E. H. Linfield, M. Lermer, S. Höfling and A. Fiore, "Spontaneous emission control of single quantum dots by electrostatic tuning of a double-slab photonic crystal cavity", oral presentation, *Photonics West 2013*, USA (2013).

- F. Pagliano, F. W. M. van Otten, **T. Xia**, L. H. Li, E. H. Linfield and A. Fiore, "Ultrafast electrical control of the exciton energy for cavity quantum electrodynamics experiments", oral presentation, *CLEO conference 2013*, USA (2013).

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- S. Fattahpoor, L. Midolo, T. B. Hoang, L. H. Li, E. Linfield, **Tian Xia**, F. W. M. van Otten, and A.Fiore, "Funneling single photons into ridge-waveguide photonic integrated circuits", paper No. 8632-2, *SPIE 2013 Photonics West conference* (2013).

- **T. Xia**, Y. J. Cho, F. W. M. van Otten and A. Fiore, Indium-assisted deoxidation of patterned "GaAs substrates for MBE growth of site-controlled InAs quantum dots", poster, *Physics @ FOM Veldhoven 2013*, Veldhoven, The Netherlands (2013).

- F. Pagliano, F. W. M. van Otten, **T. Xia**, L. H. Li, E. H. Linfield, A. Fiore, ultrafast electrical control of the exciton energy for cavity quantum electrodynamics experiments, poster, *Physics @ FOM Veldhoven 2013*, Veldhoven, The Netherlands (2013).

- **T. Xia**, F. W. M. Otten, F. Zarotti and A. Fiore, "Growth and characterization of low density InAs/GaAs quantum dots towards site-controlled quantum dots emitting at 1300nm", poster, *International Nano-Optoelectronic Workshop*, Würzburg, Germany (2011).

Curriculum vita

Tian Xia (夏天) was born on July 29th 1986, in Nanjing, Jiangsu Province, China. She obtained her high school diploma from Nanjing No.1 High School in Nanjing, China. In 2007, she finished her bachelor study in Engineering at Nanjing University of Posts and Telecommunications in Nanjing, China. From 2007 to 2008, she studied for the first part of her Master in the Department of Physics at the University of Science and Technology of China in Hefei, China. In 2010, she received her Master's degree of Engineering from Shanghai Institute of Optics and Fine Mechanics, Chinese Academy of Sciences, in Shanghai, China. Since October 2010, she has been pursuing her PhD degree in the Photonics and Semiconductor Nanophysics group at the Department of Applied Physics of Eindhoven University of Technology, the Netherlands. Her research focuses on the control of coupling of semiconductor quantum dots to optical micro-cavities. Since December 2014, she works at ASML as an Application and Business Support Engineer in the Customer Support department.