Power and area efficient reconfigurable delta sigma ADCs

POWER AND AREA EFFICIENT RECONFIGURABLE ΔΣ ADCS

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List of abbreviations

SNDR Signal-to-noise-and-distortion-ratio 7

STF Signal transfer function 27

VLSIC VLSI Circuit 9

WBAN Wireless body area networks 1

WSN Wireless Sensor Network 3

ΔΣM Delta Sigma Modulator 11

List of symbols

$\frac{\mathbf{k(t)}}{\mathbf{2^B-1}}$ *B*-bit DAC feedback signal normalized with respect to V_{ref} 51

A_c Capacitor area 44

a_i Gain coefficient of the ΔΣ loop 36

B ΔΣM internal quantizer resolution 7

C Unit capacitor of the SAR DAC array in a SAR quantizer 60

C_A Capacitance per unit area for a given technology 44

C_{eq} Capacitive equivalent load of the OTA 48

C_f Feed-forward capacitor 78

c_i Feed-forward coefficient of the ΔΣ loop 36

C_I Integrating capacitor 48

C_{inv} Equivalent input capacitance of a minimum size inverter for a given technology 63

C_L Capacitive output load of the SC integrator 50

CLK Clock signal 59

C_{LS} Capacitor of the SC level shifter in a flash quantizer 58

C_p OTA input parasitic capacitance 50

C_s Sampling capacitor 7

C_{TOT} Total capacitance commuting in the ΔΣM 57

C_u Capacitive unit element of the input DAC 43

e Quantization error 26

F Ratio between I_{bias} and I_{tail} 55

f_s ΔΣM sampling frequency 49

$g_{m,in}$ OTA input transconductance 50

g_q Quantization gain 27

1 Introduction

This chapter introduces the design of reconfigurable analogue-to-digital converters as focus of this thesis. Applications, problems and opportunities with respect to the state of the art are identified, and performance criteria, i.e. power- and area-efficiency, are presented. Also, the scientific aim and the scope of the thesis are clarified, together with the explanation of our design approach and an overview of the original contributions.

1.1 Background

Recently, there has been a growing interest in the research community and industry in the development of ultra-low power devices for various applications in the domain of wireless body area networks (WBAN). Although extensive measurement of physiological information is nowadays possible, the monitoring is generally limited to short time intervals and often to situations difficult to realize in normal life, like lying supine and sedated, or performing artificial exercise tests. The emergence of miniaturized sensors offers great promise for continuous and unobtrusive wireless monitoring, which would allow for a more timely response to any potential warning signs. The WBANs will be intelligent, context aware sensing architectures for the development of pervasive monitoring systems [1].

The basic concept of WBAN is a network of miniaturized, low cost and wireless wearable sensors that are energy-autonomous and capable of self-organizing into a collaborative network.

The design of sensor node hardware is constrained by several factors. To be energy-autonomous, nodes must be powered entirely by an energy harvesting source. This places demanding low-energy requirements on the constituent circuits [2]. It is also desirable to have sensors with redundant data to extract reliable information from biological data that are often prone to errors [1]. To give an example, different biopotentials need to be acquired and combined to define the overall health status. For instance, ECG (Electrocardiogram) signals are cross-correlated to respiration data and affected by motion artefacts, and EMG (Electromyogram) signals can be used to detect motion artefacts.

Fundamentally, the architecture of an intelligent sensor node consists of a sensor and a sensor front-end, an analogue-to-digital converter (ADC), a digital

signal processor (DSP), and a short range radio. The focus of this work is the design of an ADC suitable for sensor nodes and specifically for biopotential signals. Based on the considerations above, several key features need to be implemented:

1. The ADC has to be power-efficient to comply with the limited power budget of wireless sensors.
2. The ADC has to be area-efficient to match to the small form factor of modern sensor nodes and decrease costs.
3. The ADC should offer high-resolution and linearity to enable accurate conversion of small amplitude signals in the vicinity of strong interferences.
4. The ADC must be reconfigurable to adapt to heterogeneous biopotential signals, which are characterized by different amplitude levels and frequency ranges.

For instance, we can apply reconfigurability to the readout of biopotential signals (EEG, ECG, and EMG) according to the specifications of Table I (see also Table X in Section 4.2.2).

TABLE I
EXAMPLE OF SPECIFICATIONS FOR RECONFIGURABILITY

	ENOB	*BW* [Hz]	Target application
High resolution/ low *BW* (HRLB)	16	256	EEG, ECG
Medium resolution and *BW* (MRMB)	14	2048	EMG
Low resolution/ high *BW* (LRHB)	12	16 k	Hearing-aids

Considering the working modes of Table I, it is clear that, to meet the required performance and ensure low power consumption, a high-resolution reconfigurable ADC is needed which can change its resolution and adjust its power according to the requirements of different physiological signals.

The concepts of reconfigurability, power- and area-efficiency will be explained in detail in Section 1.1.1 and Section 1.1.2, respectively. Subsequently, the state-of-the-art of reconfigurable ADCs will be summarized in Section 1.1.3.

1.1.1 Reconfigurability

An increasing number of applications require the acquisition of signals with a wide range of bandwidths and with varying resolution. These applications range from multi-standard communication systems to sensor systems in and around the body.

In mobile communication systems, the most advanced smart phones already support a large number of standards. The trend toward an ever-increasing flexibility of use demands radio transceivers that can operate complying with a variety of standards [3]. The multi-standard transceivers must fulfil the performance requirements of each standard separately and, in some cases, concurrently. For instance, wireless hand-held terminals may use simultaneously Bluetooth and GSM standards in a voice transmission using Bluetooth headphones. At the same time, the mobile terminal can be used to check the e-mail via a WLAN/UMTS data network [4].

In biomedical applications, a high recurrent design cost of wireless sensor networks (WSNs) is due to tailoring the sensors to a specific application. Ad hoc deployment will be possible if sensor nodes become fault tolerant and able to cope with different biosignals [2]. Sensors that monitor physiological parameters have indeed to process signals that have different amplitude levels and frequency ranges. Besides, the characteristics of the same physiologic signal may vary with time according to the body activity.

In order to satisfy the above mentioned system-level requirements, flexible analogue mixed-signal circuits and systems are needed. In multi-standard mobile terminals and wireless sensor nodes the most challenging part in the hardware design is probably the ADC interface. The ADC must indeed handle with flexibility a wide range of signals at varying sampling rates and resolutions, a feature which is difficult to implement in the analogue domain. Moreover, as power autonomy is still a major challenge in both these applications, the ADC must meet different design specifications while keeping the lowest possible power consumption.

To meet all these requirements, *reconfigurable* ADCs are needed that can change their resolution and bandwidth (*BW*) and adapt their power consumption accordingly.

Several ADC architectures (like algorithmic, flash, pipeline, and delta–sigma converters) have been discussed in literature. Each of these architectures, however, can work optimally only for a specific range of resolution and *BW*. Fig. 1 shows different types of state-of-the-art ADCs with different input signal bandwidth $f_{snyq} = 2 \cdot BW$ and different resolution [5]. Looking at Fig. 1 it can be noticed that pipeline converters are typically used at low-to-medium resolutions and medium-to-high speeds, while delta-sigma (ΔΣ) and incremental converters are mostly exploited for medium-to-high resolution applications in the low-to-medium frequency range. Flash and folding ADCs are suitable for applications requiring very large bandwidths and relatively low resolution, while extended counting ADCs are used for medium bandwidth and medium-to-high resolution applications [6]- [7]. SAR and VCO-based ADCs most commonly range in resolution from 8 to 14 bits. From this analysis, it is clear that a conventional ADC with fixed topology and parameters cannot efficiently convert signals over a wide range of bandwidths at varying resolutions while optimizing power consumption [3].

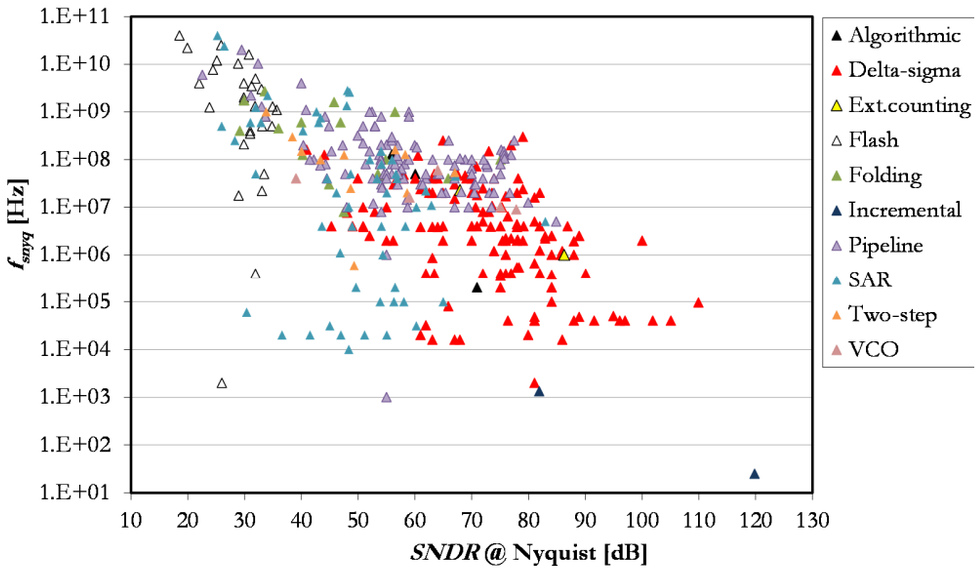


Fig. 1. Conversion bandwidth versus *SNDR* performance of state-of-the-art ADCs.

A simple approach to reconfigurability would be to employ an array of ADCs, each one customized to work for a narrow range of resolution and input *BW*. Such a converter implementation, however, would require many ADCs and would result in a significant increase of the overall silicon area. As demonstrated by recent reconfigurable implementations, a power- and area-efficient approach to reconfigurability is possible using one single ADC able to achieve different resolution and bandwidth with minimal area overhead. However, reconfigurable solutions are still not competitive with state-of-the-art point- solution ADCs in terms of performance and power efficiency.

Reconfigurable ADCs reported in literature feature reconfiguration at different levels:

- *Algorithm-type reconfiguration*

For each given combination of resolution and *BW*, the most suitable ADC algorithm is chosen to minimize the power consumption. For instance, at low-to-medium resolutions and medium-to-high speeds a pipeline algorithm is adopted, at high resolutions and low-to-medium speeds the ΔΣ algorithm is used [8]- [9]. ADC topologies are indeed composed of similar basic components such as op-amps, comparators, switches, and capacitors. Reconfigurability can thus be implemented by using these analogue building blocks in conjunction with configurable switches. A drawback of this approach is that switch parasitics often lead to performance degradation.

- *Bandwidth reconfiguration*

Assuming a constant supply voltage, the power consumption of both digital and analogue circuits (in weak inversion) is directly proportional to their operating speed. In the case of digital circuits (or fully-dynamic analogue implementations), the power automatically scales with the operating frequency f_s according to $\frac{1}{2} f_s C V_{DD}^2$. The *BW* reconfiguration approach can thus be easily applied to mostly-digital ADC architectures [10]- [11]. In the case of analogue circuits, the power does not scale automatically with the sampling rate as static currents are used to bias analogue transistors in their operating region. A common method to achieve a scalable analogue power is to adaptively scale transistor bias currents with the sampling rate [12]- [13]. However, this approach can be affected by implementation problems. For a wide variation of sampling rates, indeed, the bias currents must vary largely, even by more than one order of magnitude. MOS transistors can thereby be driven into deep weak inversion, where they are more susceptible to mismatch and variability [2]. Alternatively, power scalability can be achieved in burst mode by performing conversions at a constant, maximum rate and by power-gating analogue

circuits when a reduced sampling rate is desired [14]. This approach requires, on the other hand, careful design to minimize the bias-up time in the transition between sleep and active mode.

- *Algorithm-parameter reconfiguration*

In this approach the type of ADC algorithm is kept the same and the ADC is modified at the architectural level by changing the parameters which determine its resolution. The most common approach consists in using switchable blocks which are opportunely enabled to increase the ADC performance and disabled to save power. The advantage of this reconfigurability approach is that the bias conditions of the ADC can be kept mostly unchanged, mitigating the need of tuning the bias of analogue building blocks [15]. In pipeline ADCs like [3] and [16] the size of the capacitors and the length of the pipeline can be modified. In ΔΣ architectures the parameters determining the final resolution can be adapted to the target resolution: the number of stages (in cascade architectures), the filter order (N) , the quantizer resolution (B) and the size of the sampling capacitors (C_s) are opportunely changed to achieve the required signal-to-noise-and-distortion-ratio (*SNDR*) [17]-[18]. In successive approximation (SAR) ADCs, the architecture of the internal logic, the digital-to-analogue converter (DAC) and the comparator are changed according to the target resolution [19].

By using and combining these techniques, more and more ADC programmability has been achieved during the last years. For the future, it is expected that this trend will continue until a large resolution and bandwidth space is covered with minimal power at each performance level. In this respect, the reconfigurability trend will lead new opportunities to ADC design, but will also have to cope with new challenges. An important challenge is for example the fact

that nanometer CMOS processes are optimized for digital circuitry and high speed, but can be disadvantageous for analogue circuits and for low-frequency applications. On the other hand, the use of oversampling strategies for the analogue signal processing facilitates the integration of reconfigurable ADCs in modern IC technologies. ΔΣ ADCs, for instance, use redundant temporal data to reduce the quantization noise. This approach results in high-performance, robust ADCs which are able to exploit the inherent time resolution of modern technologies also for low frequency signals.

1.1.2 Power-efficiency and area-efficiency

As stated above, ADCs are among the most challenging parts of multi-standard mobile transceivers and biomedical sensor nodes and, as the number of applications is continuously increasing, it is expected that the flexibility required to reconfigurable ADCs will be larger and larger.

A reconfigurable ADC must offer two main characteristics, power-efficiency and area-efficiency.

A reconfigurable ADC is power efficient if the power-efficiency of the ADC can be kept constant and optimal as much as possible, despite the change in desired resolution and bandwidth. This requires that the ADC is scalable in terms of resolution, bandwidth and power.

In literature the power-efficiency of analogue-to-digital converters is commonly quantified using the Figure of Merit (*FoM*) [20]:

$$FoM_1 = \frac{P_{TOT}}{2 \cdot BW \cdot 2^{ENOB}} [\mathrm{J/c.s.}] \quad (1)$$

where P_{TOT} is the total power consumption and BW is the input signal bandwidth; $SNDR_{dB}$ is the signal-to-noise-and-distortion ratio expressed in dB and the effective number of bits is $ENOB = \frac{SNDR_{dB} - 1.76}{6.02}$.

In (1) the power per Nyquist sample $P_{TOT}/2 \cdot BW$ is normalized by the effective number of quantization steps 2^{ENOB}. This is based on the assumption that doubling precision would double power, which finds only empirical justification [20]. Moreover, the 2x relationship between precision and energy is not valid for high-resolution designs. Fig. 2 shows a scatter plot of state-of-the-art ADC designs, presented at the IEEE International Solid-State Circuit Conference (ISSCC) and the VLSI Circuit (VLSIC) Symposium [5]. It represents the power per Nyquist sample $P_{TOT}/2 \cdot BW$ against the achieved $SNDR$ [21]. The FoM in (1) is included as a straight line for the numerical example of 100fJ/c.s., while the FoM in (2) is included as a dashed line for the numerical example of 170 dB.

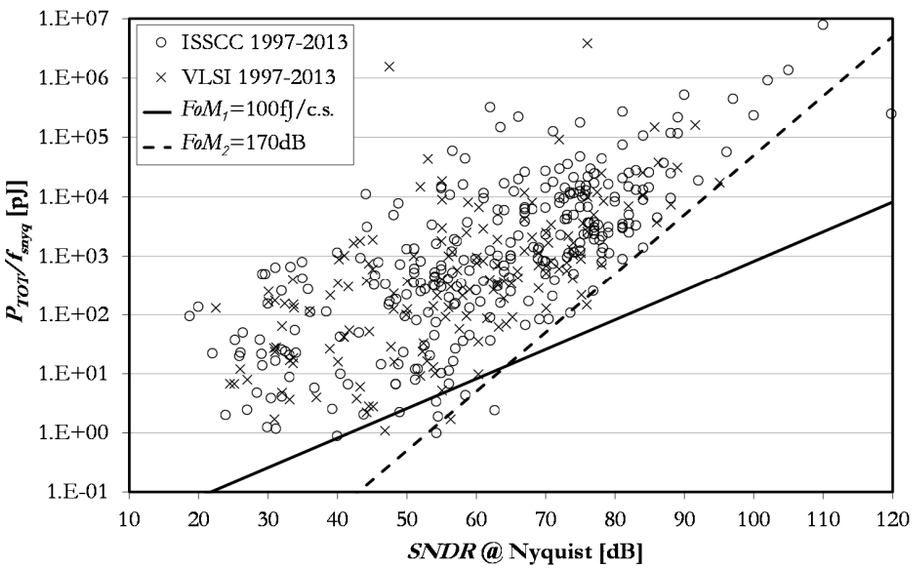


Fig. 2. Power-efficiency versus $SNDR$ performance of state-of-the-art ADCs.

Fig. 2 shows that state-of-the-art high-resolution designs (*SNDR*>75dB) do not obey the 2x increase per bit implied by (1). In theory, indeed, if a converter is purely limited by thermal noise, its power quadruples per added bit [22]. In this case, a different *FoM* is used, defined as [23]:

$$FoM_2 = DR_{dB} + 10\log_{10}\frac{BW}{P_{TOT}}[\text{dB}] \quad (2)$$

where DR_{dB} is the dynamic range of the converter. This equation is represented in Fig. 2 as a dashed line for the numerical example of 170dB.

Given the controversy about the definition of a Figure-of-merit for ADCs, the following twofold approach is chosen here.

When we compare data across a large range of architectures and resolutions, we avoid using (1) or (2). We represent instead the ADCs power performance in terms of power per Nyquist sample $P_{TOT}/2{\cdot}BW$ versus *SNDR*, like in the plot of Fig. 2 [21].

When we benchmark implementations targeting comparable resolutions, we employ FoM_1 or FoM_2 depending on the fundamental limit for the resolution of those ADCs. If the ADC is matching limited (low-to-medium *SNDR*) we will use FoM_1, if the ADC is thermal-noise limited (medium-to-high resolution) we will use FoM_2. In the rest of this work, we will refer to the expression in (1) simply as *FoM* as this expression is broadly used here.

A reconfigurable ADC is called area-efficient if the reconfigurability implies negligible area overhead with respect to point-optimized solutions. The area-efficiency is evaluated by comparing the area occupied by the reconfigurable ADC with the area of point-optimized implementations that achieve similar maximum

SNDR. To compare different designs, we will plot their reported area against the achieved *SNDR* [21].

In Section 1.1.3 the power-efficiency and the area-efficiency of some state-of-the-art reconfigurable ADCs is evaluated.

1.1.3 State-of-the-art reconfigurable ADCs

As an illustration of state-of-the-art reconfigurable ADCs, Fig. 3 plots some of the most recent reconfigurable designs in the plane power per Nyquist sample P_{TOT}/f_{snyq} ($f_{snyq} = 2 \cdot BW$) versus resolution. Data are displayed as curves connecting the points associated to their different modes of operation. Reconfigurable ADCs are compared in terms of power-efficiency with state-of-the-art tailored designs already represented in [5]. Reconfigurable Nyquist ADCs ([16], [19], [24], [25], [26]) are displayed as black curves, while reconfigurable oversampling ADCs ([17], [18], [27]) are shown as red curves. Please note that the power reported for oversampling ADCs is only the power dissipated by the ΔΣ modulator (ΔΣM) blocks. Both *FoM* lines of Fig. 2 are included, corresponding to the trends shown in equations (1) and (2). They are plotted as a straight line and as a dashed line for the numerical value of 100fJ/c.s. and 170dB, respectively.

On the one hand, it can be noted that ΔΣ architectures (for instance [18] or [27]) are able to cover wider *SNDR* regions than Nyquist-rate ADCs (see [16] or [25]). Thanks to the oversampling technique, indeed, ΔΣ ADCs are able to trade off speed for resolution which offers inherent reconfigurability [27]. Moreover ΔΣ ADCs are able to filter the noise (noise shaping) and push it out of the signal band. The use of these analogue signal-processing strategies results in high-performance, robust ADCs, which have lower sensitivity to circuit imperfections than Nyquist-rate ADCs.

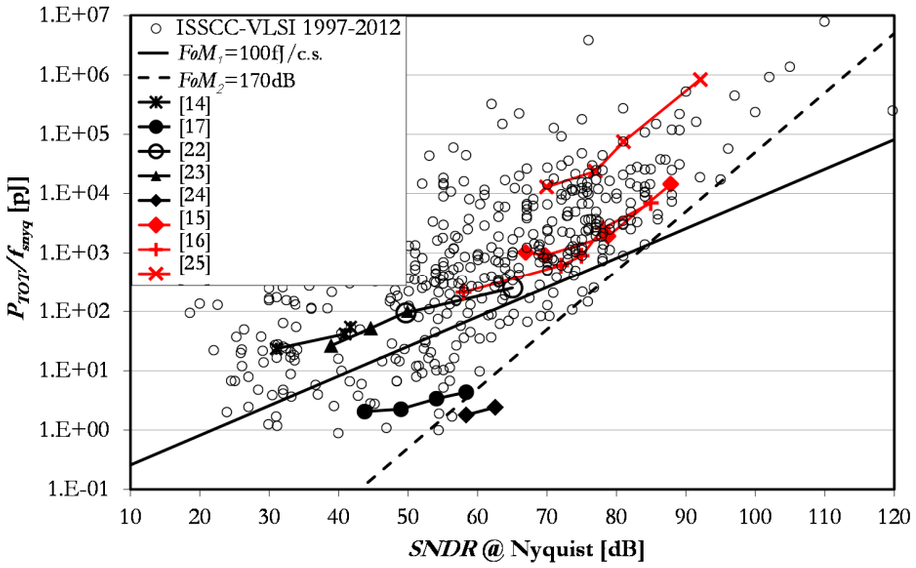


Fig. 3. Power-efficiency versus *SNDR* performance of state-of-the-art tailored (ISSCC-VLSI 1997-2012) and reconfigurable ADCs.

These properties make it easier to change resolution and speed without significant performance degradation and have motivated the use of ΔΣ approaches in the majority of reconfigurable ADCs reported so far [4].

On the other hand, Fig. 3 shows that reconfigurable Nyquist ADCs are always matching-limited designs, and they follow the trend implied by FoM_1 for different configurations. ΔΣ designs, instead, do not follow the same FoM_1 trend in all modes of operation. At low-to-medium resolutions (*SNDR*<75 dB) they are matching-limited as well. But, for higher resolutions, reconfigurable ΔΣ architectures break away from the FoM_1-line and follow the FoM_2-line. This fact has two main reasons:

- Firstly, beyond the threshold *SNDR* of 75dB most state-of-the-art ADCs can be considered to be limited by thermal noise [21]. Therefore, their power tends to

increase more than 2x per bit, until it reaches the 4x increase per additional bit associated to the FoM_2-line.

- Secondly, although oversampling plus noise shaping helps in relaxing some specifications of ΔΣ analogue building blocks, ΔΣ still share some design constraints of Nyquist converters. More specifically, the signal swing at the OTAs output can be large, especially in single-bit topologies, or if loop coefficients are not specifically chosen to reduce integrators' output swing. Also high oversampling ratios (*OSR*s) pose challenging specifications to the settling speed of the OTAs [28]. Moreover, high linearity is required in the input DAC when multi-bit quantizers are employed. Indeed, as the errors of multi-bit DACs are injected at the modulator input, the corresponding non-linearities are not mitigated by the noise shaping. The linearity of a multi-bit modulator will be thus no better than that of the multi-bit embedded DAC and the latter must be designed to reach the linearity targeted for the whole ΔΣM [29]. These technology constraints strongly affect also the power-efficiency of our implementations, as it will be shown in Section 5.

We can now focus on the area-efficiency of state-of-the-art reconfigurable ADCs. As discussed before, a reconfigurable ADC is called here area-efficient if its area is comparable to the area of custom ADCs targeting the same maximum *SNDR*. Fig. 4 shows the same reconfigurable designs as in Fig. 3 in the area versus *SNDR* plane. The designs from the IEEE ISSCC and the VLSIC Symposium are plotted on the same plane for comparison [21].

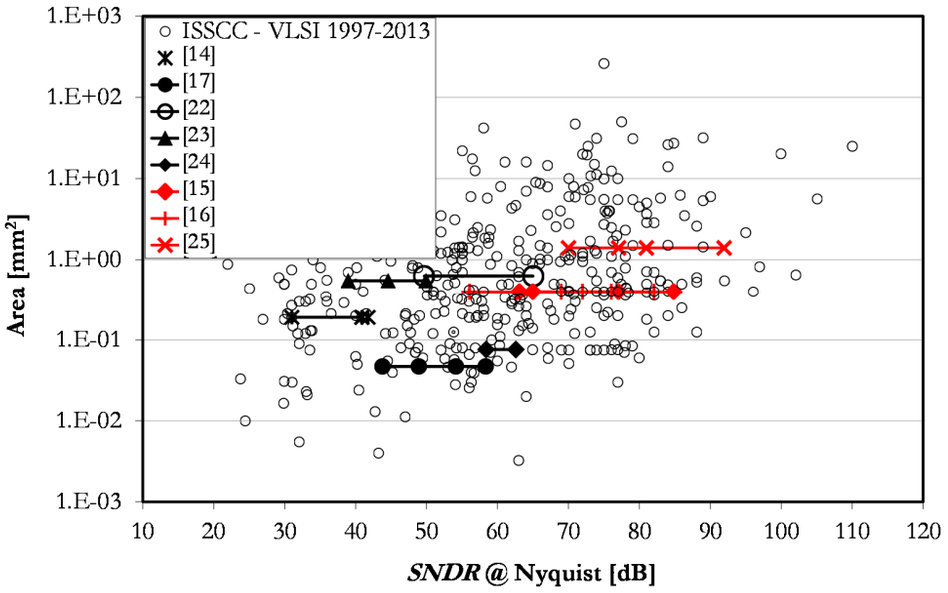


Fig. 4. Area-efficiency versus *SNDR* performance of state-of-the-art tailored (ISSCC- VLSI 1997-2012) and reconfigurable ADCs.

As mentioned before, state-of-the-art custom designs which target *SNDR* below 75 dB are mostly Nyquist-rate designs, while point-solution designs which target *SNDR*>75 dB are generally oversampling ADCs [21].

Reconfigurable Nyquist ADCs (black curves) are generally not optimized in terms of area. The area occupied by these designs is indeed much higher than the area of custom ADCs targeting the same maximum *SNDR*. The area overhead is due to the fact that reconfigurability is achieved here by using switchable blocks which are opportunely enabled to increase the ADC performance and disabled to save power (algorithm-parameter reconfiguration). Reference [19] represents an exception to this trend. In this implementation area-efficiency (as well as power-efficiency) is

obtained by minimizing the capacitors size in the SAR DAC, which usually dominates the overall area budget in SAR ADCs[1].

⊿Σ *modulators* (red curves) show better area-efficiency when compared to point-solutions achieving the same maximum resolution. Both point-solution and reconfigurable designs target indeed high-resolution (maximum *SNDR*>75 dB). The area is thus dominated in both cases by the size of the sampling capacitors, fixed by thermal noise requirements. The area overhead to implement reconfigurability is, on the other hand, mostly negligible.

1.2 Problem statement

From the prior art discussed in Section 1.1.3, it becomes clear that reconfigurable AD converters exist, but their performance is not optimized in terms of power-efficiency and area-efficiency.

More specifically, in the design of medium-to-high-resolution (*SNDR*>75 dB) reconfigurable ADCs, three problems constitute the scientific focus of our research:

1. We want to demonstrate that it is possible to design a reconfigurable ADC which is able to keep state-of-the-art power-efficiency in all its reconfigurability modes.
2. We want to investigate whether the power performance of the reconfigurable ADC will be thermal-noise-limited or technology-limited over its *SNDR* range. In other words, our aim is to check whether the ADC power will increase 4x

[1] In this design the unit capacitor elements of the SAR DAC are implemented as custom interdigitated capacitors with an extremely small value of 0.5fF which are made possible by the 90nm CMOS technology used.

per added bit, following the trend given by FoM_2 in Fig. 3, or 2x per added bit, following the FoM_1 trend.

3. We want to show that a reconfigurability approach can be implemented with negligible area overhead with respect to point-solution ADCs targeting the same maximum *SNDR*.

1.3 Aim of the thesis

The aim of this thesis is to show that it is possible to design reconfigurable medium-to-high resolution ADCs which are both power-efficient and area-efficient. In doing so, the combination of reconfigurability and power-efficiency is addressed as the main design challenge. In other words, the reconfigurable ADC has to achieve *FoM* values which are both close to minimum with respect to state-of-the-art and constant over the whole conversion range.

Pursuant to this aim, a design methodology is proposed to optimize both the power- and the area-efficiency of reconfigurable ADCs.

1.4 Scope of the thesis

Some limitations on the scope of the thesis are described below. A detailed explanation of these choices will be provided in Section 2.4.

- *Delta-sigma AD converters with focus on ΔΣMs*

ΔΣ architectures will be studied to extend reconfigurability to high-resolution AD conversion. This is motivated by the fact that these architectures are the preferred ones in this resolution area. Moreover, as aforementioned, they offer

inherent reconfigurability as they are able to trade resolution with speed. The limitation to ΔΣ modulators is motivated by the fact ΔΣMs have largest influence on the overall performance and power consumption of ΔΣ ADCs. Digital filters are not going to be studied in our research as they are far less constraining.

- *Discrete-time (DT) and single-loop switched-capacitor (SC) implementation*

Discrete-time (switched-capacitor) ΔΣMs will be studied for the implementation of reconfigurable ΔΣ modulators. Moreover, the work is limited to single-loop architectures. The limitation to discrete-time architectures is motivated by their high potential for reconfigurability, especially in biomedical applications. They offer indeed a straightforward reconfigurability of the system by arbitrarily adjusting the sampling frequency [30]. This is not the case for continuous-time (CT) modulators. The limitation to single-loop ΔΣMs is motivated by simplicity as it is sufficient for the demonstration of the proposed reconfigurability approach. The approach, however, can be extended to cascaded architectures if high-order noise-shaping is needed and stability becomes a constraint.

- *CMOS technology*

CMOS is the preferred technology choice for the implementation of digital circuits. As ΔΣ AD conversion implies the integration of analogue circuits (the ΔΣ modulator) and digital circuits (the digital filter), the limitation to CMOS technology is a logical choice. Because of practical reasons (technology availability in this project), all simulations, calculations and implementations are focused to a 0.18μm CMOS technology. However, the proposed concepts could be implemented in other technologies as well.

- *Biomedical applications*

The structured design approach to the power-optimal design of reconfigurable ΔΣMs does not aim for a specific application. In other words, the method can be adapted to any purpose by opportunely incorporating constraints and assumptions related to the target application. However, for the design cases here presented, the design procedure is aimed at the biomedical case. More specifically, out approach will take advantage of the low-frequency nature of the input signals and considers designs as thermal-noise limited. The latter assumption is valid for high-resolution AD conversions.

1.5 Approach

As anticipated in Section 1.3, a design methodology is proposed here to improve the performance of high-resolution reconfigurable ADCs with respect to power-efficiency and area-efficiency.

Our method can be summarized as follows:

- Definition of target specifications.
- Investigation of the fundamental constraints to be considered in the design.
- Analysis of the actual constraints determined by technology.
- Evaluation of prior-art and identification of the trade-offs limiting reconfigurable ADCs performance.
- Identification of a design strategy to implement reconfigurability.

The last step deserves further explanation. Our design strategy consists indeed of the following sub-steps:

1. As a starting point, we identify the possible approaches to reconfigurability.
2. We compare the reconfigurability approaches in terms of power-efficiency.

3. We evaluate them subsequently in terms of area-efficiency.
4. Based on the results of the comparison both in terms of power- and area-efficiency, we select the most promising reconfigurability approach to be implemented and identify a generic design strategy for it.

1.6 Original contributions

This work aims at advancing state-of-the-art in different fields:

Analysis

- Analysis of the power consumption of DT single-loop ΔΣMs, both feedback and feed-forward. The specific focus is on the dependency of the different power contributions on the main design parameters of the modulator, namely filter order, quantizer resolution and oversampling ratio.
- Analysis of the conventional ways to implement the analogue addition required in feed-forward topologies at the input of the quantizer: active addition and passive addition. Analysis of the impact of these solutions on power consumption.

Design

- Introduction of a power-optimal high-level design method for point-solution single-loop ΔΣMs.
- Introduction of a power-optimal high-level design method for reconfigurable single-loop ΔΣMs.
- Design of an alternative summing SAR ADC quantizer based on passive addition and SAR analogue-to-digital conversion algorithm.

Implementation and verification

- Implementation and experimental evaluation of a ΔΣM for hearing aids application including the summing SAR ADC quantizer solution.
- Implementation and experimental evaluation of a power-efficient reconfigurable ΔΣM for biomedical applications.

1.7 Outline of the thesis

The outline of this thesis is briefly explained below.

Chapter 2 introduces ΔΣ architectures foundations with respect to their ideal behaviour and performance criteria. A classification of practical implementations of ΔΣ modulators is presented. Moreover, an overview of state-of-the-art reconfigurable ΔΣMs is given and design choices which limit the scope of the thesis are motivated.

Chapter 3 presents a methodology for the power-optimal design of high-resolution low-bandwidth switched-capacitor ΔΣMs. The method is based on an analytic model of all different contributions to the power dissipation of a SC single-loop ΔΣM. As a second step, techniques that enable power-efficiency at the circuit level are discussed, with particular emphasis on a novel circuit solution which combines multi-bit quantization and analogue addition, i.e. the summing successive-approximation ADC quantizer. Finally, the design of two high-resolution ΔΣMs for hearing aids application is discussed both at the system and circuit level, together with the corresponding simulation and experimental results.

Chapter 4 presents a methodology to design reconfigurable switched-capacitor ΔΣ modulators that are able to keep the power-efficiency constant and optimal for a

set of different resolutions and bandwidths. The method is based on the structured design method for point-solution ΔΣMs presented in Chapter 3. As the size of the sampling capacitors is crucial to determine power consumption, three approaches to achieve reconfigurability are compared: dimension the sampling capacitors to achieve the highest resolution and keep them constant, change only the first sampling capacitor according to the targeted resolution or program all sampling capacitors to the required resolution. The second approach results in the best compromise between power-efficiency and low design complexity. A reconfigurable ΔΣM for biomedical applications is fabricated in a 0.18μm CMOS process for validating the proposed methodology.

Finally, conclusions are drawn in Chapter 5.

2 Power-efficient reconfigurable ΔΣ modulators for autonomous biomedical applications

This chapter introduces ΔΣ architectures foundations with respect to their ideal behaviour and their performance criteria. A classification of practical implementations of ΔΣ modulators is also presented. Moreover, an overview of state-of-the-art reconfigurable ΔΣMs is given and design choices which limit the scope of the thesis are presented and motivated: the focus of this work will be on low-pass discrete-time ΔΣ single-loop architectures implemented using SC techniques.

2.1 ΔΣ modulation for reconfigurable and power-efficient high-resolution ADCs

Fig. 5 depicts again the state-of-the-art ADC designs in the plane power per Nyquist sample ($P_{TOT}/2 \cdot BW$) against achieved *SNDR* [5]. Different AD algorithm types are identified by different colours.

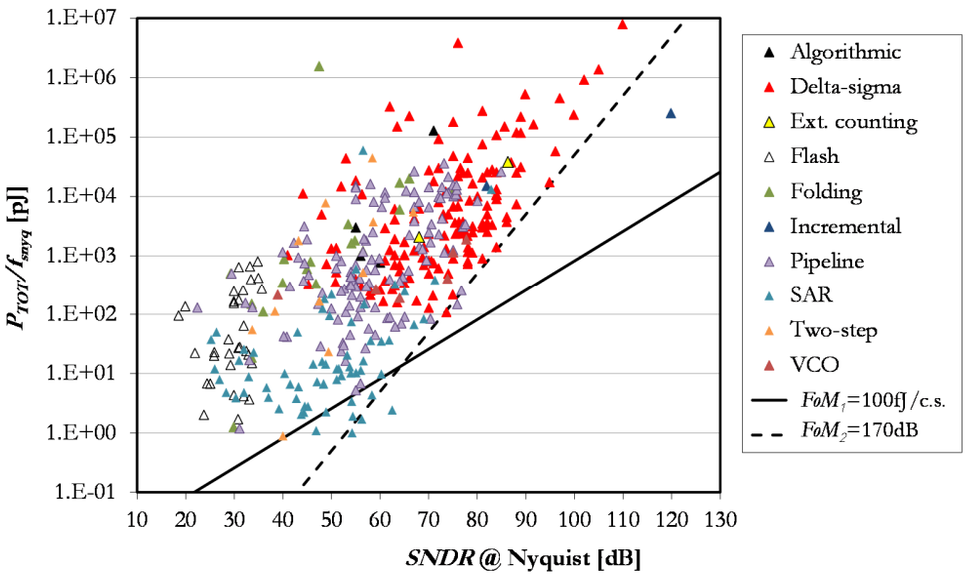


Fig. 5. Power-efficiency versus *SNDR* performance of state-of-the-art ADCs.

Among all the ADC topologies, ΔΣ architectures and incremental ADCs are suited for the implementation of high resolution AD converters. Incremental ADCs are ΔΣ ADCs operated in "one-shot" mode, which perform a fixed number of conversion steps and then reset [31].

As aforementioned, ΔΣ ADCs combine redundant temporal data with filtering to reduce the quantization noise and to push this noise out of the signal band,

respectively. The use of these analogue signal-processing strategies results in high-performance, robust ADCs, which have lower sensitivity to circuitry imperfections than Nyquist-rate ADCs, thus making easier to increase their resolution [4]. Further, as resolution increases beyond 70-dB *SNDR*, they are shown in Fig. 5 to be the most power efficient ADCs [2]. Moreover, ΔΣ ADCs cover a wide *SNDR* region, ranging over more than 50 dB. This feature motivates the use of this data conversion technique for the implementation of reconfigurable ADCs. As mentioned above, ΔΣ ADCs have demonstrated to be very advantageous when reconfigurability is needed, thanks to their inherent trade-off between accuracy and sampling speed [4].

An alternative, similar to approaches chosen in [14] and [32], would be to operate incremental ΔΣ architectures with the same bandwidth and sample rate, and power down circuits between conversions. The resettable operation of incremental ADCs makes them suitable for power-scaled operation which is not straight-forward with oversampled ADCs. At the same time, they are able to achieve high-resolution and good energy-efficiency (see [33] and [34] in Fig. 5). However, the medium bandwidth required for some ADC modes of Table I are more amenable to the use of oversampled ΔΣ ADCs. In view of these considerations, ΔΣ architectures are chosen as focus of our research.

Different architectural- and circuit-level strategies are studied to increase the programmability and adaptability of the ΔΣ ADC performance to a wide number of biomedical specifications with power consumption scalability (for power-efficiency) and large hardware reuse (for area-efficiency). In Section 2.2 the foundations of ΔΣ architectures are introduced. The basic scheme of a ΔΣ ADC is presented, together with its ideal behaviour and a definition of its performance criteria. A classification of practical implementations of ΔΣ modulators is also presented. In Section 2.3 a survey of the state-of-the-art performance of

reconfigurable ΔΣMs is given. As aforementioned in Section 1.1.1, these ΔΣMs are mostly employed in highly integrated wireless transceivers for multi-standard telecom systems. Finally, in Section 2.4, we detail and motivate the design choices limiting the scope of this thesis, as anticipated in Section 1.4.

2.2 ΔΣ ADCs: basics and topologies

Fig. 6 illustrates the basic scheme of a ΔΣ ADC. As shown, a ΔΣ converter is made of two main blocks:

• **Delta-Sigma Modulator.** It simultaneously performs the oversampling and quantization of the band-limited input signal. Quantization error is also high-pass filtered by means of a given noise-shaping technique. This is accomplished by placing an appropriate loop filter $H(z)$ before a low-resolution B-bit quantizer and closing a negative feedback loop around them. The in-band quantization noise is therefore greatly decreased in comparison to that of the embedded quantizer. The output of the ΔΣM is a B-bit digital stream at f_s sampling rate.

• **Decimator.** It reduces the rate of the ΔΣM output stream down to the Nyquist rate. At the same time, the word length increases from B to the final effective number of bits (*ENOB*) in order to preserve resolution as the word rate decreases.

The ΔΣ modulator is the block that has most influence on the ADC performance, basically because it is responsible of the sampling and quantization processes and, therefore, ultimately limits the accuracy of the AD conversion [4]. It also determines the most stringent constraints on power consumption. This analogue block will be thus the object of the research described in this work.

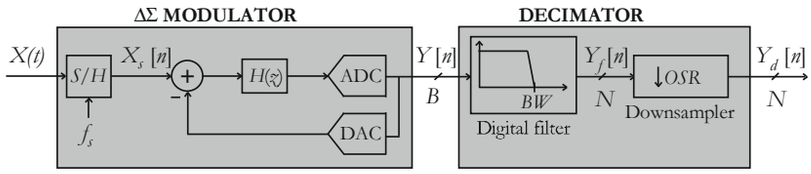


Fig. 6. Generic scheme of a ΔΣ ADC

Fig. 7 (a) shows the basic scheme of a ΔΣ modulator. It consists of a feed-forward path formed by a loop filter $H(z)$ and a B-bit quantizer and a negative feedback path around them using a B-bit DAC.

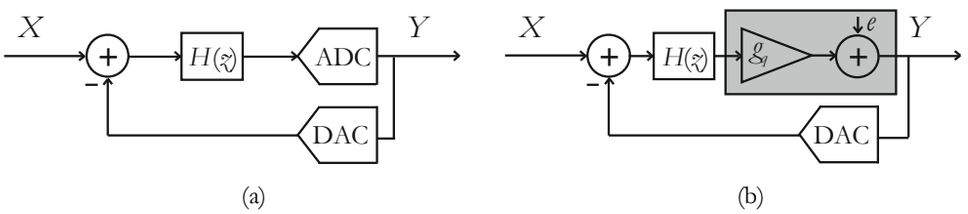


Fig. 7. ΔΣM architecture (a) Basic scheme, (b) Linear model.

Assuming that $H(z)$ has large gain inside the signal band and small gain outside of it, the error signal X- Y is zero in the signal band thanks to the negative feedback. This way, most of the differences between X and Y will therefore be placed at higher frequencies, shaping quantization error and pushing it outside the signal band. Fig. 7 (b) shows the linear model of a ΔΣM, in which the DAC is assumed to be ideal, and the additive white noise approximation is considered for the quantization error e. According to this model, the modulator can be viewed as a two-input system whose output is represented in z-domain as

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{3}$$

where $X(z)$ and $E(z)$ are the z-transform of the input signal and the quantization noise, respectively, and $STF(z)$ and $NTF(z)$ are the respective transfer functions, given by

$$STF(z)=\frac{g_q H(z)}{1+g_q H(z)}, \qquad NTF(z)=\frac{1}{1+g_q H(z)} \tag{4}$$

g_q is the gain of the quantizer (see Fig. 7 (b)) .

Since the signal and the noise pass through different transfer functions, $H(z)$ can be chosen such that the noise shaping does not affect the signal. Using a loop filter with large gain within the signal band, the signal and noise transfer functions can be indeed approximated to

$$STF(z)\approx 1, NTF(z)\approx \frac{1}{g_q H(z)} \ll 1 \tag{5}$$

The noise-shaping function can be built with proper selection of $H(z)$. The simplest loop filter that exhibits the desired frequency performance is an integrator, whose z-domain transfer function is

$$H(z)=\frac{z^{-1}}{1-z^{-1}} \tag{6}$$

Such a modulator is called a 1st-order ΔΣM, referring to the order of the noise shaping. Assuming that the quantizer gain g_q equals unity, the ΔΣM output yields

$$Y(z)=z^{-1}X(z)+\left(1-z^{-1}\right)E(z). \tag{7}$$

The dynamic range of an ideal N-order ΔΣM with a B-bit embedded quantizer that operates at a given oversampling ratio is [35]

$$DR=10\log_{10}\left(\frac{3}{2}\left(2^B-1\right)^2\cdot\frac{(2N+1)OSR^{(2N+1)}}{\pi^{2N}}\right) \tag{8}$$

and therefore it can be increased if *N*, *OSR* and/or *B* become higher. The advantages and disadvantages of each possibility are discussed below:

- **Increasing the modulator order** considerably improves the performance of a ΔΣM, since quantization error will be more attenuated at low frequencies and pushed to high frequencies. However, stability problems arise when using high-order shaping (*N*>3).
- **Increasing the oversampling ratio *OSR*** leads to an increase in the dynamic range of 3(2*N*+1) dB/octave for an ideal *N*-order ΔΣM. The combined action of oversampling and noise shaping considerably improves performance. However, for a given signal band, larger *OSR*s lead to higher sampling frequencies and penalize power dissipation.
- **Increasing the resolution of the modulator embedded quantizer** leads to an increase in the *DR* of approximately 6dB (1bit) per extra bit in the quantizer [36]. A higher B also decreases the stability issues that are induced by the nonlinear errors in the quantizer, and consequently allows higher input signals. However, ΔΣMs with an internal multi-bit quantizer require a multi-bit DAC in the feedback loop, and this block is not inherently linear. As aforementioned, the linearity required in the DAC equals the overall linearity required to the ΔΣ modulator.

The above-mentioned strategies can be combined in many different ways giving rise to different ΔΣM topologies reported in literature. These can be grouped according to the following criteria [37]:

- The nature of the signals being converted: low-pass versus band-pass ΔΣMs.
- The type of dynamics of the loop filter: discrete-time or continuous-time ΔΣ modulators. CT ΔΣMs use CT loop filters but DT quantizers. Also hybrid CT-DT modulators have been reported recently [38].

- The number of quantizers employed. Single-loop ΔΣMs employ only one quantizer. Cascade ΔΣMs employ several quantizers.
- The number of bits in the embedded quantizer. Single-bit ΔΣM modulators featuring a single-comparator as quantizer are inherently linear. Multi-bit ΔΣMs use instead multi-bit quantizers, mostly flash-ADC or SAR-ADC topologies.
- Type of circuitry employed, devices available in the fabrication process, voltage supply, etc. Most of the reported DT implementations employ switched-capacitor (SC) circuits with dedicated high-density and high-quality capacitors, other employ capacitors available in standard CMOS technologies, active capacitors built with MOS transistors, switched-current (SI) circuits, etc.

Describing all possible ΔΣM architectures derived from these classification criteria goes beyond the scope of this work. In the next sections, we will use these basic concepts to analyse state-of-the-art reconfigurable ΔΣM performance and trends and to address the challenge of designing reconfigurable ΔΣMs for biomedical applications.

2.3 State-of-the-art reconfigurable ΔΣ modulators

ΔΣMs are very suited for the implementation of reconfigurable ADCs [39]. Indeed, the combination of different architectural and circuit strategies overviewed in Section 1.1.1, together with the variation of basic ΔΣM parameters, i.e., *OSR*, *N*, and *B*, can contribute to adapt the ADC performance to different specifications with a high level of hardware reuse [40].

Several state-of-the-art reconfigurable ΔΣMs are able to handle more than two standard specifications. Fig. 8 depicts state-of-the-art reconfigurable ADCs employed for multi-mode applications on the resolution-bandwidth plane. The same

symbols represent different reconfigurability points for the same IC. Discrete-time ΔΣ architectures are depicted in black, continuous-time ΔΣMs in red. Single-loop topologies are represented as empty shapes while cascade ΔΣMs are filled shapes.

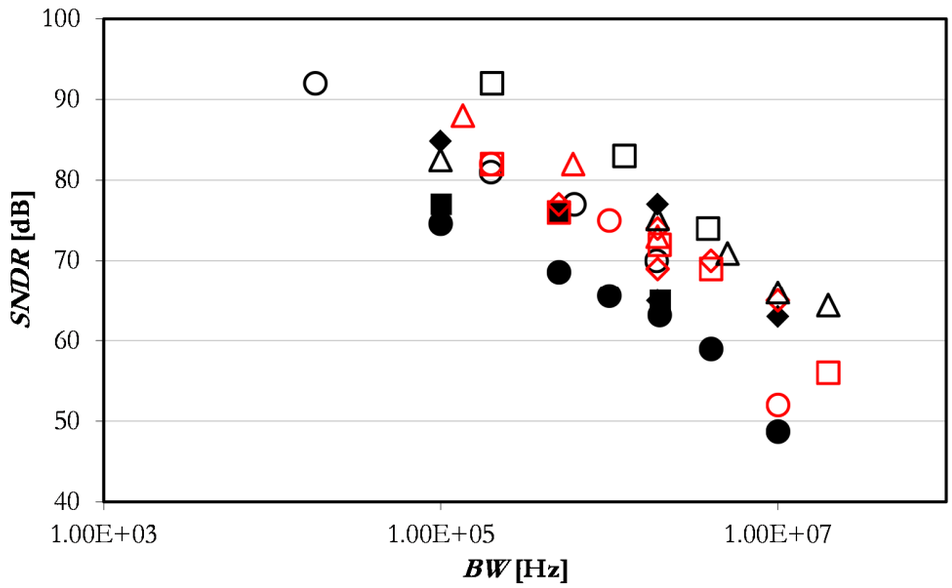


Fig. 8. State-of-the-art reconfigurable ADCs for multi-standard applications. Continuous-time ΔΣ architectures are depicted in red, discrete-time ΔΣMs in black; single-loop topologies are represented as empty shapes, cascade as filled shapes.

In Fig. 8 the following trends can be observed:

- State-of-the-art reconfigurable ΔΣMs cover in total a range of more than 40 dB in *SNDR*, and approximately 3 decades in signal bandwidth, between 18 kHz and 20 MHz, respectively. These ranges of resolution and *BW* make them suitable for multi-standard wireless transceivers applications.
- The majority of state-of-the-art ΔΣMs are DT implementations. They offer indeed a straightforward reconfigurability of the system by arbitrarily adjusting the sampling frequency, which is not the case for CT modulators (this concept will be further

clarified in the next section). CT circuits are sometimes used to implement functions like blocker-rejection filtering, frequency-mixing process, channel-selection and anti-aliasing filtering. The resulting ΔΣM-based transceivers may become more efficient than conventional ones in terms of analogue circuit complexity, shared building blocks, and reduced power consumption [39].

- Most of the designs choose single-loop ΔΣ topologies because of their robustness to non-idealities of circuit components. Furthermore the relatively simple structure makes it more suitable for the complex reconfigurable circuit design [41].

2.4 Reconfigurable ΔΣMs for biomedical applications

Existing reconfigurable ΔΣMs are conceived for medium-resolution high-frequency radio-transmission applications. The design alternatives for the implementation of state-of-the-art ICs are outlined in the previous section (Fig. 8). To extend the use of reconfigurable modulators to low-frequency high-resolution biomedical applications, we will hereafter focus on discrete-time ΔΣ single-loop architectures implemented using SC techniques.

Although continuous-time ΔΣ modulators are sometimes preferred to DT ΔΣMs for their inherent anti-alias filter function, DT ΔΣ implementations are chosen here for their robustness. Their transfer functions rely indeed on capacitor ratios, an advantage which is expected to become more and more pronounced as technology will scale further. Moreover, DT ΔΣMs can be easily rconfigured by adjusting the sampling frequency [30]. This feature has high potential for reconfigurable ΔΣMs, especially in biomedical applications. At low frequencies, indeed, the sampling speed is not constrained by technology limits and arbitrarily changing the *OSR* can be used to tune the final resolution of the modulator. Also, we do not expect to suffer from

severe settling time requirements in the SC-integrators, as the signal bandwidth to be covered is not large (the maximum bandwidth is in the audio range). .

Single-loop ΔΣMs have been chosen because of the relaxed constraints on their analogue blocks [39]. Moreover, this class of ΔΣMs is suitable for high accuracy low-to-moderate bandwidth specifications, which characterize the biomedical applications of this work. Our research, however, can be extended to cascaded architectures if high-order noise-shaping is needed and stability becomes a constraint.

2.5 Conclusion

In this chapter, ΔΣM architectures were identified as focus of our research. Among all state-of-the-art AD topologies, ΔΣMs are indeed demonstrated to be the most suitable for the power-efficient implementation of high resolution and reconfigurable AD converters.

Consequently, the basic principles of ΔΣ modulation were presented and the benefits of oversampling and noise shaping on the ADC performance were discussed. Topological alternatives for the practical implementation of ΔΣ modulators were also described.

Finally, the state of the art of reconfigurable ΔΣMs was summarized and our design choices for the implementation of reconfigurable ΔΣMs suited to biomedical applications were explained.

3 Power optimal design of SC ΔΣ modulators for given resolution and bandwidth

This chapter presents a methodology for the power-optimal design of high-resolution low-bandwidth switched-capacitor ΔΣMs. The method is based on an analytic model of all different contributions to the power dissipation of a SC single-loop ΔΣM which enables an accurate system-level optimization. As a second step, techniques that enable a further improvement of power-efficiency at the circuit level are discussed, with particular emphasis on a novel circuit solution which combines multi-bit quantization and analogue addition, i.e. the summing successive-approximation ADC quantizer. Finally, the design of two high-resolution ΔΣMs for hearing aids application is discussed both at the system and circuit level, together with the corresponding simulation and experimental results. The comparison between the power estimated by the analytic model and transistor-level simulations validates the proposed design methodology. The power-efficiency of the summing SAR quantizer is confirmed by measurement results. Parts of this chapter have been published in [42], [43].

3.1 Introduction

The preliminary step towards the implementation of a power-efficient reconfigurable ΔΣ modulator consists in defining a method for the power-optimization of single-loop SC ΔΣMs [35]. This design methodology will also be used in Chapter 4 to compare the power consumption when using different strategies for reconfigurability.

The resolution of a ΔΣM is mainly determined by *N, B, OSR*, and by the sampling capacitors of each integrator $C_{s,i}$[2], thus several combinations of these parameters can provide the target *SNDR* in the given bandwidth. The power-optimization method presented in Section 3.2 explores the solution space defined by these design variables and selects the architecture that fulfils the specifications of resolution and bandwidth with the lowest power consumption.

The methodology is applied to the design of a high-resolution ΔΣ modulator for hearing aids application. The contributions to the total power consumption are calculated and their dependency on the design parameters (*N*, *B*, and *OSR*) is analysed. Based on the result of the power-optimization, a second-order multi-bit feed-forward topology is chosen for hearing aids application.

Once the architecture is selected, the focus of the chapter moves to circuit techniques for the power-efficient implementation of SC feed-forward ΔΣMs. More specifically, a summing successive-approximation quantizer able to perform multi-bit quantization together with analogue addition is discussed in Section 3.3. The combination of passive addition and SAR quantization helps to reduce both

[2] The index i ($1 \leq i \leq N$) indicates the position of each integrator in the ΔΣM starting from the input.

complexity and power consumption of the ΔΣ modulator, as these operations typically require considerable power in FF topologies.

In the last section of the chapter, Section 3.4, two transistor-level implementations are discussed, which validate the proposed design methodology and confirm the beneficial effect of the summing SAR ADC approach on power-efficiency.

3.2 Power optimization method

As motivated in Section 2.4, this analysis is applied to the design of SC single-loop ΔΣMs. Single-loop ΔΣMs are chosen as they are suitable for high accuracy low-to-moderate bandwidth applications, including the ones of the case studies presented in Sections 3.4.1 and 3.4.2. Fig. 9 (a) and (b) show the general scheme of feedback (FB) and feed-forward (FF) single-loop modulators, respectively.

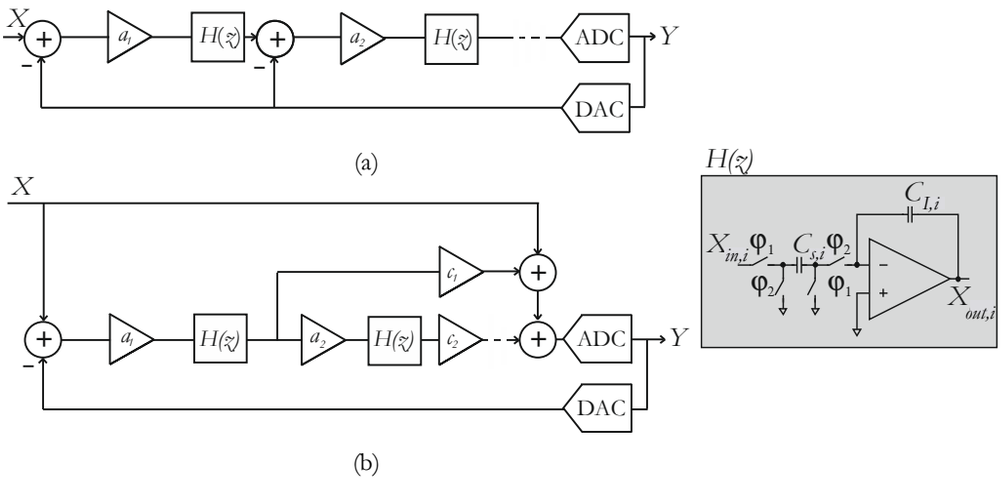


Fig. 9. Conventional FB (a) and FF (b) single loop ΔΣ modulators. The implementation of the SC integrators $H(z)$ is shown the inset.

The simplified SC implementation of the integrator blocks $H(z)$ is shown in the inset on the right. φ_1 and φ_2 are two non-overlapping phases of the SC integrator, the sampling phase and the integrating phase, respectively ; a_i and c_i (i=1: N) are the in-loop coefficients of the ΔΣM.

3.2.1 Global design methodology

The design methodology defined in this work is summarized by the flow diagram in Fig. 10.

The *SNDR* specification of the ΔΣM in input to the flow diagram is defined as:

$$SNDR = 3 \cdot 2^{2 \cdot ENOB - 1} = \frac{V_{in,MAX}{}^2}{P_{Th} + P_Q + P_{HD}} \tag{9}$$

where $P_{Th,}$ P_Q and P_{HD} are the power of the in-band thermal noise, quantization error, and distortion components, respectively. $V_{in,\,MAX}$ is the maximum input range of the modulator, here defined as $V_{in,MAX} = OL \cdot V_{in,FS}$. The overload level OL is the maximum amplitude relative to the input full scale $V_{in,\,FS}$ at which the modulator still operates correctly [44]. Once the OL point is approached, the ΔΣM experiences a steep decrease of performance due to the overloading effect of the quantizer. Most publications consider that the modulator operates correctly until the *SNDR* falls 6dB below the peak-*SNDR* [45]. The noise power term P_{HD} is related to non-linearities in the ΔΣM. The harmonic distortion is a consequence of applying a non-linear operation to the input signal. In SC implementations, the main causes of distortion are the non-linear OTA gain, the non-linear settling of the integrators, non-linear capacitances and the non-linear switches [46]. P_{Th} and P_Q in (9) are defined for a fully-differential ΔΣM implementation as [47]- [48]:

$$P_{Th} = \frac{2kT}{OSR \cdot C_{s,1}} \tag{10}$$

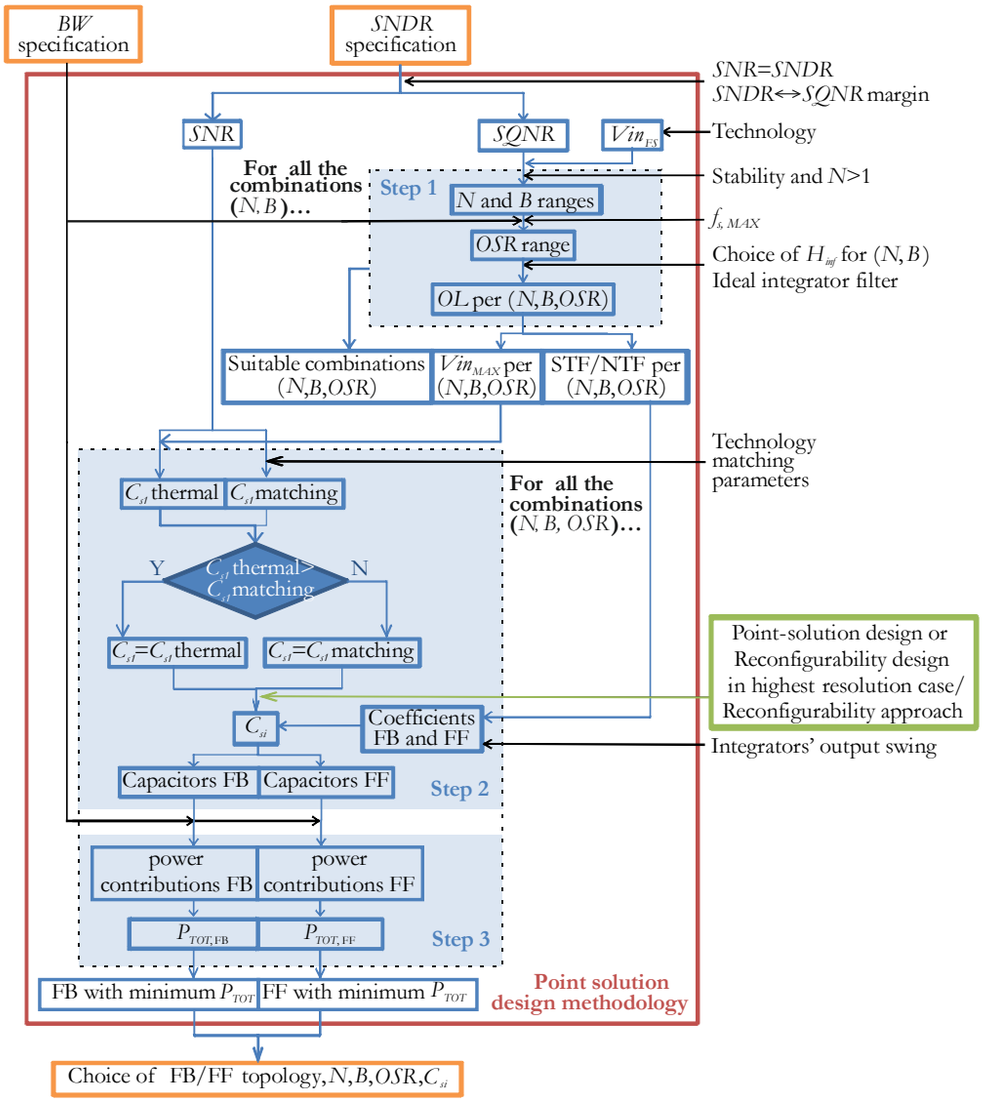


Fig. 10. Flow diagram of the proposed method for power-optimal point-solution ΔΣ designs. The index i (i=1,…,N) indicates the position of each integrator in the ΔΣM starting from the input.

$$P_Q = \frac{\left(2V_{in,FS}\right)^2}{12} \frac{\pi^{2N}}{(2N+1)\cdot OSR^{2N+1}\left(2^B-1\right)^2} \tag{11}$$

where $C_{s,1}$ is the first-integrator sampling capacitor and variables k and T stand for the Boltzmann constant and the absolute temperature, respectively. In (10) only the thermal noise coming from the sampling operation of the switches is considered [47]. This is based on the assumption that the contribution of the OTA noise is negligible with respect to the noise of the switches. This assumption is going to be verified a posteriori by means of behavioural simulations.

All this said, for an *SNDR* target specification (at top of Fig. 10) we will globally structure the design procedure in three major steps, as discussed here below.

Step 1 - As a first step, we identify the combinations of (*N*, *B*, *OSR*) that are able to achieve the specified *ENOB*. This selection is based only on quantization-noise requirements (Step 1-box in the upper right part of Fig. 10). Therefore, we combine (9) and (11) by temporarily assuming *OL*=1 and neglecting both P_{Th} and P_{HD} in (9). In other words, we simplify (9) as:

$$\frac{V_{in,FS}^{\ 2}}{P_Q} = \frac{(2N+1)\cdot OSR^{2N+1}\left(2^B-1\right)^2}{3\pi^{2N}} = SQNR \tag{12}$$

The *SQNR* is set to be 10 dB higher than the *SNDR* specification value, i.e. $SQNR = SNDR + 10dB$. This margin guarantees that the quantization noise is well below the thermal noise P_{Th} and takes into account sources of distortion P_{HD} that are not included in the analytical model [49]. This noise-budget strategy aims at making the thermal noise dominant in the modulator as is common for power-efficient designs: indeed, suppressing the thermal noise costs a lot of power.

Based on (12) all the combinations (N, B, OSR) that are able to fulfil the $SQNR$ specifications are identified as indicated in the Step 1-box of Fig. 10. At the same time, the values of OL associated to each suitable (N, B, OSR) combination are derived, as will be explained in Section 3.2.2. From this OL-value we then derive $V_{in,MAX}$ and the transfer functions STF and NTF.

Step 2 – As a next step, we calculate the minimum value of sampling capacitors $C_{s,1}$ in the first integrator which satisfies the $SNDR$ requirement in terms of thermal noise and DAC linearity (Step 2-box on the lower left of Fig. 10).

- The thermal noise requirement is satisfied by using together (9) and (10) for all the combinations of (N, B, OSR) in the solution space identified in Step a). The term P_{HD} in (9) is neglected now assuming that $SNDR$=SNR, i.e. supposing that the distortion components are submerged in the noise-floor. SNR is the signal to noise ratio.
- The capacitive input DAC gives the dominant contribution to non-linearity[3]. Therefore, to ensure that the distortion level is indeed below the noise, we impose that the signal to distortion ratio of the DAC is as large as the total $SNDR$. This requirement results in a second minimum size of $C_{s,1}$, see Fig. 10, based on matching requirements.

$C_{s,1}$ is finally chosen to be the maximum of the values given by thermal noise or linearity requirements. More details on the procedure to select $C_{s,1}$ are given in Section 3.2.3.

The values of sampling capacitors $C_{s,i}$ in the integrators following the first one (i>1) are calculated starting from $C_{s,1}$ for both feedback and feed-forward single-loop topologies. As specified in Fig. 10, this calculation is different depending on

[3] This assumption is going to be validated a posteriori using transistor-level simulations.

whether the power-optimization method is applied to a point-solution or to a reconfigurable design. In this chapter the point-solution case is described in detail (Section 3.2.3), while the reconfigurable case will be further clarified in Chapter 4.

Step 3 - We estimate the total power consumption of the ΔΣM (Step 3-box on the bottom left of Fig. 10) for all the combinations in the (*N*, *B*, *OSR*) solution space found in Step a) for both feedback and feed-forward topologies. This is done using the values of $C_{s,i}$ found in Step b). Additional inputs needed to calculate the power are the *BW* specification, the STF and NTF for each (*N, B, OSR*) and the desired output swing for the integrators (Fig. 10). The power is calculated for all the combinations of (*N*, *B*, *OSR*) in the solution space using the analytic model presented in Section 3.2.4 and the ΔΣ architecture granting the lowest power solution is selected. As shown at the bottom of Fig. 10, the power-optimal architecture is defined by the following design variables:

- the topology (feedback or feed-forward)
- *N*, *B*, *OSR*
- the value of the sampling capacitors $C_{s,i}$.

3.2.2 Step 1 - Choosing OL, STF/NTF for each (N, B, OSR)

As mentioned above, the first step of the design methodology consists in defining the solution space, i.e. in finding all the combinations (*N*, *B*, *OSR*) suitable to achieve the target *SQNR* (*SQNR*=*SNDR*+10dB). At the same time, their associated value of *OL* and the transfer functions (STF and NTF) must be derived.

At this point, for all the possible combinations (*N*, *B*) we follow the procedure shown in the light blue box on the upper right part of Fig. 10: First, a design choice about the *range of N and B* is made. Usually, first-order filter loops are avoided due to the high correlation between the quantization error and the input signal, which

leads to a non-linear dynamic behavior of the ΔΣM. To choose the maximum values of N and B, the tendency to instability of high-order single-loop ΔΣMs and the increased linearity requirements of multi-bit topologies, respectively, must be taken into account (see Section 2.2).

Second, we determine the *OSR range*. The minimum value of *OSR*, OSR_{MIN} is found using (12) and the target *SQNR*. The choice of the maximum *OSR*, OSR_{MAX} depends on the target input signal bandwidth and on the maximum speed available in the given technology.

Third, we derive a specific value of *OL* to be assigned to each combination of (*N*, *B*, *OSR*). The *OL* is a weak function of *OSR*, for sufficiently large *OSR*. Thus, as shown in Fig. 10, this dependency is neglected in the rest of the thesis. The determination of *OL* requires careful consideration. The *OL* is indeed a function of the infinity norm $\|H_\infty\|$[4], a parameter which strongly affects the stability of the loop and thus the final ΔΣM performance. In the case of a single-bit quantizer, the infinity norm is traditionally chosen to be 1.5. In the case of a multi-bit quantizer, $\|H_\infty\|$ can be increased to improve the signal-to-quantization noise ratio (*SQNR*). However, this cannot be pushed too far, because then the *OL* starts to decrease. In [41] specific values of infinity norm $\|H_\infty\|$ have been chosen for different combinations of filter orders and quantizer resolutions to maximize the *SQNR* while minimizing the decrease of the *OL*. In this work we adopt the same choice for

[4] $\|H_\infty\|$ is the maximum gain of the NTF $H(z)$ over frequency, also known as the infinity-norm of $H(z)$ [23]. According to Lee's Criterion [86], a single-bit ΔΣM is likely to be stable if $\|H_\infty\|$ <1.5. Note that this criterion is neither necessary (some stable high-order modulators are reported for which higher values are allowed), nor sufficient (this criterion says nothing about a limit on the input signal) [23].

$\|H_\infty\|$, while the STF and the NTF are determined using [50]. More specifically, the optimal NTF is determined using the *synthesizeNTF* function in [50], and then the corresponding *OL* values are found. Finally, the modulator stability is verified by means of long-term transient simulations in the transistor-level design phase.

3.2.3 Step 2 - Sizing of the sampling capacitors

For all the combinations of (*N*, *B*, *OSR*) in the solution space determined in the previous Section, the sampling capacitor $C_{s,1}$ of the first integrator (see the inset of Fig. 9) in the loop filter is calculated from thermal noise requirements according to [47]:

$$C_{s,1} = \frac{2kT}{OSR} \cdot \frac{SNR}{\left(V_{ref} \cdot OL\right)^2} \tag{13}$$

where V_{ref} is the reference voltage for the quantizer . V_{ref} is assumed to coincide with the supply voltage V_{DD} in both the FB and FF topologies. As aforementioned, we assume here that *SNR*=*SNDR*.

DAC linearity and matching requirements also set a lower boundary for $C_{s,1}$. As shown in Fig. 11, when the feedback DAC functionality is integrated in the SC integrator block, two different configurations are possible. The two schemes differ in the sense the sampling capacitor is merged or not with the DAC capacitor array. Consequently, they differ in power consumption and timing constraints. Their function, however, is the same [47]. Moreover, in both cases the total capacitance implementing the total *B*-bit feedback DAC has the same size as the corresponding sampling capacitor.

As the *B*-bit feedback DAC is implemented in SC designs as a capacitive array of 2^B-1 unit elements C_u (see Fig. 11), the overall size of $C_{s,1}$ is equal to the sum of the individuals capacitances C_u:

$$C_{s,1} = \left(2^B - 1\right) \cdot C_u \tag{14}$$

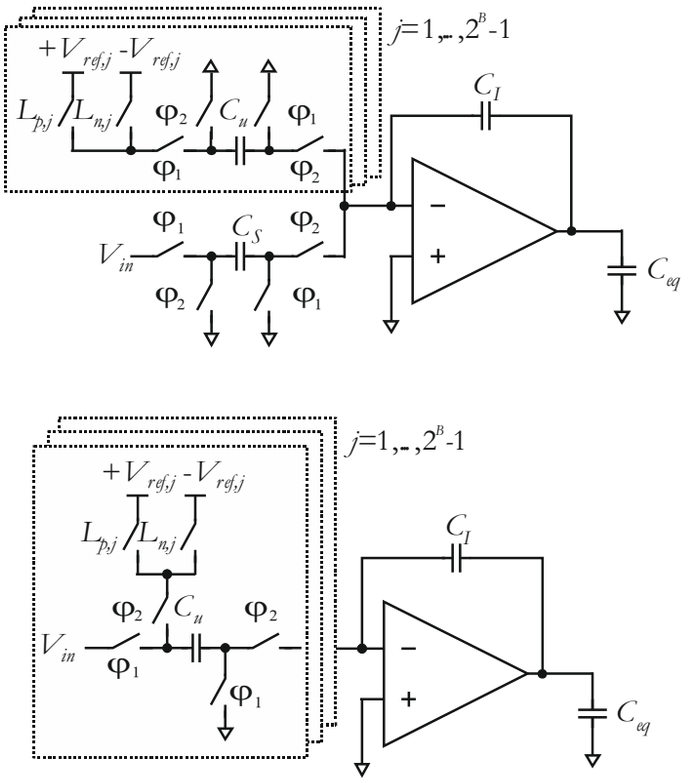


Fig. 11. Different feedback configurations of an SC integrator. A single-ended implementation is shown for simplicity. $L_{p,j}$ and $L_{n,j}$ are feedback signals driving the DAC (j=1, …, 2^B-1).

To improve the linearity of the DAC, a dynamic element matching technique called data weighted averaging (DWA) [51] is used throughout this work. This algorithm makes a cyclic selection of the elements participating in the DA conversion and guarantees that all the elements are almost equally selected over any arbitrarily long time period. As a consequence, the DWA rejects most of the mismatch noise outside the baseband with first-order noise shaping and the

requirements on the DAC matching accuracy needed to ensure a DAC signal to distortion ratio equal to the total *SNDR* are relaxed according to [52]:

$$\frac{\sigma_{C_u}}{C_u} = \frac{\sqrt{3\cdot\left(2^B-1\right)\cdot OSR^3}}{\pi}\cdot\frac{1}{2^{ENOB}}\cdot\frac{2^B-1}{2^B-2} \tag{15}$$

The matching accuracy of a capacitor is related to its area (A_c) through the relation [53]:

$$\frac{\sigma_{C_u}}{C_u} = \frac{K_\sigma}{\sqrt{A_c}} = K_\sigma\sqrt{\frac{C_A}{C_u}} \tag{16}$$

where K_σ is the matching constant of capacitors and C_A is the capacitance per unit area for the given technology . The minimum size for the first sampling capacitor $C_{s,1}$ can thus be expressed from (14) to (16) as:

$$C_{s,1} = 2^{2\cdot ENOB}\cdot\pi^2\cdot {K_\sigma}^2\cdot\left(\frac{2^B-2}{2^B-1}\right)^2\cdot\frac{C_A}{3\cdot OSR^3} \tag{17}$$

Finally, $C_{s,1}$ is sized to be the maximum of the values given by (13) and (17).

Taking into account the gain and the noise filtering introduced by the previous integrators in the ΔΣM, the sampling capacitors $C_{s,i}$ in the integrators after the first one (i>1) can be sized from thermal noise requirements as [47]:

$$C_{s,i} = C_{s,1}\frac{\pi^{2i-2}}{OSR^{2i-2}\left(2i-1\right)}\prod_{k=2}^{i}\frac{1}{{a_{k-1}}^2} \tag{18}$$

where a_k are the in-loop coefficients of single-loop ΔΣMs. The coefficients a_k are shown in Fig. 9 (a) and (b) for FB and FF ΔΣM topologies, respectively.

3.2.4 Step 3 - Power consumption estimation

Once the minimum value of the sampling capacitors $C_{s,i}$ is known as a function of (*N, B, OSR*), it is possible to estimate the power contributions and the total power dissipation of the ΔΣM.

The total power consumption P_{TOT} consists of four main contributions: the static power of the OTAs P_{STAT}, the dynamic power for charging the capacitors in the modulator P_{DYN}, the power dissipated by the quantizer P_{QUANT} and the power dissipated by the DWA digital circuitry P_{DWA}. Thus,

$$P_{TOT} = P_{STAT} + P_{DYN} + P_{QUANT} + P_{DWA}. \tag{19}$$

These calculations are represented by the blocks called power contributions and P_{TOT}, respectively, in the Step 3-box of Fig. 10 both for FB and FB configurations. The calculation of the power contributions is elaborated in the following sections (from Section 3.2.5 to Section 3.2.8) and is summarized by the flow diagram of Fig. 12. The calculation of P_{TOT} is explained in Section 3.2.9.

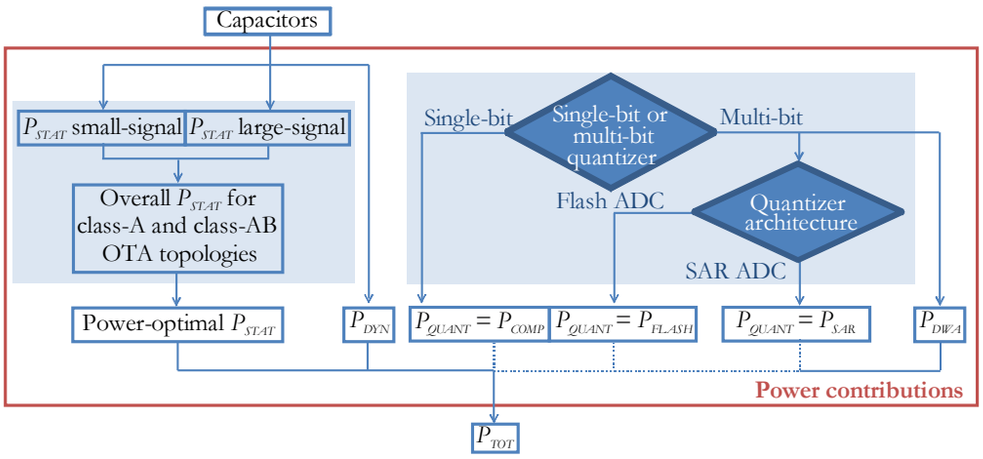


Fig. 12. Flow diagram of the procedure to calculate the power contributions of the ΔΣM.

3.2.5 Static power

It is a common approach to calculate the ΔΣM static power taking into account only small-signal settling requirements and without including the slewing behaviour of the OTAs [35]. This is a rather coarse approximation for OTAs in ΔΣ modulators, especially in single-bit topologies, where the feedback signal is

inherently large. Moreover, in literature, the power comparison between different OTAs topologies is mostly limited to class-A OTAs [47]. We address these issues by providing a model of OTA static power which has the following characteristics:

- it considers both the small-signal and the large-signal behaviour of the OTAs;
- it finds an expression for the OTA power consumption during the time interval in which the OTA has a large-signal behaviour, which is a function of the feedback signal and thus of the number of bits *B* of the quantizer;
- it derives specific expressions for several class-A and class-AB OTA topologies.

This improved model enables an accurate estimation of P_{STAT} and makes it possible to compare the power consumption of different circuit implementations of the OTA. In this way, we can choose the most power efficient OTA implementation for each combination of (*N, B*). The comparison does not take into account OTAs non-idealities. We assume indeed that all the topologies are able to satisfy the design requirements both in terms of noise and DC gain. This assumption is going to be finally verified by means of behavioural simulations.

This static power model is based on the analysis described in [54]. However, the method presented in that paper is only valid for single-bit SC ΔΣMs. Here, we derive an expression for the feedback signal which is a function of the quantizer number of bits *B* and thus extends the power model to multi-bit quantizers.

Another power-efficient implementation for OTAs used in SC circuits is a simple digital inverter. It operates indeed with very low supply voltages, allows class-AB operation and has large output swing [55]. However, this approach is not considered in the static power model presented in the next sections. At the time this research started, the performance of inverter-based modulators was limited by intrinsic limitations of traditional inverters. The DC gain of class-C inverters, below 60 dB, caused leaking and non-linearity of inverter-based integrators and made them

unsuitable for high-resolution applications. Moreover, inverters operated in a sub-threshold region and their performance (such as slew-rate, bandwidth) degraded at slow process corners [56]. Finally, the single-ended nature of the inverter necessitates the use of pseudo-differential structures to enhance its noise rejection, which complicates the design of common-mode feedback [57]. Recently, several ΔΣ designs have been presented which solve these problems by employing gain-boosted class-C inverters with increased DC gain [55]- [56]. In these solutions, robustness over PVT variations is also achieved by means of dedicated biasing schemes which use LDOs and constant-Gm sources in [55] and on-chip body bias techniques [56]. Such improvements make inverter-based architecture an attractive solution for high-resolution modulators, to be included in future analysis of the static power contribution.

3.2.5.1 Small-signal and large-signal behaviour

The single-ended implementation of an SC integrator is represented in Fig. 13. Please note that in this picture and in this whole section the subscript *i* is neglected for simplicity. As aforementioned, this feedback scheme is one of the two options (see Fig. 11). We will use here this configuration in analogy with [54]; the results are the same for the alternative scheme in Fig. 11. The analysis of a single-ended OTA is also chosen for simplicity. Note that all the formulae can be derived in a similar way for the fully differential implementations. φ_1 and φ_2 are, again, the two non-overlapping phases, φ_1 the sampling phase and φ_2 the integration phase. During φ_1, the input signal V_{in} is sampled onto the input capacitor C_s and the feedback signal is generated by the sampling of the references. The reference voltages $+V_{ref,j}$ or $-V_{ref,j}$ are sampled on each of the 2^B-1 unit elements C_u depending on the feedback signals $L_{p,j}$ and $L_{n,j}$ generated by the DWA (j=1, …, 2^B-1) .

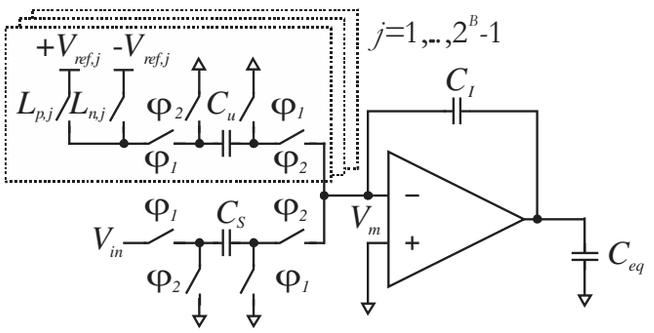


Fig. 13. Single-ended implementation of an SC integrator. The feedback signals $L_{p,j}$ and $L_{n,j}$ are controlled by the digital output code of the quantizer

During φ_2, the charge stored in these capacitors is transferred to the integrating capacitor C_I. In this phase, the OTA shows two different behaviours: large-signal and small-signal, depending on the voltage at the inverting input node of the OTA V_m. Following the approach in [54]., we define ΔV_{th} as the differential input voltage at which the output current saturates to its maximum value I_{SAT}. As long as V_m is larger than the "differential-pair threshold voltage" ΔV_{th}, the OTA is in large-signal behaviour and its output dynamics is limited by slewing. When V_m becomes lower than ΔV_{th}, the OTA approaches small-signal behaviour and its gain-bandwidth GBW is assumed to determine the settling performance. The integrating phase φ_2 is consequently divided into two periods, called large-signal period and small-signal period, respectively [54]..

The average power $\overline{P}$ dissipated in one clock period T by the OTA can be calculated as a weighted sum of the power consumed during the large-signal period P_{la} and of the power consumed during the small-signal period P_{sm}:

$$\overline{P} = \alpha\theta \cdot P_{la} + \beta\varsigma \cdot P_{sm} \tag{20}$$

where variables a and β are parameters dependent on the OTA topology. Until now we have considered just the power dissipated by the OTA during the integrating

phase, during the large-signal period P_{la} and during the small-signal period P_{sm}, respectively. ζ and θ are corrective terms which are added to take into account the power dissipated by the OTA during the sampling phase φ_1 (see Fig. 13).

3.2.5.2 Small-signal power consumption

The calculation of P_{sm} is derived based on settling requirements. A conservative choice to ensure settling of the amplifier before the subsequent sampling moment is $GBW = 5 \cdot f_s$ [5], where f_s is the modulator sampling frequency [35]. The current flowing in the input stage of a single-stage OTA can therefore be calculated from:

$$\frac{g_{m,in}}{C_{eq}} = GBW \cdot 2\pi \tag{21}$$

where $g_{m,in}$ is the OTA input transconductance and C_{eq} is the equivalent load capacitance[6]. C_{eq} can be expressed, for both FB and FF topologies, as [35]:

$$C_{eq} = C_s + C_p + C_L\left(1 + \frac{C_s + C_p}{C_I}\right) \approx C_s + C_L\left(1 + \frac{C_s}{C_I}\right) \tag{22}$$

Note that C_{eq} corresponds to the effective closed loop capacitive load of an SC integrator during the integration phase. Here, C_p is the OTA input parasitic capacitance and C_L is the integrator output load . C_p is assumed negligible since its value is normally minimized by design.

Assuming the transistors of the input stage biased in weak inversion, the bias

[5] If the output of the integrator has a single pole response, for an integrator settling time constant τ and an allowed settling time T_A, the integrator output settles to a voltage $V_{settle} = V_{ideal} \cdot \left(1 - e^{-N}\right)$ where $N = T_A / \tau$ and V_{ideal} is the voltage toward which the output is settling asymptotically. N is the number of time constants allowed for settling. T_A is typically slightly less than half the sampling period [56].

[6] For a given GBW and load capacitance C_{eq}, the current drawn by a Miller OTA can be calculated instead as $\frac{g_{m,in}}{C_M} = GBW \cdot 2\pi$ where C_M is the Miller compensation capacitance.

current becomes

$$I_{BIAS,in} = GBW \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq} \tag{23}$$

where V_{Th} is the thermal voltage (V_{Th}=26 mV at 300K), and n is the weak inversion slope factor (1.3-1.5) . The power consumed during the small-signal period is therefore calculated as:

$$P_{sm} = 5 \cdot f_s \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq} \cdot V_{DD} \tag{24}$$

3.2.5.3 Large-signal power consumption

The power for charging the capacitors during the large-signal period P_{la} is a function of both the input signal V_{in} and the reference voltages and can be expressed as:

$$P_{la}\left(V_{in}, V_{ref}\right) = \left(C_s \cdot V_{in} \pm \sum_{j=1}^{2^B-1} C_u \cdot V_{ref,j} \right) V_{DD} \cdot f_s \tag{25}$$

Please note that this contribution is input-signal dependent as the first factor in (25) is the charge stored on C_s and C_u at the beginning of the integrating phase φ_2.

If we now assume x to be the normalized input signal with respect to the reference voltage V_{ref}, i.e. $x = V_{in}/V_{ref}$, the notation $P_{la}(V_{in}, V_{ref})$ can be rewritten as:

$$\begin{aligned} P_{la}(V_{in}, V_{ref}) &= \left(C_s \cdot x \cdot V_{ref} \pm \sum_{j=1}^{2^B-1} C_u \cdot V_{ref,j} \right) V_{DD} \cdot f_s = \\ &= \left| \frac{k(t)}{2^B - 1} \mp x \right| \cdot C_s \cdot V_{ref} \cdot V_{DD} \cdot f_s \end{aligned} \tag{26}$$

where $\frac{k(t)}{2^B - 1}$ is the B-bit DAC feedback signal normalized with respect to V_{ref}, and, again, $C_s = (2^B\text{-}1) \cdot C_u$.

$P_{la}(V_{in}, V_{ref})$ is the minimum power consumption for the combination of the input signal and the reference voltage during the large-signal period. $P_{la}(V_{in}, V_{ref})$ is

both dependent on the number of bits of the feedback DAC B and on the input signal as it includes x and $k(t)$. The feedback signal $k(t)$ is a B-bit representation of x, i.e. of V_{in}/V_{ref}. Depending on the amplitude of the input signal, $k(t)$ ranges between 0 and 2^B-1 and its value corresponds to the number of DAC elements C_u connected to $+V_{ref}$ (see Fig. 13).

3.2.5.4 Overall static power for specific OTA topologies

The overall power dissipation for sinusoidal inputs can now be derived for the different OTA topologies. Let us first assume a high *OSR*, so that any sampled value of the sinusoidal signal can be treated as a quasi-static input [54].. We will consider the input signal to be $x = b + a\sin\omega t$, where b is the DC bias set to $V_{ref}/2$ (b = 1/2), and a is the amplitude (a=OL/2), with OL standing for the overload level.

To simplify the formulas, the power consumption is divided by the factor $C_s \cdot V_{ref} \cdot V_{DD} \cdot f_s$, to obtain the normalized power $\hat{P}(x)$. The final static power model is derived in the following sub-sections for both class-A OTAs and class-AB OTAs.

3.2.5.5 Static power model of class-A OTAs

Since the supply current in a class-A OTA is fixed, the OTA should be designed to handle the largest charge transfer. Therefore, the minimum power required during the large-signal period is equal to the largest of the two values that the expression (26) can assume, i.e.:

$$\hat{P}_{la,A}\left(x,k(t)\right) = \max\left(\left|\frac{k(t)}{2^B-1}-x\right|,\left|\frac{k(t)}{2^B-1}+x\right|\right) = \frac{k(t)}{2^B-1}+|x| \qquad (27)$$

If the maximum value of the sinusoidal signal x is $b+|a| = \frac{1}{2}+\frac{OL}{2}$, the corresponding power will be:

$$\hat{P}_{la,A} = \frac{k(t)}{2^B - 1} + \frac{1}{2} + \frac{OL}{2} \tag{28}$$

The total normalized power consumption of a class-A OTA can thus be found from(20), (24) and (28):

$$\hat{P}_A = \alpha\theta \cdot \left(\frac{k(t)}{2^B - 1} + \frac{1}{2} + \frac{OL}{2} \right) + \beta\varsigma \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s} \right) \tag{29}$$

3.2.5.6 Static power model of class-AB OTAs

Class-AB OTAs adaptively adjust their output current depending on the required output voltage, and thus to the needed charge transfer in a SC circuit. Therefore, their average power dissipation during the large-signal period will be a function of the actual signal x and of the normalized DAC feedback signal $\frac{k(t)}{2^B - 1}$. Given a certain sampled value of x, the output of the ΔΣM will toggle between two digital B-bit output values with a certain statistics. The statistics will be different depending on where x is with respect to the two closest quantization levels. As a result, the DAC feedback will toggle, with the same statistics as the ΔΣM output, between the two DAC levels, k1 and k2, which are the closest to x, above and below._We can thus express the average power dissipation in (26) as:

$$\hat{P}_{la,AB}\left(x, k(t)\right) = P_{la,AB}\left(x, k1\right) \cdot f\left(x, k1\right) + P_{la,AB}\left(x, k2\right) \cdot f\left(x, k2\right) \tag{30}$$

where $P_{la,AB}(x,k1)$ and $P_{la,AB}(x,k2)$ are the power consumptions associated to the DAC feedback values $k1$ and $k2$, respectively. $f(x,k1)$ and $f(x,k2)$ are the probability of $k1$ and $k2$ given the value of x. The values of $f(x,k1)$ and $f(x,k2)$ can be found as

a function of x and B [7]. The average power dissipation during the large-signal period can thus be expressed for a certain sampled value of x as:

$$\hat{P}_{la,AB}\left(x,k(t)\right)=\frac{k(t)}{2^B-1}-\left(2^B-1\right)\cdot x^2 \tag{31}$$

The normalized average power dissipation is finally obtained by time-averaging (31) over one signal period T:

$$\begin{aligned}\hat{P}_{la,AB}&=\frac{1}{T}\int_0^T\left[\frac{k(t)}{2^B-1}-\left(2^B-1\right)\cdot\left(b+a\sin\omega t\right)^2\right]dt=\\&=\frac{1}{T}\int_0^T\left[\frac{k(t)}{2^B-1}-\left(2^B-1\right)\cdot\left(\frac{1}{2}+\frac{OL}{2}\sin\omega t\right)^2\right]dt\end{aligned} \tag{32}$$

This equation allows us to average over all the possible values of the sinusoidal signal x. Please note that, contrary to [54]., a closed form cannot be found for this integral as it includes the feedback signal $k(t)$, which varies during the period T. $k(t)$ is indeed a B-bit representation of V_{in}. The total normalized power consumption of a class-AB OTA is finally derived from (20), (24) and (32) as:

$$\hat{P}_{AB}=\alpha\theta\cdot\frac{1}{T}\int_0^T\left[\frac{k(t)}{2^B-1}-\left(2^B-1\right)\cdot\left(\frac{1}{2}+\frac{OL}{2}\sin\omega t\right)^2\right]dt+\beta\varsigma\cdot\left(\frac{5\cdot2\pi\cdot n\cdot V_{Th}\cdot C_{eq}}{V_{ref}\cdot C_s}\right) \tag{33}$$

The total normalized power dissipations in (29) and (33) are summarized in Table II for class-A and class-AB OTAs.

---

[7] In the appendix of [47] the expressions of $f(x,k1)$ and $f(x,k2)$ are derived for single-bit modulators. We follow the same procedure here to derive $f(x,k1)$ and $f(x,k2)$ for multi-bit ΔΣMs.

TABLE II
STATIC POWER DISSIPATION FOR SINUSOIDAL INPUTS

OTAs	Normalized power dissipation
Class-A	$\hat{P}_A = \alpha\theta \cdot \left(\frac{k(t)}{2^B - 1} + \frac{1}{2} + \frac{OL}{2} \right) + \beta\varsigma \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s} \right)$
Class-AB	$\hat{P}_{AB} = \alpha\theta \cdot \frac{1}{T} \int_0^T \left[\frac{k(t)}{2^B - 1} - \left(2^B - 1\right) \cdot \left(\frac{1}{2} + \frac{OL}{2} \sin \omega t \right)^2 \right] dt + + \beta\varsigma \cdot \left(\frac{5 \cdot 2\pi \cdot n \cdot V_{Th} \cdot C_{eq}}{V_{ref} \cdot C_s} \right)$

3.2.5.7 Static-power comparison of class-A and class-AB topologies

We can now compare the power dissipation of different OTA topologies to determine the power-optimal OTA to be used in a ΔΣM with given (*N*, *B*). Current-mirror and folded-cascode OTAs are listed here as examples of class-A OTAs while the "Castello" topology [58] is used as an example of a class-AB OTA. Telescopic OTAs are not considered, despite their power-efficiency, because they are not suitable for low-voltage operation, which is the focus of this work. Fig. 14 shows the simplified circuit schematics of the OTA topologies.

Table III provides the constants a, β, θ, ζ corresponding to each circuit. M is the current mirror ratio in Table III and Fig. 14 (a) and (c). F is defined as $F = I_{bias} / I_{tail}$ where I_{bias} is the extra current used for biasing the class-AB output branch and I_{tail} is the OTA tail current (Table III and Fig. 14 (c)). We assume that the minimum value of I_{bias} and I_{tail} is 50nA for matching purposes. When applying these formulas in our designs and in our comparison, we will always set F to 0.25, 0.5 or 1 to reduce the design space while considering the aforementioned matching constraint. The ratio between the sampling and the integration time is γ, with

$\gamma = T_{sam} / T_{int}$ (typically γ=1).

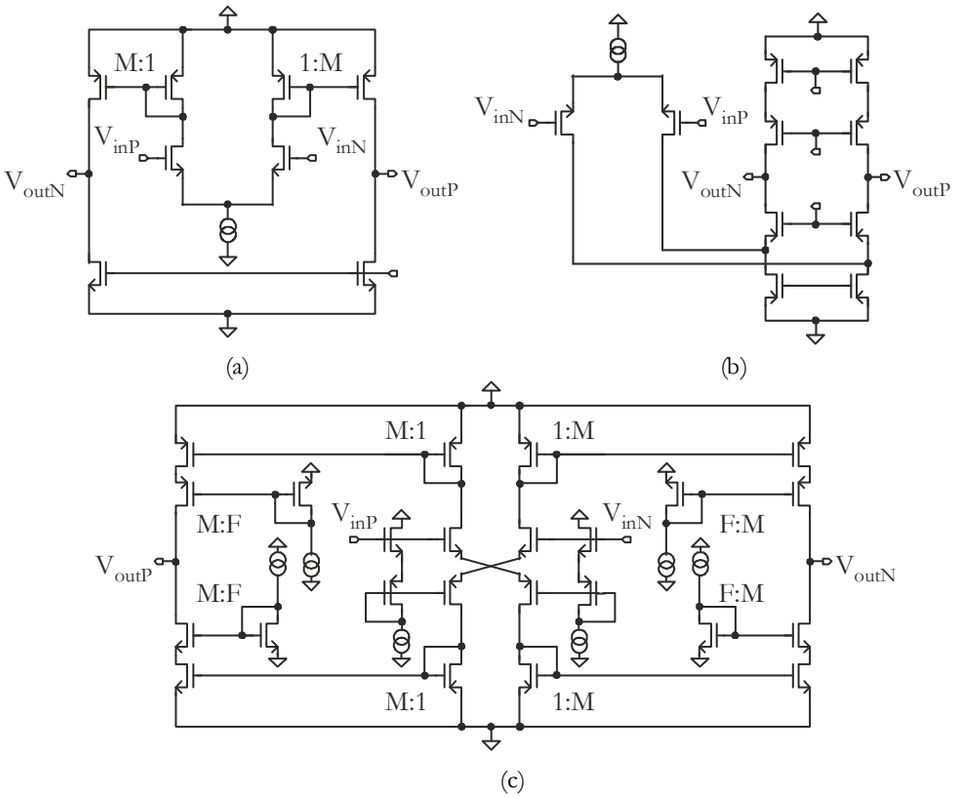


Fig. 14. Simplified circuit schematic for current-mirror (a) OTA, folded-cascode OTA (b) and Castello OTA (c) [58]

TABLE III
COEFFICIENTS FOR VARIOUS OTAS

Topology	a	β	θ	ζ
Current-mirror	$\frac{1+M}{M}$	$\frac{1+M}{M}$	$1+\gamma$	$1+\gamma$
Folded-cascode	2	2	$1+\gamma$	$1+\gamma$
Castello [48]	$\frac{1+M+F}{M}$	$\frac{1+M+F}{M}$	1	$1+\gamma$

Fig. 15 illustrates the behaviour of the normalized static power with respect to B (number of bits in the quantizer) for N=3. In the single-bit configuration, the class-AB OTA is power-optimal. The OTA is indeed required to provide large output current due to the large feedback signal inherent in single-bit ΔΣ modulators. As B grows, class-A current-mirror OTAs become more and more power efficient. In multi-bit topologies, indeed, the difference between the input and the feedback signals is smaller and class-AB OTAs mostly show small-signal behaviour. With respect to class-A OTAs, they thus pay the power penalty of the extra current used for biasing the class-AB output branch. Class-A folded-cascode topologies always show the worst power performance in the comparison.

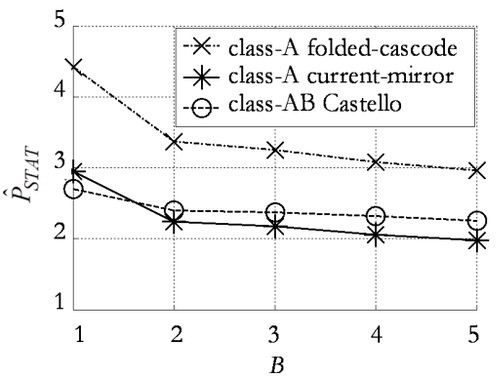


Fig. 15. Normalized power dissipation of class-A and class-AB topologies as a function of B for N=3

3.2.6 Dynamic power

The dynamic power for charging a capacitor C_{TOT} at the frequency f_s to the reference voltage is [35]:

$$P_{DYN} = V_{ref}^{\ 2} \cdot C_{TOT} \cdot f_s \tag{34}$$

C_{TOT} is the total capacitance commuting in the ΔΣM and can be expressed respectively for FB and FF topologies as:

$$C_{TOT,FB} = 2\sum_{i=1}^{N} C_{s,i}\left(1+\frac{1}{a_i}\right) \tag{35}$$

$$C_{TOT,FF} = 2\cdot C_{s,1}\left(1+\frac{1}{a_1}\right). \tag{36}$$

Considering fully-differential circuitry, C_{TOT} includes 4xN capacitances (all the sampling and integrating capacitors) in FB topologies and 4 capacitors (the sampling and integrating capacitors of the first integrator) in FF topologies. In the former case, indeed, we always have more than one DAC (up to N) in the feedback path. In the latter case, we just have one DAC in the feedback path, at the input of the ΔΣM; the capacitors of other integrators and the feed-forward capacitors have negligible sizes.

3.2.7 Quantizer power

The power consumption of the quantizer is estimated for three different architectures, which are commonly used in discrete-time ΔΣMs. The analysis is made here for a single-bit comparator-based quantizer, for a multi-bit flash quantizer and for a successive-approximation quantizer.

3.2.7.1 Single-bit comparator-based quantizer

The power consumption of a dynamic single-bit comparator-based quantizer is estimated using the results in [59] as:

$$P_{COMP} = \frac{V_{eff}}{\eta} V_{DD} L_{min} OSR\cdot\left(2\cdot BW\right) \tag{37}$$

where V_{eff} is the effective voltage $V_{eff} = \delta V_{DD} - \varepsilon V_{SW}$ of the circuit, V_{DD} is the supply voltage, V_{SW} is the input signal swing , η is a power-efficiency parameter and L_{min} is the gate length for the used technology . The parameters δ, ε, η are

derived from transistor level simulations in [41] (δ=0.6, ε=0.3, η=32100) .We have verified the reliability of these values through data fitting with experimental values obtained from [46]. For the sake of simplicity, we don't consider the constraint on the comparator's offset in this power estimation. Clearly, this constraint impacts the comparator's power consumption and is dependent on B as it has a stronger impact in multi-bit quantizers than in single-bit ones.

3.2.7.2 Multi-bit flash quantizer

The B-bit flash quantizer is assumed to be implemented as in [47]: the ADC thresholds are generated by a resistor ladder and the rail-to-rail input range of the comparator is ensured by the SC level shifter network in Fig. 16. During one phase (φ_2), the threshold voltages are sampled on the capacitor of the SC level shifter C_{LS}; during the other phase (φ_1), the pre-charged capacitor is connected to the input signals [47].

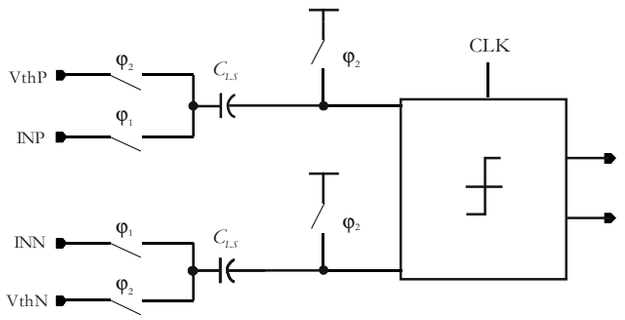


Fig. 16. Circuit implementation of the fully-differential comparator

The power dissipated by a B-bit flash quantizer can be written as:

$$P_{FLASH} = \left(2^B - 1\right) \cdot P_{COMP} + P_{ENC} + P_{RES} \tag{38}$$

where 2^B-1 is the number of comparators, and P_{ENC} is the power consumption of the encoder , usually negligible; P_{RES} is the power consumption of the resistor ladder

which generates the ADC thresholds: $P_{RES} = \frac{V_{DD}^{\ 2}}{R_T}$ where R_T is the total value of the resistor ladder . The resistor ladder is dimensioned for appropriate settling of the ADC thresholds during φ_2. If the ADC thresholds have to settle with an accuracy better than $2^{-(B+1)}$, the settling time T_{sett} must be $T_{sett} > \tau \cdot (B+1) \cdot ln(2)$, τ being the settling time constant for the resistor ladder . Considering the simplified model of the resistor ladder shown in Fig. 17, $\tau = \left(\frac{R_T}{4} + 2R_{SW} \right) \cdot C_{LS}$, where R_T is the total value of the resistor string, R_{SW} is the switch resistance (assumed negligible since its value is small with respect to R_T), and C_{LS} is the capacitor of the SC level shifter.

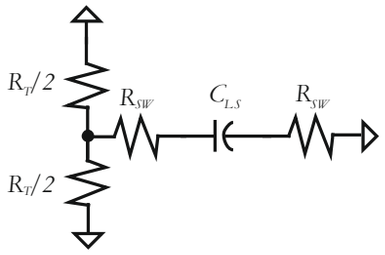


Fig. 17. Simplified model of the resistor ladder generating the thresholds of the flash ADC

Recalling that the time allowed for settling is one phase (half-clock period), so $\frac{T_S}{2} = \frac{1}{2 \cdot (2 \cdot BW \cdot OSR)}$, we get:

$$R_T < \frac{1}{BW \cdot OSR \cdot C_{LS} \cdot (B+1) \cdot ln(2)} \tag{39}$$

Using (38) and (39) a minimal value of the power consumption can be found:

$$P_{FLASH} = \left(2^B - 1\right) \cdot P_{COMP} + V_{DD}^{\ 2} \cdot BW \cdot OSR \cdot C_{LS} \cdot (B+1) \cdot ln(2) \tag{40}$$

3.2.7.3 Multi-bit SAR quantizer

The simplified representation of a SAR ADC using a conventional *B*-bit binary weighted capacitor DAC is shown in Fig. 18 (a). Its power consumption can be estimated as:

$$P_{SAR} = B \cdot P_{COMP} + 2V_{DD}{}^2(1+0.5) \cdot 2^B \cdot C \cdot (2BW \cdot OSR) + P_{LOGIC} \quad (41)$$

where B is the quantizer resolution and $2^B \cdot C$ is the total capacitance of the SAR DAC array (C is the unit capacitor of the binary-scaled capacitive array). P_{LOGIC} is the power consumption of the SAR logic (considered negligible compared to the other terms in the formula).

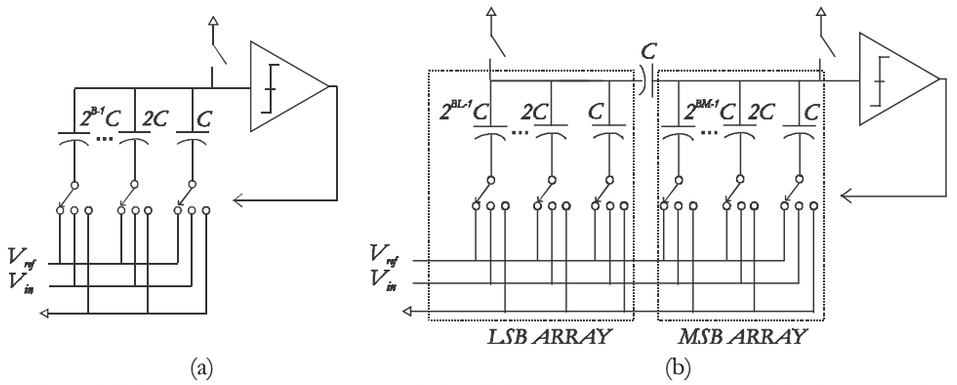


Fig. 18. Schematic representation of a SAR ADC using (a) a conventional *B*-bit binary weighted capacitor DAC (b) a "split" *B*-bit capacitor DAC with unit value bridge capacitor.

The estimation in (41) assumes that B comparisons are necessary per ADC conversion. The term (1+0.5) is introduced because each capacitor in the DAC is set once, at the beginning of the SAR conversion. Depending on the outcome of the comparisons, each DAC capacitor is kept charged or discharged again. If the capacitor is kept charged, there is no additional power consumption. If it is discharged, there is an additional term of dynamic power, since the DAC is differential and the complementary capacitor will be charged. Assuming that the

outcome of the comparator is uniformly distributed between 'ones' and 'zeros', on average this second term happen in 50% of the cases.

Alternative architectures are available for the implementation of a SAR DAC array called "segmented" or "split" architectures [60]. In these arrays, an attenuation capacitor is used to separate the capacitive DAC into B_M-bits MSB and B_L-bits LSB arrays (B_M+B_L=B). Thus, smaller capacitor ratios can be achieved as compared to the binary weighted capacitive array. In Fig. 18 (b), a unit bridge capacitor architecture is shown in which the total weight of the *LSB* array achieves the same weight as the lowest bit in the *MSB* array. The power consumption of this "split" *B*-bit SAR ADC can be estimated as:

$$P_{SAR} = B \cdot P_{COMP} + 2V_{DD}{}^2(1+0.5)\left(\sum_{i=1}^{B_L} C_{eq,Vref_i} + \sum_{j=1}^{B_M} C_{eq,Vref_j}\right)(2BW \cdot OSR) + P_{LOGIC} \quad (42)$$

where $C_{eq,Vref\,i}$ and $C_{eq,Vref\,j}$ are the equivalent capacitances of the B_L and B_M capacitors with respect to the reference voltage V_{ref}, respectively.

Please note that in the power estimations of Section 3.2.10.3 and Section 4.2.2 the formula in (41) will be used for simplicity. This same formula is reported in Table IV for reference.

3.2.8 DWA Power

The power penalty to correct for capacitor mismatch errors is calculated considering a first-order data weighted averaging approach. The dynamic power dissipation of CMOS digital gates can be expressed as:

$$P_{DWA} = \sum_{m=1}^{K} \psi_m \cdot C_{in,m} \cdot V_{DD}{}^2 \cdot f \quad (43)$$

where K is the number of the internal nodes, ψ_m is the switching activity of each node m, and $C_{in,m}$ is the parasitic capacitance of each internal node m [61].

The DWA architecture contains a binary-to-thermometer converter which is implemented by means of logic gates, a $(2^B\text{-}1)$-bit barrel shifter and a B-bit accumulator as illustrated in Fig. 19 [51].

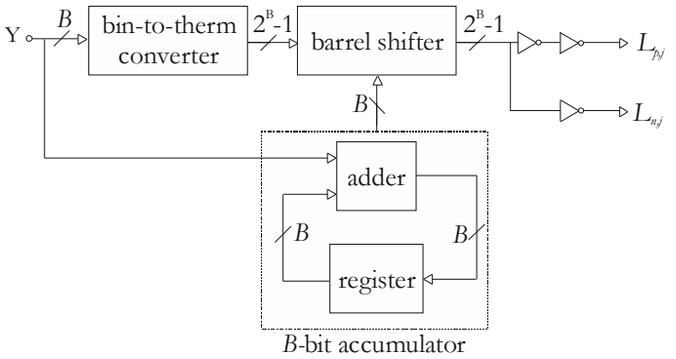


Fig. 19. Practical implementation of the DWA

The barrel shifter is implemented using $2^B \cdot \log_2 2^B = B \cdot 2^B$ multiplexers (MUXs) and 2^B inverters. Each MUX is equivalent to two switching inverters. The B-bit accumulator comprises a B-bit adder and a B-bit register. Assuming each internal node loaded only by the gates connected to that specific point and expressing the equivalent load of any logic gate as a multiple of the inverter equivalent load, the power dissipated can be approximated as ($\psi_m \approx 1$):

$$P_{DWA} = V_{DD}{}^2 \cdot C_{inv} \left(2BW \cdot OSR\right) \cdot \left[\left(2^B - 1\right)\left(B+1\right) + \sum_{n=0}^{B-1} \left(2^B - 2^n\right) + 8B \right] \tag{44}$$

where C_{inv} is the equivalent input capacitance of a minimum size inverter. According to [62], C_{inv} is assumed here to be 10fF for a minimum-size 0.18μm CMOS inverter.

The DWA power contribution is not added to the total power consumption for architectures with B=1, as linearity is not a concern in single-bit designs.

3.2.9 Total Power consumption

All formulae needed to estimate the different contributions to power consumption are summarized in Table IV. Note that the formulae for the (normalized) power $\hat{P}_{A,i}$ and $\hat{P}_{AB,i}$ are already shown in Table II.

TABLE IV
ΔΣM POWER CONTRIBUTIONS

P_{STAT}	*Class-A*	$P_{STAT-A} = V_{DD} \cdot (2BW \cdot OSR) \cdot V_{ref} \cdot \sum_{i=1}^{N} C_{s,i} \cdot \hat{P}_{A,i}$
	Class-AB	$P_{STAT-AB} = V_{DD} \cdot (2BW \cdot OSR) \cdot V_{ref} \cdot \sum_{i=1}^{N} C_{s,i} \cdot \hat{P}_{AB,i}$
P_{DYN}		$P_{DYN} = V_{ref}^{\ 2} \cdot C_{TOT} \cdot (2BW \cdot OSR)$
P_{QUANT}	*Single-bit comparator*	$P_{COMP} = \frac{V_{eff}}{\eta} V_{DD} L_{\min} (2BW \cdot OSR)$
	Multi-bit Flash	$P_{FLASH} = (2^B - 1) \cdot P_{COMP} + + V_{DD}^{\ 2} (B+1) \cdot C_{LS} ln(2) \cdot (BW \cdot OSR)$
	Multi-bit SAR	$P_{SAR} = B \cdot P_{COMP} + + 2V_{DD}^{\ 2} (2^B - 1) \cdot 1.5 C_{SA} (2BW \cdot OSR)$
P_{DWA}		$P_{DWA} = V_{DD}^{\ 2} \cdot C_{inv} (2BW \cdot OSR) \cdot \cdot \left[(2^B - 1)(B+1) + \sum_{n=0}^{B-1} (2^B - 2^n) + 8B \right]$

3.2.10 Power optimization of a ΔΣM for hearing aids application and impact of design parameters on power consumption

The presented power estimation methodology has been applied to a ΔΣ modulator able to achieve an *SNDR* of 86dB (*ENOB*=14) within a 10-kHz signal bandwidth, in order to clarify the impact of the design parameters on power consumption. These values of resolution and bandwidth have been selected as they are the target requirements for the design that will be illustrated later (see Section 3.4). For a 0.18μm CMOS technology, the order of the loop filter has been limited to 4, and the resolution of the internal quantizer to 5bits. The *OSR* is swept between 8 and 128. When choosing the *OSR* for the actual implementation, only powers of 2 are considered as candidate, to simplify the design of the decimation filter. It turns out that orders higher than N=2 are needed to achieve the target resolution for this *OSR* range. In the following figures, missing and incomplete curves represent (*N, B, OSR*) combinations with insufficient resolution. FF topologies are applied to any combination of (N, B) able to achieve the target resolution as long as $B \geq N$, following the rule of thumb for stability proposed in [62].

A supply voltage V_{DD} of 1.8 V has been assumed to overcome any switch-driving problem. P_{QUANT} has been calculated both for a multi-bit flash quantizer and for a multi-bit SAR quantizer. These two approaches reflect the quantizer design choices of Section 3.4.1 and 3.4.2, respectively. The reference voltage V_{ref} is assumed to coincide with V_{DD} in both FB and FF topologies. The switching energy of a minimum size inverter is estimated from [63] to about 5fJ, corresponding to a capacitance C_{inv} of 10fF per logic node.

The performance of single-loop architectures is also greatly influenced by the in-loop coefficients (a_i and c_i) in Fig. 9 (a) and (b). On the one hand, these coefficients

have to be selected to provide a stable operation in the whole input range [64]. On the other hand, they can be scaled in order to reduce the swing at the outputs of the integrators with respect to the reference voltage [45]. In this case, the values of the loop coefficients have been selected using the function *scaleABCD* in the toolbox [50], being adjusted such that the integrators output range is 50% of the reference level. They have thus been set to a_1=4, a_2=9/5, c_1=7/15, c_2=2/15. Moreover, in SC modulators, these coefficients are implemented as ratios of capacitors. Due to process variations, these capacitors will be slightly different from their intended value. Extensive behavioural simulations have shown that variations as large as 2% do not degrade the performance of the ΔΣM for the target resolution. Considering the matching properties of capacitors in a 0.18μm CMOS technology, the minimum size for the sampling capacitors in the integrators following the first $C_{s,i}$ (i>1) has been set accordingly to 50fF. The constraints on these capacitances are far less stringent than the one for $C_{s,1}$, given by (17), as errors introduced by the subsequent integrators are shaped by the transfer function of the previous ones.

3.2.10.1 Static Power

As can be seen in Fig. 20, the static power increases with N; according to the expression of P_{STAT} in Table IV this contribution increases indeed with the number of integrator stages.

Moreover, P_{STAT} decreases with increasing B. This is because the use of a multi-bit quantizer in the ΔΣ modulator reduces the quantization noise and improves the stability of the ΔΣM loop; the voltage levels at the integrators' outputs are thus reduced and the allowed OL levels become larger.

As a consequence, the maximum input signal of the converter increases, and the minimum required $C_{s,1}$ decreases according to (13), lowering P_{STAT} as shown in (22), (29) and (33). This effect is present for all the orders. The only exception to this

general trend is for single-bit FB topologies, for which power-efficient class-AB OTAs are used (see Fig. 15).

Fig. 20 shows that it is only possible to reach a good trade-off between thermal noise power and quantization noise power contributions (the local minimum in the curves) for low *OSR*s. The OTA static power indeed increases with *OSR* through its *GBW*; at the same time, it includes $C_{s,1}$ and $C_{s,i}$ (see (45) and (46)). At low *OSR*, $C_{s,1}$ and $C_{s,i}$ decrease with *OSR* increasing. At low *OSR*, the proportionality of the static power to *OSR* can be approximated as:

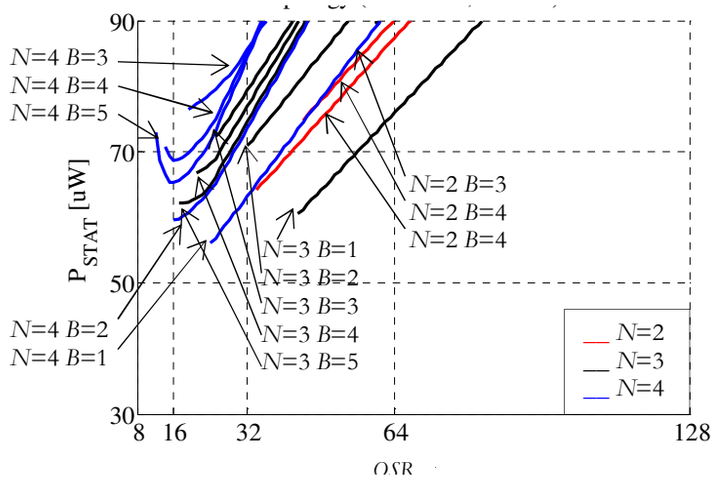
$$P_{STAT} \sim OSR \cdot \left(C_{s,1} + \sum_{i=2}^{N} C_{s,i} \right) \sim k + \frac{1}{OSR^{2i-2}} \tag{45}$$

At high *OSR*, $C_{s,1}$ and $C_{s,i}$ reach the minimum value determined by matching requirements. Therefore, in this case they are constant and:

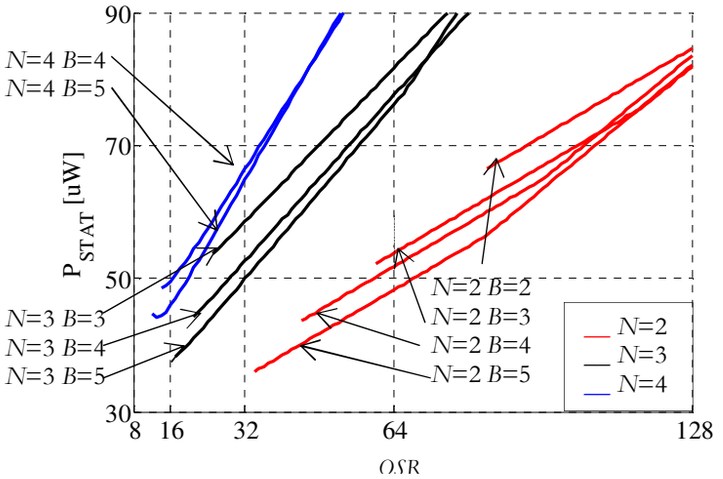
$$P_{STAT} \sim OSR \cdot \left(C_{s,1} + \sum_{i=2}^{N} C_{s,i} \right) \sim OSR \cdot k \tag{46}$$

In this design example, $C_{s,i}$ (i>1) are always set to the minimum value given by matching requirements, already at low *OSR*. The discontinuity in the curves in Fig. 20 (b) is due to the different limiting factors to find $C_{s,1}$ at low and high values of *OSR*s, respectively: at low *OSR*s, $C_{s,1}$ is thermal noise limited and scaled according to (13); at high *OSR*s, $C_{s,1}$ becomes matching limited, and P_{STAT} increases with *OSR*.

As FF topologies have higher *OL* levels, they need smaller $C_{s,1}$ for the same *OSR* (see(13)); for this reason, they present better power performance with respect to FB topologies.



(a)



(b)

Fig. 20. Static Power estimation as a function of *OSR* in FB (a) and in FF (b) implementations

3.2.10.2 Dynamic Power

As shown in Fig. 21. , the behaviour of P_{DYN} with respect to the filter order N is similar to that observed for P_{STAT} as it also depends on the values of the sampling capacitors (see (35) and (36)).

In FB topologies (see Fig. 21. (a)), P_{DYN} increases with N because the number of feedback branches increases with the order of the filter. FF topologies instead have only one feedback branch connected to the converter input. Since P_{DYN} is less influenced by N, the curves relative to different orders for FF ΔΣM are close to each other. P_{DYN} increases with B decreasing: increasing the quantizer resolution reduces P_{DYN} because of the smaller $C_{s,1}$ thanks to the larger OL.

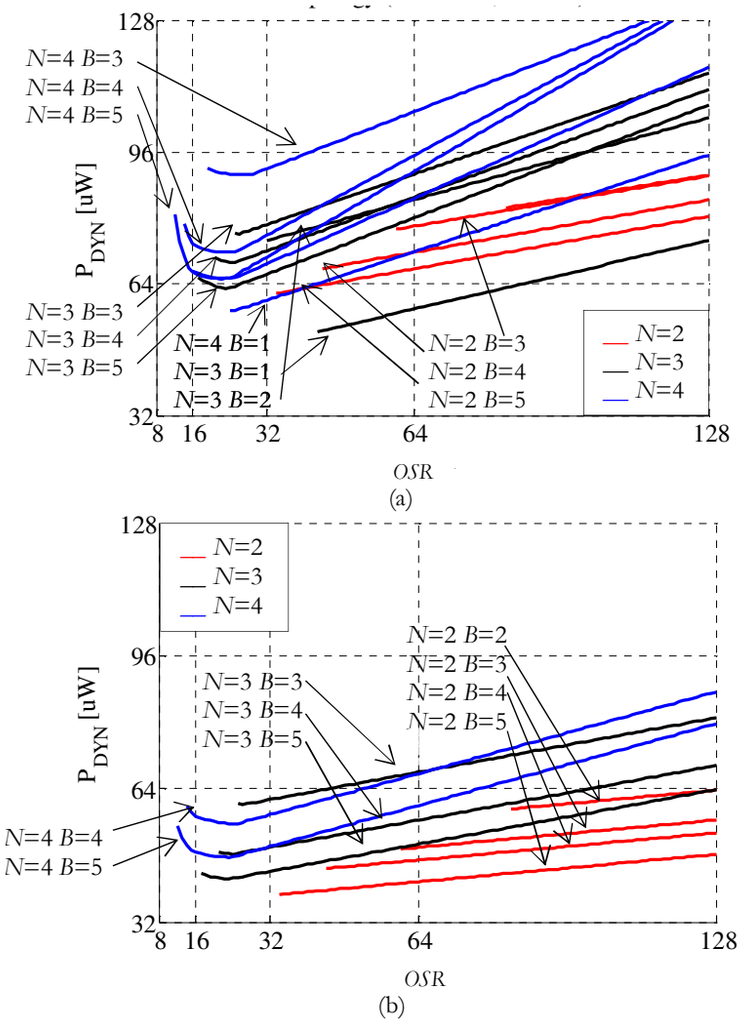


Fig. 21. Dynamic Power estimation as a function of OSR in FB (a) and in FF (b) implementations

3.2.10.3 Quantizer Power

The quantizer power does not vary with N and its estimation is the same for both FB and FF topologies. The flash and the SAR quantizer contributions are as shown in Fig. 22 (a) and (b), respectively.

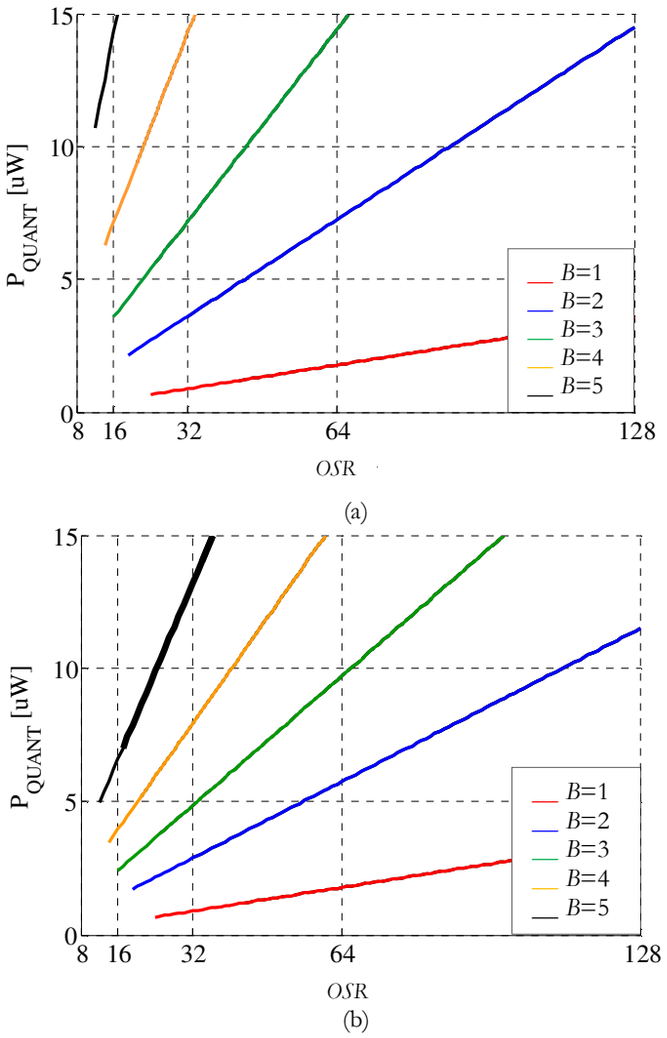


Fig. 22. Flash quantizer(a) and SAR quantizer (b) Power estimation as a function of *OSR* in FB and FF implementations

The flash contribution exhibits a 2x increase per additional quantizer bit, while the SAR quantizer contribution shows less dependency on *B*. Both contributions increase with *OSR*.

3.2.10.4 DWA Power

The power contribution related to the DAC mismatch-shaping system is shown in Fig. 23. The considerations made for the power estimation of flash and SAR quantizers above apply also to this case.

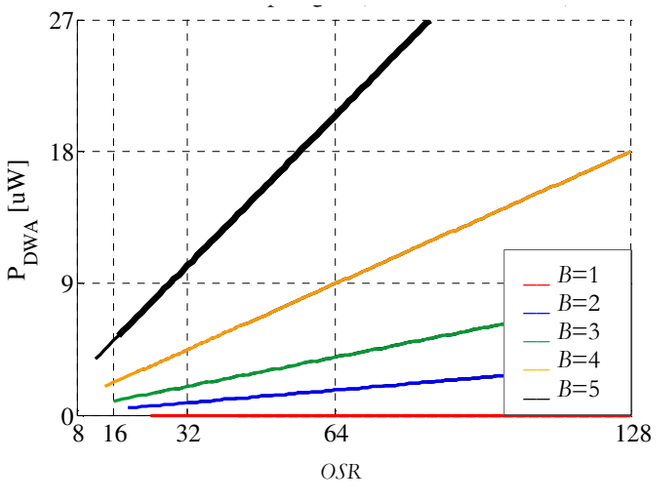
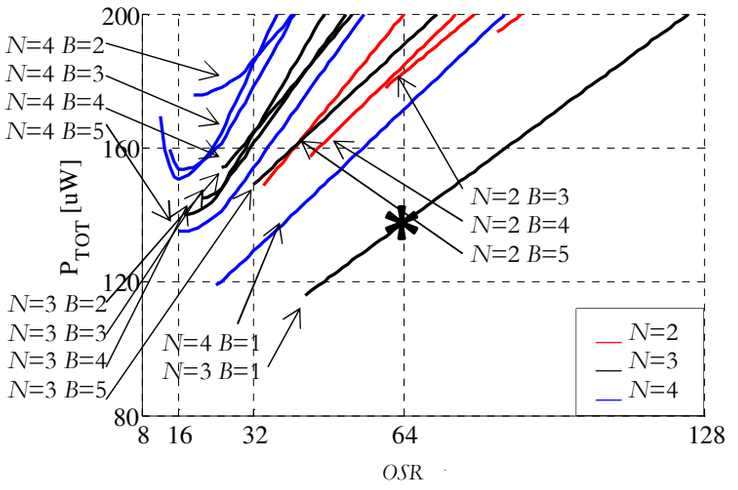


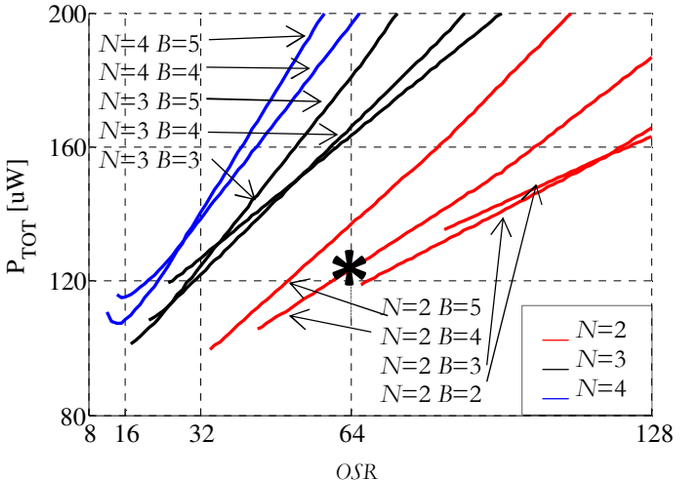
Fig. 23. DWA Power estimation as a function of *OSR* in FB and in FF implementations

3.2.10.5 Total Power consumption and global design considerations

The total power consumption P_{TOT} obtained for each topology (*N*, *B*) is plotted as a function of *OSR* in Fig. 24. A SAR quantizer has been assumed for the estimation of P_{QUANT}. The result would be similar if a flash quantizer was considered, as the power contributions of the two multi-bit quantizer choices are of the same order of magnitude and negligible in the total power consumption (see Fig. 22).



(a)



(b)

Fig. 24. Total Power estimation as a function of *OSR* in FB (a) and in FF (b) implementations. The minimum power consumption for both cases is marked with an asterisk.

FF topologies exhibit lower power consumption given the target bandwidth: the signal passing through the loop filter in low-distortion FF modulators is the quantization noise, which is much smaller in amplitude than the input signal [65].

Therefore, the ability to handle input signals is increased without overloading the modulator, and higher *OL*s minimize the sampling capacitor size according to (13).

The power-efficiency is higher for low-order circuit topologies: P_{STAT} and P_{DYN} terms dominate the overall power budget and their values are minimized for a small number of integrator stages *N*. In FB topologies, single-bit quantizers result in minimum power consumption thanks to the use of power-efficient class-AB OTAs which minimize the static power (see Fig. 15). In FF topologies, B=1 is not admitted as a solution because the loop is not stable in architectures in which $N<B$ [62]. The best efficiency is achieved for B=4. *OSR* is approximately 64, so that f_s= 1.28 MHz. The result of this power optimization methodology is confirmed by recent works in literature. Indeed, very good power-efficiency has been reported recently for a second-order, 4-bit ΔΣM as in [66]; this implementation chooses indeed to dimension the capacitances following the procedure for C_s described in Section 3.2.3 and targets similar resolution and bandwidth as in this example.

FF topologies are generally prone to timing problems. Both the analogue addition (at the input of the quantizer) and the quantization are indeed performed during φ_1. This constraint reduces the time available for the OTAs to settle to the required accuracy [67]. Also, especially in multi-bit SC implementations, the timing of the quantization and feedback blocks (the DWA in our case) becomes more critical than in single-bit and potentially power hungry. In our model conservative choices are made to ensure sufficient DAC settling and OTAs bandwidth. The timing difficulties in the quantization and feedback blocks, on the other hand, are easily solved for the low-frequency applications that we target: in Section 3.4 more details are given on how to distribute the timing signals without creating any critical path.

Since the power optimization obtained with this study is based on the assumption that *SNR*=*SNDR* (see Section 3.2), the power curves in Fig. 24 should

be considered in general as a lower limit, obtained for single loop designs that are not limited by linearity issues. It is however useful to analyse in a qualitative way the impact of linearity on the different single-loop architecture choices (feedback or feed-forward topologies, single-bit or multi-bit) and to test if our choice for multi-bit FF topologies would remain valid when linearity issues are considered as well. Our discussion will always be restricted to the hypothesis of high-resolution low-bandwidth SC ΔΣMs.

The main causes of non-linearity in SC ΔΣ modulators, besides the mismatch in the DAC, are: the non-linear OTA gain, the non-linear settling of the integrators, non-linear capacitances and the non-linear switches [46]. In submicron technology, the problem of non-linearity coming from the non-linear OTA gain is severe, because the low-voltage environment imposes stringent limitations on the OTAs headroom. In FB topologies the gain non-linearity of the OTA causes large harmonic distortion in the modulator because the non-linearity of the loop filter affects the signal quality; in FF topologies, this problem is solved by the inherent unity signal transfer function of the ΔΣM. As a consequence, in FF topologies, DC gain and linearity requirements of the OTAs used to implement the integrators are relaxed [46]. Moreover, in FB topologies, there is a dependence of the input of the first integrator on the modulator input. This may result in a large signal at the integrator input which can cause slewing in the OTA and, in turn, distortion. In FF topologies, the input of the first integrator no longer depends on the modulator input and the signal range can be reduced by employing multi-bit quantization [62]. Summarizing, it is thus expected that FB topologies will require higher OTA linearity and faster settling, causing an even higher power consumption than the one calculated with our approach, and thus reinforcing the validity of our choice of FF topologies for low-bandwidth specifications. It is true that multi-bit modulators require very good matching between circuit elements in the feedback DAC, but this

linearity limitation is already taken into account in our design methodology (and thus in Fig. 24), as the matching requirement on the capacitors in the DAC and the power overhead due to the DWA are included in multi-bit implementations. Finally, in modern CMOS technologies, the MIM capacitance linearity is quite good and the non-linear switch problems can be solved easily with power-friendly techniques [46].

3.2.11 Results of the power optimization procedure

The results of the power optimization of Section 3.2.10 are summarized in Table V. The values of loop coefficients are reported here, together with the size of the first integrator's sampling capacitor. The power breakdown is detailed, too.

TABLE V
ΔΣM POWER-OPTIMAL ARCHITECTURE AND POWER BREAKDOWN

PARAMETER	VALUE
***Signal BW* [Hz]**	10K
***Target SNDR* [bits]**	14
Topology	Feed-forward
a_1, a_2, c_1, c_2	$4, 9/5, 7/15, 2/15$
N	2
B	4
OSR	64
$C_{s,1}$ **[pF]**	1.92
P_{TOT} **[μW]**	124
***ENOB* [bits]**	15.4*
***FoM*[pJ/c.s.]**	0.13
P_{STAT} **[μW]**	53
P_{DYN} **[μW]**	48
$P_{SA\text{-}ADC\,QUANT}$ **[μW]**	14
P_{DWA} **[μW]**	9

* Based on the target resolution specified for the model. This value includes a 10dB design margin, as explained in Section 3.2.2.

The ΔΣM specifications are a nominal 86 dB *SNDR* within a 10-kHz input signal bandwidth, with minimal power consumption. The best power-efficiency is obtained by employing a second order feed-forward architecture with a 4-bit quantizer and an *OSR* of 64. P_{STAT} has been calculated assuming class-A current-mirror OTAs, as this architecture minimizes the static power contribution for this combination of (*N*, *B*) (see Fig. 15). P_{QUANT} is reported for a 4-bit SAR quantizer. The result of this power optimization methodology is confirmed by recent works in literature targeting similar resolution and bandwidth as this study. Indeed, very good power-efficiency has been reported recently for feed-forward second-order multi-bit ΔΣMs, with 4-bit [66] or 5-bit quantizers [68]- [69].

3.3 Design techniques for power-efficient SC feed-forward ΔΣMs

In feed-forward topologies the input signal X and the integrators' outputs X_i, scaled by the feed-forward coefficients c_i, are added at the input of the quantizer. This is shown in Fig. 25 for a second-order multi-bit FF topology. In traditional multi-bit FF topologies, the quantizer and the analogue summation block have a strong impact on the total power budget due to high power consumption of the multi-bit flash ADC and of the active adder blocks that are typically used [70].There are two conventional ways to implement the analogue sum: active addition and passive addition. These techniques are summarized as a reference in Sections 3.3.1 and 3.3.2, respectively.

In Section 3.3.3 we present a novel approach called summing successive-approximation quantizer, which combines a SAR quantizer with a passive addition block. This solution enables analogue addition of the input signal (X) with the state

variables (X_1 and X_2 in Fig. 25) and multi-bit quantization with a very low power and area budget.

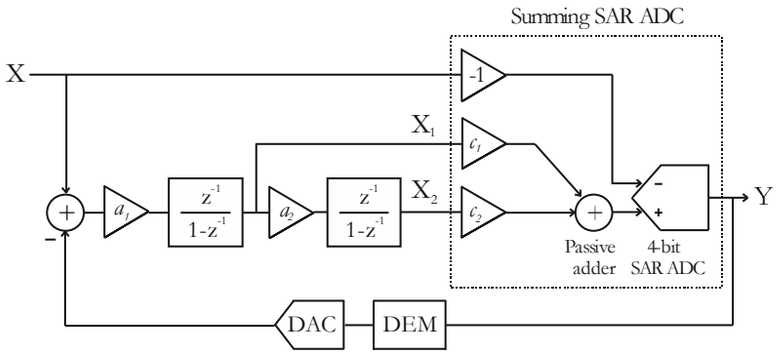


Fig. 25.Second-order 4-bit FF architecture

3.3.1 Active addition

In this case, a SC amplifier is used to add the signals without attenuating X_{out} due to capacitive division, as shown in Fig. 25 (a). At the end of the sampling phase φ_1:

$$X_{out} = X + c_1 \cdot X_1 + ... + c_N \cdot X_N \quad (47)$$

c_i is the feed-forward coefficient of the *i-th* integrator stage $c_i = C_{fi} / C_{f0}$ (for $i = 1, .., N$ being N the loop order).

To relax the quantizer offset requirements, X_{out} should have a rail-to-rail signal swing. Therefore, a two-stage OTA is typically used to meet the headroom requirements and provide enough gain. This approach is power hungry as adds a high-performance amplifier on top of the filter amplifiers in the ΔΣM architecture.

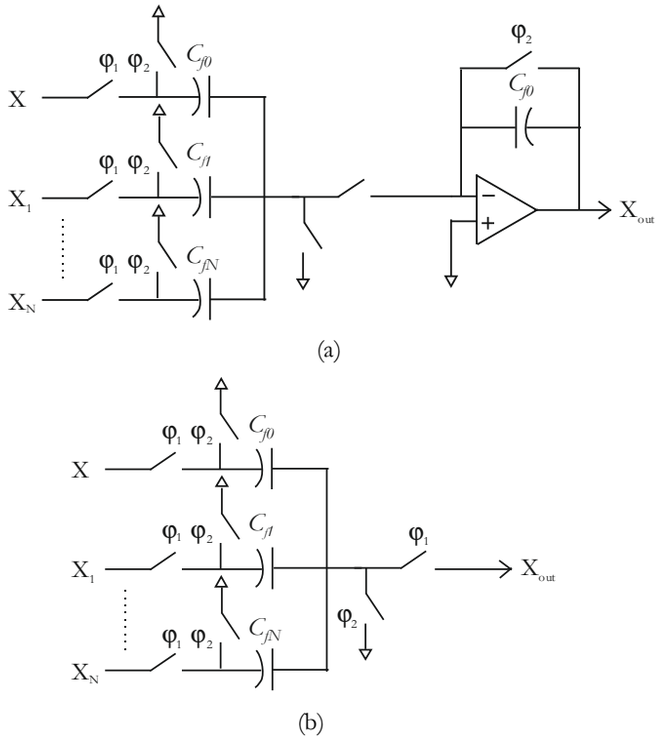


Fig. 26. Active addition (a) and passive addition (b)

3.3.2 Passive addition

A more power-efficient solution can be implemented summing the signals by means of passive charge sharing. Signal addition is implemented in this case with a SC network consisting of N switched branches as shown in Fig. 25 (b). If the sum of all coefficients c_i is smaller than one, the capacitors used to implement the FF coefficients are integer fractions of the capacitor C_{f0} so that $c_i = C_{fi} / C_{f0}$ for $i = 1, .., N$.

At the end of the sampling phase φ_1, the output signal is

$$X_{out} = \frac{X + c_1 \cdot X_1 + ... + c_N \cdot X_N}{1 + c_1 + ... + c_N} \tag{48}$$

which is attenuated by a factor $1 + \sum_{i=1}^{N} c_i$ with respect to (47). Although this approach eliminates the summing amplifier, the signal to be quantized X_{out} is attenuated, resulting in more stringent offset requirements for the quantizer. The use of offset cancellation techniques may become unavoidable, and this will typically result in a power penalty (think of, for instance, the use of preamplifiers).

3.3.3 The summing SAR quantizer

In this work, a novel summing SAR-ADC block is used to accomplish a two-fold function: the passive addition of the input signal with the integrators outputs without attenuation, and the multi-bit quantization of the resulting sum. A simplified representation of the summing SAR ADC is shown in Fig. 27 [43].

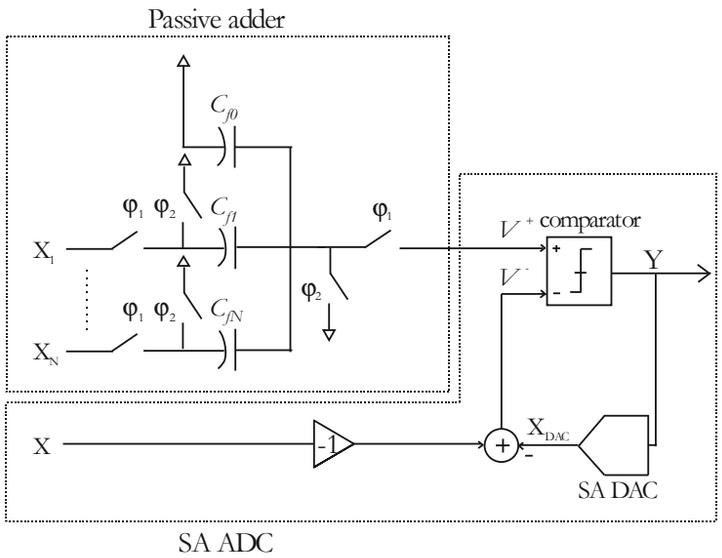


Fig. 27. Simplified representation of the summing SAR ADC

The passive addition block consists of the capacitors C_{f0}, and C_{fi} (i= 1,..,N) with C_{fi} connected to the outputs of the N integrators X_i. The weighted summation is implemented by charge sharing between the capacitors, which are sized according to the in-loop coefficients c_i of the FF modulator as:

$$\begin{aligned} C_{fi} &= c_i \cdot C_{tot} \\ C_{f0} &= (1-\sum_{i=1}^{N} c_i) \cdot C_{tot} \end{aligned} \tag{49}$$

with $C_{tot} = C_{f0} + \sum_{i=1}^{N} C_{fi}$.

As in (48), the comparator positive input signal V^+ is

$$V^+ = X_{out} = \frac{X_1 \cdot C_{f1} + ... + X_N \cdot C_{fN}}{C_{tot}} = \sum_{i=1}^{N} c_i X_i \tag{50}$$

The SAR-ADC block performs a binary search to determine the digital output code Y. Once the analogue input signal –X is sampled, the SAR algorithm converts it, one bit at a time, by comparing –X with its successive-approximation X_{DAC}, generated by the SAR DAC. During each cycle, the comparator, negative input signal V^- is:

$$V^- = X_{DAC} - X \tag{51}$$

As a result, the comparator takes decisions based on the input differential signal $V^+ - V^-$ which, from (50) and (51), is:

$$V^+ - V^- = \sum_{i=1}^{N} c_i X_i + X - X_{DAC} \tag{52}$$

According to (52), the overall quantizer input signal $X + \sum_{i=1}^{N} c_i \cdot X_i$ is converted in its digital representation Y by the summing SAR ADC without attenuation of the input signal. It is important to notice that the signal –X is always available in fully

differential implementations of the circuit, and thus no added circuitry is needed to generate it.

3.4 Design examples

Based on the results of the power-optimization of Section 3.2.10, two different implementations are presented here. In both designs, ΔΣM architectures are targeted to be used for hearing-aids applications, aiming at a *SNDR* of about 90dB (*ENOB*=14) within a 10-kHz signal bandwidth. Ideally, a hearing-aid should be able to process signals corresponding to sound pressure levels (SPL) ranging from the threshold of hearing to the level of discomfort. For a normal person, this corresponds to a dynamic range of 120 dB [71]. Such a *DR* value is very challenging for a ΔΣ ADC, and in order to achieve the large *DR*, it is necessary to take advantage of a variable gain amplifier to be employed as the microphone preamplifier [43]. In this way, requirements for the input *DR* of the ΔΣM can be relaxed to about 90dB. The signal bandwidth is designed to be 10kHz as this specification would suffice, even for high-end hearing-aids [71].

The first design, described in Section 3.4.1, is a second order FF ΔΣM with a 17-levels flash quantizer, which has been designed at transistor level in a 0.18μm CMOS technology. This implementation validates the results obtained with the presented power optimization procedure. It combines indeed multi-bit flash quantization and active addition and shows the power-efficiency limitations of such traditional multi-bit FF topologies. The second one, presented in Section 3.4.2, is a second order FF architecture with a 16-levels SAR quantizer. Fabricated in a 0.18μm CMOS technology, it features the novel summing SAR quantizer described in Section 3.3.3.

The power comparison between the two designs confirms the beneficial effect of the summing SAR ADC on power-efficiency.

3.4.1 A 95dB DR 10-kHz SC ΔΣM for digital hearing-aids application

Fig. 28. illustrates the implementation of the modulator, drawn as a single-ended circuit for simplicity; the actual implementation is fully differential. The ΔΣ modulator is designed at transistor-level and simulated in 0.18μm CMOS technology and operates with a supply voltage of 1.8V.

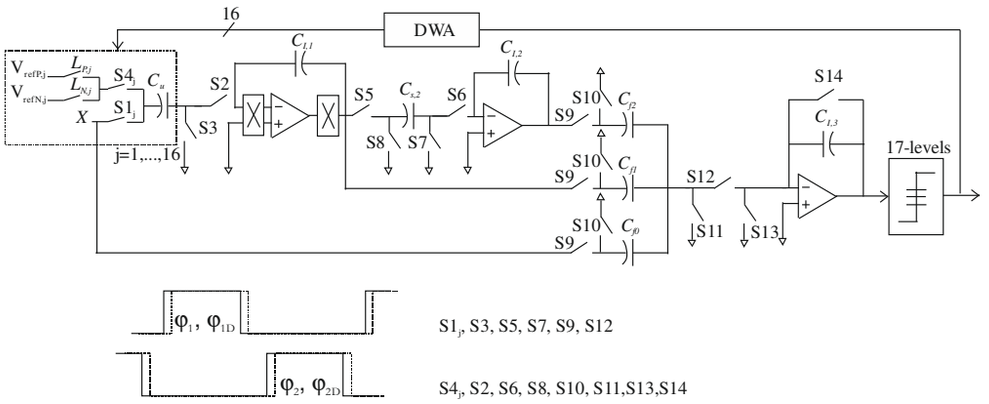


Fig. 28. SC implementation of the FF modulator

The first amplifier uses chopping to attenuate the influence of its offset and low-frequency noise [72]. The first integrator sampling capacitors $C_{s,1}$ are dimensioned as in Table V and they consist of 16 unit capacitors, each C_u equal to 0.13pF. Considering the matching property of the capacitors and the minimum size available in the CMOS 0.18μm process we used, the second sampling capacitor is set to 0.32pF. It is indeed composed by 9 minimum size elements resulting in $C_{s,2} = 9 \cdot 36\text{fF} \approx 0.32\text{pF}$. Together with $C_{I,2} = 5 \cdot 36\text{fF} \approx 0.18\text{pF}$, it implements the

loop-coefficient a_2=9/5. All the capacitor sizes are summarized in Table VI. The feed-forward signals are summed by an active adder and then fed to the 17-levels flash quantizer. The active addition needs one extra folded-cascode OTA. The timing of the modulator consists of two non-overlapping phases, φ_1 and φ_2, and two delayed versions of them, φ_{1D} and φ_{2D} (Fig. 28.), which are used to avoid signal-dependent charge injection. In order to overcome possible timing problems, the quantizer makes the conversion during φ_1, while the DWA rotates at φ_2, providing the feedback signals $L_{p,j}$, $L_{n,j}$. These signals are going to drive the feedback DAC at φ_{2D}.

TABLE VI
CAPACITOR SIZES OF THE ΔΣM

Sampling capacitors	Integrating capacitors	Feed-forward capacitors
$C_{s,1}$ = 2.08pF	$C_{I,1}$= 0.52pF	C_{f0} = 15*36fF
$C_{s,2}$ = 0.32pF	$C_{I,2}$ = 0.18pF	C_{f1} = 7*36fF
		C_{f2} = 2*36fF
		$C_{I,3}$=15*36fF

The reduced output voltage swings allow the use of a single-stage folded-cascode OTA. This topology has been selected for lower design complexity, in contrast with the result of the power optimization shown in Table V. This architecture choice is indeed sub-optimal with respect to current-mirror OTAs in terms of power consumption (see Fig. 15). The multi-bit quantizer consists of a 16-comparator flash ADC. ΔΣMs show little sensitivity to the static and dynamic errors induced during the internal quantization, as the position of the quantizer in the loop causes these errors to be shaped and attenuated in the signal band. For this reason, a dynamic architecture like the one in [73] is used for the comparator. The output codes of the multi-bit quantizer are five binary outputs, from B0 to B4, which are given as input

to the DWA. The DWA block outputs a thermometer code driving the unit elements of the feedback DAC.

Table VII draws a comparison between the values of power consumption and *FoM* obtained from Section 3.2.10 and for the simulated prototype. The power contributions are detailed for both cases.

TABLE VII
ΔΣM PERFORMANCE SUMMARY

		Theoretical Model	Transistor level implementation
***Signal BW* [Hz]**		10K	10K
***Target SNDR* [bits]**		14	14
N		2	2
B		4 (17 LEVELS)	4 (17 LEVELS)
OSR		64	64
$C_{s,1}$ [pF]		1.92	2
P_{TOT} [µW]		139	280
***ENOB* [bits]**		15.4*	15.5**
***FoM*[pJ/c.s.]**		0.16	0.3
P_{STAT} [µW]	*Current-mirror*	53	-
	Folded-cascode	90	166
P_{DYN} [µW]		48	48
$P_{FLASH\text{-}ADC\ QUANT}$ [µW]		29	36
P_{DWA} [µW]		9	13
Other contributions [µW]		-	17

* Based on the target resolution specified for the model. This value includes a 10dB design margin, as explained in Step a) of Section 3.2.
** Based on simulation results

The *FoM* is calculated as in (1). In the transistor-level implementation the static power is 3x times higher that the contribution predicted by our calculations. As aforementioned, folded-cascode OTAs are used in the actual design, which are not

the best choice for power-efficiency. Class-A current-mirror OTAs are instead assumed in the theoretical calculations of Table V. This topology is indeed the power-optimal one among the different circuit implementations of the OTA that we listed (see Fig. 15). Using folded-cascode OTAs for the integrators within the analytic model determines an increase of 1.7x in the estimation of the static power (see Table VII). The extra power consumption that is still present in the simulations is mostly due to the additional OTA in the active adder. This contribution, not included in the theoretical power estimation of Section 3.2.10, determines indeed an overhead of approximately 50μW in simulation. This OTA is indeed implemented as a folded-cascode architecture and the size of its equivalent load $C_{eq,ADDER}$ is not negligible. During φ_1, $C_{eq,ADDER}$ includes both the feed-forward capacitors C_{f0}, C_{f1} and C_{f2} (in Table VI) and the capacitors of the SC level shifter C_{LS} at the input of the flash quantizer (C_{LS}=0.1pF). According to (22), $C_{eq,ADDER}$≈1.1pF. The dynamic power consumption is the same in both model and simulation, since the capacitances have been dimensioned following the procedure described in Section 3.2.2. The expression for a multi-bit flash quantizer is used to calculate P_{QUANT} (see Table IV). As this calculation matches the actual implementation, the value of P_{QUANT} in simulation is close to the theoretical estimation. This result validates the power estimation of multi-bit flash quantizers. P_{DWA} is close to the theoretical model, as the model calculations again match the actual design. This power contribution is anyhow negligible in the overall power budget. We assumed in Section 3.2 that the requirement on the matching of the DAC unit elements is satisfied by using a first-order DWA algorithm. The power breakdown shows that we would even have room for a more complex DWA algorithm in the power budget. The clock generator circuit causes some additional power consumption which has not been included in the analytic model.

Fig. 29 shows the comparison between output spectra obtained by behavioural simulation in Simulink environment (solid line), and by transistor-level simulation in Cadence environment (curve marked with asterisks). *SNDR* and *ENOB* values in the inset result from the transient noise simulations of the ΔΣM, in which both the OTAs and the flash ADC are described at transistor-level. The good agreement between the curves simulated at behavioural level and the curves simulated at transistor-level confirms the validity of the design of the modulator.

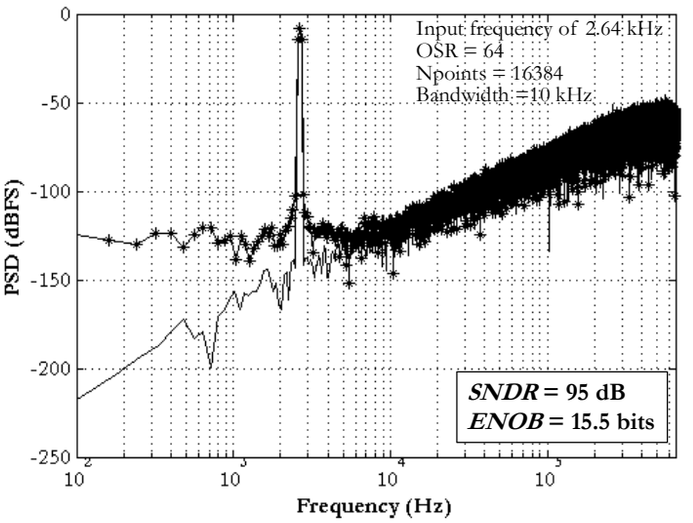


Fig. 29. Output spectra obtained by transistor-level simulation in Cadence environment (curve with asterisk marks) and by behavioural simulation in Simulink environment (solid line)

3.4.2 A 1.8-V 88dB DR ΔΣM for digital hearing aids using a novel summing SAR quantizer

In traditional multi-bit FF ΔΣMs the main power overhead with respect to the model is given by the flash quantizer and by the active adder. This is well known in

literature [70] and clear from the power breakdown shown in Table VII. The summing SAR quantizer of Section 3.3.3 is a good candidate to solve this issue as it combines the passive addition of input signal and state variable signals at the quantizer input with multi-bit quantization.

To validate this low-power circuit solution, a second order FF ΔΣM with a 16-levels summing SAR quantizer has been implemented in 0.18µm CMOS technology from a 1.8-V supply voltage. For the sake of simplicity, a single-ended representation of the proposed **ΔΣM** is shown in Fig. 30.

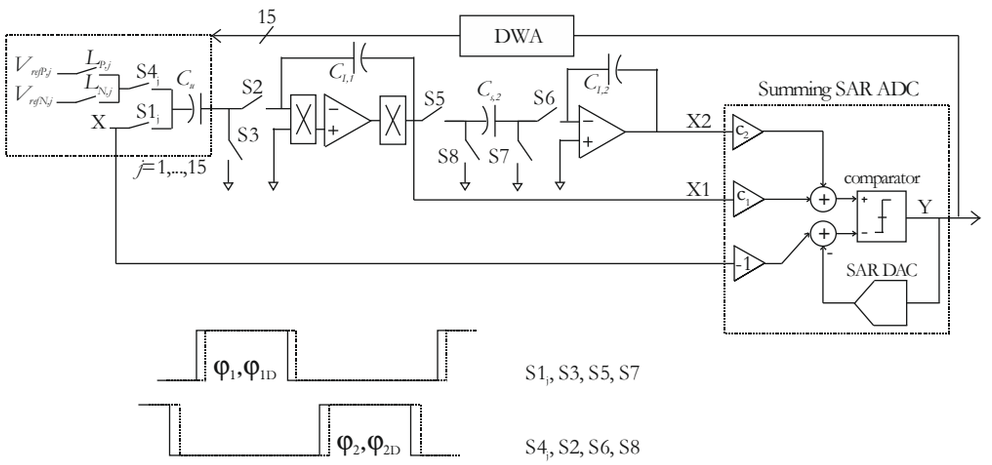


Fig. 30. SC implementation of the **ΔΣM**

The sampling capacitors $C_{s,1}$ of the first integrator are dimensioned as in Table V and consist of 15 unit capacitors C_u=0.142pF. The second sampling capacitor $C_{s,2}$ is set again to 0.32pF. The integrating capacitances are sized according to the loop coefficients a_i. All the capacitor sizes are summarized in Table VIII.

TABLE VIII
CAPACITOR SIZES OF THE ΔΣM

Sampling capacitors	Integrating capacitors	Feed-forward capacitors
$C_{s,1}$ = 2.13pF	$C_{I,1}$= 0.53pF	C_{f0} = 6*36fF
$C_{s,2}$ = 0.32pF	$C_{I,2}$ = 0.32pF*5/9	C_{f1} = 7*36fF
		C_{f2} = 2*36fF

The operation of the modulator is controlled by two non-overlapping clock signals and two delayed versions of them, used to avoid signal-dependent charge injection. The OTAs of the integrator stages have been implemented with fully-differential folded-cascode OTAs in analogy with the previous design (Section 3.4.1). The first OTA uses chopping to attenuate the influence of its offset and low-frequency noise.

Fig. 31 shows in a single-ended representation the architecture of the passive addition and SAR quantization block. ΔΣMs show little sensitivity to the errors introduced by the internal quantization, since the position of the quantizer in the loop causes these errors to be shaped and attenuated in the signal band. This allows using a dynamic comparator [73] in the SAR ADC.

The SC SAR DAC, shown in Fig. 31, includes a split capacitor array. The coupling capacitor has a unit-value capacitance *C,* while the two capacitor arrays are binary weighted. The SC DAC is controlled by the same non-overlapping clock, φ_2, used to control the integrators, and by the signals (BC, CLK) which are generated by the asynchronous SAR logic. The timing diagram is shown in the inset of Fig. 31. During the purging phase (φ_2 high) all the capacitors are discharged. During the sampling phase φ_1, the SAR conversion is performed: as explained in Section 3.3.3, throughout the sampling phase (SMPL high), the capacitors are driven by the analogue input voltage (-X), while during the bit-cycling phase (BC high), the SAR

algorithm is performed. Thanks to the asynchronous implementation of the SAR logic, the ADC does not require any additional high-frequency clock.

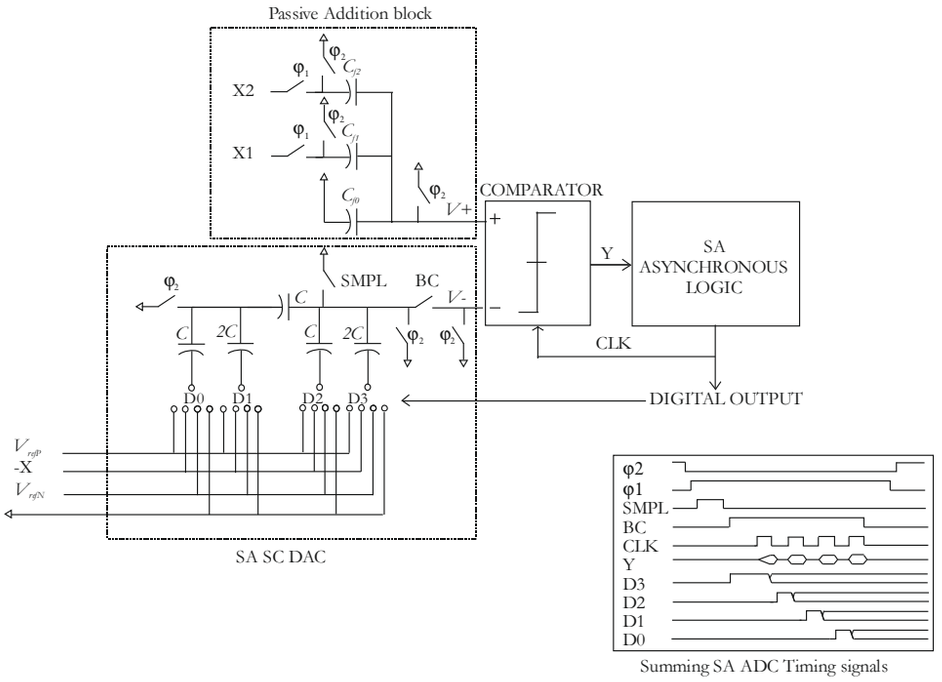


Fig. 31. Single-ended implementation of the Summing SAR ADC and timing diagram (inset).

A prototype of the proposed modulator has been fabricated in a 0.18μm general purpose CMOS process. Fig. 32 shows the die microphotograph. The total area is 1.3 x 1.1 μm^2; the active area of the modulator is 0.65 x 0.75 μm^2.

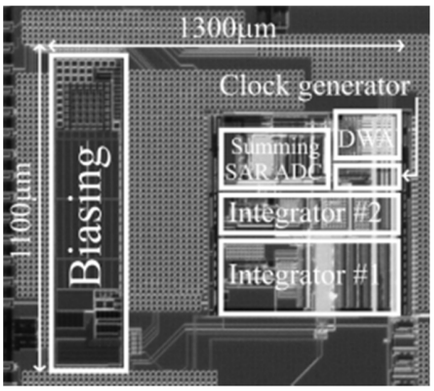


Fig. 32. Microphotograph of the implemented ΔΣM

Fig. 33 shows the measured *SNR* and *SNDR* versus the input amplitude relative to full-scale. A peak *SNR* of 84.4 dB and a peak *SNDR* of 84 dB are achieved at –3.2 dBFS input. The modulator achieves 88 dB dynamic range. Fig. 34 shows the output spectrum obtained from a 16 K-point FFT for the same input. The odd-order harmonics present in the spectrum are mostly related to the insufficient gain of the comparator in the SAR ADC, which does not include a pre-amplifier. This design problem is not fundamental and has been solved in the reconfigurable ΔΣ implementation of Section 4.4. The even-order harmonics are related to the generation of the time signals in the clock generator.

The total measured power consumption of the modulator is 155µW. The modulator achieves a *FoM* based on the *SNDR* of 570fJ/conversion step. The *FoM* is calculated according to (1).

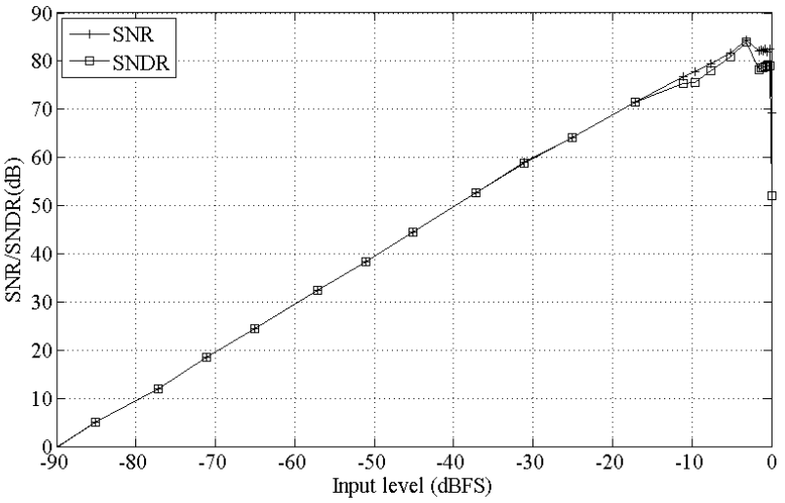


Fig. 33. Measured *SNR*/*SNDR* characteristic versus input amplitude

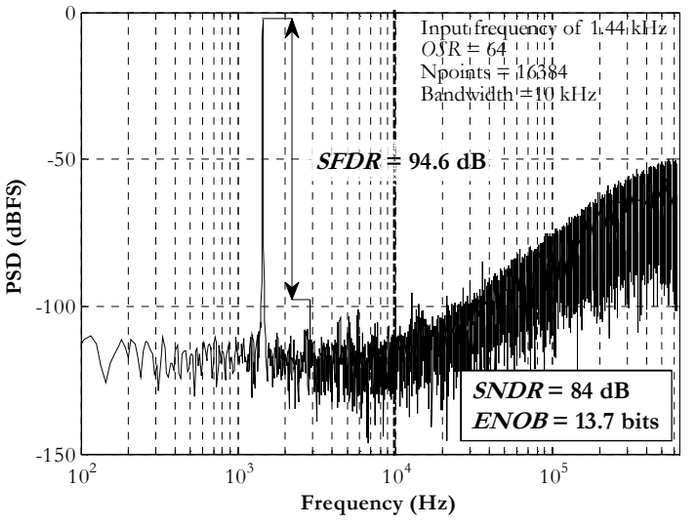


Fig. 34. Measured output spectrum for -3.2-dBFS input level

Table IX shows the comparison between the power breakdown of this circuit and the theoretical results of Section 3.2.11.

TABLE IX
ΔΣM PERFORMANCE SUMMARY

	Theoretical Model		Transistor level implementation	
***Signal BW* [Hz]**	10K		10K	
***Target SNDR* [bits]**	14		14	
N	2		2	
B	4 (17 LEVELS)		4 (16 LEVELS)	
OSR	64		64	
$C_{s,1}$ **[pF]**	1.92		2	
P_{TOT} **[µW]**	124		155	
***ENOB* [bits]**	15.4*		SIMULATION	15.4
			MEASUREMENTS	13.7**
***FoM* [pJ/c.s.]**	0.13		SIMULATION	0.18
			MEASUREMENTS	0.57
P_{STAT} **[µW]**	***Current-mirror***	53	-	
	(*Folded-cascode*)	90	85	
P_{DYN} **[µW]**	48		48	
$P_{SA\text{-}ADC\ QUANT}$ **[µW]**	14		7	
P_{DWA} **[µW]**	9		10	
Other contributions [µW]	-		5	

* based on the target resolution specified for the model. This value includes a 10dB design margin, as explained in Step a) of Section 3.2.
** based on measurements results

The measured static power is halved with respect to the one reported in Table VII. No additional OTA is indeed needed in the summing SAR quantizer and significant power saving is provided. Now the measured P_{STAT} matches the value provided by the model for a folded-cascode implementation of the OTAs. Of course the measured value is still high compared to the contribution predicted for the power-optimal class-A current-mirror topology (see Table V). The dynamic power consumption is the same in both cases since the capacitances have been

dimensioned following the procedure described in Section 3.2.2. The quantization power in the real implementation is lower than in the theoretical estimation of Table V. This difference is mostly due to the dynamic power for switching the internal SAR DAC. The model uses (41) as it considers a binary weighted capacitor array, while the SAR DAC implemented at transistor level follows (42) as it is a segmented architecture with a central coupling capacitor. P_{DWA} is close to the theoretical model, while the clock generator circuit determines additional power consumption not considered in our calculations. The total power consumption is close to the theoretical minimum provided by the model and is much lower than the one reported for the previous design. The comparison validates the power estimation procedure also for the case of a multi-bit SAR quantizer and confirms the beneficial effect of the summing SAR ADC on power-efficiency. This power improvement is unfortunately not completely reflected in the *FoM* values in Table IX. As aforementioned, the insufficient gain of the comparator in the SAR ADC generates odd-order harmonic distortion (see Fig. 34). This effect strongly affects the final resolution and reduces the measured *ENOB* 1.7 bits below the simulated value (15.4 bits). This resolution loss severely affects the value of *FoM* for this design. The design problem of the comparator will be solved in the implementation of the reconfigurable ΔΣM of Section 4.4.

Table X shows a comparison of this implementation with current state-of-the-art ΔΣMs including a multi-bit SAR quantizer ([59]-[60], [73]-[75]). The beneficial effect of the novel summing SAR ADC on power-efficiency is reflected in the *FoM* values in Table X, where the *FoM* simulated for our work compares favourably to other designs. Only ΔΣMs presented in [59] and [75] achieve better performance than this work, thanks to the lower supply voltage and to the use of more power-efficient OTAs, respectively.

TABLE X

ΔΣM PERFORMANCE COMPARISON

	[83]	[84]	[68]	[69]	[81]	This work
CMOS Process (nm)	500	130	65	180	40	180
Supply voltage (V)	1.5	1.2	0.6	3.3	1.2	1.8
***BW* (Hz)**	50k	1.92M	24k	24k	1.92M	10k
***DR* (dB)**	-	-	91.9	88	83.4	88
***SNR* (dB)**	58	65	-	-	80	84.4
***SNDR* (dB)**	56	59	90.2	120	79.6	94.5 (sim.) 84 (meas.)
Area (mm²)	0.6	0.36	0.41	0.49	0.051	0.49
***P*$_{TOT}$ (μW)**	120	3100	133	20000	1.91	155
***FOM* (fJ/conv.)**	2347	788	100	509	64	183 (sim.) 570 (meas.)

3.5 Conclusion

In this chapter a method for the design of power-efficient SC ΔΣMs was presented. To find the power optimal solution among single-loop topologies, feedback and feed-forward, we firstly identify all the combinations of (*N*, *B*, *OSR*) able to achieve the target resolution within the given bandwidth. For each of these combinations, we use an analytic model to calculate the resulting power consumption. Based on the power comparison of the combinations of (*N*,*B*, *OSR*) in the solution space, we select the architecture that can fulfil the specifications with the best power-efficiency.

The design methodology was applied to a high-resolution ΔΣ modulator for hearing-aids application. Using the power-optimization procedure, a second-order multi-bit feed-forward topology was chosen as power-optimal.

Once the architecture was selected, circuit techniques for the low-power implementation of feed-forward modulators were also discussed. More specifically, a summing SAR quantizer was presented which combines multi-bit SAR quantization with the analogue passive addition.

Finally, the methodology for the power optimization of ΔΣMs and the summing SAR quantizer block were verified with two design examples.

4 Power-efficient design of reconfigurable SC ΔΣMs

This chapter presents a methodology to design reconfigurable switched-capacitor ΔΣ modulators that are able to keep the power-efficiency constant and optimal for a set of different resolutions and bandwidths. The method is based on the structured design method for point-solution power-optimal ΔΣ modulators presented in Chapter 3. As the size of the sampling capacitors is crucial to determine power consumption, three approaches to achieve reconfigurability are compared: dimension the sampling capacitors to achieve the highest resolution and keep them constant; change only the first sampling capacitor according to the targeted resolution; or program all sampling capacitors to the required resolution. The second approach results in the best compromise between power-efficiency and low design complexity. A reconfigurable ΔΣM for biomedical applications is fabricated in a 0.18μm CMOS process to validate the proposed methodology. Parts of this chapter have been published in [74] and [75].

4.1 Introduction

As already discussed in Section 1.2, low bandwidth (up to a few tens of kHz) high resolution (>12 bits) Analogue-to-Digital Converters are more and more needed in the biomedical field. These ADCs should have excellent power-efficiency and adapt their resolution and speed to the characteristics of the different possible input signals because of the limited power budget available in autonomous sensor nodes [76]. Biopotential signals have a spectrum between a few hundreds of Hertz and a few kilohertz, with an amplitude range between a few tens of μV and a few mV. In a system able to cope with many biopotential signals, which uses only one ADC to minimize silicon area, power is therefore optimized using a reconfigurable converter (see Section 1.1). ΔΣMs are good candidates for reconfigurability because of their inherent bandwidth resolution trade-off. Reducing the sample rate lowers indeed P_{TOT}, while decreasing the resulting *ENOB* [27].

In this chapter we present a method for the design of power-optimal switched-capacitor reconfigurable ΔΣMs. The most power efficient ΔΣ architecture is identified for each mode of operation among single-loop topologies that fulfil the specifications with different *N, OSR* and *B,* using the analytic model for the power consumption presented in Section 3.2.4. Finally, the best common architecture as regards *N, OSR* and *B* is chosen, assuming capacitors can still be reconfigured. In Section 4.2, three different strategies to achieve reconfigurable ΔΣMs are identified and compared in terms of power-efficiency using the proposed design methodology: the sampling capacitors C_s of all stages sized as in the maximum resolution mode (*fixed*-$C_{s,i}$ approach); programmable C_s in all integration stages (*variable*-$C_{s,i}$ approach); and only first-stage capacitor $C_{s,1}$ programmable according to the target *ENOB* while the C_s in the other stages sized as in the highest resolution mode (*variable*-$C_{s,1}$

approach). Based on the result of their power comparison, the *variable-$C_{s,1}$* approach is identified as the best compromise between power-efficiency and low design complexity. Section 4.3 focuses on the design techniques for reconfigurability. The implementation of tunable sampling capacitors is described together with a novel power-reconfigurable and speed-scalable OTA. In Section 4.4, the transistor-level implementation of a reconfigurable ΔΣM for biomedical applications is addressed. The measurements performed on this chip validate the proposed design approach to reconfigurability. Some conclusions are drawn in Section 4.5.

4.2 Power efficient approach to reconfigurability

To find the power optimal solution for a given resolution and bandwidth, a structured design approach has been proposed in Section 3.2. The methodology is applied to the power optimization of SC single-loop ΔΣMs as motivated in Section 2.4. In this Section, the methodology is extended to address the design of power-efficient reconfigurable SC ΔΣMs.

As shown in Section 3.2.3, adapting $C_{s,1}$ to the targeted resolution according to (13) or (17) is crucial in determining the ΔΣM power consumption. For this reason three approaches to reconfigurability are possible: a *fixed-$C_{s,i}$* approach, a *variable-$C_{s,1}$* approach and a *variable-$C_{s,i}$* approach. In the *fixed-$C_{s,i}$* approach, the sampling capacitors in all working modes are the same as the ones calculated for the highest resolution mode. This strategy allows a simple and area-efficient design that does not require the use of switchable passives. However, as demonstrated by the reconfigurable implementation in [27], it leads to poor power optimization. In this design, the resolution of the ADC is modified by changing the *OSR* but the sampling capacitors are not adapted to the thermal noise requirements of each ADC

mode according to (13). Consequently, the static and dynamic powers grow linearly with the sampling rate, as described by (46). As these contributions are dominant in the overall power budget, the resulting *FoM* varies more than 5x between the minimum- and the maximum-resolution modes that we will address in this work. This approach is thus mostly avoided in state-of-the-art literature and will not be considered in the rest of this chapter.

In the *variable-*$C_{s,1}$ strategy only the size of the first-integrator capacitor $C_{s,1}$ is adapted to the targeted resolution of each working mode, while the capacitors of the following integrators are kept equal to those used in the highest resolution mode. This approach is interesting as the size of the sampling capacitors $C_{s,i}$ is crucial in determining the power consumption of the complete ΔΣM, while, on the other hand, the power dissipation due to the capacitors of the following integrators is normally negligible.

The *variable-*$C_{s,i}$ approach consists in programming the sampling capacitors of all the integrators according to the required resolution, deriving a specific size for each capacitor in each ΔΣM working mode.

These strategies for reconfigurability are compared in Section 4.2.2 in terms of power-efficiency following the structured design outlined in Section 4.2.1.

4.2.1 Overview of the methodology

The design methodology proposed in this work for the power optimization of reconfigurable ΔΣMs is summarized by the flow diagram in Fig. 35.

As starting point of the design methodology, we consider the highest resolution mode of the reconfigurable ΔΣ modulator, defined by its SNDR and signal-BW specification. The point-solution design methodology of Section 3.2 is applied to this mode through the following steps:

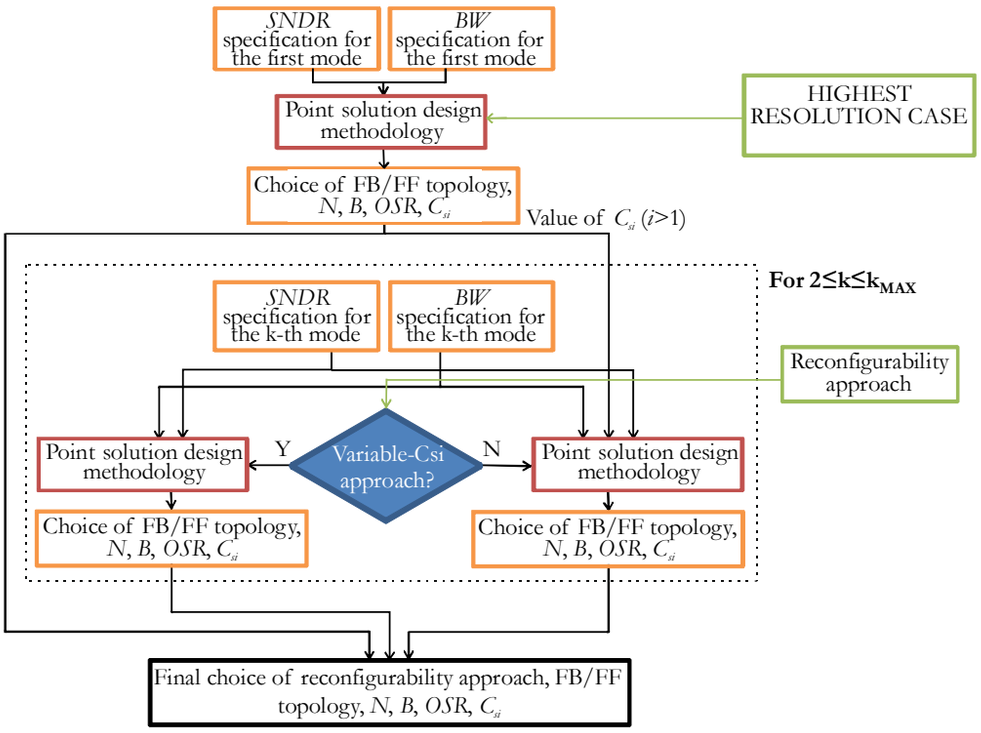


Fig. 35. Flow diagram of the proposed method for power-optimal reconfigurable ΔΣ designs

a) The combinations of (*N*, *B*, *OSR*) able to achieve the target *SNDR* within the signal *BW* are identified.

b) The minimum values for the sampling capacitors $C_{s,i}$ that satisfy both thermal noise and linearity requirements are calculated. This is done for all the (*N*, *B*, *OSR*) in the solution space selected in Step a) (see Section 3.2.2).

c) P_{TOT} is estimated for all the combinations in the solution space found in Step a) using the values of $C_{s,i}$ found in Step b). The power is calculated using the analytic model presented in Section 3.2.4. The power-optimal architecture, defined in terms of single-loop topology (feedback or feed-forward) and combination of (*N*, *B*, *OSR*)

granting the lowest power solution is then annotated as the solution to be used for this mode.

We proceed then with the lower-resolution operation modes of the reconfigurable ΔΣM. More specifically, for each lower resolution mode of the reconfigurable ΔΣM, and for each reconfigurability approach (both left and right in the figure):

d) We identify the combinations (*N*, *B*, *OSR*) that are able to fulfil the new set of requirements (*SNDR*, *BW*) following Step a).

e) We calculate the sampling capacitors $C_{s,i}$ in a similar way to what was done in Step b), but now following different strategies for the two reconfigurability modes: the *variable-*$C_{s,1}$ and the *variable-*$C_{s,i}$ approaches. In the *variable-*$C_{s,1}$ approach, $C_{s,1}$ is sized based on the new target resolution, while the capacitors of the following integrators are kept equal to those found for the highest resolution mode. In the *variable-*$C_{s,i}$ approach, the sampling capacitors of all the integrators are calculated again according to the required *ENOB*.

f) Finally, we apply Step c) for both the *variable-*$C_{s,1}$ and *variable-*$C_{s,i}$ approach and select the most power-efficient combination of (*N*, *B*, *OSR*) for each mode.

Based on the results of Step c) and f), we determine the power-optimal design of the reconfigurable ΔΣM.

4.2.2 Case study: design of a reconfigurable ΔΣM for a biomedical application set

To prove the effectiveness of the proposed methodology, the power-optimization procedure has been applied to the design of a reconfigurable ΔΣM, scalable in resolution and bandwidth, for a given set of biomedical applications: the

ΔΣM is suitable for biopotentials (EEG, ECG, EMG) and audio signals, and works in the operation modes described in Table XI (see also Table I, Section 1.1).

TABLE XI
SPECIFICATIONS FOR RECONFIGURABILITY

	ENOB	*BW* [Hz]	Target application
High resolution/ low *BW* (HRLB)	16	256	EEG, ECG
Medium resolution and *BW* (MRMB)	14	2048	EMG
Low resolution/ high *BW* (LRHB)	12	16 k	Hearing-aids

Considering the working modes of Table XI, it is clear that a constant *FoM* cannot be achieved simply: going from the medium to the high resolution mode, the *ENOB* increases by 2 bits (factor 4) while the bandwidth decreases by a factor 10. Therefore, for a constant *FoM*, the total power P_{TOT} has to decrease at least 2.5 times.

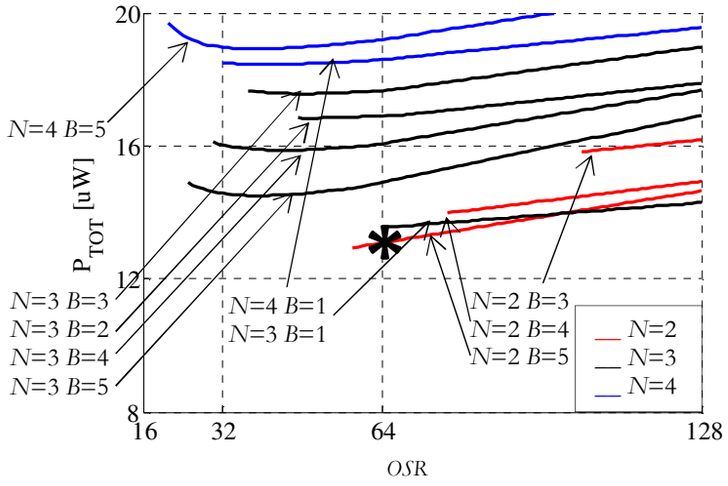
According to general methodology of Section 4.2.1, Step a) is applied to find all values of (*N*, *B*, *OSR*) which satisfy the specifications of the HRLB mode (*ENOB*=16, *BW*=256 Hz). The order of the loop filter is limited to 4, as precluding instabilities in higher order single-loop ΔΣMs mostly leads to significant degradations of *SNR* with respect to ideal [4]. The resolution of the internal quantizer is limited to 5 bits, so that a first-order DWA is sufficient to alleviate the problem of non-linearity in the transfer characteristic due to device mismatch. The *OSR* is swept between 16 and 128. This range is chosen following the criteria in Section 3.2.2. First-order architectures are not considered as they do not reach the targeted resolution for this *OSR* range. When choosing the actual *OSR* values for implementation, only powers of 2 are considered, to simplify the design of the decimation filter.

Step b) is used then to define the corresponding values of the sampling capacitors $C_{s,i}$. A supply voltage of 1V is chosen and the reference voltage V_{ref} is assumed to coincide with V_{DD} in both FB and FF topologies. The values of the in-

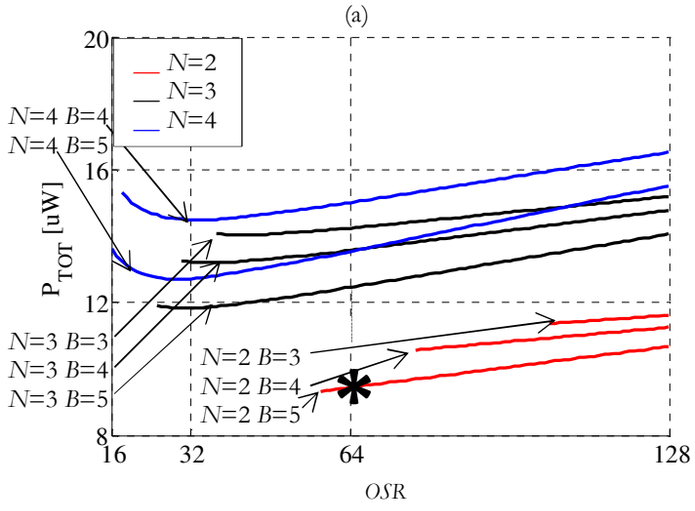
loop coefficients are selected here, using the tool in [50], as a_1=3, a_2=9/5, c_1=6/15, c_2=3/15. They are adjusted so that the integrators output range is 30% of the integrators reference voltage. Choosing the percentage value of the integrators' output swing is controversial. On the one hand, a low percentage relaxes the OTAs requirements in terms of output swing and slewing [47] but leads to larger values of capacitors in the integrating stages. On the other hand, a high percentage minimizes the size of the capacitors but makes the design of the OTAs more complex and power-hungry. In this design case, the impact of this choice on the overall power consumption has been extensively studied by using our analytical model of ΔΣMs power consumption. The percentage value of 30% has been chosen as the best compromise between the two trends mentioned. Considering the matching properties of capacitors in a 0.18μm CMOS technology, the minimum size for the sampling capacitors in the integrators following the first $C_{s,i}$ (i>1) is set to 50fF. K_σ, C_A and C_{inv} have been estimated from [63] for the given technologies as K_σ ≈2.5% μm and C_A≈2 fF/μm^2.

According to Step c) the power dissipation is calculated using the analytic power model for each ΔΣ architecture satisfying the HRLB specs. A SAR ADC has been chosen to calculate P_{QUANT}, as a SAR approach has been demonstrated to enable power-efficient multi-bit quantization. The switching energy of a minimum size inverter is estimated from [63] to 5fJ, corresponding to a capacitance C_{inv} of 10fF per logic node.

The results are presented for FB and FF implementations in Fig. 36. (a) and (b), respectively. The power consumption is shown as a function of *OSR* and for different values of (*N, B*). Missing or incomplete curves reflect combinations of (*N, B, OSR*) with insufficient resolution.



(a)



(b)

Fig. 36. Total Power estimation for HRLB mode (*ENOB*=16, *BW*=256 Hz) as a function of *OSR* in FB (a) and in FF (b) implementations

In both feedback and feed-forward topologies, the power-efficiency is higher for low-order ΔΣM and the minimum power consumption (marked with an asterisk) is obtained with a second order modulator. P_{STAT} and P_{DYN} values are indeed minimized for a small number of integrators.

The power consumption decreases with increasing B as the use of a more bits in the quantizer in the ΔΣ modulator both reduces the quantization noise and improves the stability of the loop: with increasing B the allowed OL levels become larger and, according to (13), this reduces the size of the minimum $C_{s,1}$ as well as the power. The only exception to this general trend is for single-bit FB topologies, for which class-AB OTAs are more power efficient. Moreover, a one-bit input DAC does not introduce distortion components into the ΔΣ loop, which relieves the stability problem. The best power optimization is achieved for values of N=2, B=5 and OSR=64 in both FB and FF topologies. In general, FF topologies exhibit lower power consumption.

For the other modes of operation, we will follow either the *variable-*$C_{s,1}$ or the *variable-*$C_{s,i}$ approach. The former will be investigated first.

The *variable-*$C_{s,1}$ strategy allows reconfiguring the ΔΣM in a relatively simple way. It requires only 4 switchable capacitor arrays in a fully differential SC architecture. After applying Steps d), e) and f) for this approach, the achieved values of P_{TOT} for the MRMB and the LRHB modes are shown in Fig. 37 for FF topologies. FF topologies result indeed in a lower power solution than FB topologies also in these modes. Therefore, only FF ΔΣMs are showed here.

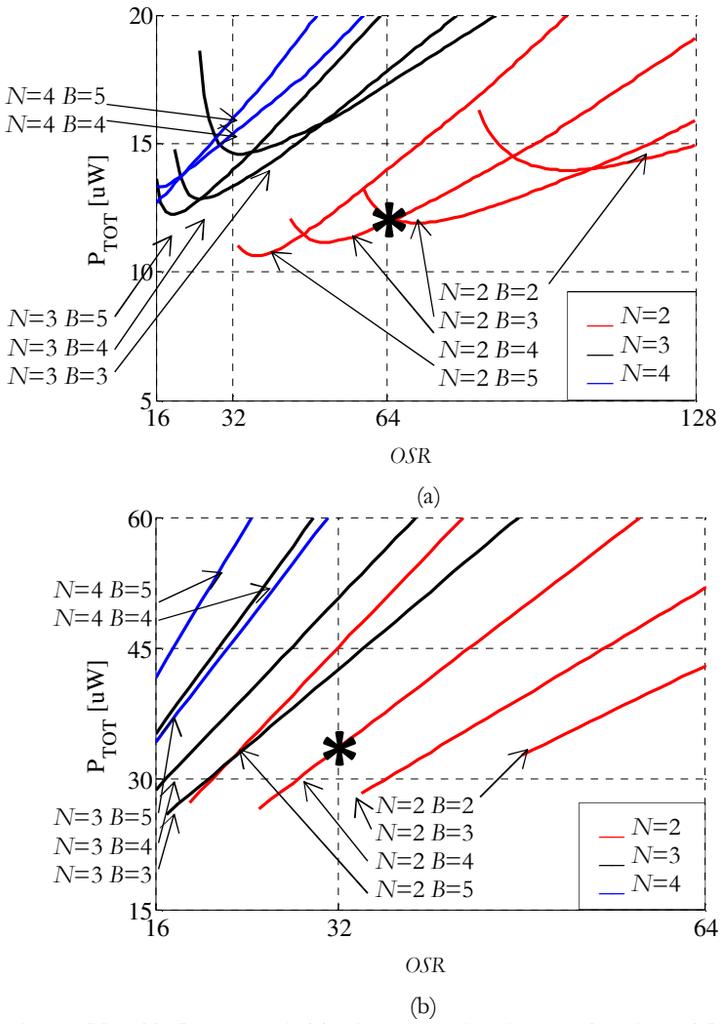


Fig. 37. *Variable-$C_{s,1}$* approach: Total Power estimation as a function of *OSR* using FF implementations for (a) MRMB mode (*ENOB*=14, *BW*=2 kHz) and (b) LRHB mode (*ENOB*=12, *BW*=16 kHz)

As in the HRLB mode, low-order topologies are more power efficient than those with higher order. In low resolution modes it turns out that the minimum value of $C_{s,1}$ is limited by matching requirements. Also in the MRMB and LRHB modes the best power-efficiency is achieved with multi-bit configurations, and the power-

optimal choice is N=2, B=4 in both MRMB and LRHB cases. As a result of the selection in Step f), the best values of power consumptions and *FoMs* are reported in Table XII for FF implementations. These values are calculated according to (1).

TABLE XII
POWER OPTIMAL SOLUTIONS FOR VARIABLE- $C_{S,1}$ APPROACH

	HRLB	MRMB	LRHB
N	2	2	2
B	5	4	4
OSR	64	64	32
$C_{s,1}$ **[pF]**	28	2	0.2
P_{TOT} **[µW]**	9.5	12	34
***FoM* [pJ/c.s.]**	0.2	0.13	0.18

Varying the first-integrator sampling capacitors according to the required resolution keeps *FoM* values almost constant among the three different ΔΣM operation modes. The *FoM* is comparable in HRLB and LRHB modes (around 0.2 pJ/c.s.) while it is slightly lower in MRMB mode (0.13 pJ/c.s.). In MRMB mode, neither high-resolution (which demands large sampling capacitors) nor high-*BW* (which requires a high-frequency sampling rate) is required, making it simpler to decrease both the static and the dynamic power of the ΔΣM.

The *variable-*$C_{s,1}$ approach to reconfigurability applied to the operation modes of Table XI requires changing the quantizer resolution between HRLB mode on the one hand, and MRMB, LRHB cases on the other hand (Table XII). This solution results in a rather complex circuit implementation. A further simplification will follow, later.

We can now apply Steps d), e) and f) to the *variable-*$C_{s,1}$ approach for comparison. The dependency of the total power consumption on the design parameters N, B and *OSR* obtained with this approach is similar to the one shown in Fig. 37. Also in this case FF topologies show to be more power efficient than FB ΔΣMs. P_{TOT} is generally minimized for low N and low *OSR* while power becomes optimum for

high resolution quantizers. The power-optimal values of P_{TOT} and *FoM* using the variable $C_{s,i}$ approach are annotated in Table XIII for FF implementations according to the results of Step f).

TABLE XIII
POWER OPTIMAL SOLUTIONS FOR VARIABLE- $C_{S,i}$ APPROACH

	HRLB	MRMB	LRHB
N	2	2	2
B	5	4	4
OSR	64	64	32
$C_{s,1}$ **[pF]**	28	2	0.2
P_{TOT} **[μW]**	9.5	11	33
***FoM* [pJ/c.s.]**	0.2	0.12	0.17

The results for the *variable-*$C_{s,i}$ approach are very similar to the ones obtained using the *variable-*$C_{s,1}$ strategy for the operation modes of Table XI, because in MRMB and LRHB modes the sampling capacitors of the integrators are limited by matching, as in the higher resolution HRLB mode.

Based on the comparison between Table XII and Table XIII, the *variable-*$C_{s,1}$ approach is the best compromise between power-efficiency and low design complexity in this case study. Indeed:

- Sizing all sampling capacitors according to the targeted resolution generates optimal power values which are only slightly lower than those obtained with the *variable-*$C_{s,1}$ approach. The difference is just 1 μW in both MRMB and LRHB modes. As mentioned above, the $C_{s,i}$ in all the integrators except the first one should ideally scale according to (18). However, the minimum size for $C_{s,i}$ is assumed in this work to be 50fF to avoid that capacitor mismatch affects the ΔΣM performance. The values of $C_{s,i}$ in the *variable-*$C_{s,i}$ approach are thus limited by matching to values close to the ones obtained under the *variable-*$C_{s,1}$ strategy, and the *variable-*$C_{s,i}$ approach allows only minimal power benefits in our case study.

• Even though the minimum power for HRLB mode is given by the FF combination (N=2, B=5, OSR=64), Fig. 36. (b) shows that a power efficient scalable ΔΣM can be obtained also by choosing (N=2, B=4, OSR=128). For this choice, the values of the first sampling capacitor, the total power and the *FoM* in HRLB mode become $C_{s,1}$=16 pF, P_{TOT}=11 μW, and *FoM*=0.23 pJ/c.s., respectively. This choice brings just a small power penalty with respect to the optimal solution. It is thus possible to avoid changing the resolution of the quantizer between the different modes paying a minor power penalty. This further simplifies the implementation of the *variable-*$C_{s,1}$ approach as power-efficiency can be guaranteed just by changing the *OSR* and the size of the first-integrator sampling capacitances for the different modes.

• More in general, implementing the *variable-*$C_{s,i}$ approach would require additional circuit complexity. 4N capacitor arrays that are suitably switched for each ADC mode would be necessary. Indeed, in *variable-*$C_{s,i}$ approach 2 sampling capacitors and 2 integrating capacitors arrays must be used in each integrator.

The final architectural choices and expected performances are listed in Table XIV for the three operational modes mentioned above.

TABLE XIV
POWER-OPTIMAL RECONFIGURABLE ΔΣM DESIGN SUMMARY

	HRLB	MRMB	LRHB
N	2	2	2
B	4	4	4
OSR	128	64	32
$C_{s,1}$ **[pF]**	16	2	0.2
P_{TOT} **[μW]**	11	12	34
FoM **[pJ/c.s.]**	0.23	0.12	0.18

4.3 Circuit design techniques for power-efficient reconfigurable ΔΣMs

As concluded from the previous section, the *variable-*$C_{s,1}$ approach offers the best compromise between power-efficiency and low design complexity as it optimizes the power vs. resolution trade-off while requiring only the first-integrator to be programmable. The size of the sampling capacitor in the first integrator and the *GBW* of the corresponding amplifier need to be adjusted for the different modes of operation. Suitable circuit techniques must be exploited to achieve this reconfigurability. First, the first-integrator sampling capacitor $C_{s,1}$ needs to be programmable. When implementing this, the parasitic capacitance determined by the configuration switches and the non-linearity of their ON-resistance must be taken into account and minimized. Second, the OTAs must adapt their power to the required *GBW* and to the capacitive load in each mode of operation, while ensuring closed-loop stability. Sections 4.3.1 and 4.3.2 will discuss in detail the circuit-level implementation of these blocks.

4.3.1 Modular $C_{s,1}$ implementation

As mentioned in Section 3.2.2, the sampling capacitor $C_{s,1}$ in multi-bit ΔΣ architectures is composed by 2^B-1 unit elements C_u as it coincides with a *B*-bit feedback DAC: $C_{s,1} = (2^B\text{-}1)\cdot C_u$. To allow the size of $C_{s,1}$ to scale according to the target resolution, C_u is thus programmed as shown in Fig. 38.

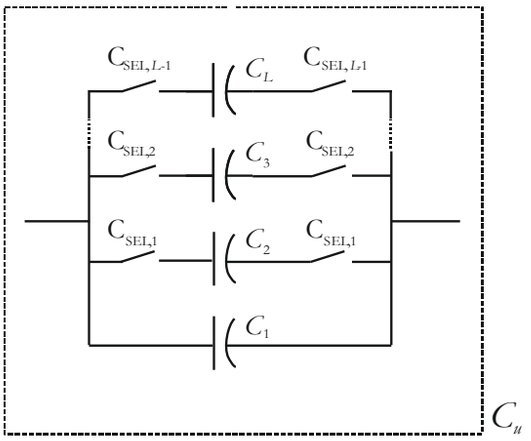


Fig. 38. SC implementation of the programmable first-integrator C_u

Being L the number of reconfigurability modes , C_u is implemented as an L-branch switchable array which is programmed according to the targeted *ENOB* via L-1 configuration bits, $C_{SEL,j}$ (j=1,…, L-1). The largest value of C_u (used in the highest resolution mode) is implemented by combining all the switchable units in parallel, while lower resolution modes reuse a subset of units, with no area overhead [77].

The shaping and the feedback of the ΔΣM do not help in reducing the DAC error as this error is injected directly at the input. It is therefore required to ensure a DAC linearity which is good enough for the requested *ENOB*. In our case, the linearity of the DAC is mainly limited by the matching of its unit elements and by the linearity of the switches. The DAC matching accuracy has already been taken into account in sizing the sampling capacitors and a suitable data weighted averaging algorithm has been applied for shaping the mismatch (see Section 3.2.2). The non-linearity of the switches is due to input voltage dependent ON-resistance (r_{ON}) .

The switch ON-resistance mainly depends on the overdrive voltage. Thus to obtain a constant r_{ON} from the switch, we need a constant overdrive voltage for

the switch transistors. In low-voltage designs, clock boosting circuits are typically exploited to solve this issue [78]. Unfortunately, the switches in the programmable sampling capacitors are static switches, and their configuration is fixed for a given mode. Therefore, using a clock boosting scheme is not as simple as for switches driven by a clock signal, as it would require the generation of additional idle phases. Other techniques are thus employed to overcome the transistor-driving problem. First of all, both n-type and p-type transistors are used to form a transmission gate and reduce the signal-dependent on-resistance of the switch. Secondly, the driving voltage of these switches is increased to 1.2-V, provided by a separate supply, $V_{DD,SW}$, higher than the analogue V_{DD} (as specified in Section 4.4, V_{DD} is 1V). The switches being static, negligible power consumption is drawn from $V_{DD,SW}$. However, extra cost is paid in terms of complexity of the overall system.

The transistors in the transmission gate are sized to minimize the drain/source capacitance, not the ON-resistance of the switches. The parasitic capacitance would indeed determine an extra load for the OTAs and a consequent increase of the static power. Reducing r_{ON} (to optimize the RC time constant of the switches) is instead not a priority for our design. On the one hand, these switches are static, so their speed is not a major concern. On the other hand, during the sampling, their r_{ON} is in series with the ON-resistance of the sampling switches (driven by φ1d and φ1, respectively). The sampling switches are implemented as minimum-size n-type transistors with clock boosting while, as mentioned above, the static switches are implemented as the parallel of minimum-size n-type and p-type transistors. Consequently, the overall resistance is dominated by the equivalent resistance of the sampling switches.

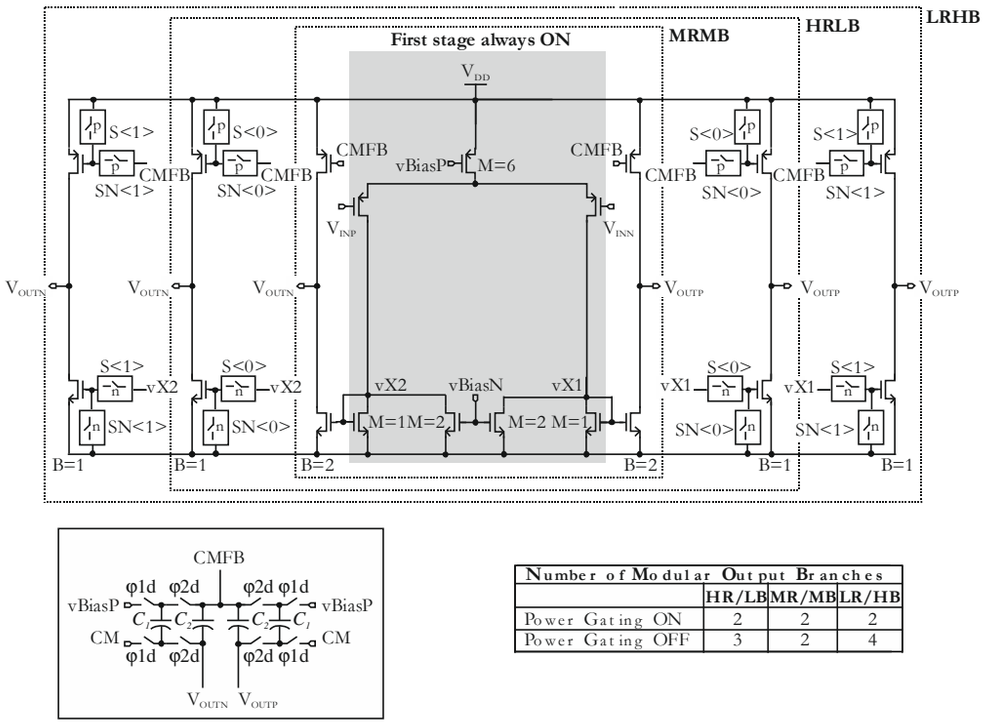
4.3.2 Programmable OTAs for power- and speed-scalability

In reconfigurable ΔΣMs power-efficiency can only be achieved by using a flexible OTA which adapts its static power consumption and *GBW* to the sampling speed and capacitive load required in each operation mode. The most common approach in literature consists of choosing a fixed circuit topology, with the input stage biased in weak inversion, and tuning the bias current to scale the *GBW* [17]. This approach, however, is not suitable for *GBW*s varying more than 10x, as required by our specifications. Another common approach is to use identical switchable amplifier cells in parallel [79].

In our architecture, we adopted a power-efficient gain-enhanced current mirror OTA [80] in which the input differential pair is biased with a fixed tail current which is always kept on. The principle is shown in Fig. 39, applied to the first-integrator OTA of the case study discussed in Section 4.2.2.

The current-mirror architecture has been chosen as this OTA offers high power-efficiency in terms of *GBW* per unit of capacitive load (see also Fig. 15). The simple gain enhancement technique presented in [80] is used to enhance the gain by about 10-20 dB without compromising the *GBW* and with no extra power consumption. Moreover, the current-mirror OTA is suitable for low-voltage design as its output stage is rail-to-rail. However, this OTA suffers from poor DC gain, employing just a single gain stage without cascoding. This drawback is not a problem in our ΔΣM as our FF architecture only needs about 40 dB DC gain.

The total OTA *GBW*, which is proportional to the number of the modular output branches, can be adjusted by switching on/off these branches. The output branches are sized considering the target *GBW* and the equivalent load specification C_{load} of each mode. The OTA of Fig. 39 is used in both the first and the second integrator of the ΔΣM. The OTA in the second integrator is designed adapting this



Number of Modular Output Branches			
	HR/LB	MR/MB	LR/HB
Power Gating ON	2	2	2
Power Gating OFF	3	2	4

Fig. 39. Programmable gain-enhanced current mirror OTA schematic

same approach to the specifications of C_{load} as will be discussed later on (and reported in Table XVI).

The main advantages of our solution compared to using identical switchable amplifier cells in parallel [80] is a reduced power and smaller area, since the first stage is shared among all the configurations. The trade-off between stability and *GBW* requires however careful design (the nodes associated to the second pole, vX1 and vX2, are loaded by the multiplexers S<0:1> and SN<0:1>).

Moreover, in order to further reduce the static power of the modulator, the first OTA is power-gated during the sampling phase φ_1. During the power-gating the switchable output stages of the first OTA are powered down, allowing a significant power saving. More details are provided in Section 4.4.

4.4 Design example: a 1-V 99-to-75 dB SNDR 256-to-16kHz reconfigurable ΔΣM

To validate the results obtained with the described analysis, a second order FF ΔΣM with a 16-level quantizer has been designed and fabricated in a standard 0.18μm CMOS process, using a 1 V supply. To meet the required *BW* and resolution, the sampling frequency is tuned between 65 kHz and 1.05 MHz, implementing *OSR*s between 128 and 32 (see Table XIV). Fig. 40 illustrates the fully differential SC implementation of the modulator.

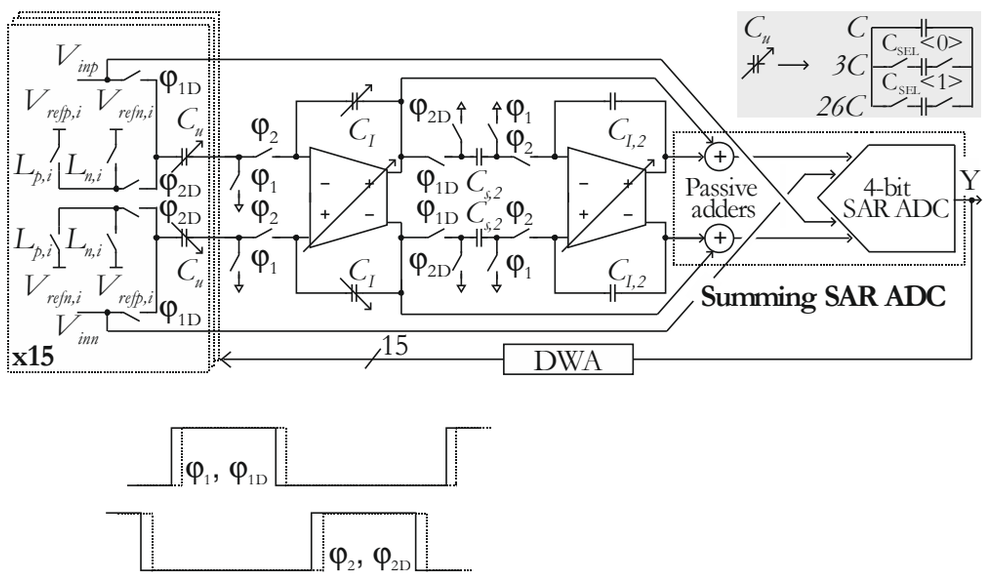


Fig. 40. SC implementation of the ΔΣM

As a result of the design choices in the Section 4.2.2, the size of the sampling capacitor of the first integrator, $C_{s,1,}$ is tuned according to the targeted *ENOB* to minimize the equivalent load of the first integrator. It is dimensioned from kT/C

noise requirements according to (13) and consists of 15 unit capacitors C_u. The circuit implementation of C_u, discussed in Section 4.3.1, is shown for this case in the inset of Fig. 40. C_u consists of 30 minimum size unit elements C (C=36fF) in HRLB mode, of 4 units in MRMB mode, and of one unit in LRHB mode. In LRHB mode $C_{s,1}$ had to be increased with respect to the minimum bound provided by the model due to constraints on the minimum unit capacitor in the process used. The minimum capacitor size available in the CMOS 0.18µm process we used is indeed 36 fF, resulting in $C_{s,1} = 15 \cdot 36\,fF \approx 0.5\,pF$, which is higher than the minimum value requested by the design methodology (see Table XIV).

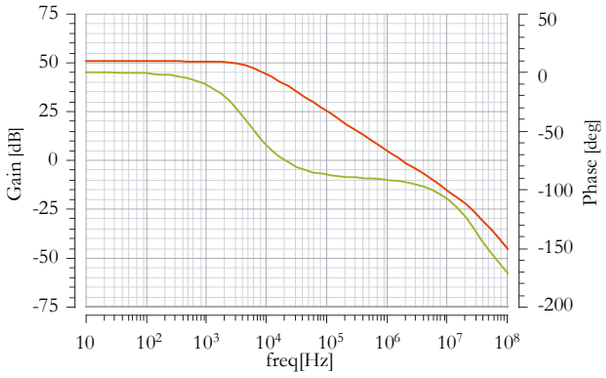
As aforementioned, the values of the loop coefficients in this design are adjusted to ensure that the output range of the integrators is 30% of the reference level. They have been selected to be a_1=4, a_2=9/5, c_1=6/15, c_2=3/15, using the method in [50]. Considering the matching properties of the capacitors and the minimum size available in the CMOS 0.18µm process, the second sampling capacitor is set to 0.32pF. It is indeed composed by 9 minimum size elements resulting in $C_{s,2} = 9 \cdot 36\text{fF} \approx 0.32\text{pF}$. Together with $C_{I,2} = 5 \cdot 36\text{fF} \approx 0.18\text{pF}$, it implements the loop-coefficient a_2=9/5. All the capacitor sizes are summarized in Table XV.

TABLE XV
CAPACITOR SIZES OF THE ΔΣM

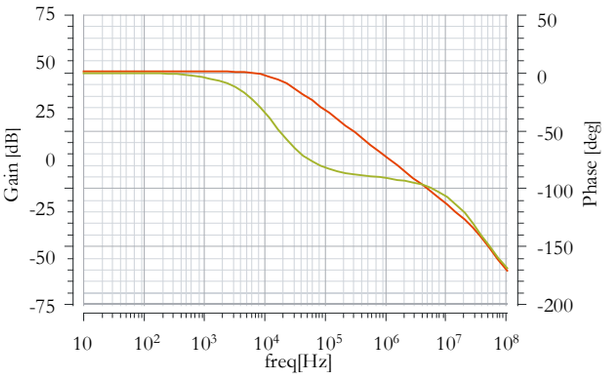
	Sampling capacitors	Integrating capacitors	Feed-forward capacitors
HRLB	$C_{s,1}$ = 16pF	$C_{I,1}$= 5.34pF	
MRMB	$C_{s,1}$ = 2.13pF	$C_{I,1}$= 0.71pF	
LRHB	$C_{s,1}$ = 0.5pF	$C_{I,1}$= 0.18pF	
all modes	$C_{s,2}$ = 0.32pF	$C_{I,2}$ = 0.18pF	C_{f0} = 3*36fF C_{f1} = 6*36fF C_{f2} = 3*36fF

The power-efficient gain-enhanced current mirror OTA, described in Section 4.3.2, is employed in both integrators. AC simulations have been performed in open loop configuration to obtain DC gain, *GBW*, and phase margin (PM) of the designed OTAs. Fig. 41 shows the Bode plots obtained for the different modes of the OTA. The results obtained from the simulations are summarized in Table XVI.

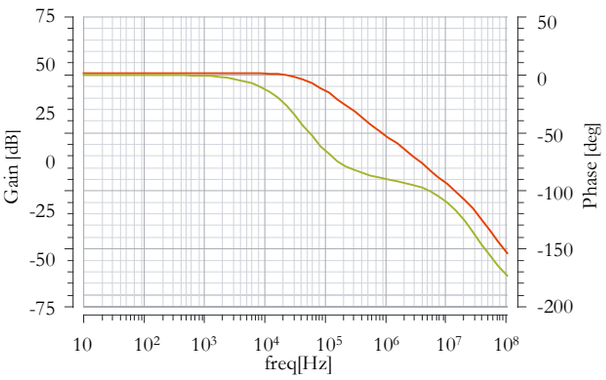
The power gating option is used in both the OTAs when the integrating phase φ_2 is not active. This time window corresponds to about 60% of the total sampling period T_s, as the two phases are not overlapping ($\varphi_1 = \varphi_2 \approx 40\% \cdot T_s$). During the power gating, the first-stage of the OTAs is kept ON while the modular output stages are switched OFF. As shown in Fig. 39, only the branches corresponding to the most power-efficient mode of the OTA are powered (MRMB mode for the first OTA, HRLB mode for the second OTA). With this technique, the OTAs exploit their programmability for minimizing the settling error during the integrating phase while consuming the lowest power possible during the rest of the period. The power-gating allows a power saving of up to 38% (in LRHB mode) with negligible circuit overhead and without affecting the modulator stability. The common-mode feedback loop is indeed never interrupted.



a)



b)



c)

Fig. 41. OTAs frequency response in HRLB mode (a) MRMB mode (b) and LRHB mode (c)

TABLE XVI
OTAS SIMULATION RESULTS

	HRLB		MRMB		LRHB	
	OTA1	**OTA2**	**OTA1**	**OTA2**	**OTA1**	**OTA2**
GBW (MHz)	1.41	1.4	2.6	2.1	7.76	8
DC gain (dB)	50.6	54	50.6	55	50.6	55
C_{load} (pF)	19.2	1.4	5.3	1.4	3.7	1.4
PM (deg)	87.7	76	85.6	68	75.5	68
IDC (μA)	4.8	0.9	4	1	5.6	8
IDC power-gating (μA)	4.3	0.9	4	0.9	4.6	3.7
Power saving w/ power-gating ON (%)	8		1		38	

The summing SAR-ADC quantizer described in Section 3.3.3 is also employed. It combines a 4-bit SAR ADC with the passive adder. The SAR features a dynamic comparator so that the quantizer power automatically scales with the different clock frequencies, and operates with asynchronous logic so that it does not need an additional high-frequency clock.

The prototype of the proposed modulator has been fabricated in a 0.18μm general-purpose CMOS process. Fig. 42 shows the die microphotograph. The active area of the modulator is 0.59 mm^2.

Fig. 43 shows the measured *SNR* and *SNDR* versus the input amplitude relative to full-scale. The measured *SNDR* curves show peak *SNDR*s of 99 dB, 87 dB, and 75 dB at –0.5 dBFS input. Fig. 44 shows the output spectrum obtained from a 16 K-point FFT for the three modes, for equal input level.

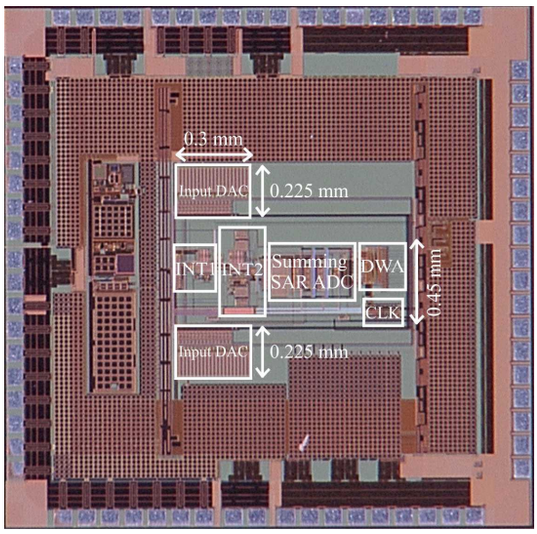


Fig. 42. Microphotograph of the reconfigurable ΔΣM

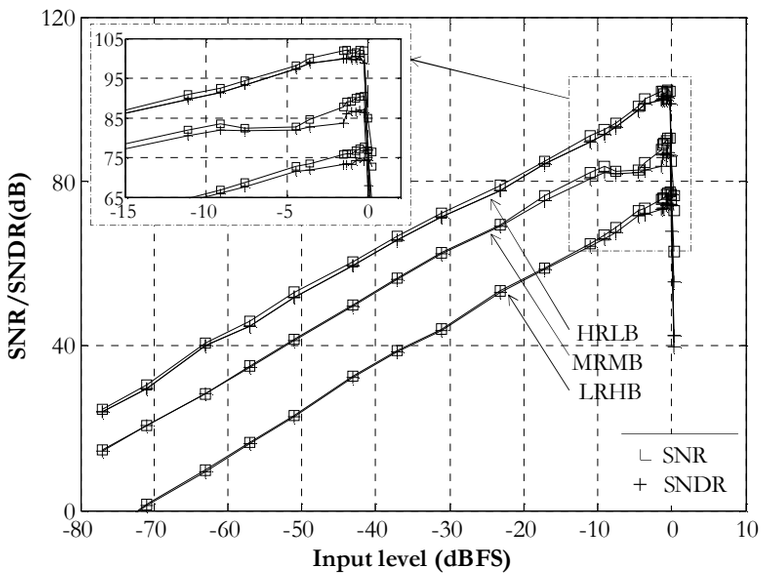


Fig. 43. Measured *SNR*/*SNDR* vs. input amplitude

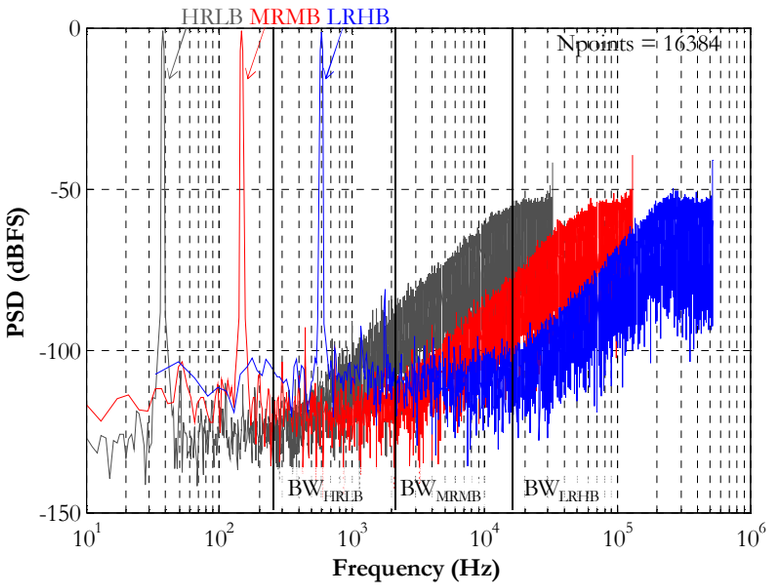


Fig. 44. Measured spectra at peak *SNDR* for HRLB (grey curve), MRMB (red curve) and LRHB modes (blue curve) for -0.5-dBFS input level

The total measured power consumption of the modulator with the power-gating option of the OTAs set to OFF is 9.6 μW in HRLB, 15 μW in MRMB and 49 μW in LRHB mode, respectively. The total power consumption with the power-gating option ON is 8.6 μW in HRLB, 15 μW in MRMB and 39 μW in LRHB mode, respectively. In the first case, the modulator achieves a *FoM* based on the *SNDR*s of 0.25 pJ/c.s. in HRLB, 0.2 pJ/c.s. in MRMB and 0.33 pJ/c.s. in LRHB, respectively. In the second case, the modulator achieves a *FoM* of 0.23 pJ/c.s., 0.2 pJ/c.s. and 0.27 pJ/c.s., respectively.

Table XVII summarizes the overall performance of the ΔΣM with power-gating option ON. The results obtained match the design specifications both in terms of achieved resolution (see Table XI) and in terms of power-efficiency. The *FoM* is

kept almost constant (between 0.2 and 0.27 pJ/c.s.) over the whole conversion range.

TABLE XVII
SUMMARY OF THE MEASURED PERFORMANCE (WITH POWER-GATING ON)

	HRLB	MRMB	LRHB
BW [Hz]	256	2048	16384
SNR [dB]	100.2	90.4	77.2
SNDR [dB]	99.1	87.1	74.8
SFDR [dB]	108.9	91.7	79.7
Power [μW]	8.6	15	39
FoM [pJ/c.s.]	0.23	0.2	0.27
Area [mm^2]		0.59	
CMOS process		0.18μm	
Supply [V]		1	

To validate the chosen approach to reconfigurability, the *variable-$C_{s,1}$* approach presented in Section 4.2, Fig. 45 compares the power breakdown of the reconfigurable ΔΣM obtained from the theoretical model with one obtained from the measurements. The results without power-gating of the OTAs are considered in the comparison, in analogy with the estimation of the static power in Section 3.2.4.

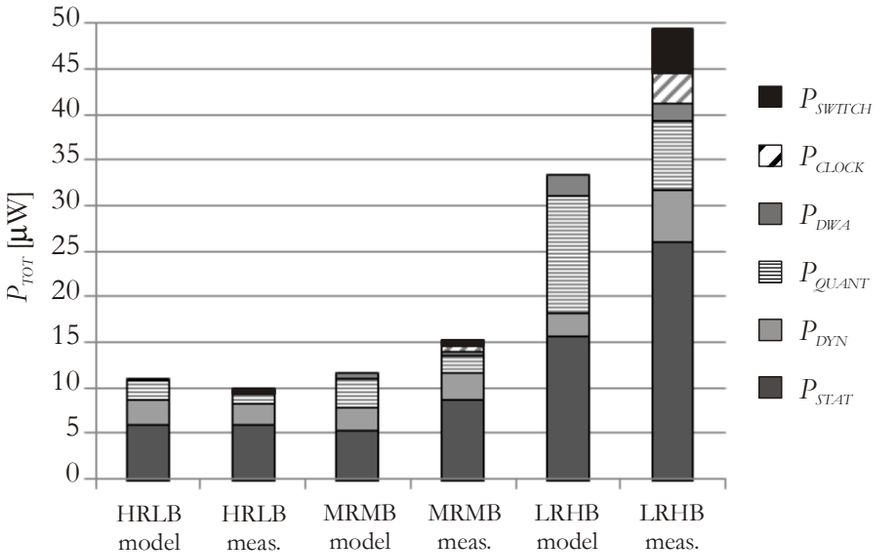


Fig. 45. Power consumption breakdown: comparison between theoretical model and transistor-level implementation in HRLB, MRMB and LRHB modes.

The values of P_{STAT} in the transistor-level implementation fit well to the contributions predicted by the model in HRLB mode. The differences in MRMB and LRHB modes are related to the real implementation of the OTAs. Issues with the OTAs stability made indeed necessary to spend a little more power in the OTAs than expected from the model. The dynamic power consumption in HRLB mode is the same in the model and the simulation since the capacitances have been dimensioned following the procedure described in Section 3.2.3. In MRMB mode, P_{DYN} is slightly higher in measurements due to the parasitic capacitance in the first integrator which is determined by the $C_{s,1}$ configuration switches. In LRHB mode the difference is even higher as the size of $C_{s,1}$ had to be increased with respect to the minimum bound provided by the model due to constraints on the minimum unit capacitor in the process used (see Table XIV and Table XV). The quantization power in the model is larger than that from the measurements. This is mostly due to the dynamic power for switching the SAR internal DAC. The model uses (41) as it

considers a binary weighted capacitor array for the SAR DAC, while the SAR DAC implemented at transistor level follows (42) as it is a segmented architecture with a central coupling capacitor. The values of P_{DWA} obtained in the real implementation are close to the theoretical estimation. Contributions of the clock generator circuit and of the analogue switches used for reconfiguring $C_{s,1}$ determine additional (but still negligible) power consumption in the real implementation.

The good agreement between the values of P_{TOT} obtained in HRLB and MRMB modes from the model and from the real implementation confirms the validity of the presented design methodology. The difference in LRHB mode (roughly 40%) is due to constraints given by the CMOS process (size of the minimum capacitor available) and to second-order effects in the transistor level implementation (capacitive parasitics, trade-off between *GBW* and stability in the OTAs). The *variable-*$C_{s,i}$ approach, which requires making all the capacitor switchable, would increase the problems related to the implementation of the reconfigurable ΔΣM. Tuning the size of all the $C_{s,i}$ would indeed result in larger parasitic capacitances due to the configuration switches.

Fig. 46 plots the performance results achieved by this work in the plane power per Nyquist sample rate P_{TOT}/f_{snyq} ($f_{snyq} = 2 \cdot BW$) versus resolution [5]. Performance data are displayed as a curve connecting the points associated to HRLB, MRMB and LRHB modes. By doing so, this reconfigurable ADC is compared in terms of power-efficiency with state-of-the-art tailored designs and reconfigurable oversampling ADCs already shown in Fig. 3. The trend lines for both *FoMs* defined in Section 1.1.2 are included: (1) and (2) are plotted as a straight line and as a dashed line for the numerical example of 100fJ/c.s. and 170dB, respectively.

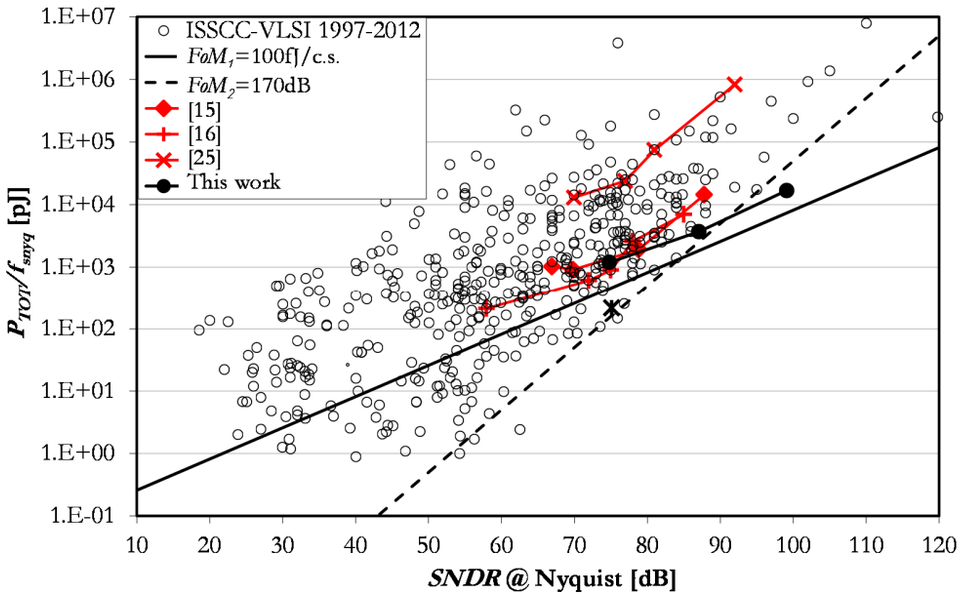


Fig. 46. Power-efficiency versus *SNDR* performance of this work compared to state-of-the-art tailored (ISSCC- VLSI 1997-2012) and reconfigurable oversampling ADCs [5]

The reconfigurable ΔΣM covers a wide *SNDR* region (between 74 and 99 dB) and is able to keep the *FoM* constant over the whole conversion range. The curve indeed agrees with the FoM_1-trend line, which is not the case for other reconfigurable ΔΣMs in Fig. 46. Moreover, the ΔΣM achieves state-of-the-art performance and shows a best-in-class performance for both HRLB and MRMB modes. In LRHB mode, one modulator targeting comparable *SNDR* show better power-efficiency than this modulator [81]. This IC implementations (represented as an asterisk in Fig. 46) is for medium-resolution and audio-frequency application. This design is a continuous-time ΔΣMs in which the power saving is obtained mainly in terms of static power, thanks to the use of more power-efficient OTAs. This choice would not be ideal for specifications considered here. First, in HRLB and MRMB modes we target low-frequency, we do not need the wide-bandwidth

performance CT modulators are usually targeted for. Second, in case high resolution is required, discrete-time modulators are preferred for their easier implementation as CT ΔΣMs are highly sensitive to jitter and process variations. Finally, DT modulators offer a straightforward reconfigurability by adjusting the sampling frequency.

Fig. 47 shows the reconfigurable design in the area versus resolution plane. The reconfigurable oversampling designs in Fig. 4 are plotted in the same plane for comparison [5].

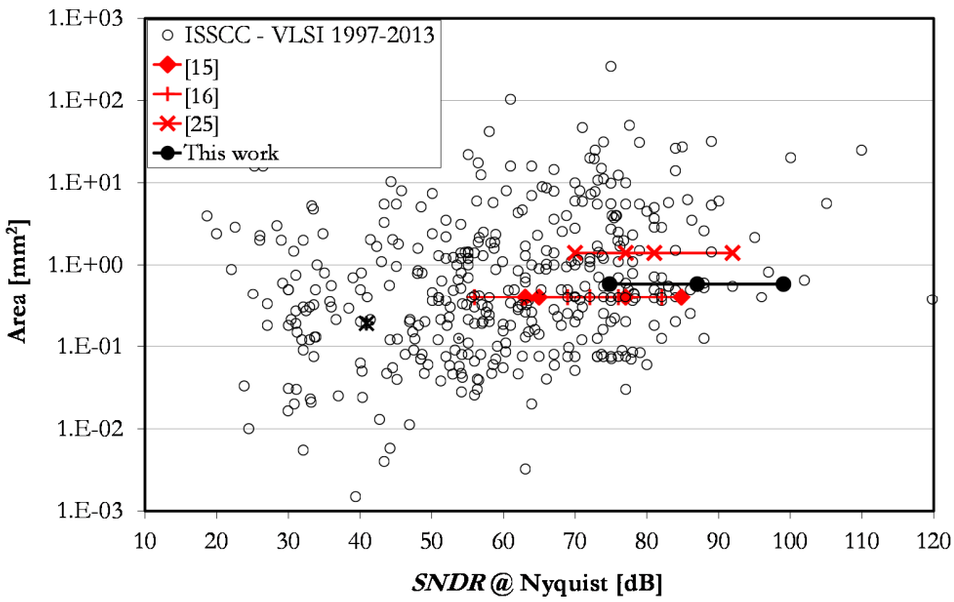


Fig. 47. Area-efficiency versus *SNDR* performance of this work compared to state-of-the-art tailored (ISSCC- VLSI 1997-2012) and reconfigurable oversampling ADCs [5].

Our chip achieves good area-efficiency, as the area occupied by this design is comparable to the area of custom ADCs targeting the same maximum *SNDR*. This result demonstrates the negligible area overhead of our reconfigurability approach,

which is competitive with area-efficient solutions adopted by state-of-the-art reconfigurable Nyquist ADCs (see reference [19] in Fig. 4).

4.5 Conclusion

In this chapter the design of power-efficient reconfigurable SC ΔΣMs was addressed. To find a power optimal reconfigurability approach, the method presented in the previous chapter was extended to address reconfigurable ΔΣMs with different modes of operation. The methodology was applied to the design of a ΔΣ modulator for bio-potential (EEG, ECG, EMG) and audio signals. As the size of the sampling capacitors is crucial in determining the total power consumption, two possible approaches to reconfigurability were compared. Programmable C_s in all integration stages (*variable-*$C_{s,i}$ approach); and first-stage $C_{s,1}$ programmable according to the target *ENOB* while the C_s in the other stages sized as in the highest resolution mode (*variable-*$C_{s,1}$ approach). For each of these strategies, we used the power estimation model of Chapter 3 to calculate the resulting power consumption in all the operational modes. Based on the result of their power comparison, the *variable-*$C_{s,1}$ approach was identified as the best compromise between power-efficiency and low design complexity. Indeed it only requires to change the size of the first integrator sampling capacitors and to adapt the power and the *GBW* of the OTAs to the sampling speed. As the equivalent load of the first integrator is minimized for the thermal noise level required in each mode, a significant reduction of the overall power is obtained.

Circuit techniques for the low-power implementation of this reconfigurability approach were then discussed. The transistor-level implementation of tunable

sampling capacitors and of the power- and speed- scalable programmable OTAs was presented.

Finally, the methodology for the design of power-efficient reconfigurable ΔΣMs was verified with a chip implementation. The IC implementation proves that the *FoM* can be both state-of-the-art and constant over the various modes by using the proposed design method for reconfigurable ΔΣMs.

5 Conclusions

This thesis contributes to the design of power-efficient and area-efficient reconfigurable ΔΣ modulators, i.e. modulators that are able to operate with a wide spread of effective resolution and signal bandwidth specifications.

The general conclusions of the thesis are summarized as follows:

1. It is possible to achieve optimum power-efficiency in point-solution ADCs by means of a proper design methodology.
2. Reconfigurability does not imply loss of *FoM* compared to corresponding point-solution ADCs if the reconfigurable ADC is properly designed.
3. Reconfigurable ADCs can achieve better area-efficiency than a number of point-solution ADCs used in parallel.
4. A method for the power-optimization of reconfigurable ΔΣMs is proposed which leads to power-efficient designs without loss of *FoM* due to reconfigurability.
5. We have contributed to improve state-of-the-art in the targeted range of *SNDR*, to shift towards the right the transition point between thermal-noise-limited and matching-limited designs on the plane power per Nyquist sample $P_{TOT}/2 \cdot BW$ against achieved *SNDR*. This achievement is obtained by using a combination of optimal architecture choice and circuit design that matches application requirements and technology limitations.
6. These results are not limited to the specific application chosen in this thesis. The procedure described here can be indeed adapted to other domains of resolution and bandwidth, to other regions of Murmann's plot. Alternatively, the same procedure can be extended to more complex architectures. For instance, for low-resolution high-frequency requirements, we can extend the power optimization procedure to cascade architectures in order to compensate for the limitation on the maximum *OSR*. Also, for those

requirements, continuous-time ΔΣ architectures can be considered in which constraints on OTA's speed are relaxed, thanks to the lack of sampling.

For the power-optimal design of point-solution ΔΣMs suitable for the specific applications considered in this thesis, the following conclusions can be drawn:

- FF architectures are better than FB architectures in terms of power-efficiency. The only exception happens for single-bit FB topologies because they use the use of power-efficient class-AB OTAs which minimize the static power. The adoption of a single-bit quantizer is allowed only for FB ΔΣMs, as stability problems occur in FF modulators. The best power efficiency is achieved for the low-bandwidth specifications considered in this thesis by employing a second-order FF architecture with a 4-bit quantizer and an *OSR* of 64.
- In FF topologies, indeed, the input of the first integrator does not depend on the modulator input. Consequently, the signal range can be reduced by employing multi-bit quantization. Multi-bit modulators require very good matching between circuit elements in the feedback DAC. This problem is solved by dimensioning the capacitors in the DAC to satisfy matching requirements and by including DWA algorithms. Moreover, as in FF ΔΣMs the signal transfer function is inherently unitary, DC gain and linearity requirements of the OTAs used to implement the integrators are relaxed.
- On top of the considerations above, the non-linearity issues that affect FB architectures are expected to increase their power consumption even more than as calculated in Section 3.2.
- The good agreement between the values of P_{TOT} obtained from the model and from the experimental implementation confirms the validity of the presented design methodology.

For the power-optimal design of reconfigurable ΔΣMs suitable for the specific applications considered in this thesis, the following conclusions can be drawn:

- The reconfigurable ADC presented here is matching-limited and its power consumption obeys a 2x increase per added bit. This implies that, on the plane power per Nyquist sample $P_{TOT}/2{\cdot}BW$ against achieved *SNDR*, the transition point beyond which state-of-the-art ADCs are estimated to be limited by thermal noise is shifted to *SNDR* values around 100 dB. This corner was indicated in [21] to be 75 dB.
- The good agreement between the values of P_{TOT} obtained in HRLB and MRMB modes from the model and from the experimental implementation confirms the validity of the presented design methodology for these two modes.
- For the LRHB mode there is a difference (roughly 40%) due to constraints given by the CMOS process (size of the minimum capacitor available) and to second-order effects in the transistor level implementation.
- The *variable-*$C_{s,1}$ approach is a better compromise than the *variable-*$C_{s,i}$ approach between power-efficiency and design complexity. Moreover, the *variable-*$C_{s,i}$ approach, which requires making all the capacitor switchable, would result in larger parasitic capacitances due to the configuration switches and in a even larger difference between the model and from the real implementation.

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Publications list

1. S. Porrazzo, F. Cannillo, C. Van Hoof, E. Cantatore, and A.H.M. van Roermund, Power optimization of high-resolution low-bandwidth SC ΔΣ modulators, Proceedings of the 2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum, Ed. K. Havrilla, 30 June - 1 July 2011, Orvieto, Italy.

2. S. Porrazzo, F. Cannillo, C. Van Hoof, E. Cantatore, and A.H.M. van Roermund, A power-optimal design methodology for high-resolution low-bandwidth SC ΔΣ Modulators, IEEE Transactions on Instrumentation and Measurement, 61(11), 2896-2904, Nov. 2012

3. S. Porrazzo, F. Cannillo, D. San Segundo Bello, C. Van Hoof, E. Cantatore, and A.H.M. van Roermund, A 155μW 88-dB DR discrete-time ΔΣ modulator for digital hearing aid application, Proceedings of IEEE BIOCAS 2012, 28-30 November 2012, Hsinchu, Taiwan.

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Summary

This thesis studies the design of reconfigurable ΔΣ modulators which are able to operate with a wide set of effective resolution and signal bandwidth specifications. The aim is to improve the performance of reconfigurable ΔΣMs with respect to power-efficiency and area-efficiency criteria. The focus of the work is on low-pass discrete-time ΔΣ single-loop architectures implemented using switched capacitor techniques.

The study is applied to the AD conversion of bio-potentials in ultra-low-power sensors for wireless body area networks. ΔΣMs must thus offer high-resolution and linearity to enable accurate conversion of small amplitude signals, possibly in the vicinity of strong interferes.

Chapter 2 introduces ΔΣ architectures foundations with respect to their ideal behaviour and their performance criteria. A classification of practical implementations of ΔΣ modulators is presented. Moreover, an overview of state-of-the-art reconfigurable ΔΣMs is given and design choices which limit the scope of the thesis are motivated.

Chapter 3 presents a methodology for the power-optimal design of high-resolution low-bandwidth switched-capacitor ΔΣMs. The method is based on an analytic model of all different contributions to the power dissipation of a SC single-loop ΔΣM which enables an accurate system-level optimization. As a second step, techniques that enable a further improvement of power-efficiency at the circuit level are discussed, with particular emphasis on a novel circuit solution which combines multi-bit quantization and analogue addition. Finally, the design of two high-

resolution ΔΣMs for application in hearing-aids is discussed both at the system and at the circuit level. The comparison between the power estimated by the analytic model and transistor-level simulations validates the proposed design methodology. The power-efficiency of the summing SAR quantizer is confirmed by measurement results.

Chapter 4 presents a methodology to design reconfigurable switched-capacitor ΔΣ modulators that are able to keep the power-efficiency constant and optimal for a set of different resolutions and bandwidths. As the size of the sampling capacitors is crucial to determine power consumption, three approaches to achieve reconfigurability are compared: dimension the sampling capacitors to achieve the highest resolution and keep them constant, change only the first sampling capacitor according to the targeted resolution or program all sampling capacitors to the required resolution. The second approach results in the best compromise between power-efficiency and low design complexity. A reconfigurable ΔΣM for biomedical applications is designed, fabricated in a 0.18μm CMOS process and measured to validate experimentally the proposed methodology.

Summarizing, the main results are:

- a methodology for the power-optimal design of high-resolution low-bandwidth switched-capacitor ΔΣMs based on an analytic model of all different contributions to the power dissipation;
- a methodology to design reconfigurable switched-capacitor ΔΣ modulators that are able to keep the power-efficiency constant and optimal for a set of different resolutions and bandwidths;
- a novel circuit solution which combines multi-bit quantization and analogue addition for improved power efficiency;

- the methodologies and the circuit solutions described have been experimentally verified with IC implementations. In particular a reconfigurable ΔΣM for biomedical applications offering state-of-the-art power efficiency in all modes of operation and low area overhead has been designed, fabricated in a 0.18μm CMOS process and measured.

Curriculum Vitae

Serena Porrazzo was born on 14-09-1984 in Como, Italy.

After finishing Maturita'Classica in 2003 at "Liceo Classico A.Volta" in Como, Italy, she studied Biomedical Engineering at Politecnico di Milano in Milano, Italy. In 2006 she obtained her bachelor degree with major in electronic design for biomedical instrumentation. She received her master degree in Electrical Engineering from Politecnico di Milano in 2008; her master thesis project consisted of the design of an Ultra-Low Power Operational Amplifier for Biomedical Devices and was carried out in collaboration with IMEC-NL Holst Center, Eindhoven, The Netherlands. From March 2009 she started a PhD project at the Mixed-Signal Microelectronics (MSM) group of the Eindhoven University of Technology in Eindhoven, The Netherlands, of which the results are presented in this dissertation. Since May 2013 she is employed at Maxim Integrated Products in Milan, Italy.