# Automated architecture synthesis and application mapping for ASIP based adaptable MPSoCs

# Automated Architecture Synthesis and Application Mapping for ASIP based adaptable MPSoCs[1]

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**ABSTRACT**

**Recent developments in modern embedded system technology have enabled the development of complex heterogeneous multiprocessor systems on single chips (MPSoCs) and created an up surge in high-performance and low-power embedded system design. This paper focuses on the automatic architecture synthesis and application restructuring and mapping for customizable ASIP-based MPSoCs. It briefly discusses the exploration methodology proposed for this purpose by the European research project ASAM of the ARTEMIS program.**

KEYWORDS: embedded systems, heterogeneous multi-processor system-on-chip (MPSoC), ASIP synthesis, design automation

## 1 Introduction

Recent developments in modern embedded system technology have enabled the development of complex heterogeneous multiprocessor systems on single chips (MPSoCs) and created an up surge in high-performance and low-power embedded system design. An embedded system serves a specific aim in a certain larger embedding system through repeatedly executing specific processes required by its application. An embedded system is specially designed to serve the execution of its specific task and needs to satisfy requirements related to attributes such as functional behavior, reaction speed or throughput, energy consumption, physical size, price, etc. The recent progress in nano-electronic technology and new applications of embedded systems fostered a situation in which increasingly complex and sophisticated embedded systems are required to fulfill real-time constraints with extremely tight energy, power, area and cost budgets. Moreover, many embedded systems are required to be highly flexible in order to enable hardware reuse among different product versions in

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reaction to market shifts, adherence to evolving standards or user requirements, and easy modification during development or even their field use. As a consequence, complex design and development challenges involving multi-objective MPSoC optimization and adequate resolution of many complex design trade-offs, have to be faced.

Our research addresses the development of heterogeneous MPSoCs based on configurable and extensible application specific instruction-set processors (ASIPs). MPSoC design technology based on adaptable ASIPs provides an extremely flexible platform that is able to deliver high performance and low energy consumption at the same time which makes it applicable for a broad range of applications and is suitable for several implementation technologies. However, despite a decade of research in the field of SoC architecture synthesis, an architecture synthesis methodology and tools for heterogeneous customizable MPSoCs based on adaptable ASIPs have not been built.

This paper focuses on the automatic architecture synthesis and application restructuring and mapping for customizable ASIP-based MPSoCs and discusses the exploration methodology proposed for this purpose by the European research project ASAM of the ARTEMIS program.

## 2 Architecture Platform, Applications, Issues and Challenges

The architecture platform targeted in the ASAM project is a configurable and extensible heterogeneous multi-ASIP platform. In particular, the project targets the MPSoC platforms of its industrial partners involving generic ASIPs customizable through instantiation (configuration) and extension. Each ASIP forms a VLIW machine capable of executing parallel software with a single thread of control supporting both SIMD and MIMD processing. The numbers, kinds, and parameters of functional units, issue slots, register files, memories, interfaces, etc. from an existing library can be selected freely, but also new modules can be developed and exploited for a specific application.

Several such different ASIPs, each customized for a particular part of a complex application, can be interconnected with global memories and other sub-systems using a configurable hierarchical interconnection network, and implemented on one chip together with possible hardware accelerators and other digital or analog sub-systems. Several such powerful ASIPs with up to 100 issue slots in total, each for 64-way vector processing, can be placed on a single chip implemented in 22nm CMOS technology, can deliver up to 1Tops/s, when operated at 400–600MHz, with a power consumption far below the upper limit of mobile devices.

The MPSoC design technology based on adaptable ASIPs is relevant for a very broad range of application domains (e.g. telecommunications, multi-media, medical, etc.) and for cross-domain convergence products.

Traditionally, embedded systems development involves largely disjoint processes, where the computation platform and the application software are developed largely independently by different teams using different tools. This leads to inefficiency, errors, and costly reiterations of the design process. Moreover, high-performance embedded applications require an application specific computation platform to satisfy the stringent requirements. Therefore, the computing platform and application software have to be developed largely in parallel. Unfortunately, the efficiency of the required parallel development technology is much too low currently, due to the lack of effective automated methods of industrial strength, and

weak interoperability of the architecture, algorithm, HW/SW, and hardware synthesis tools. While most of the existing methods and tools for ASIP construction are devoted to a single processor design, in a customizable multi-ASIP MPSoC its various ASIPs have to be customized in combination, and in a strict relation to the selection of the number of ASIPs, as well as to the scheduling and mapping of the application's required computations on the particular ASIPs. The issues and challenges in the design of massively parallel heterogeneous MPSoCs based on adaptable ASIPs for modern highly-demanding applications are discussed in more detail in [JL11].

# 3 Approach

The ASAM project aims to tackle the problems and challenges, as briefly explained in the previous section, by proposing an uniform design flow for efficient exploration of the architecture alternatives and application mapping trade-offs. The ASAM uniform design flow consists of two main sub-tasks: Macro-architecture (MPSoC-level) synthesis, and micro-architecture (ASIP-level) synthesis. Coarsely speaking, the macro-architecture synthesis accounts for the decision on the number and type of the ASIP processors, the task-level partitioning of an application, and adequate global memory and interconnection structures, while the micro-architecture synthesis takes care of the actual ASIP synthesis. In contrast to the traditional approaches (separating these two tasks, as well as, hardware and software development) followed in the state-of-the-art methods, ASAM design flow proposes one coherent and complete approach due to the strong interrelationships between the macro- and micro-architecture sub-tasks. To create feedback for both architecture design levels, a simulation and FPGA emulation prototyping environment will be used. Figure 1 demonstrates the high-level view of the ASAM design flow.

Realization of the proposed uniform design flow requires an unified synthesis and prototyping environment that involves the collaborating processes of the multi-objective macro-architecture design space exploration (DSE) and construction of the multi-ASIP system-level architecture, and the multi-objective micro-architecture exploration and architecture customization of particular generic ASIPs. The exploration and synthesis decisions are based on the application and platform analysis and restructuring(for parallelism exploitation), it produces feedbacks to the DSE processes on physical characteristics of the proposed solutions (area, delay/throughput, power) and is refined against the results of the simulation and a FPGA-based emulation. The macro-architecture synthesis proposes to use a certain number of customizable ASIP cores and assigns them parts of the application to be executed. The micro-architecture synthesis customizes each of the ASIP cores together with its local memories to execute the assigned application part as effective and efficient as possible. After several exploration iterations an optimized MPSoC architecture is constructed.

# 4 Conclusion

Highly effective, efficient and flexible parallel systems for demanding embedded applications usually involve small numbers of highly optimized powerful ASIPs. The ASAM project will facilitate the creation of such systems by developing a consistent highly efficient automatic synthesis flow from the algorithmic application specification down to its

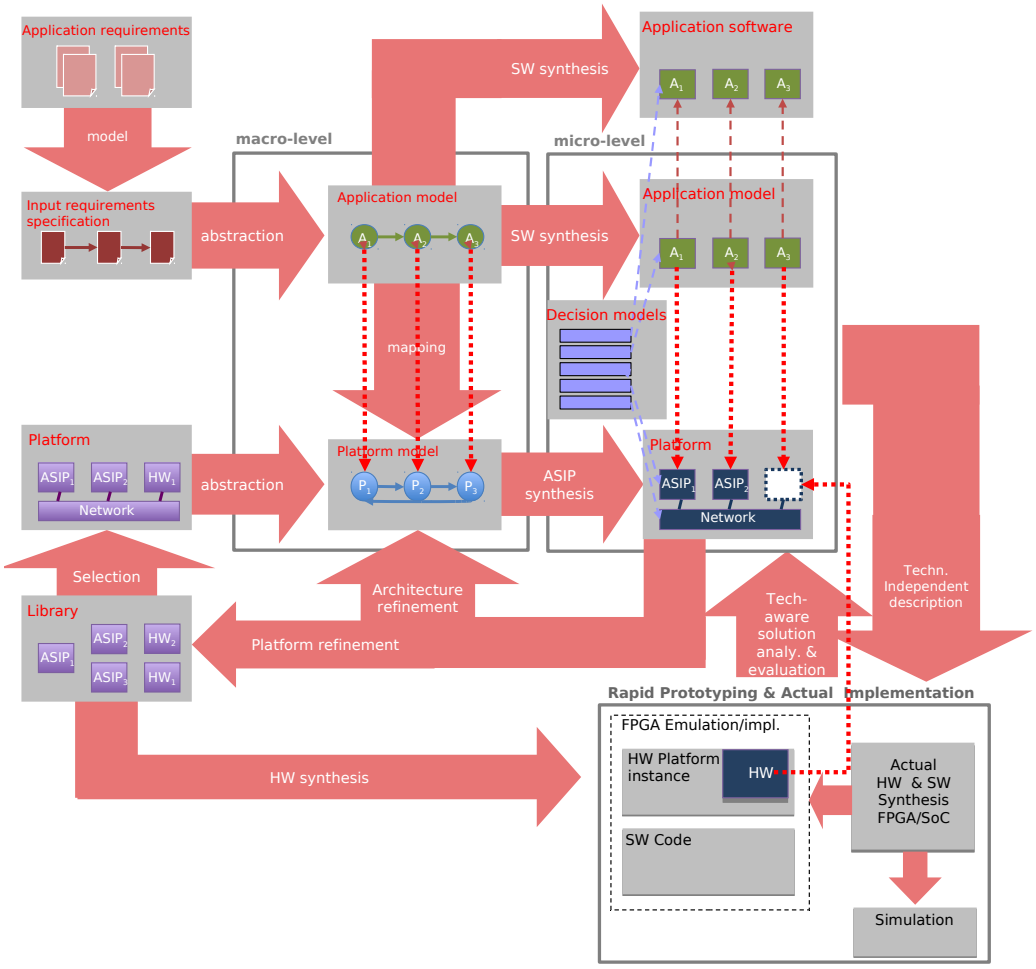


Figure 1: High-level ASAM design flow

hardware/software implementation at the circuit/code level. The new coherent automated design environment will enable the system and algorithm designers to perform rapid exploration of the high-level algorithm and architecture solution spaces, and in consequence, quickly develop high-quality designs. The ASAM webpage [web] provides more information about the research of the ASAM project and its up-to-date status overview.

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