

Origin of multiple memory states in organic ferroelectric field-effect transistors

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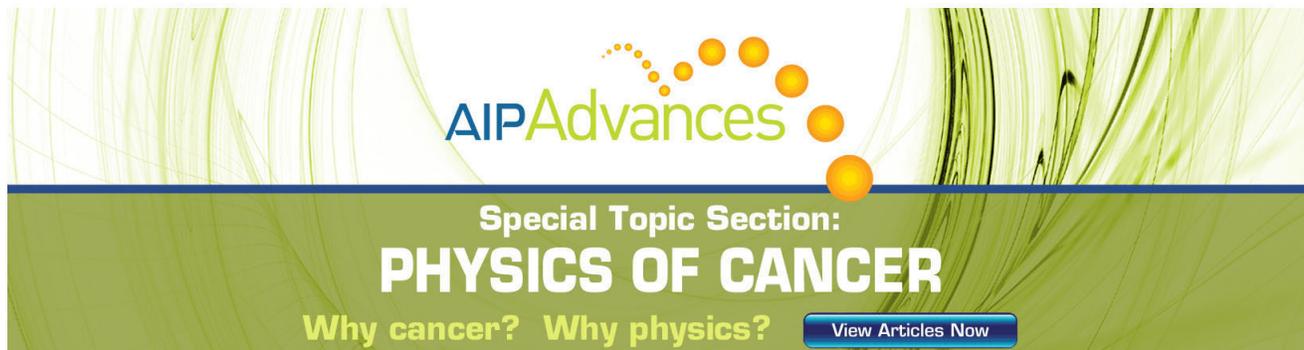
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Origin of multiple memory states in organic ferroelectric field-effect transistors

Benjamin Kam,^{1,2,a)} Xiaoran Li,^{3,4} Claudio Cristoferi,⁵ Edsger C. P. Smits,³
Alexander Mityashin,^{1,2} Sarah Schols,¹ Jan Genoe,¹ Gerwin Gelinck,³
and Paul Heremans^{1,2}

¹*Polymer and Molecular Electronics, IMEC, Kapeldreef 75, 3001 Leuven-Heverlee, Belgium*

²*ESAT, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven-Heverlee, Belgium*

³*TNO-Holst Centre, High Tech Campus 31, 5656 AE Eindhoven, The Netherlands*

⁴*Eindhoven University of Technology, Den Dolech 2, 5612 AZ Eindhoven, The Netherlands*

⁵*Politecnico di Torino, Corso Duca degli Abruzzi 24, Torino, Italy*

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In this work, we investigate the ferroelectric polarization state in metal-ferroelectric-semiconductor-metal structures and in ferroelectric field-effect transistors (FeFET). Poly(vinylidene fluoride-trifluoroethylene) and pentacene was used as the ferroelectric and semiconductor, respectively. This material combination in a bottom gate—top contact transistor architecture exhibits three reprogrammable memory states by applying appropriate gate voltages. Scanning Kelvin probe microscopy in conjunction with standard electrical characterization techniques reveals the state of the ferroelectric polarization in the three memory states as well as the device operation of the FeFET.

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Organic ferroelectric field-effect transistors (FeFET) have received much attention in the last few years as non-volatile reprogrammable memory devices in organic electronics.^{1,2} In such a FeFET, the gate dielectric of the transistor is replaced by a ferroelectric. Ferroelectric materials have permanent dipoles, which can be aligned by applying an electric field. If countercharges are present, these dipoles remain oriented when the applied electric field is removed. Due to these reversible dipoles, transfer characteristics of FeFETs exhibit a hysteresis, i.e., the forward and backward scans show two different onset voltages. Hence, FeFETs can be used as binary memory devices.³

The exact mechanism behind the bi-stable operation of FeFETs is still unclear. The discussion has risen on whether the ferroelectric layer is polarized or depolarized in the low source-drain current (“OFF”) state. In previous studies, metal-ferroelectric-semiconductor-metal (MFSM) structures were investigated.^{4–8} The ferroelectric polarization state in a FeFET however cannot be easily extracted from this structure because the channel region lacks a metal electrode. To polarize the ferroelectric in the channel, compensating charges also need to travel laterally along the ferroelectric/semiconductor interface into the channel region. Moreover, the source-drain current transition from the “OFF” to the high current (“ON”) state is found to be either gradual, starting from positive gate voltages^{4,9} or abrupt, close to the (negative) coercive voltage.^{3,10} Such an abrupt transition at the coercive voltage is also observed in ambipolar FeFETs,¹¹ in which the ferroelectric can switch between two fully polarized states.¹² The FeFETs in Refs. 3 and 10 however do not show ambipolar behavior: only hole current was observed. Ambipolarity can, therefore, not explain the different source-drain current transitions.

In this work, we investigate the ferroelectric polarization state in MFSM structures and in thin-film FeFETs. We demonstrate FeFETs that are reprogrammable in three memory states. The occurrence of three memory states is explained by three possible combinations of the ferroelectric polarization under the source-drain contact area and that under the channel area.

Bottom gate—top contact FeFETs, metal-ferroelectric-metal (MFM), and MFSM structures were fabricated in this study. Gate electrodes (5 nm Ti and 30 nm Au) were first formed on glass substrates (Eagle XG, Corning) by evaporation and were patterned by photolithography. Subsequently, poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] with 81 mol. % VDF (Solvay Solexis) was spin-coated at 2000 rpm from a filtered 42.75 mg/ml solution in cyclopentanone. The film was then annealed at 126 °C in a nitrogen glovebox for 1 h. The thickness of the resulting P(VDF-TrFE) film was 160 nm, as measured with a surface profilometer (Dektak, Veeco). For the FeFETs and MFSM structures, a 30 nm thick layer of pentacene was then thermally evaporated ($p \sim 10^{-8}$ Torr) at a rate of 0.25 Å/s and with a substrate temperature of 68 °C. Finally, the top electrodes of the MFM and MFSM structures and the top contacts of the FeFETs were formed by thermal evaporation of gold through a shadow mask.

All electrical measurements were performed in a nitrogen glovebox and samples were never subjected to air before any electrical measurements. Electric displacement versus applied voltage (D-V) hysteresis loops were measured on the MFM and MFSM structures with a virtual-ground integrator circuit. Transistor characteristics were measured using two computer-controlled Keithley 2602 units. Scanning Kelvin Probe Microscopy (SKPM) measurements were performed in a dry nitrogen environment using a Veeco Dimension 3100 with a NanoScope IVa controller operating in the lift mode. First, the height profile was recorded with tapping-mode atomic force

^{a)}Electronic mail: Benjamin.Kam@imec.be.

microscopy. In the second pass, the tip was lifted at a height of 50 nm above the surface, and the local surface potential distributions along the transistor channels were recorded during device operation at different gate voltages.

Saturated D-V hysteresis loops were measured on MFM and MFSM structures (see Fig. 1). For the MFM capacitor, the coercive field (E_C) is 0.52 MV/cm, similar to previously reported values.¹³ In such hysteresis loop measurements, actually the difference between the remnant polarizations of the two stable states is measured, i.e., $\Delta P_r = P_{r+} - P_{r-}$. For the MFM capacitor, ΔP_r is equal to 13.1 $\mu\text{C}/\text{cm}^2$. For the MFSM structure, ΔP_r is equal to 11.7 $\mu\text{C}/\text{cm}^2$. This value is 89% of the value which was obtained for the MFM capacitor, which confirms that the ferroelectric in the MFSM structure is close to fully polarized in two stable states. The MFSM structure shows a similar behavior as the MFM capacitor for negative voltages but has an additional kink at positive voltages. Because current is the derivative of charge with respect to time, the kink is equivalent to two current switching peaks at +6.5 V and 12 V, as shown in the current density measurements in the inset of Fig. 1. This shows that the switching of the MFSM structure at positive applied voltages occurs via two switching events, in agreement with earlier reports.^{5,6} Compared to Ref. 5 however, in which a similar device structure was studied, the second switching event is much more pronounced in our devices, which is most likely caused by differences in processing and/or measurement conditions. In between the two switching events, the ferroelectric is either depolarized or partially polarized.⁵

Programming the MFSM and the FeFET into the intermediate depolarized (or partially polarized) state is possible by applying a positive V_{GS} of 7.5 V, which is in between the two switching peaks. Therefore, the following programming procedure was applied on the FeFET (Fig. 2(a)). The first V_{GS} sweep is from +20 V to -20 V and back to +20 V: this ensures complete programming and erasing. Two stable states are present at $V_{GS} = 0$ V: an “OFF” state ($I_D < 10^{-10}$ A) and

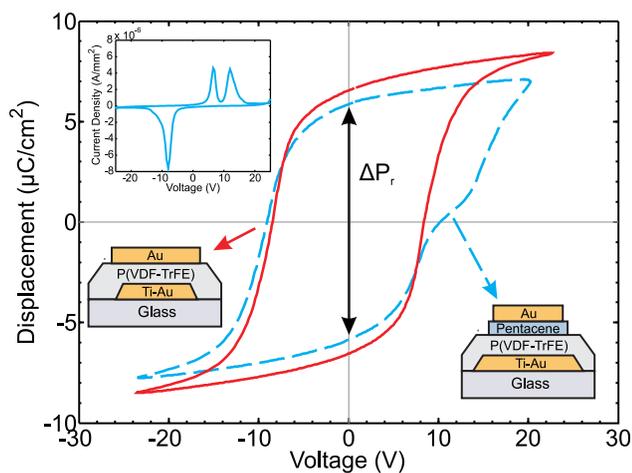


FIG. 1. Ferroelectric hysteresis loops of a MFM (red full curve) and MFSM (blue dashed curve) structure with P(VDF-TrFE) and pentacene as ferroelectric copolymer and organic semiconductor, respectively. The loops were measured using a virtual-ground integrator circuit at 100 Hz. Voltage was applied on the bottom electrode, while the top electrode was grounded. Thickness of the P(VDF-TrFE) and pentacene layer was 160 nm and 30 nm, respectively. The insets show the current density measurement on the MFSM structure and the device structures.

an “ON” state ($I_D \approx 10^{-7}$ A). A large memory window of 10 V is observed (taken arbitrarily at $I_D = 10^{-8}$ A). The onset voltage in the forward scan is located at a negative gate voltage: $V_{\text{on,forward}} = -2.6$ V. In the second sweep, the gate is brought from 0 V to -20 V and then to the intermediate gate voltage of +7.5 V (purple squares): the FeFET is now programmed in the “Intermediate” state. The subsequent sweep (third sweep) goes again from 0 V to -20 V and to the intermediate gate voltage of +7.5 V (orange crosses). $V_{\text{on,forward}}$ is now positive ($\approx +1.9$ V) indicating that the FeFET was indeed programmed in a state, different than the previous “ON” and “OFF” states. The backward scan of this third sweep is identical to that of the previous sweeps, which shows that the FeFET is switching from the “Intermediate” state to the “ON” state. A fourth sweep from 0 V to -20 V and to the intermediate gate voltage of +7.5 V (red triangles) gives identical curves as the third sweep, which shows that the switching to the “Intermediate” state is repeatable. Retention measurements show that all three memory states are stable with respect to time (see Fig. 2(b)).

To understand the occurrence of three memory states, the surface potential along the transistor channel was measured using SKPM. SKPM is a powerful tool to study the

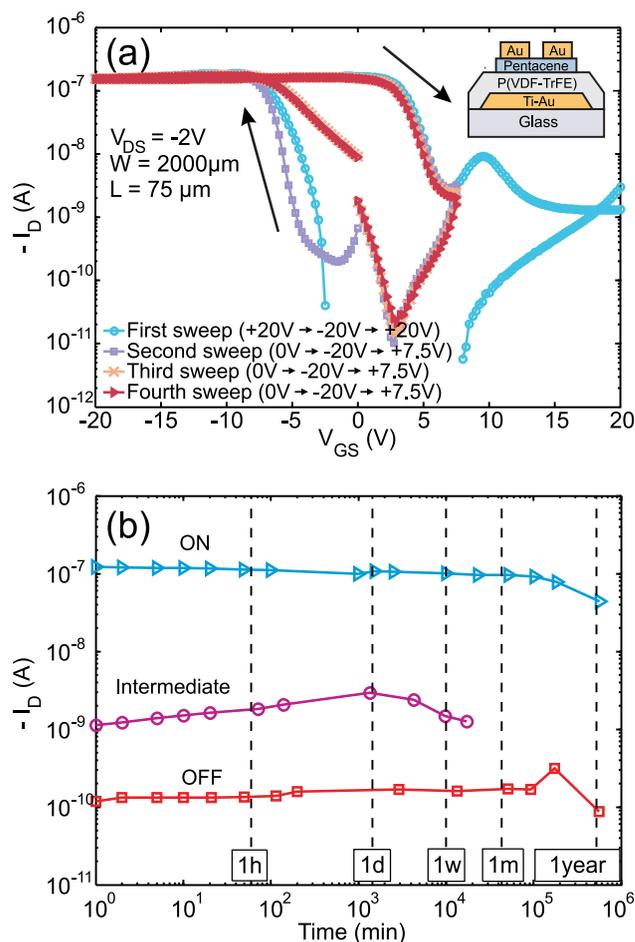


FIG. 2. (a) Transfer characteristics of a bottom gate-top contact FeFET with pentacene as organic semiconductor. Four consecutive gate voltage sweeps were measured. The different gate voltage sweeps illustrate the possibility of three reprogrammable states in this memory device. The inset shows the cross-section of the FeFET. (b) Retention measurement of the three memory states. The current was measured by sweeping a small gate voltage (0.1 V) around 0 V while the drain was biased at -2 V.

local charge-transport properties during device operation. It gives information on the charge distribution along transistor channels by mapping the local electrostatic potential on the sample surface. The FeFET was first programmed to either the “OFF” state or the “Intermediate” state using the programming scheme described above. Potential profiles were then measured in the forward and backward scans at predefined values of V_{GS} . The potential profiles starting from the “OFF” state are shown in Figs. 3(a) and 3(b), whereas the profiles starting from the “Intermediate” state are shown in Figs. 3(c) and 3(d).

At positive voltages in the forward scan (only $V_{GS} = +7.5$ V is shown here), the potential profiles are curved upward in both “OFF” and “Intermediate” cases. This indicates that the channel was depleted of charges after it was programmed to either state. Because a ferroelectric must have countercharges to remain polarized, the potential profiles, therefore, show that the channel region cannot be fully polarized in the “OFF” nor in the “Intermediate” state. This observation is in agreement with the hysteresis measurement on the MFSM structure. In the MFSM structure, electrons can be injected from Au into pentacene^{14–16} and only need to travel a short distance (30 nm) to the ferroelectric/semiconductor interface to act as compensating charges.⁵

However, for the channel region in our FeFETs, electrons would need to travel laterally along the ferroelectric/semiconductor interface, a feature which is known to be difficult for most interfaces due to electron traps.¹⁷ Moreover, the electrons would need to travel a much longer distance of several microns laterally, and under the influence of a smaller electric field in the channel region compared to the contact region. A severely hampered electron transport along the interface would also explain why we do not observe any electron current at positive V_{GS} in our pentacene FeFETs, in contrast to ambipolar FeFET devices, which show both hole and electron currents.¹¹ Because the ferroelectric polarization state in the channel region is the same in the “OFF” and “Intermediate” cases, the difference in $V_{on,forward}$ that we observe in our FeFETs must be found in the difference in polarization state of the MFSM structures that are found underneath the source/drain contact region.

For V_{GS} between 0 V and -6 V in the forward scan, potential drops close to the source and drain contacts can be clearly observed in the “OFF” case. Interestingly, the potential drops disappear abruptly at a slightly more negative V_{GS} of -8 V. The potential profile then becomes more linear, indicative of a transistor operating in the linear regime. In the “Intermediate” case, however, the potential profiles in the

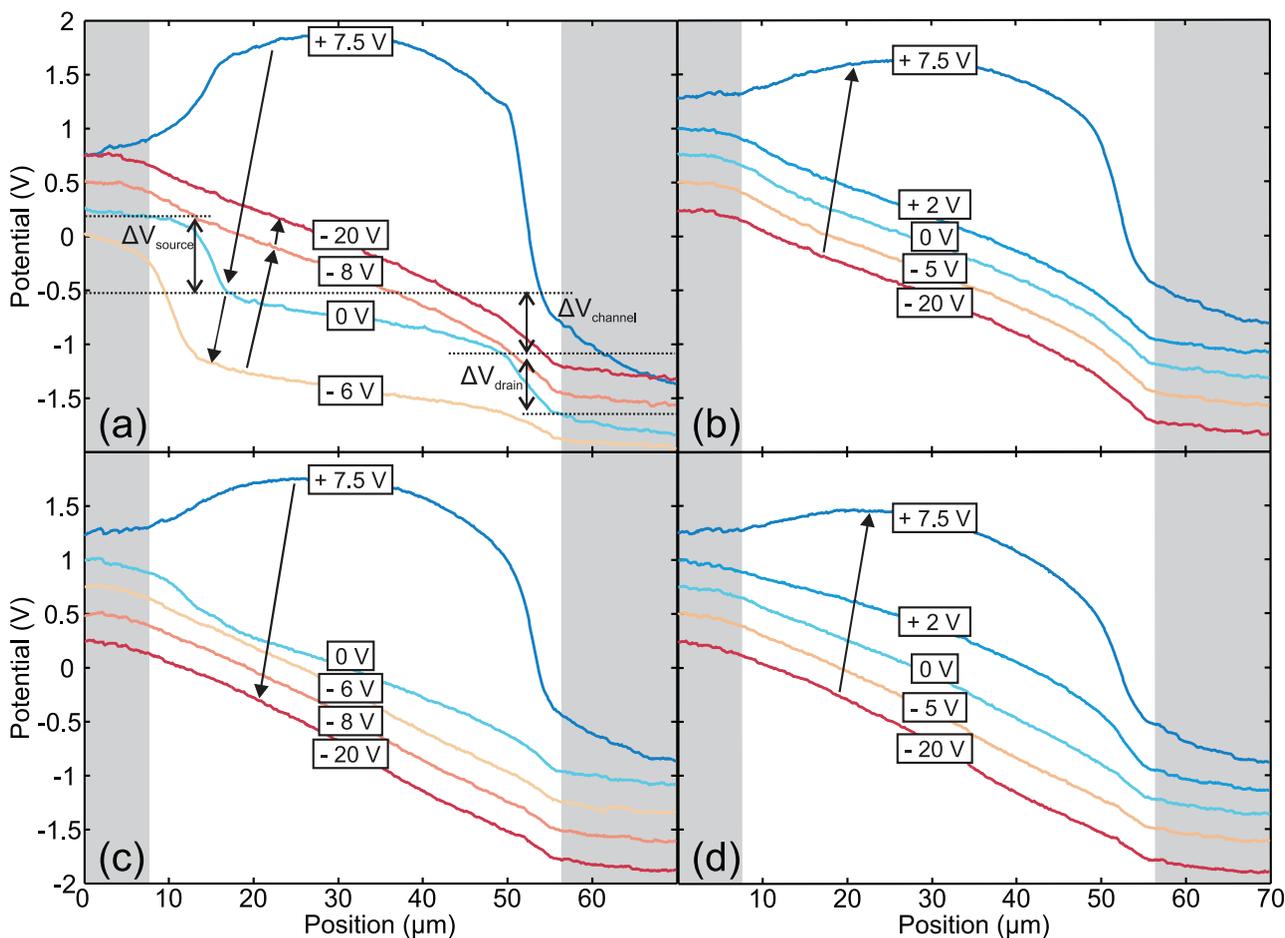


FIG. 3. Potential profiles after programming the FeFET to: (a) and (b) the “OFF” state and: (c) and (d) the “Intermediate” state. Gate voltage was swept starting from positive voltages: $+20$ V and $+7.5$ V for the “OFF” and “Intermediate” case, respectively. Full arrows indicate the sweep direction: (a) and (c) forward scans and (b) and (d) backward scans are shown. During all measurements, the drain was biased at -2 V and the source was grounded. For clarity, the profiles are shifted over the potential axis and only profiles at predefined V_{GS} are shown. Gray regions indicate the positions of the source (left) and drain (right) electrodes.

forward scan are clearly different. In this case, slight potential drops near the source and drain contacts can still be discerned for $V_{GS} = 0$ V, but they disappear gradually instead of abruptly when applying a more negative V_{GS} . Again the potential profile then becomes more linear, indicating that the transistor is now operating in the linear regime. In the backward scan, the potential profiles remain linear until $V_{GS} \approx +2$ V in both cases (see Figs. 3(b) and 3(d)). This is in agreement with the transfer characteristics: I_D remains high in the backward scan until $V_{GS} \approx +2$ V.

A potential drop near a contact is indicative of a contact resistance, i.e., $R_{\text{contact}} \gg R_{\text{channel}}$.^{18,19} In the “OFF” case of our FeFET, almost the complete source-drain voltage (-2 V) is dropped near the contacts: $\Delta V_{\text{channel}} \ll (\Delta V_{\text{source}} + \Delta V_{\text{drain}})$. Consequently, the source-drain current is limited by this contact resistance and a low I_D is, therefore, seen in the transfer curves for V_{GS} between 0 V and -6 V in the forward scan. The gate voltage, at which the potential drops disappear in the “OFF” case, corresponds strikingly with the coercive voltage of the ferroelectric layer (≈ -8 V, the voltage corresponding to the switching peak in the J-V curve) and also with the voltage at which the FeFET fully turns on. Recently, Asadi *et al.* reported a ferroelectric diode memory device²⁰ in which the polarization of the ferroelectric phase was found to modulate the injection process in the semiconductor and, therefore, causes a bistable operation in these devices.²¹ These previous findings and our current experimental observations lead us to explain the different $V_{\text{on,forward}}$ in the “OFF” and “Intermediate” case by different injection properties of the contacts, resulting from the different states of ferroelectric polarization underneath these contacts. This insight could also explain the different “OFF” to “ON” source-drain current transitions that have been observed in literature when different semiconductors are used: Naber *et al.* showed that P3HT MFSM structures only switch between a polarized and a depolarized state, and a gradual “OFF” to “ON” transition was found for P3HT FeFETs.⁴

A description for the device operation of an unipolar (p-type) organic staggered FeFET is now proposed as schematically shown in Fig. 4. In the “OFF” and “Intermediate” state, the ferroelectric layer underneath the channel region is not polarized due to the hampered accumulation of electrons at the ferroelectric/semiconductor interface. In the “OFF” state, the ferroelectric polarization underneath the source/drain contacts causes an injection barrier, which prevents holes from readily entering the channel region. This situation persists until the ferroelectric underneath the contacts is switched. Because a significant source-drain current can only flow when the ferroelectric has switched, the FeFET exhibits a negative $V_{\text{on,forward}}$. In the “Intermediate” state, the ferroelectric underneath the source/drain contacts is not polarized and no injection barrier is present. The FeFET then displays a positive $V_{\text{on,forward}}$, which would correspond to the V_{on} of a hypothetical FET with a dielectric similar to P(VDF-TrFE) but without the ferroelectric property. In the “ON” state, positive charge carriers can easily travel laterally along the ferroelectric/semiconductor interface. A conductive channel then forms, which simultaneously acts as the compensating charges for the ferroelectric layer in the channel region. The remnant polarization of

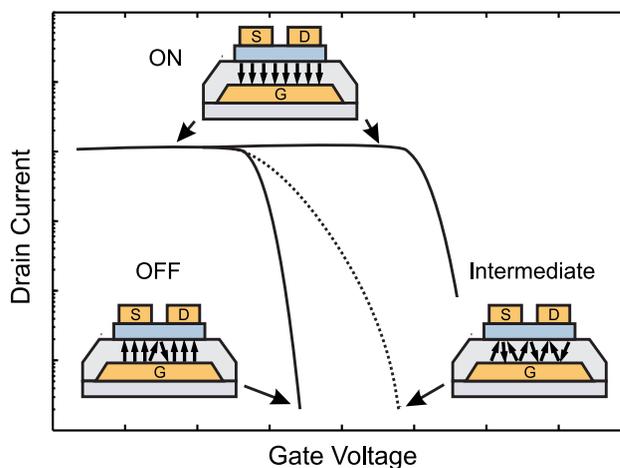


FIG. 4. Device operation of unipolar organic FeFETs in a staggered configuration. The ferroelectric polarization in the three possible states (ON, OFF, Intermediate) is shown. The arrows indicate at which point of the transfer characteristics the different states occur.

the ferroelectric causes the conductive channel to remain, even when the gate has been brought back to 0 V and leads to a positive $V_{\text{on,backward}}$.

In this paper, we provide evidence that three memory states can occur in staggered FeFET devices, due to the presence of a MSFM structure under both source/drain contacts. The detailed description of the memory states in coplanar FeFET devices needs further elaboration.

In summary, we have investigated the ferroelectric polarization state in MFSM structures and in FeFET devices using SKPM in conjunction with conventional electrical characterizations. FeFETs with a bottom gate—top contact architecture and pentacene as the semiconductor show three reprogrammable memory states: “OFF,” “Intermediate,” and “ON” state. SKPM measurements have shown that the ferroelectric layer in the channel region of the FeFET is not fully polarized in the “OFF” and “Intermediate” states. The polarization state of the ferroelectric underneath the source/drain contacts are responsible for the different injection properties of the contacts, explaining the different $V_{\text{on,forward}}$ in the “OFF” and “Intermediate” case.

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