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An intermediate frequency (IF) band digitizing radiometer system in the 100–200 GHz frequency range has been developed for Tokamak diagnostics and control, and other fields of research which require a high flexibility in frequency resolution combined with a large bandwidth and the retrieval of the full wave information of the mm-wave signals under investigation. The system is based on directly digitizing the IF band after down conversion. The enabling technology consists of a fast multi-giga sample analog to digital converter that has recently become available. Field programmable gate arrays (FPGA) are implemented to accomplish versatile real-time data analysis. A prototype system has been developed and tested and its performance has been compared with conventional electron cyclotron emission (ECE) spectrometer systems. On the TEXTOR Tokamak a proof of principle shows that ECE, together with high power injected and scattered radiation, becomes amenable to measurement by this device. In particular, its capability to measure the phase of coherent signals in the spectrum offers important advantages in diagnostics and control. One case developed in detail employs the FPGA in real-time fast Fourier transform (FFT) and additional signal processing. The major benefit of such a FFT-based system is the real-time trade-off that can be made between frequency and time resolution. For ECE diagnostics this corresponds to a flexible spatial resolution in the plasma, with potential application in smart sensing of plasma instabilities such as the neoclassical tearing mode (NTM) and sawtooth instabilities. The flexible resolution would allow for the measurement of the full mode content of plasma instabilities contained within the system bandwidth. © *2011 American Institute of Physics*. [doi:10.1063/1.3594101]

I. INTRODUCTION

In a Tokamak, a device for nuclear fusion research, high temperature plasma is confined by magnetic fields, which form nested toroidal magnetic flux surfaces,[1] characterised by their magnetic winding number q. Fusion performance limiting instabilities, such as the magneto-hydrodynamic (MHD) neoclassical tearing modes (NTMs),[2–5] occur at surfaces with simple rational q values such as 2/1 and 3/2. These NTMs create magnetic islands through the breaking and reconnection of magnetic field lines on either side of the resonant surface, leading to a flattening of the pressure profile across the magnetic islands[6] and hence a loss in plasma performance. One standard diagnostics method in Tokamak research is the measurement of electron cyclotron emission (ECE). The ECE spectrum is generated throughout the plasma volume, its frequency being characterized by the spatially varying magnetic field typically in the 100–200 GHz frequency range. The amplitude and frequency of the emissions yield information on the electron temperature and its spatial distribution, respectively, within the plasma. ECE diagnostics has been applied in MHD studies, electron kinetics and scattering, transport studies, and tearing-mode control.

Conventional ECE systems[7] consist of a radiometer where a broad radio frequency (RF) band, typically 20 GHz around a central frequency of 100–170 GHz, is down converted to an intermediate frequency (IF) band. This band is then split into a number of channels that are fed into a filter bank (or a series of multiple down convertor stages with the same bandpass filters) covering the IF range at a fixed frequency resolution, typically 0.5 1 GHz. Subsequently, the power content of the signals is detected by diodes connected to video amplifiers and digitized by analog-digital converters (ADCs) that are relatively slow, ~10 Msample/s.

The recent development of fast multi-giga sample (Gs) ADCs has enabled the development of ECE radiometer systems without the need for video detectors and amplifiers. The measured RF-signals are heterodyne down converted to the IF-band, which is divided into only a few sub-bands by secondary down convertor stages with wideband filters. Subsequently, the signal is fed directly into high bandwidth, typically >4 GHz, multi-giga sample ADCs exceeding 8 Gs/s

sampling rate. Connected to a signal processor through a fast interface, the signal is processed in real-time using field programmable gate arrays (FPGAs).

A clear advantage offered by a direct IF-band digitized ECE spectrometer system is the trade-off that can be made between spatial and temporal resolution, which can be optimized. Real-time ECE systems, coupled to soft- or hardware-fast Fourier transform (FFT) (Refs. 8 and 9) can also be employed as sensors for feedback control of Tokamak instabilities such as NTMs and sawteeth.[10] In contrast with conventional ECE systems, direct digitized radiometers measure the full wave information, including power and phase. Although phase information in typical ECE measurements is not used, a number of applications exist, see Ref. 11, where phase measurements are essential in understanding the physics of the coherent wave phenomena observed.

In this paper, we describe the novel direct IF-band digitized radiometer system equipped with back-end real-time data processing. It is applied to ECE diagnostics and real-time Tokamak control. The system is designed to cover the high dynamic range required for the measurement of coherent high power radiation injected and scattered as well as low power ECE radiation emitted, while achieving low thermal noise in the electron temperature measurement. Special emphasis is placed on the real-time calculation of frequency spectra at flexible, discrete time intervals using a FFT. The time interval taken for the FFT determines the flexibility in frequency resolution. This flexibility is not offered by a conventional ECE system, where the IF frequency signal is split into a number of frequency bands at fixed frequency resolution.

Direct digitized FFT radiometers can find application in other fields of research, including astrophysics[12–14] and earth observation[15–17] using molecular spectroscopy for the measurement of interstellar clouds, atmospheric composition, and molecular dynamics. It is also applied in the frequency spectrum measurement system of a high power free electron maser.[8]

The paper is structured as follows: Sec. II provides the theoretical basis for the performance of the FFT-based direct IF-band digitized ECE system in comparison with a classical radiometer system. The requirements for the Tokamak experiments ASDEX-Upgrade (AUG) and ITER are derived. In Sec. III, the design concept is presented of a wide spatial range, real-time hardware-FFT ECE system with variable spatial and temporal resolution. In Sec. IV, a proof of principle is given on the TEXTOR Tokamak by a software FFT radiometer system, including demonstration of the phase measurement capability. Section V discusses, summarizes, and concludes the paper. In the Appendix, details are presented of the hardware FFT system employing FPGAs.

II. THEORY AND SYSTEM REQUIREMENTS FOR A FFT-BASED REAL-TIME ECE SYSTEM FOR ASDEX AND ITER

In this section, the theoretical properties of directly digitized radiometers with FFT back-end are derived. Specific features of the FFT software and hardware implementation are discussed. From this analysis the system performance can be expressed in terms of total bandwidth, maximum spatial resolution, thermal noise suppression, and time resolution. Requirements for direct IF-band digitized systems for ASDEX Upgrade and ITER are then specified.

A. Theoretical derivation of system performance

Consider the cascade noise equation of Friis[7,18] applied to a radiometer for ECE measurements. The total equivalent noise temperature T_{total} of an ECE measurement is the sum of the thermal noise of the plasma electrons T_e and the noise temperature T_s of the ECE diagnostic itself[19]: $T_{total} = T_e + T_S$. Ideally, the thermal noise of the electrons is dominating over all other noise sources.

The radiometer system is preceded by antennas and waveguides, and these components also need to be taken into account when assessing the overall noise temperature. Thus, T_s for our system is calculated by applying the derived cascade noise equation $T_S = (L_{wg} - 1)T_0 + L_{wg}T_R$, where L_{wg} is the loss in the transmission line (waveguides and antennas) in dB, T_0 the temperature of the waveguides and T_R the equivalent noise temperature of the radiometer. Hence, the total noise temperature of the system including plasma becomes

$$T_{total} = T_e + (L_{wg} - 1)T_0 + L_{wg}T_R. \tag{1}$$

The radiometer equation used to optimize the sensitivity of the diagnostics and to optimize the minimum detectable power,[7,20] $P_{\min}$ is

$$P_{\min} = k_B B T_{total}\sqrt{\frac{2B_{vid}}{B_{\mathrm{IF}}}} \text{ with } \sqrt{\frac{2B_{vid}}{B_{\mathrm{IF}}}} = \frac{\Delta T_{\mathrm{ECE}}}{T_{av\ \mathrm{ECE}}}. \tag{2}$$

This equation expresses the minimum detectable power of a classical ECE system observing the plasma. Here, k_B is the Boltzmann constant, B is the input bandwidth, B_{vid} is the video bandwidth of the radiometer, and B_{IF} is the IF bandwidth of the radiometer (B_{IF} is equal to B if a single sideband receiver configuration is used). The statistical variation in the thermal and wave noise is expressed by ΔT_{ECE}. System design implies choices to be made for B_{vid} and B_{IF}, which leads to typical values $\Delta T_{\mathrm{ECE}}/T_{av\ \mathrm{ECE}}$ of a few percent.

Note that each component in the receiver is frequency dependent, and therefore each channel of the radiometer has its own noise temperature (T_n).

The FFT is accomplished by digital signal processing (DSP), either in software or by hardware implementations:

(1) *Software*: The ADC is connected by an interface chip to a fast bus of a computer, where the operating system runs software to perform FFT and post-processing.This method requires much effort for real-time control, since the bus speed forms a bottleneck in the amount of data, which is sampled during $\tau_{sampling}$. This means the idling time, $\tau_{idle} > 0$ has to be used to reduce the data (blockwise data acquisition), see Sec. IV, where such system is implemented and tested on TEXTOR.

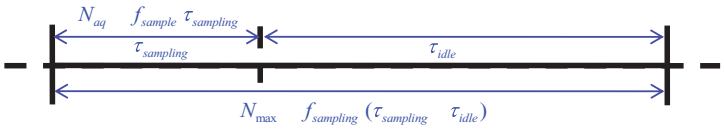

FIG. 1. (Color online) Timing diagram of typical block-wise ADC sampling.

(2) *Hardware*: The ADC chip is directly connected to a dedicated integrated circuit (IC), such as a FPGA or programmable dedicated DSP chip, which performs a real-time FFT with continuous data acquisition ($\tau_{idle} = 0$), and post-processing. This most promising approach is described in detail in Sec. III.

In both cases, additional continuous post-processing is necessary in order to achieve the required time and frequency resolution and to reduce the thermal wave noise ratio. It is also needed for the reduction of data, such that these output spectra, as a function of time, can be fed into a real-time control system[12] or a data storage system.

The time diagram of a typical sample sequence is shown in Fig. 1. Post-processing can be used either to optimize the overall signal content by summing the signals of n_{IF} frequencies in one spectrum or by averaging n_{vid} spectra at different time intervals. This renders the system superior flexibility over conventional systems. In the software FFT method, the idle time $\tau_{idle} > 0$, therefore, only the summing of frequencies applies. In contrast, the hardware implementation, in which $\tau_{idle} = 0$, allows for all post-processing tools to be used. The hardware FFT implementation is, therefore, the most promising approach for real-time plasma diagnostic and control.[21]

The video bandwidth is derived from the Nyquist criterion for $\tau_{sampling}$ and the spectral resolution Δf. The spectral resolution of the FFT is a function of the ADC sample frequency $f_{sampling}$ and the number of time domain samples N_{aq}.[22,23]

In FFT practice, some of the power in one frequency bin "leaks" into other frequency bin. This effect is called spectral leakage[22] and can be limited by applying a window on the time domain signal. Several shapes of windows are available. W is the equivalent noise bandwidth in bins[30] for a specific window on the time domain data before applying the FFT. W is a measure for the power leaked to the neighboring bins as a consequence of the applied FFT window. In case of no window applied $W = 1$. The video bandwidth B_{vid} and the IF bandwidth B_{IF} becomes

$$B_{vid} = \frac{1}{2\, n_{vid}\, \tau_{sampling}} \text{ and } B_{\mathrm{IF}} \geq \Delta f = \frac{f_{sampling}}{N_{aq}}$$
$$\rightarrow B_{\mathrm{IF}} = (W + n_{\mathrm{IF}} - 1)\ \Delta f. \tag{3}$$

In order to increase the signal-to-noise ratio (SNR) and reduce the fluctuation on the temperatures measured, the two alternative approaches can be followed, as mentioned above: the intensities on n_{IF} frequencies can be summed into one spectrum or n_{vid} intensities of multiple spectra can be averaged. The number of samples in the frequency domain can be calculated from the time domain sample size, and hence N_{aq},

$$N_f = \frac{1}{2} N_{aq} + 1. \tag{4}$$

From Eqs. (2) and (3), the minimal detectable power and the relative fluctuation on the ECE temperature can be derived

$$P_{\min\ \mathrm{FFT\,ECE}} = \frac{k_B\, f_{sample}\, T_{sys} \sqrt{W + n_{\mathrm{IF}} - 1}}{N_{aq} \sqrt{n_{vid}}}$$
$$\text{and } \frac{\Delta T_{\mathrm{ECE}}}{T_{av\ \mathrm{ECE}}} = \frac{1}{\sqrt{(W + n_{\mathrm{IF}} - 1)\, n_{vid}}}. \tag{5}$$

In order to compare the minimum power detected by a classical and a software FFT ECE system, it can be shown that

$$\frac{P_{\min\ \mathrm{FFT\,ECE}}}{P_{\min\ conv\ \mathrm{ECE}}} = \sqrt{\frac{\tau_{sampling} + \tau_{idle}}{\tau_{sampling}}} = \sqrt{\frac{N_{\max}}{N_{aq}}}. \tag{6}$$

It follows that, if the FFT radiometer can be designed in hardware, such that continuous acquisition ($\tau_{idle} = 0$) is possible than $N_{aq} = N_{\max}$ and therefore this ratio will be unity.

Now, the overall SNR of the combined system of digitizer and hardware FFT can be considered. The maximal signal-to-noise ratio or dynamic range (in dB) for an ideal digitizer, with effective number of bits N_b, bits can be calculated according to[22,23]:

$$\mathrm{SNR}\,(f) = 6.02 N_b\,(f) + 1.76\ \mathrm{dB} + 10 \log \frac{N_{aq}}{2}. \tag{7}$$

The latter part is the process gain depending on the block size during the FFT process. This equation is valid only for (sine wave) signals well within the bandwidth of the system, i.e., in the flat frequency response region of the ADC. However, for wideband ECE systems measuring thermal emission signals this equation has its limitations. In this case, the effective number of bits N_b is a frequency dependent value specified over a few frequencies by the manufacturer of the ADC. In order to calculate the complete frequency dependent signal-to-noise behavior of the ADC, the alternative equation[23] has been used. Additionally, the dynamical gain has been included leading to

$$\mathrm{SNR}\,(f) = 10 \log \left\{ \frac{3\,(2^{2b})}{2 + 3(2^b 2\pi f \sigma)^2} \frac{N_{aq}}{2} \right\}, \tag{8}$$

where b is the frequency independent, maximum effective number of bits at DC. The σ is presumed the RMS value sampling window jitter time (under the assumption that the jitter has a normal distribution with zero mean and a variance of σ^2). In Sec. IV, this equation is fitted for different block

sizes to the available frequency dependent values of the SNR obtained from the FFT of the time domain signal to derive b and σ.

In the formulas for the SNR, also the summing of intensities on frequencies in one spectrum (n_{IF}) and the averaging of intensities at multiple spectra (n_{vid}), must be included:

$$\mathrm{SNR}_{total}(f) = \mathrm{SNR}(f) + 5\log(n_{vid}\ (W + n_{\mathrm{IF}} - 1)). \tag{9}$$

This formula is valid if the ECE spectral components are larger than the product $n_{\mathrm{IF}}\ \Delta f$. Given formulas (7) and (9), doubling the size of the FFT will gain 3 dB dynamic range, while doubling the number of samples to be averaged, or the number of frequencies to be summed, will only gain 1.5 dB dynamic range. Knowing the SNR range of the ADC and the clipping power P_{clip} in dBm, one can calculate the minimum detectable power of the ADC (in milli-watt), $P_{\mathrm{min\ ADC}}(f) = 10^{(P_{clip} - \mathrm{SNR}_{total}(f))/10}$, which can be used to calculate the noise temperature of the ADC T_{ADC},

$$T_{\mathrm{ADC}}(f) = \frac{P_{\mathrm{min\ ADC}}(f)}{1000\ k_B B}. \tag{10}$$

This expression is used to calculate the system noise temperature, T_s, of the cascade noise equation of Friis[7,18] and the total noise temperature T_{total} and minimum detectable power P_{min} using Eqs. (1) and (2).

B. Requirements on ECE systems to obtain a large spatial range and high resolution

The present status of the electron cyclotron resonance heating (ECRH)-system design for ITER is described in Ref. 24. The aspect ratio of ITER (~3.1) is similar to AUG (3.2–3.3). The main differences between AUG and ITER are, first, the ITER magnetic field strength, which is about twice as high (5.3 T) as for AUG and will be constant because of the use of superconducting coils. Second, the ITER dimensions are about four times larger (minor radius 200 cm, major radius 620 cm). Thus the resulting toroidal magnetic field gradient, relevant to range and resolution of the ECE radiometer, is weaker by about half. Third, unlike AUG, the ITER EC power is injected at the fundamental cyclotron harmonic frequency, rather than the second harmonic mode, further reducing spatial resolution. Finally, the geometry of the ITER ECRH upper launcher differs from AUG in that power is injected from the upper port at a toroidal angle of ~20°, rather than equatorially at a near-perpendicular angle.

In order to set the spatial requirements for an Electron Cyclotron Current Drive (ECCD)-aligned ECE diagnostic[19] for NTM feedback purposes on AUG,[25] the requirements for positional accuracy, resolution, and range of the magnetic islands to be diagnosed need to be translated into the ECE frequency domain. The minor radius of AUG is ~0.45 m; the major radius is 1.65 m. The maximum magnetic field strength is 3.1 T. For AUG experiments on NTM control, the 140 GHz ECCD resonance condition is typically met on the high field side at a normalized flux coordinate of ~0.7. The full-width ECCD power deposition profile is ~0.7 cm, which is very similar in size to the minimum island size that has to be stabilized. The requirement on accuracy and resolution is, therefore, set to 0.7 cm, which corresponds to ~0.015 in normalized radial coordinate (or flux coordinate). A series of beam-tracing calculations for typical conditions of AUG show that the spatial requirement is met at an electron cyclotron frequency resolution equal or better than 0.7 GHz. In order to cover ~20 cm range in plasma minor radius, a frequency range of the order of 20 GHz should be adequate. Thus, the requirements on the ECCD-aligned ECE diagnostic includes a total of 29 data channels with 0.7 GHz separation centered around the ECCD frequency of 140 GHz.

Similar to AUG, the ITER EC resonance condition is met on the high field side. Targeting the NTMs occurring at the q = 2 and q = 3/2 flux surfaces, with normalized poloidal flux coordinate ranging from $0.65 < \rho < 0.93$, the launcher needs to be steered to cover this range, as variation of the magnetic field strength is not possible during an ITER discharge. The full width of the ITER EC power deposition profile projected on flux surfaces at the resonance plane is calculated to vary from 2 to 4 cm. Positional accuracy of half the beam size of 2 cm corresponds to ~0.01 flux coordinate variation.

The required frequency resolution Δf of the ECE radiometer can be expressed in terms of required spatial resolution ΔR, in first order approximation, neglecting the corrections for the non-equatorial launch geometry. This leads to the simple relation $\Delta f / n_{fce} \approx \Delta R / R_0$, where n_{fce} is the nth harmonic electron cyclotron frequency at the plasma major radius R_0 and R is the radius of the relevant q surface. A frequency resolution of 1 GHz corresponds to spatial resolution of 2.8 cm in ITER, which is just marginal for the purpose of feedback control. Therefore, 330 MHz frequency resolution is chosen which corresponds to about a tenth of an island size. A 20 GHz bandwidth corresponds to a spatial range of ~60 cm, which is hardly sufficient to span the range in major R between the q = 1 and q = 2 surfaces at the intersection point with the ECCD-beam. Therefore, the specification of the ITER ECE radiometer calls for a frequency resolution of less than 1 GHz, e.g., 330 MHz, and a frequency range of about 40 GHz centered around the ECCD frequency of 170 GHz. The typical rotation speeds of NTMs for ASDEX and ITER vary from 0 to 5 kHz and from 0 to 2 kHz, respectively. It takes about ten rotations for an appreciable change in the rotation frequency to occur.

It must be noted that these radiometer signals do not necessarily represent the actual electron temperature excursions due to the formation of NTM islands, since effects from nonthermal electrons can distort the simple proportionality between ECE-signal and electron temperature. However, along the same optical path absorption and emission profiles are affected in identical ways (as long as inhomogeneity over the absorption length remains small).

The signal-to-noise requirements for targeting the NTMs, occurring at the q = 2 and q = 3/2 flux surfaces, with normalized poloidal flux coordinate ranging from $0.65 < \rho < 0.93$, give electron temperatures which, can vary from about 0.3 to 1.5 keV for ASDEX and from 4 to 15 keV for ITER.

TABLE I. Desired system requirements of ECE systems for ASDEX and ITER.

- At least a bandwidth of 20 GHz, respectively, 40 GHz, centered around 140 GHz for ASDEX and 170 GHz for ITER, the latter with a frequency resolution of at least 330 MHz (~1/10 size of an island).
- Dynamically adjustable time and frequency (spatial) resolution to accommodate island rotation speed and size within 10 island rotation periods.
- Capable of suppression of plasma temperature fluctuations to 1%.
- Capable of producing 20 000 (ITER) to 50 000 (ASDEX) spectra per second, representing a realistic rate for multiple real-time measurements during one island rotation.
- Noise temperature few orders of magnitude lower than the minimum plasma temperature for measuring ECE and a sufficient dynamic range to measure simultaneously ECE and ECRH-scattering signals different by seven orders of magnitude.

Recently, sampling data at ultra-high speeds has become feasible through the application of modern CMOS technology. Chips capable of sampling >20 Gs/s are now being developed and produced by various manufacturers.[26,27] As shown in Sec. IV A, currently state-of-art processors are incapable of handling >20 Gs/s ADC data in real-time by software FFT, due to processor architecture. This allows implementation of the direct IF-band digitizing radiometer system with hardware DSP, simplifying the design. Next Sec. III will talk about the design and properties of such a system, aiming at desired requirements. In Table I a summary of the desired system requirements is listed for both ASDEX and ITER.

III. REAL-TIME, CONTINUOUS SAMPLING HARDWARE FFT-BASED ECE SYSTEM LAYOUT FOR ASDEX AND ITER

In this section, the design for a direct IF-band digitizing radiometer for ASDEX is presented with possible extension to ITER. This radiometer layout can also be used in other fields of research such as astrophysics, earth observation and molecular spectroscopy, and telecommunication. The software FFT system, as used on TEXTOR, is not suited for ASDEX and ITER for reasons of sampling idling time explained in Sec. II. Due to differences in ASDEX and ITER, modifications to the front end are required, notably the local oscillator (LO) frequency of the systems: 140 GHz for AUG and 170 GHz for ITER.

A. System definition of ultrafast processing setup

For 50 GHz bandwidth, the ADC must operate at a sample rate of at least at 100 GHz as the Nyquist criterion dictates. Since currently no ADC achieves this rate, multiple ADCs operating at lower frequencies are used instead. The proposed setup features four ADCs as used in 100 gigabit Ethernet diagnostics.[26,28] These ADCs have a sample rate of 56 Gs/s and an analog bandwidth of 14 GHz (−3 dB). This implies that we need four separate IF bands of 14 GHz, each having its own ADC and hardware processing. Note that also specialized 50 Gs/s ADCs exist[27] with a bandwidth exceeding 14 GHz, but presently they are not sensitive enough be-

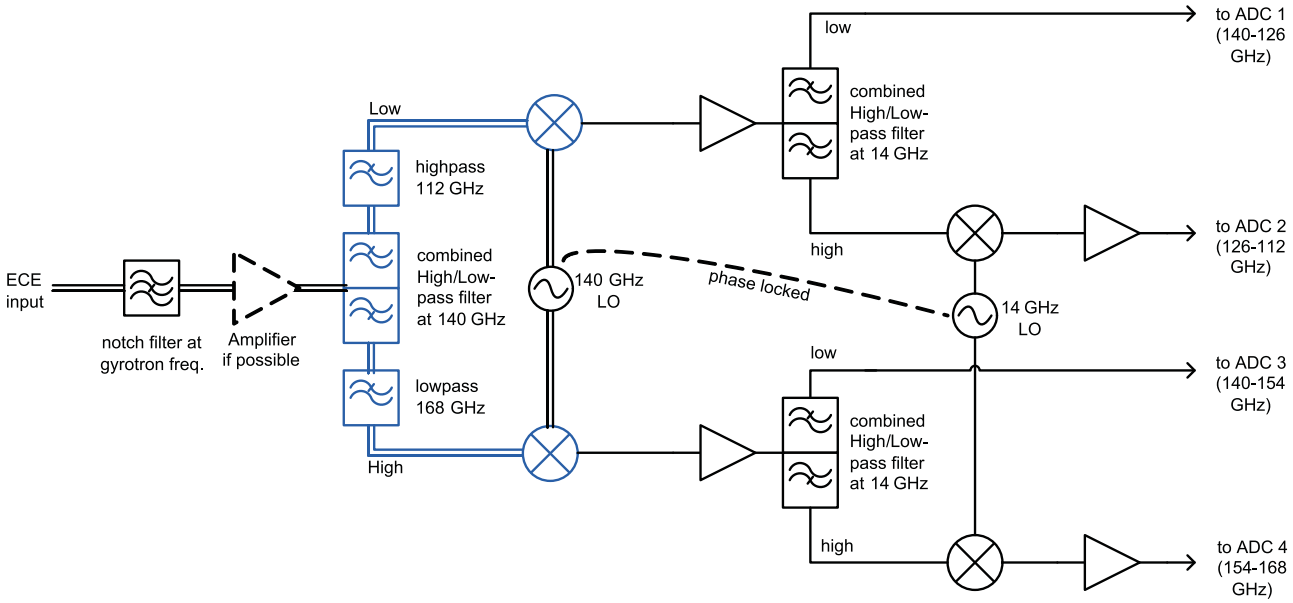

FIG. 2. (Color online) Principle of front-end RF setup: Following the signal from left to right, first the signal is filtered by a notch filter and a combined high-low pass filter, which splits the signal into two parts above and below the LO frequency. A mixer then down-converts these signals to the IF range of 0–28 GHz. The frequency band of the lower frequency signal is now reversed. The signal is then amplified by a broadband amplifier and again filtered and split at 14 GHz. The band of 14–28 GHz is then down-converted to 0–14 GHz. A subsequent amplifier is used to correct the mixer loss to the ADC input level. As an alternative to the RF filters and mixers, shown in blue, a sideband separating mixer configuration (Ref. 29) may be employed.

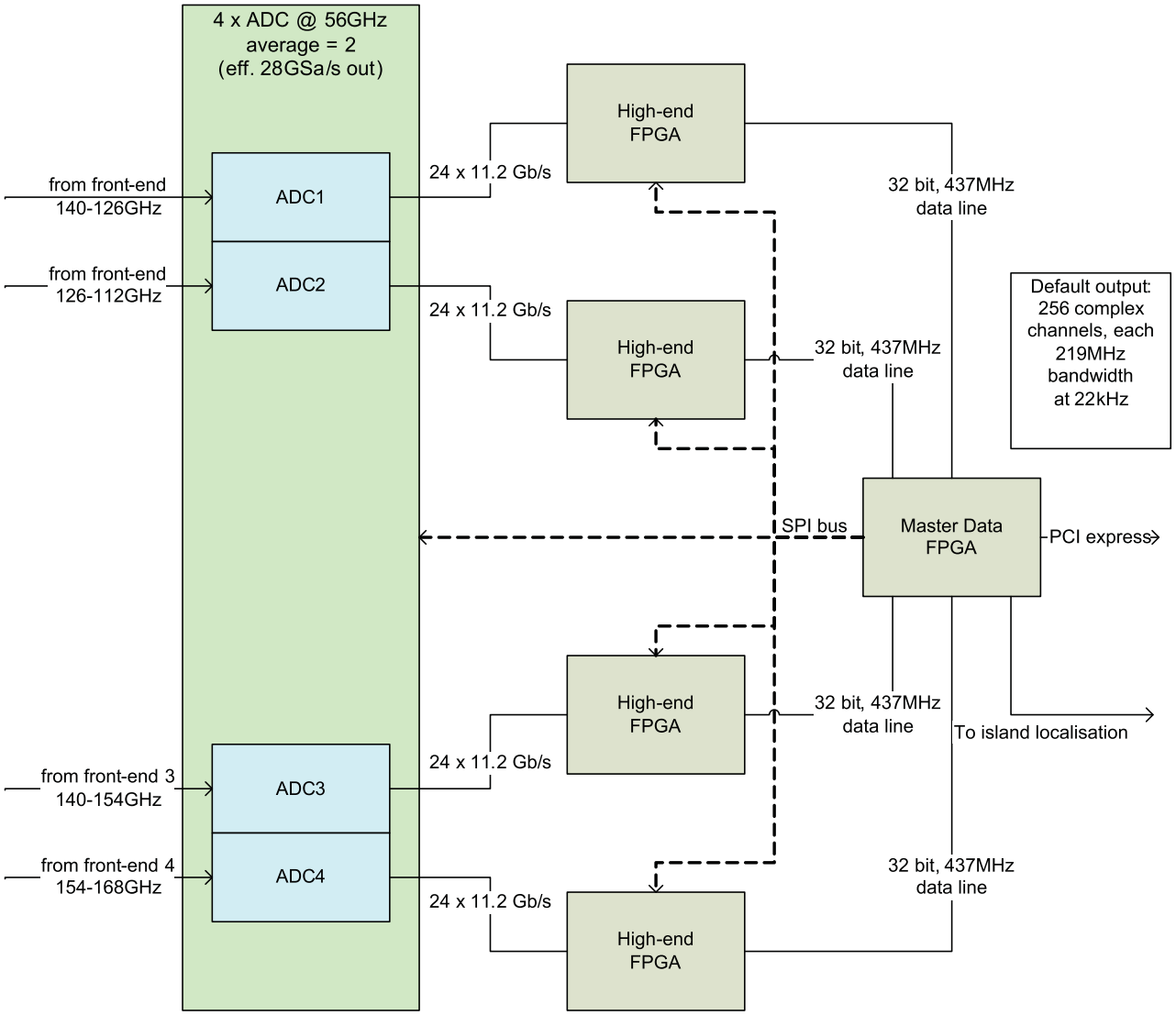

FIG. 3. (Color online) Processing back-end for hardware FFT, composed of four very fast ADCs with FPGAs.

cause of the lower effective number of bits than ADCs with a somewhat lower input bandwidth in standard commercial applications.

1. Front-end setup

Filters and mixers are required to down-convert the signal centered around 140 GHz and 170 GHz into the 4 IF bands of 14 GHz. The proposed setup is shown in Fig. 2. This setup has less signal loss and is less expensive than a conventional setup including four mixers and filters. Combined high-low pass sideband filters are proposed which do not have the −3 dB loss associated with normal splitters. Alternatively, the RF filters and mixers can also be replaced by a sideband separating mixer configuration.[29]

A single high frequency local oscillator is used to avoid the use of harmonic mixers with high conversion loss. Subject to the application, an attenuated signal of the gyrotron source for ECRH could be used as a LO. This has the advantage that the resonance frequencies will have fixed offsets in the resulting FFTs relative to the ECRH frequency. However, the disadvantage is that the frequency bins produced by the FFT no longer have a fixed absolute frequency, and no signal can be measured without ECRH. Therefore, a dedicated phase locked 140 or 170 GHz LO is preferred.

2. Digitizers

The ADC solution[26] selected has on board DSP capabilities, one of which is a finite impulse response filter, which is applied as a cut-off filter at 14 GHz. After filtering, two subsequent samples are averaged. This improves the ADC signal-to-noise at a performance of 28 Gs/s without aliasing. The data are then transferred through a high-speed parallel bus into a FPGA.

3. FPGA Post processing

The proposed setup uses four digitizers at an effective output of 28 Gs/s. The samples have a size of 8 bits. Consequently, the resulting throughput is 112 GB/s. For this

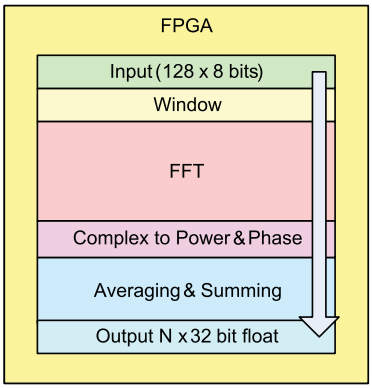

FIG. 4. (Color online) Processing sequence in FPGA for hardware FFT and signal reduction.

application, data need to be transformed into the frequency domain. Current development in FPGA technology allows for the implementation of a complete FFT algorithm on one chip. The algorithm will accept new transient data at each clock cycle and is therefore real-time.

In practice, the FFT circuit can only be produced using dedicated software to generate the hardware description, for example, using the very high-speed integrated circuit hardware description language (VHDL). The hardware description can then be compiled and transferred to the FPGA, see Fig. 3 for the proposed back-end solution using four FPGAs.

The ADCs are controlled by a clock at 437.5 MHz. By sharing the clock with the FPGAs the circuit can be designed to have 128 samples ready in the FPGA's buffer at each clock cycle. This implies that the system should be ready to accept and process this amount of data at each clock cycle in order not to lose idle time. Figure 4 shows the sequence of processing in the FPGA.

First, the window is applied to the input samples, see Sec. III A 4 for choice considerations. This takes one clock cycle for the 128 samples. When the samples have passed through a parallel FFT algorithm, this results in 65 complex spectral components running from 0 to 14 GHz. It is however possible to combine the output of two spectra into a double size spectrum as used in piped FFT algorithms. This step is repeated again, allowing to trade time resolution for frequency resolution. As noted in Sec. II A, it is always beneficial to have as much frequency resolution as possible, since time resolution is not the limiting factor. In the averaging and summing step, the frequency resolution can be reduced to the desired value. The output of this "hybrid" (combining parallel and piped methods) FFT will then consist of N frequency components.

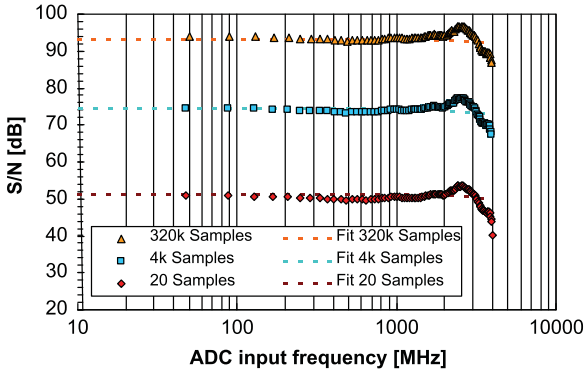

FIG. 5. (Color online) SNR (to average noise level) values as a function of frequency obtained from the FFT of the time domain signal for three different sample block sizes are shown. Fits to the data-set using Eq. (8) are presented by the dotted lines, for the maximum effective number of bits b and the RMS jitter time σ. Optimal fit is found by $b = 6.6$ and $\sigma = 0.2$ ps. For frequencies above 2 GHz, the aliasing filter in the ADC shows a rise, which is not reflected in Eq. (8). The bandwidth (−3 dB) of this ADC is about 3.5 GHz.

The third step is to convert the complex vectors into power and phase. By directly converting to power (watt) no square root is required. For phase retrieval, a two-dimensional lookup table should suffice, giving a rounding error depending on the amplitude.

The last step consists of averaging and summing. Here, time and frequency resolution can be traded for better SNR. Averaging spectral components and adding frequency bins together is a trivial step in the FPGA. The steps above are discussed more in depth in the Appendix. Section III B discusses the resulting properties of this system, and how changing the frequency and time resolution affects the signal quality.

4. Time domain window to suppress signal leakage and spurious signals

Before the FFT, a window is applied on the time domain data to remove unwanted spectral components.[30] The criteria for window selection in this application are as follows:

- Low side lobe level and high side lobe roll off for low spectral leakage and a high sensitivity of the radiometer.
- Minimal scalloping loss for precise spectral measurements in order to achieve high amplitude accuracy (frequency-bin amplitude variation) over the entire spectral range.
- High frequency resolution: at one frequency the power and phase signal should preferably not be divided over more bins than are summed by the post processing.

Given these criteria and the requirements derived in Sec. II B, for 256 spectral bins a five-term cosine window has been selected.[31] This yields optimal choice for frequency resolution and scalloping loss. This window has an equivalent noise bandwidth of 2.21 bins, a scalloping loss of 0.68 dB, and a side lobe level of −125 dB. At ECE signal levels it means that the side lobes do not contribute to the level of the noise floor of the receiver.

B. Expected system properties

The system as defined provides a total ECE bandwidth of 56 GHz (4 × 14 GHz). Other system properties including dynamic range, temperature fluctuation, and output spectra per second are presented in Table II. The system's maximum frequency resolution is 54.7 MHz (effectively, 120.3 MHz due to choice of window). This is about three times higher than required. Given a statistical variation in the thermal and wave

TABLE II. Performance of the FPGA FFT system with a constant sample rate of 28 Gs/s. The native sample rate of ADC is 56 GHz, averaging two consecutive samples, increasing the dynamic range by 1.5 dB without idle time. The time domain samples are fixed at 512 samples and the ECE characteristics are calculated from these measurements by Eqs. (2) and (3). Better temperature fluctuation suppression can be obtained by optimization against frequency resolution. The ECE temperature fluctuation has a minimal frequency resolution $B_{IF} = 120.3$ MHz. Note that the performance of this system is equal to a conventional ECE system but with more flexibility in frequency resolution.

Constants								
Samplerate [GHz]			28		Window type		5-Term cos	
Time domain samples			512		Bytes per freq. comp.		4	
Frequency bins per spectra			256		Effective Nr. of Bits		5.3	
Spectrum Acq. time [us]			18.3		Sample time [ps]		35.7	
Spectra to average	Output spectra frequency [Hz]	B_{vid} [kHz]	Dynamic range [dB] $B_{IF} = 120.3$ MHz	$\frac{\Delta T_{ECE}}{T_{av\ ECE}}$ $B_{IF} = 120.3$ MHz	Data transfer [MB/s] $B_{IF} = 120.3$ MHz	Dynamic range [dB] $B_{IF} = 339.1$ MHz	$\frac{\Delta T_{ECE}}{T_{av\ ECE}}$ $B_{IF} = 339.1$ MHz	Data transfer [MB/s] $B_{IF} = 339.1$ MHz
1[a]	54 687 500[a]	27343.8[a]	57.7[a]	67.4%[a]	53,405.8[a]	61.2[a]	40.2%[a]	10,681.2[a]
7[a]	7 812 500[a]	3906.3[a]	62.0[a]	25.5%[a]	7,629.4[a]	65.5[a]	15.2%[a]	1,525.9[a]
14[a]	3 906 250[a]	1953.1[a]	63.5[a]	18.0%[a]	3,814.7[a]	67.0[a]	10.7%[a]	762.9[a]
68[a]	804 228[a]	402.1[a]	66.9[a]	8.2%[a]	785.4[a]	70.4[a]	4.9%[a]	157.1[a]
140	390 625	195.3	68.5	5.7%	381.5	72.0	3.4%	76.3
700	78 125	39.1	72.0	2.5%	76.3	75.5	1.5%	15.3
1,300	42 067	21.0	73.3	1.9%	41.1	76.8	1.1%	8.2
1,500	36 458	18.2	73.6	1.7%	35.6	77.1	1.0%	7.1
5,000	10 938	5.5	76.2	1.0%	10.7	79.7	0.6%	2.1

[a]The values are indicative and for comparison with Table III only (the associated relative statistical temperature variation is too high for practical use).

noise fluctuation ratio of 1%, one can monitor islands with a rotation frequency up to 18 kHz, a dynamic range of 76 dB and a B_{IF} of 339 MHz, which fulfills the initial requirements. Using these values, the front-end with realistic values for conversion losses, noise figures, and gains, as described in Fig. 2, the receiver system minimal detectable power becomes −95 dBm (or 0.6 eV). This calculation ignores the background noise of the plasma.

Preliminary measurements on CHAIS ADC technology[26] show no indication of spurious frequency components at the same levels as observed in Sec. IV A, see Fig. 6.

C. Conclusions

A novel hardware FFT ECE system with direct IF-band digitization has been designed with state-of-the-art technology and verified by simulations. The system features are as follows:

- Multiple front-end systems, fitting the bandwidth of the four ADCs. These front-ends are simple, economic, and minimize losses by efficient use of special components such as an additional filter/splitter combination and sharing of local oscillators.
- Better performance compared with software FFT systems because the system measures continuously without any idling loss.
- Variable time and frequency resolution, which is configurable at runtime in the FPGA.
- A dynamic range of 76 dB.
- Capturing the full wave information, including phase and amplitude.

The high dynamic range and the phase-detection capability render the system suitable for studies of coherent wave phenomena, see Sec. IV B 1, in addition to the ECE measurement, see Sec. IV B 2. The flexible time/spatial resolution would allow adaptive sensing for MHD control including the possibility of dynamic zoom on plasma position or event.

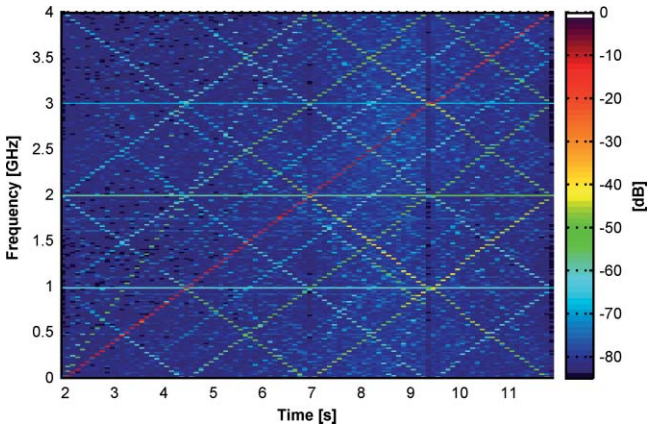

FIG. 6. (Color) Frequency sweep of generator, adjusted at −10 dBm power, connected to ADC. The spectrogram visualizes the level of spurious frequency components generated by the ADC. The sweep in red varies by +/− 5 dB around −10 dB level, depending on the frequency response of the ADC. Some harmonics of the signal generator are visible as starting from the origin (2 s, 0 GHz) in green (−50 dB) and blue (−70 dB) level. The maximum of the spurious level in yellow (−40 dB) is 30 dB lower than the source signal. This spectrum contains 16 0001 frequency domain samples from which 239 groups of 667 summed samples are computed.

TABLE III. Maximum retrigger rate measured against different time domain (block size) samples. Equations (2)–(6) are used to calculate the signal characteristics. The data transfer (Max. PCI bus = 0.5 GB/s) can be derived for the data and the measured timing. The statistical temperature fluctuation ratio is normalized to a fixed intermediate frequency resolution, in order to satisfy that $B_{IF} = 305$ MHz. The ratio between idling time and acquisition time has a direct relationship to the minimal detectable power and temperature fluctuation ratio (compared to a conventional ECE system). This system allows for detection of NTMs at 1 kHz with a noise ratio of 2%. Minimizing the idling time is the key factor in optimizing this system. The window function selected does not limit the dynamic range due to the side-lobe level (Refs. 30 and 31) (current level at −125 dB).

Time domain samples	Maximum retrigger frequency [Hz]	Data transfer [Msample/s]	Spectrum time [us]	Idle time [us]	B_{IF} [MHz]	B_{vid} [kHz]	Min. detect. power increase compared to conv. ECE [dB]	Dynamic range [dB] $B_{IF} = 305$ MHz	$\frac{\Delta T_{ECE}}{T_{av\ ECE}}$ $B_{IF} = 305$ MHz
100	11 000	2.10	0.013	90.9	176.000	40000.0	19.3	60.6	51.2%
500	10 500	10.01	0.063	95.2	35.200	8000.0	15.9	71.7	22.9%
1000	10 500	20.03	0.125	95.1	17.600	4000.0	14.4	76.3	16.2%
5000	8500	81.06	0.625	117.0	3.520	800.0	11.4	86.9	7.2%
10000	6500	123.98	1.250	152.6	1.760	400.0	10.5	91.4	5.1%
50 000	2700	257.49	6.250	364.1	0.352	80.0	8.9	101.9	2.3%
100 000	1500	286.10	12.500	654.2	0.176	40.0	8.6	106.4	1.6%
300 000	550	314.71	37.500	1 780.7	0.059	13.3	8.4	113.5	0.9%

IV. PROOF OF PRINCIPLE OF A FFT-BASED SYSTEM

A proof-of-principle employing a 4 GHz bandwidth direct IF-band digitizing radiometer system has been constructed and tested on TEXTOR featuring the key ingredients of the system described[9,21] but using software FFT instead of the hardware solution. In this software FFT system, the ADC is connected by a fast interface to a computer. The speed of the bus determines the maximum transfer rate of the data flow (commonly used cPCI ∼0.5 Gs/s). Consequently, in practice it is not feasible to have continuous data acquisition due to the large data flow of tens of giga samples (bytes) per second over the ADC output bus (cPCI). Therefore, sampling can only be accomplished through reduction of the data flow by fixed interval block-wise data acquisition during the sampling time, resulting in idling time (see Fig. 1). Even if the bus would be fast enough for real-time ADC data, memory transfer speeds, processor architecture, and real-time interrupt handling limitations, would make a constant throughput FFT system on a modern ×86 based system impractical. A computing unified device architecture (CUDA) system may be used to overcome some of these limitations.[35] However, using a non-real-time operating system handling of interrupts limits the performance of such a system (see Table III). This implies that a working implementation would also require a real-time operating system.

Because of the FFT no hardware video detection is used in the system, with conservation of signal frequency and phase. From the IF signal (in the time domain), frequency spectra at discrete time intervals can be obtained by software FFT. The data processing was carried out off-line after data storage.

A. ADC properties of software FFT system

The ADC, which is used has an equivalent sampling rate of 8 GHz. The ADC interleaves the samples of four 2 GHz ADCs into one signal. The ADCs are clocked such that each ADC is triggered in sequence. The ADCs have different amplifier settings. Sensitivity and offset calibration is done at application startup. Consider the effective number of bits and the RMS value sampling window jitter time for different FFT block sizes, given in Eq. (8) Sec. II A. These ADC parameters are obtained from the SNR measurements shown in Fig. 5. The dynamic range of >50 dB for block sizes >20 proves to be sufficient for ECE systems. For both measuring ECE and ECRH scattering an improved dynamic range >70 dB is required.

Table III shows the measured and calculated characteristics of the ADC. The suitability of this ADC for a direct digitizing radiometer is limited by the data output bus transfer rate, which limits the repetition rate of the software FFT. A saturation of the maximum retrigger rate is reached above 10 kHz, due to the non-real-time character of the used operating system (Windows XP, 32 bit), which cannot handle more interrupt calls per second. Using a real-time operating system, the maximum bus transfer speed will limit the temperature fluctuation ratio measured to ∼1% and at the same time detect rotation of the NTM islands in the plasma at frequencies in excess of 10 kHz (the desired retrigger rate is ∼100 kHz).

Other important aspects of the system performance that should be minimized are as follows:

- Non-linearity and high signal strength behavior (such as third order point interception).
- Aliasing and other spurious signals generated.

These aspects could be investigated by applying a clean signal with frequency-steps with spurious and harmonics suppressed lower than the dynamic range of the ADC. The frequency is stepped over the range from DC to half the sample frequency (see Fig. 6).

The FFT simulations have shown that timing offset jitter of ∼10% between the 2 Gs/s ADCs in combination with stepped frequency sweep of the source signal, cause the "Scottish Tartan" check pattern of the spurious frequency components. The offset differences between the ADCs generate constant 4 and 2 GHz signal. In addition, a 1 GHz spurious (clock) source signal causes the 3 GHz constant component in

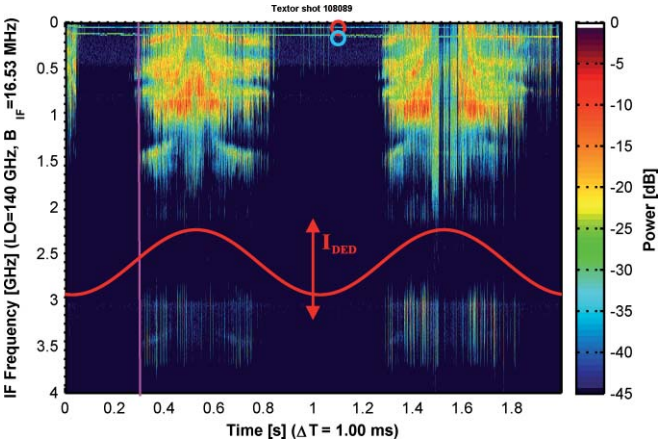

FIG. 7. (Color) Spectrogram of the direct IF-band digitizing radiometer with software FFT, showing scattered ECRH radiation. With the DED at TEXTOR a tearing mode was created and moved slowly back and forth across the ECRH beam: the symmetrical frequency change of the spectrum in time correlates completely with MHD. This spectrum contains 8001 frequency domain samples from which 242 groups of 33 summed samples are computed (remaining samples are discarded). The gyrotron frequency (~139.91 GHz) can be seen also around 87 MHz (red circle) and its second harmonic (blue circle) at 173 MHz. The purple vertical line indicates the time-point of the zoomed spectrogram shown in Fig. 9.

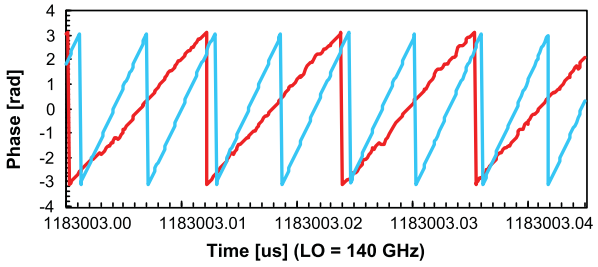

FIG. 8. (Color) Phase of first (red) and second (blue) harmonic gyrotron frequency (red) determined using a "sliding FFT" of 277 samples. Phase correlation is evident in this IF spectrum the gyrotron frequency is at 86.643 MHz, while the second harmonic is at 173.285 MHz. Using the "sliding FFT" technique phase correlations can be determined.

Fig. 6. Timing differences in the interleaved sampling ADC configurations cause inter-modulation between input signals. Offset errors in the different ADCs cause constant spurious frequencies related to the sample frequencies of the ADCs. In conclusion, the performance of this high dynamic range (>30 dB) receiver is limited by the interleaved sampling.

B. Tests on TEXTOR

The direct IF-band digitizing radiometer system with software FFT has been implemented on TEXTOR to detect ECE millimeter waves from the plasma and coherent signal components from the injected gyrotron power and the radiation resulting from the interaction of the gyrotron mm-wave beam power with the plasma. The system was mounted in the ECRH transmission line configuration, by the in-line principle.[19,32] The signals are heterodyne down-converted, amplified, and directly digitized using the fast 8 Gs/s ADC.

1. Coherent scattering

It has been reported that under some conditions anomalous scattering is observed of the ECRH mm-wave beam in TEXTOR (Refs. 9, 21, and 34) during line-of-sight measurements with electron cyclotron heating. The scattering seemingly originates from a rotating island, produced with variable current, I_{DED}, in the dynamic ergodic divertor (DED). The mechanism of the scattering is under debate.[11,34] The direct IF-band digitizing radiometer was tested by measuring the scattered power,[9,21] using the line-of-sight setup.[19,32] In Fig. 7, a measurement is presented showing bursts of radiation with different and chirping frequencies in the vicinity of the ECRH system frequency.

The dynamic range of the signals is as high as 40 dB including time-dependent chirps, which are related to details of the island location. In Fig. 7, the gyrotron frequency signal appears just below 0 GHz. An additional component is observed at slightly higher frequency. The two frequency components are indicated by the red and blue markers. The absolute phase of these two signals could be measured using a moving or sliding FFT (Ref. 33) and compared as shown in Fig. 8.

Note that the signal at a slightly higher frequency (blue circle) has exactly the double phase variation of the gyrotron

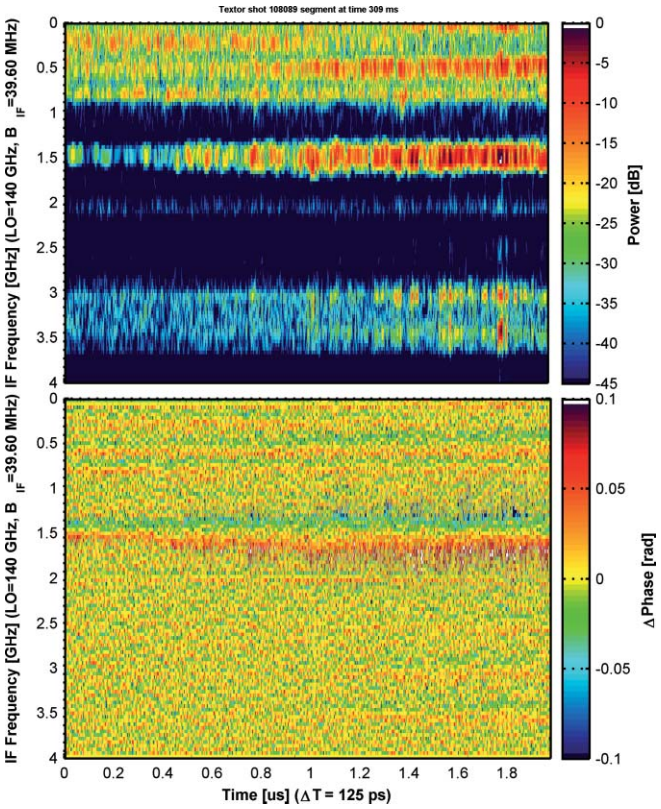

FIG. 9. (Color) Zoomed spectrogram of the direct IF-band digitizing radiometer with software FFT. The scattered ECRH radiation is given at the purple line in Fig. 7. The amplitude (top) and the phase (bottom) are shown. Fine-grained power and phase information can be extracted using a "sliding FFT" of 200 samples over one block of 16 000 time domain samples. On the phase measurement a normalization is done by subtracting the phase rotation over time for each frequency of the FFTs. In the phase plot the difference between the previous and the current FFT is plotted. At ECRH scattering phases clearly correlate with the intensity.

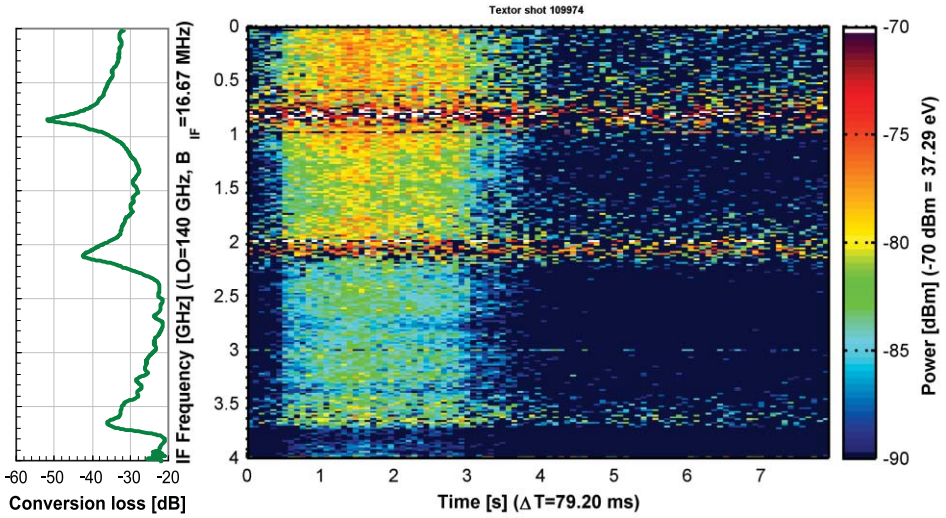

FIG. 10. (Color) ECE spectrogram as measured with the direct IF digitizing radiometer. The plasma pulse length was 2.5 s. The marginal signal quality is caused by the three maxima in conversion loss of the front-end's mixer (left) and the TEXTOR operational conditions. This spectrum contains 160 001 frequency domain samples from which 239 groups of 667 summed samples are computed to give a theoretical $\Delta T_{ECE}/T_{av\ \mathrm{ECE}}$ of 4%. Apart from these noisy signals, one can see that the ECE-intensity increases from the very edge of the plasma at $R = 1.29$ m (144 GHz at the bottom of the spectrogram) to $R = 1.34$ m (140 GHz at the top).

signal (red circle). Analysis shows that the exact frequency of the second signal stems from the mixing of the second harmonic of both the LO and the gyrotron in Fig. 7.

In conclusion, the direct IF-band digitizing radiometer enables phase measurements. This capability will be used to further investigate the scattered signal. In Fig. 9, a zoomed spectrogram of the scattered signal is presented. The timing of this data is indicated by the purple line in Fig. 7. The amplitude (top) and the phase (bottom) are shown. The phase plot is normalized by subtracting the phase variation over time for each frequency of the FFTs. The phase difference is plotted between the previous and the current FFT. It is evident that the scattered signal phase correlates with its intensity, showing that the signal has dominant coherent components.

2. Electron cyclotron emission

To increase the signal level for the ECE measurement, the transmission line was modified by removing 15 dB of attenuation.[21] With this modified setup measurements were carried out, see Fig. 10, in a standard TEXTOR plasma[9] without ECRH and a toroidal magnetic field at $R_0 = 1.75$ m of $B_t = 1.9$ T. Consequently, the ECE resonance conditions (140–144 GHz) are shifted to the high field side edge of the plasma, where the ECE emission is weak. A small part of outer edge of the temperature profile is measured. The values of the electron temperature T_e are compared by Thomson scattering (TS) diagnostic which measures T_e along a central vertical chord.[36] The TS data from the upper and lower plasma edges (~15 spatial points) were mapped to the high field side region and confirmed the electron temperature from the ECE measurement (not shown here). Phase analysis shows that in this case no coherent component can be found in the signal as expected.

C. Conclusion of direct IF-band digitizing radiometer system using software FFT

A novel direct IF-band digitizing radiometer has been developed and tested on TEXTOR as a proof-of-principle. Because of the software FFT solution, the system capabilities are limited by idling time. However, the feasibility of flexible time/spatial resolution, with optional dynamic zoom on certain plasma positions or events, has become feasible with a possible application to adaptive sensing for MHD control. The software FFT system tests reveal the following limitations:

- A saturation of maximum retrigger rate is reached slightly above 10 kHz, due to non-real-time character of the used operating system.
- The maximum bus transfer speed and interrupt handling of the OS will allow to reach the temperature fluctuation ratio of ~1% and at the same time detect rotation of the NTM islands in the plasma at frequencies above 275 Hz. However, this is at least one order of magnitude too low for control.
- Timing differences in interleaved sampling ADC configurations, in our case an ADC of 8 Gs composed from 4 ADCs of native 2 Gs, cause inter-modulation (or mixing) between input signals. Offset errors cause constant frequencies related to the sample frequencies of the ADCs. The spurious level is 30 dB lower than the source signal. This interleaved sampling is for high dynamic range (>30 dB) receivers a less preferred method. The spurious signal can be reduced by using ADCs with a higher native sample rate.

In spite of these limitations, we could demonstrate the following features:

- Variable time and frequency resolution.

- High dynamic range.
- Phase-measuring capability.
- Coherent scattering signals and incoherent ECE emission.

These results show that the development of real-time continuous sampling hardware FFT systems as presented in Sec. III will form the optimal solution.

V. DISCUSSION, SUMMARY, AND CONCLUSIONS

The underlying theory and system requirements of a real-time direct IF-band digitized ECE system for AUG and ITER are presented. It forms the basis of design for a new hardware based FFT system for direct real-time and continuous digitized measurement in the frequency range of 112–168 GHz and 142–198 GHz for ASDEX and ITER, respectively. This frequency range corresponds to ECRH&CD on these machines. The system is based on the fastest ADCs, currently under development, in combination with hardware FFT and other signal processing implemented in currently available high end FPGAs.

A proof of principle based on the software FFT system has been verified on TEXTOR. It is demonstrated that even under unfavorable conditions, ECE measurements can be carried out. The possibility of extracting phase information has been demonstrated. In addition, coherent scattered signals could be measured at high dynamic range.

For Tokamak MHD control purposes, the time required for acquisition and post-processing of the measurements is important, since this limits the overall response time of the control system. In a standard software implementation of the FFT, the desired repetition rate cannot be achieved because of idling time, which is a result of limitations on the bus speed and partially of interrupt handling.

To overcome these limiting factors in computer technology, a new hardware setup was chosen, which allows for flexible implementation of real-time analysis programs. Special emphasis is placed on the implementation of a FPGA based circuit for FFT. However, other implementations are possible such as wavelet analysis or a sliding FFT.

This FFT implementation contains a number of interesting features. First, the system allows for variable temporal and frequency resolution. This implies that in real-time the spatial resolution can be adapted to the conditions at hand. This is accomplished by using a system, which has multiple front-ends, each fitting the bandwidth of the respective direct IF-band digitizing ADC, minimizing losses by using special components. This hardware FFT system has no performance limitation compared to a conventional ECE system (no idling time) but is different from a conventional ECE system because it has variable time and frequency resolution, which is configurable at runtime in the FPGA. Furthermore, low power ECE emission measurements together with high power scattering, even with fast rotating islands (>5 kHz) and with multiple plasma modes combined, become amenable to measurement.

Another advantage is that the full wave information (amplitude and phase) remains contained in the system. This could have added value for a number of physics investigations.

- The scattering of ECRH wave as reported here;
- ion-electron interaction (collective Thomson scattering);
- parameterized instabilities;
- pulsed radar; and
- control oriented system-identification for plasma control.

This paper sets a new trend in direct IF-band digitized radiometer measurements systems including flexible time/spatial resolution by new technology enabled hardware FFT with application to adaptive (ECE) sensing for MHD control or other applications in science.

ACKNOWLEDGMENTS

We appreciate the collaboration with Fujitsu[26] and TiaLinx[27] for very fast ADC technology and like to acknowledge Chandra Ramaswany, Falk Pribbernow, (Fujitsu, Germany), Ian Dedic (Fujitsu, United Kingdom) Mehran Mokhtari, and Fred Mohamadi (TiaLinx, USA) for their hardware specification/test support of new technology ADCs. This work, supported by the European Communities under the contract of association between EURATOM-FOM, was carried out within the framework of the European Fusion Program. The views and opinions expressed herein do not necessarily reflect those of the European Commission.

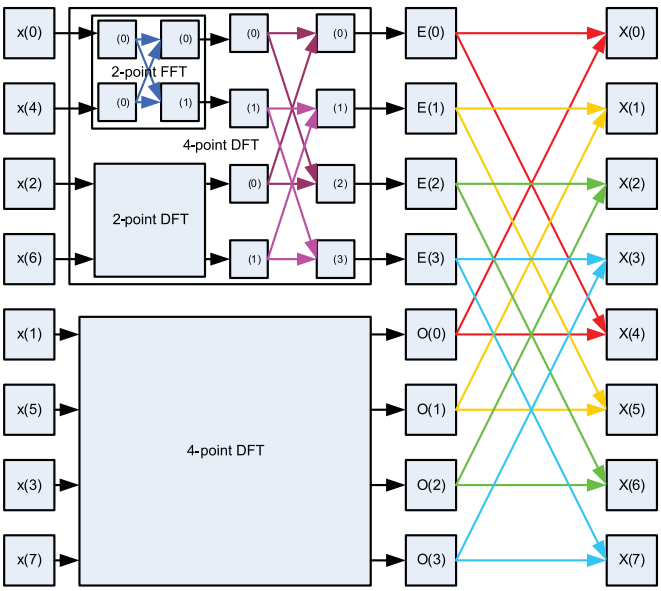

FIG. 11. (Color online) Parallel FFT transform flow diagram with eight samples, showing each nested level. For each level, one DFT box has been opened to show the inside. As seen from the figure basically each level of a FFT takes two spectra and merges them into one. It repeats this step for each stage, merging two $N/2$ spectra into one N sized spectra, by applying butterfly operations. For clarity each butterfly is shown in a different color.

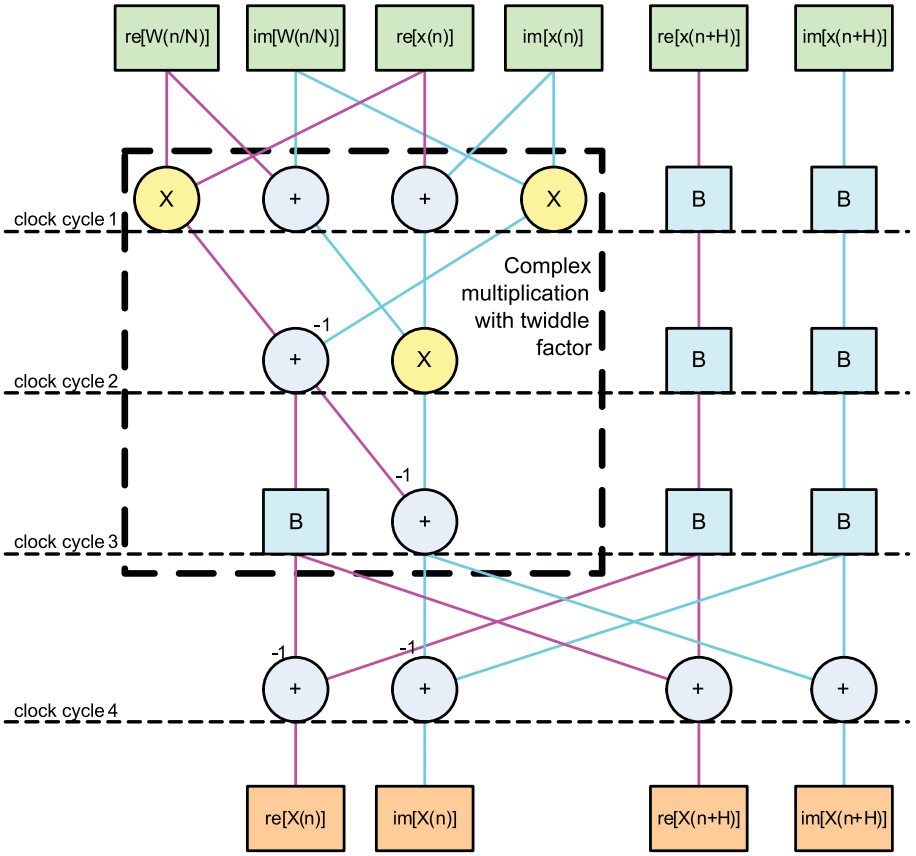

FIG. 12. (Color online) Butterfly in a FPGA. The inputs (boxes at the top) are: X(n) the input of the butterfly, W is the twiddle factor (Ref. 41), X(n) (partial) frequency domain output (boxes at the bottom). The multipliers (circles marked 'X') are DSP blocks. The boxes marked "B" are buffers, required for correct timing. The whole butterfly takes up three real number multiplications, four additions, and four subtractions.

APPENDIX: FFT SIGNAL PROCESSING ON FPGA

The implementation of the processing logic on the FPGA is presented in detail.

After receiving the 128 samples from the high-speed busses on the FPGA, the first step of the process is to apply the five-term cosine window, as discussed in Sec. III A 4. The output of an 8 bit ADC, in the range of −128–127, needs to be converted to 2 V_{pp} input range. To apply the window and the scaling in one step, the terms of the cosine window is scaled by$1/128$. From the cosine window, a template is created of 128 multiplications which can apply the window in one go using special DSP blocks present in modern FPGAs. This would allow for application of the window in one clock cycle. A small program is written to generate the template in VHDL code.

Figure 11, shows the FFT consisting of nested Discrete Fourier Transform (DFT) computations. In each nesting the output of two $N/2$ DFTs is combined into one N size DFT by the use of "butterflies," named after their shape.

The parallel architecture of FPGA is well suited for implementing FFTs. As noted in Sec. II A, it is beneficial to maximize the size of the FFT for maximum frequency resolution, since the time resolution increase is negligible, but allows for maximum dynamic range. State-of-art FPGAs (Refs. 37 and 38) contain around 3000 DSP blocks, which set the upper limit for the achievable frequency resolution, given a specific FFT implementation and additional processing. Therefore, the efficiency of the FFT needs to be maximized, by minimizing the multiplications per frequency component. These define the fundamental operation of a Fast Fourier Transform.[39] One butterfly is a two sample DFT, giving the spectral representation of these two samples. This is known as a radix-2 FFT algorithm, allowing a minimal spectrum of two samples. There are alternatives, such as the radix-4 and the split-radix.[40] Implementing these algorithms will be similar to steps discussed below. For simplicity the radix-2 will be further discussed.

The structure in Fig. 11 must be implemented on the FPGA. One butterfly requires one complex multiplication, an addition, and a subtraction. Although complex multiplication normally uses four real multiplications, in Fig. 12 a butterfly implementation is presented that uses only three multiplications. This is the implementation chosen, as this increases the number of possible butterfly multiplications by 25%. The whole process takes four clock cycles to complete. However, it also processes four spectra at the same time.

From Figs. 11 and 12, the formula for the number of DSP blocks can be derived as $3/2N\log^2(N)$, with N the number of elements in the input of the FFT. As it can be seen the maximum capacity of the FPGA is reached at input 256 samples, whereas 512 samples would require too many DSP blocks.

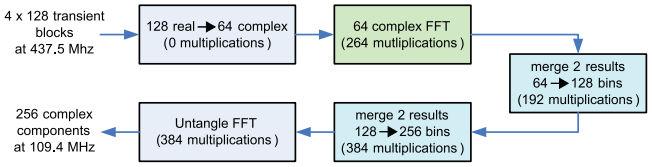

FIG. 13. (Color online) The 128 real values are entangled into 64 complex values. The parallel FFT (green box) transforms the 64 complex samples into 64 spectral components. The piped FFT (blue) takes these 64 components and waits for the next clock cycle. Then it combines the 2×64 components in one 128 complex spectrum. Each piped FFT step halves the output frequency. After the processing the results will need to be untangled.

To maximize the frequency resolution of the FPGA processing, the following optimizations will be used:

1. Using a real FFT instead of a complex FFT;
2. omitting obsolete multiplications; and
3. using a number of pipelined FFT steps after the normal (parallel) FFT.

These points will be addressed below.

1. The input consists of real-valued numbers only. Therefore, the computationally more efficient real-FFT can be used. Here, the odd indexed numbers are put in the imaginary part of the even index numbers,[22] the newly created 64 complex samples are fed into a normal complex FFT, and afterwards the output needs to be untangled requiring an additional pass of butterflies.

2. Many of the twiddle factors are either 1, $1j$, or $\pm\sqrt{2} + \sqrt{2}j$ further improvements in the efficiency can be achieved by omitting or simplifying complex multiplications involving these twiddle factors. This optimization will reduce the number of multiplications for 64 complex samples by more than 50%. The resulting formula for calculating the number of multiplications in a parallel FFT becomes

$$F_{parallel}(N) = \tfrac{3}{2} N \log^2(N) - 5N + 8, \tag{A1}$$

where N (with $N > 4$) is the size of the FFT.

3. The parallel FFT is needed to process all the samples at each clock cycle. After this step, it becomes possible to combine the output of two consecutive FFT results into one double-sized FFT result using an additional butterfly step. This results in one step in a "pipelined" FFT, which has the advantage of requiring less multiplications than a parallel FFT of the same size. Multiples of these steps can be put in sequence, each step doubling the output size of the FFT and halving the time resolution. Shown in Fig. 13, combining parallel and pipelined FFT, a hybrid FFT is realized with superior frequency resolution.

The number of multiplications required for the piped FFT can be calculated as followed, depending on the target size:

$$F_{piped}(N, B) = 3B\left(\tfrac{N}{B} - 1\right), \tag{A2}$$

where B is the output size of the parallel FFT, and N is the target size. Note that $N > B$ and always a power of two. Here, some multiplications can be omitted again; however, in this case it would be a negligible improvement.

The untangling of the phase and frequency requires an additional $N/2$ butterfly steps.

Subsequently, the power and phase per frequency component needs to be extracted. Normally, this is done by first taking the modulus and atan2 of the outputs of the FFT, writing volts per spectral component and then calculating the power. The modulus can be taking in one step, with the advantage that no square root operation is required, a resource intensive operation in a FPGA. R is the resistance of the digitizer in Ohms. P is the power in watts,

$$P(f) = \frac{re[X(f)]^2 + im[X(f)]^2}{R}. \tag{A3}$$

Since the output is 256 spectral components, two multiplications are required to get the modulus, another one is required to carry out the division, i.e., multiplication of $1/R$th. However, this can also be done after the summation process. The phase is obtained by a two dimensional lookup table with imaginary and real values along the axes and atan2 of the ratio inside. If a value is outside the range of the table, then the ratio of complex and real values is scaled to fit in range. For better resolution a CORDIC (Ref. 42) algorithm could be implemented. This however requires multiple clock cycles or more DSP blocks. The result of the above steps is a digital circuit on a FPGA, providing one power spectrum per four clock cycles with 256 spectral and phase components over a 14 GHz bandwidth.

The next step is to improve the signal-to-noise ratio and to reduce the statistical variation in the thermal and wave noise. This is done by averaging a number (n_{IF}) of the spectra per frequency and components, and summing frequencies together (n_{vid}), see Sec. II A. Both operations will increase the dynamic range and allow for variable time and frequency resolution.

The first substep is averaging. The FPGA has 256 accumulator registers, at each new spectrum, these values are added to the accumulator. Also the FPGA has 256 accumulator registers for the phase, and two buffers, for the previous phase samples. First, the phase is stored in a free buffer. Then its phase is unwrapped and subtracted from the phase in the other buffer, thus the difference in phase is determined. This buffer is freed, so it can be reused. The phase difference is then added to the accumulator registers.

After a number of additions (n_{IF}), the registers are then divided by the number of times they are summed (multiplication by $1/n_{\mathrm{IF}}$). The unwrapped phase difference is normalized to its frequency by subtracting bin frequency phase changes during the block time. The resulting values are summed by adding n_{vid} values and writing the outcome to the send buffer. These operations allow for an improvement of $5 \log(n_{vid}\, n_{\mathrm{IF}})$ dB in the dynamic range of the output spectra.

The total number of DSP blocks per FPGA can now be calculated, as the total of the multiplications required by the window, the FFT (parallel and piped) and the conversion to power,

$$M_{total} = N_{aq} + F_{parallel}\left(\tfrac{N_{aq}}{2}\right) + F_{piped}\left(n_{out}, \tfrac{N_{aq}}{2}\right) + 4\tfrac{1}{2} n_{out}. \tag{A4}$$

Here, n_{out} is the requested number of frequency bins and N_{aq} is the block size in the time domain. Both must be powers of two. In our case N is always 128. As mentioned in Sec. II A, it is always beneficial to increase the size of the FFT, where possible in order to gain a better dynamic range. However, if one wishes to implement a FFT with 512 samples, the number of DSP blocks would be 3528, which is currently beyond the capabilities high-end FPGAs. The present 256 frequency components would require a total of 2376 multiplications, which is acceptable, and leave plenty of multiplier capacity for additional processing.

This completes the post-processing of the FPGA. Subsequent logic would be required only for logistical purposes, i.e., getting the data from the send-buffer to the island localization module and tearing mode feedback controller and to a computer for diagnostic purposes.

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