

Literature review on thermo-mechanical behavior of components for LED system-in-package

Citation for published version (APA):

Esfahanian, M. (2012). *Literature review on thermo-mechanical behavior of components for LED system-in-package*. Technische Universiteit Eindhoven.

Document status and date:

Published: 01/01/2012

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

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Literature review on thermo- mechanical behavior of components for LED System-in- Package

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MT 12.08

Literature Review Report

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Eindhoven, February 2012

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1. Introduction

Reducing energy consumption is a main concern in the world. Typically 19% of the global energy produced is consumed in lighting. Although traditional incandescent light bulbs are already being replaced by more efficient kinds of light sources, there is still a lot to do in this field and many believe using LEDs promises a very efficient and bright future.

In the past, LED was widely used in traffic lights, indicator, and decorative lighting applications. The recent enhancements in LED efficacy and cost reduction contributed to LED's dramatic market penetration in various fields, such as, display, portable electronics, indoor and outdoor lighting applications. Compared to lighting products with conventional light source, comprehensive considerations in terms of optical, thermal, mechanical, and electrical were required in the development of LED lighting products.

Using the concept of "System in Package" to make solid state lighting LEDs as a part of ENIAC ESiP project is a collaboration between some companies in Europe to achieve a more efficient way of lighting and reduce energy consumption in this field.

System in Package (SiP) is characterized by any combinations of active electronic components of different functionality with passives and other devices like Micro Electro-Mechanical System (MEMS) assembled into a single standard package [1]. The demand of the semiconductors industry for high levels of integration, lower costs and a growing need for complete system solutions has led to the emergence of SiP solution which is based on the increase of the integration of different components in a same package.

Making LEDs in the form of SiP reduces the cost of final product by cutting the price of packaging since instead of packaging each component separately there is just one packaging step. Moreover, miniaturization without losing light density (because of the presence of more than just one LED) can be reached which expands the verity of applications for LEDs, like room lighting. These two features together will attract the consumers' attention, make LED technology more applicable and as a result the lighting energy consumption can be reduced dramatically.

Researchers at TNO organization -as a partner in ENIAC ESiP project- already made some efforts to make LED SiPs. An arrangement of components for a LED SiP is already designed at TNO from an optimization point of view which is shown in Figure 1. In this figure the green blocks are the driver and other passive components, the white-blue parts are LED dies and the gray material part represents the black molding compound which covers everything but the LEDs which are covered by a transparent material. As an improvement to the mentioned design, this literature study tries to answer the following questions:

- What types of materials could be used in these packages for each different part? Which ones may lead to better results?
- Which method of attaching the parts together may lead to a better design?

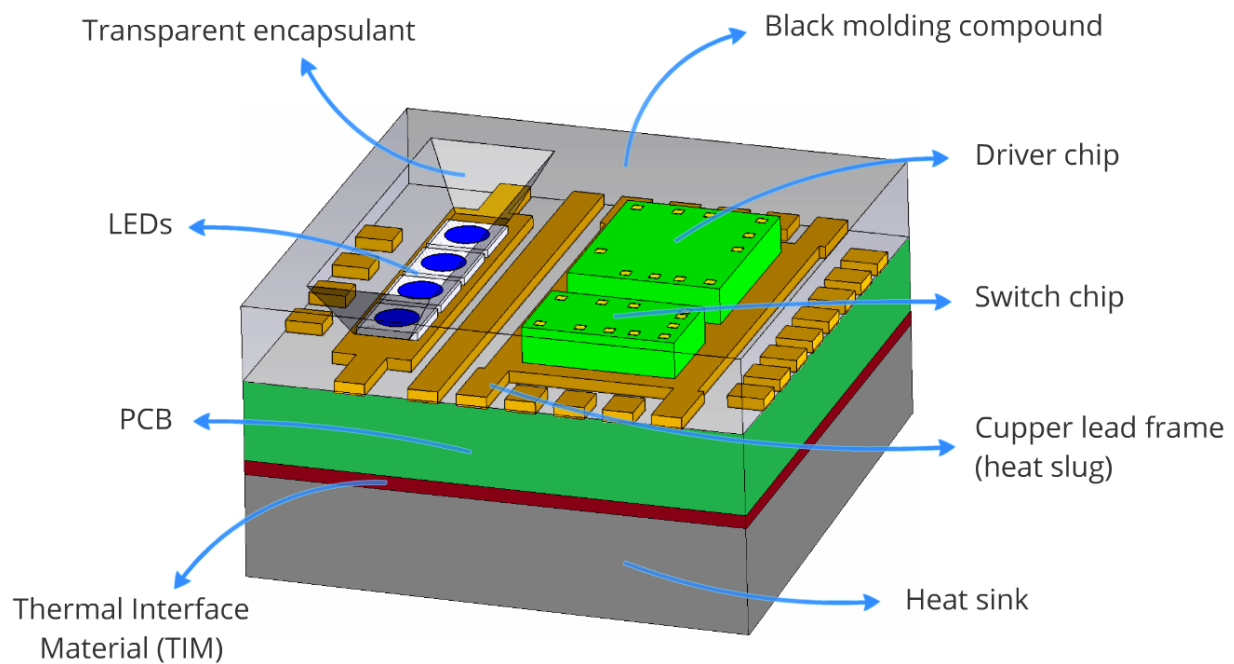


Figure 1- Current base design of TNO's LED SiP, a QFN like package (9x9mm) [2] [3]

Since the concept of these LED packages is a brand new topic and there is no previous study on it from a thermo-mechanical perspective, to answer the abovementioned questions the knowledge of both package design and making normal LEDs have to be applied. Based on the acquired information, some possible ways of making LED SiPs from different combination of materials and joints could be suggested, considering their potential failure modes.

The literature study is finalized by proposing some hypotheses on the feasible combinations of materials and interconnects for better performance of the LED SiPs in long term, considering the downside of each proposal. These proposals will be investigated in further detail in the phases after this brief study.

2. Components

Making a LED system in package, as shown and briefly introduced in the previous chapter, requires some components from different materials which are attached and connected together via different methods. By making use of other studies and published papers, this chapter tries to make suggestions on these materials, how to electrically connect the components and basically introduce the options to further improve this design.

2.1. Black molding compound

A large part of the whole LED SiP is covered under a black molding compound. This compound is essentially what makes the “package”.

The size of whole package can be reduced more by directly mounting the driver, without using a specific package for the driver, which is a suitable scenario for use in the intelligent LED SiP concept. Since the driver electronics should be placed in a dark setting for best performance and the molding compound of the package in a way also acts as the driver package, this compound is selected to be dark [2].

On the other hand, proper selection of materials of LED package components with similar coefficients of thermal expansion (CTEs) and coefficients of moisture expansion (CMEs) is required to release thermo-mechanical stress and hygro-mechanical stress [4]. The mismatching CTEs in LED packages induce thermal stress during the reflow soldering process [5]. Also mismatching CMEs induce hygro-mechanical stress in LED packages and cause the LED packages to swell after absorbing moisture. Different levels of swelling occur between polymeric and non-polymeric materials as well as among the polymeric materials. This differential swelling induces hygroscopic stress in the package, thus adding thermal stress at high reflow temperatures, thereby inducing delamination [6].

2.1.1. Polymer-based materials

Epoxies are the most common molding compound materials. Silicones, polyurethanes, and phenolics are also used as primary encapsulant materials or resins. Other materials may be added to this compound, referred to as “additives,” to achieve various functions and properties. The selection of the additives is influenced by the overall functions of the product, processing techniques and conditions, cost, and availability [7].

A molding compound may contain over ten additives such as fillers, accelerators, flame retardants, and curing agents. Each additive has a specific function that contributes to the encapsulation process and overall performance and reliability of the package. For instance, silica fillers used as additives in molding compounds reduce the coefficient of thermal expansion (CTE) and increase thermal conductivity of the molding compound. This will lead to lower thermal mismatch stress between the molding compound and the adjacent materials and, therefore, improve the reliability of the electronic package [7]. In some cases up to 70% of the compound could be of silica fillers so that it has less CTE mismatch with other silicon chip components of the package and reduce thermal stresses.

Multifunctional and biphenyl epoxy resins have been developed to address the need of reliable thin quad flat packages. The multifunctional epoxy resin shows very low shrinkage, low stress, and high glass transition temperature ($>170^{\circ}\text{C}$). Biphenyl resin is composed of 80% biphenyl and 20% novolac resin. Biphenyl resins exhibit high strength, low stress, and low moisture absorption. These two types of epoxy resins are primarily used for surface-mount packages [7].

Epoxy encapsulating resins have been synthesized with improved popcorn resistance (during reflow soldering in printed wiring assembly). The popcorn effect occurs during soldering, when moisture absorbed by plastic-packaged parts turns to steam, building up pressure inside the component and causing the package to crack [8]. Factors contributing to popcorn resistance are moisture diffusion, adhesion, curing shrinkage, physical strength at elevated temperatures, and package toughness. These factors are addressed by modifying molding compound chemistry and composition [7].

Other kinds of polymeric materials that can be used for the black molding compound are polyphthalamide (PPA) or liquid crystal polymer (LCP) [4] which are typically used as housing material in the application of making a normal LED device.

2.1.2. Ceramics

As mentioned, the disadvantages of the epoxy resin are lack of chemical stability, moisture-proof ability, and relatively bad thermal properties which can limit inherent performance of LED chips. Ceramic materials with high thermal conductivity, good environment stability, and high moisture-proof ability have been widely used in modern electronic packaging and can be regarded as a primary candidate for a package material of high power LEDs [9].

Hu et al. presented thermal and mechanical analyses of high power LEDs with ceramic packages [10]. The advantages of ceramic packages replacing the plastic molds include high thermal conductivity, excellent heat endurance, the ability to withstand hazardous environments,

flexibility for small and thin structures, enhanced reflectivity due to advanced surface-finishing technology, less CTE mismatch with the LED die, and high moisture resistance [11] [12]. Ceramic packages reduce thermal resistances from the LED junction and other heat generating parts of LED SiP to the ambient. As a result, ceramic packages lower delamination between interface layers in LED packages [4].

2.2. Transparent encapsulant

LEDs are encapsulated to prevent mechanical and thermal stress shock and humidity-induced corrosion. The encapsulant is a transparent material positioned over the LEDs so that light can come out of the package and it is made of a resin material.

The typical material types for the resin are epoxy and silicone [4]. However, epoxy resins have two disadvantages as LED encapsulants. One is that cured epoxy resins are usually hard and brittle owing to rigid cross-linked networks. The other disadvantage is that epoxy resins degrade under exposure to radiation and high temperatures, resulting in chain scission (which results in radical formation) and discoloration (due to the formation of thermo-oxidative cross-links). This is called encapsulant yellowing. Modification with silicone materials has been considered an efficient method to increase the toughness and thermal stability of transparent epoxy encapsulant resin. However, silicone compound as an LED encapsulant can have flaws, such as lower glass transition temperature (T_g), larger CTE, and poor adhesion to housing [4]. Li et al. [13] found that siloxane-modified LED transparent encapsulant is one possible way to improve the thermal mechanical properties, as the multi-functionality of siloxane compounds raises the crosslink density. The increase of the cross-link density means that siloxane compounds improve the bond energy of the polymer chains to mitigate the chain scission.

The other common type of materials to be used as transparent encapsulant are polymers like Polycarbonate (PC) and Poly(methyl methacrylate) (PMMA). The characteristics of polycarbonate are quite like those of PMMA, but polycarbonate is stronger, usable in a wider temperature range than PMMA. However, it is more expensive. Polycarbonate is highly transparent to visible light and has better light transmission characteristics than many kinds of glass.

Silicone resin to be used on top of LEDs can be mixed with different phosphor to achieve desired color, Correlated Color Temperature (CCT) and Color Rendering Index (CRI) [14].

In LED SiP application basically there are two ways of encapsulating the LEDs shown in Figure 2. Design (a) fills the whole cavity above the LEDs with a suitable material and in design (b) each LED is encapsulated separately and then a simple plastic like material (e.g. PMMA [15]) covers the whole array of LEDs which also acts as an optical lens.

A study by Lin et al. [14] is done on these two arrangements of LEDs for mobile flash module application where design (a) consists of three high power typical LED chips and design (b) uses vertical LED chips. At the end it is proved that design (b) has better performance, as especially

in CRI, in comparison to design (a). It is because vertical LED chips were employed, where light is only emitted on the top surface of the chips, therefore light absorption by neighboring chips found in design (a) was not observed. Moreover, better color uniformity was observed in design (b), where a uniform thickness layer of phosphor mixture was applied with conformal coating method.

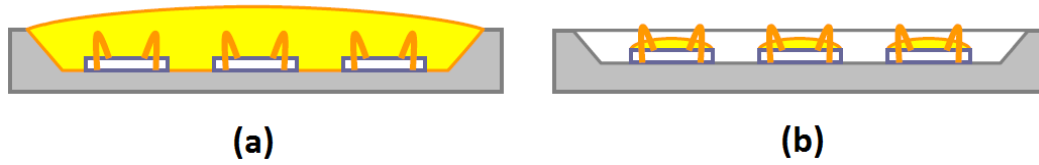


Figure 2- Two possible scenario to encapsulate LEDs in a SiP [14]

2.3. Circuit board

LED packages are usually bonded to a ceramic (e.g. Al_2O_3 , SiC, AlN), metal (MCPCB), or organic (FR-4) Printed Circuit Board (PCB) using a solder [4]. In this section each material is shortly introduced and also some new ways of making a circuit board for a LED SiP.

2.3.1. FR-4 Printed Circuit Boards

FR-4 PCB laminate is the most commonly used base material for printed circuit boards. The “FR” means Flame Retardant, and Type “4” indicates woven glass reinforced epoxy resin. A thin layer of copper foil is laminated to one, or both sides of an FR-4 glass epoxy panel. These are commonly referred to as “copper-clad laminates”. FR-4 copper-clad sheets are fabricated with circuitry etched into copper layers to produce printed circuit boards [16].

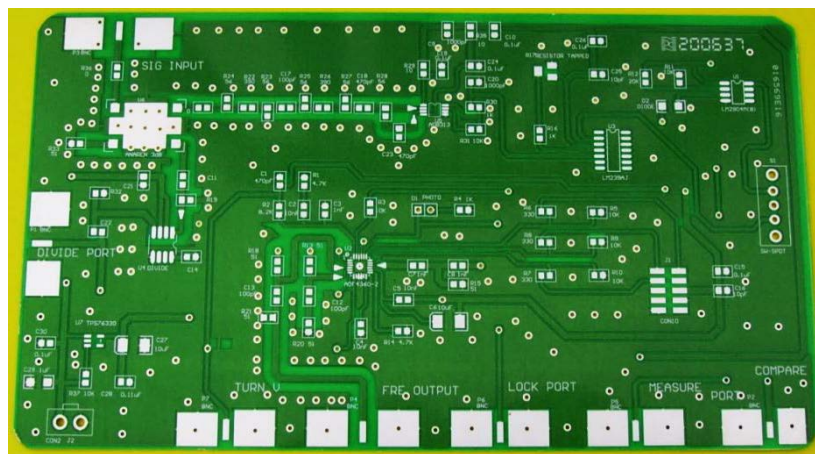


Figure 3- An example of a single sided printed circuit board FR-4 High TG PCB Manufacturing; Zoomtak Electronics Co., Ltd.

Because of its availability and low cost, FR-4 is so popular and commonly used that even the first prototype LED SiP of TNO is mounted on this type of PCBs [3]. An example of a FR-4 PCB is presented in Figure 3.

2.3.2. Metal Core Printed Circuit Boards (MCPCB)

Metal Core PCB means the base material for PCB is metal, not normal FR-4 etc. Currently aluminum and copper alloy are used as the core material. MCPCBs are used instead of traditional FR-4 PCBs because of the ability to efficiently transfer the generated heat away from the components. A layer of insulator is applied on the metal core to prevent any short circuit. Furthermore MCPCB can take advantage of incorporating a dielectric polymer layer with high thermal conductivity for lower thermal resistance [16].

In most cases, power LEDs will be mounted on MCPCB, which will be attached to a heat sink. Heat flows from the LED junction through the MCPCB to the heat sink by way of conduction, and the heat sink diffuses heat to the ambient surroundings by convection. In the application of LED SiP since in the package there are more than just 1 LED and also driver and other heat generating passive components, they add up to the working temperature of the package. In this situation using MCPCB could be a nice way to reduce predictable high temperature of the LED SiP. The following figure shows the cross section of a MCPCB and its main layers.

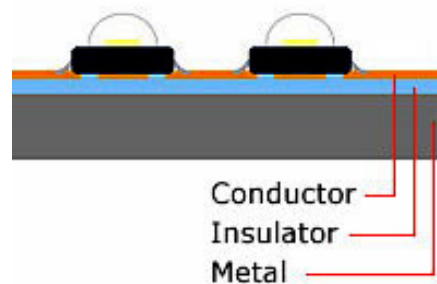


Figure 4- Schematic cross-section of a MCPCB with 2 LEDs mounted on it; Anglia Lighting Ltd.

2.3.3. Ceramic Printed Circuit Boards

Apart from MCPCB, in high pressure, high insulation, high frequency, high temperature, and high reliable and minor volume electronic products application, ceramic PCB will be the best choice [17], although they cost much more than FR-4 and MCPCB board types. The main thermal advantages of ceramic materials are mentioned in section 2.1.2. and they also stand for the use of ceramics in a circuit board. An example of such LEDs is presented in Figure 5.



Figure 5- An example of LEDs mounted on ceramic PCB; BANQ Technology Co., Ltd.

2.3.4. Silicon based substrates

2.3.4.1. Passive Integration Connective Substrate (PICS) technology

The PICS technology launched by Philips utilizes back-end Si processing to integrate passive components such as high quality Radio Frequency (RF) inductors, accurate Metal-Insulator-Metal (MIM) capacitors, resistors, as well as high-density capacitors onto a Si substrate. Thus it can serve as a platform for hetero-integration to form a Si-based System-in-Package. Such a SiP contains active component dies, MEMS, etc., using flip-chip techniques to minimize interconnect parasitics and footprint area [1] [18].

PICS technology is proposed as a way to achieve silicon based System-in-Package. Passive integration is the first step toward this kind of SiP and it is very interesting in terms of miniaturization, but also in terms of performance. Very efficient and high quality factor capacitors and inductors have been integrated, allowing the creation of complete modules including active devices, filters, decoupling capacitors. The solution proposed to have even smaller functional SiPs is the use of a substrate or interconnection die carrying the passive devices [19].

Basically PICS substrates use silicon as the base material and the advantage is the integration of part of the circuit components inside the board itself to save more space. It is obvious how LED SiPs design can benefit from this technology. Since making a LED SiP requires the integration of some electronic parts such as driver (which is made lots of passive components) by use of this method at least some of these components could be integrated inside the substrate.

2.3.4.2. 3D micro Through Silicon Vias (TSVs) technology

Although wire bonding is widely used in the 3D integration, the needs for high electric properties and small form factor drive the industries to adopt the TSV technology which is a rather new topic.

Compared with wire bonding, TSV has numerous advantages, including high density, high electrical performance, high signal speed, and low power consumption. However, the cost of the TSV manufacturing could be the biggest obstacle to achieve market adoption. The technology of 3D TSVs has been developed at NXP Semiconductors. The micro vias, for an aspect ratio (AR) up to 2.3, can be successfully covered by a sputtered 3 μm thick copper layer [20]. Because of its high aspect ratio structure, the manufacturing process is slow and complicated, resulting in the low throughput of the TSV process [21].

The TSV interconnect process is composed of via forming, insulation/seed layer deposition, and via filling. Cu electroplating is widely used in TSV filling process. However, via filling time of the Cu electroplating increases as via depth increases. Cu electroplating requires relatively long time for high AR via filling. Recently, via filling with molten metal has been developed for low cost process [21].

An example of a SiP conceived by this method is shown in Figure 6, which includes the vertical inter-connections between different dices on both side of the main bulk silicon carrier. These

vertical interconnections are provided by the copper TSVs formed on the carrier with connecting lines on each side. Since in this example the package is used in RF application, some passive components are also added on the carrier surface to enhance the electrical performance of the signal transmissions.

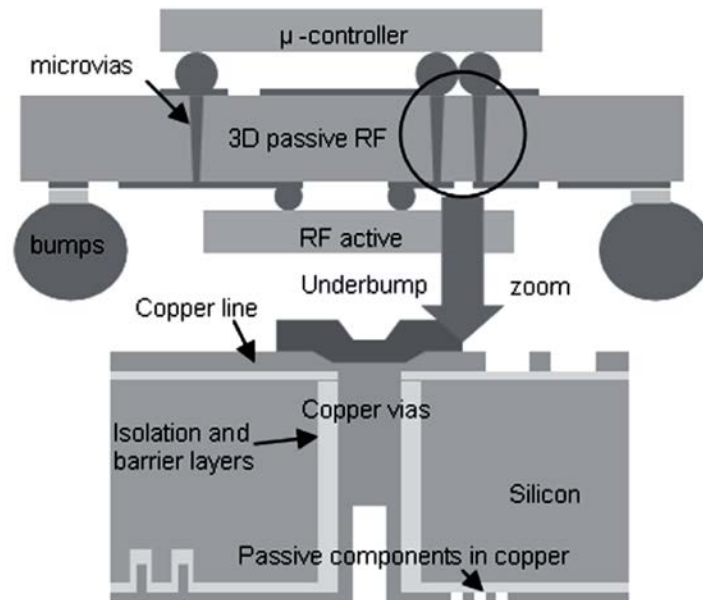


Figure 6- Schema of SiP conceived by NXP for RF application and copper vias within it [20]

Although not very economic friendly, using TSV technology enables even more compact package design for LED SiPs.

2.4. Interconnects

In TNO LED SiP, interconnections are considered to be of solder joint type [3]. Though solder joints are widely used for this kind of applications, in this section some other methods are introduced, along a way to improve the reliability of solder joints.

2.4.1. Solder bonding and flip-chip technology

Soldering provides a cost-effective means for attaching electronic packages to circuit boards using both small and large-scale manufacturing processes. In the electronic industry, it is widely used for assembling components, whether it is on circuit boards or on silicon wafers, to provide a reliable mechanical joint as well as an electrical interconnection [22]. Soldering processes accommodate through-hole leaded components as well as surface-mounted packages, including the newer area array packages such as Ball Grid Arrays (BGAs), Chip Scale Packages (CSPs), and flip-chip technology [23]. Flip-chip technology (a method of attaching chips using solder bumps directly on substrates for providing high density electrical interconnection) has emerged as a new

assembly tool for providing the fine alignment. This technology provides both the needed electrical interconnection and a low-cost passive alignment method [22].

Basically there are two general types of solder joint technologies used in electronics. They are through-hole and surface mount technology. Through-hole solder joints date back to the first electronic devices fabricated in the early part of the twentieth century. Although still a cost-effective means for assembling many types of electronic hardware, through-hole technology is being replaced in many applications with surface mount technology [23]. Even in the design of TNO's LED SiP the method of installing the whole package on the external circuit board is considered to be surface mounting and that is the reason for the QFN like design of this package. Furthermore, this method could be applied to connect the electrical components inside the package. Smaller package footprints and denser signal traces allow surface mount technology to realize significant weight and size reductions over comparably functional through-hole product. The advantages of surface mount include reduced board size through denser circuitry, lower product weight through device miniaturization, simplified circuit board fabrication with the absence of holes, and faster circuitry because package leads and long signal traces are eliminated [23].

The selection of solder depends on a number of parameters, such as melting point, coefficient of expansion, fatigue, creep behavior, solder wetting time and its reflow characteristics. For instance the need for low creep and high fatigue solder alloy has led to use of alloys such as Au80/Sn20 and Bi58/Sn42. Furthermore, with electronic manufacturers moving towards the use of lead-free solders, solders such as Bi/Sn and Sn/Sb are gaining popularity [22].

Pb-free solder materials are used in various parts of interconnections in electronic packages. The first-level interconnect is between the chip and the package substrate and lead-free solder bump material are used in the case of a flip-chip BGA (FCBGA). The second-level interconnect is the solder joint between the package substrate and the PCB [24]. Figure 7 shows the first and second level of interconnection in a flip-chip assembly.

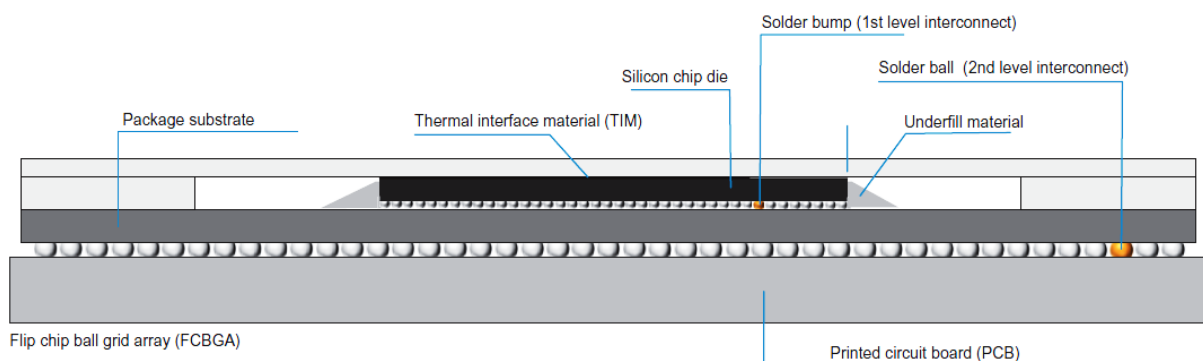


Figure 7- Schematic diagram of a flip-chip ball grid array (FCBGA) package [24]

Area array I/Os are an increasingly popular surface mount package configuration; the most widely used is the BGA. The advantage of BGA packages is the larger number of signal I/Os (upwards of several thousand). Smaller, finer pitched versions of the BGA have been marketed under the trade names of mini-BGA and μ BGA. Further miniaturization of the area array

package has been achieved with the CSP where the lineal dimensions of the package are less than, or equal to, 1.2 times those of the silicon chip [23].

The ultimate step in chip packaging is directly mounting the silicon chip to the circuit board, using an area array of solder bumps located directly on the chip; this approach is referred to as flip-chip technology. The metallurgy of a flip-chip solder joint (or “bump”) on a ceramic substrate is shown in Figure 8.

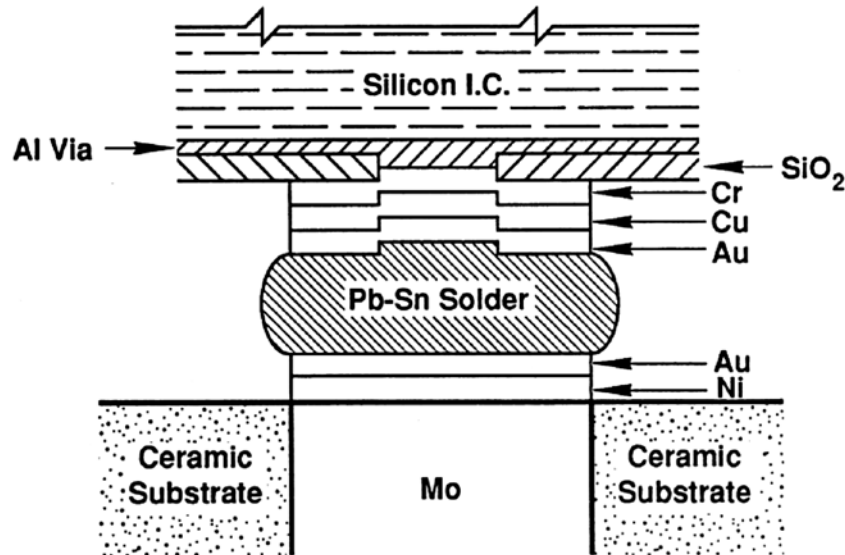


Figure 8- Metallurgy of flip-chip solder joints, in this case on a ceramic substrate [23]

The traditional assembly process for surface mount circuit boards has been furnace reflow. Solder paste (85±90wt.% metal powder) is deposited on the circuit board lands; the package is placed on the board so that the leads or terminations are located on top of the paste deposit; then, the assembly is passed through a furnace to melt the solder and form the joints. Surface mount boards have also been assembled by wave soldering, by hand soldering with an iron and solder wire, as well as by thermal conduction using the “hot bar” technique. In addition, laser techniques have shown promise for soldering surface mount interconnects [23].

In an attempt to enhance solder joint bonding strength, R. Cheng et al. [25] made use of Electrowetting-on-Dielectric (EWOD) effect. Testing results on the EWOD enhanced packaging structures of solder balls, flip-chip and solder ring hermetic package generally show about 50% enhancement in bonding shear strength. The significantly enhanced solder link bonding strength is hopeful for improving packaging reliability and is promising to be used in high performance silicon based electronic SiP.

The EWOD phenomenon of a molten Sn solder ball on silicon substrate is schematically shown in Figure 9, where a dielectric thin film was previously processed on the silicon surface. When an electrostatic voltage is applied between the metal solder and the conductive silicon substrate, the molten droplet spreads the contact area with the solid that is accompanied with a reduction in the contact angle. Reduction of this angle and the height of processed solder ball is the reason of its improved characteristics.

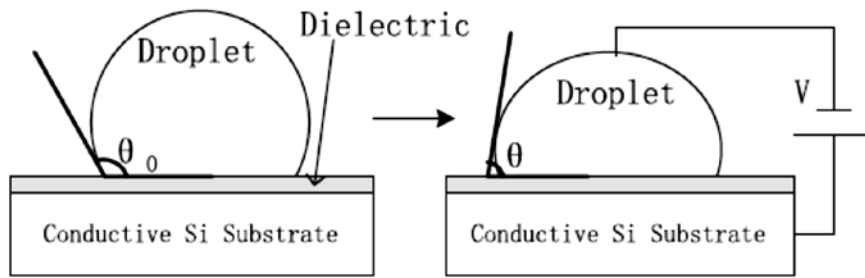


Figure 9- Schematic of EWOD driven contact angle (area) change between the molten solder and the silicon substrate [25]

The process starts with a solder ball sitting on an interconnecting line that is electrically isolated with the silicon substrate by using a dielectric thin film on the silicon surface. When the temperature is increased to the melting point of the solder ball, a voltage is applied between the metal line and the silicon substrate. Considering the wide use of solder balls in flip-chip packaging process, the EWOD enhanced bonding technique can also be used for flip-chip solder balls. In the solder bump flip-chip structure, the voltage can be easily applied between the cap and the bottom silicon chips, as is shown in Figure 10. In both situations, the contact angle of the molten balls will decrease due to the EWOD effect. Therefore, the contact area between the solder ball and the substrate will be enlarged, thereby, significantly enhancing the solder joint strength for highly reliable microsystem packaging [25].

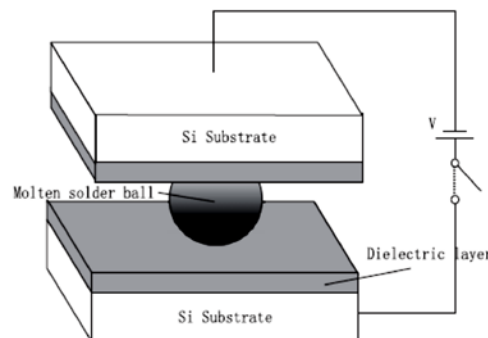


Figure 10- Schematics of the EWOD enhanced bonding strength for a solder bump flip-chip structure [25]

2.4.2. Adhesive bonding

Adhesives used in surface-mount applications are generally electrically insulative types whose main functions are mechanical attachment and thermal dissipation. Electrically conductive, silver-filled epoxies have been used for many years as ohmic contact adhesives to interconnect bare chip devices in hybrid microcircuits and are used as solder replacements for surface mounting of components on printed circuit boards [26]. Conductive adhesives are used in electronic packaging applications when constraints such as process temperatures, stress levels, metallization options, contact pad pitch, or cost require an alternative to soldered interconnections [27]. As an example, researchers at Chalmers University of Technology have focused on high-density packaging and interconnect using conductive adhesives for this type of packaging, using liquid crystalline polymer (LCP) as a repairable and planar substrate with roughly the same CTE value as Si [28].

Two basic types of adhesives are used to formulate both Isotropically Conductive Adhesives (ICAs) and Anisotropically Conductive Adhesives (ACAs): thermoplastic and thermosetting. Thermoplastic adhesives are high molecular weight molecules that are rigid at temperatures below the glass transition temperature (T_g) of the polymer. Above this temperature, polymer flow can occur. When using this type of material, assembly temperatures must exceed T_g to achieve good adhesion. Thus, T_g must be low enough to prevent thermal damage to the electronic circuits during assembly [27]. Epoxies are the most widely used matrices for thermosetting adhesives and for most common applications these epoxies contain approximately 30% vol. silver flakes [27].

Thermosetting adhesives are applied as mixtures of a curing agent with unreacted monomers of relatively low viscosity. Curing the mixture, typically with heat, causes a chemical reaction between curing agent and resin to form a three-dimensional cross-linked molecular network with a high T_g [27].

2.4.3. Anodic bonding

In its most used form, the anodic bonding process consists of joining silicon with borosilicate glass. Ceramics can also be used instead of glass. Bonding of glass and ceramics can also be done against metals, alloys and other semiconductors, provided the thermal expansion coefficients of the two materials are closely matched. Joining two silicon wafers by anodic bonding using a thin intermediate glass film, deposited by sputtering or by vacuum evaporation, has also attracted the attention of both research and industry [29]. The latter could be applied in fabrication of LED SiPs.

The silicon–silicon anodic bonding with a thin intermediate glass layer takes advantage of the relatively low-temperature, specific to the anodic bonding, and the low residual stress characteristic to the bonding of two wafers made of the same material. Because the glass layer is very thin (few micrometers), its influence on the thermal behavior of the bonded ensemble is negligible for most applications [30].

The glass layer can be deposited either by sputtering or evaporation. The bonding procedure with intermediate glass is basically the same as the one for bulk glass which will be described in the next paragraph, with the mention that the negative voltage is applied to the glass-coated wafer. Since at the bonding temperature silicon acts as a metal, an equipotential surface establishes immediately across the glass-coated silicon wafer, regardless of the shape of the cathode of the bonding equipment; therefore, bonding begins simultaneously at many points [29].

Anodic bonding is an electrochemical process that relies on the polarization of the alkali-containing glasses. It can be achieved by setting the two wafers together on a hot plate (300 - 450 °C) and applying a high DC voltage to the pair (400 – 1000 V), such that the glass is negative with respect to the silicon. When a DC voltage is applied to such a glass at elevated temperatures, the alkali cations are depleted from the vicinity of the anode and transported towards the cathode, as illustrated in Figure 11. For most of the glasses used for anodic bonding the conduction is primarily realized by Na^+ ions and in a very small extent by K^+ ions. As the

positive alkali ions are displaced towards the cathode, they leave near the anode an alkali-depleted region. Its depth increases in time and depends on the applied voltage [29].

Because of the surface roughness, the initial contact between silicon and glass occurs only at a few locations. The two wafers are separated over almost their entire area by a small gap (see the detail in Figure 11). Due to the fact that the rest of the glass is conductive, almost the entire applied voltage is shared between the growing alkali-depleted layer and this gap. Since electrostatic forces of attraction are largest where the gap is narrowest (i.e., around the periphery of the contact points) the nearby regions will be the next to be pulled together. In this way, the area of contact spreads outwards from the initial contact points across the entire wafer. When silicon and glass are in intimate contact, chemical reactions take place at the interface, resulting in the oxidation of the silicon substrate and, hence, in permanent bonds between silicon and glass. There is no general agreement on the chemistry of the interface reactions, but the formation of a thin oxide layer during bonding has been proved experimentally. [29]

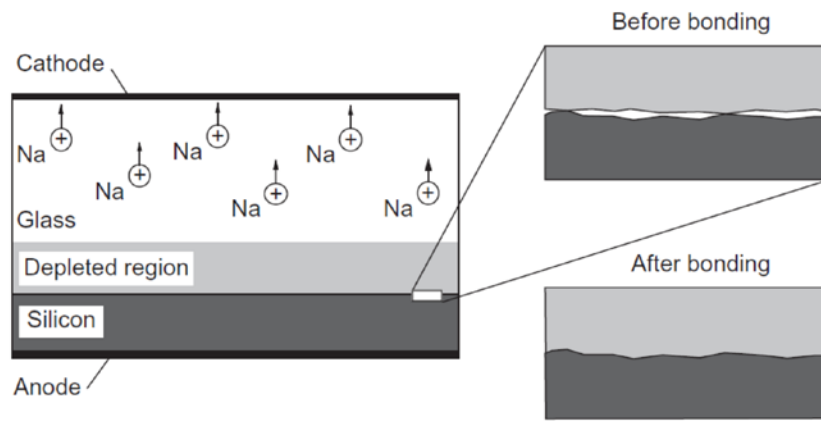


Figure 11- The mechanism of the silicon-glass anodic bonding [29]

However there are some drawbacks to this method of bonding. The production of a glass layer that can withstand the high electric field required for bonding, sensitivity to the surface imperfections, conflicting effects of bonding temperature etc. are some of them [29]. The deposition and bonding parameters still need to be optimized and the process to be proved successful for the bonding of wafers containing microstructures, in industrial conditions.

2.5. Thermal interface

Due to the miniaturization and increased power of electronics, the density of generated heat is higher during their operation. Research work has been done to dissipate the heat generated by electronic components during use to reduce the adverse effects of heat on the performance of the electronics.

In order to obtain effective heat dissipation, a low thermal resistance of the interface between the heat sink and the heat source is crucial. The effectiveness of heat dissipation depends in part on the geometric cross-sectional area of the conductive path and in part on the degree of

smoothness of the adjoining surfaces of the device and of the heat sink. However, the surfaces usually are not perfectly smooth. Irregularities on the surfaces of heat sink and heat source, even in a microscopic scale, form pockets and gaps in which air can be entrapped (Figure 12(a)) [31] [32]. The micro roughness is superimposed on a macroscopic non-planar in the form of a concave, convex or wavy surface, resulting in as much as 99% of the interface surface area being separated by air filled gaps [32]. Theoretically, the contacting surfaces will only contact one another at discrete points. The number of contact points increases with increasing pressure on the interface. Because air is a very poor thermal conductor, it acts as a thermal barrier preventing efficient heat transfer across the interface. To alleviate these problems, a Thermal Interface Material (TIM) is used between the heat sink and the heat source to fill in the surface irregularities and eliminate the air pockets and gaps [16] [31] [32].

The path of heat removal from an electronic package such as a LED SiP, involves conduction across the interface of the package case surface, through a TIM, into a heat sink and then convection to the environment.

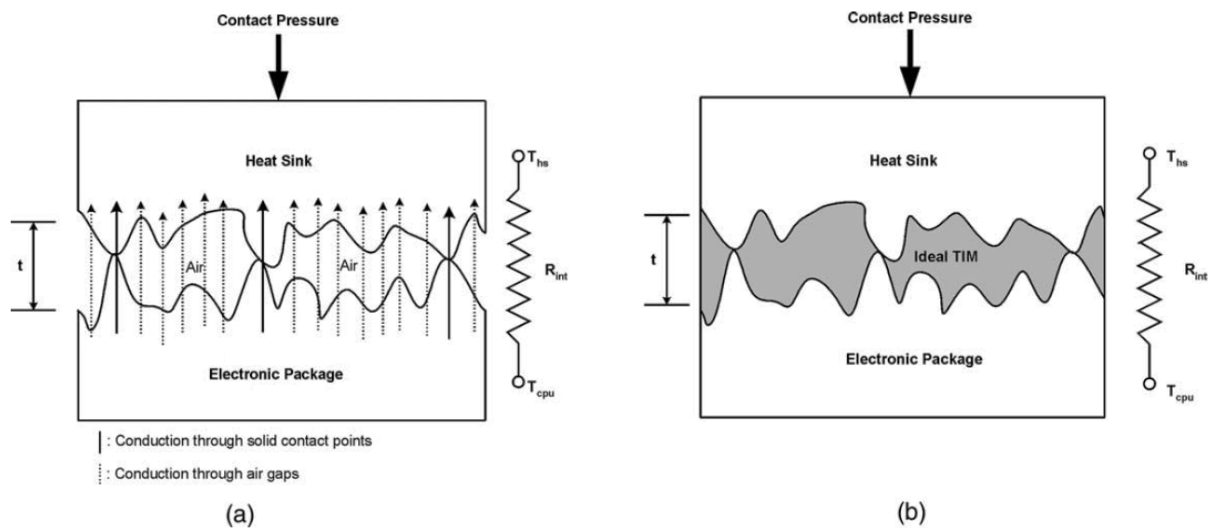


Figure 12- Exploded view of thermal interface when (a) no TIM is used and (b) when an ideal TIM is used [32]

For solids of high thermal conductivity, the contact resistance may be reduced by the following two methods: [32]

- Increasing the area of contact spots, accomplished by (a) increasing contact pressure which will flatten the peaks of the micro roughness, and deflecting the mating surfaces to reduce any non-flatness, or (b) reducing the roughness of the surfaces before the interface is formed by grinding the surfaces to remove non-flatness.
- Using a TIM of high thermal conductivity that can conform to the imperfect surface features of the mating surfaces.

Load constraints on electronic components and circuit boards make it unfeasible to use high contact pressure. Manufacturing highly finished surfaces is not practical due to cost constraints. Therefore, the practical alternative is to use a TIM applied at a moderate contact pressure.

The ideal TIM (Figure 12(b)) would have the following characteristics: [32]

- High thermal conductivity
- Easily deformed by small contact pressure to contact all uneven areas of both mating surfaces, including surface pores.
- Minimal thickness.
- Would not leak out of the interface.
- Would maintain performance indefinitely.
- Non-toxic.
- Manufacturing friendly (easy to apply and remove).

Ideal TIM has not yet been discovered, but several options are available to provide reduced interface resistance. However, an actual TIM will not be able to completely fill the cavities, and small air pockets will likely remain on both sides of the interface material. Pressure increases the actual contact area and reduces the amount of air remaining at the interface, thus reducing contact resistances on either side of the interface material. Increasing contact pressure can also decrease the conduction resistance of the interface material itself, by reducing its thickness.

Silicon or metal based thermal greases, phase change materials (PCMs), thermally conduction elastomers, thermally conductive adhesive tapes, gel-like TIMs, low melting temperature alloys (LMTAs), carbon nanotubes and liquid metal materials are some types of TIMs. In the following sections the most popular types of TIMs are further introduced.

2.5.1. Thermal greases and thermal adhesives

Thermal grease is composed of thermally conductive fillers dispersed in silicone or a hydrocarbon oil to form a paste. Recent improvements have been made in the application of thermal greases by developing printable greases, which can be screen-printed onto a heat sink baseplate at a specified thickness. Thermal grease exhibits high thermal performance at small contact pressures. These materials are attractive on the basis of their ability to fill the interstices and eliminate the interstitial air with a material whose thermal conductivity is much higher than that of air. Interface pressure causes excess grease to flow from the interface and form a thin thermal joint and surfaces to contact. It is probable that all of the air pockets are not eliminated. Also these materials do not require curing [32] [33]. Thermal greases can have thermal interface resistances ranging between 20 and 100 mm²KW⁻¹ when filled with conductive powders, while it can be as low as 6 mm²KW⁻¹ when filled with sodium silicate + boron nitride [34].

On the other hand, Thermal greases are not manufacturing friendly in that they are messy and difficult to apply and remove. Excess grease that flows out of joint must be removed to prevent contamination and possible electrical shorts. Joint integrity must be maintained with mounting hardware. Heat sink removal and re-installation requires cleaning the grease from the interface and a new application. Grease does not provide electrical insulation between contacting surfaces and can be pumped out of the interface under thermal cycling because of the relative motion of the mating surfaces under thermal expansion and contractions. Grease joints can dry out with time, resulting in increased thermal resistance. Grease degradation rate is a strong function of operating temperature and number of thermal cycles [16] [33].

Thermal adhesive is a type of thermally conductive glue used for electronic components and heat sinks. Thermal adhesive is similar to thermal grease but the glue is usually a two-part epoxy resin [16]. Thermally conductive adhesive tapes have poor thermal performance (test data show only slightly better performance than a dry joint) [32].

2.5.2. Phase Change Materials (PCMs)

A liquid or semi-liquid usually has good fluidity, and therefore, high conformability. The most common carrier in thermal greases is silicone. The disadvantages of silicone grease are messiness and difficulty of removal by dissolution. Silicone rubber was tried as a carrier to replace silicone grease. However, it needs higher pressure and sometimes, even under pressure it still does not fill the air gaps, due to its higher viscosity and consequent less conformability. A common disadvantage of using a liquid or semiliquid carrier is that it tends to flow out, whether it is in service or not. Thus, a better choice is a carrier which is in the solid state at room temperature and in the liquid or semi-liquid state at the higher service temperature; hence, a phase change material (PCM) [31].

PCMs are made of a mixture of suspended particles of high thermal conductivity, such as fine particles of a metal oxide and a base material. Although phase change of the base material is implied, this is not the case. These materials do not actually change phase, but their viscosity diminishes so that they flow. The base material can be a natural material such as fully refined paraffin, a polymer, a co-polymer, or a combination of all of these [32].

PCMs typically have high published thermal performance at moderate contact pressures; further, they exhibit low contact resistance. Material flows throughout the thermal joint to fill air gaps and provide minimum thickness by allowing the mating surfaces to come into contact. Alternatively when the joint becomes thin, the viscosity prevents pump out from mechanical flexure of the interface surfaces. Use of this material requires moderate compressive force to bring the mating surfaces together and cause the TIM to flow. The desired phase change property limits the choice of polymer and filler combinations; limiting the thermal performance of these materials. PCMs possess relatively low thermal conductivity [32].

The performance of a PCM TIM may be enhanced by mixing the PCM with polymers and with particulate fillers of high thermal conductivity. However, most PCMs with high energy storage density have an unacceptably low thermal conductivity [31]. Also in the application of PCMs, high conductance is achieved primarily by enhancing the gap materials' spreadability and elasticity. Further, issues such as dry-out/pump-out and mechanical fatigue compromise the long-term reliability of these materials [35].

2.5.3. Nanostructured TIMs

Micro and nano scale research is enabling new nanostructured materials, which can be used either in conjunction with modern TIMs, or as stand-alone materials which possess improved thermal and mechanical properties. These materials include nanoparticle laden TIMs, dispersed

carbon nanotubes (CNTs) in a polymer matrix, vertically aligned carbon nanotubes (VACNTs) and graphite nanoplatelets (GNPs).

Nano composite TIMs can be described as materials consisting of embedded nanoparticles in a polymer matrix. Generally speaking, for the same type of filler, larger average particle sizes lead to higher effective thermal conductivity for a fixed volume fraction. On the other hand, through the infusion of nanoparticles, there is a greater likelihood of a fully percolating network for heat flow, thereby increasing the composite's overall thermal conductivity. Figure 13 elaborates this concept [36].

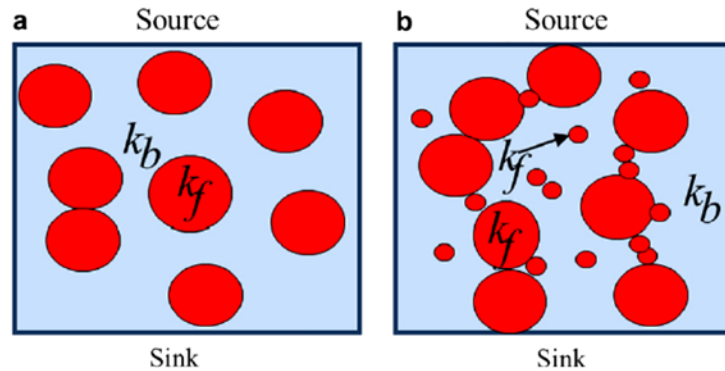


Figure 13- Percolation network through inclusion of nanoparticles. (a) Large agglomerations fail to produce fully conducting network from source to sink. (b) Inclusion of nanofiller completes network thereby increasing effective thermal conductivity of the matrix [36]

Early work using nanotubes includes dispersing them randomly in a matrix material forming a percolating network, which increases heat flow similar to nanoparticle laden TIMs. Typically, the thermal conductivity of the base polymer is orders of magnitude lower than the expected value for the nanotubes. The challenge is to enhance the thermal conductivity of the matrix by adding CNT at a low loading level [36].

Improved methods of dispersing the nanotubes involve better alignment along the heat flow path. Choi et al. [37] noted an increase of 10% above the original composite conductivity by aligning the nanotubes in a magnetic field. Compared to randomly dispersed tubes in polymer matrices, several experimental results have shown that the VACNTs (Figure 14) compare favorably to other modern TIMs. The mechanical compliance of carbon nanotubes has been of particular interest since elements of device package have different coefficients of thermal expansion, which may eventually lead to delamination of other TIMs, causing overheating and device failure. Since the nanotubes have high intrinsic axial conductivity, the primary source of thermal resistance is the boundary resistance at the free ends of the tubes [36]. The thermal contact resistance can be reduced by coating the tips of the CNTs with metals, or by using thermo compression bonding of CNTs [34].

Nanostructured TIMs promise improvement in effective thermal resistance compared to conventional bulk materials. However, a number of advancements are needed before the promise of such materials is fully realized in practical applications. Particular emphasis is needed on the alignment of materials and reduction of boundary resistances at the interfaces between

the fillers and the matrix. For VACNT TIM, improvements in CNT synthesis including precise control over volume fraction, elimination of defects, and array height are all needed [36].

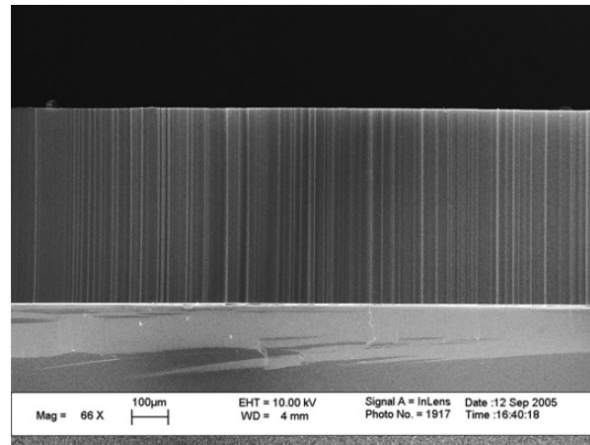


Figure 14- SEM images of VACNT (100 μm scale bar) [36]

Graphite nanoplatelets are another emerging class of nano materials that are gaining favor for many technological applications such as conducting composites, electronics, batteries, sensors, etc. GNPs offer an alternative to carbon nanotubes due to their excellent physical and chemical properties and low cost. GNPs have a platelet thickness in the range of 0.35-100 nm. “GNP” in the literature refers to various forms of graphite such as exfoliated graphite, expanded graphite or graphene. GNP/polymer conducting composites have been developed by dispersing GNPs in both thermoplastics and in thermosetting polymers for potential applications such as thermal interface applications due to the high thermal conductivity of GNPs [38]. M.A. Raza et al. [38] showed the thermal conductivities of GNP/silicone composites produced by mechanical mixing represents an 11-fold increase over that of silicone and is a 35% more than similar composites prepared by speed mixing.

In another work D.D.L. Chung et al. [39] use flexible graphite penetrated by a carbon black thermal paste, due to its conformability and thermal conductivity as a thermal interface material. Flexible graphite is a material made by the compression of exfoliated graphite, which is in turn made by the exfoliation of intercalated graphite flake. Although flexible graphite is conformable, it is not as conformable as thermal interface materials in the form of pastes (known as thermal pastes). A particularly conformable type of thermal paste is a paste with carbon black as the solid component and a polyester oil as the vehicle. Due to its high conformability and spreadability, the carbon black thermal paste is much more effective than flexible graphite as a thermal interface material [39].

2.6. Heat sink

As shown in Figure 1 the top part of LED SiP design is completely covered by either black molding compound or transparent encapsulant, which are poor thermal conductors. Nearly all heat, generated from the P-N junction of LEDs, driver and other electrical passive components,

has to exit the package through the other side of the package. Heat sink is the last part of this path where heat generated by these sources is conducted to outside ambience.

Generally heat sinks play two key roles in electronic packaging: thermal management and mechanical support. The external heat sink size of LED is not allowed to be large and fans are not permitted to be used for additional cooling (from the view points of economy and reliability) [40].

Common heat sink materials are metals, e.g., copper, aluminum (which is already used in TNO's first LED SiP design), and related alloys such as copper/tungsten or copper/molybdenum [41] [42]. Because of the shortcomings of these traditional heat sinks, there has been considerable work on new materials, primarily composites reinforced with fibers and particles. Advantages of these new materials include high thermal conductivities; low, controllable coefficients of thermal expansion; weight reductions; high strength and stiffness; and availability of net shape fabrication processes. In some cases the new materials are cheaper than the ones they replace [41]. There are four key classes of composite materials used in electronic packaging thermal management: Polymer Matrix Composites (PMCs), Metal Matrix Composites (MMCs) and carbon/carbon composites (CCCs). Polymers reinforced with continuous pitch-based carbon fibers have the highest thermal conductivity of all commercial PMCs. Perhaps the most successful of MMCs is Al-SiC, which was first used in packaging in the 1980s. Another effective MMC is beryllia particle-reinforced beryllium. It is also used in commercial applications, although not as widely as Al-SiC because of its higher cost. CCCs (e.g. ThermalGraph) are very attractive thermal control materials for weight sensitive applications [41].

Ceramics have also been attracting vast attention as heat sinking materials; especially AlN is actively applied to LED packages [9]. Thermal conductivity can be as high as $200 \text{ WK}^{-1} \text{ m}^{-1}$ by material purification; impurities are separated at the grain boundaries. It is also advantageous that thermal expansion coefficients are close to those of semiconductor materials. Ceramics are electrically insulating and optically nonreflecting; surface metallization is usually necessary [42].

In some other electronics applications boards with thermal vias are also used. Thermal vias are often used to reduce the thermal resistance of materials with low thermal conductivities. Figure 15 shows an example of such thermal enhancement using vias for the Intel's TCP (Tape Carrier Package) developed for the mobile applications. The thermal paths are through the top and bottom of the chip. Heat sink can be thermally connected to the chip through the vias [43]. Troubles like high thermal concentration in the LED SiP, heat management of the package can benefit from this method.

In the application of high-power LED packages X.-y.Lu et al. [40] made a new type structure of flat heat pipe (FHP) cooling device as shown in Figure 16. The FHP consists of an evaporator, an adiabatic section and a condenser. The FHP circulates the vapor and liquid in the same pipe line. The FHP is a copper/water unit; namely, the material of FHP is copper, the working fluid in the loop is water and the porous wick structure material is copper mesh. Under steady state condition, when enough heat load is supplied to the evaporator, the liquid water in the evaporator is vaporized, and flows along the adiabatic section to the condenser, where the heat is removed by phase change to the ambient environment and the working fluid turns back to liquid

phase, and then reflows to the evaporator through the porous wick on the wall of the FHP, so the working fluid is circulated by capillary forces is supplied by the wick structures, and forms a thermal circulation. If necessary, this technique can be also applied to the LED SiP structure.

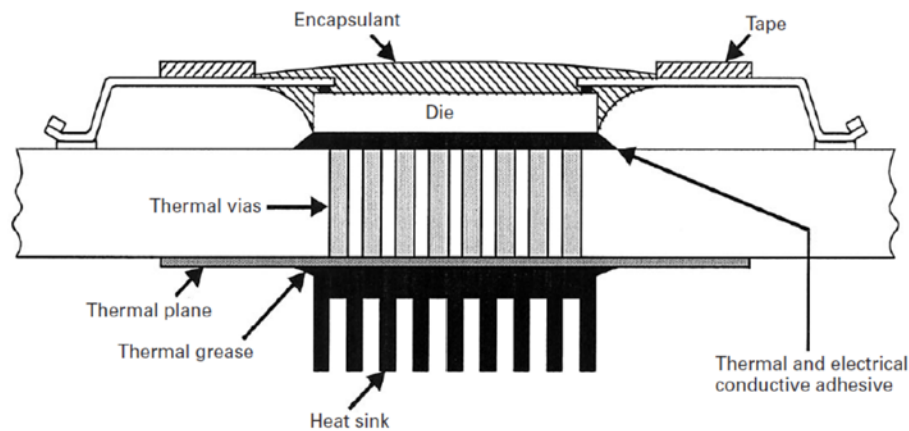


Figure 15- Intel Tape Carrier Package using thermal vias to enhance thermal performance [43]

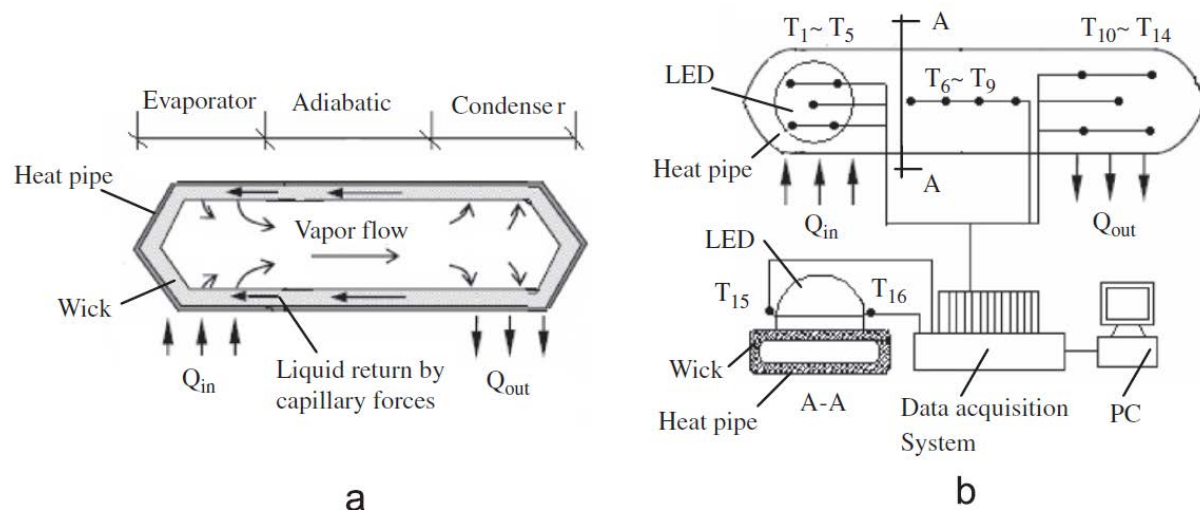


Figure 16- (a) schematic diagram of the FHP and (b) LED on top of the FHP [40]

2.7. Inkjet printing, a new approach to make SiPs

Additive manufacturing technology using inkjet offers several improvements to electronics manufacturing compared to current non-additive masking technologies. Manufacturing processes can be made more efficient, straight forward and flexible compared to subtractive masking processes, several time-consuming and expensive steps can be omitted. Due to the additive process, material loss is minimal, because material is never removed as with etching processes. The amounts of used material and waste are smaller, which is advantageous in both productivity and environmental means. Furthermore, the additive inkjet manufacturing process

is flexible allowing fast prototyping, easy design changes and personalization of products. Additive inkjet processing offers new possibilities to electronics integration, by enabling direct writing on various surfaces, and component interconnection without a specific substrate.

Inkjet printing has been developed as a ceramic processing method over the last 15 years and has been used as a tool in graphics output for over 30 years. Objects are fabricated by the interaction of individual drop deposited on a substrate or on previously deposited layers [44]. The process is complex and involves a number of distinct steps.

Furthermore, using injectable polymer dielectrics and conductive nanoparticle inks is an interesting and flexible way to connect components together in high-performance and high functionality systems, such as SiPs and multi-chip packages (MCP). J. Miettinen et al. [45] reported inkjet printing of the interconnections for a complex electronic module consisting a whole functional subsystem, i.e. SiP. The interconnection between several bare die components and discrete passive components is done using injectable conductive Ag nanoparticle ink and injectable epoxy-based dielectric material. The structure of inkjet printed SiP is shown in Figure 17, where there are six conductive layers and Inkjet printing is utilized only in interconnecting the components.

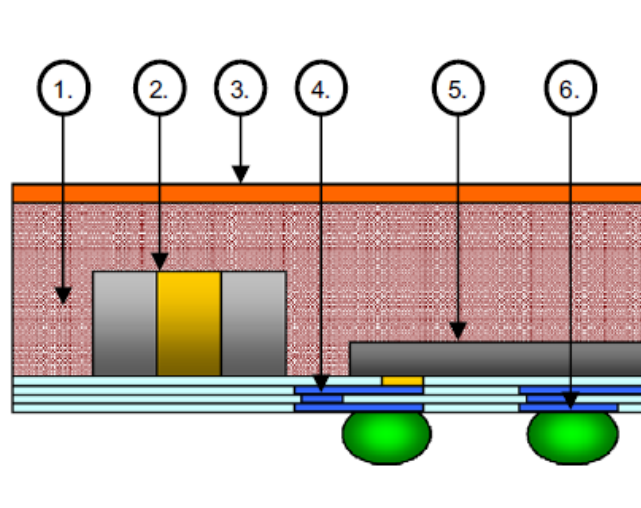


Figure 17- The structure of printed SiP by using inkjet printing: (1) molding material, (2) the embedded discrete components, (3) a film to improve the mechanical properties of the module, (4) the embedded bare die components, (5) inkjet printed conductive and dielectric layers including planes, traces and vias, (6) the terminals for the second level interconnection [45]

Furthermore, inkjet printing could be utilized in fabricating passive components, e.g. resistors, capacitors and inductors and active components such as transistor, diodes, and LEDs [45]. Taking the full advantage of inkjet printing in module manufacturing by making integrated passive components and possibly some lower performance active parts would enable further miniaturization of electronic systems. Of course increasing the variety of materials makes the design and processing far more complex due to the material and process compatibility issues. Also the lower conductivity of low-temperature sintered nanoparticle ink, process control, multilayer structure and fine pitch traces set some restrictions on the design of inkjet printed SiP [45].

Although no specific substrate is needed for interconnecting and for carrier for components, in the inkjet printed SiP the components are embedded inside molding material that works as a substrate for inkjet printing and the first dielectric layer is used to level the topography and form a uniform surface for conductive ink printing. To ensure the smoothness, surface energy is increased to achieve hydrophilic behavior, still maintaining a controlled pattern shape [46]. A schematic view of the steps to manufacture a SiP device interconnection by this method is shown briefly in Figure 18.

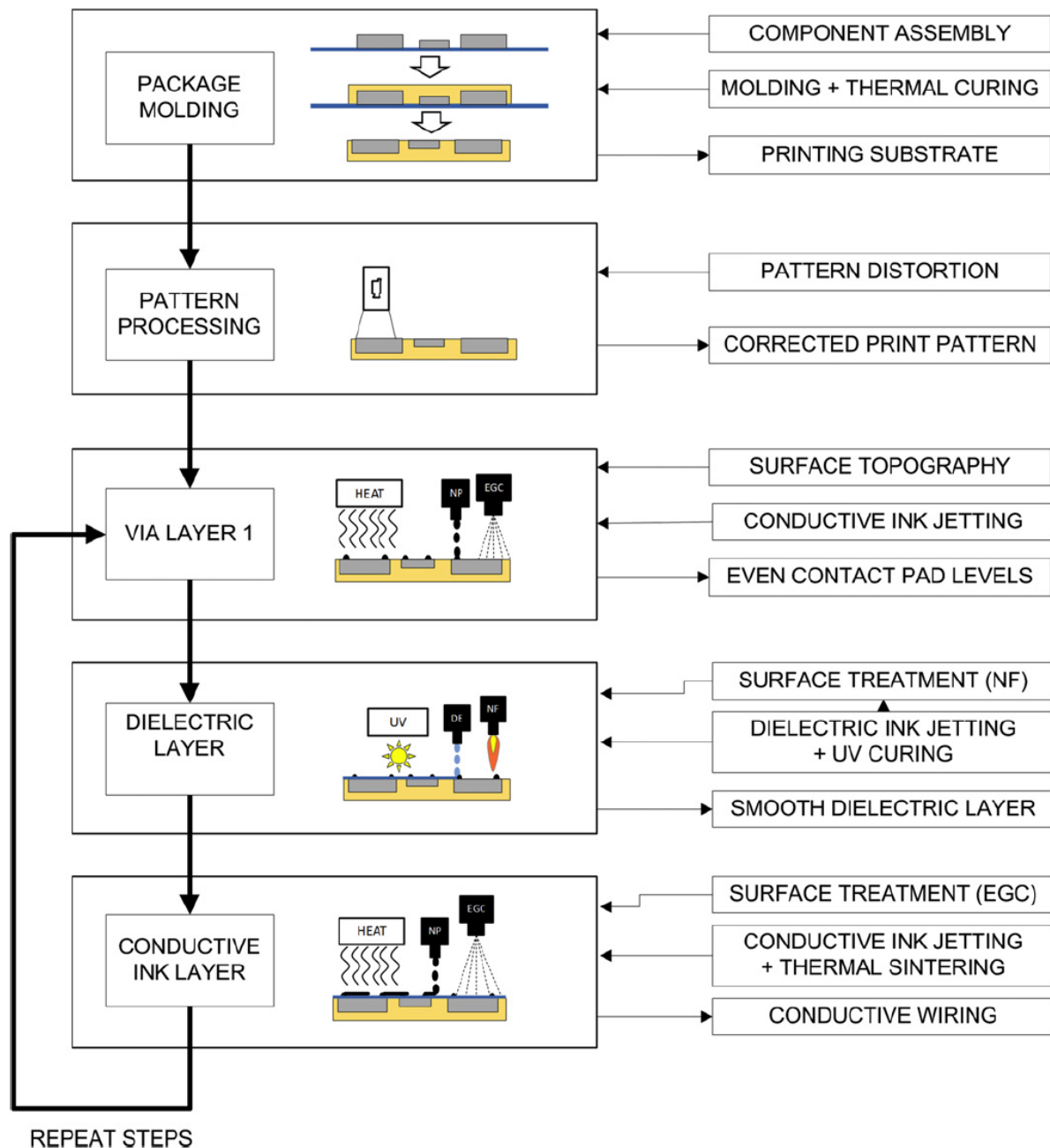


Figure 18- SiP device interconnection manufacturing process flow using inkjet printing [46]

2.8. Materials overview

A lot of materials with different properties and advantages/disadvantages were introduced in this chapter so far. Also having less CTE mismatch of the components' materials were pointed out as an important remark to reduce thermal stresses and to have a more reliable SiP. The following table summarizes thermo-mechanical properties of some of these materials which are commonly used for making electronic devices. One should notice that this table just gives a rough estimation, especially in case of alloys and polymeric materials where changing the fraction of a component or adding an additive can make a big difference in the mentioned properties.

	E [GPa]	CTE [$\mu\text{m/m.K}$] (@ 25°C)	Thermal conductivity [W/m.K]	T _g [°C]
Si (Polycrystalline)	169	2.6	148	-
Si ¹ (Monocrystalline)	$C_{ij} = \begin{bmatrix} 166 & 64 & 64 & 0 & 0 & 0 \\ 64 & 166 & 64 & 0 & 0 & 0 \\ 64 & 64 & 166 & 0 & 0 & 0 \\ 0 & 0 & 0 & 80 & 0 & 0 \\ 0 & 0 & 0 & 0 & 80 & 0 \\ 0 & 0 & 0 & 0 & 0 & 80 \end{bmatrix}$	2.5 - 2.62	20 - 140	-
FR-4	In-plane dir. 16.8 Transverse dir. 7.3	11 - 15 50 - 67	0.27 - 0.525	135
MCPCB	-	-	2.2	-
SiC	400 - 700	4.3 - 4.6	115 - 150	-
AlN	308 - 330	4.15 - 5.27	150 - 285	-
Al ₂ O ₃	220 - 460	7.2 - 8.2	16 - 31	-
Polyurethanes	2.2 - 4	63 - 100	0.19 - 0.6	-
PPA	2.1 - 2.2	-	0.15	92 - 127
LCP	10 - 40	50	0.2	275
PMMA	3.2	75	0.19	110
Polycarbonate	2.3	66	0.2	150
80Au / 20Sn	59.1	16	57	-
58Bi / 42Sn	35	15	19	-
95Sn / 5Sb	58	31	28	-
Thermal grease	-	150 - 300	0.8 - 3	-
PCM	-	-	0.25 - 20	-
CNT (VACNT)	-	-	10 - 250	-
Al ²	70	23.1	237	-
Cu ³	110 - 128	16.5	401	-

Table 1- Properties of some of the most commonly used materials in electronics industry. [16] [47] [48] [49] [50] [51] [52] [53]

¹ - For a (1 0 0) silicon wafer

² - For bulk material, there might be some differences in case of thin film application.

³ - For bulk material, there might be some differences in case of thin film application.

3. Loads and failure mechanisms

In chapter 2 we mainly focused on the components and interconnections between them separately, and some ways to improve their functionality and reliability. In some cases, other materials and methods of fabrication were introduced which can be used instead of the ones in the current LED SiP design for a better product. This chapter emphasizes more on the reliability of a LED SiP which could be subjected to different loads and different modes of failure might happen. Getting to know the critical points, interfaces and components of the package and their mechanism of failure helps the improvement of the design and leads to a better and more reliable product.

To be economically viable, the lifetime of LED SiP needs to be much longer than traditional electronics. The design lifetime of LED luminaires is typically 25 to 50 thousand hours. An initial assessment of the thermal performance of TNO's LED SiP shows that the thermal management is challenging the reliability limits, and with optimization the thermal loads can be accommodated at reasonable levels. Also very basic failure calculations indicate that the required lifetime is feasible [3]. As the light color and the light output depend on the temperature the package must demonstrate a stable thermal behavior. Narenran [54] estimates that the life of a LED is reduced with 50% for every 10°C increase in temperature. Commercially available LEDs typically have a maximum junction temperature of 120°C for a lifespan of 25 to 50 thousand hours. In the current design of the package, the junction temperature of the LEDs will be around 142°C which is clearly too high [3].

It is important to notice that the lifetime of the package as system is not solely determined by the LEDs. It is strongly influenced by the other components and interconnects that are present in the system. This is the reason why failure modes of a LED SiP could be complicated and one needs to consider common failure modes of LEDs, along with failures that might happen in other parts of the SiP.

LED lifetime is measured by lumen maintenance, which is how the intensity of emitted light tends to diminish over time. The Alliance for Solid-State Illumination Systems and Technologies

(ASSIST) defines LED lifetime based on the time to 50% light output degradation (L50: for the display industry approach) or 70% (L70: for the lighting industry approach) light output degradation at room temperature. For the LED itself, two types of failure are dominant: failures in the bulk of the LED material and failures at the interface. As stated before, the junction temperature is seen as most critical for these failures. The junction temperature is dependent on the operating conditions (the forward current and the forward voltage) and operating environment.

Another study by Han and Nahrendran [55] on failure modes of standalone LED drivers showed electrolytic output capacitors in the driver were the weakest link in the driver. Failure of the driver was caused by elevated pin temperatures. A lifetime of 7000 hours at a pin temperature of 100°C was measured in this study.

Severe light output degradation and burned/broken metallization on the LED die, interconnect failures of the packages including electrical overstress-induced bond wire fracture and wire ball bond fatigue, electrical contact metallurgical inter-diffusion, and electrostatic discharge, which leads to catastrophic failures of LEDs are other types of failure mechanism for a LED SiP. Carbonization of the encapsulant, encapsulant yellowing, phosphor thermal quenching, solder joint fatigue, and delamination of layers are also considered as potential failure mechanisms. Usually, the failure mechanism is derived and the root cause is found by failure analysis [56].

Although study of each component by itself does not give a valid judgment on failure of the LED SiP, it is a start and the next step would be considering the analysis and failure of the whole package together, as failure of the package might be the result of contribution of more than just one failure mechanism. Integrating more components in the package (e.g. for making it intelligent) involves other failure possibilities and makes the analysis even more complicated. Functionality and reliability of a LED SiP could be investigated under different loading conditions such as thermal loading, humidity, thermal shock, high current and voltage, on/off switching cycles etc. or a combination of these. The following parts of this chapter try to look into the most probable potential failure mechanisms of a LED SiP under different loading conditions from a thermo-mechanical point of view.

3.1. System in Package as a whole

With their complex structure, the SiP products usually have many more interfaces than a single chip package. The Coefficient of Thermal Expansion (CTE) mismatch between the different materials makes interface failure more pronounced and thermo-mechanical stresses very critical. Various reliability problems have been identified as major bottlenecks in the development of SiP products as for example passivation cracks, interfacial delamination, solder fatigue, Top to Bottom Metal Short (TBMS) which can occur due to temperature cycling stress. Thus, it has been observed that the qualification time becomes more critical than ever before and makes development of SiP products more difficult.

C. Regard et al. [57] propose a fast reliability qualification of SiP products by means of a new accelerated preconditioning. Although the package they consider does not include a LED, it gives a good insight to the potential failure of a SiP. Figure 19 shows the geometry of their SiP consisting of an active die placed on a Quad Flat Non-leaded (QFN) die pad, a passive integrated capacitor on silicon attached to the active die and flipped–chipped to the terminals of the QFN. All components are over-molded with an epoxy molding compound. It has been observed that the most critical interface that may lead to interfacial delamination is located between the glue and the lead frame (pointed out in the figure).

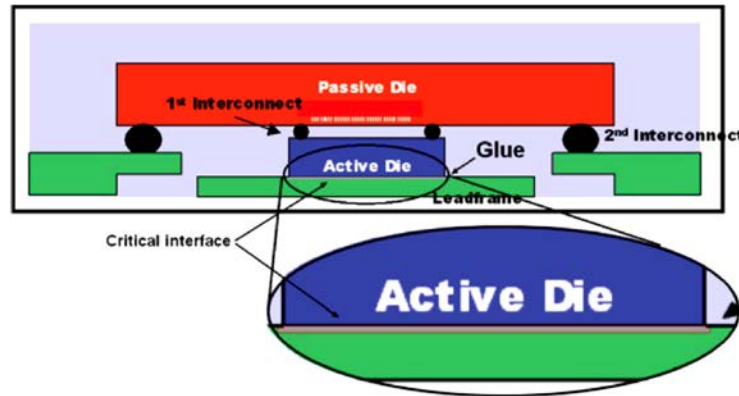


Figure 19- Schematic view of the SiP used by C. Regard et al. [57]

Though one of the most severe and universally used stresses is the thermal shock test, in order to accelerate this test, they define a new combined stress test method that consists of accelerating the failure mechanism by adding a moisture ingress before every cycle of thermal shock. The addition of a moisture step increases the stress level and accordingly reduces the time to failure. The combination of thermal shock and moisture storage seems to be a good way to accelerate the failure mechanisms of SiP products. Indeed, the moisture has two major effects:

- Decreasing of the interfacial strength
- Material expansion due to moisture ingress

3.2. Defect and dislocation generation and movement in the LED die

The lifetime and performance of LEDs are limited by crystal defect formations in the epitaxial layer structure of the die. Crystal defects are mainly generated in contacts and in the active region [58]. Crystal defects result in a reduction in the lifetime.

Defects introduced during crystal growth are divided into interface defects and bulk defects. Interface defects include stacking faults, V-shaped dislocations, dislocation clusters, microtwins, inclusions, and misfit dislocations. Bulk defects include defects propagating from the substrate and those generated by local segregation of dopant atoms or native point defects. Structural imperfections due to thermal instability also contribute to defect generation during crystal growth. Degradation modes of defect generation in LED dies are divided into rapid degradation

(random or sudden unpredicted degradation) and gradual degradation (wearout degradation). Recombination-enhanced dislocation climb and glide are responsible for rapid degradation [59].

Future research on defect and dislocation generation and motion will require improved structural and material design of LED dies and improved internal thermal management handling of thermal resistance from junction to the package to reduce the formation of crystal defects and dislocation movements caused by high-current-induced thermal effects and high ambient temperature [4].

3.3. Die cracking of LEDs

Extreme thermal shocks can break the dies of LEDs, such as GaN-based and GaAs-based LED dies. Due to differences in material properties (such as the coefficient of thermal expansion), LED packages can be subjected to mechanical stress when a high drive current is applied (which causes Joule heating at a fast rate) or when high ambient temperature conditions are suddenly applied. The high electrical stress and extreme thermal shock are the causes of die cracking. Barton et al. [60] found that the light output degradation was due, not to a change in contact resistance or the optical transmission of the plastic encapsulation, but to die cracking.

Initial defects, such as tiny notches or micro-cracks, caused by the sawing and/or grinding process may act as a starting point for die cracking. Chen et al. [61] reported that the strength of LED dies cut from wafers has to be determined for the needs of the design in order to assure the good reliability of the packages in manufacturing and service.

3.4. Electro-migration and electrical contact metallurgical inter-diffusion

Electro-migration is electrically induced movement of the metal atoms in the electrical contact to the surface of the LED die (such as GaN-based and GaAs-based LED dies) due to momentum exchange with electrons. Inadequately designed LEDs may develop areas of lower and higher thermal resistance (and temperature) within the substrate due to defects, electro-migration, or incomplete soldering. This leads to current crowding, causing thermal runaway, which results in severely increasing temperature in the package and reduction of the life of LEDs [62].

Electrical contact metallurgical inter-diffusion is caused by thermally activated metal–metal and metal–semiconductor inter-diffusion [63]. Electrical contact metallurgical inter-diffusion differs from electro-migration in the sense that electrical contact degrades due to out-diffusion and in-diffusion of the electrical contact. On the other hand, electro-migration is due to crystalline defects or defect tubes forming in the metal and places where metal atoms accumulate. The continuous metallurgical inter-diffusion causes electrical contact degradation, which results in the alloying and intermixing of the contact metals.

The failure modes of the electrical contact metallurgical inter-diffusion of LED packages are light output degradation, an increase in parasitic series resistance, and short circuits of LEDs. The driving forces of failures are high drive current and high temperature increase. Proper thermal management and innovative package designs are required to solve electro-migration and electrical contact metallurgical inter-diffusion. Thermal conductivities of interface materials, which constitute a large portion of the thermal resistance, should be improved to prevent these two phenomena because the contact resistances of the interface materials can affect the overall thermal resistance.

3.5. Carbonization and yellowing of the encapsulant

Carbonization of the plastic encapsulation material on the diode surface under electrical overstress resulting in Joule heating or high ambient temperatures leads to the formation of a conductive path across the LED and subsequently to the destruction of the diode itself. Carbonization of the encapsulant decreases the encapsulant's insulation resistance, significantly inhibiting its ability to provide electrical insulation between adjacent bondwires and leads [64]. The loss in insulation resistance of the plastic combined with latch-up of the device at temperatures above threshold temperature (such as 200 °C of high ambient temperature for plastic-encapsulated microcircuits) can initiate a thermal runaway process leading to carbonization of the encapsulant. In this process, the fusing of the bondwires at high current causes the current to be shunted through the plastic, leading to Joule heating of the plastic. This Joule heating further decreases the insulation resistance and can eventually result in carbonization of the encapsulant [65].

Fine-tuning of absolute maximum ratings of electrical current and ambient temperature for usage conditions as well as thermal management are required to avoid unexpected high loads resulting in carbonization of the encapsulant.

As mentioned before, transparent epoxy resins are generally used as LED encapsulant. However, epoxy resins have two disadvantages as LED encapsulants. One is that cured epoxy resins are usually hard and brittle. The other disadvantage is that epoxy resins degrade under exposure to radiation and high temperatures which is called encapsulant yellowing. Modification with silicone materials has been considered an efficient method to increase the toughness and thermal stability of transparent epoxy encapsulant resin. However, silicone compound as an LED encapsulant can have flaws. Li et al. [13] found that siloxane-modified LED transparent encapsulant is one possible way to improve the thermal mechanical properties, as the multi-functionality of siloxane compounds raises the crosslink density.

The failure modes of encapsulant yellowing are decreased light output due to decreased encapsulant transparency and discoloration of the encapsulant. The basic causes of encapsulant yellowing are (1) prolonged exposure to short wavelength emission (blue/UV radiation), which causes photo-degradation; (2) excessive junction temperature; and (3) the presence of phosphors.

3.6. Solder joint fatigue

Wherever solder joint is used, it may fatigue and may lift off and/or degrade. Failure modes and their mitigation of solder joint fatigue are associated with the degradation of electrical connections (solder joints) as well as the degradation of LEDs with time. The degradation of electrical connections increases forward voltage.

The solder interconnects go through stress reversals due to the CTE mismatch between the different part of LED SiP and the circuit board [66], resulting in thermo-mechanical fatigue of the solder joint. The failure mechanism could be fatigue due to deformation in response to applied mechanical stresses, cyclic creep and stress relaxation, fracture of brittle intermetallic compounds, or combinations thereof [67]. During temperature changes, shear is the primary stress on solder joints. As a result, the surfaces of solder joints slide relative to one another during thermal cycling, producing electrical transients that are typically of short duration.

Common failure causes of solder joint fatigue are CTE mismatch between the package and circuit board, the geometry of the package, solder joint material and thickness, temperature swings and dwell time, the modulus and thickness of the circuit dielectric, and the thermal resistance of the dielectric [68].

In section 2.4.1. a new way to improve solder joint bonding was introduced where Electrowetting-on-Dielectric (EWOD) effect is used to enhance the area of solder balls and make their bonding shear strength generally about 50% more.

3.7. Delamination

Repeated cyclic stresses can cause the material layers of LED SiP to separate, causing significant loss of mechanical toughness. This causes delamination. Delamination can either occur between the LED die and silicone encapsulant [69], between the encapsulant and packaging lead frame [70], between the LED die and die attach [71], or any other interface in the SiP. The failure mode associated with delamination is generally decreased light output. When delamination occurs in a thermal path, the thermal resistance of the delamination layer is increased. The increased thermal resistance leads to increased junction temperature, which also affects many other failure mechanisms and ultimately reduces the life of product. Delamination may also cause a permanent reduction in light output. Failure causes are thermo-mechanical stresses, moisture absorption, and/or interface contamination.

The mismatching coefficients of thermal expansion (CTEs) between different components of LED SiP also induce thermal stress during the reflow soldering process. A high temperature gradient can cause delamination between the LED die and the encapsulant, which forms a thin chip-air-silicone interface inside the LED package [5].

In the manufacturing process, a CTE mismatch between the bonding solder and bonded parts during temperature cycling causes delamination between the bonded surfaces. The curing of epoxy resins involves the repetition of shrinkage and the development of internal stress, which may also cause delamination [72]. Nano-sized silica fillers around 25 nm to 50 nm are sometimes incorporated into encapsulant materials to minimize CTE mismatch and transmission loss as well as increase thermal conductivity [73].

As mentioned before, Hu et al. [10] presented thermal and mechanical analyses of high power LEDs with ceramic packages instead of usual plastic molding compound. Ceramics show better performance due to their better thermal conductivity and less CTE mismatch with LED dies.

There can be two effects on a device (thermo-mechanical and hygro-mechanical stress) that are responsible for initiating delamination, which can result in reduced light output over a period of time. Proper selection of materials of LED SiP components with similar CTEs and CMEs is required to release these stresses.

4. Conclusion and recommendations

There are a lot of challenges on the way of making LED SiPs and amongst the most important ones, thermo-mechanical challenges. Proper thermal management of the package plays a critical role on durability and reliability of a LED SiP during its predicted life time. Making connection between different materials and introducing new interfaces are inevitable facts of making a SiP and the necessity of keeping the junction temperature of the LEDs below 120 °C doubles the importance of proper thermal management. This is why using materials with less CTE mismatch and finding ways to improve thermal conductivity of the used materials gain more attention.

In the previous chapters and based on the first design of a LED SiP by TNO, some ways of improvement of this design were introduced, including the use of another material for some parts or other ways of making the thermal/mechanical/electrical connections. These recommendations are not necessarily cost-effective and may result in more expensive product. For instance, although using inkjet printing technique to make the package or VACNTs as TIM of the SiP enhances the performance of LED SiP, they are not economically favorable unless mass production of LED SiPs lowers the cost of final product.

Another remark to mention is the possibility of making use of the introduced techniques and materials. As mentioned before, making a LED SiP is a new topic and what is done in this survey is to combine the knowledge from LED field and SiP field and propose some ways to improve the performance of the final product. In some cases there might be some conflicts when someone wants to apply these techniques. For instance, enhancing the shear strength of solder joints by the use of EWOD effect might be very interesting; however, using this concept in a LED SiP might cause damage to the other components of the package since it needs rather high temperature and exposure of the SiP to a voltage at the same time.

Considering all these facts, below are few recommendations that might improve the product:

- Using ceramic as the black molding compound. Ceramics has better thermal conductivity than normal epoxy and resins and can help to have a better dissipation of heat from the top of the package, though the main way of heat dissipation is still from the other side of SiP. However, since ceramic adds to the final cost of the product, using silica filled polymers is more favorable.
- Adding thermally conductive fillers to the transparent encapsulant to improve its thermal conductivity.
- Using MCPCB because of its better heat dissipation properties. On the other hand if miniaturization of the package is more important, using PICS or TSV technology are the suitable options.
- Although anodic bonding and conductive adhesives are new ways of connecting the passive chips and components to the substrate, it seems that solder bonding is still more reliable and effective. Moreover, this method brings the possibility of using flip-chip technology which can benefit the miniaturization of the whole package.
- Thermal greases and thermally conductive adhesives are commonly used as thermal interface materials for lots of application. But since they are messy and not manufacturing friendly, using other options like PCMs and nanostructured methods (e.g. CNTs) makes more sense.

Whether these recommendations are effective or not needs more analysis and perhaps experiments. Numerical analysis is the first step to find out more about their effectiveness.

Bibliography

- [1] V. Georgel, F. Verjus, E. van Grunsven, P. Poulichet, G. Lissorgues, C. Pellet, S. Chamaly and T. Bourouina, "A SAW filter integrated on a silicon passive substrate used for system in package," *Sensors and Actuators A: Physical*, vol. 142, no. 1, pp. 185-191, 2008.
- [2] E. Borst, "Design Parametrization of an integrated intelligent LED System-in-Package," Eindhoven, The Netherlands, 2011.
- [3] A. Gielen, P. Heslen, F. Swartjes, H. van Zeijl, F. Boschman, J.-E. Bullema, R. Werkhoven and S. Koh, "Development of an intelligent integrated LED system-in-package," 2011.
- [4] M.-H. Chang, D. Das, P. Varde and M. Pecht, "Light emitting diodes reliability review," *Microelectronics Reliability*, 2011.
- [5] L. Zhou, B. An, Y. Wu and S. Liu, "Analysis of delamination and darkening in high power LED packaging," *16th IEEE international symposium on the digital object, IPFA 2009*, no. 6, p. 656–660, 2009.
- [6] E. Wong, K. Chan, R. Rajoo and T. Lim, "The mechanics and impact of hygroscopic swelling of polymeric materials in electronic packaging," *ASME J Electron Pack*, vol. 124, p. 122–126, 2002.
- [7] H. Ardebili and M. Pecht, *Encapsulation Technologies for Electronic Applications (Materials and Processes for Electronic Applications)*, Elsevier (William Andrew Publishing), 2009.
- [8] "Online postgraduate courses for the electronics industry," University of Bolton, [Online]. Available: <http://www.ami.ac.uk/>. [Accessed January 2012].
- [9] L. Yang, S. Jang, W. Hwang and M. Shin, "Thermal analysis of high power GaN-based LEDs with ceramic package," *Thermochimica Acta*, vol. 455, no. 1–2, pp. 95-99, 2007.
- [10] J. Hu, L. Yang and M. Shin, "Thermal and mechanical analysis of high-power LEDs with ceramic packages," *IEEE Trans Dev Mater Reliab*, vol. 8, p. 297–303, 2008.
- [11] B. Vandeveld, D. Degryse, E. Beyne, E. Roose, D. Corlatan, G. Swaelen, G. Willems, F. Christiaens, A. Bell, D. Vandepitte and M. Baelmans, "Modified micro–macro thermo-mechanical modelling of ceramic ball grid array packages," *Microelectronics Reliability*, vol. 43, no. 2, pp. 307-318, 2003.

- [12] Y. M. Noor, S. Tam, L. Lim and S. Jana, "A review of the Nd:YAG laser marking of plastic and ceramic IC packages.," *Journal of Material Process Technology*, vol. 42, no. 1, p. 95–133, 1994.
- [13] H. T. Li, C. W. Hsu and K. C. Chen, "The study of thermal properties and thermal resistant behaviors of siloxane-modified LED transparent encapsulant," Industrial Technology Research Institute, Hsinchu, 2007.
- [14] J. R. Lin, T. Y. Ng, Z. Wang, S. M. Wan, K. W. Wong, M. Lu and E. Wu, "Wafer-level LED-SiP based mobile flash module and characterization," *Microelectronics Reliability*, 2011.
- [15] S. Ebnesajjad, "Adhesives for Electronics," in *Handbook of Adhesives and Surface Preparation*, Pennsylvania, Elsevier, 2005, pp. 260-300.
- [16] "Wikipedia, the free encyclopedia," Wikimedia Foundation, Inc, [Online]. Available: www.wikipedia.org. [Accessed January 2012].
- [17] "Best Technolog," Best Technology Co., Limited., [Online]. Available: www.bestpcbs.com.
- [18] F. Roozeboom, A. Kemmeren, J. Verhoeven, F. van den Heuvel, J. Klootwijk, H. Kretschman, T. Frič, E. van Grunsven, S. Bardy, C. Bunel, D. Chevie, F. LeCornec, S. Ledain, F. Murray and P. Philippe, "Passive and heterogeneous integration towards a Si-based System-in-Package concept," *Thin Solid Films*, vol. 504, no. 1-2, pp. 391-396, 2006.
- [19] F. Murray, F. LeCornec, S. Bardy, C. Bunell, J. F. Verhoeven, F. van den Heuvel, J. Klootwijk and F. Roozeboom, "Silicon Based System-in-Package: a new technology platform supported by very high quality passives and system level design tools," Silicon Monolithic Integrated Circuits in RF Systems, 2007 Topical Meeting on, Long Beach, CA, 2007.
- [20] C. Fang, A. Le Corre and D. Yon, "Copper electroplating into deep microvias for the "SiP" application," *Microelectronic Engineering*, vol. 88, no. 5, pp. 749-753, 2011.
- [21] Y.-K. Ko, H. T. Fujii, Y. S. Sato, C.-W. Lee and S. Yoo, "High-speed TSV filling with molten solder," *Microelectronic Engineering*, vol. 89, pp. 62-64, 2012.
- [22] N. R. Basavanahally and M. F. Brady, "Optoelectronic Packaging: Solder Assembly," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2001, pp. 6482-6485.
- [23] P. T. Vianco, "Electronic Packaging: Solder Mounting Technologies," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2001, pp. 2705-2715.
- [24] T. R. Bieler and T.-k. Lee, "Lead-free Solder," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2001, pp. 1-12.
- [25] R. Cheng, K. Jiang and X. Li, "Enhanced solder joint bonding strength of electronic

- packaging with electrowetting effect," *Microelectronic Engineering*, vol. 88, no. 11, pp. 3244-3248, 2011.
- [26] J. J. Licari and D. W. Swanson, "Chapter 4 - Adhesive Bonding Processes," in *Adhesives Technology for Electronic Applications (Second Edition)*, 2011, Pages, Elsevier (William Andrew), 2011, pp. 143-216.
- [27] A. Lyons, "Electronic Packaging: Conductive Adhesives," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Murray Hill, New Jersey, Elsevier, 2001, pp. 2654-2659.
- [28] L.-R. Zheng and J. Liu, "System-on-package: a broad perspective from system design to technology development," *Microelectronics Reliability*, vol. 43, no. 8, pp. 1339-1348, 2003.
- [29] A. C. Lapadatu and H. Jakobsen, "Chapter Thirty Two - Anodic Bonding," in *Handbook of Silicon Based MEMS Materials and Technologies*, Horten, Norway, Elsevier, 2010, pp. 513-520.
- [30] R. Holm, T. Kvister, H. Jakobsen, A. Hanneborg and P. Ohlckers, "Stability and common mode sensitivity of piezoresistive silicon pressure sensors made by different mounting methods," in *Solid-State Sensors and Actuators, 1991. Digest of Technical Papers*, San Francisco, CA, 1991.
- [31] Z. Liu and D. Chung, "Calorimetric evaluation of phase change materials for use as thermal interface materials," *Thermochimica Acta*, vol. 366, no. 2, pp. 135-147, 2001.
- [32] J. P. Gwinn and R. L. Webb, "Performance and testing of thermal interface materials," *Microelectronics Journal, Volume*, vol. 34, no. 3, pp. 215-222, 2003.
- [33] R. Viswanath, V. Wakharkar, A. Watwe and V. Lebonheur, "Thermal Performance Challenges from Silicon to Systems," *Intel Technology Journal Q3, Microprocessor Packaging*, vol. 4, no. 3, 2000.
- [34] A. M. A. Hamdan, R. Richards and C. Richards, "Characterization of a liquid-metal microdroplet thermal interface material," *Experimental Thermal and Fluid Science*, vol. 35, no. 7, pp. 1250-1254, 2011.
- [35] J. Xu and T. S. Fisher, "Enhancement of thermal interface materials with carbon nanotube arrays," *International Journal of Heat and Mass Transfer*, vol. 49, no. 9-10, pp. 1658-1666, 2006.
- [36] A. J. McNamara, Y. Joshi and Z. M. Zhang, "Characterization of nanostructured thermal interface materials - A review," *International Journal of Thermal Sciences*, 2011.
- [37] E. S. Choi, J. S. Brooks, D. L. Eaton, M. S. Al-Haik, M. Y. Hussaini, H. Garmestani, D. Li and K. Dahmen, "Enhancement of thermal and electrical properties of carbon nanotube polymer composites by magnetic field processing," *Journal of Applied Physics*, vol. 94, no. 9, pp. 6034 - 6039, 2003.

- [38] M. A. Raza, A. Westwood, A. Brown, N. Hondow and C. Stirling, "Characterisation of graphite nanoplatelets and the physical properties of graphite nanoplatelet/silicone composites for thermal interface applications," *Carbon*, vol. 49, no. 13, pp. 4269-4279, 2011.
- [39] K. Hu and D. Chung, "Flexible graphite modified by carbon black paste for use as a thermal interface material," *Carbon*, vol. 49, no. 4, pp. 1075-1086, 2011.
- [40] X.-y. Lu, T.-C. Hua and Y.-p. Wang, "Thermal analysis of high power LED package with heat pipe heat sink," *Microelectronics Journal*, vol. 42, no. 11, pp. 1257-1262, 2011.
- [41] C. Zweben, "Electronic Packaging: Heat Sink Materials," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2001, pp. 2676-2682.
- [42] H. Masui and S. Nakamura, "White Light-emitting Diodes," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2010, pp. 1-6.
- [43] H. Xie, Q. Tan and Y. C. Lee, "Electronic Packaging: Thermal, Mechanical, and Environmental Durability," in *Encyclopedia of Materials: Science and Technology (Second Edition)*, Elsevier, 2001, pp. 2715-2725.
- [44] B. Derby, "Inkjet printing ceramics: From drops to solid," *Journal of the European Ceramic Society*, vol. 31, no. 14, pp. 2543-2550, 2011.
- [45] J. Miettinen, V. Pekkanen, K. Kaija, P. Mansikkamäki, J. Mäntysalo, M. Mäntysalo, J. Niittynen, J. Pekkanen, T. Saviauk and R. Rönkkä, "Inkjet printed System-in-Package design and manufacturing," *Microelectronics Journal*, vol. 39, no. 12, pp. 1740-1750, 2008.
- [46] V. Pekkanen, M. Mäntysalo, K. Kaija, P. Mansikkamäki, E. Kunnari, K. Laine, J. Niittynen, S. Koskinen, E. Halonen and U. Caglar, "Utilizing inkjet printing to fabricate electrical interconnections in a system-in-package," *Microelectronic Engineering*, vol. 87, no. 11, pp. 2382-2390, 2010.
- [47] V. Siklitsky, "New Semiconductor Materials. Characteristics and Properties," Ioffe Physico-Technical Institute, [Online]. Available: <http://www.ioffe.rssi.ru/SVA/NSM/Semicond/index.html>. [Accessed 2 2012].
- [48] "Make It From," 2009. [Online]. Available: <http://www.makeitfrom.com/>. [Accessed 2 2012].
- [49] B. Houtzager, R. Overbeeke and R. Vennix, "Matbase, a leap forward in material data," 2009. [Online]. Available: <http://www.matbase.com/index.php>. [Accessed 2 2012].
- [50] "Optimizing PCB Thermal Performance for Cree® XLamp® LEDs," Cree, Inc., Durham, NC, 2010-11.
- [51] "Typical in-house specifications for soldering alloys," INDIUM CORPORATION OF

AMERICA, EUROPE and ASIA.

- [52] "Thermal Interface Materials For Electronics Cooling," Parker Hannifin Corporation, 2011.
- [53] J. Wilson, "ElectronicsCooling, Phase Change Materials Thermal Properties," Electronics Cooling magazine, 2005. [Online]. Available: <http://www.electronics-cooling.com/>. [Accessed 2 2012].
- [54] N. Narendran, J. Bullough, N. Maliyagoda and A. Bierman, "What is useful life for white light LEDs?," *Journal of the Illuminating Engineering Society*, vol. 30, no. 1, p. 57, 2001.
- [55] L. Han and N. Narendran, "Developing an accelerated life test method for LED drivers," in *Ninth International Conference on Solid State Lighting*, San Diego, 2009.
- [56] J.-S. Jeong, J.-K. Jung and S.-D. Park, "Reliability improvement of InGaN LED backlight module by accelerated life test (ALT) and screen policy of potential leakage LED," *Microelectronics Reliability, Volume*, vol. 48, no. 8-9, pp. 1216-1220, 2008.
- [57] C. Regard, C. Gautier, H. Fremont, P. Poirier, M. Xiaosong and K. M. Jansen, "Fast reliability qualification of SiP products," *Microelectronics Reliability, Volume*, vol. 49, no. 9-11, pp. 958-962, 2009.
- [58] A. Uddin, A. Wei and T. Andersson, "Study of degradation mechanism of blue light emitting diodes," *Thin Solid Films, Volume*, vol. 483, no. 1-2, pp. 378-381, 2005.
- [59] M. Fukuda, "Laser and LED reliability update," *Journal of Lightwave Technology, Volume*, vol. 6, no. 10, pp. 1488-1495, 1988.
- [60] D. Barton, M. Osinski, P. Perlin, C. Helms and N. Berg, "Life tests and failure mechanisms of GaN/AlGaIn/InGaIn light emitting diodes," in *Light-Emitting Diodes: Research, Manufacturing, and Applications II*, San Jose, CA, 1998.
- [61] C. Chen, M. Tsai, J. Tang, W. Tsai and T. Chen, "Determination of LED Die Strength," in *International conference of EMAP*, Daejeon, 2008.
- [62] J. Arnold, "When the Lights Go Out: LED Failure Modes and Mechanisms," DFR solutions, 2004.
- [63] M. Damann, A. Leuther, F. Benkhelifa, T. Feltgen and W. Jantz, "Reliability and degradation mechanism of AlGaAs/InGaAs and InAlAs/InGaAs HEMTs," *Physica status solidi (a)*, vol. 195, no. 1, pp. 81-86, 2003.
- [64] P. McCluskey, K. Mensah, C. O'Connor, F. Lilie, A. Gallo and J. Pink, "Reliability of commercial plastic encapsulated microelectronics at temperatures from 125°C to 300°C," in *Aerospace Conference Proceedings, 2000 IEEE*, Big Sky, MT, USA, 2000.

-
- [65] P. McCluskey, K. Mensah, C. O'Connor and A. Gallo, "Reliable use of commercial technology in high temperature environments," *Microelectronics Reliability, Volume*, vol. 40, no. 8-10, pp. 1671-1678, 2000.
- [66] E. Hong and N. Narendran, "A Method for Projecting Useful Life of LED Lighting Systems," *Proceedings of SPIE*, vol. 5187, pp. 93-99, 2004.
- [67] H. Qi, N. Vichare, M. Azarian and M. Pecht, "Analysis of Solder Joint Failure Criteria and Measurement Techniques in the Qualification of Electronic Products," *Components and Packaging Technologies, IEEE Transactions on*, vol. 31, no. 2, pp. 469 - 477, 2008.
- [68] M.-H. Chang, D. Das and M. Pecht, "Interconnect reliability assessment of high power Light Emitting Diodes (LEDs) through simulation," in *2nd International Conference on Reliability, Safety and Hazard (ICRESH)*, 2010.
- [69] "LUXEON Reliability, Reliability Datasheet RD25," Philips Lumileds, 2006.
- [70] X. Luo, B. Wu and S. Liu, "Effects of Moist Environments on LED Module Reliability," *Device and Materials Reliability*, vol. 10, no. 2, pp. 182-186, 2010.
- [71] A. Gladkov and A. Bar-Cohen, "Parametric dependence of fatigue of electronic adhesives," *Adhesive Joining and Coating Technology in Electronics Manufacturing*, pp. 116-124, 1998.
- [72] N. Shammass, "Present problems of power module packaging technology," *Microelectronics Reliability*, vol. 43, no. 4, pp. 519-527, 2003.
- [73] Y. Lin, N. Tran, Y. Zhou, Y. He and F. Shi, "Materials Challenges and Solutions for the Packaging of High Power LEDs," *Microsystems, Packaging, Assembly Conference Taiwan. IMPACT 2006*, pp. 1-4, 2006.

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