Integrated Schottky logic

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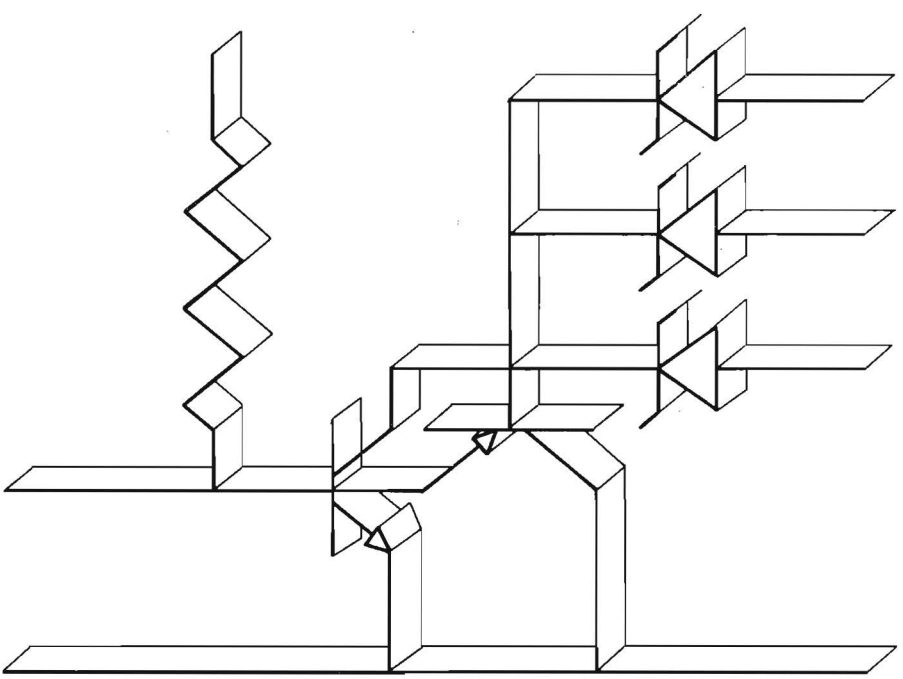

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INTEGRATED SCHOTTKY LOGIC

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PROEFSCHRIFT

TER VERKRIJGING VAN DE GRAAD VAN DOCTOR IN DE TECHNISCHE WETENSCHAPPEN AAN DE TECHNISCHE HOGESCHOOL EINDHOVEN, OP GEZAG VAN DE RECTOR MAGNIFICUS, PROF. IR. J. ERKELENS, VOOR EEN COMMISSIE AANGEWEZEN DOOR HET COLLEGE VAN DEKANEN IN HET OPENBAAR TE VERDEDIGEN OP VRIJDAG 13 NOVEMBER 1981 TE 16.00 UUR

DOOR

JAN LOHSTROH

GEBOREN TE 'S-GRAVENHAGE

DIT PROEFSCHRIFT IS GOEDGEKEURD
DOOR DE PROMOTOREN

prof.dr. F.M. Klaassen

en

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Aan Yolanda en Tjitske

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Eindhoven, November 1981.

Contents

1
General Introduction

Twenty years after the introduction of the first integrated circuit (which contained a few transistors in combination with a few passive elements) silicon integrated circuit technology has reached a very high level of perfection, resulting in I.C.'s with 10.000 transistors and an equal number of passive elements made in processes with economical production yields.

The process development has still not reached saturation level; in the future the integration of even 10^5 - 10^6 and perhaps more transistors on a chip, known as VLSI (= Very Large Scale Integration) and ULSI (= Ultra Large Scale Integration) are expected. The factors responsible for this dramatic expansion are:

a) continuing improvement in processes, partly due to the introduction of better chemical and physical processing steps, and partly due to elimination of first-order and second-order process variations; this is all made possible by expertise built up from the production of millions of I.C.'s (learning curve);
b) continuing improvement in photolithography and etching techniques, which means that device sizes can be decreased, resulting in a better packing density of the circuitry;
c) invention of new devices and circuits, which means that basic electronic functions can be performed with fewer or smaller basic elements (to improve the packing density) and/or at lower power dissipation level (which allows more functions on a chip).

Integrated Schottky Logic (ISL) is an example of the latter factor. It is a new bipolar logic concept that can be realized using existing processes. It combines device structures, which in fact were already known separately, with a very attractive type of logic gate which can be used for high speed VLSI.

This book discusses a large number of aspects of ISL, such as the original concept, its performance in different processes, switching speed (calculated and measured), first order modeling, its behaviour as a function of temperature, the noise margins as a func-

tion of temperature and its applications.

The next section entitled: "Aspects of Integrated Schottky Logic (ISL) and comparison with I^2L and STL", is an extensive introductory discussion to the contents of the book; for detailed information reference should be made to the subsequent sections, where reprints of already published papers and not yet published papers are given. These papers include an overview article on "Devices and circuits for bipolar (V)LSI" (where bipolar circuits are compared with MOS circuits in general, and where bipolar circuit/technology-combinations which satisfy VLSI requirements are discussed), and an article on "Static and dynamic noise margins of logic circuits" (where a general noise-margin test method is proposed, which is applicable to every type of logic circuit).

The subsections of section 2 and the corresponding section 3 to 12 are arranged in the following order: overview of devices and circuits for bipolar VLSI (section3), introduction to pn-isolated and oxide-isolated ISL (sections 4 and 5), comparison speed of ISL and I^2L (section 6), analytical expressions for propagation delay times (sections 7 and 8), modeling of pn-isolated and oxide-isolated ISL (sections 9 and 10), static and dynamic noise margins of logic circuits in general and of ISL in particular (sections 11 and 12), and the temperature behaviour of the static noise margins of ISL and STL (section 13). Appendix A discusses ISL applications and appendix B is a product specification of the 8A1200 ISL gate array.

2

Aspects of Integrated Schottky Logic (ISL) and Comparison with I^2L and STL

2.I. Introduction

Silicon integrated circuits are fabricated using two main-stream technologies: bipolar and unipolar circuits. In the last group we find the MOSFET, MESFET and JFET circuits. Anno 1981 both technologies (bipolar and unipolar) circuits employ lithography techniques allowing minimum details of 2-3 μm in standard production lines.

Production yields are high enough to obtain IC's with many thousands of transistors on an economical scale.

The two technologies differ in the electrical performance and packing density that can be obtained with the present 2-3 μm lithography rules. Except for I^2L, bipolar circuits, in general, exhibit higher speeds than unipolar circuits at the cost of a somewhat smaller packing density and/or a more complex technology, which means that the production yield of bipolar circuits per unit area tends to be lower than that of unipolar circuits. For this reason the minimum gate count in bipolar VLSI circuits is often taken to be a factor of two lower than the gate count in unipolar VLSI circuits (5000 and 10000 respectively).

2.II. Comparison between bipolar and MOS-type circuits

To obtain an electrical comparison between bipolar and MOS-type circuits the propagation delay times and power delay products will be discussed.

As explained in Section 3.II, the first order average propagation delay times for bipolar and MOS circuits are

$$t_{\text{dbipolar}} \approx \frac{(C_j + C_w)\Delta V}{i} + \frac{W_B^2}{2\mu kT/q} \tag{1}$$

$$t_{\text{dMOS}} \approx \frac{C_j(W) + C_w(W)}{(W/L)\mu C_{ox} V_T} + \frac{2L^2}{\mu V_T} \tag{2}$$

where C_j and C_w are junction and on-chip wiring capacitances, ΔV the logic swing, i the current per gate, W_B the basewidth of the bipolar transistor, W the width of the MOS transistor, L the gate length of the MOS transistor, C_{ox} the gate oxide capacitance per unit square, and V_T the threshold voltage of the MOS enhancement driver transistor. Fig. 1 shows a graphical representation of (1) and (2). The essential difference between (1) and (2) is that in the bipolar case the current per gate i is easily increased (a factor of 10 for every 60 mV more base-emitter voltage at room temperature) without increasing the transistor size, due to the exponential characteristic of the transistor. This means that when no limiting effects occur due to series resistances, the bipolar propagation delay time can be minimized to the transit time (which is of the order of $W_B^2/(2\mu kT/q)$ for a

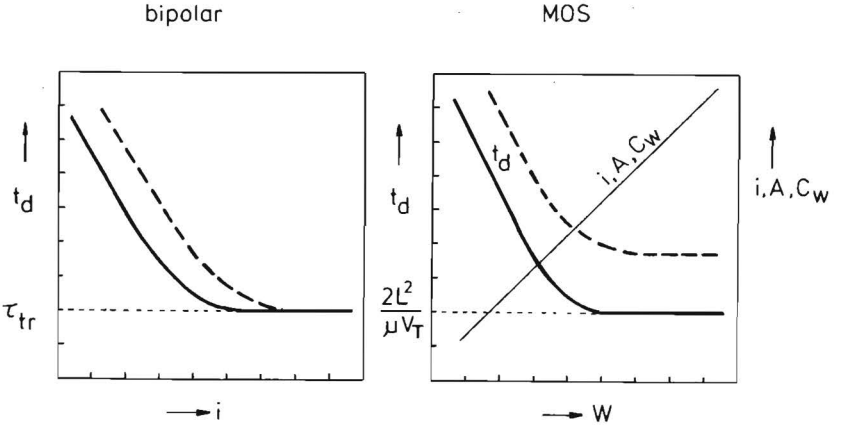

Fig. 1. Propagation delay times of bipolar and MOS circuits as a function of current per gate (in the bipolar case) or transistor width (in the MOS case). The solid line is without on-chip wiring capacitance; the dashed line is with on-chip wiring capacitance C_w.

normal bipolar transistor) by increasing i.

As the first-order average propagation delay time in the MOS case is independent of the power supply voltage, the only way to increase the speed (and the current) is to increase the transistor W/L ratio as shown by (2), which means that W has to be increased in a given technology where L had already been minimized. Thus transistors with a larger minimum width have to be used, thereby increasing the packing density and causing larger junction capacitances and larger on-chip wiring capacitances (both C_j and C_w depend on W). This implies that it is impossible to improve the speed any further if C_w increases linearly with W [1], and if C_w increased more than linearly with W, the propagation delay time would even increase. MOS type of circuits are therefore less suitable for high speed VLSI [2].

In GaAs where the first-order mobility μ (disregarding velocity saturation) is a factor of 5 higher than in silicon, smaller transistors can be used to obtain the same current.

This gives a higher packing density and consequently a smaller C_w, and thus the speed may be about the same factor of 5 higher. The GaAs technology, however, is not yet considered mature enough for LSI and VLSI circuits and the advantages still cannot be utilized on an economical scale [3].

Note that Fig. 1 shows only qualitative first-order effects. The theoretical minimum propagation delay times are different for different types of transistors. In non-saturated ECL circuits, τ_{tr} of the normal operated n-p-n transistor can be as low as $\tau_{tr} = W_B^2/(2\mu kT/q) = 20$ ps when the base width W_B is 0.3 μm. In the I^2L case where inverse operated n-p-n transistors are used τ_{tr} can be as large as 10 ns. In ISL, τ_{tr} is about 1.5 ns in the pn-isolated case and 250 ps in the oxide-isolated case. In MOS circuits with 3 μm minimum gate length $2L^2/\mu V_T$ is about 500 ps.

Another point to be made is that in practical bipolar circuits, including ISL, the theoretical minimum of the average propagation delay time is difficult to achieve due to series resistances (base series resistance, collector series resistance, Schottky diode series resistance) which limit peak currents which have to flow to charge and discharge capacitances (see Fig. 2). Also in MOS circuits the theoretical minimum of the propagation delay time is difficult to achieve due to the fact for instance that depletion loads in ED-logic do not behave as ideal current sources.

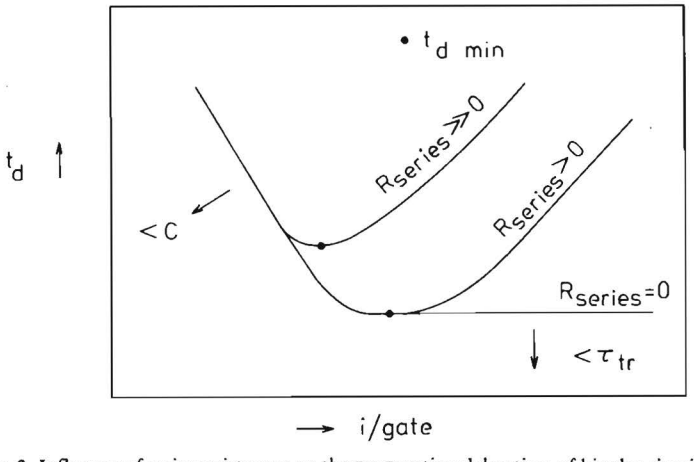

Fig. 2. Influence of series resistances on the propagation delay time of bipolar circuits.

So far only propagation delay times have been discussed. Another important figure of merit is the power-delay product $P_{td} = iV^+t_d$ which would be $V^+\Delta VC_w$, if the on-chip wiring capacitances were dominant (V^+ is the power supply voltage); see Section 3.II. For bipolar circuits the $V^+\Delta V$ product can be minimized to 0.2 V^2 irrespective of transistor size. For MOS type of circuits the same value can be obtained, but this

makes only sense for scaled devices ($L < 0.5$ μm), otherwise the speed will be disappointingly low.

Thus the advantages of bipolar circuits over MOS circuits are that: a) optimum speed can be obtained with minimum size transistors (disregarding series resistances), b) small voltage swings are possible (due to the exponential characteristics), resulting in a relatively small speed degradation due to on-chip wiring capacitances, c) V^+ and ΔV can be minimized independently of transistor size.

In Integrated Schottky Logic (ISL) where minimum-size transistors are always used, the logic swing is as low as 200 mV, and using resistors as current sources instead of p-n-p transistors the power supply voltage is about 1.5 V, which means that the $V^+\Delta V$ product is 0.3 V^2; thus a low power-delay product is obtained (only 0.1 V^2 more than the minimum possible).

Note that in this sub-section (and in Section 3) bipolar and MOS gates are only compared for speed and power-delay product and not for many other important properties such as packing density, wiribility, suitability for dynamic storage etc.

For instance MOS circuits with polysilicon gates have 2½ effective interconnection layers when using 1 layer metal, whereas in bipolar circuits 2 layers metal are needed to obtain the same interconnect possibilities. Another point is for instance dynamic storage, which is extremely simple in MOS circuits and very difficult in bipolar circuits.

This all means that bipolar circuits may be faster (gate-wise), but that they miss a lot of convenient properties which are available in MOS circuits.

2.III. Logic circuits for high speed bipolar VLSI

Nowadays most medium-size chip packages do not allow a higher power dissipation than about 1 W, and therefore, for most VLSI circuits with more than 5000 gates per chip the maximum power dissipation per gate has to be smaller than 200 μW.
Furthermore, with maximum chip areas of 25 mm^2, packing densities better than 200 gates/mm^2 are required.

Section 3.VIII examines the question as to which logic circuit/technology combinations fulfil these requirements. Only the most important logic types such as LS, I^2L, STL, ISL, DTL, ECL, and NTL are considered.

The result of the comparison is that in oxide-isolated processes with 3 μm minimum details, STL, ISL and I^2L satisfy the VLSI requirements, with about 1 ns average propagation delay time for STL and ISL, and about 5 ns for I^2L. ECL and DTL are VLSI candidates only in more sophisticated processes using polysilicon electrodes.

	pn-isolated 5 μm min. details	oxide-isolated 3 μm min. details
epithickness epithickness after all processing steps	2.9 ± 0.3 μm 2.4 ± 0.3 μm	1.2±0.05 μm 1.0 ±0.05 μm
ρ_{epi}	0.3 Ωcm	0.3 Ωcm
base x_{jB} base sheet res.	1.2 μm 200 Ω/□	0.5 μm 600 Ω/□
emitter x_{jE}	0.8 μm	0.25 μm
resistor x_{jR} resistor sheet res.	0.5 μm 2000 Ω/□	0.5 μm 2000 Ω/□
photoresist	neg./contact printing	pos./optical projection
min. emitter mask size	5 × 8 μm^2	3 × 5 μm^2
1st metal mask width/spacing 2nd metal mask width/spacing	5 μm/5 μm 10 μm/14 μm	3 μm/5 μm 11 μm/5 μm
via's (mask)	8 × 10 μm^2	5 × 7 μm^2
alignment tolerance	3 μm	1 μm

Table 1. Most relevant process parameters of processes in which ISL has been made.

2.IV. Bipolar processes for ISL

Section 3.IV-VII gives an extended survey of production and experimental processes for bipolar LSI and VLSI circuits. ISL has been made in existing production processes only. Initially, the pn-isolated SBC process (Standard Buried Collector) was used with a 3 μm thick epitaxial layer and 5 μm minimum dimensions; later an oxide-isolated process was used with a 1.2 μm thick epitaxial layer and 3 μm minimum dimensions. Details of these processes are given in Section 8 and Section 10 respectively; table 1 lists the most important numbers.

In both processes Schottky diodes are made with PtNi-silicide (60% Pt and 40% Ni) with a barrier height of about 0.78 eV.

2.V. The original concept of ISL

ISL was initiated to fill the gap between low-power Schottky TTL and I^2L without changing the technological standard process, for those circuits where low-power Schottky TTL consumes too much power and takes up too much chip area, and when I^2L does not attain the required speed [4,5,6] (see Section 4). In fact, ISL is a compromise between Schottky-diistor logic [7] (also called Schottky Coupled Transistor Logic (SCTL) [8]) which is made in a process with one type of Schottky diode, and Schottky Transistor Logic [9] (also called Complementary Constant Current Logic (C^3L) [10]) which is made in a process with two types of Schottky diode. The electrical diagrams of Schottky-diistor logic, STL and ISL are shown in Fig. 3; all p-n-p transistors are used in the standard downwards mode. All these logic types are of the wired-AND type; they have one input and a multiple output. The disadvantage of Schottky-diistor logic is that it becomes heavily saturated which means that it is rather slow. STL, on the other hand, is Schottky clamped and consequently relatively fast, but has the disadvantage that the process in which it has to be made is much more complex due to the fact that two types of Schottky diodes have to be made with different barrier heights (a high barrier for the clamp diode and a low barrier for the output diodes) to obtain a reasonably large voltage swing.

In ISL the clamp action is provided by a p-n-p transistor (see Fig. 3); the n-p-n still goes into saturation, but as soon as the n-p-n base-collector junction is forward biased the superfluous base current is drained to ground by the p-n-p transistor which means that the n-p-n transistor goes less far into saturation.

The effectiveness of a p-n-p transistor as a fast clamp device depends mainly on the minority carrier storage in its base, hence the base width has to be small.

Fig. 4 shows a top view and cross section of an ISL gate made in a standard pn-isolated process. A vertical clamp p-n-p is obtained by not extending the buried layer under the base-contact of the n-p-n transistor. The parasitic lateral p-n-p action to the

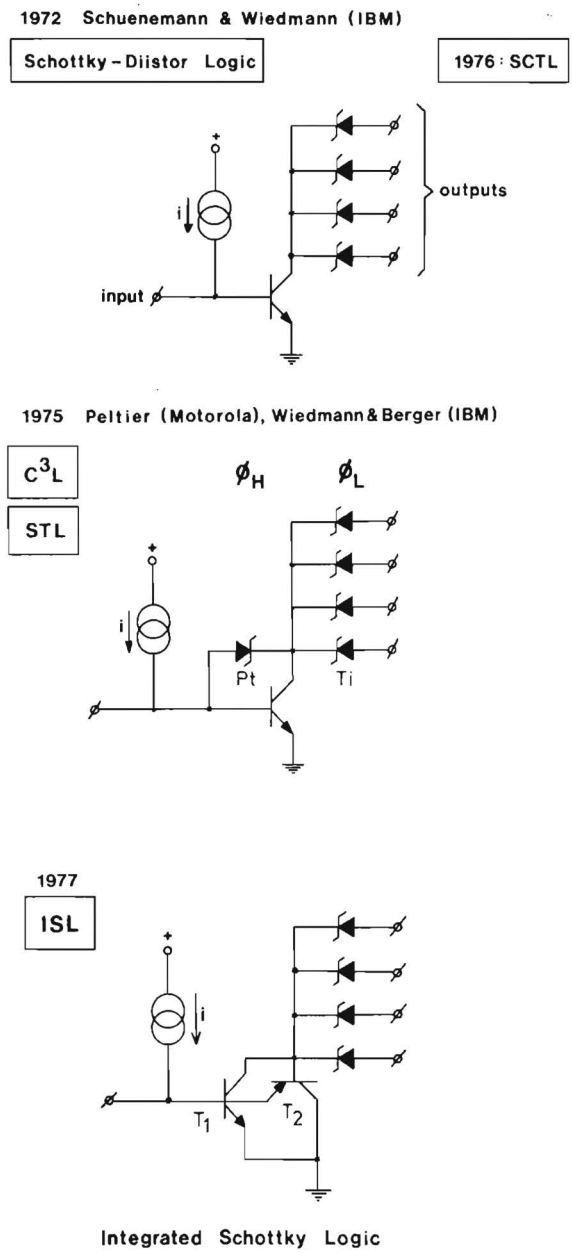

Fig. 3. Circuit diagrams of Schottky-diistor logic or SCTL [7,8], STL or C^3L [9,10], and ISL.

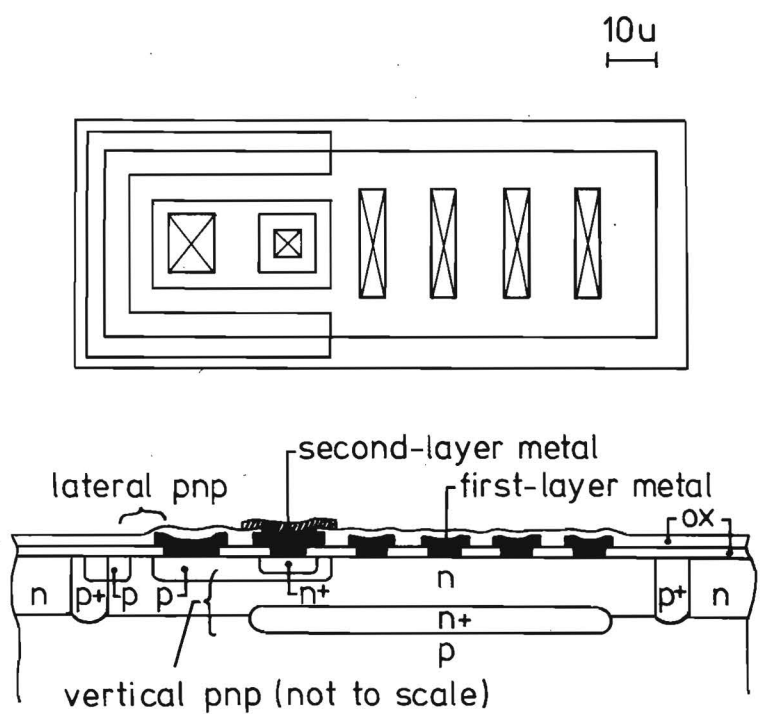

Fig. 4. Top view and cross-section of a pn-isolated ISL gate without current source; 5 μm minimum details are used.

isolation diffusion is inevitable in pn-isolated processes.

To reduce the minority carrier storage in these lateral areas, the lateral p-n-p base width is reduced by the application of a shallow isolation-diffusion overlapping p-ring at a minimum-detail distance around the p-base (5 μm for instance).

The base thickness of the vertical p-n-p is determined by the thickness of the epitaxial layer; the thinner this epilayer, the faster the logic is.

A p-n-p clamp transistor has been proposed to control the saturation in an I^2L type of structure [11], but to implement a merged clamp p-n-p with an inverse operating n-p-n, requires a dramatic deviation from the standard process [11].

Although ISL is, in principle, a wired-AND type of gate (see Fig. 5(a)), the extra internal collector node (which does not exist in I^2L) makes collector dotting possible to obtain NOR functions and also AND TO OR NOT functions (see Fig. 5(b,c)). Collector dotting is obtained either by placing more base areas in one collector island, or by interconnection of more collector islands with n^+ collector contacts and an interconnect wire.

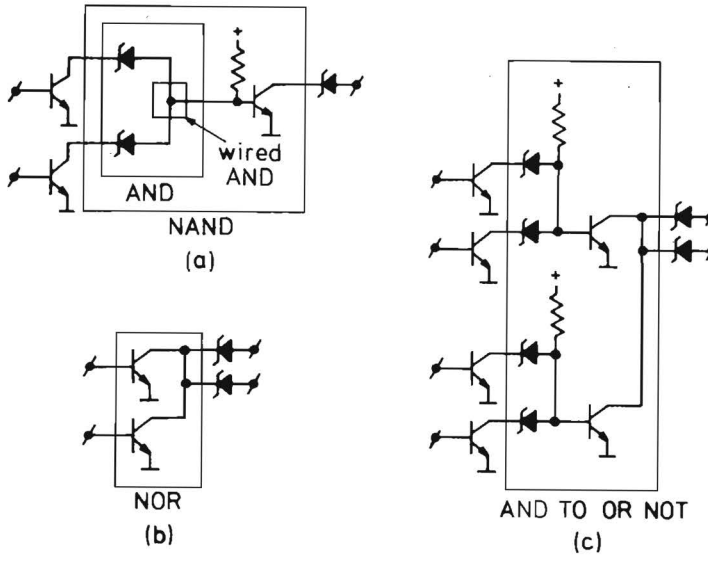

Fig. 5. (a) Wired-AND construction to obtain AND and NAND functions, (b) collector dotting to obtain NOR functions, (c) combination of a and b to obtain AND TO OR NOT functions.

2.VI. Performance of pn-isolated ISL

As the n-p-n transistor in ISL is used in the normal (downward) mode, the current source cannot be merged with this transistor as in I^2L [12,13]. Either a separate transistor or a resistor in a separate island has to be made. This means that the packing density is about 30% lower than in I^2L. The logic voltage swing is $\Delta V = (kT/q)\ln(\alpha_{p\text{-}n\text{-}p} I_{d0}/I_{p0})$, where I_{d0} and I_{p0} are the saturation currents of the Schottky diode and the p-n-p transistor respectively. In processes with an epilayer thickness of about 3 μm and PtNi-silicide diodes (ϕ_B = 0.78 eV) and using 5 μm minimum details (see Fig. 4) a logic swing of 200 mV is obtained. With resistors as current sources, and washed emitters, a minimum average propagation delay time of 2.7 ns at 200 μA/gate is obtained (see Fig. 6). Despite a voltage swing which is about 500 mV smaller than that of I^2L, most of the ISL noise margins are larger than those of I^2L. The main reasons, as explained in chapter 2.XV, are that the current source is a resistor instead of a saturated p-n-p transistor (this improves the power supply line and ground line noise margins) and that the current gain of the normal operating n-p-n is generally much higher than the current gain of the inverse operated n-p-n (this improves the parallel current noise margin). This makes the ISL a more "forgiving" circuit than I^2L [4].

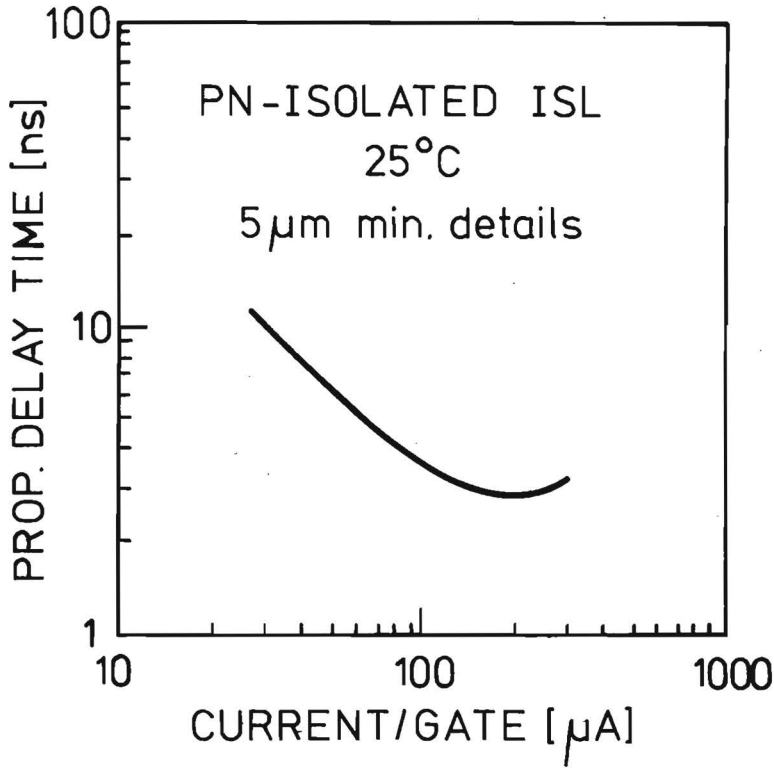

Fig. 6. Average propagation delay times of the ISL gate of Fig. 5. The epilayer thickness is 2.9 μm; the current sources are ion-implanted resistors.

As the ISL gates are made in a standard buried collector process, they can easily be combined with I^2L, low-power Schottky TTL and ECL on the same chip. Even in analog processes with thicker epilayers, ISL has been demonstrated to have a 5 to 10 times better speed than I^2L.

2.VII. Oxide-isolated ISL technologies

Using oxide isolation, ISL gates can be fabricated without the relatively slow lateral p-n-p transistor which is inevitable in pn-isolated processes. As shown in Section 5, the clamping action is provided either by a fast vertical p-n-p only, or a reverse operated n-p-n (see Fig. 7 and 8); a 1.2 μm thick epilayer and 3 μm min. dimensions are used. Fig. 9 shows t_{pd} as a function of current per gate for type A (vertical p-n-p clamp) and type B (reverse operated n-p-n clamp). Type A is the most successful one; t_{pd} is about 0.7 ns at a current level of 200 μA/gate ($t_{pd}D \approx 0.2$ pJ). The reason why type B is slower is due to the fact that the saturation current of the minimum size inverse n-p-n is about a factor of

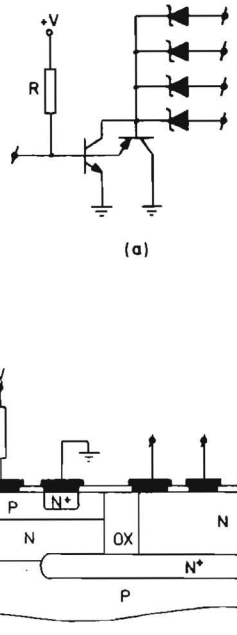

Fig. 7. Oxide isolated ISL with a vertical p-n-p clamp.

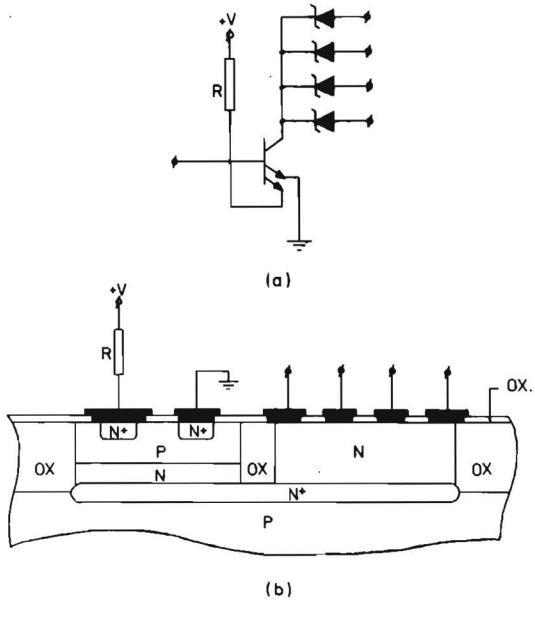

Fig. 8. Oxide isolated ISL with reverse operated n-p-n clamp.

5 smaller than the saturation current of the vertical p-n-p. This means that the normal operated n-p-n becomes much more heavily saturated than with p-n-p clamping, causing much more hole storage in the n-epilayer underneath the base. The speed could be improved by increasing the size of the inverse n-p-n transistor, but the improvement may be small if the size of the total structure then needs to be increased (which would cause an increase in base-collector capacitance and an increase in island capacitance).

Using a small size vertical p-n-p clamp therefore ISL has been realized in a standard oxide-isolated process, featuring sub-nanosecond propagation delay times with sub-picojoule speed-power products. This makes this type of logic very attractive for high speed VLSI. Oxide-isolated ISL has also been tested by others with 5 μm details [14] and even 1.25 μm details [15]; in the last case t_{pd} = 0.7 ns at 100 μA/gate was reported.

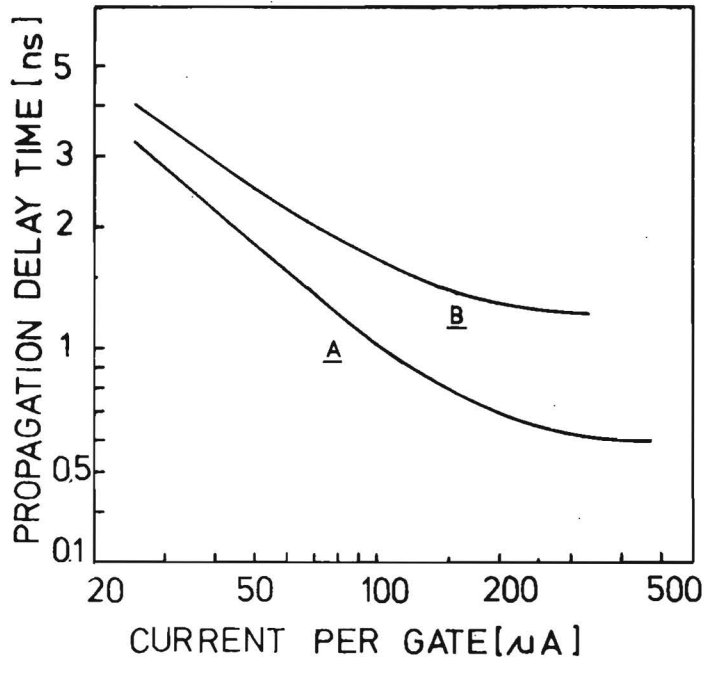

Fig. 9. Measured propagation delay times of oxide isolated ISL with vertical p-n-p clamp (A) and reverse operated n-p-n clamp (B).

2.VIII. Speed comparison of ISL and I^2L

As already mentioned, the minimum average propagation delay time of ISL is a factor of 5 to 10 better than the speed which can be obtained with I^2L in the same process. This is explained in Section 6.

For comparison, ISL and I^2L gates are considered which are made in the same process with the same epilayer thickness and the same minimum dimensions, see Fig. 10.

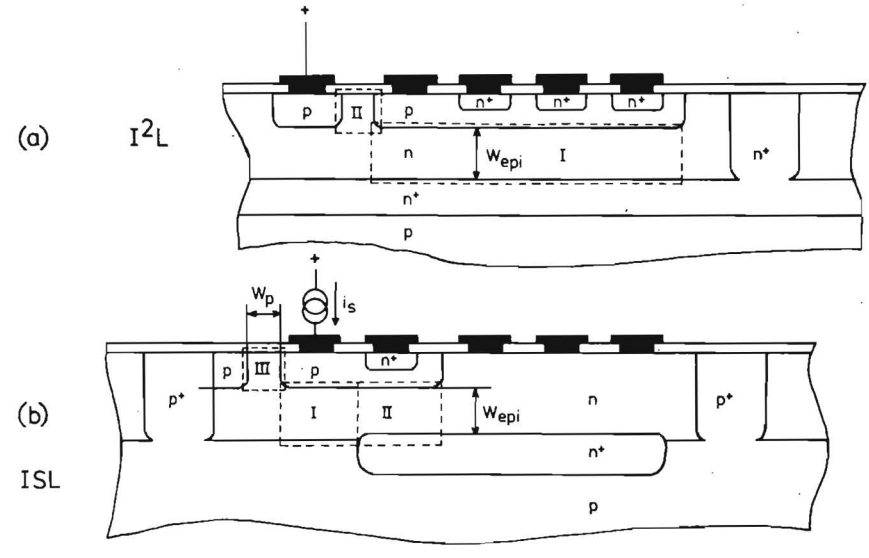

Fig. 10. Cross-section of I^2L (a) and ISL (b) made in the same pn-isolated process. Active charge will be found mainly in areas I and II (I^2L) and I, II and III (ISL).

For small currents ISL will be faster than I^2L because of the smaller voltage swing (200 mV instead of 700 mV), whereas the junction capacitances are comparable.

At high current levels, at maximum speed, the active charges dominate. It is characteristic of I^2L that the active charge is found mainly in the n-p-n emitter area (see Fig. 10(a)), whereas in ISL the active charge is found mainly in the n-p-n collector area (= p-n-p base) because of the saturation of the n-p-n (see Fig. 10(b)). These active charges can be represented by non-linear capacitances between base and emitter in I^2L and between base and collector in ISL (see fig. 11(a) and 12(a) respectively). As shown in Section 6, the ratio of the intrinsic current-independent average propagation delay times of I^2L and ISL is about $2\sqrt{\beta_{\text{upeff}}}\, f_{T\ \text{PNP ISL}}/f_{T\ \text{NPN up I}^2\text{L}}$.

For processes where W_{epi} is 2 μm, $f_{T\ \text{PNP ISL}}$ and $f_{T\ \text{NPN up I}^2\text{L}}$ are both about 15 MHz. Fig. 11(b) shows for this case the typical switching behaviour of I^2L when $\beta_{\text{up eff}} = \beta = 4$ and $f_{T\ \text{NPN up I}^2\text{L}} = 15$ MHz.

The transient behaviour of the currents illustrated is obtained with a computer simulation program. At $t = 0$ the switch is opened and TN1 starts to conduct. The collec-

tor cirrent of TN1 increases relatively slowly: $i_{c1} = \beta i_{c1}[1 - \exp(-t2\pi f_T/\beta)]$.

It takes a relatively long time to discharge Q_2 due to the fact that TN2 is heavily saturated. After 30 ns TN2 is no longer saturated and it takes another 7 ns to completely switch OFF TN2. So the average propagation delay is 37/2 = 18.5 ns.

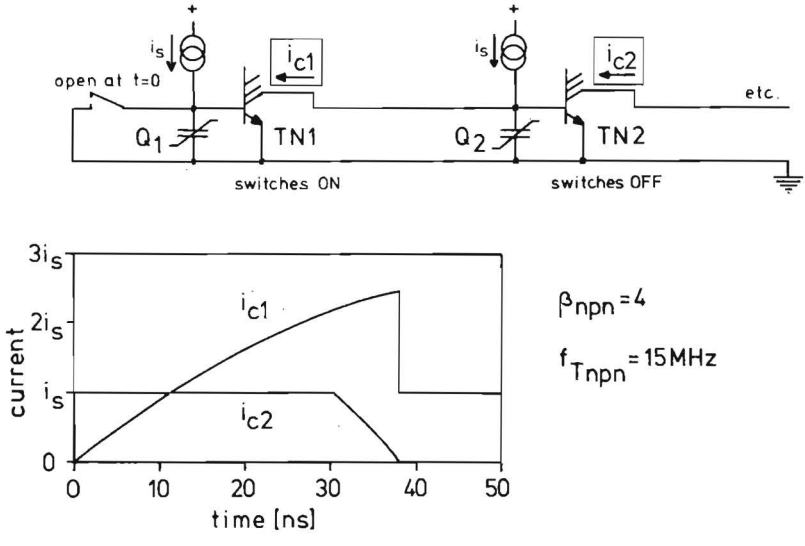

Fig. 11. Inverter chain made with I²L (a) and the behaviour of i_{c1} and i_{c2} as a function of time (b).

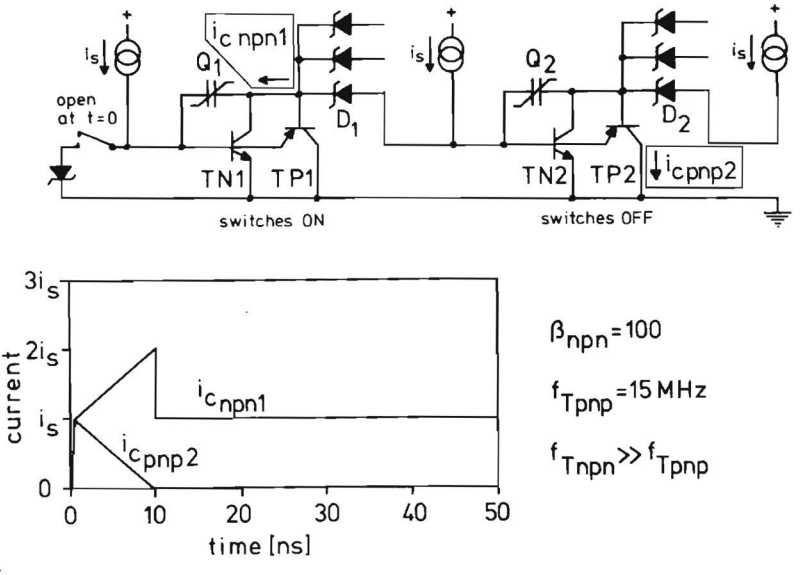

Fig. 12. Inverter chain made with ISL (a) and the behaviour of $i_{cn\text{-}p\text{-}n1}$ and $i_{cp\text{-}n\text{-}p2}$ as a function of time (b).

Fig. 12(b) shows the ISL case with $f_{T\ PNP\ ISL} = 15$ MHz. We assume that $f_{T\ NPN} \gg f_{T\ PNP}$. In this case, shortly after $t = 0$, TN1 can sink any amount of current up to $i_{cmax} = \beta_{n\text{-}p\text{-}n} i_s$. This maximum current will not be reached since the discharge path to remove Q_2 goes through the fan-out diode D2 and is limited to i_s.

This means that $i_{c\ p\text{-}n\text{-}p2}$ decreases linearly ($i_{c\ p\text{-}n\text{-}p2} = i_s\,(1 - t2\pi f_{T\ PNP})$) and $i_{cn\text{-}p\text{-}n1}$ increases from i_s to $2i_s$ with the same amount. The charge Q_2 is thus removed in about 10 ns and so the average propagation delay time in this particular ISL-case is 5 ns (compare with 18.5 ns in the I^2L case).

Measurements of I^2L and ISL made in the same process show about the same or an even larger factor in maximum speed, because in most cases $f_{T\ NPN\ ISL} > f_{T\ NPN\ up\ I^2L}$.

2.IX. Propagation delay time of I^2L at low current levels

Before the propagation delay times of ISL and STL are calculated (for low and intermediate current levels), first the propagation delay time of I^2L at low current levels is calculated, because with its simple electrical diagram it gives a convenient introduction to the more complicated ISL/STL case.

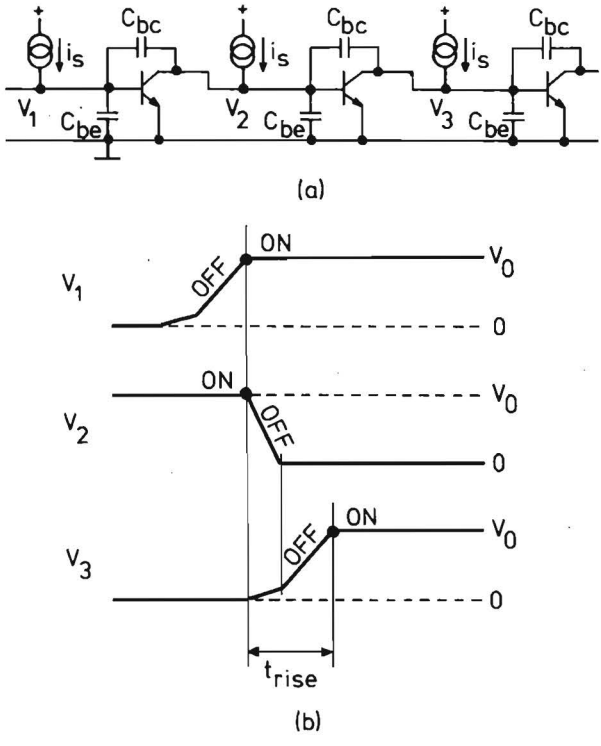

Fig. 13. Chain of I^2L inverters (a) and the behaviour of the node-voltages as a function of time (b).

As shown in Section 7, the calculation of the I^2L case is relatively simple due to the low number of electrical nodes, see Fig. 13(a). For the calculation the following simplification is introduced: the transistor is assumed to be ON as soon as V_{be} reaches it maximum value $V_{bemax} = V_0$, and OFF when $V_{be} < V_0$ (see Fig. 13(b)). This simplification is justified by the exponential current/voltage characteristic of the transistor, and also verified by computer simulations. It implies that V_3 and V_5 start to decrease and increase respectively *at the same time* when V_1 reaches V_0; this means that the average propagation delay time is equal to $t_{rise}/2$ when $t_{rise} > t_{fall}$ (see Fig. 13(b)). It is shown in Section 7 that $t_{rise} > t_{fall}$ in a 3-stage ring oscillator when $\beta_{eff} > 2$ and that t_{rise} is equal to $(3C_{bc} + C_{be})V_0/i_s$. In ring oscillators which have more than 3 stages β_{eff} is permitted to be somewhat lower than 2; with an infinite number of stages β_{eff} can be very close to 1.

2.X. Propagation delay times of ISL and STL at low and intermediate current levels

The calculation of the propagation delay times of ISL and STL at low current levels is more difficult than of I^2L due to the fact that ISL and STL have more electrical nodes than I^2L (compare Fig. 14 with Fig. 13(a)).

As shown in Section 8, the voltage swing at the internal nodes V_2, V_4, etc. is twice as large as the voltage swing at the input/output nodes V_1, V_3, V_5, etc.

Here the propagation delay time is not determined only by t_{rise} of the input node, because V_5 does not start to rise immediately after V_1 has reched V_{bemax}, due to the fact that the internal node V_2 first has to be discharged sufficiently to forward biase D1 and to switch OFF T2 (V_5 starts to rise when $V_3 < V_{bemax}$). The average propagation

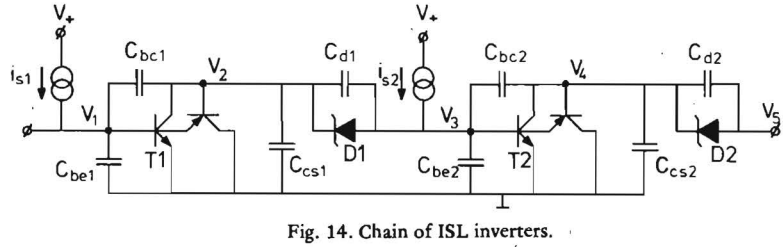

Fig. 14. Chain of ISL inverters.

delay time is now determined as $t_{charge}/2$ where t_{charge} is t_{rise} plus the times it takes to decrease the voltage of the next internal node to switch OFF the subsequent n-p-n transistor. As the internal node voltages do not reach their eventual DC-level, an exact expression for t_{charge} is difficult to derive. With empirical factors a reasonable approximation is obtained for instance for a 21-stage ring oscillator:

$t_{charge} = (4.0\,C_{bc} + 1.3\,C_{cs} + C_{be})\,\Delta V/i_s$, where ΔV is the voltage swing.

As shown in Section 8, the average propagation delay times of ISL and STL are very similar at low current levels; at intermediate current levels, the intrinsic average propagation delay time of ISL being about $\alpha^* \tau_p^*/2$ has to be added in the ISL case only (α^* is

the effective α of the p-n-p transistor; τ_p^* is the effective forward transit time of the p-n-p with the active charge stored in the n-p-n-collector added to the charge stored in the p-n-p base). At high current levels the propagation delay times of both ISL and STL are increased by series resistance effects. It is shown by calculation and measurements that, when compared in pn-isolated processes with 3 μm epilayer, the speed difference, at intermediate and high current levels between ISL and STL can be quite large due to the relatively high value of τ_p^*.

This high value of τ_p^* (1.5 ns) is caused both by the relatively thick epilayer and by the presence of the relatively slow lateral p-n-p. In oxide isolated processes with a thinner epilayer, τ_p^* is much smaller (250 ps), also because the lateral p-n-p, which is inevitable in pn-isolated processes, is fully eliminated. In an oxide isolated process with 3 μm minimum details $t_{pd\ ISL}$ and $t_{pd\ STL}$ are about 0.95 ns and 0.75 ns respectively at 100 μA/gate.

2.XI. Fan-in and Fan-out aspects of ISL and STL

Both ISL and STL suffer from speed degradation due to fan-in. Fan-out, in general, has a speeding-up effect. In real logic circuits combinations always occur, and thus that speed degradation due to fan-in may be compensated or partly compensated by speed improvement due to fan-out. Nevertheless, critical paths are always found where speed degradation due to fan-in is dominant, so this determines the worst case situation. Fig. 15 shows the effect. Here the fan-in is F_i, and n gates switch OFF simultaneously. Now the current source i_s has to charge more than one base-collector capacitance (C_{bc}) and island capacitance (C_{cs}). In Section 8 expressions are derived for t_{pd} where this fan-in effect is

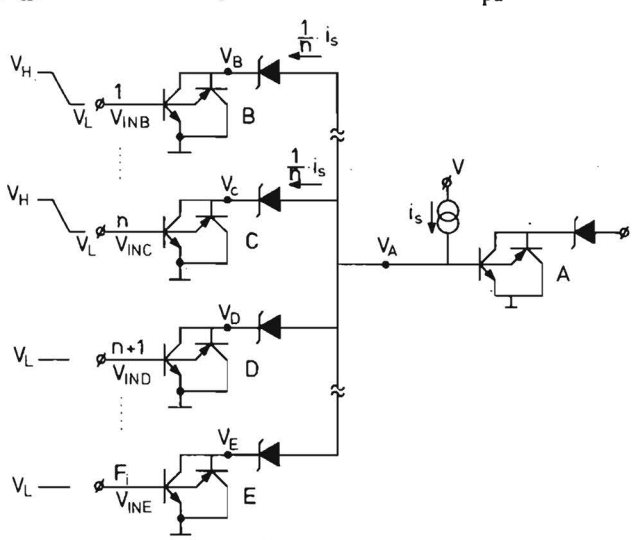

Fig. 15. ISL situation with fan-in > 1. The current source has now to charge more capacitance if n input gates switch OFF simultaneously.

included. Measures of obtaining delay times that are independent of fan-in are also discussed. One of them is to use dummy gates as shown in Fig. 16. Here the speed improvement of fan-out is used to compensate a speed degradation of fan-in.

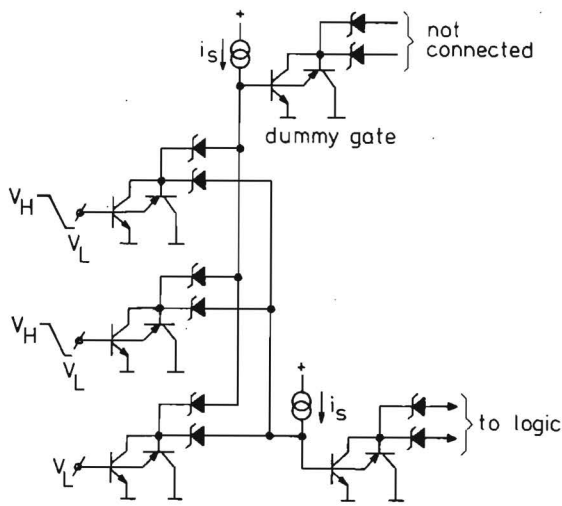

Fig. 16. A dummy gate is used to compensate the speed degradation due to fan-in.

2.XII. Performance, temperature behaviour and first-order modeling of ISL

So far analytical expressions for the average propagation delay time have been derived, where series resistances and non-linearities of capacitances have been ignored. With an appropriate model and a circuit simulation program the more refined behaviour of the gate can be studied.

Fig. 17 shows a complete model of pn-isolated ISL, including all series resistances, junction capacitances and non-linear diffusion capacitances (minority carrier storage). The p-n-p is split into two parts, the lateral and the vertical one. Fig. 18 shows a to-scale cross section of the lateral p-n-p, the vertical p-n-p and n-p-n transistors. The depletion layers and hole distributions are indicated. Hole storage is found in three regions: in the base of the lateral p-n-p, in the base of the vertical p-n-p and in the collector of the n-p-n. The storage is calculated from all junction depths, and forward and reverse transit times for the n-p-n, and both p-n-p's are derived. Beta's of transistors are measured and capacitances are measured and/or calculated. In Section 9 it is shown, both by measurements and simulations, that the voltage swing decreases with increasing temperature due to the different temperature coefficients of the base-emitter voltage of the combined p-n-p's and of the anode-cathode voltage of the Schottky diodes. At room temperature the voltage swing is about 200 mV; at 150°C the swing is reduced to about 150 mV.

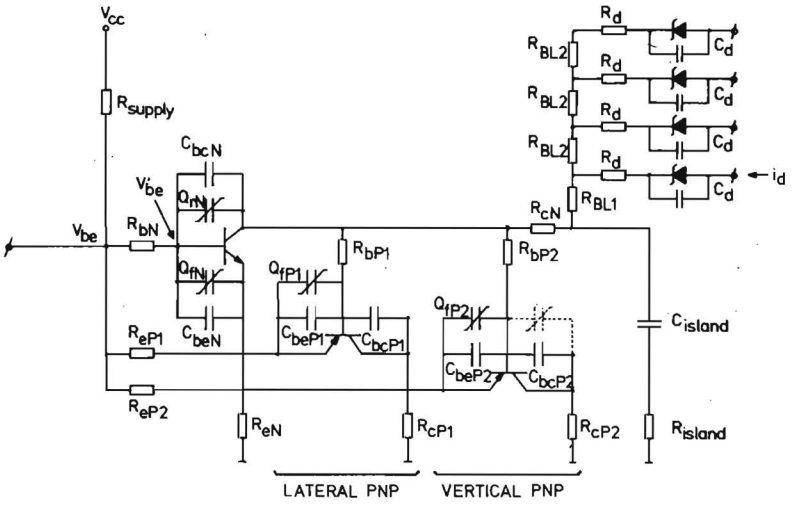

Fig. 17. Complete model of pn-isolated ISL.

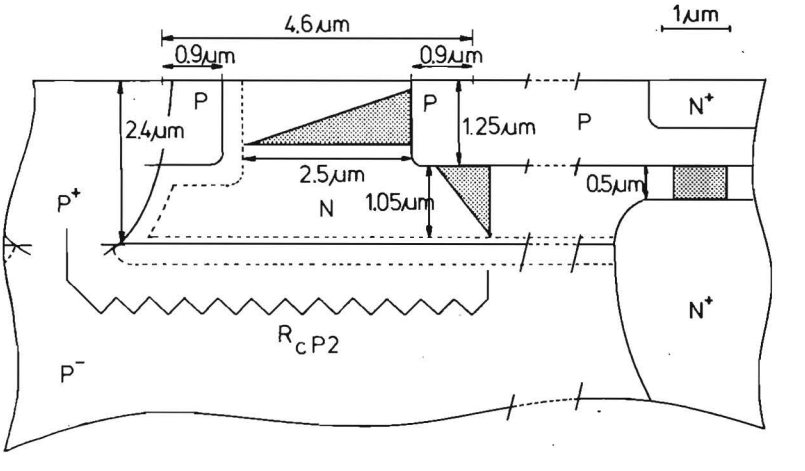

Fig. 18. To-scale cross-section of a typical pn-isolated ISL gate. Minority carrier storage is indicated.

It is further evident from measurement that the vertical p-n-p has a very large collector series-resistance of 8 kΩ at room temperature when ISL is processed in the original low-power Schottky TTL process with a substrate resistivity of 5-14 Ω•cm. Moreover, this resitance has a very high temperature coefficient which means that the series resistance increases to 16 kΩ at 150°C. The consequence is that, already at inter-

mediate current levels, the vertical p-n-p goes into saturation, causing a dramatic increase in the propagation delay time (see Fig. 19). The only way to get rid of this effect is to decrease the resistivity of the substrate below 5 Ω•cm at the cost of higher island capacitance of the n-p-n. Using the higher doped substrate (called ISL process) therefore the average propagation delay time at low current levels will be somewhat higher than in the LS-process, but the minimum t_{pd} is much lower, due to the elimination of the saturation of the vertical p-n-p (see Fig. 19). The intrinsic delay time being $\tau_p^*/2$ is 750 ps. As explained in Section 9, all results are obtained with minimum design rules of 5 μm causing a lateral p-n-p base width of 2.5 μm. It may be asked whether a similar performance with a similar delay time could be obtained with a lateral p-n-p only. Of course this would be possible, but then the base width of the lateral p-n-p would have to be 0.7 μm, which means that instead of 5 μm, 2.8 μm minimum details would have to be used in the same process. However, for standard production lines this value is much too small.

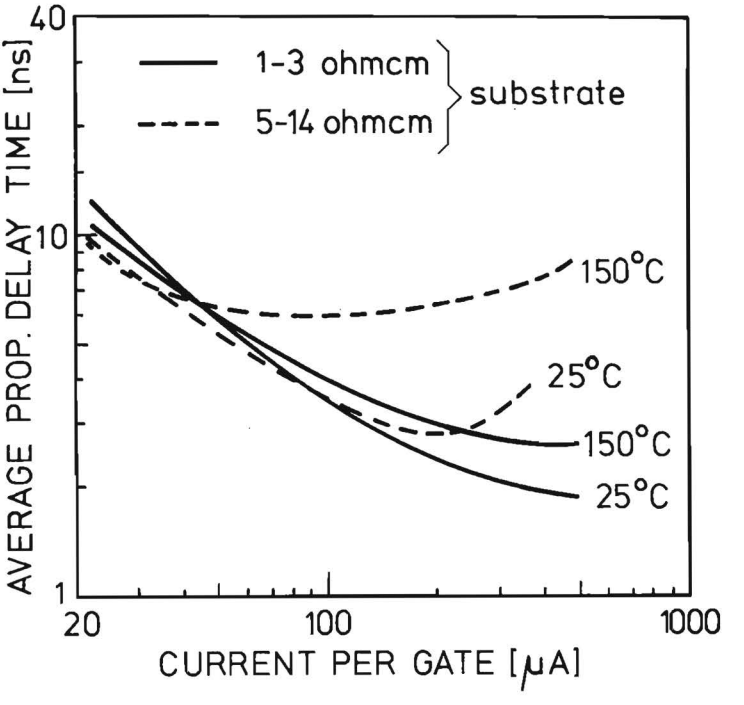

Fig. 19. Average propagation delay times of ISL made on a 5-14 Ω•cm substrate (dashed lines) and on a 1-3 Ω•cm substrate (solid lines).

2.XIII. First-order modeling of oxide-isolated ISL

Oxide-isolated ISL, in the p-n-p clamped version, can be modeled in a similar way to pn-isolated ISL. As the lateral p-n-p does not exist, the most simple model would contain only one n-p-n transistor and one p-n-p transistor to model the merged n-p-n/p-n-p structure. However, in oxide isolated processes with a thin epilayer, a very shallow base diffusion (0.5 μm) and a very shallow emitter (0.25 μm), the base series resistance tends to be very high, especially in cases where the emitter is oxide-walled on two sides. This causes a relatively large voltage drop across this resistance and the base collector junction thus injects more holes outside the intrinsic n-p-n region than inside the intrinsic n-p-n region when the transistor goes into saturation. As a first-order approximation all hole injection is modeled by a diode, and the hole storage under the n-p-n is then assumed to occur as a result of lateral flow of holes (see Fig. 20). Fig. 21 shows the complete model derived in Section 10. All parameters for this model are obtained from measurements and calculations. Due to the p^+ channel stop in the process, the collector series resistance of the clamp p-n-p is relatively small ($\sim$ 1.5 kΩ), which means that low doped substrates can be used. It is shown that, already at 100 μA/gate, series resistances affect the propagation delay time seriously. Without series resistances t_{pd} would have been 0.8 ns instead of the measured value of 1 ns (at room temperature). Simulations have shown that the relatively high base-series-resistance of the n-p-n causes the largest speed degradation. Special attention is paid to all temperature coefficients of the device parameters, to obtain a good agreement with the measurements in the temperature range from 25°C to 125°C.

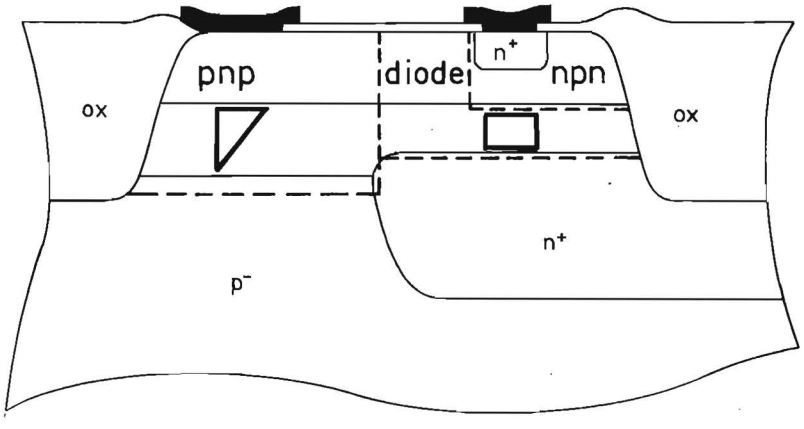

Fig. 20. Subdivision of the merged transistor structure in oxide-isolated ISL into a p-n-p, a diode and an n-p-n transistor. The hole storage under the base of the saturated n-p-n is associated with the diode. Hole storage is indicated for the p-n-p (triangle) and diode (box).

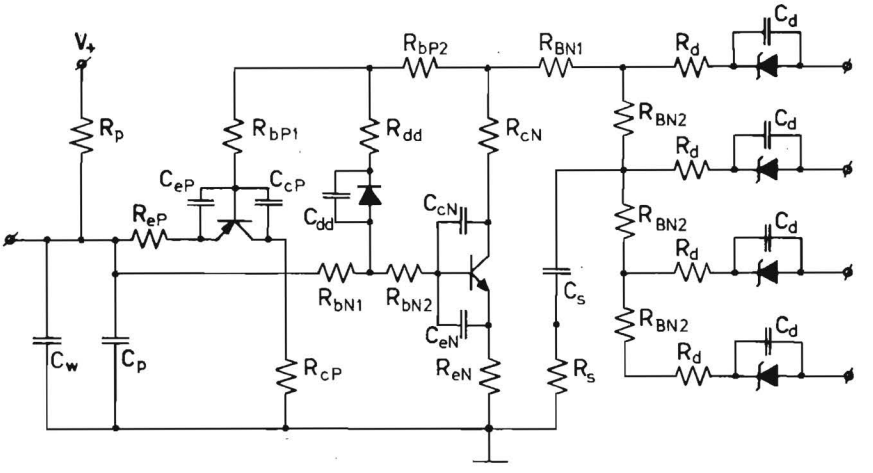

Fig. 21. Complete model of p-n-p clamped oxide-isolated ISL.

2.XIV. Static noise margins of logic circuits

The noise margins of logic circuits are often the subject of confusion because there are different types of noise, and the worst case situations depend on fan-in, fan-out and the way the noise sources are applied.

In Section 11 it is shown that four basic noise sources can be considered: series--voltage noise (δV_{series}), parallel-current noise (δi), voltage noise at the ground line (δV_{gnd}) and voltage noise at the power-supply line (δV_{supply}). When identical noise sources of opposite sign in the even and odd stages of an infinitely long chain put this chain on the very edge of switching to the wrong state, the amount of noise is considered the worst case noise margin Δ ($\Delta = \delta_{max}$). Instead of an infinitely long chain, a flip-flop (made with two inverters) can also provide the same result [16]. When the often disregarded condition that the output impedance of a gate is very much smaller than its input impedance ($R_{out} \ll R_{in}$) is satisfied, ΔV_{series} can be found using the maximum square method of the voltage transfer characteristics of the logic gate [16]; see Fig. 22.

To explain what happens in a flip-flop, Fig. 23 shows series voltage noise in a fan-in = fan-out = 1 flip-flop. It is assumed that $R_{out} \ll R_{in}$. When the noise sources are incorporated in gate 1 and gate 2, overall transfer characteristics can be obtained (for gate I and gate II respectively). Fig. 24(a) shows the two transfer characteristics when $\delta V_{series} = 0$. There are three states: two stable states where the small signal voltage loop-gain $A^* = (dV_2/dV_1)_I \cdot (dV_1/dV_2)_{II}$ is smaller than 1 (at cross points A and C) and a metastable state where $A^* > 1$ (at cross point B). Let us assume that the flip-flop is in the stable state A and the noise amplitude starts to increase. In Fig. 24(b) the intermediate

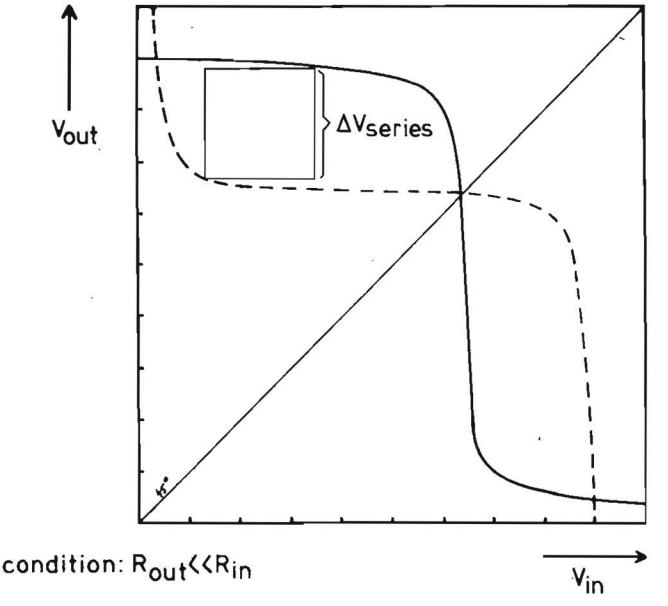

Fig. 22. Determination of the worst-case series voltage noise margin ΔV_{series} of an inverting gate, when $R_{out} \ll R_{in}$, by mirroring the voltage transfer characteristic and by finding the maximum square which fits between the characteristics [16].

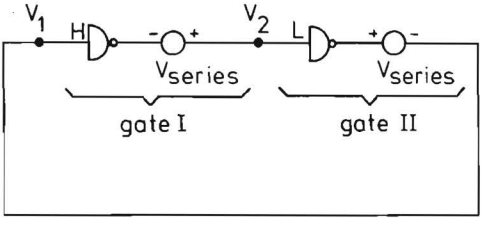

Fig. 23. Flip-flop built up with two identical gates, disturbed by series voltage noise sources δV_{series}.

situation is shown where $0 < \delta V_{series} < \Delta V_{series}$; the transfer characteristics are shifted but the flip-flop still remains at point A (at this point the loop gain has increased but is still smaller than 1). In Fig. 24(c) the noise margin ΔV_{series} is reached; points A and B merge together (B = A) and at this point the loop gain is exactly 1. When δV_{series} is made larger than ΔV_{series} the flip-flop switches to state C.

In cases where R_{out} is not much smaller than R_{in}, the voltage transfer characteristics have no relevance any more, because the output voltage depends now both on R_{out}

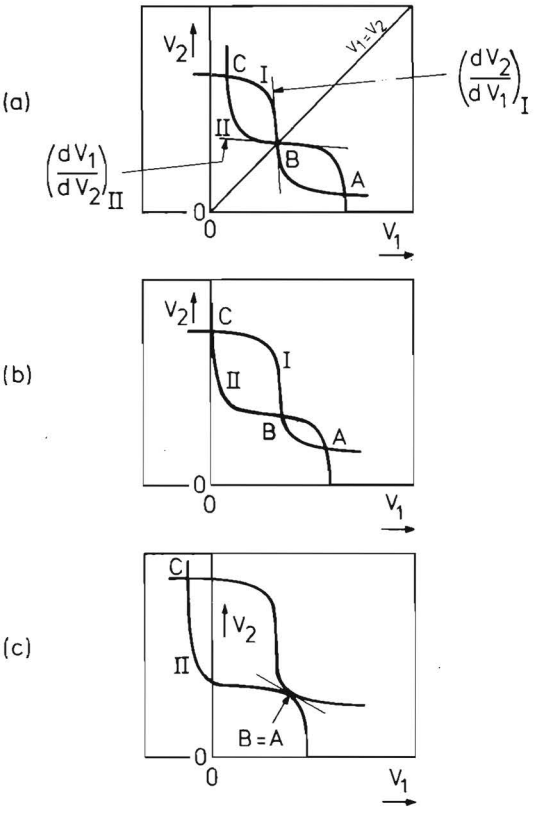

Fig. 24. Transfer characteristics of the gates I and II of Fig. 23 for different values of δV_{series}; (a) $\delta V_{series} = 0$, (b) $0 < \delta V_{series} < \Delta V_{series}$ and (c) $\delta V_{series} = \Delta V_{series}$. In the last case the small signal voltage loop gain is 1.

and R_{in}. In this case the noise margin can be found as the amount of noise which has to be applied to achieve a situation in which both small signal voltage and small signal current loopgains are equal to 1. This method is explained in Section 12 [17] where, as an example, ΔV_{series} is calculated for I^2L (fan-in = fan-out = 1).

As a reaction to [17] Seevinck showed [18] that instead of a careful examination of the small signal loops and of assuming that current loopgain and voltage loopgain are 1, it is possible to calculate instead the condition for which the Jacobian of the complete set of Kirchoff equations is zero. This provides a more mathematical approach, but physically it is exactly the same, so both methods deliver exactly the same value for a particular noise margin.

Only simple mathematical results are obtained when series resistances are ignored. I^2L, SI^2L, ISL and STL circuits are then translinear circuits [19], and the noise margins are current independent.

When calculations are too difficult (which certainly is the case when all series resistances are included), computer simulations have to be carried out.

The best way is to carry out quasi-static transient simulations by increasing the noise sources slowly compared with the switching speed of the flip-flop, and detect the noise amplitude at which the flip-flop switches to the wrong state.

2.XV. Static noise margins of ISL, STL, I^2L and SI^2L

A. ISL and STL

Fig. 25 shows the logic swing and the worst case room temperature static noise margins (simulated) of pn-isolated ISL with $F_i = F_o = 4$, $\beta_{fN} = 20$ and $\alpha_p = 0.9$. The results are obtained with an asymmetric flip-flop (see Section 11). The figure shows the logic swing, ΔV_{series}, ΔV_{gnd} and $\Delta i/i$ as a function of I_{do}/I_{po}. Stable flip-flop operation starts when $I_{do}/I_{po} > 120$; the logic swing increases with increasing I_{do}/I_{po}.

Fig. 26 shows the same as Fig. 25, but this time for more parameter values ($\beta_{fN} = 20$ and 100, $F_i = F_o = 1$ and 4) [20]. Measurements have been done for $I_{do}/I_{po} = 4.10^3$; and they coincide with the simulations. As shown by Fig. 26, ΔV_{series} is about 100 mV

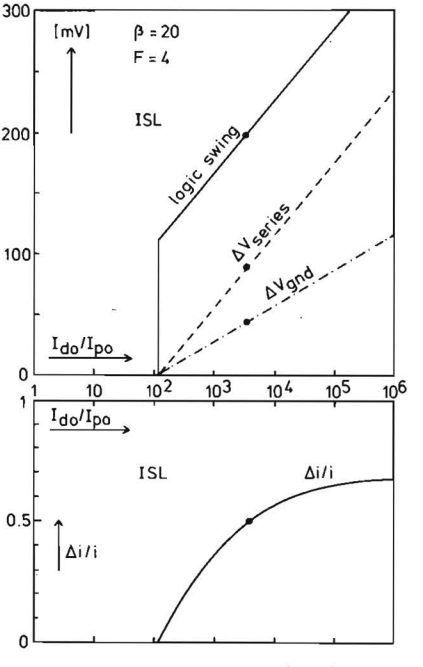

Fig. 25. Logic swing and worst-case room temperature static noise margins (simulated) of pn-isolated ISL with $F_i = F_o = 4$, $\beta_{fN} = 20$ and $\alpha_p = 0.9$ as a function of I_{do}/I_{po}.

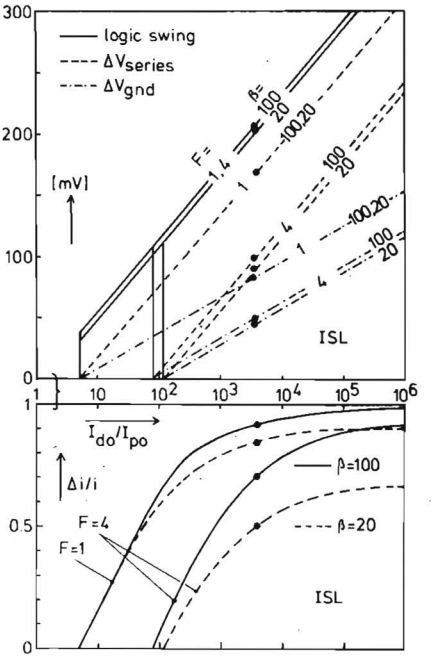

Fig. 26. As Fig. 25, but also for the parameters $F_i = F_o = 1$ and 4, and $\beta_{fN} = 20$ and 100.

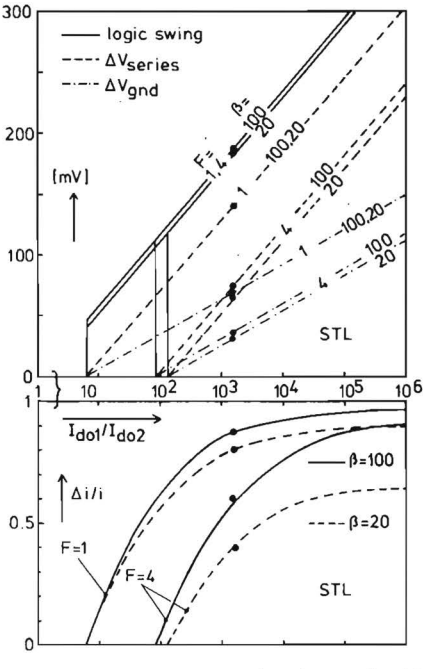

Fig. 27. Logic swing and worst-case room temperature static noise margins (simulated) of STL as a function of I_{do1}/I_{do2}.

smaller than the logic swing; ΔV_{gnd} is about 50 mV smaller than half of the logic swing; $\Delta i/i$ increases to $(\beta_{fN} - F)/(\beta_{fN} + F)$ for large values of I_{do}/I_{po}. Fig. 27 shows the logic swing and noise margins of STL [20]. The curves are very similar to those of ISL; along the abscissa is I_{do1}/I_{do2} instead of I_{do}/I_{po}.

B. SI^2L and I^2L

Fig. 28 shows the logic swing, ΔV_{series}, ΔV_{gnd} and $\Delta i/i$ for SI^2L [21] and I^2L for the case where $\beta_{up\ eff} = 2$, $\beta_{down} = 100$ and $F_i = F_o = 4$ at room temperature [20]. Along the abscissa are the saturation currents I_{do}/I_{no} for SI^2L, where I_{do} is the saturation current of the Schottky diode and I_{no} the saturation current of the inverse operated n-p-n. A saturated p-n-p current source is used both for SI^2L and I^2L. The voltage swing and ΔV_{series} of I^2L are not indicated in Fig. 28 because those values (~ 700 mV and ~ 600 mV respectively) are outside the scale of this figure. Fig. 29 also shows $F_i = F_o = 1$ and 4, and $\beta_{up\ eff} = 2$ and 10.

It has been suggested in the literature [12,22] that ΔV_{series} would be equal to $(kT/q)\ln\beta_{up\ eff}$; this is not true however.

The ground line noise margin ΔV_{gnd} is rather small due to the fact that the p-n-p current sources have their bases connected to ground, which implies that the current

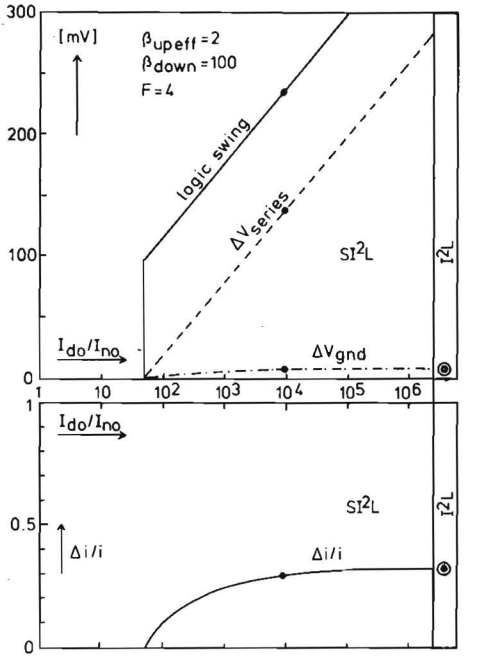

Fig. 28. Logic swing and worst-case room temperature static noise margins (simulated) of SI^2L and I^2L for the case where $\beta_{up\ eff} = 2$, $\beta_{down} = 100$, and $F_i = F_o = 4$. The voltage swing and ΔV_{series} of I^2L (~ 700 mV and ~ 600 mV respectively) are outside the scale of this figure.

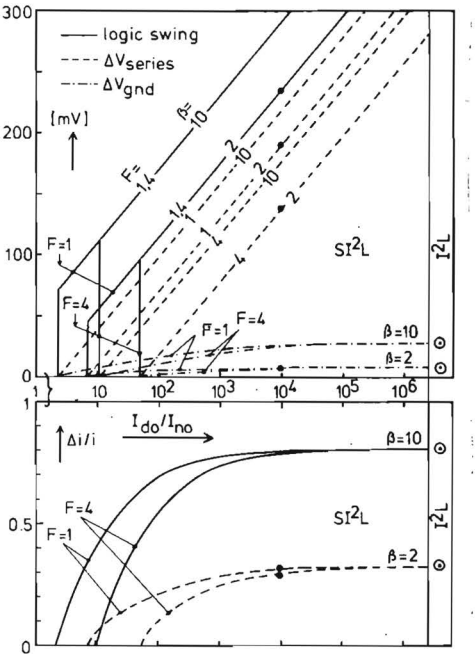

Fig. 29. As Fig. 28, but also for the parameters $F_i = F_o = 1$ and 4, and $\beta_{up\ eff} = 2$ and 10.

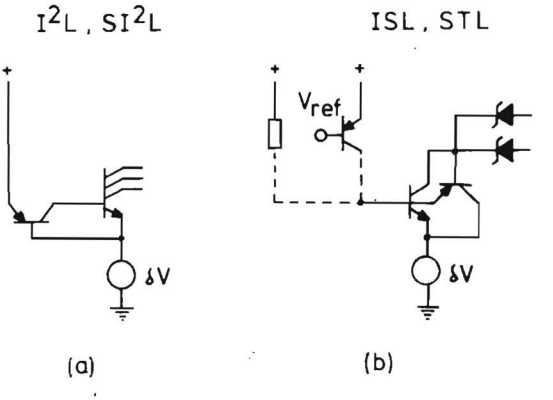

Fig. 30. Ground line voltage noise in SI²L and I²L (a) and in ISL and STL (b). As SI²L and I²L have a p-n-p current source which is exponentially modulated by δV_{gnd}, ΔV_{gnd} is much smaller than in ISL and STL.

sources are exponentially modulated by δV_{gnd} (see Fig. 30(a)). In ISL and STL this modulation is not very effective (see Fig. 30(b)), so ΔV_{gnd} and also ΔV_{supply} will be essentially higher for ISL and STL.

For I^2L, ΔV_{gnd} is equal to $\frac{1}{2}(kT/q)\ln\beta_{up\ eff}$, which is half the value given in [12] and [22].

The relative parallel current noise margin $\Delta i/i$ increases with increasing voltage swing to a maximum value of $\Delta i/i = (\beta_{up\ eff} - 1)/(\beta_{up\ eff} + 1)$.

No separate computer simulations have been done to determine ΔV_{supply}, because this value can directly be calculated from $\Delta i/i$ as the power supply is only connected to the emitter of the p-n-p. Calculation shows that $\Delta V_{supply} \approx (kT/q)\ln(1 + \Delta i/i)$, which is 5 mV for $\Delta i/i = 0.2$ for instance.

2.XVI. Dynamic noise margins of logic circuits

The static noise margins indicate the maximum DC noise amplitudes that can be withstood by the logic. This means that the noise may be present for an infinitely long time without bringing gates into the wrong state.

It is very well known that if the noise is present in pulse form, the noise amplitudes are allowed to be higher than the static margins, without affecting the proper logic states. Fig. 31 shows this phenomenon. For very long pulses the situation is quasi-static and the margins are determined by the static worst-case margins Δ_{static}.

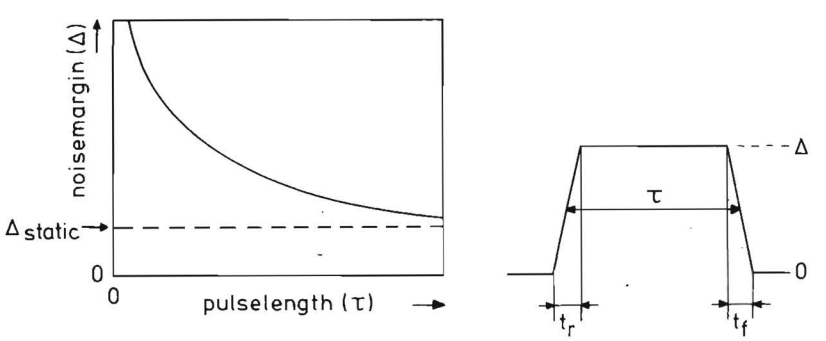

Fig. 31. General behaviour of the dynamic noise margins; amplitudes of noise pulses are allowed to be higher for short pulse widths. For very long pulses, the situation is quasi-static and the noise margins will reach their minima.

For short pulses the noise margins increase. The combination of the pulse length and amplitude now depend also on the switching speed of the gates.

Section 11 gives a first-order explanation as to wat happens in a logic cirucit when series voltage noise and parallel current noise is applied in pulse-form. During such a pulse

energy is delivered to or sinked from (= negative delivery) the circuit to bring it into the wrong state. It appears that the energies in these noise pulses are generally different for series voltage noise sources and parallel current noise sources; it is impossible therefore to speak of a typical energy noise margin as a figure of merit. In general, the energy delivered by a series voltage noise pulse increases with decreasing pulse-width, and the energy delivered by a parallel current pulse decreases with decreasing pulse width; this has also been demonstrated with pulsed noise in ISL.

2.XVII. Dynamic noise margins of ISL

Fig. 32 shows four noise sources in an pn-isolated ISL flip-flop ($F_i = F_o = 1$) without series resistances. These noise sources have been investigated separately for dynamic noise margins (the noise sources are not applied simultaneously, but separately).

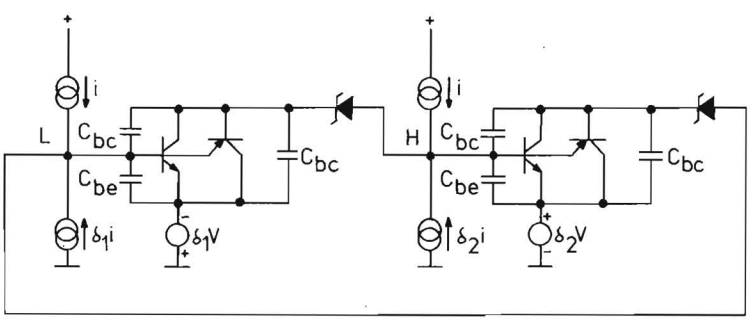

Fig. 32. Four noise sources in an ISL flip-flop ($F_i = F_o = 1$), which are investigated for the dynamic noise margins. The noise sources are not applied simultaneously.

Fig. 33(a) shows computer simulated dynamic voltage noise margins and relative current noise margins as a function of pulse width for the four noise sources. Fig. 33(b) shows the energy content of the same noise pulses (energy noise margins). Indeed the energy in the voltage pulses increases with decreasing pulse width and the energy in current pulses decreases with decreasing pulse widths.

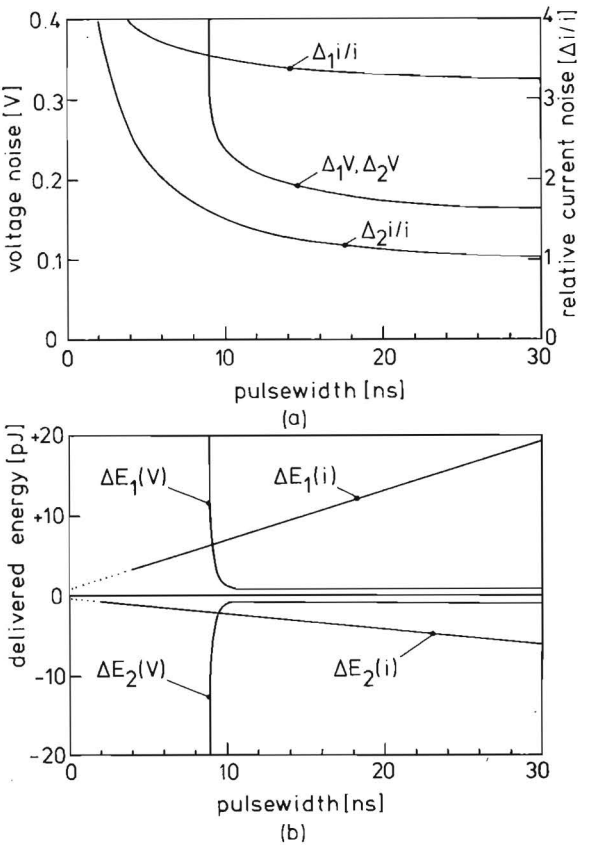

Fig. 33. Computer-simulated dynamic noise margins (a) and dynamic energy noise margins (b) of the ISL flip-flop of Fig. 32.

2.XVIII. Temperature behaviour of the static noise margins of ISL and STL

When, at room temperature, the voltage swings of ISL and STL are equal, then the room temperature values of the noise margins of ISL are a little better, due to the fact that in ISL the superfluous base-current of the saturated n-p-n transistor is sinked to ground (by the p-n-p transistor), whereas in STL this current has to flow through the n-p-n transistor. With a temperature increase, however, the noise margins of ISL are very soon smaller than those of STL, mainly because of the high negative temperature coefficient (− 0.6 mV/°C) of the voltage swing of ISL (as a first-order approximation the voltage swing of STL is independent of the temperature). Section 13 gives an analysis of the voltage swings of ISL and STL, and analytical expressions for the low-current worst-case static noise margins of ISL and STL. At high current levels series resistances can no longer be ignored and the noise margins are obtained with computer simulations.

Fig. 34(a) shows half the voltage swing and the worst-case static ground-line voltage noise margins of oxide-isolated ISL at 100 μA/gate with F = fan-in = fan-out as parameter, as a function of temperature. In this case the noise margin ΔV_{gnd} for $F = 4$ is quite low and even negative for temperatures higher than 50°C. Fig. 34(b) shows similar results but this time with a gate input current of 50 μA and an internal pull-up current of 50 μA. It is obvious that the noise margins have been increased dramatically; for $F = 4$

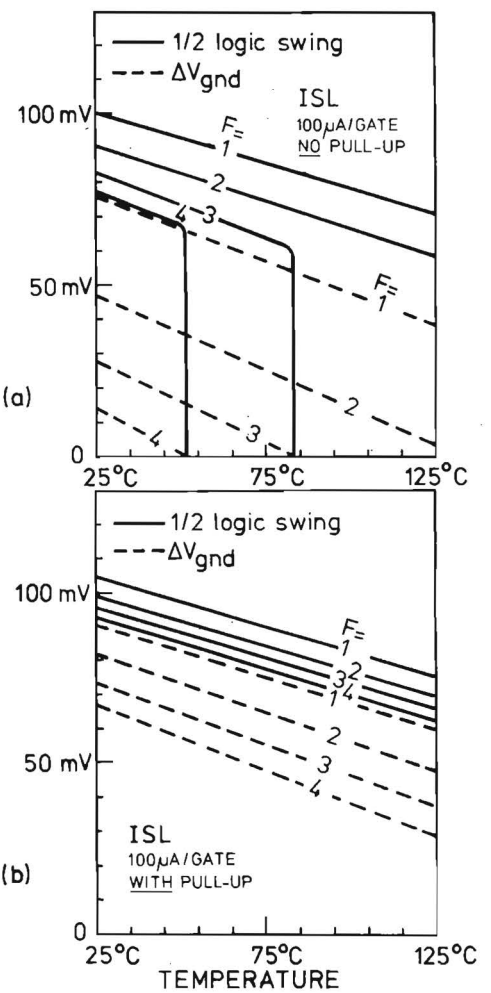

Fig. 34. Half the voltage swing and the worst-case static ground-line voltage noise margins at 100 μA/gate of oxide-isolated ISL without internal pull-up current (a) and with internal pull-up current (b), as a function of temperature, with F = fan-in = fan-out as parameter.

save operation is now possible up to 200°C. The noise margins of STL are always somewhat better due to the temperature-independent voltage swing, but without pull-up current $\Delta V_{gnd\ STL}$ is zero at 80°C for oxide-isolated STL at 100 μA/gate; also for STL the application of an internal pull-up current improves the noise margins (see Section 13). Thus the application of internal pull-up currents improves the noise margins and decreases the propagation delay time depending on the fan-in (see Section 2.XI) of ISL and STL.

2.XIX. Applications of ISL

Until now all ISL applications have been made in a pn-isolated process with a 3 μm epitaxial layer and 5 μm minimum details.

In appendix A some designs are discussed; a 256 bits shiftregister, a pipeline--multiplier, a counterchip (which combines ECL, I^2L, ISL and TTL), a custom library called CCL (= Composite Cell Logic) with as example a FIFO memory controller and a 1200 gate array (8A1200).

Appendix B summarizes the main characteristics and specifications of the 8A1200 gate array.

Oxide-isolated ISL applications such as a high performance gate array, and a 12x12 bit parallel multiplier are in preparation. Samples of both chips are expected in December 1981.

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3

Devices and Circuits for Bipolar (V)LSI

Abstract — **It is shown that bipolar circuits can continue to play an important role in high-performance LSI and VLSI circuits, because power supply voltages and logic swings can be minimized independently of transistor dimensions, and because the speed degradation due to on-chip wiring capacitances is less severe than in MOSFET/MESFET types of circuit. General performance improvements (in speed and packing density) of logic gates are obtained by increasing transistor f_T, and decreasing parasitic capacitances, series resistances and device areas, by using oxide isolation, self-aligned techniques and polysilicon electrodes. Fast switching diodes (such as Schottky barrier diodes and lateral polydiodes) improve the flexibility of circuit design. Logic circuits (such as I^2L, LS, DTL, ISL, STL, ECL, and NTL), which already perform in LSI and VLSI circuits or are realistic proposals for them, are discussed.**

3.I. Introduction

Although a clear definition of VLSI is hard to find, the most common opinion is that pure digital VLSI circuits should have at least 5000 (bipolar) or 10 000 (MOS) gates per chip. Analog VLSI is much more difficult to define; multifunctionality is here required, for instance 20 operational amplifiers on a chip. Also combined analog/digital functions can lead to VLSI chips (analog/digital, digital/analog converters with other systems). Both digital and analog VLSI will benefit from shrinking dimensions and reduced current levels. Power supply voltage reduction, however, is much more difficult to realize in analog circuits, due to high signal-to-noise ratio requirements, which means that large power supply voltages are needed. This also means that breakdown voltage requirements are much more stringent in analog circuits than in digital circuits; consequently the process developments for analog and combined analog/digital IC's do not always coincide.

As this article is focused on digital VLSI, only digital developments will be discussed.

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Nowadays most medium-size chip packages do not allow a higher power dissipation than about 1 W, which means that for most VLSI circuits with more than 5000 gates/chip the maximum power dissipation per gate has to be smaller than 200 μW. Furthermore, with maximum chip areas of 25 mm^2, packing densities better than 200 gates/mm^2 are required.

By extrapolating the development of IC technology from 1960 to 1980, forecasts have been made about the state of the art of silicon VLSI at the end of this century. Such forecasts envisage logic chips of 30 mm^2 having 25 000 gates per chip with gate-delay times of 100 ps, using standard production minimum details of 0.7 μm [1]. Memory chips, according to these predictions, will be much larger ($\sim$ 3 cm^2), containing at least 5×10^6 bits/chip and using the same minimum dimensions of 0.7 μm [1]. For large memory VLSI chips ($>$ 64 bit) which fit into main-frame memory systems with relatively long cycle times (300-800 ns), the Si MOSFET technology will be the favorite one. For fast memories (needed in cache-memory structures to bridge the gap between fast processors and the relatively slow main-frame memories) and for fast logic chips, five technologies can be considered: Si bipolar, Si MOSFET or MESFET, Si CMOS, Si JFET, and GaAs MES- or JFET. To make the right choice for a given application, a set of specific requirements has to be fulfilled, such as speed, power dissipation, packing density, noise margins, temperature stability, radiation hardness, sensitivity to power supply variations, costs (the latter depending on process complexity and yield in a given process), etc.

Section II gives a first-order comparison between bipolar and MOS-type circuits. It will be shown that the speed degradation in bipolar circuits due to on-chip wiring capacitances is less severe than in MOS/MES – FET types of circuits. In Section III the general behaviour of switching speed and power-delay product of bipolar circuits is explained.

In Sections IV-VII the processes for n-p-n transistors, p-n-p transistors, Schottky and polysilicon diodes, and resistors are treated. In Section VIII, logic circuits are given and a comparison is made. It will be shown that some types of circuits in combination with the appropriate technology are good candidates for high speed VLSI.

Whether the bipolar technologies will really become commercially successful as VLSI technologies not only depends on their technical potentials. For instance reduced power supply voltages (e.g., 0.8-3.0 V) have to be accepted for system applications. Further market factors as second-sourcing and accessibility of a technology for custom design as well as yield cost tradeoffs are very important. These items, however, will not be included in this technical article.

3.II. Comparison Between Bipolar and MOS-Type Circuits

Fig. 1 shows two basic inverter stages of a ring oscillator built with arbitrary devices. The logic swing is given by $\Delta V = V_H - V_L$. The load capacitance C_L is the sum of the junction capacitance C_j, the on-chip wiring capacitance C_w, and a third capacitance. In the bipolar case this third capacitance is a non-linear one with charge $Q = i\tau_{tr}$ (where τ_{tr} is the transit-time of the bipolar transistor); in the MOS case this capacitance is the (linear) gate capacitance C_g. As a very first-order approach, neglecting series resistances, the propagation delay times are given by

$$t_{d\text{bipolar}} \approx \frac{(C_j + C_w)\Delta V}{i} + \tau_{tr} \tag{1}$$

$$t_{d\text{MOS}} \approx \frac{(C_j + C_w)\Delta V}{i} + \frac{C_g \Delta V}{i}. \tag{2}$$

Due to the exponential current/voltage characteristic of the bipolar transistor, the current in the bipolar case can be increased many decades by changing V_{BE} with some amounts of $(kT/q)\ln 10$ (= 60 mV at room temperature) without increase of transistor size. This means that the idealized propagation delay time of the bipolar circuit can be minimized down to τ_{tr}, by increasing the current level and/or decreasing ΔV.

In the MOS-case it is much more difficult to increase the current level, due to the quadratic current/voltage characteristic. The current is increased by increasing the transistor size, but by doing so, also C_g will increase. The minimum propagation delay time is calculated in the following way. With $V_{\text{in}} = V^+$ the output voltage of the inverter has to be about half the threshold voltage ($V_T/2$). This means that $\Delta V = V^+ - V_T/2$. The driver transistor, which operates in the triode region, has to draw the current i, which means

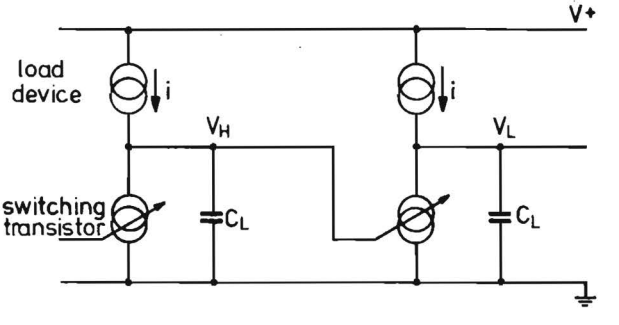

Fig. 1. Two basic inverter stages of a ring oscillator built with arbitrary devices. C_L represents the total capacitance (logic gate capacitance + on-chip wiring capacitance).

that $(W/L)\beta_{\square}(V_T/2)\Delta V = i$ where W is the transistor width, L the transistor length, and $\beta_{\square}$ the gain factor.

Furthermore, $\beta_{\square}$ is given by $\beta_{\square} = \mu C_{ox}$, where μ is the surface mobility and C_{ox} the gate oxide capacitance per unit square. With the above mentioned formulae, and neglecting velocity saturation, equation (2) is easily transformed to

$$t_{dMOS} \approx \frac{C_j + C_w}{(W/L)\mu C_{ox} V_T} + \frac{2L^2}{\mu V_T}. \tag{3}$$

Equation (3) says that the MOS propagation delay time can be minimized down to $2L^2/\mu V_T$ by increasing W (the current level increases linearly with W).

This means that larger transistors than minimum-size transistors have to be used to obtain this minimum. This measure, however, affects the packing density of the circuits (which is a disadvantage for VLSI). Further with increasing W, and decreasing packing density, the length of the interconnect wires will increase and thus C_w is going to increase, which means that in reality the minimum $2L^2/\mu V_T$ can never be reached [2]. This all means that the performance of MOS circuits with minimum-size transistors is strongly affected by wiring capacitances. In GaAs where μ is about a factor of 5 higher than in Si this is still true, but there the speed can be anyhow the same factor of 5 faster.

Another figure of merit is the power-delay product $Pt_d = iV^+t_d$. In the bipolar case $Pt_{dbip.} = V^+\Delta V(C_j + C_w) + V^+ i\tau_{tr}$ and in the MOS case $Pt_{dMOS} = V^+\Delta V(C_j + C_w + C_g)$. In scaled Si MOS and CMOS, V^+ and ΔV are not allowed, for noise margin reasons, to be lower than 0.5 and 0.4 V respectively, [3]. In bipolar circuits V^+_{min} can be between 0.8 and 1 V (being V_{BE} plus a voltage drop across the load device), independent on scaling, while ΔV_{min} can be between 150 and 200 mV [4]. This means that eventually the minimum $V^+\Delta V$ product is quite independent of the technology ($\sim 0.2\ V^2$). In large chips with dominating C_w the power-delay product would be independent of the technology when using this minimum $V^+\Delta V$ product!

A comparison of Si bipolar and Si MOS shows that, when the wiring capacitance is neglected, the Pt_d product is smaller for bipolar circuits when using minimum details $> 1\ \mu m$ [5,6]; furthermore t_{dmin} is smaller for bipolars when using minimum details $> 0.5\ \mu m$ [5,6].

Summarizing it can be said that the advantages of bipolar circuits over MOS circuits are that: a) optimum speed can be obtained with minimum size transistors, b) smal voltage swings are possible (due to the exponential characteristics), resulting in a relative small speed degradation due to on-chip wiring capacitances, c) V^+ and ΔV can be minimized independent of transistor size.

This all means that bipolar circuits can keep an edge in the IC market where ultimate speed performance is required. GaAs MESFET's can take over a part of the market

share, but this technology is not yet considered as a mature one [7], and if it does reach maturity its success will depend on the cost/performance ratio.

3.III. General Behavior of Switching Speed and Power-delay Product of Bipolar Circuits

In general, the switching speed of bipolar circuits increases (propagation delay time decreases) when the current per gate is increased. At relatively low current levels the storage of minority carriers can be disregarded, and the switching speed is determined only by the capacitances $C_L = C_j + C_w$ (junction capacitances + on-chip wiring capacitances). In this case the approximated average propagation delay time t_d equals $C_L \Delta V/i$, where ΔV is the logic swing and i the current per gate. The power-delay product yields $C_L V^+ \Delta V$.

Without series resistances the propagation delay time decreases linearly with increasing current, whereas the power-delay product remains constant (see low-current part of curve A in Fig. 2). At relatively high current levels the storage of minority carriers starts to play a dominant role. As the storage increases linearly with the current (assuming

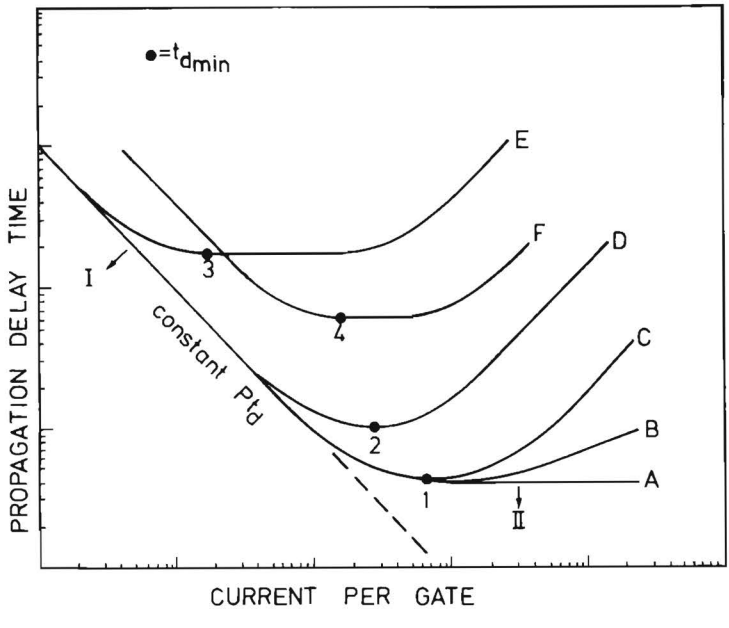

Fig. 2. General behaviour of the switching speed as a function of current per gate of bipolar circuits.
A: no series resistance(s), constant f_T; *B*: no series resistance(s), decreasing f_T; *C*: as *A* or *B* with series resistance(s); *D*: as *A* or *B* with high series resistance(s); *E*: as *A* or *B* with very high series resistance(s); *F*: as *D* with a higher load capacitance.
Arrow I: less capacitance; Arrow II: less minority carrier storage (higher f_T).

that the transition frequency f_T of the transistor is constant), no speed improvement is possible; t_d remains constant (see the high current part of curve A in Fig. 2). Note that $t_{d\min}$ is found at a higher power-delay product than the delay times at low-current levels.

In practical cases f_T will decrease with increasing current at sufficiently high-current levels, which means that t_d tends to increase with higher currents (see curve B in Fig.2). So far the ideal case has been considered where series resistances are disregarded. In practice however series resistances can affect the performance of the logic seriously. If series resistances are present in paths where switching peak currents have to flow, they limit these peak currents and consequently the switching speed of the gates is reduced [8,9]. The most troublesome series resistances are base- and collector-series resistances of switching transistors and series resistances of Schottky diodes. Depending on the values of the series resistances, deviations of curve A and B can occur. With very small series resistances the same $t_{d\min}$ can be obtained as for curves A and B (see point 1 on curve C in Fig. 2). At higher currents t_d increases strongly because the minority carrier storage increases, whereas the available current to discharge this charge remains limited by the series resistances.

With higher series resistances point 1 cannot even be reached because t_d already starts to increase at lower current level (see curve D with $t_{d\min}$ at point 2 in Fig. 2). With very high series resistances t_d remains limited by RC-time effects ($R_{\text{series}}\, C_L$), long before minority carrier storage plays a role, and increases again as soon as minority carrier storage is no longer negligible (see curve E with $t_{d\min}$ at point 3 in Fig. 2; remark that in this case a plateau occurs in the curve).

When C_L in a given circuit is increased by adding a relatively large wiring capacitance to the logic gate, $t_{d\min}$ can start to be limited by RC-time effects as shown by curve F in Fig. 2, which has the same series resistances as curve D. Due to the larger capacitance C_L, the power-delay product is increased, and due to the larger value of $R_{\text{series}}\, C_L$, $t_{d\min}$ is found at point 4, instead of at point 2.

From this information, it can be concluded that the performance of bipolar circuits is optimized by: a) minimizing V^+, ΔV, and C_L (see arrow I in Fig. 2); b) minimizing the minority carrier storage by realizing a high f_T for the switching transistors and eliminating or minimizing saturation effects (see arrow II); c) reducing critical series resistances to acceptably low values.

As already mentioned in Section II, the $V^+\Delta V$ product can be minimized to about 0.2 V^2, independent of the feature sizes in the process. Junction and dielectric capacitances can be decreased by scaling the process to smaller dimensions. The transition frequencies of the transistors can be increased by making shallower layers and steeper doping profiles [10]. In scaling down, physical limitations such as punchthrough and base-stretching (Kirk effect) must be avoided by increasing the base and collector doping

respectively, as base width and the current density increases [8]. This processes can continue until other limitations such as contact resistance, tunneling, or base doping fluctuations [11] are encountered [8,12]. Further, unless higher base dope levels are used, transistor base series resistances may increase when shallower junctions are used, which means that a tradeoff between forward current gain and base series resistance has to be made. Also, due to smaller dimensions, the current densities tend to increase, causing transistors to go into high injection at lower current levels, which affects f_T. This, therefore, means that it is impossible to give the best combination of measures beforehand, because many tradeoffs can be made, depending on the type of logic circuits and the type of specific technology used.

In the following sections it will be shown how process modifications can improve the performance of n-p-n transistors, p-n-p transistors, Schottky diodes, polysilicon diodes, and resistors.

3.IV. The n-p-n Transistors

A. SBC, CDT, and 3D Processes

Since the early 1960's integrated circuits have been made with p-n isolation, either with or without the application of an epitaxial layer.

The process most commonly used has been the standard buried collector (SBC) process, which uses an n^+ buried layer to reduce the collector series resistance, an n-epitaxial layer and a p^+ isolation diffusion (Fig. 3(a)).

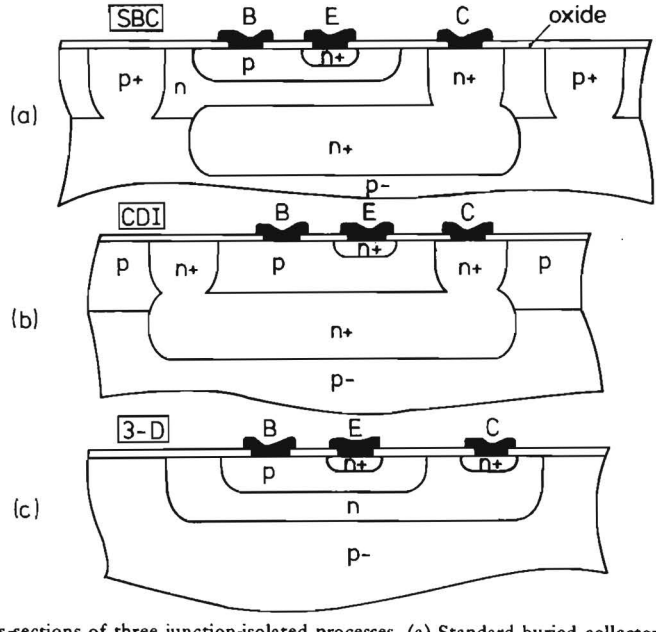

Fig. 3. Cross-sections of three junction-isolated processes. (a) Standard buried collector (SBC) process. (b) Collector diffused isolation (CDI) process. (c) Tripple diffused (3D) process.

Another process, called collector diffused isolation (CDI), uses a p-epitaxial layer and an n^+ isolation diffusion which also provides the contact to the buried layer. The base, which is relatively thick, is formed by the epitaxial layer (Fig. 3(b)) [13,14]. To obtain an epilayer thickness independent base-width, the dope level of the epilayer can be decreased and an extra base-diffusion can be applied.

By application of an accurate ion implantation for the n-collector well, n-p-n transistors can be made directly in a p-substrate in a process called triple-diffused (3D) [15] or also called guard-ring isolated monolithic IC (GIMIC-O) [16], see Fig. 3(c). Due to its simplicity this process has a high yield and relatively low manufacturing costs.

B. VLSI Process Requirements

Although the aforementioned technologies are used in MSI and some LSI circuits, the areas of the transistors are not small enough for the packing densities needed in VLSI circuits. Also the junction capacitances are rather high due to the relatively large areas, and some transistors suffer from either a low f_T (CDI) or large collector series resistance (3D); this makes that neither a small power-delay product nor a small $t_{d\min}$ can be obtained with these technologies.

Several processes have been developed to obtain the required properties for high-speed LSI and VLSI. These properties are: small active transistors areas (for packing density and reduction of capacitances), shallow layers and diffusions and steep doping profiles (to obtain high f_T) and small series resistances.

Most efforts are directed to the following:

a) minimizing the emitter area to reduce C_{be} and the base series resistance R_{bb}', (a very narrow emitter stripe is the most effective one, because of the current crowding effect);
b) placing the base contact as close as possible to the emitter, to reduce the size of the base area (reduction of C_{bc}) and to reduce R_{bb}';
c) application of oxide isolation to obtain walled emitters and walled base areas, which means that C_{be}, C_{bc}, and the collector substrate capacitances are reduced (furthermore, oxide isolation provides the possibility to make small-area walled p-n-p transistors and JFET's instead of the area-consuming ring-p-n-p and ring-JFET transistors which have to be made in p-n-p isolated processes).

C. Oxide Isolation Processes

Oxide isolation can be obtained by different means. The best known technique uses the mask properties of Si_3N_4 to obtain local oxidations. The technique has been described by several authors, using different acronyms: LOCOS [17,18]; Isoplanar [19,20, 21]; OXIM [22]; Planox [23]; OXIS [24]; and ISAC [25].

The processes use either n-type or a p-type epitaxial layers and are well established. Production yields are reasonable high and small transistor sizes are obtained with thin epitaxial layers and small dimensions. These processes will be the standard in the 1980's.

When the epilayer is too thick ($> 1.5\ \mu m$) for oxide isolation, a combination of oxide isolation and p-n isolation can be made called recessed oxide isolation (ROI) [26,27].

Fig. 4 shows a part of the LOCOS process sequence. After implantation and oxidation of the walled base area (the base-mask overlaps the thick oxide), contact holes are made with a composite mask, containing the base contact, the collector contact, and the emitter area which is usually walled at two sides. After covering the base contact with photoresist (with an extra noncritical mask), an arsenic ion implant is done to form the washed emitter and the collector contact. As the base contact to emitter contact distance is not influenced by an alignment procedure, this distance can be minimized to the minimum metal spacing. For this reason the area of the transistor can be relatively small and the base series resistance is minimized.

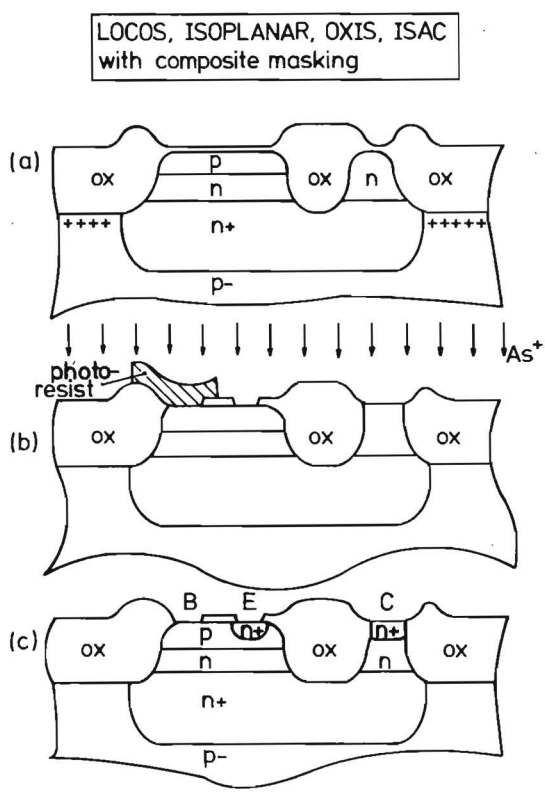

Fig. 4. Part of process sequence of an oxide isolated process. (a) Base formation. (b) Contact holes for base contact, emitter, and collector contact plus laquer coverage of base contact plus arsenic ion implant. (c) Removing laquer plus stripping of thin oxide for washed emitters.

With a thin epitaxial layer and small minimum dimensions, small-area high-performance transistors are made with f_T's between 3 and 5 GHz. Table I compares transistors made in the SBC process with 3-μm epitaxial layer and 5-μm minimum details, and in a typical LOCOS process with 1.2-μm epitaxial layer and 3-μm minimum details. Both transistors have a single base contact. The packing density of the LOCOS transistors is a factor three higher than of the SBC transistors. All capacitances and resistances of the

		SBC 3 μm epi 5 μm min. details	LOCOS 1.2 μm epi 3 μm min. details
area	[μm^2]	1500	500
C_{be}	[pF]	.1	.07
C_{bc}	[pF]	.12	.05
C_{cs}	[pF]	.52	.13
$R_{bb'}$	[Ω]	250	800
R_e	[Ω]	6	9
R_c	[Ω]	40	20
f_T	[GHz]	1	3-5

TABLE I
Comparison of Transistors Made in the SBC Process with 3 μm Epitaxial Layer and 5 μm Minimum Dimensions, and in a Typical Oxide Isolated Process with 1.2 μm Epitaxial Layer and 3 μm Minimum Details.

LOCOS transistors are smaller, except for the base-series resistance, which is larger, due to the more shallow base. Very often the extrinsic base area is provided with an extra boron dope to reduce $R_{bb'}$ (base boost). Also a double-base contact can be applied to reduce $R_{bb'}$ with a factor of 2 to 4; this of course increases the transistor size. A non-walled transistor (which is larger in size) will also have a lower $R_{bb'}$ [28].

A type of transistor isolation which has not gained very wide acceptance is the Polyplanar process [29] or IOP (isolation by oxide and polysilicon) process [30], uses V-grooves (obtained by anisotropic etching) which are oxidized and backfilled with polysilicon. Some improvements in transistor size and in reduction of sidewall capacitances are obtained.

D. Polysilicon Processes

The introduction of polysilicon in bipolar processes has opened up a number of new ways to improve both packing density and/or the performance of the transistors. In most cases the processes are much more complicated than the standard oxide isolated processes, which means that production yields will be relatively low; however, the yields may improve when the experience with polysilicon increases in the future.

An example is a process called elevated electrode integrated circuits (E^2IC) where As-doped polysilicon is used for the emitter diffusion source as well as for the elevated emitter and collector electrodes as shown in Fig. 5(a) [31]. The polysilicon is processed to form an overhanging edge; consequently, the evaporated metal on the rooftop of polysilicon is isolated from the metal on the lower ground level. This means that the separation between base and emitter electrodes is self-aligned and less than 0.4 μm. The lateral gap between electrodes from the top view is apparently zero. The process features an emitter size of 3×4 μm^2, together with a base area of 64 μm^2, $R_{bb}' = 111\ \Omega$, and $f_T = 7$ GHz [31].

Another recently published process [32] has the same aim as E^2IC, but tries to achieve it by a more direct method. Here too the emitter is out-diffused from As-doped polysilicon, but the metal contact to the emitter is not directly on top of the structure;

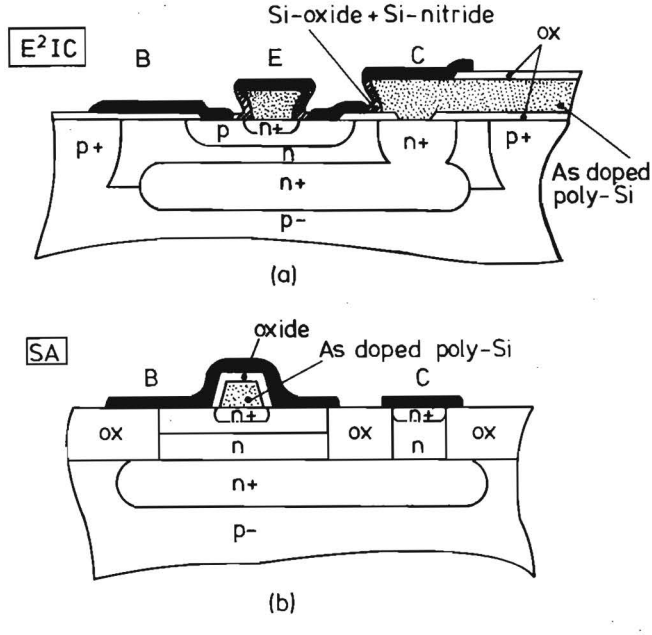

Fig. 5. (a) Cross-section of the E^2IC process. (b) Cross-section of the self-aligned preferential-oxide-etch polyprocess.

a piece of lateral polysilicon remains between the emitter and metal contact (see Fig. 5(b)).

By oxidation of the polysilicon and by doing a selective etch it is possible to remove the oxide on the transistor base area while maintaining the oxide on the polysilicon. Metal can now be deposited which contacts the base and which is isolated from the emitter. In this manner, the base contact is self-aligned to the emitter.

Base emitter self-aligned technology (BEST) is another process that can be used to make the base area and the distance from base contact to emitter smaller than determined by the metal spacing on top of the structure (Fig. 6(a)) [33]. In this process, which starts with an n-epilayer and non-doped polysilicon, two boron and one arsenic implants and

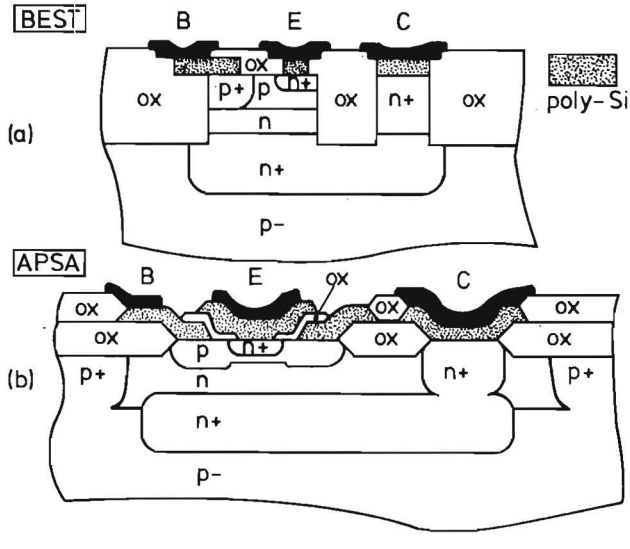

Fig. 6. (a) Cross-section of the BEST process. (b) Cross-section of the APSA process.

diffusions through the polysilicon are done successively to achieve the intrinsic base, base--contact and emitter, respectively. Although the transistor size can be very small, some extra base series resistance has to be accepted due to series resistance in the boron-doped polysilicon. The extra resistance makes this process unsuitable for very high speed.

The resistors are simultaneously made with the boron-doped polysilicon; this gives a reduction of parasitic capacitances and of the distance between resistors.

A poly-self-aligned process (PSA) is quite similar to BEST except for the fact that the polysilicon electrodes and interconnections are alloyed with platinum to reduce the sheet resistivity to 3 $\Omega/\square$ [34]. The most advanced type of this process, called advanced PSA (APSA) uses two layers of polysilicon, allowing for small emitters with close base

contacts and overlapping electrodes (Fig. 6(b)) [35]. Emitters 1 μm wide are made by using fine lithography and Si_3N_4 masking. Transistors have been fabricated with a 1 x 3 μm^2 emitter area, and a base area of 42 μm^2, C_{be} = 13 fF, C_{bc} = 22 fF, C_{cs} = 110 fF, and $R_{bb}' = 367\ \Omega$.

E. Influence of Polysilicon on the Emitter

Having the emitter covered with polysilicon has advantages in processes where silicide Schottky diodes are made as well and where the silicide step is maskless in all the contact holes. In that case the silicon-consuming silicide step does not consume n^+-monocrystalline silicon from the emitter region, which means that the emitter Gummel number and consequently the current gain of the transistor are not affected. When a very thin layer of SiO_2 is present between the polysilicon and the n^+-emitter, the emitter Gummel number is increased, which means that the transistor current gain is increased [36,37,38]. A selectively grown epitaxial layer on top of the emitter can also provide the same effect [39]. In this way the base thickness may be increased if the higher current gain is not wanted; in that case R_{bb}' is reduced (at the expense of a somewhat lower f_T).

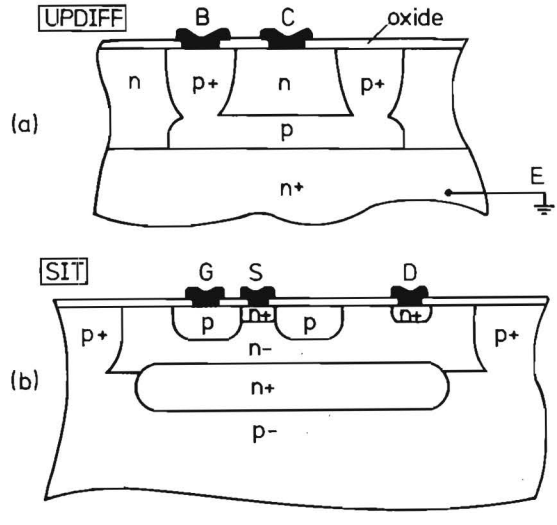

Fig. 7. (a) Cross-section of the inverse-operated up-diffused n-p-n transistor. (b) Cross-section of the short-channel vertically normally-off n-channel JFET (BSIT).

F. Up-Diffused Base Processes

In some logic circuits, such as I^2L, n-p-n transistors are used in the reverse mode, the buried layer operating as the emitter. To obtain a steep emitter-base diffusion profile and a base width that is nearly independent of the thickness of the epilayer an up-diffused

technology has been developed in which B and Sb are implanted prior to the growth of the epilayer. During n-epi growth and subsequent high-temperature processing the p-type boron up-diffuses in the n-epi film at a rate faster than that of the n^+ buried layer dopant, creating a vertical n-p-n with a heavily doped n^+ emitter, a sharply graded p-base region ($W_B \sim 0.3$ μm) and a lightly doped collector region (Fig. 7(a)) [40]. Ohmic contact to the buried p-base and definition of the n-epi collector area is then obtained by diffusing a p^+ annular ring down through the n-epi to touch the up-diffused base. Oxide isolation can be combined with this technology [41].

Although these processes show attractive electrical features, the yield and reproducibility is not proven at this moment.

G. Short-Channel JFET Transistors (SIT)

A transistor structure called static induction transistor (SIT), which is in fact a short-channel vertical JFET, is made on a low-doped epitaxial layer ($N_D = 10^{13} - 10^{15}$ cm^{-3}), which means that for channel widths in the μm region the channel is pinched-off in the nonbiased condition, resulting in a normally-off transistor [42,43,44]; see Fig. 7(b).

For small forward biased base-emitter (gate-source) voltages a punchthrough current flows from emitter (source) to collector (drain) [45,46]. Due to its highly two--dimensional behaviour, the internal voltage barrier (which determines the punchthrough current [47]), is modulated by both V_{ce} and V_{be}. The i_c - V_{be} characteristic is exponential with a non-ideality factor which is fundamentally larger than one [45,46]; this means that in the low-current region the transistor behaves like a bipolar transistor, but with a lower transconductance than a normal bipolar transistor. At higher current levels the depletion layers withdraw and an n-channel JFET current flows from emitter to collector. The injection of holes further causes conductivity modulation, providing a highly conductive channel; in that case the minority carrier storage will affect the f_T considerably.

Due to the high influence of V_{ce} on the collector current, the output conductance of the SIT transistor is very poor compared with a real bipolar transistor.

It has been shown [43,45,46], that the current through the SIT device is very sensitive to lateral dimensions, which makes it doubtful whether the SIT transistor is a reliable device for VLSI.

3.V. p-n-p Transistors

The p-n-p transistors are mostly used as load devices for n-p-n switching transistors, and have to be made in n-p-n compatible processes.

A. Lateral p-n-p Transistor Types

In most cases a lateral p-n-p device is made using the n-p-n-compatible shallow

p-diffusion (n-p-n-base) for emitter and collector, while the n-epilayer provides the p-n-p base. The thickness of the p-n-p base is mask-determined and also dependent on lateral out-diffusion of boron, which owing to process variations, makes it difficult to make reliable basewidths below 0.5 μm. Further hole injection from the p-emitter area is also downwards into the epilayer, which means extra storage of minority carriers; and when holes diffuse through the buried layer a loss current flows to the substrate (parasitic vertical p-n-p). This all means that the f_T of the lateral p-n-p is low and that the current gain is rather limited. Further the transisitor will go into high injection at relatively low--current levels owing to the low-doped epilayer. With oxide isolation a walled structure can be achieved in processes where the channel-stop diffusion under the thick oxide does not make a short circuit between collector and emitter.

When using a p-type epitaxial layer a submicrometer base-width can be obtained by doing a double diffusion (phosphorous first, then boron) through the same contact opening [48,49]. Details of the reliability of this last method have not yet been published.

B. Vertical p-n-p Transistor Types

Vertical p-n-p transistors can have much better properties than the lateral type. In the n-p-n-compatible processes with thin epilayers a relatively fast vertical p-n-p is obtained between the shallow p diffusion and p substrate, when the n^+ buried layer is not inserted at this point. However, as the substrate has to be connected to a fixed voltage,

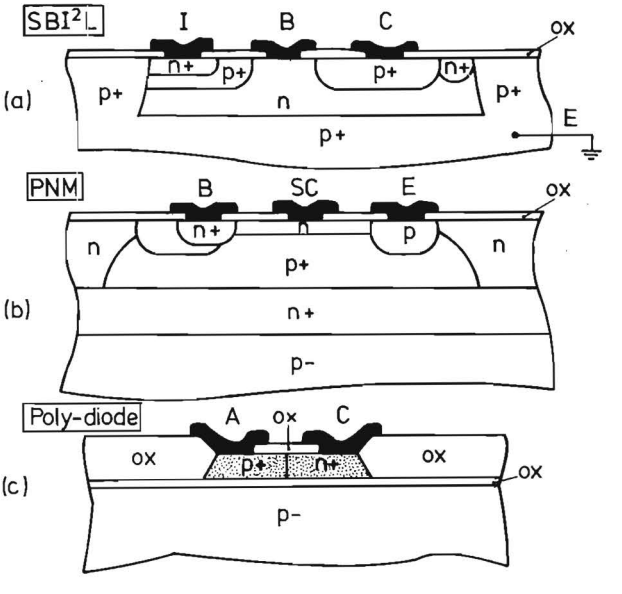

Fig. 8. (a) Cross-section of a vertical inverse-operated p-n-p switching transistor used in Schottky base I^2L. (b) Cross-section of a vertical inverse-operated p-n-m transistor, which is a p-n-p transistor with a Schottky diode as collector. (c) Cross-section of a lateral polysilicon diode.

such a p-n-p can only be used as an emitter follower (with the substrate as collector) or as an p-n-p-clamp device (for instance in ISL [50]).

C. Reverse Operated Vertical p-n-p Transistor Types

Sometimes, reverse operated vertical p-n-p transistors are used as the basic switching transistors in logic circuits. This has been demonstrated in an experimental I^2L process, called Schottky base I^2L, where the load device is a lateral n-p-n (fig. 8(a)) [51].

The f_T of vertical p-n-p's will be lower, however, than the f_T of vertical n-p-n's because of the lower mobility of holes in the p-n-p base.

A special type of reverse-operated p-n-p uses a Schottky diode as collector area of the transistor [52,53]. This type of transistor is also called p-n-m (where m stands for metal). Fig. 8(b) shows such a transistor; the advantage is that the transistor is automatically Schottky clamped. It has been shown that the p-n-m can be made in a vertical n-p-n--compatible process with an extra up-diffused p^+ region [53]; if no yield problems arise, this p-n-m transistor can be attractive in some type of circuits.

3.VI. Schottky Diodes and Polysilicon Diodes

Diodes are used either to keep transistors out of saturation (clamping) or for logic functions. For speed, the switching time has to be small (small junction capacitance and low amount of minority carrier storage); for packing density the area has to be small. For clamping the Schottky barrier diode only is suitable (due to the low forward voltage), while for logic functions both Schottky diodes and polysilicon diodes can be used.

A. Schottky Barrier Diodes

Schottky barrier diodes are made by applying metal directly on top of n-doped silicon. When using homogeneously doped epilayers, the doping of the epilayer has to be sufficiently low to prevent the barrier from being penetrated by tunneling electrons; in practice, this limits the doping to less than about $10^{17}cm^{-3}$ [54]. Different Schottky barrier heights can be used for different purposes and can be achieved by using different metals and/or by doing a barrier-lowering shallow n^+ ion implant just underneath the Schottky diode [55,56,57]. Because of the concentration of electric field lines near the corners, the reverse breakdown voltage of a Schottky diode is not an abrupt function of voltage and occurs at a relatively low bias. Several techniques, such as the use of diffused guard rings or field plates, have been developed to improve the reverse characteristics. Because they often complicate the circuit processing, and they consume extra area, these techniques are avoided unless especially needed. Self-aligned guard rings have been reported [58], but at the expense of a more complicated process.

Aluminium, which is mostly used for the wiring on the chip, can also be used to

form Schottky diodes (with a barrier height of 0.7 eV), but reproducibility problems often arise, especially in the case of diodes without guard ring. More reproducable Schottky diodes are made with a platinum-nickel compound Ni_xP_{1-x} that forms a silicide layer with the silicon underneath. By changing the nickel-platinum ratio, barrier heights between 0.64 eV (for 100-percent Ni) to 0.84 eV (for 100-percent Pt) can be obtained [59]. Titanium and tungsten can be used to obtain diodes with much lower barrier heights (0.53 and 0.59 eV, respectively).

B. Lateral Polysilicon Diodes

Lateral polysilicon diodes can be fabricated on top of the oxide (Fig. 8(c)). With narrow polysilicon lines, active areas of a few square micrometers can easily be realized. For clamping of bipolar transistors the forward voltages of these diodes are generally too high; because the exponential current increase with bias voltage is slower than in bipolar transistors ($\exp(qV/2kT)$ instead of $\exp(qV/kT)$) [60-62]. However, the switching times are very short due to the short lifetimes of minority carriers. Therefore this type of diode can be used as a logic switching diode very well [34].

3.VII. Resistors

A. Diffused and Ion-implanted Resistors

For low ohmic resistors the diffusions for the base and emitter of the n-p-n transistor can be used. High-value resistors are often made with an extra shallow ion implant step. Using the last method, reproducible sheet resistances up to 20 kΩ ± 10 percent per square are possible (p-ion implant in n-epilayer). The higher the sheet resistance the less accurate and reproducible the resistance will be, due to: variation in the doping of the epilayer, spread in the ion implantation, spread in oxide charge in the oxide layer on top of the resistor (this can cause a depletion or enhancement layer at the oxide interface), and influence of potentials applied to metal lines which cross such a resistor. The highest resistor values are limited by the fact that the p-ion implant must overdope the n-epilayer at least with a factor of 2.

B. Polysilicon Resistors

A way to achieve high ohmic resistors is to make them with doped polysilicon on top of the oxide. Undoped layers may reach a specific sheet resistivity of 10^8 Ω per square, but are generally not reproducible. The sheet resistance is reduced by doping the polysilicon. As the resistivity strongly depends on the doping level (the sheet resistance decreases more than linear with the dope level) and grain size of the polysilicon, the reproducibility of the resistors remains poor, which means that polysilicon resistors can be used only in circuits where high resistance variations are tolerated.

The temperature coefficient of these resistors is rather high and, in contrast to im-

planted resistors in crystalline silicon, it may be negative. A description of the conduction mechanism underlying the complex behaviour has been given [63].

At the cost of higher processing complexity, polysilicon resistors make it possible to construct high-value small-area loads, and do generally offer additional area reduction in bipolar technology as compared with the shallow ion-implanted resistors. In processes where polysilicon electrodes to the transistors are made (BEST, APSA, etc.) these resistors fit very well.

3.VIII. Logic Circuits

Many types of logic circuits exist which are already performing in, or are realistic proposals for LSI and VLSI circuits. Since an extensive treatment of all circuits would be impossible within the limited scope of this article, only the most important ones will be discussed. These are LS, I^2L, STL, ISL, DTL, ECL, and NTL.

The state-of-the-art of these circuits in their optimized technologies will be discussed.

At the end of this section the performance (t_d, P, Pt_d, and packing density) of the most important circuits will be compared and it will be checked which circuit/technology combinations fulfil the VLSI requirements: $P < 200$ μW and packing density > 200 gates/mm^2.

Other circuits as bipolar (E)(P)ROM and (F)PLA circuits play a considerable role in LSI circuits where system transparency and turn-around time are important items; these circuits, however, may not provide optimal speed and optimal packing density and are not considered as real VLSI candidates and therefore not treated in this article.

A. Low-Power Schottky (LS) TTL

For LSI circuits the optimum packing density is required, and, therefore, the simplest unbuffered low-power Schottky (LS) TTL gate is used for internal chip gates, whereas the output interface circuits are buffered with the more powerful totempole circuit [64]. Fig. 9 shows a simple LS gate (two-input NAND); the circuit requires two collector islands, whereas the resistors can be placed in a common island. Both transistors are Schottky clamped; the voltage swing at the input is about 600 mV. Using an SBC process with 3-μm epilayer and 5-μm minimum dimensions, typical gate delays are 4 ns at 5 mW/gate ($Pt_d = 20$ pJ) and 7 ns at 2 mW/gate (14 pJ) with $V_{CC} = 5$ V; packing densities of about 40 gates/mm^2 can be realized. Using the Isoplanar II process with 3-4 minimum dimensions subnanosecond gate delays have been measured [65].

B. Integrated Injection Logic (I^2L)

The standard cell, suitable for wired AND logic, is made with a multicollector

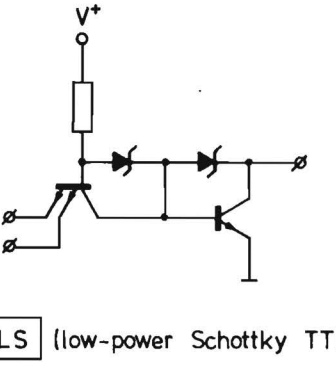

Fig. 9. Circuit diagram of a two-input non-buffered low-power Schottky TTL circuit.

inverse-operated n-p-n transistor, using a saturated lateral p-n-p transistor as a load device (Fig. 10(a)) [66,67]. In the SBC process a n^+ isolation diffusion between the inverse-operated n-p-n transistors is convenient to increase their current gain. The power supply voltage is 0.8-1.0 V and the logic swing is about 700 mV. The packing density of I^2L is the best of all bipolar logics due to the compact structure which does not need the conventional p isolation. The speed, however, is relatively low, because of the low f_T of the inverse--operated n-p-n [68]. By reducing the thickness of the epilayer, the storage of minority carriers (holes) is reduced, which improves the speed. With a 2-μm epilayer and 5-μm

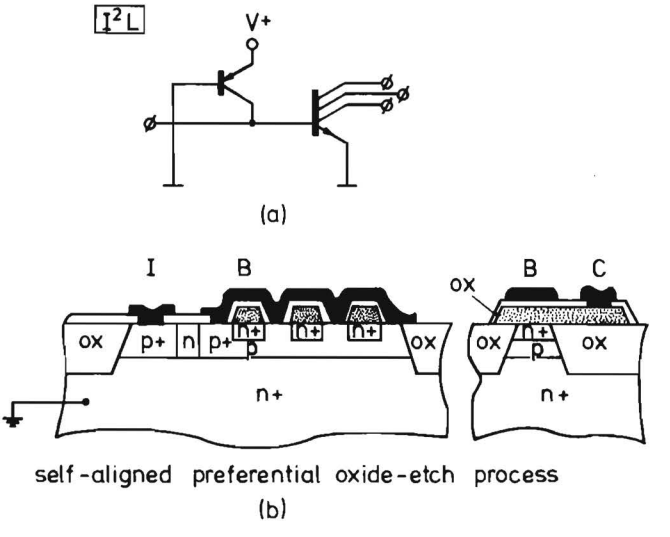

Fig. 10. (a) Circuit diagram of I^2L. (b) A cross-section of I^2L made in the self-aligned preferential-oxide--etch polysilicon process.

minimum details $t_{d\min}$ is 20 ns at 100 μA/gate (1.4 pJ), featuring packing densities of 150 gates/mm^2 [69]. By using oxide isolation and scaling of the dimensions the results can be improved. With a 1.0-μm epilayer and 0.9-μm details $t_{d\min}$ is 3 ns at 200 μA/gate (0.5 pJ) [70]. Although the packing density in this case is very high (up to 1000 gates/mm^2), the speed is still relatively low.

A real improvement is obtained by using the self-aligned polyprocess [32], see Fig. 10 (b). Due to the self-aligned base contacts, the base area of the multicollector n-p-n can be much smaller, which improves the f_T of the inverse n-p-n. The extrinsic base regions between n^+ collectors are stitched together with a metal overlay, reducing series resistances in the length direction of the gate, eliminating the difference in switching times between the first and last collector. For a fanout of 3, with 2.5-μm design rules, I^2L circuits of this type show 0.8 ns gate delays at about 100 μA/gate ($\sim$ 0.1 pJ) [32].

In another approach to I^2L the multicollector inverse-operated n-p-n is replaced by a multicollector inverse-operated static induction transistor (BSIT). With such a structure $t_{d\min} = 3.5$ ns at 300 μA/gate is achieved [70].

C. Schottky Transistor Logic (STL)

Fig. 11(a) shows the circuit diagram of STL [52,72]. The gate is quite similar to I^2L; single-input multiple-output for wired-AND logic. The n-p-n transistor is normally operated and clamped by a Pt Schottky diode. A voltage swing of about 200 mV is obtained either by using Ti Schottky diodes for the output diodes [73], or Pt Schottky diodes with a barrier-height-reducing shallow ion implant. Using oxide isolation and 3.8-μm minimum dimensions $t_{d\min}$ is 0.8 ns at 400 μA/gate (0.64 pJ, when $V_{CC} = 2$ V) has been measured. Even higher speeds have been measured for voltage swings as low as 125 mV, but the safety margins of these circuits may be too low in real circuits, owing to a limited noise margin [4]. Due to the separated load device (resistor or p-n-p in a separate island) the packing density is lower than that of I^2L; however packing densities of 250 gates/mm^2 can be obtained. A problem in STL can be that leakage currents through the lower barrier Schottky diodes affect the noise margin of the circuit.

D. Integrated Schottky Logic (ISL)

In standard bipolar technology (SBC), ISL has been developed to bridge the gap between I^2L (which has VLSI capabilities, but not a very high speed) and low-power Schottky TTL (which features a good speed but consumes too much power). The circuit is similar to STL except for the clamp diode which is replaced by a combined vertical/lateral p-n-p clamp transistor (see Fig. 11(b) and (c)) [50,74,75]. It has been shown that for the same epilayer thickness and the same minimum dimensions ISL is a factor of 5 to 10 faster than I^2L [74]. With an epilayer thickness of 3-μm and minimum details of 5-μm $t_{d\min} = 2.7$ ns is obtained at 200 μA/gate and $V_{CC} = 2$ V (1.2 pJ). The packing density is

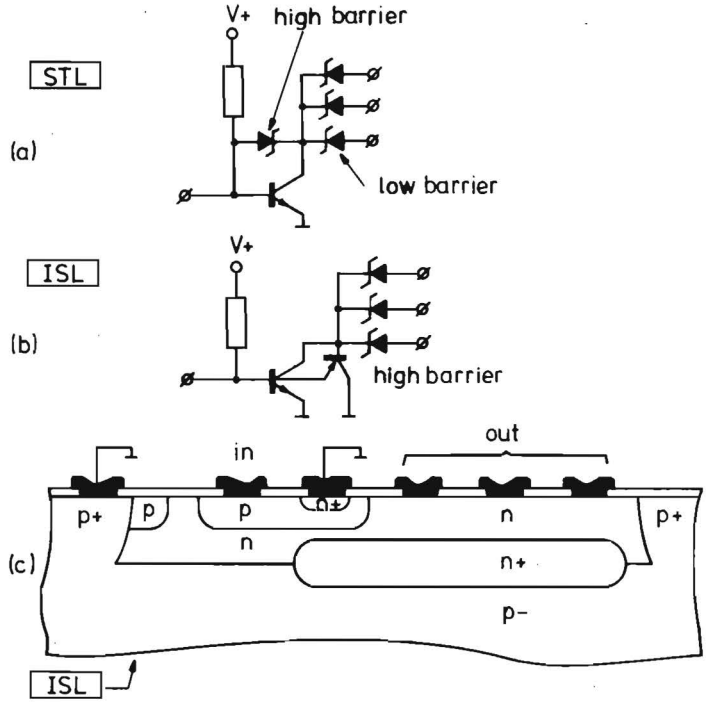

Fig. 11. (a) Circuit diagram of STL. (b) Circuit diagram of ISL. (c) A cross-section of an ISL gate in a p-n isolated process.

about 80 gates/mm^2. Only one type of Schottky diode is needed in this process. To obtain a voltage swing of 200 mV, PtNi-silicide Schottky diodes (60 percent Pt, 40 percent Ni) are used with a Schottky barrier height of 0.78 V. The minimum propagation delay time depends heavily on the storage of minority carriers in the base of the p-n-p. By applying a thinner epilayer and oxide isolation, the slow lateral p-n-p can be eliminated, which improves the speed considerably. With epilayers thinner than 1.5 μm the storage of active charge in the vertical p-n-p will be much smaller than the charge in the junction capacitances, which makes ISL nearly as fast as STL.

Delay times of 0.7 ns at 200 μA/gate and 1 ns at 100 μA/gate have been measured in an oxide isolated process with 1.2 μm epi and 3 μm minimum dimensions, featuring a packing density of about 250 gates/mm^2 [76]. Even oxide isolated ISL with 1.25 μm minimum details has been demonstrated [77].

In another approach to ISL, the p-n-p transistor is replaced by a static induction transistor (BSIT); with this structure $t_{d\min} = 2.5$ ns has been measured at 400 μW/gate [71].

E. Diode Transistor Logic (DTL)

Fig. 12 shows the simplest form of DTL, which is very similar to LS, except that the input devices are diodes (instead of a multi-emitter transistor) and that an extra level-shift diode plus an extra resistor to ground is used. The input and level-shift diodes may be Schottky diodes, but in that case the packing density would be low, because each Schottky diode has to be placed in a separate island. By using lateral polysilicon diodes in the PSA or APSA process, the occupied area of the diodes is very small; also the junction capacitances to ground are minimized with these devices. DTL with polysilicon

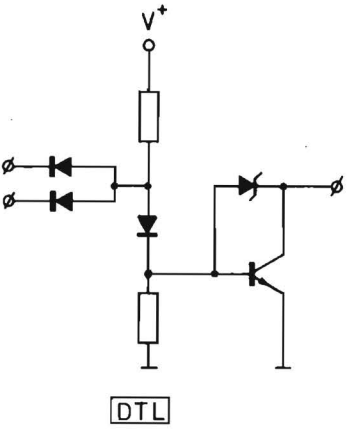

Fig. 12. Circuit diagram of of DTL. The input diodes and level-shift diodes can be either Schottky diodes or lateral polysilicon diodes.

diodes has been realized in the PSA process with 3-4 μm minimum details featuring $t_{d\min} = 1.6$ ns at 0.5 mW/gate (0.8 pJ), and a packing density of 400 gates/mm^2. As all diodes and resistors are formed in the polysilicon layer, only the transistors are made in the crystalline silicon, resulting in very high packing densities [34].

F. Emitter Coupled Logic (ECL)

This type of logic, also called current mode logic (CML) is a non-saturated circuit, which means that no clamping devices are needed; Fig. 13(a) shows the basic diagram. The voltage swing of this logic is 200-700 mV. The circuit can be very fast when transistors with a high f_T are used; in that case the speed is determined by *RC* times [8,9], which means that reduction of junction capacitances and series resistances directly improves the performance of ECL. Although the packing density of ECL is relatively low (because of the large number of components), the logic is more powerful than other circuits, because the inverted output signal is available. This means that the effective packing density of ECL is about 1.4 times the real density. Another feature is that gates can be

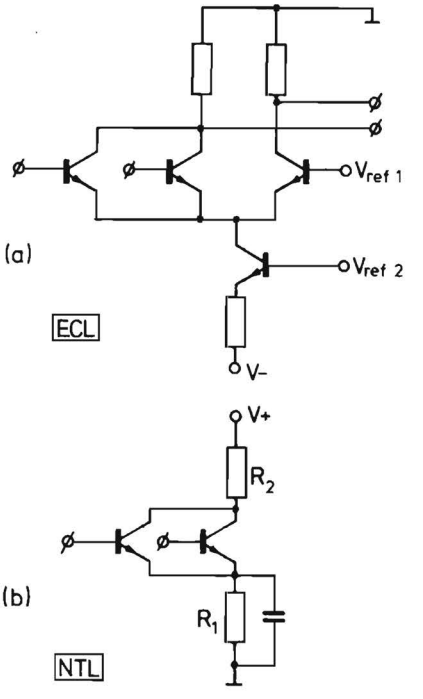

Fig. 13. (a) Circuit diagram of ECL. (b) Circuit diagram of NTL.

stacked, using the same current source (current routing). Using oxide isolation, propagation delay times of 0.5 ns have been achieved at 3 mW/gate (1.5 pJ) [25]; also delay times of 0.35 ns at 2.2 mW (1.3 pJ) have been reported [78]. The effective packing densities are about 150 gates/mm^2.

With the BEST process $t_d = 0.65$ ns at 0.6 mW/gate (0.39 pJ) is achieved [33] and with the APSA process $t_d = 0.29$ ns at 1.48 mW/gate (0.43 pJ) is reported, with packing density of about 200 gates/mm^2 [35]. This means that ECL belongs to the fastest type of logic, however, at the expense of a larger power dissipation. By decreasing the current level a speed degradation occurs, but still very attractive propagation delay times of 1-2 ns can be realized at 200 μW/gate.

G. Non-Threshold Logic (NTL)

NTL is also a non-saturated logic which operates with two resistors with a small resistance ratio ($R2/R1 \approx 1.5$); see Fig. 13(b). The resistor $R1$ is shunted with a speed-up capacitance [79]. The packing density is about the same as for ECL; the speed can be even higher at the expense of smaller noise margins. In a junction-isolated process $t_d = 0.4$ ns with $Pt_d = 8$ pJ has been obtained [80]; in the E^{2}CL process $t_d = 0.085$ ns has been measured with a power delay product $Pt_d = 0.19$ pJ [31].

H. Circuit/Technology Combinations Comparison

To obtain some relevant trends, for the most important circuits, a rough comparison is setup in Table II for three types of processes; SBC, LOCOS and PSA with 3 μm/5 μm, 1-1.5 μm/3 μm and 2 μm/3 μm epithickness/minimum-dimensions combinations, respectively. For I^2L also an experimental process with 0.9 μm min. dimensions,

SBC 3/5	LOCOS 1-1.5/3	PSA 2/3	t_d [ns]	P [mW]	Pt_d [pJ]	Packing density [gates/mm^2]
VLSI requirements →				<.2		>200
LS			7	2	14	40
	LS		3	1	3	100
		DTL	1.6	.5	.8	**400**
I^2L			20	**.07**	1.4	150
	I^2L		5	**.15**	.8	**300**
	I^2L 1/.9		3	**.15**	.5	**1000**
	I^2L 1/2.5 exp. Poly process		.8	**.12**	.1	**500**
	STL		.5	.4	.24	} **250**
	,,		1	**.2**	.2	
ISL			3	.4	1.2	80
	ISL		.6	.4	.24	} **250**
	,,		1	**.2**	.2	
	ECL		.35	2.2	1.3	} 150 eff.
	,,		2	**.2**	.4	
		ECL	.29	1.5	.5	} **200** eff.
		,,	1	**.2**	.2	

TABLE II

Circuit/Technology Combinations Comparison for Three Types of Processes: SBC, LOCOS and PSA with 3 μm/5 μm, 1-1.5 μm/3 μm and 2 μm/3 μm Epilayer/Min. - Details Combinations Respectively. Also Two Experimental I^2L Processes are Listed: a 1/0.9 Oxide Isolation Process and a 1/2.5 Oxide Isolated Self-Aligned Polyprocess. Figures Which Meet the VLSI Requirements are Printed in Bold Figures.

and an experimental self-aligned polyprocess [32] with 2.5-μm design rules are listed.

Most figures can be found in the literature; when published figures belong to other processes then listed in the table, an estimated adaptation has been done.

When figures meet the VLSI requirements, they are printed in bold figures. The most important conclusion from Table II is that the following circuit/technology combinations meet the VLSI requirements: DTL in PSA when operated at a lower power level than listed in the table, ECL in PSA at 200 μW power level, I^2L in LOCOS, STL in LOCOS at 200 μW power level, ISL in LOCOS at 200 μW power level. I^2L has the best packing density but the lowest speed (except for the experimental self-aligned polyprocess). ECL, STL and ISL have the same speed ($\sim$ 1 ns) at 200 μW; STL and ISL have a better packing density.

3.IX. Conclusions

It has been shown that bipolar circuits can continue to play an important role in high performance (fast) LSI and VLSI circuits, due to the facts that power supply voltages and logic swings can be minimized independent of transistor dimensions, and that the speed degradation due to on-chip wiring capacitances is less severe than in MOSFET/MESFET types of circuits. General performance improvements (in speed and packing density) of logic gates are obtained by increasing transistor f_T, and decreasing parasitic capacitances, series resistances and device sizes, by the introduction of oxide isolation, self-aligned techniques and polysilicon electrodes. Fast switching diodes like Schottky barrier diodes and lateral polydiodes improve the flexibility of circuit design. In the choice of circuit type for a given set of minimum details, a trade-off has to be made between speed, power dissipation and packing density.

VLSI requirements can be fulfilled by DTL, I^2L, ECL, STL and ISL, using oxide isolated or polyelectrode processes with 3-μm details. I^2L has the best packing density, but a relatively low speed. ECL, STL and ISL fulfil the VLSI requirements by limiting the power dissipation at 200 μW; in that case all these three circuits will have a propagation delay time of about 1 ns (STL and ISL, however, have a better packing density than ECL). Improvements, both in speed and packing density can be expected when in the future the processes are further scaled and smaller minimum dimensions are possible.

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4

ISL, A Fast and Dense Low-Power Logic, Made in a Standard Schottky Process

Abstract — **Integrated Schottky logic (ISL) is a new 200 mV voltage-swing LSI logic that can be made in standard Schottky processes with a double-layer metallization. It fills the gap between low-power Schottky TTL and I^2L for those circuits where low-power Schottky TTL consumes too much power and takes up too much chip area, and when I^2L does not attain the required speed. An ISL gate consists of a current source, a normally operated n-p-n transistor with a merged p-n-p transistor, and a set of Schottky output diodes (wired AND gate). The merged p-n-p transistor clamps the n-p-n transistor and prevents the n-p-n from going too deeply into saturation. Minimum propagation delay times of 2.7 ns at 200 μA/gate are obtained, with a speed-power product of 1.2 pJ. The packing density of ISL is 120 to 180 gates/mm^2. Notwithstanding the small voltage swing, the noise margins of ISL are in most cases better than the noise margins of I^2L. The logic can be combined with ECL, I^2L, and TTL on the same chip, and can also be made in analog processes. Proposals are given on how to make ISL in advanced oxide isolated processes in which propagation delay times below 1 ns can be obtained.**

4.I. Introduction

A gap exists between low-power Schottky TTL (LS) and integrated injection logic (I^2L), both of which are commercial circuits that can be made in standard processes with a high production yield.

Though I^2L has the advantages of high packing density and low power consumption, it cannot attain the speeds desirable for many applications. Low-power Schottky TTL, on the other hand, features good speed but consumes too much power and takes up too much chip area for LSI.

The wish to fill this gap with a new logic that can also be made in a standard process has led to the invention of integrated Schottky logic (ISL) [1,2].

A predecessor of ISL was a proposal named Schottky-diistor logic [3], consisting of a current source, an n-p-n transistor, and a set of Schottky diodes (see Fig. 1). Later,

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the name of this logic was changed to Schottky coupled transistor logic (SCTL) [4]. The logic swing of SCTL is about 200 mV, being the difference between the base/collector voltage of the saturated n-p-n transistor and the forward voltage of the Schottky diode. In SCTL the n-p-n transistor can be used either in the normal downward-operated mode or in the reverse mode. When the n-p-n is used in the normal mode, this transistor will go heavily into saturation in the ON state, causing a large saturation delay. When the reverse mode is used, the current source can be merged with the n-p-n transistor as in I^2L [5,6];

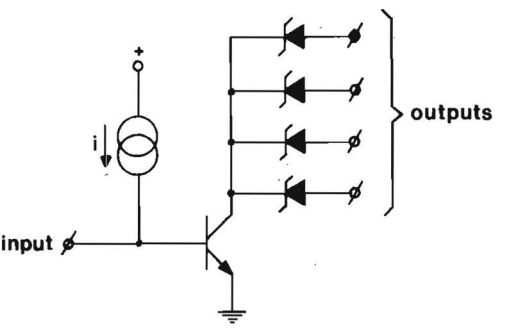

Fig. 1. Schottky-diistor logic, later called SCTL, consisting of a current source, an n-p-n transistor, and a set of Schottky fan-out diodes [3,4].

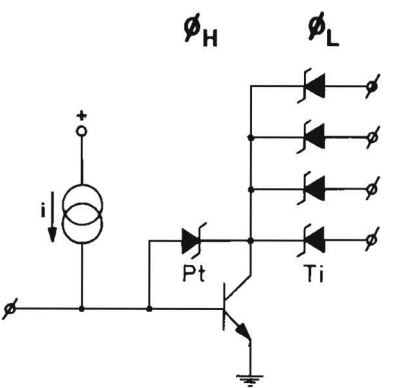

Fig. 2. Schottky transistor logic (STL [18] or C^3L [19]), which has a Schottky clamp to keep the n-p-n transistor out of saturation. This concept is best seen from an electronic standpoint, but is not producible in a standard process, because two types of Schottky diodes are needed with different Schottky barrier heights.

in this case, the maximum speed, however, is limited by the low cut-off frequency of the n-p-n by the same amount as in I^2L. This means that SCTL is not very much faster than I^2L, if compared in the same process [7].

Seen from a purely electronic standpoint, the best way to obtain a high speed is to use the n-p-n in the normal mode and prevent saturation by Schottky clamping. To ob-

tain a logic swing, two types of Schottky diodes with different barrier heights have to be used. This type of logic has been introduced under the names of Schottky transistor logic (STL) [8] and complementary constant current logic (C^3L) [9]. Fig. 2 shows the basic diagram. The clamp Schottky diode must have a sufficiently low barrier height to keep the n-p-n out of saturation. The output Schottky diodes must have a barrier height about 200 mV lower than the barrier height of the clamp diode. For instance, titanium output diodes together with a platinum clamp diode can fulfill the requirements. The current source can be either a p-n-p transistor or a resistor.

A technological drawback of STL is the fact that it cannot be made by existing standard processes, in which only one type of Schottky diode is available. This means that if the object is to obtain a speed improvement within a standard process, a change has to be made at mask level rather than at process level.

Sacrificing a bit of the inherently excellent speed of STL, it is possible to replace the fast Schottky clamp diode by a somewhat slower silicon clamp device.

Silicon clamp devices can be made with normally operated n-p-n transistors [10] or with merged inversely operated n-p-n transistors [11-13] used as diodes. Both methods provide a clamp over the base/collector junction of the n-p-n transistor used in the logic circuit. The first method requires an extra collector island per logic gate, which is a drawback for large-scale integration, and the second method only works effectively if the inverse current gain is high, which is mostly not the case in standard processes.

Other approaches reduce the current gain of the n-p-n in the logic circuit by shunting the base/emitter junction with a transistor structure, for saturation control [14, 15]. However, the current gain has to be decreased to very low values to decrease the minority carrier storage of the saturated n-p-n; for those low values of β the noise margin of STL-type logic circuits will be unacceptably low [16].

In this paper a new logic, ISL, is introduced which uses a p-n-p as a silicon clamp device to keep the n-p-n transistor out of heavy saturation. Although the new logic is not as fast as STL, the concept can be implemented in a standard process, and it turns out that the logic is considerably faster than I^2L. This means that the gap between low-power Schottky TTL and I^2L can now be filled.

4.II. Principle of Integrated Schottky Logic

It has been found that the saturation delay can be reduced considerably by the introduction of a merged p-n-p transistor that controls the saturation of the n-p-n transistor.

This leads to the ISL concept shown in Fig. 3. The n-p-n transistor still goes into saturation, but no longer as heavily, because most of the n-p-n input current is drained off to ground by the p-n-p as soon the n-p-n base/collector junction becomes forward biased. A first-order calculation shows that the logic voltage swing equals $(kT/q)\ln(\alpha_{\text{p-n-p}} I_{d0}/I_{p0})$,

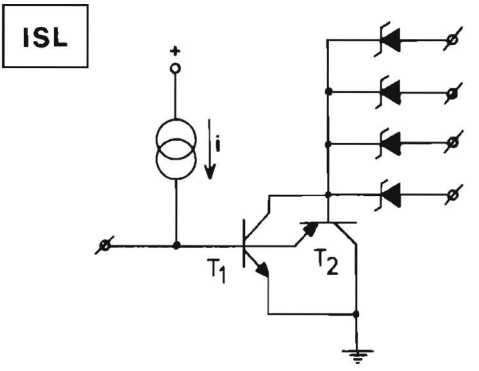

Fig. 3. Integrated Schottky logic (ISL) which can be made in a standard process. A merged p-n-p transistor is added to the n-p-n to control the degree of saturation. It has been found that the saturation delay is reduced considerably by the n-p-n clamp transistor.

where I_{d0} and I_{p0} are the saturation currents of the Schottky diode and p-n-p transistor, respectively. If the n-p-n transistor T_1 is a normal downward-operating n-p-n, the p-n-p transistor T_2 is, in fact, already present as the parasitic substrate p-n-p. In ISL, this parasitic p-n-p is deliberately enhanced in order to fulfill the saturation control requirements. Two methods have been used to enhance the parasitic p-n-p without causing an increase in n-p-n transistor size: 1) around the base of the n-p-n transistor a shallow p-ring in the shape of a horseshoe is diffused, which overlaps the isolation diffusion; and 2) a vertical substrate p-n-p is introduced by applying a shorter buried layer than is usual for the n-p-n transistor [17] (see Fig. 4).

No shallow p-stripe is needed between the base of the n-p-n and the first Schottky diode. Holes injected by the base in the n-area under the first Schottky diode will be collected by this diode. At that place the holes recombine immediately, causing a small increase in current through the diode. This current increase does not affect the behaviour of the gate.

The minimum propagation delay of ISL depends to a great extent on the amount of holes stored in the base areas of the composite p-n-p (lateral and vertical) [18,19]. The overall effective cut-off frequency belonging to the composite p-n-p is increased by making either a thinner lateral p-n-p base or a thinner vertical p-n-p base. The thickness of the lateral p-n-p base is limited by lithographical and diffusion tolerances and cannot usually be made thinner than 3 μm. The thickness of the vertical p-n-p base is determined by the epilayer thickness minus the shallow p diffusion depth and can easily be made thinner than 3 μm, resulting in a high p-n-p cut-off frequency.

To avoid crossing problems with the ground line (which has to ground all emitters) and logic interconnection lines (which have to interconnect base nodes with fan-out

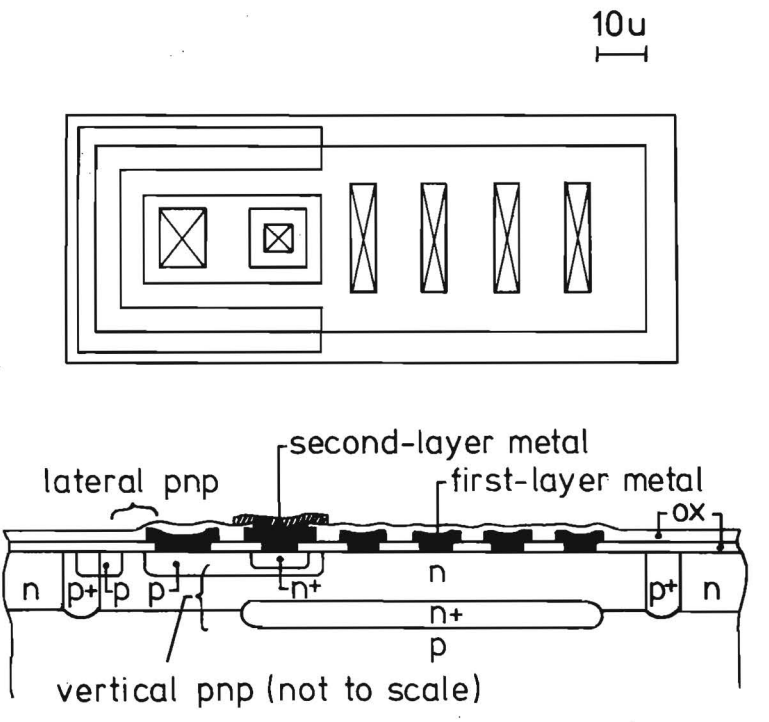

Fig. 4. Cross-section of an ISL gate without current source. The p-n-p transistor consists of two parts: a lateral one and a vertical one. With thin epitaxial layers, the base of the vertical p-n-p can be made thinner than the lateral p-n-p base, which improves the speed.

Schottky diodes), a double-layer metallization can successfully be used. As shown in Fig. 4, a via is made on top of the emitter, which makes it possible to interconnect all emitters with a second-layer metal line.

4.III. Current Sources

The current sources needed to supply current to each ISL input can be either p-n-p transistors or resistors. If p-n-p transistors are used, they cannot be merged with the n-p-n transistors as in I^2L, owing to the fact that the n-p-n transistors are used in the normal downward mode. This means that an extra (common) island has to be made for these p-n-p's. Despite a somewhat worse power economy [20], the island potential, which is the base potential of all current-source p-n-p's, should be some 200 mV higher than the ground potential to keep the p-n-p's out of saturation. This measure results in maximum possible noise margins [16,21] because, in that case, the β of the n-p-n is not affected by the back-injection effect in the p-n-p.

Instead of p-n-p's, one can also use resistors. In that case, the power-supply voltage has to be increased somewhat to prevent excessive modulation of the currents flowing in

resistors connected to gates that are ON and OFF.

The introduction of the extra current-supply island, with either p-n-p's or resistors, implies that the packing density of ISL is smaller than the packing density of I^2L when compared in the same process.

4.IV. Layout Technique

The layout technique of ISL is very similar to that of I^2L. As Fig. 5 shows, gates are laid out perpendicular to a current-supply island; in this example, resistors are used at half the pitch of the minimum pitch in which the ISL gates can be placed. The layout example comprises two *D*-flip-flops and shows how the two layers of metallization are used. The first layer is used to make the logic interconnections and the connections between base nodes and current sources. The second layer is used to interconnect all emitters and to interconnect the resistors at the power-supply side. If first Schottky diodes (i.e., those closest to the base of the n-p-n transistor) are not used in the logic interconnection, they can be left floating (see Fig. 5). These floating Schottky diodes still collect holes and will be automatically forward biased to collect an electron current to compensate for the collected hole current.

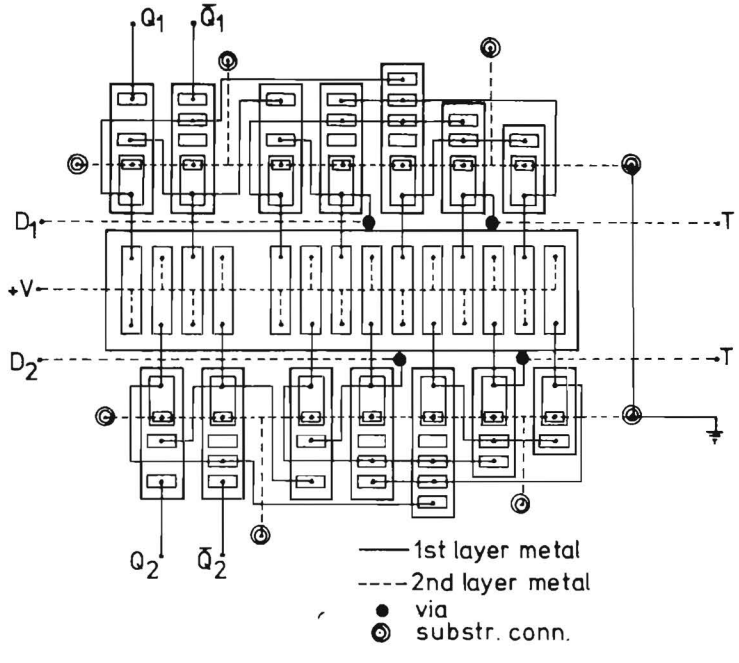

Fig. 5. Example of the layout technique of ISL (two *D*-flip-flops). The gates are placed perpendicular to a current supply island with resistors. Two-layer metallization is used. Floating Schottky diodes can be placed if the first Schottky diode has no logic function to improve the speed.

If a complicated fan-out wiring affects the packing density in some particular interconnection cases, simpler and denser layouts may be obtained by the introduction of some extra islands with fan-out Schottky diodes (see Fig. 6). With such a solution, the fan-out wiring can be placed at the most convenient positions. This method is particularly convenient for clock line distribution to registers, for example [22].

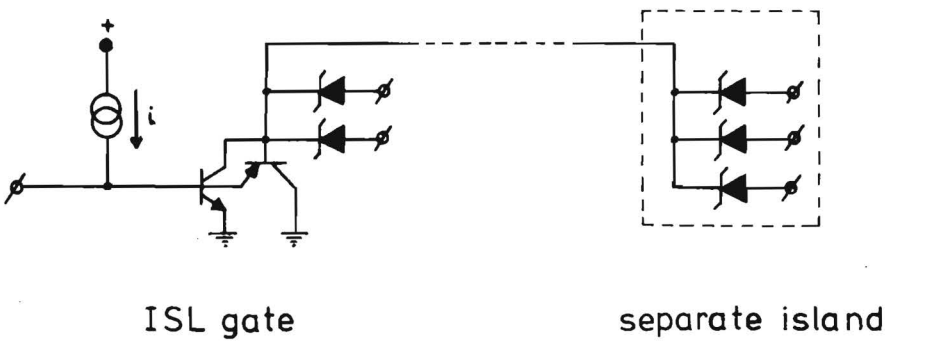

Fig. 6. Schottky diodes can be placed in an extra island to avoid complicated interconnection problems.

4.V. Processes and Propagation Delay Measurements

ISL has been made in two processes, both using double-layer metallization and PtNi Schottky diodes (60-percent Pt and 40-percent Ni) with a Schottky barrier height of about 0.78 eV. The first process *A* has a 3.2 μm thick epitaxial layer, n-type, 0.7 Ω•cm, and normal-cut emitters. The second process *B* has a 2.9 μm thick epilayer, n-type, 0.3 Ω•cm, with washed emitters and ion-implanted resistors of 1500 $\Omega/\square$.

Table I shows some relevant parameters of both processes. In both cases, the logic swing is about 210 mV. For process *A*, p-n-p current sources are used; while for process *B*, ion-implanted resistors of 5 kΩ are taken as current sources. For both processes, 5 μm minimum details are used. Fig. 7 shows the propagation delay versus current per gate, measured with 11-stage ring oscillators for both processes. With the p-n-p's as current sources (curve 1 in Fig. 7), the logic can be driven at each current level; with the resistors as current sources (curve 2 in Fig. 7), the logic operates only when a sufficient voltage drop is developed over the resistors.

The speed-power product at low current levels is 0.5 pJ for process *A* (curve 1) and 0.25 pJ for process *B* (curve 2) (calculated with $V_{CC} = 1$ V).

	process A	process B
n-type epilayer		
thickness [μm]	3.2	2.9
ρ [Ωcm]	0.7	0.3
base diffusion		
junction depth [μm]	1.7	1.2
sheetresistance [Ω/□]	200	200
ion-impl. resistors		
junction depth [μm]	1	0.5
sheetresistance [Ω/□]	1500	1500
emitters	cut	washed
junction depth [μm]	0.9	0.6
sheetresistance [Ω/□]	10	12

TABLE I
Some relevant process parameters of processes *A* and *B* used for the ISL devices.

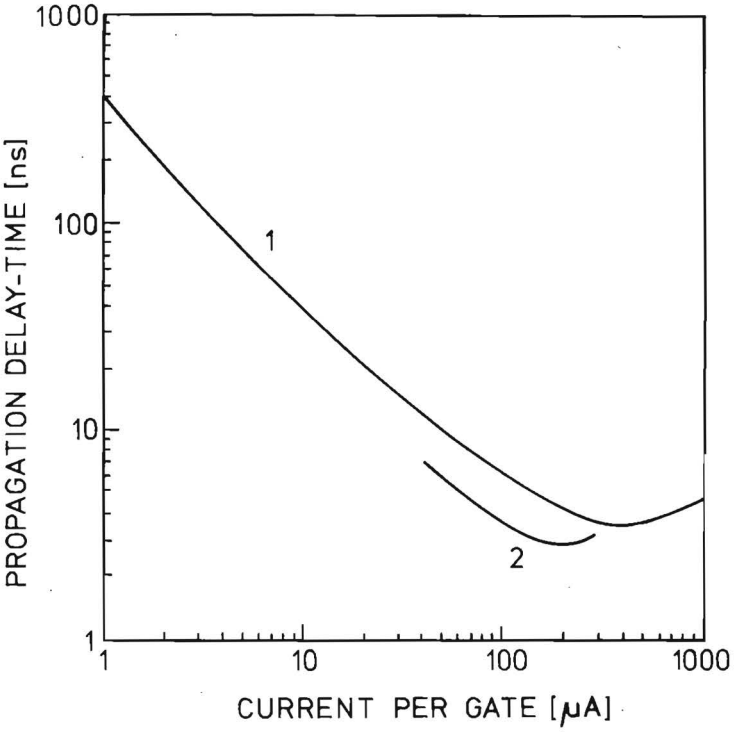

Fig. 7. Propagation delay per gate versus current per gate, measured for two processes. Curve 1 has been measured for a ring oscillator with p-n-p current sources, made in process *A* with 3.2 μm epilayer, 0.7 Ω·cm, and normal cut emitters; curve 2 was measured for a ring oscillator with ion-implanted resistors as current sources, made in a process *B* with 2.9 μm epilayer, 0.3 Ω·cm, with washed emitters.

The minimum propagation delay time is 3.5 ns at 400 μA for process *A* and 2.7 ns at 200 μA for process *B*. The speed-power products at these minima are 1.4 pJ (with $V_{CC} = 1$ V) and 1.2 pJ (with $V_{CC} = 2$ V) respectively.

The better results from process *B* are due to the much smaller emitter area of the n-p-n (less C_{be} capacitance) and to the thinner epilayer (less storage of holes).

Figs. 8 and 9 show photomicrographs of test *D*-flip-flops made in process *A* with p-n-p current sources (Fig. 8) and in process *B* with resistors (Fig. 9). The flip-flop in Fig. 8 has closed p-rings around the n-p-n base, whereas, the flip-flop in Fig. 9 has horse-shoe rings that are open at the Schottky sides. Note that in the flip-flop of Fig. 9 no floating Schottky diodes are present at the first Schottky positions. With the flip-flop made in process *A*, a maximum toggle frequency of 60 MHz was measured. With the flip-flop made in process *B*, the maximum frequency measured was 70 MHz.

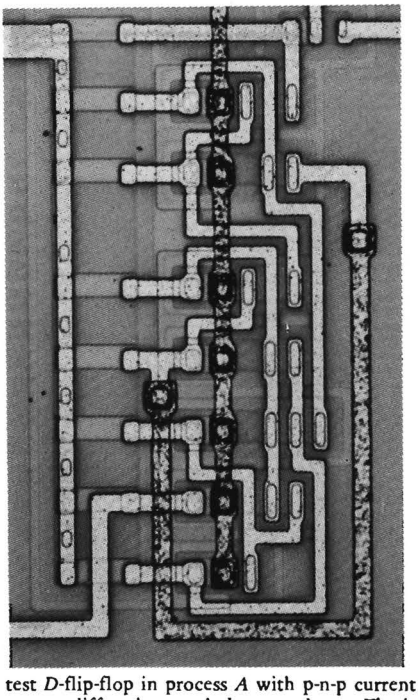

Fig. 8. Photomicrograph of a test *D*-flip-flop in process *A* with p-n-p current sources. In this particular structure, closed shallow p-rings are diffused around the n-p-n bases. The bases of the current supply p-n-p's are kept at a reference potential. A maximum toggle frequency of 60 MHz has been measured for this flip-flop.

4.VI. Fan-out, Fann-in; Speed Comparison with I^2L; Absence of Parasitic SCR-Latching

Measurements have shown that a fan-out of 4 can be realized without difficulties. There is no increase in delay time for the more removed Schottky diodes. This is an advantage over I^2L, where the increasing base series resistance causes an increasing propagation delay time for the more removed collectors.

An interesting feature of ISL is that the minimum propagation delay time decreases with increasing fan-out [18,19]. This is caused by the fact that the minimum propagation delay time depends on the time needed for the removal of the active charge stored in the base of the merged p-n-p. For this removal action a discharge current has to flow through the fan-out diodes. If more fan-out diodes are available also, more discharge current is available and the faster the active charge is removed from the p-n-p base [18].

On the other hand, the ISL propagation delay time can increase for fan-in > 1 in some particular switching cases. This can happen if two or more ISL gates have to switch OFF simultaneously and if these gates have to share discharge current in the case where some of their fan-out diodes are connected to the same input node of another ISL gate [19].

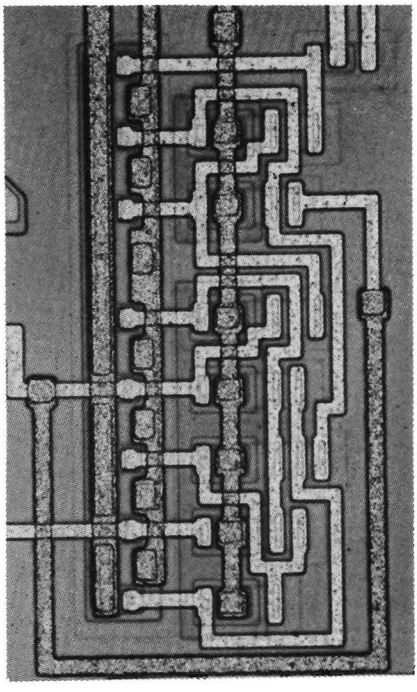

Fig. 9. Photomicrograph of a test *D*-flip-flop in process *B* with ion-implanted resistors as current sources. The shallow p-rings around the n-p-n bases are in the shape of a horseshoe. In this particular flip-flop, no floating Schottky diodes are placed at the first Schottky positions. A maximum toggle frequency of 70 MHz has been measured for this flip-flop.

It can be shown, both theoretically and experimentally, that the minimum propagation delay time of ISL is a factor of 5 to 10 smaller than the minimum propagation delay time of I^2L, if compared in the same process [18]. It appears that ISL is faster because of a different switching behaviour, and also because of the fact that in most cases the cut-off frequency of the merged p-n-p in ISL is higher than the cut-off frequency of the inversely operated n-p-n transistor in I^2L.

It has been shown [23] that parasitic silicon-controlled rectifier (SCR) latching can occur between a Schottky diode and an adjacent n-p-n transistor. In that case, the injection of holes by the forward-biased Schottky diode creates a lateral p-n-p where the Schottky diode acts as emitter and the base of the n-p-n transistor as collector. The combination of the downward-operated n-p-n and the lateral p-n-p transistor forms an SCR. In order to keep the SCR from latching, the product of the common-emitter current gains β_n and β_p of the n-p-n and p-n-p transistors has to be smaller than 1.

In ISL, a parasitic SCR latching may occur between the n-p-n and the first Schottky diode. Measurements have shown that the current gain product $\beta_n\beta_p$ remains well below 0.1 up to current levels of 10 mA per gate. This means that for the practical

current levels, which are even below 1 mA per gate, there is no reason to fear any parasitic SCR-latching problem with the type of Schottky diodes presented.

4.VII. Noise Margins of ISL (Comparison with I^2L) [16,21]

Due to the fact that ISL has a smaller voltage swing than I^2L, it has a smaller worst case static voltage noise margin (ΔV_{series}) than I^2L has. However, this type of noise, which is mostly generated by inductive coupling, hardly appears in integrated circuits. At room temperature the ΔV_{series} is about 100 mV for ISL with a logic swing of 200 mV.

The worst case static ground-line noise margin ΔV_{gnd} of ISL is much better than that of I^2L, due to the fact that the current source is a resistor or a non-saturated p-n-p rather than a saturated p-n-p as in I^2L. At room temperature, the value of ΔV_{gnd} is about 50 mV for ISL with a voltage swing of 200 mV.

The worst case static relative parallel-current noise margin ($\Delta i/i$) is usually better in ISL than in I^2L because the current gain of the normally operated n-p-n in ISL is usually higher than that of the inverse-operated n-p-n in I^2L. At room temperature, $\Delta i/i > 0.5$ for ISL if $\beta_{n\text{-}p\text{-}n} > 20$ for a fan-out of 4.

The worst case static power-supply voltage noise margin of ISL (which can be calculated from $\Delta i/i$) will be large when resistors are used as current sources. In the case of p-n-p current sources the variation of the power-supply voltage is limited to about $(kT/q)\ln(1 + \Delta i/i)$ and will be 10 mV at room temperature for $\Delta i/i = 0.5$. This value is rather low but still better than for I^2L, where $\Delta i/i$ is lower in most cases.

All mentioned static noise margins will decrease at very high current levels due to the collector series resistance of the n-p-n transistors and the individual series resistances of the Schottky diodes.

The dynamic noise margins are larger than the static margins; the energy noise margins have minima between 0.5 and 1.0 pJ, but their meaning as a figure of merit is doubtful [21].

4.VIII. ISL in Analog Processes

As analog processes use a thicker epitaxial layer (7-15 μm) to obtain a certain required base/collector breakdown voltage, the ISL vertical merged p-n-p is no longer effective as a current sink. Nevertheless, the p-ring around the base can sink enough current, and the overall effective cut-off frequency belonging to the composite p-n-p will still be higher than the cut-off frequency of an inverse operated I^2L n-p-n transistor made in the same process. This means that in analog processes, too, ISL will be 5 to 10 times faster than I^2L [18]. ISL has been measured in an 6.5 μm epitaxial process, having a minimum propagation delay of 8 ns.

4.IX. Advanced ISL Proposals

Decrease of the minimum details, together with the reduction of the thickness of the epitaxial layer and the application of oxide isolation, will improve the speed of ISL. It has been shown [24] that the minimum propagation delay time of ISL will be about 800 ps for 1 μm minimum details together with a minimized epilayer thickness. I^2L remains slower; $\tau_{min} = 2$ ns for the same process [24].

Another proposal is to use the merged inversely operated n-p-n clamp method [11-13] in an advanced oxide isolated process, as shown in Fig. 10(a). Basically, an n-type epilayer is used. At the location of the n-p-n transistors, the epilayer is p-overdoped with an ion implantation and acts as base area. This makes the n-p-n transistors practically symmetrical, which results in a high inverse current gain. Two emitter diffusions are made. The base contact overlaps the second emitter. Fig. 10(b) shows the electrical diagram. Computer simulations have shown that a minimum propagation delay of 1 ns will be obtained for $W = 1$ μm and 0.5 ns for $W = 0.7$ μm, where W is the base thickness between the emitters and buried layer.

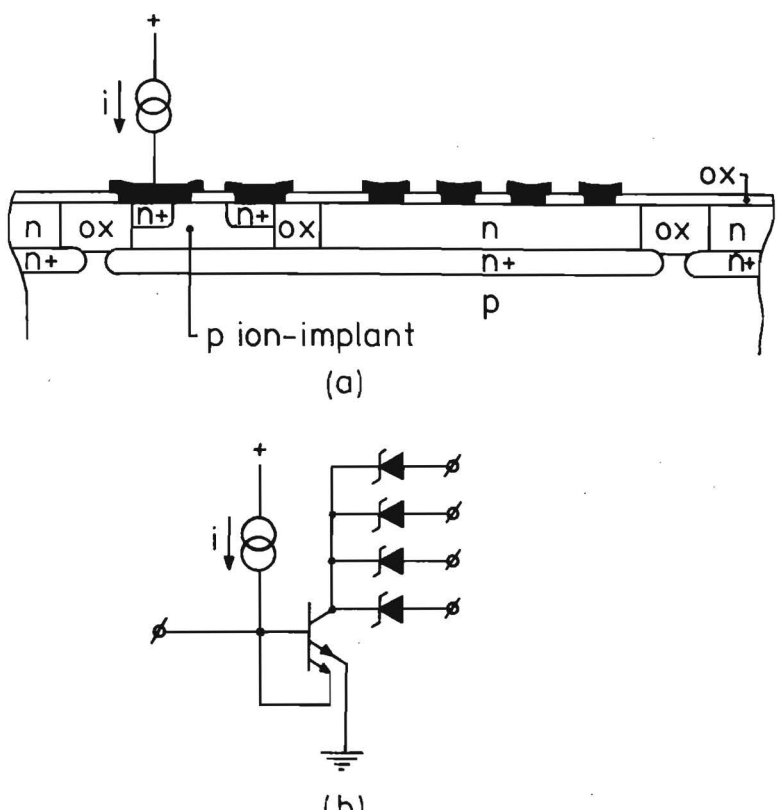

Fig. 10. Example of an advanced ISL proposal using the merged inversely operated n-p-n clamp method. A cross section is given in (a) and the electrical diagram in (b). Propagation delays below 1 ns can be realized with this structure.

4.X. Conclusions

ISL is a new 200 mV voltage-swing LSI logic that can be made in standard Schottky processes with a double-layer metallization. The minimum propagation delay is 5 to 10 times better than that of I^2L made in the same process. Although the packing density is lower than that of I^2L (about 40 percent less), the improvement in packing density and power consumption is dramatic compared with low-power Schottky TTL. This means that circuits that require a TTL speed and a real LSI complexity can be made in ISL. It is also possible to combine ISL with ECL, I^2L, and TTL on the same chip.

Table II gives a comparison of ISL with I^2L and low-power Schottky TTL, all three made in the same process with an epitaxial layer of about 3 μm thick and the same minimum details of 5 μm. The table shows the packing density, speed-power product, minimum propagation delay time, and *D*-flip-flop toggle frequency. As both ISL and I^2L have to be buffered with TTL circuitry to increase the noise margins at the chip interface, the

	Low Power Schottky TTL	ISL	I^2L
average packing density			
centre of chip	15-20	120-180	200-280
complete chip	10-20	60-100	120-180
[gates/mm^2]			
speed-power product [pJ]	19	0.5-1.5	0.5-2
V_{CC} [V]	5	1-3	0.7-1
min. prop. delay-time [ns]	5-10	2-5	10-20
D-flipflop maximum toggle frequency [MHz]	33	60	18

TABLE II
Comparison of ISL with I^2L and low-power Schottky TTL, all three made in the same process with an epitaxial layer about 3 μm thick and with the same minimum dimensions (5 μm).

average packing density of the gates together with the buffer circuits will (depending, of course, on the number of input and output pins) be smaller than the packing density in the middle of the chip. Furthermore, ISL can be combined with analog circuitry in analog processes with some reduced performance.

Notwithstanding the small voltage swing, the noise margins of ISL are in most cases even better than the noise margins of I^2L, specifically if resistors are used as current

sources. This means that ISL is a more "forgiving" circuit than I^2L [25].

In the future, speed improvements of ISL can be made with advanced oxide isolated processes. With minimum dimensions of 1 μm, the propagation delay time can be 0.8 ns; using the merge inversely operated n-p-n clamp approach, delay times between 0.5 and 1.0 ns can be realized.

Acknowledgment

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5

Oxide-Isolated ISL Technologies

J. Lohstroh, J.D.P. v.d. Crommenacker, and A.J. Linssen

Abstract — **Using oxide isolation, ISL gates can be fabricated without the relative slow lateral p-n-p transistor which is inevitable in pn-isolated processes. Now the clamping action is provided either by a fast vertical p-n-p only, or a reverse operated n-p-n. Using a 1.2 μm thick epilayer and 3 μm minimum dimensions, propagation delay times of 0.7 ns are obtained at a current level of 200 μA per gate.**

Oxide isolated ISL (Integrated Schottky Logic) is a fast bipolar logic with a high packing density and a low-power consumption, highly suitable for high speed VLSI.

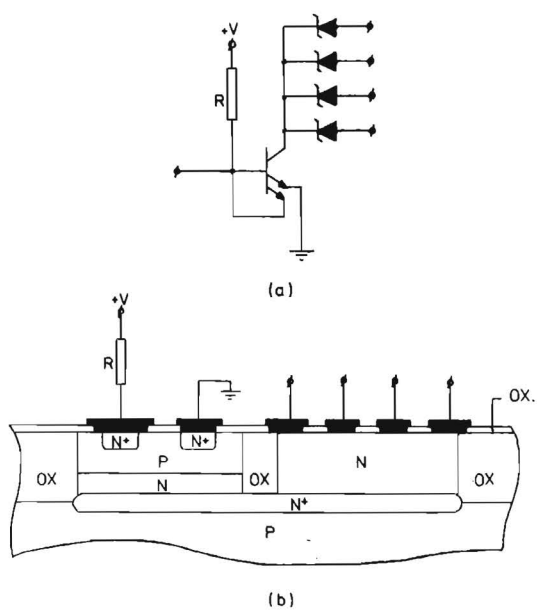

Fig. 1. Oxide isolated ISL gate using a vertical p-n-p clamp (type *A*). Circuit diagram (a) and not-to-scale cross-section (the emitter is walled in the direction parallel to the cross-section) (b).

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The ISL gate is a single input, multiple output wired-AND gate with an n-p-n driver transistor and Schottky diode outputs. Clamping of the n-p-n transistor is provided by either a vertical p-n-p (type *A*, see Fig. 1) or a reverse operated n-p-n (type *B*, see Fig. 2) [1].

In oxide isolated processes the n-p-n base can be completely walled (4 sides) by oxide, fully eliminating the relatively slow lateral p-n-p which is inevitable in pn-isolated processes [1,2].

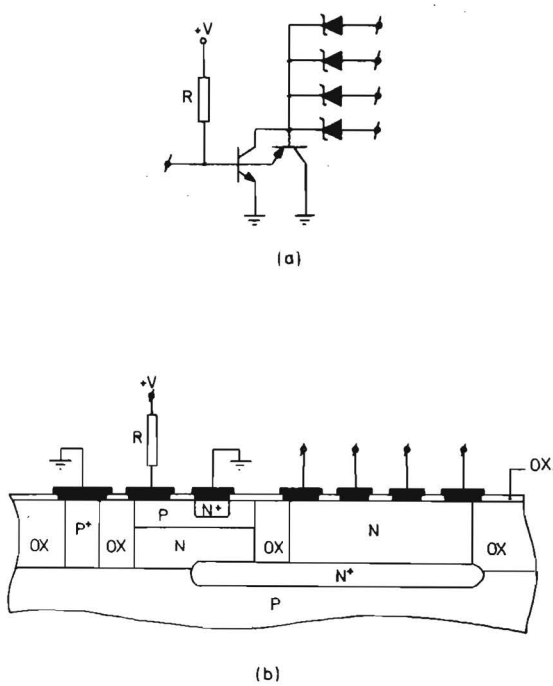

Fig. 2. Oxide isolated ISL gate using a reverse operated n-p-n clamp (type *B*). Circuit diagram (a) and not-to-scale cross-section (the emitter is walled in the direction parallel to the cross-section) (b).

A non-optimized form of oxide isolated ISL has been published [3], where the base is walled on three sides; in this structure still parasitic minority carrier storage will occur in the lateral p-n-m-structure, decreasing the f_T of the composite clamping p-n-p.

Although in principle the switching speed of oxide isolated ISL will be somewhat slower than of oxide isolated STL (Schottky Transistor Logic), due to minority carrier storage in the clamp device (p-n-p or reverse operated n-p-n), the speed difference will be very small as soon as the amount of this in minority carrier charge is small compared with the charge in the junction capacitances. This is the case when a shallow epitaxial layer is used; then ISL is made with a high performance and in a simpler process than STL which uses two types of Schottky diodes [4]. Further leakage problems, which can occur in

the lower barrier height Schottky diodes in STL [5], will not be present in ISL which uses Schottky diodes with a relatively high barrier height.

ISL gates have been made in a standard oxide isolated process using a 5 Ω•cm substrate, a Sb buried layer, a 1.2 μm thick epitaxial layer (0.6 Ω•cm), ion implanted walled bases (0.5 μm and 0.7 μm thick for type *A* and *B* respectively), ion implanted two-sides--walled As emitters (0.25 μm), and walled PtNi-silicide Schottky diodes with a barrier height of 0.78 eV. Type *A* has been fabricated with 3 μm minimum dimensions and type *B* with 2.5 μm minimum dimensions, featuring maximum packing densities of 250 and 400 gates/mm^2 respectively.

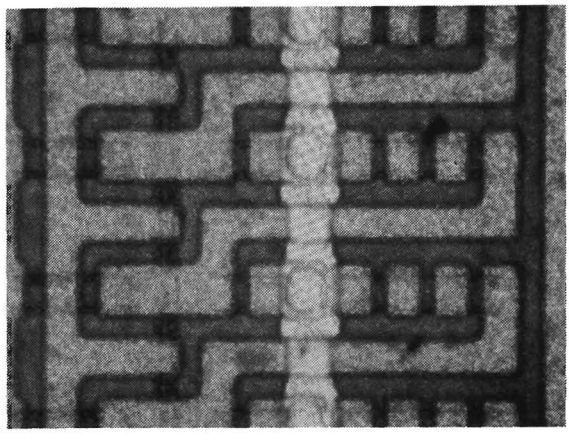

Fig. 3. Photograph of a part of a 21-stage ring-oscillator, built-up with gates of type *A* (fan-out = 4), using 3 μm minimum details.

Fig. 3 shows a photograph of a part of a 21-stage ring-oscillator built-up with gates of type *A*. The current sources are ion-implanted resistors of 12 kΩ; the gates have a fan--out of 4.

Fig. 4 shows the measured propagation delay times of both type *A* and *B*. In spite of the somewhat smaller dimensions, type *B* (with the reverse operated n-p-n clamp) is slower than type *A*. This is caused by the facts that a) the area of the feedback emitter is only 16% of the total n-p-n base area and b) hole storage is present in the epilayer between the n-p-n base and buried layer (the buried layer acts as emitter for the reverse operated n-p-n). Speed improvements are possible by increasing the feedback emitter size and/or decreasing the epi-thickness to achieve a direct contact between the base and the buried layer.

Type *A* which, uses the vertical p-n-p clamp, shows a very good performance. Propagation delays of 0.7 ns at 200 μA/gate are measured (τD = 200 fJ for a power supply voltage of 1.6 V).

Both types have a logic swing of about 190 mV.

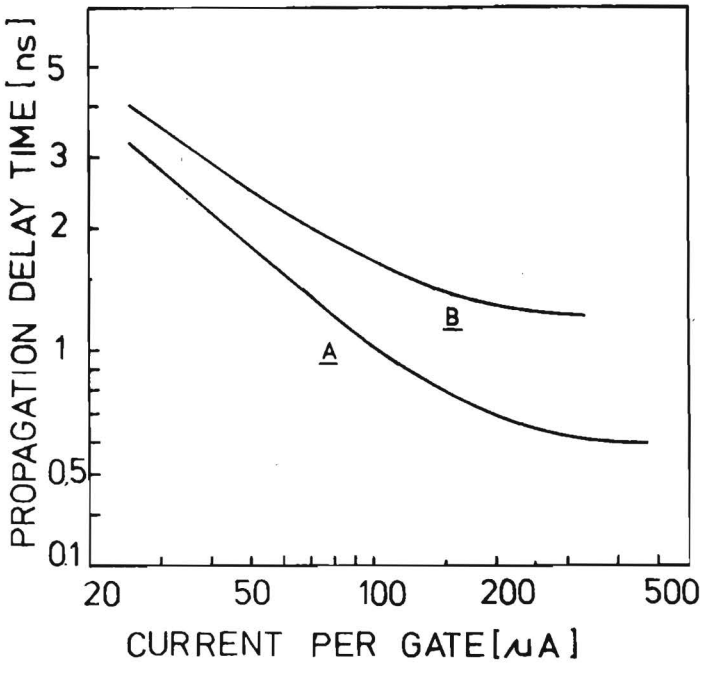

Fig. 4. Measured propagation delay times of gates of type *A* and *B*.

CONCLUSION

Oxide isolated ISL is made in a rather simple process and features sub-nanosecond propagation delay times with sub-picojoule speed-power products. This makes this type of logic very attractive for high speed VLSI.

A good clamping action is provided by the vertical p-n-p transistor. The clamping action of the here presented reverse operated n-p-n transistor can be further improved.

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6

Performance Comparison of ISL and I^2L

ISL (Integrated Schottky Logic) [1,2,3,4] and I^2L are both bipolar LSI logic circuits that can be processed in standard, pn-isolated, (Schottky) processes. Figure 1 shows an example of an ISL-*D*-flip-flop [1]. Good functioning circuits with more than 500 ISL gates have already been made. In I^2L the n-p-n transistors are used in the inverse mode;

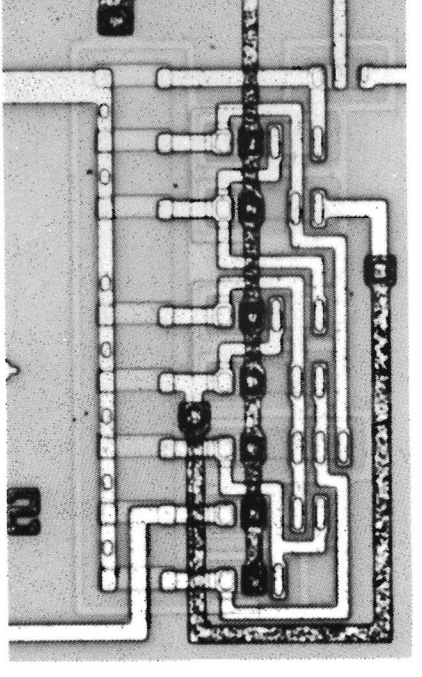

Fig. 1. ISL-D-flip-flop with resistors as current sources [1].

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the p-n-p current sources can be merged with the n-p-n's in a very area-saving way. In ISL the n-p-n transistors are used in the normal mode; in this logic the current sources (p-n-p's or resistors) have to be made in a separate island, which means that the packing density is smaller compared to that of I^2L [1,2]. For speed, however, ISL outrivals I^2L.

For comparison, we can consider ISL and I^2L gates which are made in the same process with the same epi-layer thickness and same minimum dimensions; Figure 2.

For small currents ISL will be faster than I^2L because of the smaller voltage swing (200 mV instead of 700 mV), while the junction capacitances are comparable.

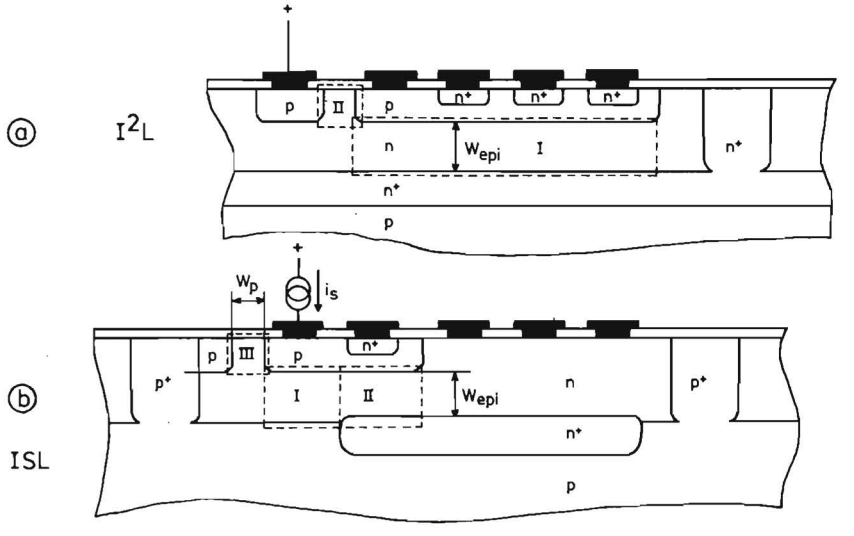

Fig. 2. Cross section of I^2L (a) and ISL (b) made in a standard process. Active charge will be found mainly in areas I and II (I^2L) and I, II and III (ISL).

At high current levels, at maximum speed, the active charge dominates. It is characteristic of I^2L that the active charge is found mainly in the emitter, whereas in ISL the active charge is found mainly in the n-p-n collector (= p-n-p base), because of saturation. The active charges can be represented by capacitances between base and emitter in I^2L and base and collector in ISL, respectively; Figure 3.

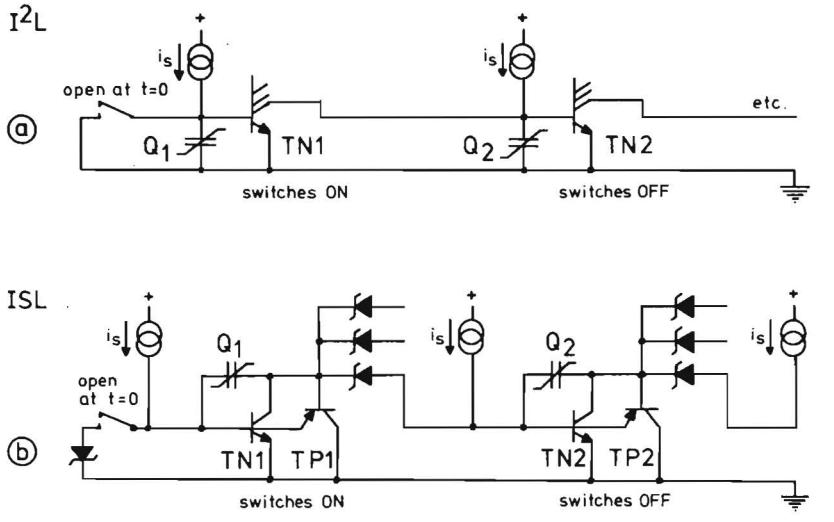

Fig. 3. Inverter chains made with I^2L (a) and ISL (b) gates. The active charge Q_1 and Q_2 will be found in the emitter in I^2L and in the collector (p-n-p base) in ISL. To calculate the minimum propagation delay time, the input switch is opened at $t = 0$.

The minimum propagation delay time of I^2L can be found with the circuit shown in Figure 3(a) [5]. TN1 switches ON rather slowly, because active charge Q_1 has to be built up in the emitter. TN2 is switched OFF, if all active charge Q_2 in its emitter is removed. The initial value of Q_2 depends both on F_{I^2L} (= fan-out) and $\beta_{\text{up eff}}$ and will be found in the n-emitter area and p-n-p base; regions I and II in Figure 2(a) [5,6]. Calculations [5] have shown that the average propagation delay time τ_{I^2L} is given by equation (*1*), where $\beta_{\text{up eff}}$ and $f_{T\ \text{n-p-n up}}$ are the effective current gain and the cut-off frequency of the inverse operated n-p-n.

The minimum propagation delay time of ISL (τ_{ISL}) is found in a similar way; Figure 3(b). The switch ON time of TN1 (normal operated!) is very short compared to the switch OFF time of TN2 which has an appreciable amount of active charge in the merged p-n-p base. This means that the switch OFF time of TN2 determines τ_{ISL}. For $t \geqslant 0$, TN1 can sink any amount of current up to $i_{cmax} = \beta_n i_s$. This maximum current will not be reached since the discharge path to remove Q_2 goes through the fan-out diodes and hence, the discharge current is limited by $F_{ISL} i_s$ (F_{ISL} = fan-out). In fact the discharge current will be somewhat higher due to the fact that TN2 operates in the reverse mode during its switch OFF time. The reverse current depends on $\gamma = I_{n0}/I_{p0}$, where I_{n0} and I_{p0} are the saturation currents of the n-p-n and p-n-p, respectively. Maximum storage of active charge is found for $\beta_{\text{n-p-n}} \to \infty$ and $\alpha_{\text{p-n-p}} \to 1$. τ_{ISL} is found as half the switch OFF time of TN2 and is given by equation (*2*) in which $f_{T\ \text{p-n-p}}$ is the overall

$$\tau_{I^2L} = \sqrt{\beta_{up\,eff}}\,/(2\pi f_{T\,npn\,up\,I^2L}) \qquad (1)$$

$$\tau_{ISL} = \left[\ln(1+\gamma/F_{ISL})\right]/(4\pi\gamma f_{T\,pnp\,ISL}) \qquad (2)$$

$$\tau_{I^2L}/\tau_{ISL} = 2F_{ISL}\sqrt{\beta_{up\,eff}}\,f_{T\,pnp\,ISL}/f_{T\,npn\,up\,I^2L}, \text{ for } \gamma<1 \qquad (3)$$

$$f_{T\,npn\,up\,I^2L} = 0.7\,D_n N_{epi}/\left[2\pi(F_{I^2L}+1)W_{epi}\int N_B dx\right] \qquad (4)$$

$$f_{T\,pnp\,ISL} = D_p(1+W_{epi}/W_p)/\left[2\pi W_{epi}(\tfrac{1}{2}W_p+\tfrac{3}{2}W_{epi})\right] \qquad (5)$$

TABLE 1. Equations.

effective cut-off frequency belonging to the composite p-n-p with active base charge in the regions I, II and III; Figure 2(b). τ_{ISL} reduces to $1/(4\pi f_{T\,p\text{-}n\text{-}p}F_{ISL})$ for $\gamma < 1$. The ISL/I^2L speed comparison delivers equation (*3*) for $\gamma < 1$. The cut-off frequency $f_{T\,n\text{-}p\text{-}n\,up}$ is given by equation (*4*) [5], where W_{epi} is the width of the epitaxial layer between base and substrate and $\int N_B dx$ the base dope integral. Where ISL, the injecting cross-sectional areas, indicated by I, II and III, are equal, then with $f_T = i/(2\pi Q_{active})$, equation (*5*) is found where W_p is the width of the base of the lateral p-n-p. Table 2 gives, for different values of W_{epi}, measured delay times of ISL and I^2L, as well as measured and calculated speed ratios. Measurements have been done for devices with 5 μm minimum details. Calculations are made using equations (*3,4,5*), and $\int N_B dx = 1$ to 3.10^{12}cm^{-2}, $N_{epi} = 10^{16}$ cm^{-3}, $\beta_{up\,eff} = 4$, $F_{I^2L} = 4$ and $F_{ISL} = 1$. Here it appears that ISL is at least a factor of 5 faster than I^2L. As ISL becomes faster for $F_{ISL} > 1$ this factor of 5 is a worst case value; in some particular cases, however, the ISL delay time can increase for fan-in > 1 [7].

Also in scaled-down devices, with oxide isolation, ISL will be faster than I^2L. It has been found that with 1 μm minimum details, ISL and I^2L will have minimum delay times of 0.8 ns and 2 ns, repsectively [8].

	measured			calculated
	τ_{min} ISL F=1	τ_{min} I^2L F=4	$\frac{\tau_{ISL}}{\tau_{I^2L}}$	$\frac{\tau_{ISL}}{\tau_{I^2L}}$
$W_{epi} = 8\mu m$	10ns	100ns	0.1	0.14
$W_{epi} = 5\mu m$	7ns	50ns	0.14	0.15
$W_{epi} = 2\mu m$	3ns	15ns	0.2	0.16

TABLE 2. Measured minimum propagation delay times of ISL and I^2L made with 5 μm details. Both measured and calculated speed ratios are included.

CONCLUSION

At small current levels ISL is faster than I^2L because of the smaller voltage swing. At high current levels ISL is faster because of its different switching behaviour and due to the fact that in most practical cases $f_{T\ \text{p-n-p ISL}} > f_{T\ \text{n-p-n up } I^2L}$.

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7

Propagation Delay Time of I^2L at Low Current Levels

Indexing terms: Bipolar integrated circuits, Delays, Integrated logic circuits

It is shown that the propagation delay time of i.i.l. at low current levels is given by $t_r/2$ if $t_f < t_r$, where t_f is the fall time and t_r the rise time at an i.i.l. input node. An expression for t_r and t_f can easily be found.

An analytical expression for the propagation delay time of i.i.l. at low current levels can easily be derived by considering a 3-stage ring oscillator as shown in Fig. 1*a*. The active charge is assumed to be small compared with the passive charge in the capacitances C_{be} and C_{bc}, so only low current levels are considered. It is further assumed that the voltage fall time at the base nodes is smaller than the voltage rise time. In that case the node voltages as a function of time will be as illustrated in Fig. 1*b*, which is confirmed by numerical computer simulations and measurements (Fig. 1*c*). From Fig. 1*b* it is evident that the average propagation delay time t_p is equal to $(t_{PLH} + t_{PHL})/2 = T/6 = t_r/2$, where in this particular case t_r is taken from 0% to 100% instead of 10% to 90%, which is more usual. This means that if indeed $t_f < t_r$ the average propagation delay is given by $t_r/2$. To calculate t_r the ring oscillator is first considered from $t = 0$ up to $t = t_f$. During this period transistor T2 is on, which means that node 2 is constantly high at $V = V_0$ and that both transistors T1 and T3 are off while nodes 1 and 3 are charging and discharging, respectively; the electrical diagram can be replaced by the diagram given in Fig. 2*a*. From Fig. 2*a* it follows that

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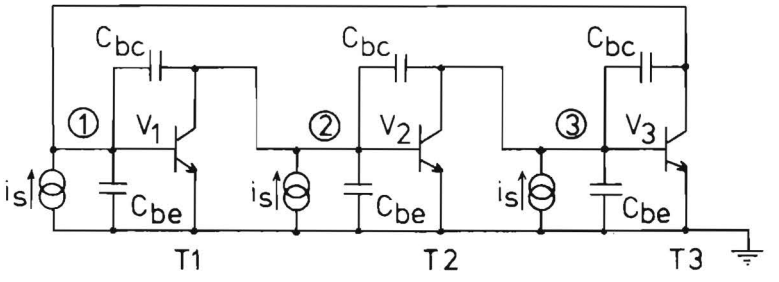
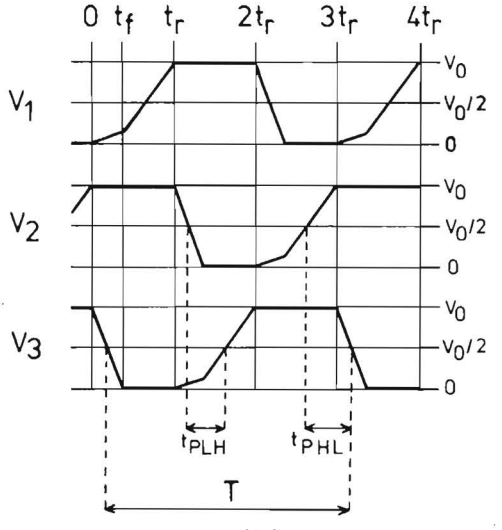
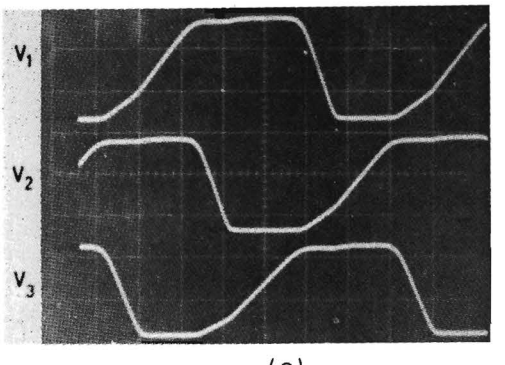


(a)



(b)



(c)

Fig. 1

a A 3-stage i.i.l. ring oscillator
b Idealised waveforms of nodes 1, 2 and 3
c Measured waveforms of nodes 1, 2 and 3
Vertical: 250 mV/div; Horizontal: 1 μs/div

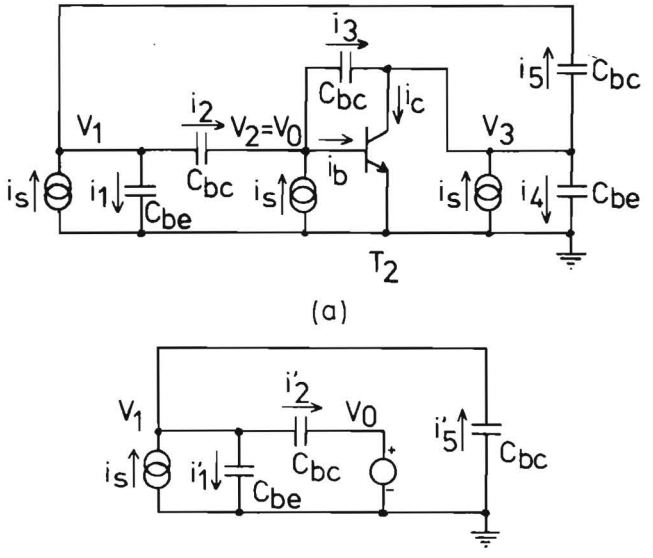


Fig. 2

a Equivalent diagram of the 3-stage i.i.l. ring oscillator for when transistor T2 is on but not saturated

b Equivalent diagram for when transistor T2 is saturated

$$i_1 = C_{be}\frac{dV_1}{dt} \qquad i_s = i_1 + i_2 - i_5$$

$$i_2 = C_{bc}\frac{dV_1}{dt} \qquad i_s = i_b + i_3 - i_2$$

$$i_3 = -C_{bc}\frac{dV_3}{dt} \qquad i_s = i_c - i_3 + i_4 + i_5$$

$$i_4 = C_{be}\frac{dV_3}{dt} \qquad i_c = \beta_{up\ eff}\, i_b = \beta i_b$$

$$i_5 = C_{bc}\left(\frac{dV_3}{dt} - \frac{dV_1}{dt}\right)$$

with $\beta = \beta_{up\ eff}$.

The solution of this set of equations leads to

$$\frac{dV_1}{dt} = \frac{t_s}{(\beta + 1)\,C_{bc} + C_{be}} \qquad (1)$$

and

$$\frac{dV_3}{dt} = -\frac{(\beta - 1)\, i_s}{(\beta + 1)\, C_{bc} + C_{be}} = -(\beta - 1)\frac{dV_1}{dt} \tag{2}$$

which means that $t_f < t_r$ if $\beta > 2$.

Consider the case where $\beta > 2$. From eqn. 2 it follows that

$$t_f = \frac{V_0\{(\beta + 1)\, C_{bc} + C_{be}\}}{(\beta - 1)\, i_s} \tag{3}$$

which is the time for which the voltage at node 3 is decreased to zero. The minimum value of t_f is $V_0 C_{bc}/i_s$ for $\beta \gg 2$ and $\beta C_{bc} \gg C_{be}$. At $t = t_f$ the voltage at node 1 is increased to $V_0/(\beta - 1)$.

In the interval $t_f < t < t_r$, transistor T2 is saturated, which means that during this period the circuit diagram shown in Fig. 2*b* is valid. Now

$$\frac{dV_1}{dt} = \frac{i_s}{C_{be} + 2C_{bc}} \tag{4}$$

and

$$t_r - t_f = \frac{(\beta - 2)\,(C_{be} + 2C_{bc})\, V_0}{(\beta - 1)\, i_s} \tag{5}$$

Addition of eqns. 3 and 5 gives

$$t_r = \frac{(3C_{bc} + C_{be})\, V_0}{i_s} \tag{6}$$

and consequently

$$t_p = \frac{(3C_{bc} + C_{be})\, V_0}{2i_s} \tag{7}$$

which is independent of β if $\beta > 2$. This result is also given in Reference 1 for when the fan-in is equal to 1.

From eqn. 7 it follows that t_p is determined only by V_0/i_s and the capacitances. This consideration can be used to calculate t_p in the general case. Fig. 3 shows a general case with fan-in $= F_i$ and fan-out $= F_o$. The time needed to charge the input node of T1 is given as

$$t_r = V_0\{F_0\, C_{bc} + C_{be} + 2nC_{bc} + (F_i - n)\, C_{bc}\}/i_s$$

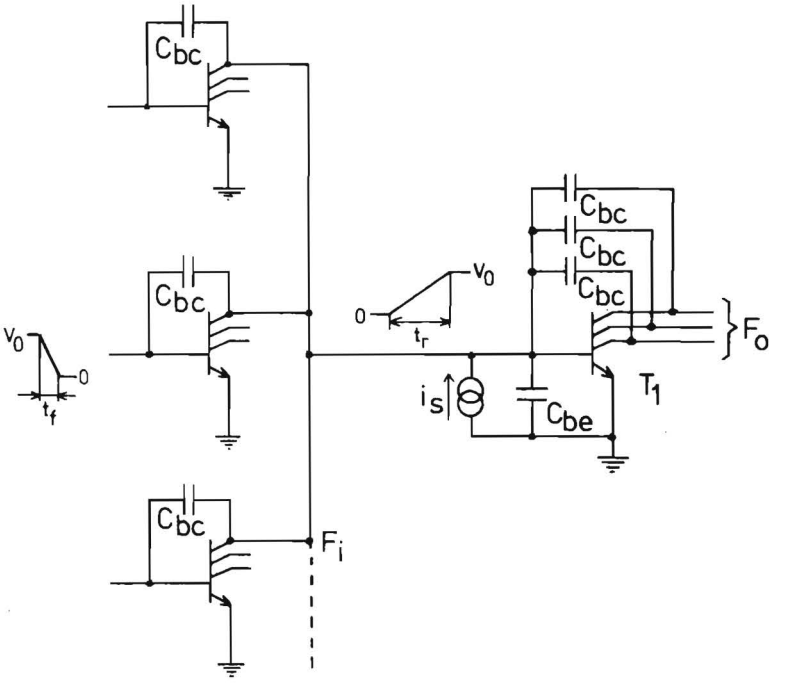


Fig. 3 *General case with fan-in = F_i and fan-out = F_o*

where $1 \leqslant n \leqslant F_i$. The number n indicates how many inputs of the fan-in transistors switch down at the same moment while the inputs of $(F_i - n)$ transistors are already low. The propagation delay time is again given by $t_r/2$.

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Reference

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8

Propagation Delay times of ISL and STL

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Abstract – **Propagation delay times of high-speed VLSI candidates ISL and STL are calculated analytically. It is shown by calculations and measurements that STL is marginally faster than ISL in oxide-isolated processes, at the cost of higher process complexity. Both logic forms suffer from speed degradation due to fan-in. Measures to obtain delay times that are independent of fan-in are discussed. Fan-out aspects are also considered. It is shown that ring oscillators exhibit a somewhat better speed than logic gates that start to switch from the DC state. This speed difference is expressed in an empirical formula.**

8.I. Introduction

Integrated Schottky Logic (ISL) [1] and Schottky Transistor Logic (STL) [2,3] are strongly upcoming high speed LSI and VLSI circuit techniques. Due to their small voltage swing (~ 200 mV) and their simple gate structure, they combine a relatively low speed--power product with a high packing density [4].

Although custom circuits have been made with ISL and STL, gate arrays [5-10] and composite cell logic [5,11] are the most favoured applications at the moment.

The first generations of ISL and STL were pn-isolated [1,2,3,12]. The second generations are oxide-isolated [13-18]; they offer a better speed, a lower speed-power product and a higher packing density than the first generations.

No complete analytical analysis of the propagation delay times of ISL and STL has yet been presented, nor up to now has the difference between these two logic forms been analyzed very well. The purpose of this paper is to provide a detailed analysis of ISL and STL, giving an investigation of the fan-in and fan-out aspects, and a comparison between the two logic forms.

In section II the external and internal DC voltage levels of ISL and STL are calculated. In section III the low current propagation delay times are calculated, and measures are discussed to reduce or eliminate the increase of propagation delay time when fan-in > 1.

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In section IV propagation delay times at medium and high current levels are calculated and it is shown that the same measures as discussed in section III can be used to eliminate fan-in dependent times. In section V the influence of series resistances and wiring capacitances is discussed. Section VI makes a comparison between ISL and STL, and various measurements by other authors are included. It is shown that STL will be a little faster than ISL when made in the same basic process and with the same minimum dimensions, at the cost of higher process complexity.

8.II. External and internal DC voltage levels

Fig. 1 shows both for ISL and STL two sections of an inverter string with fan-in and fan-out = 1 ($F_i = F_o = 1$). The current sources deliver a current $i = i_s$. It is assumed that the first stage is ON, and that the collector current i_{cOFF} of the previous stage is very small compared with i_s.

A. ISL

Neglecting series resistances, the inverse base-current of the saturated n-p-n transistor can mathematically easily be added to the forward base-current of the p-n-p transistor. This creates an effective forward collector-emitter current ratio α_p^* of the p-n-p transistor which simplifies the equations for the voltage levels.

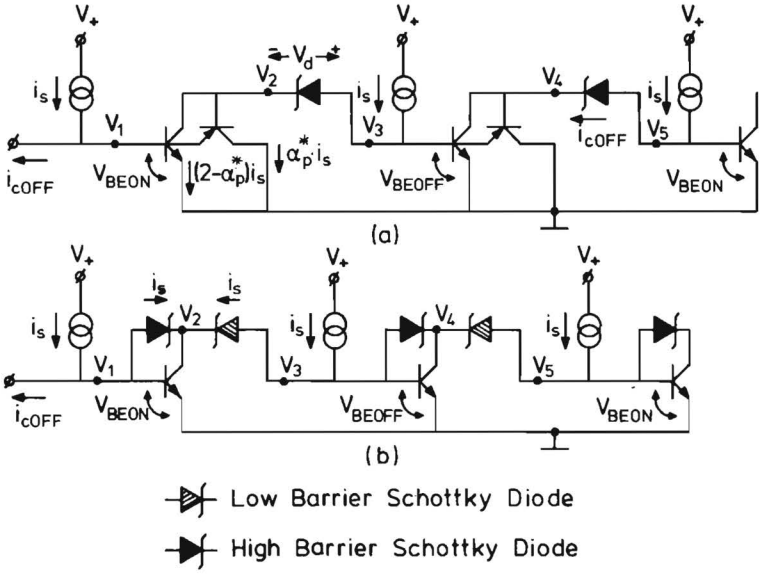

Fig. 1. Two sections of an inverter string for ISL (a) and STL (b). The first state is ON, the second stage is OFF.

When forward base current of the n-p-n transistor is neglected (which is allowed for practical circuits where $\beta_{fN} \geqslant 30$), the effective forward α_p^* of the p-n-p is given by:

$$\alpha_p^* = 1/(1 + \gamma/\beta_{rN} + 1/\beta_{fp}), \tag{1}$$

where $\gamma = I_{n0}/I_{p0}$ (being the saturation current ratio of the n-p-n transistor and p-n-p transistor), β_{rN} is the inverse current gain of the n-p-n and β_{fp} the forward current gain of the p-n-p; it is assumed that the p-n-p does not go into high injection.

When both for the p-n-p and Schottky diode the ideality factor is 1, the logic swing is given by:

$$\begin{aligned}
\Delta V_{ISL} &= V_{BEON} - V_{BEOFF} \\
&= V_1 - V_3 \\
&= V_{BE\,p\text{-}n\text{-}p} - V_d \\
&= \frac{kT}{q} \ln \frac{\alpha_p^* i_s}{I_{p0}} - \frac{kT}{q} \ln \frac{i_s}{I_{d0}} \\
&= \frac{kT}{q} \ln \frac{\alpha_p^* I_{d0}}{I_{p0}},
\end{aligned} \tag{2}$$

where I_{d0} is the saturation current of the Schottky diode.

Further with the schematic of Fig. 1 it can be calculated that the absolute values of V_1, V_2, V_3 and V_4 are

$$\left.\begin{aligned}
V_1 &= \frac{kT}{q} \ln \frac{(2 - \alpha_p^* + \gamma\alpha_p^*) i_s}{I_{n0}}, \\
V_2 &= \frac{kT}{q} \ln \frac{2 - \alpha_p^* + \gamma\alpha_p^*}{\gamma\alpha_p^*}, \\
V_3 &= \frac{kT}{q} \ln \frac{(2 - \alpha_p^* + \gamma\alpha_p^*) i_s}{\gamma\alpha_p^* I_{d0}}, \\
V_4 &= \frac{kT}{q} \ln \gamma\alpha_p^* (I_{d0}/I_{n0})^2,
\end{aligned}\right\} \tag{3}$$

assuming that $V_5 = V_1$, and neglecting the forward base currents of the n-p-n transistors.

The voltage swing ΔV_i of the internal node equals

$$\Delta V_{iISL} = V_4 - V_2 = 2\Delta V_{ISL} - \frac{kT}{q} \ln (2 - \alpha_p^* + \alpha_p^* \gamma). \tag{4}$$

For practical values of α_p^* close to 1, and γ being $\leqslant 1$, the second term of (4) is small compared with $2\Delta V_{ISL}$, which means that the voltage swing of the internal node has about double the value of the logic swing ΔV_{ISL}.

B. STL

Similar calculations can be done for STL. In that case the input current i_s of the first stage has to flow through the non-saturated p-n-p transistor, which now has to draw a collector current of $2i_s$. When the ideality factors of both Schottky diodes are 1, the logic swing is given by:

$$\Delta V_{STL} = V_1 - V_3 = \frac{kT}{q} \ln \frac{I_{d01}}{I_{d02}} , \tag{5}$$

where I_{d01} and I_{d02} are the saturation currents of the output diode and clamp diode respectively.

Further the swing of the internal node can be calculated to be

$$\Delta V_{iSTL} = \frac{kT}{q} \ln [(I_{d01}/I_{d02})^2 + \frac{1}{2}] . \tag{6}$$

In this case the second term in the logarithm is small compared with $(I_{d01}/I_{d02})^2$ which means that there, too, the voltage swing of the internal node has about double the value of the logic swing.

C. Fan-in and/or fan-out larger than 1

Both for ISL and STL it has been assumed as a first-order approximation that i_{cOFF} is small compared with i_s. When $F_i = F_o = 1$, i_{cOFF} in the ISL case equals $I_{n0} \exp (qV_3/(kT)) = (2 - \alpha_p^* + \gamma\alpha_p^*) I_{p0} i_s/(\alpha_p^* I_{d0})$; in the STL case it can be calculated that $i_{cOFF} = 2I_{d02} i_s/I_{d01}$; when $\alpha_p^* I_{d0}/I_{p0}$ and I_{d01}/I_{d02} are larger than 100 (then the voltage swings are $>$ 120 mV), these currents are indeed small compared with i_s.

For larger values of F_i and F_o multiple values of i_{cOFF} occur, which means that larger voltage swings are needed to allow these total OFF-currents to be treated as neglible. As shown in [19,20] voltage swings of at least 150 mV are needed to obtain stable ISL and STL circuits when $F_i = F_o = 4$.

Although ΔV and ΔV_i depend on F_i and F_o, this dependence is only a weak one, which means that the values obtained for $F_i = F_o = 1$ in the equations (2,4,5,6) are good enough as first-order approximations.

8.III. Low current level propagation delay times

A. General expression for the propagation delay time for $F_i = F_o = 1$

At low current levels, the average propagation delay time t_{pd} is mainly determined

by the junction capacitances. At practical values of β_{fN} ($\geqslant 30$) the input rise time t_{rise} is longer than the input fall time, and therefore the average propagation delay time has to be at least $t_{rise}/2$. This is confirmed by circuit simulations which show that t_{pd} is indeed somewhat longer than $t_{rise}/2$, due to the existence of the internal node (only in I^2L, which does not have the internal node, is t_{pd} exactly equal to $t_{rise}/2$ [20]).

Fig. 2 shows two stages of ISL and STL with all junction capacitances included. In STL the capacitance C^*_{bc} is the combined capacitance of the base-collector junction of the n-p-n and the clamp Schottky diode.

At low current levels there is no fundamental difference between the switching mechanism of ISL and STL, which means that the mathematical expression for t_{pd} is valid for ISL and STL.

Suppose now that two stages of Fig. 2 are preceded and followed by long chains of identical stages, and that a pulse with a pulsewidth T is propagating through the chain. Fig. 3 shows the node voltages (See Fig. 2) as a function of time. The time origin ($t = 0$) is placed at the point where V_1 starts to rise. The node voltages are obtained with a circuit analysis program using the following transistor and capacitance parameters:
$\gamma = 0.15$, $\beta_{fN} = 50$, $\beta_{rN} = 3$, $\beta_{fP} = 30$, resulting in $\alpha^*_p = 0.92$, $C_{be} = 0.1$ pF, $C_{bc} = 0.1$ pF, $C_{cs} = 0.4$ pF, $C_d = 0$. As C_d behaves like a speed-up capacitance (it couples the output node with the internal node, which latter makes a larger swing), the simulation of Fig. 3 shows a worst-case behaviour by disregarding C_d; in practical circuits C_d is small compared to the other capacitances anyway, which means that the result of Fig. 3 is quite close to reality.

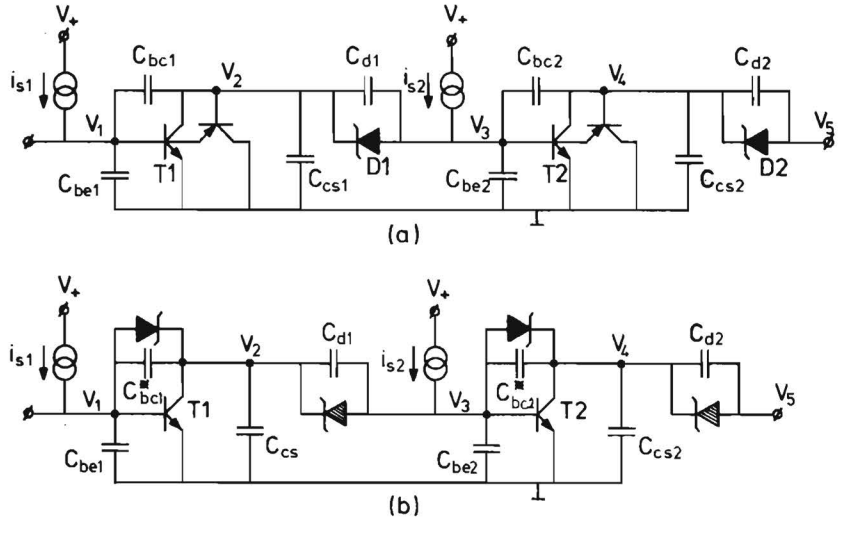

Fig. 2. Two stages of ISL (a) and STL (b); all junction capacitances are included. It is assumed that very long chains precede and follow these two sections.

To obtain the average propagation delay time t_{pd}, we have to find the repetitive time between similar waveforms; for instance the time difference between $t = 0$, where V_1 starts to rise, and $t = t_{charge1}$, where V_5 starts to rise (note that $t_{charge1}$ is longer than t_{rise1}, the latter being the rise time from 0% to 100% of V_1). It will be clear that t_{pd} is related to t_{charge} by

$$t_{pd} = t_{charge}/2. \tag{7}$$

At t = T the opposite pulse-edge propagates through the chain. As shown in Fig. 3 node V_4 did not reach its ultimate value V_{iH} due to the large differential resistance of the Schottky diode $D2$ ($R_{diff.max.} = kT/(qi_{cOFF})$), through which this internal node has to be charged. The consequence is that $t_{charge3}$ (to charge node 3) is shorter than $t_{charge1}$ (to charge node 1); the dotted lines indicate what V_4 and V_5 would have been if T had been infinitely long. This means that t_{pd} is longer for gates which start to switch from their completely relaxed DC states than for gates which reswitch within a certain time interval. As the switching event at $t = T$ (see Fig. 3) is the more general case, this event will be studied in more detail.

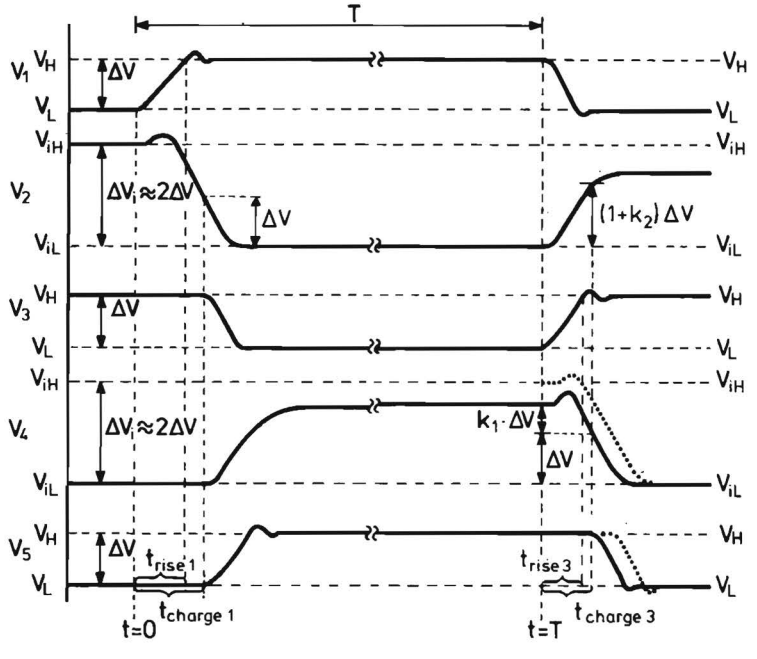

Fig. 3. Node voltages of the nodes in Fig. 2, when a pulse with a width T is propagating through the chain.

Taking $\Delta V_i = 2\Delta V$ for the *DC* case (see Section II) the *AC* swing at $t = T$ is $(1 + k_1)\Delta V$, where $0 \leqslant k_1 \leqslant 1$ depending on T. The charge time is the time which it takes for current source i_{s2} to discharge V_4 from $V_{iL} + (1 + k_1)\Delta V$ to $V_{iL} + \Delta V$ (during this time V_3 is charged in the time t_{rise3} from V_L to V_H). As soon as V_4 equals $V_{iL} + \Delta V$ the output diode of T2 will be sufficiently forward biased to draw the current i_{s3} and consequently T3 will switch off and V_7 will start to rise. Fig. 4 shows all elements connected to node 3 and the considered voltage swings. During $t_{charge3}$ node 2 is not charged to $V_{iL} + 2\Delta V$, but to $V_{iL} + (1 + k_2)\Delta V$, where $0 \leqslant k_2 \leqslant 1$. The capacitance $C_{bc1}//C_{cs1}$ together with $R_{diff.D1}$ form an *RC* time load to node 2, where $R_{diff.D1}$ increases with increasing voltage at node 2. The value of k_2 is very difficult to calculate because it depends on $t_{charge3}$. Furthermore, node 3 has to deliver base current to T2 between t_{rise3} and $t_{charge3}$ (the time interval in which T2 is ON). However, this base current can be neglected in practical circuits, where $\beta_{fN} \geqslant 30$.

The voltage swing across the capacitances between $t = T$ and $t = T + t_{charge3}$ is $(2 + k_2)\Delta V$ for C_{bc1}, $(1 + k_2)\Delta V$ for C_{cs1}, ΔV for C_{be2} and $(1 + k_1)\Delta V$ for C_{bc2} (see Fig. 4). So the time to charge node 3 equals:

$$t_{charge} = \frac{(3 + k_1 + k_2)C_{bc} + (1 + k_2)C_{cs} + C_{be}}{i_s}\ \Delta V,$$

and consequently

$$t_{pd} = \frac{(3 + k_1 + k_2)C_{bc} + (1 + k_2)C_{cs} + C_{be}}{2i_s}\ \Delta V. \tag{8}$$

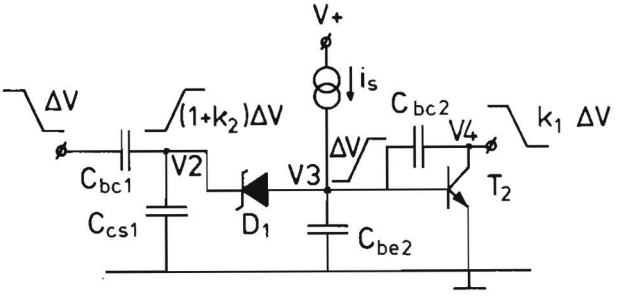

Fig. 4. A simplified diagram of Fig. 2 in which all the capacitances to be charged by i_{s2} are indicated.

B. Propagation delay time starting from the DC situation ($F_i = F_o = 1$)

As shown in III.*A*, k_1 is 1 when gates switch from their *DC* state. Further, from various circuit simulations a practical value for k_2 is found to be 0.3. This means that during the charge time the internal node makes a voltage swing of 1.3 ΔV. Substitution of these values in (8) yields

$$t_{pd} = \frac{4.3C_{bc} + 1.3C_{cs} + C_{be}}{2i_s} \Delta V. \tag{9}$$

C. Propagation delay time in a ring oscillator ($F_i = F_o = 1$)

Fig. 3 shows that the internal node V_4 charges very slowly after its voltage is increased to $V_{iL} + 1.3\Delta V$; this is due to the steeply increasing differential resistance of the Schottky diode by which this node is charged. In a ring oscillator with a limited number of stages the internal node will not reach V_{iH} and consequently k_1 is reduced. Even in a ring oscillator with as many as 21 stages, a significant reduction of k_1 is observed. Values around 0.7 can be found, so the average propagation delay of a 21-stage ring oscillator is about

$$t_{pd} = \frac{4.0C_{bc} + 1.3C_{cs} + C_{be}}{2i_s} \Delta V. \tag{10}$$

For shorter ring oscillators k_1 will be even smaller, of course.

D. Fan-out $\geqslant 1$

Fig. 5 shows ISL with fan-out = F_o. When gate *A* is ON, the n-p-n of gate *A* has to sink a larger current than in the case where $F_o = 1$. Due to this larger current, V_{BEON} of gate *A* has to be somewhat larger. It can be calculated that the increase of V_{Hin} is

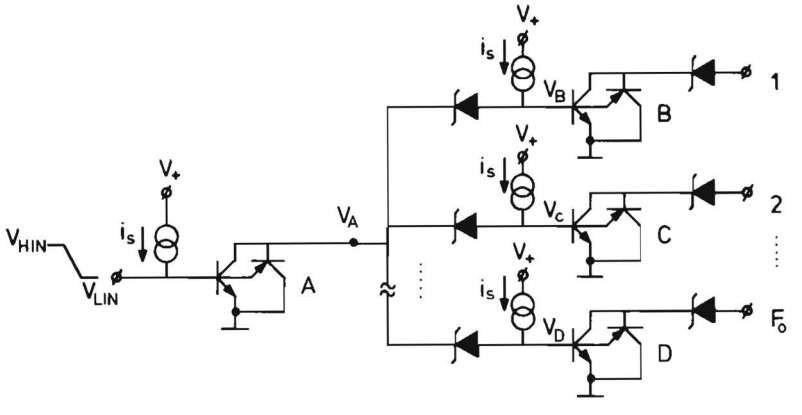

Fig. 5. ISL situation where gate *A* has a fan-out of F_o.

$$\delta V_{\mathrm{Hin}} = \frac{kT}{q} \ln \left(\frac{F_o + 1 - \alpha_p^* + \alpha_p^* \gamma}{2 - \alpha_p^* + \alpha_p^* \gamma} \right). \tag{11}$$

As the V_{BE} of the p-n-p of gate A remains constant, V_A is increased by the same amount δV_{Hin} and so are the low level inputs of gates B, C and D (V_{LB}, V_{LC} and V_{LD}). This means that the logic swing of the nodes B, C and D is somewhat smaller than ΔV calculated for $F_i = 1$ (see Section II). However, the decrease of the propagation delay time due to this effect is small compared with the decrease of the propagation delay time caused by the extra current $(F_o - 1)i_s$ which is available to charge node A; this also holds for STL. This means that the first-order propagation delay time for both ISL and STL equals

$$t_{pd} = \left[(1 + k_1 + \frac{2 + k_2}{F_o}) C_{bc} + (\frac{1 + k_2}{F_o}) C_{cs} + C_{be} \right] \frac{\Delta V}{2 i_s}, \tag{12}$$

where $F_o \geqslant 1$.

This equation shows that for $F_o > 1$ there is a considerable decrease in the average propagation delay time, because in practical circuits C_{bc} and C_{cs} are larger than C_{be}.

E. Fan-in $\geqslant 1$

Fig. 6 shows an ISL configuration with $F_i > 1$. Suppose that gate A is OFF, due to the fact that one or more of the preceding gates are ON. In the general case n gates of the preceding gates are ON and (F_i-n) gates are OFF.

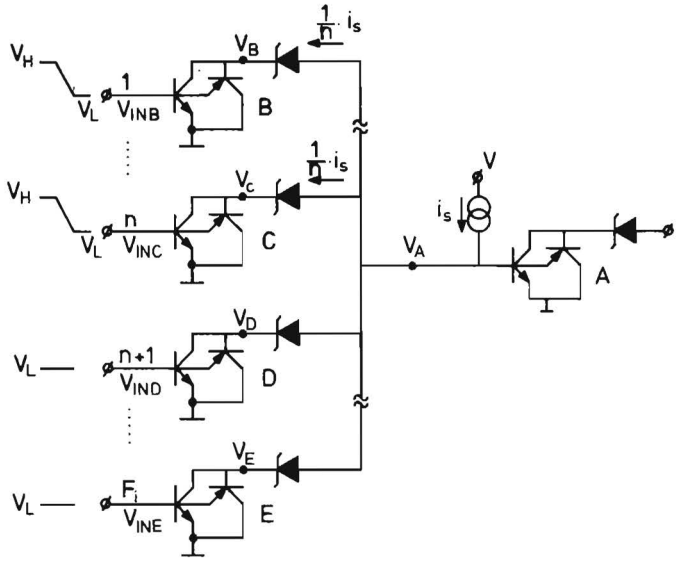

Fig. 6. ISL situation where gate A has a fan-in of F_i. Of the F_i input gates, n gates are switching OFF simultaneously.

Due to the fact that n gates are ON, when $n > 1$, the low level voltage of node A (V_{AL}) is somewhat lower than in the case when $F_i = 1$ (where n is always 1). This means that the logic swing at node A is somewhat larger than ΔV calculated in Section II. However, the increase of the propagation delay time due to this effect is small compared with the increase of propagation delay time caused by the extra capacitive loading of node A by the n preceding gates,

Fig. 7 shows the node voltage $V_B = V_C$, $V_D = V_E$ and V_A during charging of node A. As gates D and E are OFF, the node voltages V_D and V_E are about $V_{iH} - \Delta V = V_{iL} + \Delta V$, which means that nodes D and E are already charged for a large part of the main increase from V_{iL} to $V_{iL} + (1 + k_2)\Delta V$. So at $t = 0$, V_B and V_C will start to rise up to $V_{iL} + \Delta V$ (see t_1 in Fig. 7); from this moment on V_B, V_C, V_D and V_E will be raised simultaneously up to $V_{iL} + (1 + k_2)\Delta V$. All the capacitances are charged by only one current source at the input of gate A.

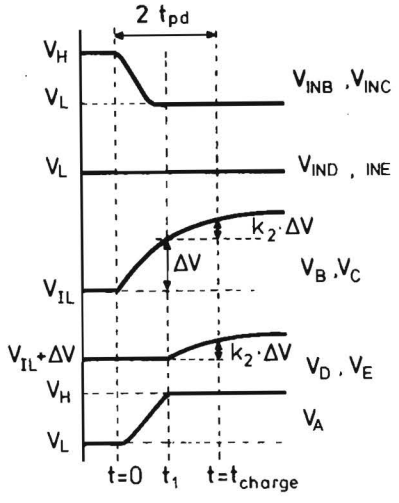

Fig. 7. Node voltages of the nodes in Fig. 6. Gates B and C have an internal voltage swing which is ΔV larger than the internal voltage swing of D and E.

It can easily be calculated that in this case the average propagation delay time both for ISL and STL is

$$t_{pd} = \left[(1 + 2n + F_i k_2 + k_1)C_{bc} + (n + F_i k_2)C_{cs} + C_{be}\right] \frac{\Delta V}{2i_s}, \qquad (13)$$

where $F_i \geqslant 1$ and $1 \leqslant n \leqslant F_i$.

F. Measures to obtain fan-in independent propagation delay times in ISL and STL

Sections III.*D* and III.*E* dealt with circuit configurations where $F_i \geqslant 1$ or $F_o \geqslant 1$. In real logic circuits combinations will always occur, which means that speed degradation due to fan-in may be compensated or partly compensated by speed improvement due to fan-out. Nevertheless always critical paths may appear where speed degradation due to fan-in is dominant, so for worst-case analysis expression (13) must be taken into account with all inputs switching simultaneously ($n = F_i$).

At the cost of extra power dissipation the fan-in dependency of the propagation delay time can be reduced or eliminated by electronic methods.

There are three possibilities: a) fan-in dependent increase of the input current; b) introduction of a pull-up resistor to the internal node; c) use of dummy gates.

a) Fan-in dependent increase of input current.

When the current source to node A in Fig. 6 is increased to a level of, for instance, $F_i i_s$, the worst-case average propagation delay times decreases to

$$t_{pd} = \left[(2 + k_2 + \frac{1 + k_1}{F_i})C_{bc} + (1 + k_2)C_{cs} + \frac{C_{be}}{F_i}\right] \frac{\Delta V}{2i_s} \qquad (14)$$

with all inputs switching simultaneously. In ISL the input current has to flow through the p-n-p in the *DC* case. This might be problematical for high values of n, when series resistances cannot be neglected.

b) Pull-up resistor to the internal node.

Fig. 8 shows the case where each gate has a pull-up resistor connected to the internal node, providing a current i_i. When $i_i/(C_{bc} + C_{cs}) \geqslant i_s/(C_{be} + C_{bc})$ then $\frac{dV_A}{dt} \geqslant \frac{dV_B}{dt}$, which means that the charge time on node A becomes fan-in independent. In that case the average propagation delay time becomes

$$t_{pd} = (C_{be}\Delta V + C_{bc}V^+)/2i_s \qquad (15)$$

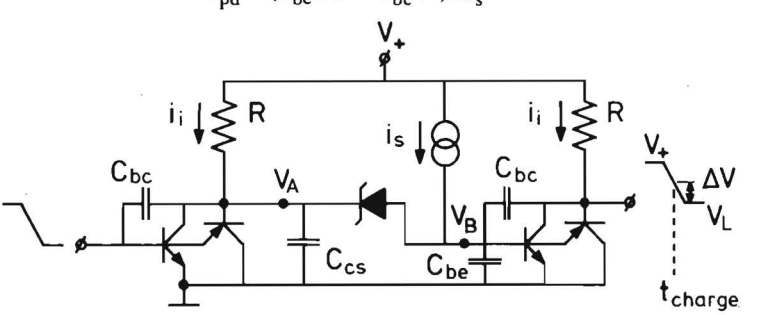

Fig. 8. To decrease the speed degradation by fan-in, a pull-up resistance R is used to charge the internal node.

where V^+ is the power supply voltage.

To reduce the effective power supply voltage for the pull-up resistor a Schottky diode can be placed in series [14].

When $i_i/(C_{bc} + C_{cs}) < i_s/(C_{be} + C_{bc})$ then the fan-in dependency is not eliminated but reduced. In that case the t_{pd} result will be between the values obtained by (15) and (13).

c) Use of dummy gates.

In gate arrays [23], dummy gates can be connected to gates which are connected with their other outputs to gates that have a relatively large-fan-in (see Fig. 9) and which are in a time-critical path. When this is done the current source to node A does not have to charge all internal nodes of the F_i gates when they all are connected to a dummy gate. Here the speed improvement of a fan-out is used to compensate a speed degradation of fan-in.

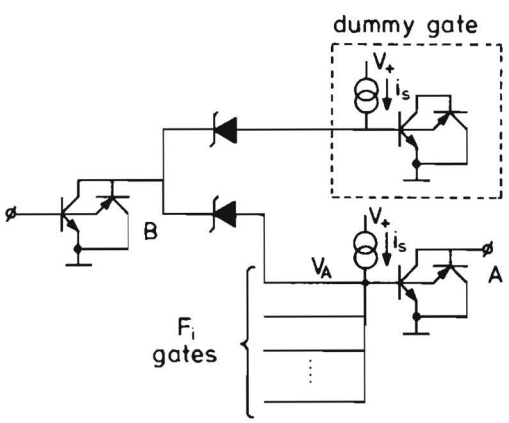

Fig. 9. To decrease the speed degradation by fan-in, a dummy gate provides an extra charge current for gate *B*.

8.IV. Propagation delay times at medium and high current levels

A. ISL at high current levels with $F_i = F_o = 1$

At high current levels the active minority carrier storage dominates the charges in the depletion capacitances. As the minority carrier storage is proportional to the current, the intrinsic propagation delay times are independent of the current level, as long as no series resistances are taken into account.

Fig. 10(a) shows a chain with ISL inverters. For $t \leqslant 0$ switch S is closed, which means that both TN1 and TP1 are OFF, and TN2 and TP2 are ON. When $t > 0$ the switch

is opened causing TN1 and TP1 to charge and consequently TN2 and TP2 to discharge. For practical devices the forward transit time of the n-p-n is much shorter than the forward transit time of the vertical p-n-p (in the oxide isolated case [13]) or composite p-n-p (in the junction isolated case [12]). This means that for the first-order approach the forward transit time of the n-p-n may be neglected. When further all series resistances are disregarded the reverse excess charge q_{rN} of the n-p-n can easily be mathematically combined with the forward excess charge q_{fp} of the vertical or composite p-n-p, forming an effective forward excess charge associated with the collector current of the p-n-p:

$$q_p^* = q_{fP} + q_{rN} = i_{cP}(\tau_{fP} + \gamma\tau_{rN}) = i_{cP}\tau_p^* \ , \tag{16}$$

where τ_p^* is the effective forward transit time of the p-n-p. This excess charge can be seen as a non-linear capacitance between the emitter and base node of the p-n-p [22] (see Fig. 10(a)).

As the n-p-n transistor is very fast compared with the p-n-p transistor, TN1 can sink any amount of current up to $\beta_{fN} i_s$ when $t > 0$. This means that the forward excess charge of TN2 is also removed very fast, causing V_3 to switch down immediately to V_{BEOFF}. However, the base-emitter junction of TP2 remains forward biased as long as excess charge is present. This means that shortly after $t = 0$ node 4 and node 5 make the same negative step as node 3, and that TP2 in the first instance keeps sinking $i_2 (= i_s)$; see Fig. 10(b). The voltage at node 4 will become negative. As the voltage between node 3 and 4 does not change very much for a long period after $t = 0$, the reverse collector current of TN2 keeps flowing, which implies that the net current through TN2 changes sign and changes amplitude!

When $t > 0$, the collector current of TN2 becomes $i_{cTN2} = -\gamma i_{cTP2}$, and the current through D2 remains $i_3 = i_s$; so the total current to discharge q_{p2}^* equals

$$\frac{dq_{p2}^*}{dt} = -i_s - \gamma \frac{q_{p2}^*}{\tau_p^*} \ , \tag{17}$$

where $q_{p2}^* = \alpha_p^* i_s \tau_p^*$ at $t = 0$.
Solution of (17) yields

$$q_{p2}^* = \left[(1 + \alpha_p^*\gamma)e^{-\gamma t/\tau_p^*} - 1\right] \frac{\tau_p^* i_s}{\gamma} \ , \tag{18}$$

which is zero for $t_1 = (\tau_p^*/\gamma)\ln(1 + \alpha_p^*\gamma)$. (19)

At $t = t_1$, TP2 is switched OFF and consequently TN3 is switched ON. The average propagation delay t_{pd} is therefore $t_1/2$, so

$$t_{pd} = (\tau_p^*/2\gamma)\ln(1 + \alpha_p^*\gamma) \ , \tag{20}$$

which reduces to

$$t_{pd} = \alpha_p^*\tau_p^*/2 \tag{21}$$

when $\gamma \ll 1$ (because always $\alpha_p^* \leqslant 1$).

Fig. 10(b) shows the collector current through TP2 for the case where $\gamma \ll 1$. In that case the reverse collector current of TN2 is neglected, which means that i_{cTP2} decreases linearly ($i_{cTP2} = (\alpha_p^* - t/\tau_p^*)i_s$). The current through D1 is also indicated.

When $t > 0$ the i_{D1} immediately switches from zero (at $t = 0$) to i_s being i_3 flowing through q_{p2}^*. As q_{p2}^* is now discharged linearly in time (see eq. (17) with $\gamma \ll 1$), the collector current of TP2 decreases also linearly (from i_s to zero). This means that TP2 cannot fully sink i_2 anymore, and consequently the (increasing) rest of this current flows through D1. Therefore i_{D1} increases from i_s to $2i_s$ between $t = 0$ and $t = t_1$. At $t = t_1$, q_p^* is zero, causing i_3 to flow into TN3 and the current through D1 changes from $2i_s$ to i_s (see Fig. 10 and also Fig. 7 in [12]).

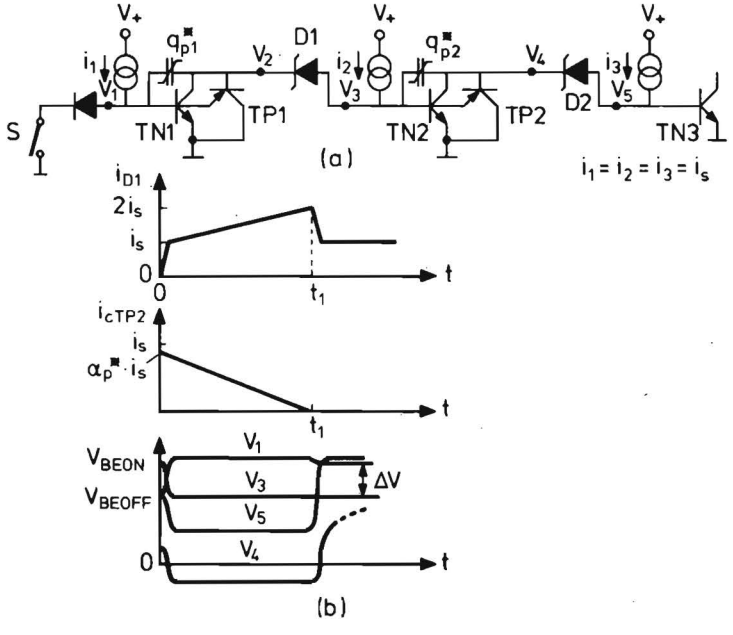

Fig. 10. (a) An ISL inverter chain is shown. Switch S opens at $t > 0$. Excess charge storage is represented by a non-linear capacitance. (b) For $\gamma \ll 1$ the waveforms of i_{D1}, i_{cTP2}, V_1, V_3, V_4 and V_5 are shown.

Fig. 11 shows i_{cP2} and i_{D1} for $\alpha_p^* = 1$ and $\gamma = 0.1$, 1 and 10 respectively. For $\gamma = 10$ a peak current of 11 i_s flows through D_1 immeadiately after $t = 0$ and t_1 is reduced to 0.24 τ_p^*. For practical devices γ is approximately 0.1, which means that t_1 is about 10% below τ_p^*, so a first-order approximation of t_{pd} is indeed $t_{pd} = \alpha_p^* \tau_p^*/2$.

In cases where the forward transit time is not neglected, an analytical expression for t_{pd} is not very easy to derive. However, in practical devices $\tau_{fN} \ll \tau_{fP}$, which means that such an analytical expression would not be very useful for practical cases.

In ring oscillators q_p^* may not reach the eventual value $\alpha_p^* i_s \tau_p^*$. When a gate switches ON, the effective forward excess charge of the p-n-p is built up exponentially as given by

$$q_p^* = (1 - e^{-t/\tau_p^*}) \alpha_p^* i_s \tau_p^*, \tag{22}$$

which means that q_{p2}^* is charged to 95% for $t = 3\ \tau_p^*$. This means that a seven-stage ring oscillator provides a t_{pd} which is up to 5% too optimistic.

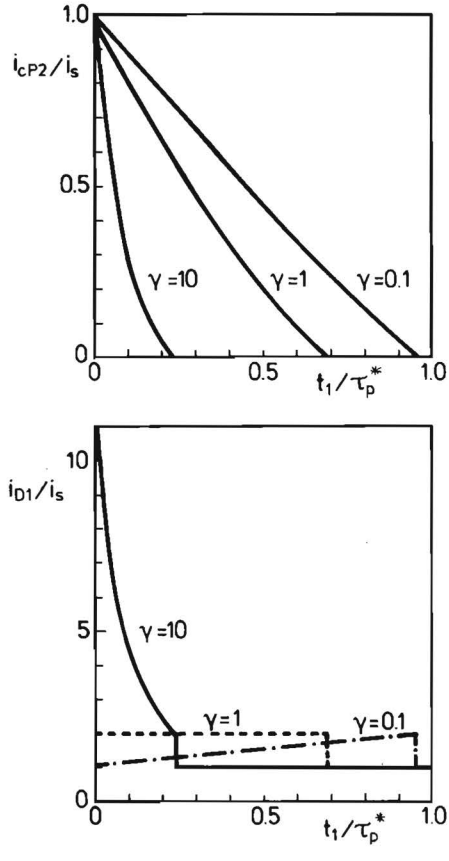

Fig. 11. The current i_{cP2} and i_{D1} of Fig. 10(a) as a function of γ when $\alpha_p^* = 1$ (worst-case value of α_p^*).

B. ISL at medium current levels when $F_i = F_o = 1$

As the effective forward excess charge of the p-n-p can be seen as a non-linear capacitance between the base and collector node of the n-p-n (being the emitter and base node of the p-n-p), the average propagation delay time can also be found as half the charge time of the input node (as explained in Section III) with the non-linear n-p-n base collector capacitance charged to $Q_1 = q_p^* = i_s \alpha_p^* \tau_p^*$ (see Fig. 12).

In this way the high current level t_{pd} expression (21) and low current level t_{pd} expression (8) are easily combined to give

$$t_{pd} = \left[(3 + k_1 + k_2)C_{bc} + (1 + k_2)C_{cs} + C_{be}\right]\frac{\Delta V_{ISL}}{2i_s} + \frac{\alpha_p^* \tau_p^*}{2} . \qquad (23)$$

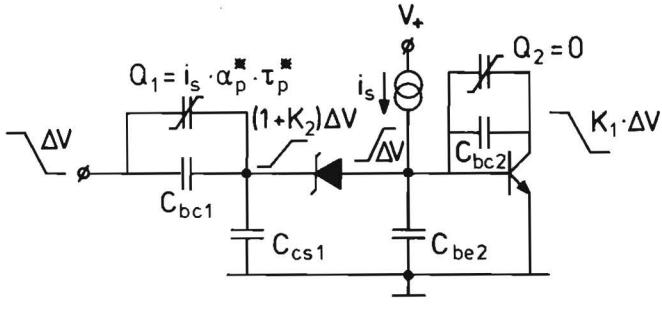

Fig. 12. As Fig. 4, with the p-n-p-transistor minority carrier storage indicated as a non-linear capacitance.

C. ISL at medium and high current levels when $F_i \geqslant 1$ and $F_o \geqslant 1$

At medium and high current levels, too, ISL will be slower for $F_i > 1$ and faster for $F_o > 1$. Mathematical expressions similar to these derived in section III.*D* and III.*E* can be derived when starting from (23). The electronic methods described in III.*F* to obtain fan-in independent propagation delay times also work out for high current levels. When the first method is used, where the input current is increased, the non-linear capacitance may be charged to $Q_1 = n\, i_s \alpha_p^* \tau_p^*$, causing an increased switch-off time of the p-n-p.

D. STL

In STL the relatively slow p-n-p does not exist; only the short forward transit time of the n-p-n plays a role. In practical devices the stored excess charge in the base of the n-p-n is very small compared with the charge in the junction capacitances, which means that for high current levels, too, expression (8) is valid, as long as no series resistances are taken into account.

8.V. Series resistances and wiring capacitances

A. Series resistances in ISL

Fig. 13 shows all relevant series resistances in ISL. At high current levels the series resistances can cause a considerable increase in the propagation delay time [4,12], and a decrease in voltage swing and noise margins [19,20].

It is mainly the Schottky series resistances R_d that will decrease the voltage swing. Although this would decrease t_{pd}, RC time effects and peak-current limiting effects have in general a stronger influence in practical circuits, which means that t_{pd} increases [12,24].

At high current levels the series resistances cause a different current distribution between the base current of the n-p-n and emitter current of the p-n-p, which can increase τ_p^*, and furthermore the p-n-p may go into saturation due to a too large voltage drop over its collector series resistance R_{cP} [12].

All these effects make it very difficult to derive a mathematical expression for t_{pd}, which includes all series resistances. In fact only a circuit simulation program can provide the information [12,24].

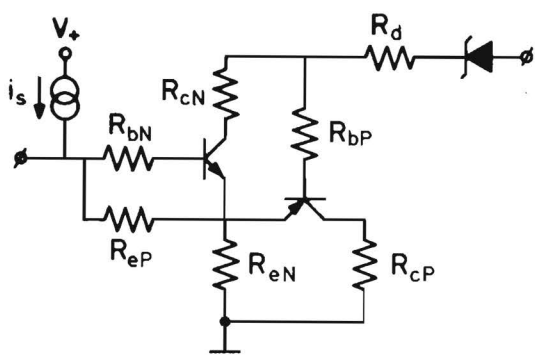

Fig. 13. An ISL stage with all relevant series resistances included.

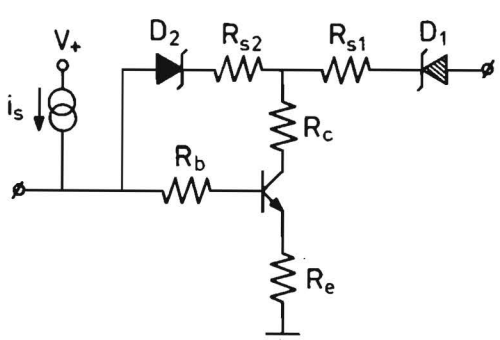

Fig. 14. An STL stage with all relevant series resistances included.

B. Series resistances in STL

Fig. 14 shows all relevant series resistances in STL. The logic swing equals $\Delta V'_{STL} = \Delta V_{STL} + (R_{s2} - R_{s1})i_s$. In practical cases R_{s1} will be larger than R_{s2}, which means that $\Delta V'_{STL}$ will decrease at high current levels. But here too, t_{pd} will increase due to the RC time effects and peak current limiting.

Further the series resistance of the clamp diode R_{s2} and the n-p-n collector resistance R_c can cause the n-p-n transistor to go into saturation at high current levels.

In STL, too, mathematical formulas including all series resistance effects are very difficult to derive, and computer simulations have to be used to obtain the information.

C. Wiring capacitances in ISL and STL

Wiring capacitances always increase the propagation delay time in ISL and STL.

These capacitances are parallel to C_{be}, so the mathematical expressions for t_{pd} can be used by replacing C_{be} by $C'_{be} = C_{be} + C_w$, where C_w is the particular wiring capacitance.

Especially when the fan-in is larger than 1, the influence of wiring capacitances is not negligible.

8.VI. ISL/STL comparison and measurements

A. Theoretical comparison

As shown in Section III, the propagation delay times of ISL and STL at low current levels would be identical for equal values of the junction capacitances C_{bc}, C_{cs}, C_{be} and the voltage swing ΔV. When ISL and STL are laid out in the same technological process, using the same process and same minimum design rules, small differences in the average values of C_{bc} and C_{cs} over their voltage swings may occur due to the fact that the juntion capacitances are essentially non-linear and the bias voltages are slightly different. In ISL C_{bcN} and C_{csN} intend to be a little larger than in STL because the base--collector junction is about 100 - 200 mV more forward-biased, and the collector-substrate junction is about 100 - 200 mV less reverse-biased. In STL, however, the junction capacitance of the clamp diode has to be added to the base-collector capacitance of the n-p-n, and further C_{csN} will be a little larger due to the larger collector island which is needed to include the clamp diode (see Fig. 15).

As shown in Section II, the voltage swings are determined mainly by the saturation currents of the clamp devices and output Schottky diodes (I_{p0} and I_{d0} in ISL; I_{d01} and I_{d02} in STL). The smaller ΔV, the faster the logic and the smaller the noise margins are [19,20]. So with ΔV a trade-off is made between speed and noise margins. For circuits with $F_i = F_o = 4$, a ΔV of about 150 - 200 mV is required to obtain positive noise margins [19,20].

At higher currents, ISL will be somewhat slower than STL because of the minority

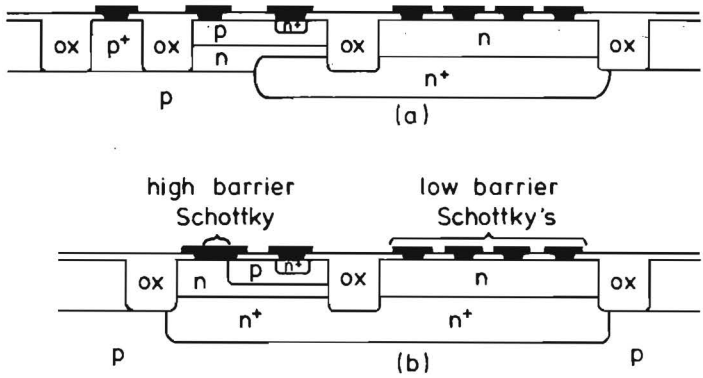

Fig. 15. (a) Not-to-scale cross section of ISL in an oxide-isolated process [13]. (b) Proposed not-to-scale cross section of STL in the same basic process as (a).

carrier storage in the p-n-p (see Section IV). As shown by equation (23), the average propagation delay time is increased with $\alpha^*\tau_p^*/2$, where τ_p^* is the effective forward transit time of the composite p-n-p. Here the thickness of the epitaxial layer and the width of the lateral base are very important. In pn-isolated ISL with a 2.9 μm epitaxial layer and 5 μm details, τ_p^* is 1.5 ns at room temperature (see τ''_{fP} in [12]), which means that the average propagation delay time is increased by about .75 ns. In oxide-isolated ISL with a 1.2 μm epitaxial layer and 3 μm details [13], the relatively slow lateral p-n-p is eliminated, yielding a τ_p^* of about 250 ps (at room temperature), which means that t_{pd} is increased by about 125 ps only. At very high current levels the speed of both ISL and STL is limited by the various series resistance effects. As explained in Section V, it is very difficult to derive mathematical expressions for this region, so computer simulations and experiments have to be carried out.

B. Measurements, simulations and calculations

Fig. 16 shows average propagation delay times versus current per gate for oxide-isolated ISL and STL structures. All have voltage swings of at least 180 mV. Very fast oxide-isolated STL with a voltage swing of 125 mV has also been published [17,18]. However, this logic swing is too small for realistic logic circuits (very small or negative noise margins for $F_i > 1$ and/or $F_o > 1$) and is therefore not indicated in Fig. 16. It is clear from Fig. 16 that ISL and STL have comparable speeds when made in the same process with the same voltage swing. All ISL and STL examples exhibit curved lines at high current levels due to series resistance effects. The measurements on ISL ring oscillators (21 stages) with 3 μm design rules [13] and PtNi-silicide Schottky diodes (ϕ_B = 0.78 eV) were done with the structure shown in Fig. 15(a) [13]. For this structure a model was derived [24] and the circuit simulation provides a t_{pd} curve which is identical

with the measured one (see Fig. 16).

If STL would have been made in the same basic process (see cross section in Fig. 15(b)) with a PtNi-silicide clamp diode (ϕ_B = 0.78 eV) and TiW fan-out diodes (ϕ_B = 0.53 eV) the logic swing would be identical with the ISL swing (≈ 200 mV) and the propagation delay time would indeed be somewhat smaller than that of ISL (see Fig. 16). The main speed difference is caused by τ_p^* in ISL, which makes the delay time about 125 ps longer. Thus a little speed improvement is obtained with STL at the cost of a more complex technology. The calculated propagation delay time for STL and ISL with equations (8) and (23), respectively, is also indicated in Fig. 16.

The following measured parameters are used for both equations C_{bc} = 0.056 pF, C_{cs} = 0.26 pF, C_{be} = 0.035 pF, ΔV = 210 mV, k_1 = 0.7, k_2 = 0.3, α_p^* = 0.96 and τ_p^* = 250 psec. The simulation results for STL and ISL in Fig. 16 were carried out with a 21-stage ring oscillator. The factors k_1 and k_2 belong to this 21-stage ring oscillator (see Section III.C).

At i_s = 50 μA the calculated values are: t_{pdISL} = 1.46 nsec; t_{pdSTL} = 1.33 nsec. These values are very close to the simulated and measured results (see Fig. 16).

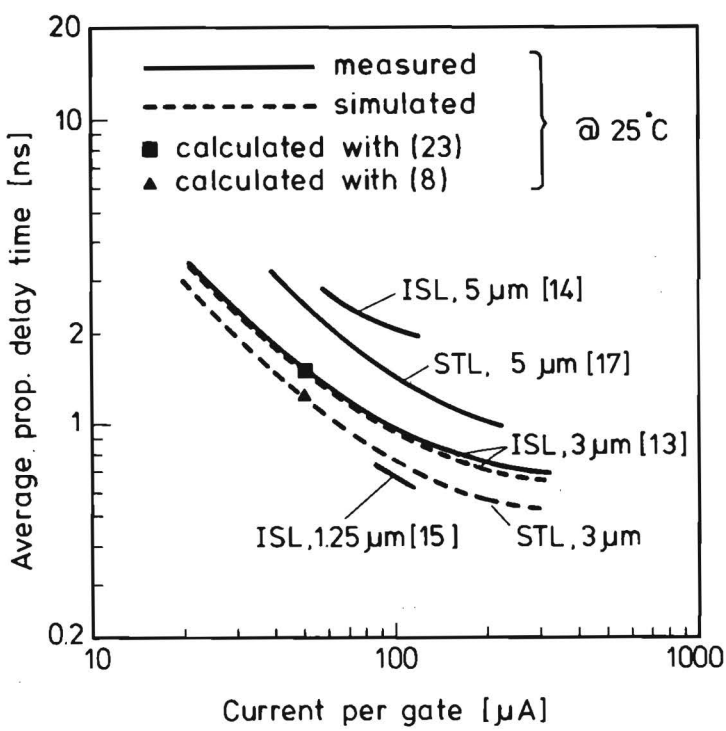

Fig. 16. Measured, simulated and calculated average propagation delay times at room temperature of ISL and STL made in oxide-isolated processes with different minimum details. References are made to [13,14,15,17].

For i_s = 100 μA the calculated values are: t_{pdISL} = 0.79 nsec; t_{pdSTL} = 0.66 nsec. At this current level series resistances are no longer negligible and the curve starts to deviate from these calculated propagation delay times (these calculations are not shown in Fig. 16).

8.VIII. Conclusions

It has been shown that high-speed VLSI candidates ISL and STL are quite similar in behaviour. The only basic difference is that the n-p-n clamp device is a p-n-p in ISL and a Schottky diode in STL. This means that, owing to minority carrier storage in the p-n-p, ISL will be somewhat slower than STL when the logic swing and the junction capcitances are identical. In pn-isolated structures with a combination of a lateral and a vertical p-n-p the extra delay in ISL is about 0,75 ns; in oxide-isolated processes, where the relatively slow lateral p-n-p is eliminated, the extra delay is about 125 ps. Analytical expressions for the average propagation delay time (t_{pd}) have been derived. Both logic forms suffer from delay time increase with fan-in increase. Measures to obtain fan-in independent delay times have been discussed, and it has been shown that they increase the power dissipation. Fan-out can increase the speed of both logic circuits.

Due to the behaviour of the internal node, the measured propagation delay times when starting from the *DC* state will be different from those starting from an *AC* state as ring oscillators. In the latter case shorter propagation delay times will be measured.

Series resistances cause an increase in propagation delay times at higher current levels. Analytical expressions are very difficult to obtain for this region; here information can only be obtained from circuit simulation and measurements. As a general conclusion it can be said that when compared in oxide-isolated structures with thin epilayers STL is marginally faster than ISL at the cost of a more complex technology (two masks extra, and one control of barrier height extra).

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9

Performance, Temperature Behaviour, and First-Order Modeling of ISL

J. Lohstroh and J.D.P. van den Crommenacker

Abstract – **The minimum propagation delay time of Integrated Schottky Logic (ISL) made in a standard LS process is determined by saturation of the vertical p-n-p clamp transistor. A performance improvement is obtained by increasing the dope of the substrate to prevent this saturation effect. When using 5 μm minimum dimensions the minimum propagation delay times is then well below 3 ns over the full temperature range from −55 up to 150°C chip temperature. It is shown that a vertical p-n-p clamp transistor is essential to obtain a high speed when relaxed design rules are used.**

Furthermore, it is shown that ISL can be modeled in a relatively simple manner with one n-p-n transistor and one or two p-n-p transistors, depending on the resistivity of the substrate.

9.I. Introduction

Integrated Schottky Logic (ISL) is a 200 mV voltage swing LSI logic that can be fabricated in standard Schottky processes with a double layer metallization [1]. It fills the gap between low-power Schottky TTL (LS) and integrated injection logic (I^2L) for those circuits where LS consumes too much power and takes up too much chip area, and when I^2L does not attain the required speed.

It has been shown [2] that the minimum propagation delay time of ISL is about five times smaller than that of I^2L, when compared in the same process.

In this paper the performance and temperature behaviour of ISL, fabricated in a standard LS process, is compared with the performance and temperature behaviour in a modified process. Only the original ISL gate with p-n-p clamp is considered.

For ISL made in a standard LS process, a first-order model consisting of one n-p-n transistor and two p-n-p transistors can describe the temperature behaviour adequately. The n-p-n and p-n-p transistor models can be simple one-lump charge control models.

ISL made in the LS process exhibits quite a high temperature coefficient for the

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minimum propagation delay time.

A performance improvement can be achieved with a slightly modified LS process (which has an increased substrate dope level), and using 5 μm minimum dimensions. In that case the minimum propagation delay times can be well below 3 ns over the full temperature range from −55 up to 150°C chip temperature. It will be shown that with sufficiently increased substrate dope levels the ISL model can be simplified to a model with one n-p-n transistor and only one p-n-p transistor.

It will further be shown that the vertical p-n-p clamp transistor is essential to obtain a high switching speed when relaxed minimum design rules are used.

9.II. Measurements and modeling of ISL in a standard LS process

ISL was originally fabricated in a standard process developed for LS. To reduce the collector-island capacitances of the LS gates, the substrate resistivity of the LS process was chosen at a rather high (non-critical) value of 14 Ω•cm. In ISL gates the substrate has not only an isolation function, it also has a conduction function to conduct the current from the vertical p-n-p collector areas to the p^+ isolation grid, which is contacted and grounded at several points on a chip. This introduces a conflicting requirement for the resistivity of the substrate because an effective low-storage clamp action requires that the vertical p-n-p transistor of ISL should not be allowed to go into saturation, which means that only small voltage drops are allowed over the conducting paths in the substrate.

Fig. 1 shows a cross section of an ISL gate (not-to-scale). For a first-order modeling setup the lateral and vertical p-n-p's are modeled separately. The splitup between the transistors is indicated with the dashed lines. The shaded areas indicate the storage of active charge (holes). The distribution of holes in the bases of the p-n-p's is triangular in shape, as long as the transistors are not saturated. In the collector of the saturated n-p-n the hole distribution is block-shaped due to the hole-reflecting buried layer.

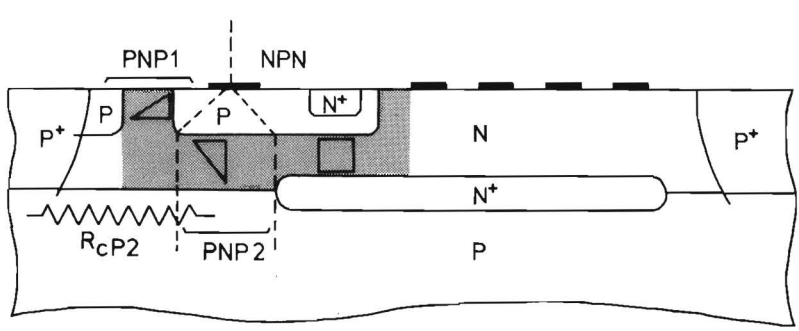


Fig. 1. Cross section of an ISL-gate (not-to-scale). The shaded areas indicate the storage of active charge. The clamp p-n-p transistor is split up into a lateral transistor p-n-p1 and a vertical transistor p-n-p2. The vertical p-n-p2 has a collector series resistance R_{cP2} which limits the speed of ISL in a standard LS process.

The complete model of the ISL gate (without input current source) is shown in Fig. 2. The fixed capacitances represent the depletion capacitances and the variable capacitances represent the storage of active charge.

The modeling and measurements are done for a process with 2.9 μm epitaxial layer and 5 μm minimum details [1]. The thickness of the epitaxial layer decreases during the fabrication process due to silicon consumption (during the various oxidation steps); at the end of the process the thickness is 2.4 μm. Fig. 3 shows a to-scale cross section of the lateral p-n-p, the vertical p-n-p, and the n-p-n transistors; also the depletion layers and the hole distributions are indicated.

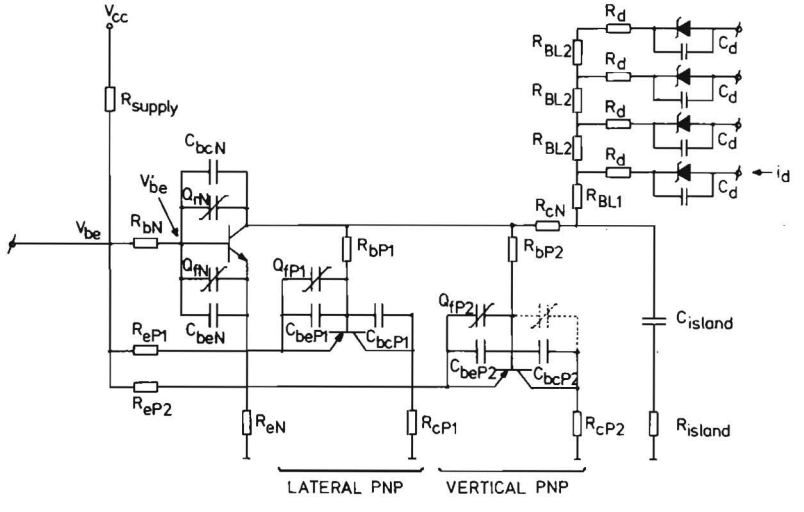


Fig. 2. Model of the ISL gate of Fig. 1.

When the p-n-p's are forward biased, the depletion layer between emitter and base (between p-island and n-epi) is assumed to be neglectably small, which means that active charge has to be taken into account over an effective neutral base thickness W_{Beff} reaching from the metallurgical base-emitter junction towards the base-collector depletion layer [3]. This approach is confirmed by a one-dimensional computer program, using the Poisson equations and the electron and hole continuity equations, and which uses the dope profiles as input [4].

This effective base-thickness of the lateral p-n-p is 2.5 μm and the effective base--thickness of the vertical p-n-p is 1.05 μm (for the lateral p-n-p the mask determined base-width is 4.6 μm, being 5 μm minus two underetch distances of 0.2 μm) (see Fig. 3). The dope of the epitaxial layer is $2.10^{16}cm^{-3}$.

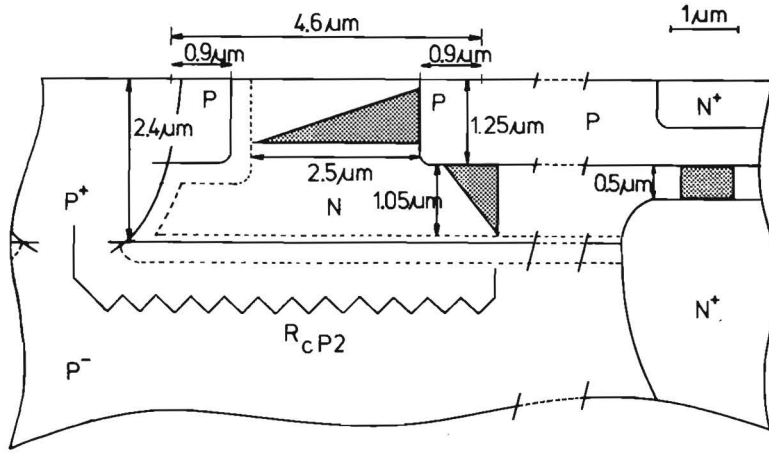


Fig. 3. To scale cross section of the lateral p-n-p, the vertical p-n-p, and n-p-n transistors. The depletion layers and hole distributions are indicated.

The area of the p-island is 15x30 μm, equally divided into 15x15 μm^2 for the region where the buried layer is present underneath (in this region the emitter is placed) and 15x15 μm^2 for the region without buried layer (vertical p-n-p). The area of the lateral p-n-p ($P_E \cdot x_j$) is about 125 μm^2 (where P_E is the perimeter of the lateral p-n-p, and x_j the base junction depth). This means that the saturation current ratio of the lateral and vertical p-n-p equals

$$\frac{I_{oP1}}{I_{oP2}} = \frac{A_{P1}}{W_{BeffP1}} \cdot \frac{W_{BeffP2}}{A_{P2}} \qquad (1)$$

where I_{oP1} and I_{oP2} are the saturation currents of the lateral and vertical p-n-p, respectively, and A_{P1} and A_{P2} the areas of the lateral and vertical p-n-p, respectively. Equation (1) yields 0.23 for the given parameters. Measurements done with gates *with and without* vertical p-n-p (and equal base-island) show that $I_{oP1}/I_{oP2} = 0.25$. This value is somewhat larger than the calculated value because (1) is not corrected for the fact that effective area of the lateral p-n-p is somewhat larger than $P_E \cdot x_j$ [5]. For the simulations $I_{oP1}/I_{oP2} = 0.25$ is taken.

The active hole-charge in the base of the vertical p-n-p and in the collector of the n-p-n are about equal because the areas of the vertical p-n-p and the base-collector junction of the n-p-n are equal (15x15 μm^2 each), and the effective base-width of the vertical p-n-p is twice as thick as the distance between the metallurgical base-collector junction of the n-p-n and the (hole reflecting) buried layer (see Fig. 3).

This implies that the reverse transit time of the n-p-n τ_{rN} equals $\tau_{rN} = \tau_{fP2}/\gamma$, neglecting the extra storage in the base of the n-p-n, where τ_{fP2} is the forward transit time of the vertical p-n-p P-N-P2 and γ the saturation current ratio I_{n0}/I_{oP2} of the n-p-n and the vertical p-n-p. Furthermore, if the forward base current of P-N-P2 and the reverse base current of the n-p-n are assumed to be equal, then $\beta_{rN} = \gamma\beta_{fP2}$, where β_{rN} and β_{fP2} are the reverse current gain of the n-p-n and the forward current gain of the vertical p-n-p, respectively. The junction capacitance between the n-p-n base island and the epi-layer is split up as follows:

$$C_{bcN} = C_{beP1} = C_{beP2}.$$

The n-island to substrate capacitance is devided into C_{island}, being the capacitance of the island under the Schottky diodes, and C_{bcP1} and C_{bcP2} ($C_{bcP1} = 3C_{bcP2}$). For the computer simulations the following measured room temperature values for the most important parameters are used: $\gamma = 0.2$, $\tau_{fN} = 0.1$ ns, $\beta_{fN} = 80$, $\beta_{fP} = 20$, and $\beta_{rN} = \gamma{\cdot}\beta_{fP} = 4$; $C_{beN} = 0.1$ pF, $C_{bcN} = 0.06$ pF, $C_{beP1} = 0.06$ pF, $C_{beP2} = 0.06$ pF, $C_{island} = (0.2 + F{*}0.1)$ pF, where F = fan-out, $C_{bcP1} = 0.15$ pF, $C_{bcP2} = 0.05$ pF, $C_d = 0.04$ pF, $R_{bN} = 300\ \Omega$, $R_{eN} = 6\ \Omega$, $R_{cN} = 14\ \Omega$, $R_{bP1} = 100\ \Omega$, $R_{eP1} = 30\ \Omega$, $R_{cP1} = 30\ \Omega$, $R_{bP2} = 100\ \Omega$, $R_{eP2} = 20\ \Omega$, $R_{cP1} = 8$ kΩ, $R_{island} = 160\ \Omega$, $R_d = 80\ \Omega$, $R_{BL1} = 11\ \Omega$, and $R_{BL2} = 10\ \Omega$. The junction capacitances are given for the non-biased condition.

The room temperature value for the forward transit time of the vertical p-n-p (τ_{fP2}) equals $W^2_{BeffP2}/2D_p = 0.55$ ns and consequently the reverse transit time of the n-p-n equals

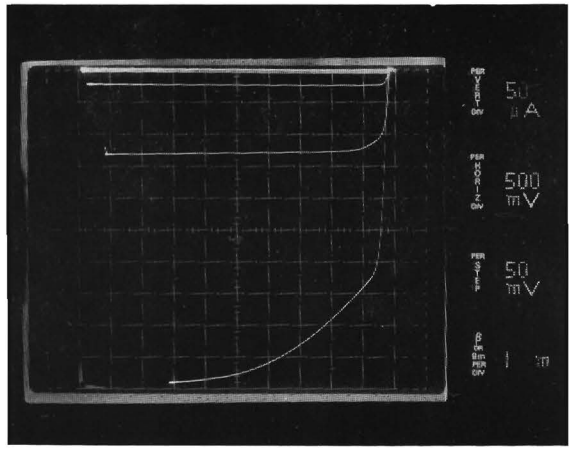
$$\tau_{rN} = \tau_{fP2}/\gamma = 0.55\ \text{ns}/0.2 = 2.8\ \text{ns}.$$

The transit times τ_{fP1} and τ_{rP1} of the lateral p-n-p are equal to $W^2_{BeffP1}/2D_p = 3.1$ ns.

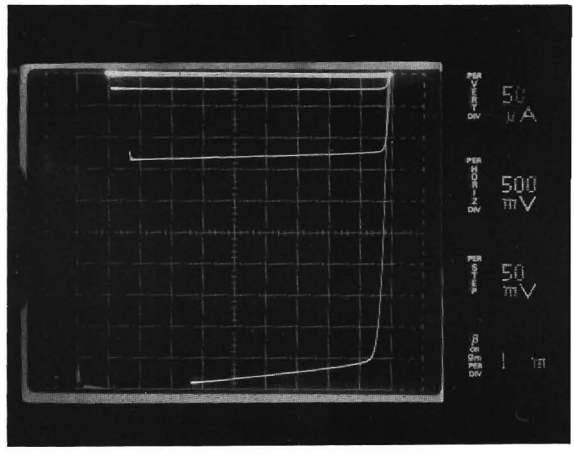
When the vertical p-n-p becomes saturated, electrons are injected into the substrate. The reverse transit time (τ_{rP2}) has been curved fitted to be 5 ns.

The highest series resistance is R_{cP2}, the collector series resistances of the vertical p-n-p. Fig. 4(a) shows a curve tracer picture (I_c/V_{ce}-characteristics) of the lateral and vertical p-n-p in parallel, at room temperature. The larger the combined collector current, the larger V_{ce} has to be bring the vertical p-n-p out of the saturation region. The slope of the saturation region shows that the collector series resistance of the vertical p-n-p is about 8 kΩ.

At higher temperatures than room temperature, all transit times, current gains, capacitances, and resistances will increase, depending on their specific temperature coeffi-



14 OHMCM
(a)



2 OHMCM
(b)

Fig. 4. I_c versus V_{ce} characteristics of the lateral and vertical p-n-p in parallel in a (a) standard LS process made on a 14 Ω•cm substrate, and (b) in a modified process made on a 2 Ω•cm substrate, both at room temperature.

cients. R_{cP2}, which is formed by the low-doped substrate, has the largest temperature coefficient. Measurements have shown that at 150°C chip temperature the resistance of R_{cP2} doubles (from 8 to 16 kΩ).

Fig. 5 shows measured and computer-simulated propagation delay times of ISL made in the LS process with 5 kΩ reistors as current sources, for different currents per gate (obtained by variation of the power supply voltage) and with temperature as parameter. The measurements and simulations were done for an 11-stage ring oscillator. For the simulations the program PHILPAC was used. As shown in Fig. 5, the simulations agree very well with the measurements.

At room temperature the minimum propagation delay time is 2.8 ns for 200 μA/gate and at 150°C the minimum propagation delay time is 6.1 ns at 80 μA/gate. So the temperature coefficient of the minimum delay time is quite high: + 30 ps/°C. From the simulations it can easily be found (from the internal transistor current) that the minimum propagation delay time is determined by the saturation of the vertical p-n-p. The voltage drop across R_{cP2} becomes about 0.7 V at room temperature for a current level of 200 μA/gate. At larger currents the clamp action of the fast vertical p-n-p is lost and the slower lateral p-n-p has to take over. This means that the logic will become slower. With increasing temperature R_{cP2} increases, which means that the saturation of p-n-p2 will occur at a lower current level. To gain some insight into the optimum speed obtainable with ISL at a given temperature, we examine in the next section the intrinsic and extrinsic behaviour versus temperature.

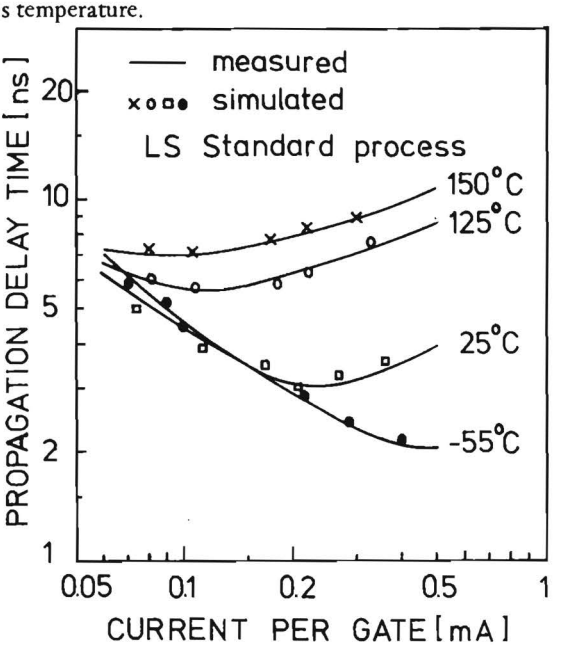


Fig. 5. Measured and computer-simulated propagation delay times for an 11-stage ring oscillator for different average currents per gate, with temperature as parameter, of ISL made in a standard LS process.

9.III. Intrinsic and extrinsic behaviour versus temperature of ISL

The extrinsic behaviour of ISL is the measured behaviour. Here the transistor transit times, the junction capacitances, and the series resistances determine the speed of the logic. The intrinsic behaviour would be the behaviour when all junction capacitances and series resistances are ignored, and the absolute minimum propagation delay is obtained independently of the current level.

A. Intrinsic behaviour

To study the intrinsic behaviour of ISL, we carried out computer simulations for an 11-stage ring oscillator with fan-out = 1 (see Fig. 6). Fig. 7 shows three succeeding node voltages V_{be}, three succeeding Schottky diode currents i_d, and three succeeding combined p-n-p collector currents $i_{cP} = i_{cP1} + i_{cP2}$ of three succeeding stages of the ring oscillator of Fig. 6, for 25°C (see Fig. 7(a)) and 150°C (see Fig. 7(b)), for $R_{supply} = 5$ kΩ, and $V_{cc} = 1.7$ V (resulting in an average current per gate of about 200 μA).

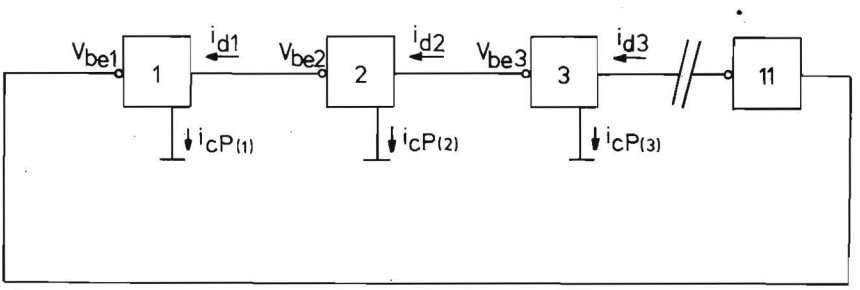


Fig. 6. Part of an 11-stage ring oscillator with fan-out = 1, V_{be}, i_d, and $i_{cP} = i_{cP1} + i_{cP2}$ of three succeeding states as presented in Fig. 7-9, and indicated in Fig. 2.

Without the series resistances the lateral and vertical p-n-p can be combined to form one transistor with a saturation current which is the sum of the saturation currents of both transistors, and a forward transit time τ'_{fP} which is the weighted average of τ_{fP1} and τ_{fP2} ($\tau'_{fP} = (I_{oP1} \cdot \tau_{fP1} + I_{oP2} \cdot \tau_{fP2})/(I_{oP1} + I_{oP2})$).

Furthermore, Q_{rN} (see Fig. 2) can be wholly ascribed to the forward minority charge storage of the combined p-n-p.

With equal charges in the collector of the n-p-n and in the base of the vertical p-n-p ($Q_{rN} = Q_{fP2}$) the forward transit time of the combined p-n-p becomes $\tau''_{fP} = (I_{oP1}\tau_{fP1} + 2I_{oP2}\tau_{fP2})/(I_{oP1} + I_{oP2})$. The reverse transit time of the n-p-n τ''_{rN} will then be zero. At room temperature (25°C), $\tau''_{fP} = 1.5$ ns, and at 150°C $\tau''_{fP} = 2.6$ ns (τ is proportional to $(T/T_{ref})^{1.6}$). As the intrinsic current-independent propagation delay time is given by $\tau''_{fP}/2$ [2], the delay times would have been 0.75 and 1.3 ns, respectively. The

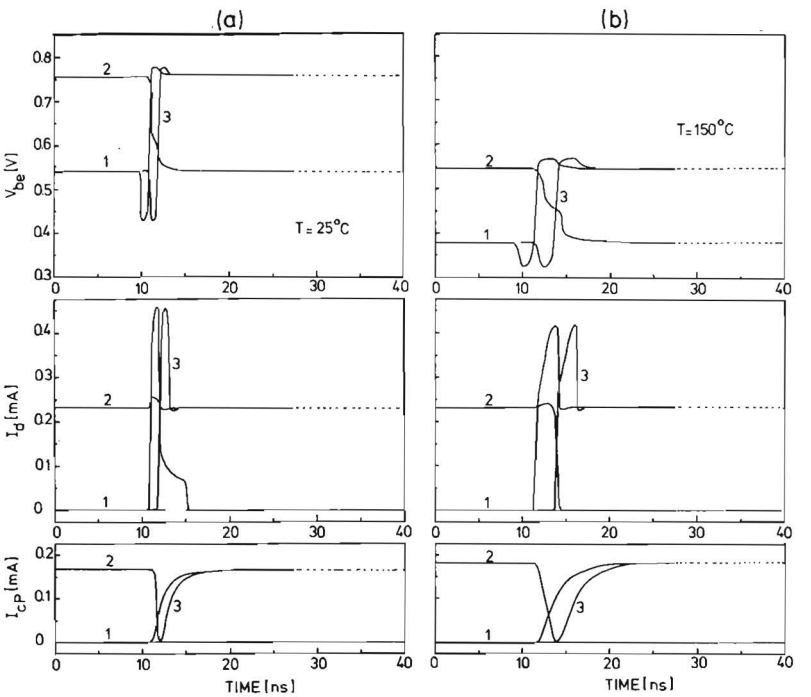


Fig. 7. Computer simulations for (a) 25°C and (b) 150 °C of a ring oscillator with fan-out = 1 for the *intrinsic* current-independent case where all series resistances and junction capacitances are neglected. Shown are V_{be}, i_d, and $i_{cP} = i_{cP1} + i_{cP2}$ of three succeeding stages (see Fig. 6). R_{supply} = 5 kΩ and V_{cc} = 1.7 V.

simulated results are somewhat faster (0.5 and 1.2 ns), due to the fact that the resistors are not constant current sources (the input current of a gate is smaller than the n-p-n collector current) and the base currents of the transistors are not zero. For T = 150°C the logic swing is decreased from 210 to 150 mV owing to the difference in temperature coefficients of the saturation currents of the p-n-p transistors and Schottky diode; this difference is about 0.5 mV/°C. For the p-n-p transistor the saturation current is proportional to $T^{1.6}\exp(-qV_g/kT)$; whereas the saturation current of the Schottky diode is proportional to $T^2\exp(-q\phi_B/kT)$, where V_g and ϕ_B (= 0.78 V) are the silicon band-gap and Schottky barrier height, respectively.

Notice that i_d has a current peak with a magnitude of double the supply current.

B. Extrinsic behaviour without junction capacitances for 200 μA/gate

Fig. 8 shows for 25°C (see Fig. 8(a)) and 150°C (see Fig. 8(b)) the behaviour of the gates, now with series resistances included, but the junction capacitances still neglected, and at the same current level of 200 μA/gate. The delay times are increased considerably (1 and 4.5 ns, respectively) compared with the intrinsic case. This is mainly due to the

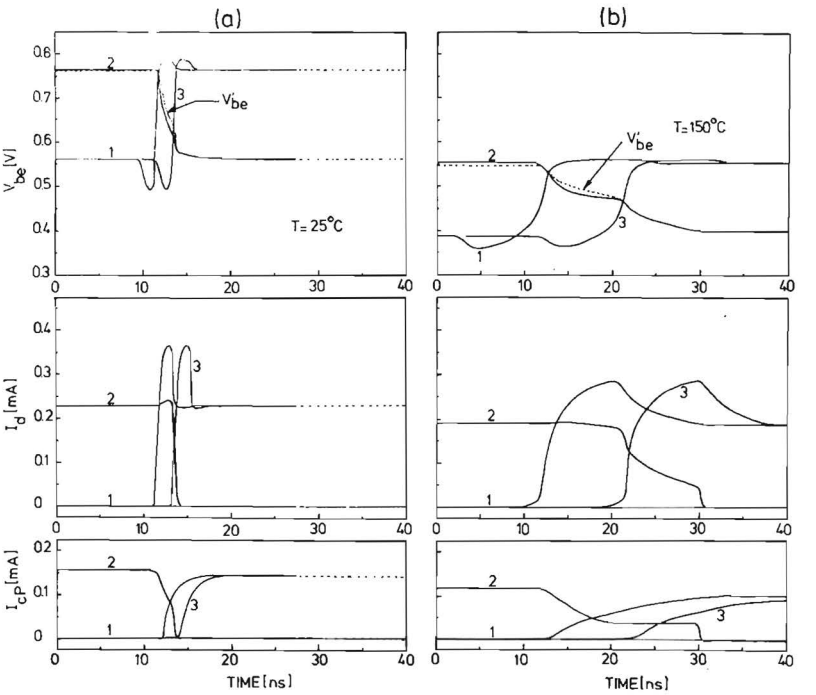


Fig. 8. As Fig. 7, but now for the *extrinsic* case where the *junction capacitances are still neglected.* The series resistances are included and belong to the standard LS process. The current per gate is 200 μA, and the vertical p-n-p goes into saturation, causing a much longer propagation delay time. Furthermore, the internal V'_{be} of the n-p-n (indicated by dashed line) lags behind, due to a voltage drop across R_{bN}. This effect prevents a fast switch-OFF of the n-p-n.

fact that the vertical p-n-p goes into saturation, which is caused by the voltage drop across R_{cP2}, the collector series resistance of the vertical p-n-p. The saturation becomes more severe at elevated temperatures, due to the large temperature coefficient of R_{cP2}. The resistance value of R_{cP2} increases from 8 kΩ at 25°C to 16 kΩ at 150°C. This means that at higher temperatures the vertical p-n-p will go into saturation at smaller currents.

Another limiting effect is caused by the active charge Q_{fN} in the collector of the n-p-n, which has to be removed through the base series resistance R_{bN} to switch OFF the n-p-n. During the switch-OFF action of the n-p-n a voltage is developed across R_{bN}, causing V'_{be} (internal base-emitter voltage, see Fig. 2) to lag behind (see dashed lines in Fig. 8) and preventing a fast switch-OFF. Mainly at 150°C, where R_{bN} has its largest value and where also the voltage swing is reduced, this effect imposes a real limitation on the speed of ISL.

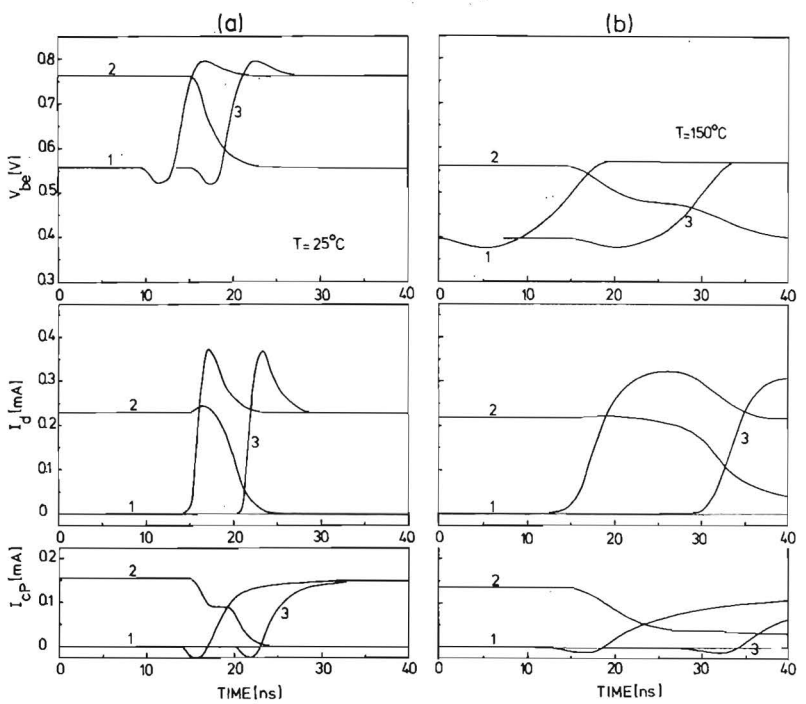


Fig. 9. As Fig. 8, but now in the complete *extrinsic* case. Compared with Fig. 8 all junction capacitances are included (belonging to the standard LS process).

C. Extrinsic behaviour at 200 μA/gate

Fig. 9 shows the voltage and currents with all series resistances and junction capacitances included.

The delay times at 25 and 150°C are now increased to 3 and 7.7 ns respectively. Note the extra current spikes in i_{cP}, which arise during charging and discharging of $C_{bcP1} + C_{bcP2}$.

9.IV. Measurements and modeling of ISL in an improved process (ISL process)

As shown in the previous section, the minimum propagation delay time of ISL made in a standard LS process is determined by saturation of the vertical p-n-p. With a sufficiently negative biased substrate this saturation effect could be prevented; however, this means that an extra supply voltage would be necessary and that the power dissipation of the gates in the ON state would be increased dramatically. A better solution is to increase the substrate dope level to decrease the collector series resistance R_{cP2} and prevent saturation at not too high current levels. Doing this, the collector-island junction capa-

citances will increase, which means that the speed of the logic is affected at low current levels. It has been found that a substrate resistivity of 2 Ω•cm is a good compromise. The extrinsic speed will be much closer to the intrinsic speed in this case.

Fig. 4(b) shows the curve tracer picture of the vertical and lateral p-n-p in parallel at room temperature; saturation of the vertical p-n-p is hardly perceptible anymore (compare with Fig. 4 (a)). The model can be simplified in this case by combining the vertical and lateral p-n-p in one model, by summation of the saturation currents, and introduction of the weighted average of the transit times $\tau'_{fP} = (I_{oP1} \cdot \tau_{fP1} + I_{oP2} \cdot \tau_{fP2})/(I_{oP1} + I_{oP2})$. Taking the same transit times as in Section II and having $I_{oP2} = 4I_{oP1}$ then $\tau'_{fP} = 1.1$ ns. Furthermore, C_{bcP1}, C_{bcP2}, and C_{island} are increased by 40 percent.

Fig. 10 shows the measured and computer-simulated propagation delay times of ISL made on a substrate with a resistivity of 2 Ω•cm. The simulations agree very well with the measurements. At room temperature the minimum propagation delay time is 1.7 ns at 1 mA/gate, and at 150°C the minimum propagation delay time is 2.8 ns at 350 μA/gate. The temperature coefficient of the minimum propagation delay times is now reduced to 6 ps/°C. This means that the performance is improved considerably compared with ISL made in a standard Schottky process.

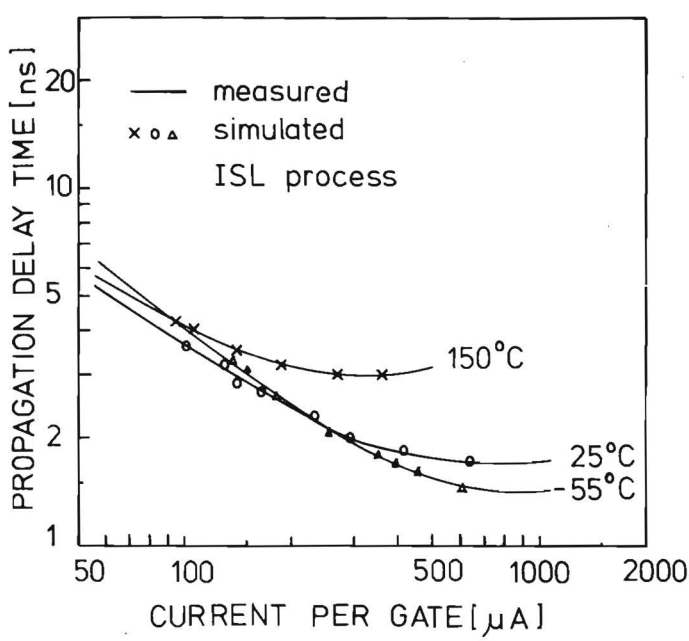


Fig. 10. Measured and computer-simulated propagation delay times for an 11-stage ring oscillator for different average currents per gate, with teperature as parameter, of ISL made on a substrate with a resitivity of 2 Ω•cm.

9.V. ISL performance with lateral p-n-p only

As stated in [1], the speed of ISL in standard processes is mainly determined by the base-thickness of the vertical p-n-p. Measurements of ISL with and without vertical p-n-p underline this statement. Fig. 11 shows the measured propagation delay times of ISL made in the ISL process, with and without vertical p-n-p (in the version without vertical p-n-p, the buried layer is not cut away under the base contact). The measurements are done for room temperature. Fig. 11 shows that without vertical p-n-p (which means that only the lateral p-n-p is doing the clamp action) the performance is decreased dramatically. The question can now be arised what the basewidth of the lateral p-n-p should be to obtain the same performance as ISL with the vertical p-n-p. In that case the same room temperature value of $\tau''_{fP} = 1.5$ ns should be obtained for ISL with lateral p-n-p only (τ''_{fP} is the forward transit time of the p-n-p with Q_{rN} wholly ascribed to the p-n-p; see Section III.*A*). It can easily be shown that in that case

$$\tau''_{fP} = \frac{W^2_{BeffP1}}{2D_P} + \frac{A_{base\ island}}{A_{P1}} \cdot \frac{W_{BeffP1} \cdot W_C}{D_P} \tag{2}$$

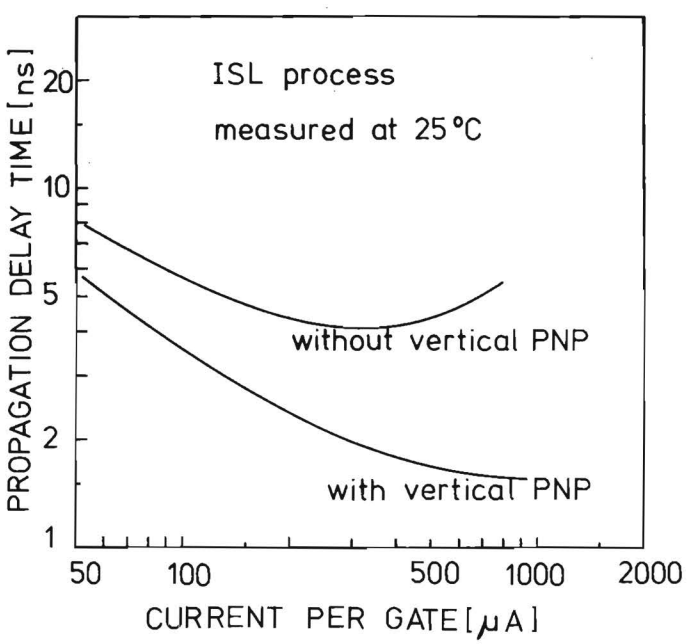


Fig. 11. Measured propagation delay time of ISL *with* and *without* vertical p-n-p, made in the ISL process. In the case without vertical p-n-p, only the lateral p-n-p is present which has a much thicker base than the vertical p-n-p. Only with improved lithography a thin base could be achieved for the lateral p-n-p. With relaxed design rules it is much easier to rely on the vertical p-n-p.

where W_C is the thickness of the epitaxial layer between base and buried layer (metallurgical junctions) and $A_{\text{base island}}$ is the total area of the base island. With $W_C = 0.5\ \mu m$ (see Fig. 3), $A_{\text{base island}} = 15 \times 30\ \mu m^2$, and $A_{P1} = 125\ \mu m^2$, (2) yields 1.5 ns for $W_{\text{BeffP1}} = 0.7\ \mu m$. This implies that the distance between the diffusion openings of the lateral p-n-p should be 2.8 μm, using the same process. This value is quite small for standard contact printing processes which will also give large spread on this value (the spread directly influences the speed of the logic). Therefore, it is much easier to rely on the vertical p-n-p when more relaxed design rules are used.

9.VI. Conclusions

It has been shown that the minimum propagation delay time of ISL, made in a standard LS process with 5 μm design rules, is determined by saturation of the vertical p-n-p transistor. The temperature coefficient of the minimum propagation delay time is rather high in this case.

Improved performance is achieved by increasing of the dope of the substrate. It is then found that the minimum propagation delay time is well below 3 ns over the full temperature range from -55 up to 150°C chip temperature; moreover, the temperature coefficient of the minimum propagation delay time is reduced to the very low level of 6 ps/°C.

Although ISL can operate with a lateral p-n-p clamp only, it is much easier to rely on a vertical p-n-p because in that case the layout rule independent base-thickness of the vertical p-n-p can be thin enough to achieve a high speed logic. When a lateral p-n-p is used only, the lithography needs to be improved to obtain design rules below 3 μm.

It has been shown that ISL can be modeled in a relatively simple manner with one n-p-n transistor and one or two p-n-p transistors, depending on the restitivity of the substrate.

Acknowledgment

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10

First-order Modeling of Oxide-Isolated ISL

J. Lohstroh and R.M. Pluta

Abstract — **A model is derived for an oxide-isolated ISL gate with fan-out = 4. The model includes an n-p-n transistor, a p-n-p transistor, a silicon diode and four Schottky barrier diodes. Special attention is paid to all temperature coefficients of the device parameters.**

Very good agreement is obtained with measurements in the temperature range from 25°C to 125°C.

Due to the p^+ channel stopper in the process, the collector series resistance of the clamp-p-n-p is relatively small.

10.I. Introduction

After the first ISL generation which was made in pn-isolated processes [1], the second ISL generation uses oxide-isolated processes to obtain a much better performance and packing density suitable for high speed VLSI [2-5].

The average propagation delay time of ISL is relatively easily calculated for low and intermediate current levels [5]; at high current levels series resistances start to play a dominant role, which makes an analytical calculation practically impossible, so for that current region only measurements and/or computer simulations can be done [5]. For this last approach an appropriate model which models at least all first-order effects is needed.

A first-order model of pn-isolated ISL has already been published [6].

In this paper a model is derived for the oxide isolated case, including walled emitters, buried layers (covered with oxide or epitaxial material), channel-stop ion-implants, etc. Special attention is paid to temperature coefficients of resistors, capacitors, bandgap-voltages and Schottky barrier heights.

Only oxide-isolated ISL with vertical p-n-p clamp [3] is modeled.

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10.II. Device structure

Fig. 1 shows a top view and cross section of an oxide-isolated ISL [3] testgate which has an additional collector contact compared with the gates used in an 21-stage ring oscillator (see Fig. 2). This collector contact is used to determine some device parameters (Schottky diode series resistance, p-n-p effective current gain, etc.); the collector contact is not used in the eventual ISL gate model, because in ISL circuits this contact is not needed.

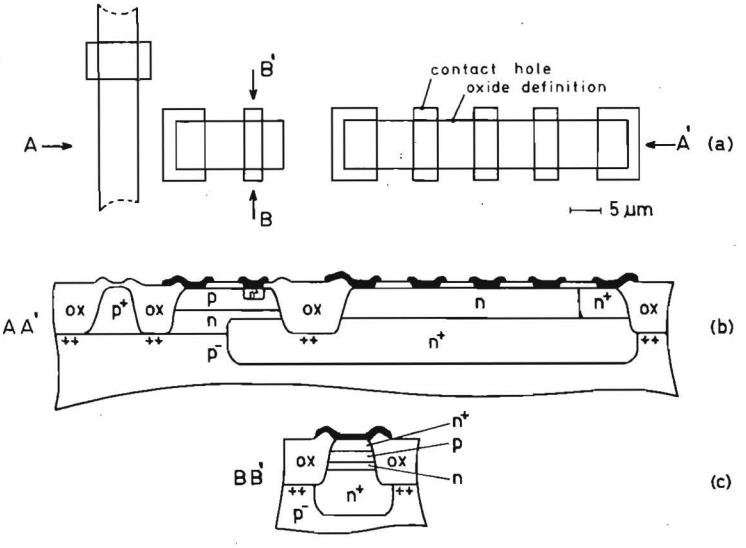

Fig. 1. Top view (a), and cross sections (b,c) of oxide-isolated ISL made with 3 µm min. details [3]. The vertical dimensions are not to scale. Self-aligned channel-stoppers are present under the thick oxide.

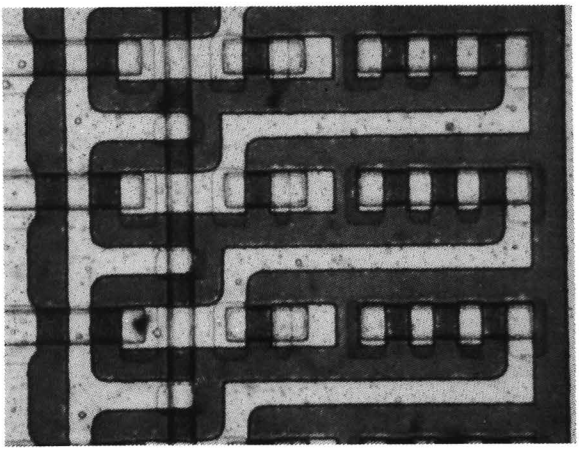

Fig. 2. A part of the 21-stage ring oscillator in which the gate of Fig. 1 (without collector contact) is used. The second layer metal which connects all the n-p-n emitters is not present.

Fig. 1. shows the lateral dimensions after all processing steps. The substrate is 5 Ω•cm and an Sb buried layer is made before epitaxial growth. The resistivity of the epitaxial layer is 0.3 Ω•cm (2.10^{16} cm^{-3}); after all oxidation steps the epithickness is reduced from 1.2 μm to 1.0 μm. The updiffusion of the buried layer is 0.3 μm. Under the isolation oxide a p-type channel stop is made to prevent n-MOS channels between the buried layers. Base and emitter junction depths are 0.5 and 0.25 μm respectively. Fig. 3 shows the profiles. All contacts are covered with PtNi (60%, 40%) to form PtNi-silicide. Ohmic contacts are made to the base and emitter; Schottky barrier diodes are made to the epilayer.

Typical sheet resistances are 30 Ω/□ and 50 Ω/□ for the buried layer when covered with epitaxial material or oxide respectively, 600 Ω/□ for the base diffusion, 8 kΩ/□ for the pinched-base area, and 28 Ω/□ for the emitter. As shown by Fig. 1 the base, the

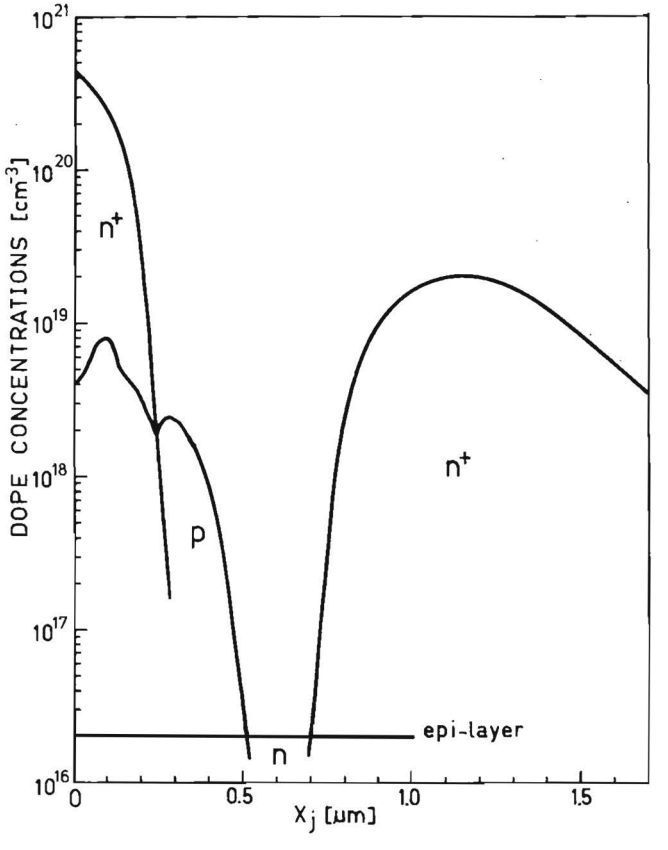

Fig. 3. Dope profiles of emitter, base and buried layer of the oxide-isolated process.

emitter and the Schottky diodes are partly walled.

The substrate is contacted and grounded with a deep p^+ plug, placed as close as possible to the vertical p-n-p, to obtain a low-ohmic path for its collector current.

10.III. Modeling of the merged transistor part

The most complicated part of the ISL structure is the merged transistor part. In the subsequent sections, series resistances, transit times and depletion capacitances are considered and it is indicated how a reasonable split-up is made to model the structure with a minimum number of basic modeling elements.

A. Series resistances

Fig. 4 shows all relevant series resistances. Although the merged structure could be modeled roughly with only one n-p-n and one p-n-p transistor, the distribution of junction capacitance, diffusion capacitance (hole storage) and series resistance around the n-p-n requires in principle a split-up into more elements, mainly because of the high pinched resistance (~ 8 kΩ/□) of the base area of the n-p-n. As shown in Fig. 4, the introduction of two extra diodes (D1 and D2) is in agreement with the physical reality.

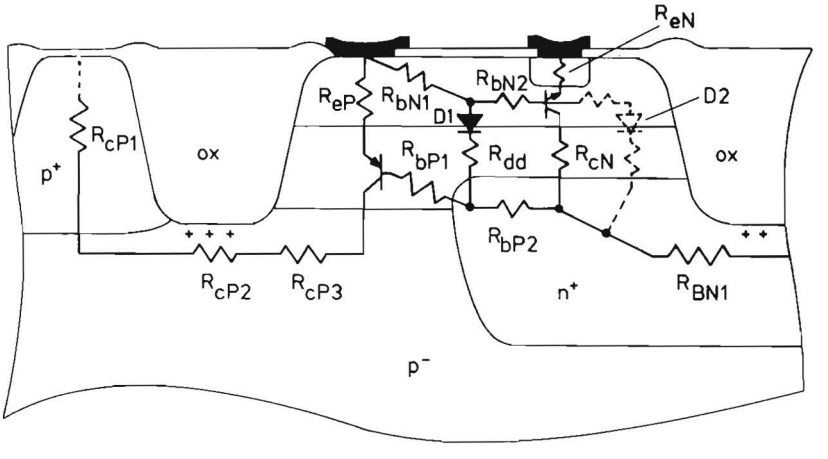

Fig. 4. Not to scale cross section of the merged transistor part of oxide-isolated ISL. All relevant resistances, transistors and diodes are shown. Diode D2 increases the accuracy of the model only marginally, and is left out in the final model.

By doing simulations, including D1 and D2, and simulations including D1 only (with D2 combined with the n-p-n), only marginally small differences in propagation delay times were found. The trade-off between accuracy and minimization of simulation time favored the last one, so in the final model diode D2 was left out.

Most series resistances are obtained by calculation from measured sheet resistances. As effective base-series-resistance of the n-p-n transistor, 1/3 of the total pinched resistance under the emitter is taken.

The effective base-series-resistance of the p-n-p is calculated as two resistances in series, a) the epi-resistance from buried layer to epi region under the metal contact of the p-n-p emitter, b) 1/3 of the epi-resistance under the metal contact. This is done because most base current of the p-n-p is an electron current flowing from the epilayer to the metal contact [7].

The collector series resistance of the vertical p-n-p consists of three parts: the resistance of the p^+ plug R_{cP1}, the resistance R_{cP2} which is the lateral resistance of the p^+ channel stop shunted by the p^- substrate material, and R_{cP3} which is the effective resistance between the point where the (self-aligned) channel-stopper is discontinued and the collector of the vertical p-n-p. None of these resistances can be measured separately; only the total resistance $R_{cP} = R_{cP1} + R_{cP2} + R_{cP3}$ can be measured. R_{cP1} consists of a lateral part (due to the lay-out considerations; see Figs. 1 and 2) and a vertical part; this total resistance is low. R_{cP2} depends mainly on the ion-implant dose of the channel-stopper. R_{cP3} depends on $\rho_{substrate}$ and the distance between the channel-stopper and the collector of the p-n-p. Although this last distance is not more than a few micrometers, with a low substrate dope R_{cP3} is dominant. Measurements of the structure described in Section II, which is made with a channel-stopper with a maximum boron concentration of $8.10^{16}\,cm^{-3}$ under the oxide, show that R_{cP} is not more than 1.5 kΩ, which is considerably smaller than in the pn-isolated structure where this resistance is about 8 kΩ [6]. So the oxide isolation with self-aligned channel-stopper reduces R_{cP} to an acceptably low level without the need to decrease $\rho_{substrate}$ to prevent saturation of the vertical p-n-p. This means that no trade-off between R_{cP} and the island capacitance has to be made when this type of oxide-isolated ISL is operated up to a current level of 200 μA/gate.

B. Transit times and transistor base-currents

Fig. 5 shows an appropriate split-up of the merged transistor structure into a p-n-p, a diode and an n-p-n transistor. When the n-p-n transistor goes into saturation, the base collector junction injects more holes outside the intrinsic n-p-n region than inside the intrinsic n-p-n region, due to a larger voltage drop over the high base-series-resistance of the n-p-n (R_{bN2} = 2 kΩ) than the voltage drop over its relatively small internal collector-series-resistance (R_{cN} = 30 Ω).

As a first-order approximation all hole injection in the n-p-n region is modeled by the diode, and the hole storage under the n-p-n transistor is than assumed to occur by lateral flow of holes.

The diode current is one of the components of the effective p-n-p base current,

when the current gain of the structure of Fig. 5 is measured as a p-n-p, with the n-p-n emitter left floating. This measured current gain β_{fPeff} of the complete structure is 40. In the appendix it is calculated, with device parameters obtained from measurements on vertical p-n-p test-structures with buried layers [7], that the forward current gain of the p-n-p transistor is 48. Also calculated in the appendix is the saturation current of the diode, as well as the reverse current gain of the n-p-n ($I_{ddo} = 33.10^{-21}$ and $\beta_{rN} = 300$).

The forward transit time τ_{fP} of the vertical p-n-p is calculated with $W^2_{Beff}/2D_p$ [6], where W_{Beff} is the effective neutral base width reaching from the metallurgical base-emitter junction towards the base-collector depletion layer. In our particular case (see Section II), τ_{fP} is calculated to be 0.13 ns. The hole storage in the p-n-p (see triangle in Fig. 5) is directly related to the collector current of the p-n-p ($Q_{p\text{-}n\text{-}p} = i_{cP} \cdot \tau_{fP}$).

The ratio between the hole storage in the diode and the p-n-p is $Q_{diode}/Q_{p\text{-}n\text{-}p} = A_{diode} W_{diode}/(\frac{1}{2} A_{p\text{-}n\text{-}p} W_{Beffp\text{-}n\text{-}p})$, where A_{diode} and $A_{p\text{-}n\text{-}p}$ are the areas of the diode and p-n-p respectively in which hole storage is present (see Fig. 5), and W_{diode} is the distance between the metallurgical pn junction and nn^+ junction. In our process with the lay-out shown in Fig. 1, this ratio is 0.9 (in the pn isolated case this value is 1 [6]).

The transit time of the diode τ_{dd} is now calculted to be $\tau_{dd} = (Q_{diode}/Q_{p\text{-}n\text{-}p}) \cdot (I_{po}/I_{ddo}) \cdot \tau_{fP} = 177$ ns. If all hole storage were associated with the p-n-p, then τ_p^*, being the effective forward transit time of the p-n-p [5], would become $\tau_p^* = (1 + Q_{diode}/Q_{p\text{-}n\text{-}p}) \cdot \tau_{fP} = 0.25$ ns.

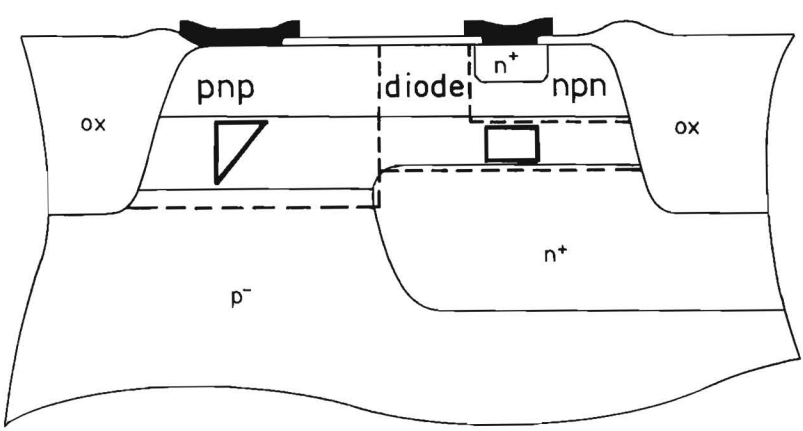

Fig. 5. Split-up of the merged transistor structure into a p-n-p, a diode and a n-p-n transistor (not to scale cross section). The hole storage under the base of saturated n-p-n is associated with the diode. Hole storage is indicated for the p-n-p (triangle) and diode (box).

C. Depletion capacitances

The depletion capacitances of the p-n-p (C_{eP} and C_{cP}), the diode (C_{dd}) and the n-p-n (C_{eN} and C_{cN}) are indicated in Fig. 6. The distributed capacitance of the buried layer to the substrate is combined in one single capacitance which is introduced in the Schottky diode part of the ISL gate (Fig. 7).

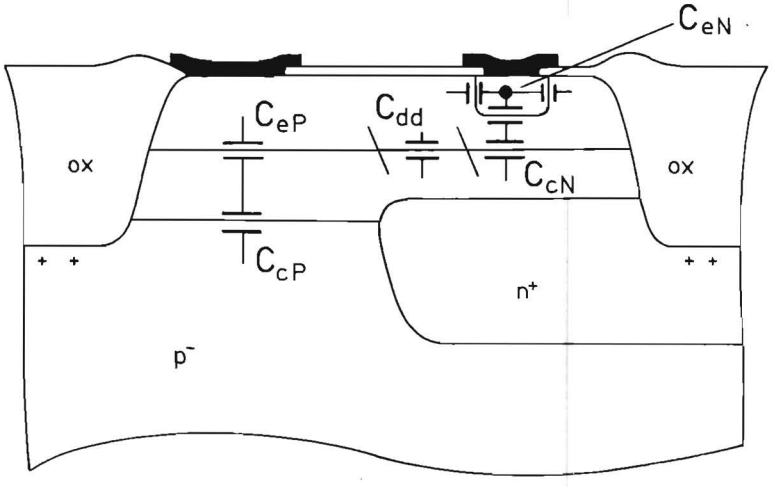

Fig. 6. Depletion capacitances in the merged transistor structure (not to scale cross section).

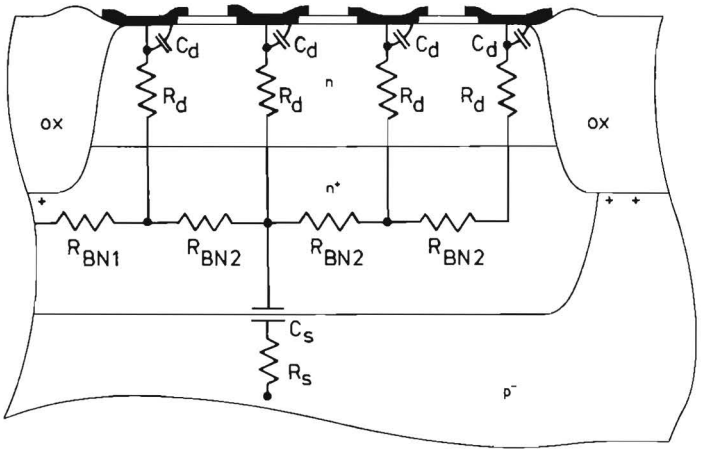

Fig. 7. Not to scale cross section of the Schottky diode part. All distributed depletion capacitances of the buried layer are modeled with one capacitance.

10.IV. Modeling of the Schottky diode part

Fig. 6 shows the split-up into Schottky diodes and resistances in the Schottky diode part of the ISL gate. The resistance R_{BN1} is the effective resistance between the collector of the n-p-n (see Fig. 4) and the first Schottky diode. Here the buried layer is partly under the epitaxial layer and partly under the thick oxide; in these regions the sheet resistances are different, so the total resistance has to be modeled carefully.

The capacitance of the buried layer to the substrate can be modeled with only one junction capacitance C_s, due to the relatively low series resistance in the buried layer (RC times are here neglected).

10.V. The complete model of an ISL gate

Fig. 8 shows the complete model of the oxide-isolated ISL gate with fan-out = 4; here the results obtained from Figs. 4-7 are combined together with R_p, C_p and C_w which model the ion-implanted power supply resistor (R_p), its effective capacitance to the substrate (C_p), and the fan-in wiring capacitance (C_w) of the metallization to the substrate (thick-oxide capacitance).

As in standard simulation programs transistor models and diode models are available with base, emitter and collector series resistances and also base-emitter and base--collector depletion capacitances included; the total node count of the model is 14.

The most relevant parameters at room temperature obtained from measurements, calculatons and some estimations, are listed in table 1.

For the capacitances measured values of capacitance per unit area and per unit perimeter and grading factors of all pn junctions are known [7]. The buried layer has a higher capacitance per unit area for the sidewalls than for the bottom, due to its overlap with the channel-stopper under the field oxide. Resistances are obtained by calculation

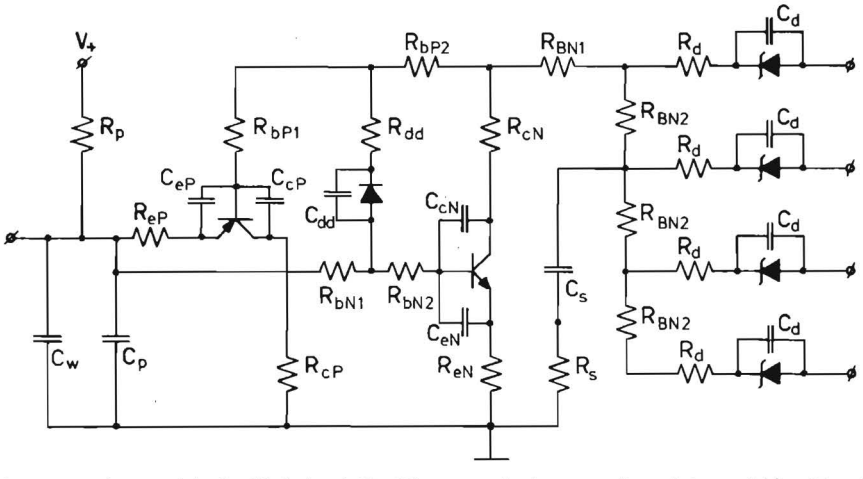

Fig. 8. Complete model of oxide-isolated ISL. When a standard program is used the model has 14 nodes.

pnp	npn	diode	Schottky diode
$I_{po}=5.10^{-17}$A	$I_{no}=10^{-17}$A	$I_{ddo}=33.10^{-21}$A	$I_{do}=25.10^{-14}$A
$\beta_{fP}=48$	$\beta_{fN}=70$	$\tau_{dd}=177$ns	$R_d=70\Omega$
$\beta_{rP}=0.04$	$\beta_{rN}=300$	$R_{dd}=40\Omega$	$C_d=0.008$pF
$\tau_{fP}=0.13$ns	$\tau_{fN}=28$ps	$C_{dd}=0.009$pF	
$\tau_{rP}=5$ns	$\tau_{rN}=75$ps	resistors	capacitances
$R_{eP}=20\Omega$	$R_{eN}=10\Omega$	$R_{bN1}=1k\Omega$	$C_s=0.2$pF
$R_{bP1}=6k\Omega$	$R_{bN2}=2k\Omega$	$R_{bP2}=30\Omega$	$C_p=0.015$pF
$R_{cP}=1.1k\Omega$	$R_{cN}=30\Omega$	$R_{BN1}=100\Omega$	C_w=circuit dependent
$C_{eP}=0.025$pF	$C_{eN}=0.04$pF	$R_{BN2}=45\Omega$	
$C_{cP}=0.007$pF	$C_{cN}=0.009$pF	$R_s=200\Omega, R_p=12k\Omega$	

Table 1. Most relevant parameters at room temperature of the complete model shown in Fig. 8.

from measured sheet resistances, calculated from dope profiles or by direct measurements. The parameters β_{fP}, β_{rN} and I_{ddo} are obtained from the measured value of $\beta_{fP\,eff} = 40$ as shown in Section III.*B* and in the appendix. The parameters τ_{fP} and τ_{dd} are also calculated as shown before. The parameters β_{rP} and τ_{rP} have been estimated; they do not play a role as long as the p-n-p transitor does not go into saturation (no saturation is a requirement for a properly functioning ISL gate anyway). The parameter τ_{rN}, the reverse n-p-n base transit time (retarding field) is also estimated; its accuracy is not very important because the hole storage in the epitaxial layer (modeled with the diode) is much larger than the electron storage in the reverse n-p-n base.

10.VI. Temperature dependency of model parameters

Saturation currents, transit times in transistors and diodes, depletion capacitances, built-in voltages, current gains of transistors and resistances are all temperature dependent parameters.

These temperature effects will be discussed in the above mentioned sequence. Table 2 contains all the temperature coefficients used in the model.

A. Saturation currents of transistors and Schottky diodes

The voltage swing of ISL is determined mainly by the saturation currents of the p-n-p and the Schottky diodes [5], and therefore these parameters have to be modeled carefully as a function of temperature.

The saturation current of the p-n-p transistor can be written as:

$$I_{poT} = I_{poR}\left(\frac{T}{T_R}\right)^{1.8} \exp\left[\frac{qV_{G0}}{k}\left(\frac{1}{T_R} - \frac{1}{T}\right)\right], \qquad (1)$$

pnp	npn	diode	resistors
$T\beta_{fP}=2.10^{-3}$ $T\beta_{rP}=2.10^{-3}$	$T\beta_{fN}=56.10^{-4}$ $T\beta_{rN}=27.10^{-4}$ $T^2\beta_{rN}=-7.10^{-6}$		$TR_{bN1}=2.10^{-4}$ $T^2R_{bN1}=7.10^{-6}$ $TR_{bP2}=13.10^{-4}$ $TR_{BN1}=TR_{BN2}=13.10^{-4}$ $TR_s=8.10^{-3}$ $TR_p=3.10^{-3}$ $TR_d=6.10^{-3}$
$TV_{bieP}=-24.10^{-4}$ $TV_{bicP}=-32.10^{-4}$	$TV_{bieN}=-2.10^{-3}$ $TV_{bicN}=-24.10^{-4}$	$TV_{bi}=-24.10^{-4}$	
$TC_{eP}=12.10^{-4}$ $TC_{cP}=16.10^{-4}$	$TC_{eN}=10^{-3}$ $TC_{cN}=12.10^{-4}$	$TC_{dd}=12.10^{-4}$	capacitances
			$TC_s=16.10^{-4}$ $TC_p=12.10^{-4}$
$TR_{eP}=2.10^{-4}$ $T^2R_{eP}=7.10^{-6}$ $TR_{bP1}=6.10^{-3}$ $TR_{cP}=8.10^{-3}$	$TR_{eN}=10^{-3}$ $TR_{bN2}=2.10^{-3}$ $T^2R_{bN2}=6.10^{-6}$ $TR_{cN}=6.10^{-3}$	$TR_{dd}=6.10^{-3}$	

Table 2. All temperature coefficients used in the model. The given values are linear temperature coefficients, except where T^2 is used (in that case the quadratic temperature coefficient is indicated).

where T is the absolute temperature, T_R is the reference temperature (room temperature for instance) in °K, V_{G0} is the linearly extrapolated bandgap at 0°K, and I_{poR} is the saturation current at the reference temperature.

As the dope level of the p-n-p base is quite low, the bandgap narrowing can be neglected and V_{G0} equals 1.206 V [8].

For the n-p-n transistor the same temperature correction holds, except for a small bandgap narrowing which yields V_{G0} = 1.16 V for an average base dope level of $10^{18}\,cm^{-3}$ [8].

The saturation current of the Schottky diode is given by $I_{do} = AA^*T^2\exp(-q\phi_B/(kT))$ [9], where A is the diode area, A^* the Richardson constant and ϕ_B the Schottky barrier height. The current through the Schottky diode equals $i = I_{do}[\exp(\frac{qV}{nkT}) - 1]$, where n is the non-ideality factor. For practical devices $1 < n < 1.05$. From measurements it is found that the barrier height ϕ_B has to be extrapolated linearly to ϕ_{B0} at 0°K as is done to find V_{G0} [8].

When this is done, the saturation current for the Schottky diode becomes:

$$I_{doT} = I_{doR}\left(\frac{T}{T_R}\right)^2 \exp\left[\frac{q\phi_{B0}}{k}\left(\frac{1}{T_R} - \frac{1}{T}\right)\right]. \qquad (2)$$

To make an appropriate measurement of ϕ_{B0} which is as accurate as possible over the temperature range to be modeled, first I_{doR} is measured at the lowest temperature (at T_R = 25°C for instance). Then I_{doT} is measured at the highest temperature (125°C for instance), and with (2) ϕ_{B0} is found. Following this measuring method the PtNi silicide diodes have ϕ_{B0} = 0.80 eV, where ϕ_B at 25°C is about 0.78 eV.

If, as a first-order approximation, the non-ideality factors of the Schottky diode and the p-n-p are taken unity, the temperature coefficient of the ISL voltage swing is calculated as follows. The voltage swing at temperature T is: $\Delta V(T) = (kT/q)\ln\alpha_p^* I_{doT}/I_{poT}$ [5].

Substituting (1) and (2) it is found that

$$\Delta V(T) = \Delta V_R + \frac{kT}{q}\ln\left(\frac{T}{T_R}\right)^{0.2} + \left(1 - \frac{T}{T_R}\right)(V_{G0} - \phi_{B0}),$$

where ΔV_R is the voltage swing at the reference temperature.
Differentiation of the last equation yields

$$\left.\frac{d(\Delta V)}{dT}\right|_{T_R} = \frac{\Delta V_R + \phi_{B0} - V_{G0} + 0.2\,kT_R/q}{T_R}. \qquad (3)$$

When ΔV_R = 220 mV, then the temperature coefficient is − 0.6 mV/°C at room temperature.

B. Transit times of transistors and diodes

The transit times of the transistors and diodes are modeled as

$$\tau_T = \tau_R\left(\frac{T}{T_R}\right)^{1.6},$$

where τ_R is the transit time at the reference temperature. No split-up is made for the different devices, and a mean exponent of 1.6 is used to model the transit time increase caused by the decrease of minority carrier mobility with increasing temperature.

C. Depletion capacitance and built-in diffusion voltages

In most simulation programs the expression for the depletion capacitance C has the zero bias depletion capacitance, the built-in voltage and the grading coefficient as parameters. For a one-side abrupt junction C_o can be approximated as

$$C_o = A\sqrt{q\epsilon_s N_B/(2V_{bi})}, \qquad (4)$$

where A is the area of the junction, N_B is the concentration at the low doped side, and V_{bi} is the built-in diffusion voltage. The voltage V_{bi} decreases with the temperature, and accordingly C_o and C will change with the temperature.
V_{bi} is given by

$$V_{bi} = \frac{kT}{q} \ln \left[\frac{N_A N_D}{n_i^2}\right],$$

where n_i^2 is given by

$$n_i^2 = c_1 T^3 \exp\left[\frac{-q(V_{G0} - \alpha T)}{kT}\right] = c_2 T^3 \exp\left[\frac{-qV_{G0}}{kT}\right],$$

where V_{G0} is the extrapolated bandgap, and α the temperature coefficient of V_G; c_1 and c_2 are constants. Differentiation of the expression of V_{bi} delivers

$$\left.\frac{dV_{bi}}{dT}\right|_{T_R} = \frac{V_{biR} - V_{G0} - 3kT_R/q}{T_R}, \tag{5}$$

where V_{biR} is the built-in voltage at the reference temperature. With V_{G0} being 1.206 V, this temperature coefficient at room temperature equals

$$\left.\frac{dV_{bi}}{dT}\right|_{300°K} = (-43.10^{-4} + 33.10^{-4} V_{bi\ 300°K})\ VK^{-1}. \tag{6}$$

Expression (4) was also found in [10].
When (4) is substituted in (3) the relative temperature coefficient of C_o is found:

$$\frac{1}{C_o}\frac{dC_o}{dT} = -\frac{1}{2V_{bi}}\frac{dV_{bi}}{dT} K^{-1}. \tag{7}$$

For low-doped junctions where V_{bi} is about 0.75 V this temperature coefficient is about $12.10^{-4} K^{-1}$, which means that for a temperature increase of 100°C, the capacitances increase by 12%.

For non-abrupt junctions equations (6) and (7) no longer hold. The temperature coefficient of V_{bi} will then be somewhat larger. But as the capacitance is less dependent on V_{bi} in that case [10], the temperature coefficient of C_o will be marginally lower than given by (7), which means that (7) is a realistic first-order approach to the temperature coefficient for all types of junctions.

In the used model for the ISL gate, temperature coefficients are introduced for V_{bi} and C_o of all junctions capacitances except for the built-in voltage and junction capacitance of the Schottky diode, because this last small capacitance plays only a minor

role [5].

D. Current gains of the transistors

The relative temperature coefficients of the current gains are of the same order as the relative temperature coefficients of depletion capacitances and resistances. Measured values are used for the n-p-n transistor ($56.10^{-4}K^{-1}$ for the forward β and $27.10^{-4}K^{-1}$ for the reverse β). No measured values were available for p-n-p's. From theoretical considerations the temperature coefficients must be less, but still positive [11]. As a first-order approximation $2.10^{-3}K^{-1}$ has been used.

E. Resistances

All resistances increase with temperature and can be described by

$$R_T = R_R\,[1 + \gamma(T - T_R) + \eta(T - T_R)^2]\,,$$

where R_R is the resistance at the reference temperature T_R, and γ and η are the linear and quadratic temperature coefficients respectively. In general the higher the resistivity the higher the linear temperature coefficient is.

All γ's and η's are measured and included in the model. Quadratic temperature coefficients are indicated only where they are relevant.

10. VII. Measurements, analytical calculations and simulations

Fig. 9 shows the measured and simulated average propagation delay times (obtained with a 21-stage ring oscillator) of the oxide-isolated ISL discussed in this paper. The simulations both at 25°C and 125°C are in good agreement with the measurements. Analytical calculations can only be done neglecting series resistances [5]. Two values are calculated at room temperature at 50 μA/gate and at 100 μA/gate. Fig. 9 also gives simulated results at 25°C when all series resistances are neglected.

It is obvious that at low current levels the series resistances do not affect the propagation delay time; also the measured results coincide with the analytical calculation. In this region only the depletion capacitances and logic swing determine the propagation delay time. Despite the increase of the depletion capacitances with increase of temperature, (about 10% with 100°C increase), the propagation delay time decreases with temperature due to the dominating decrease of the logic swing (about 25% with 100°C increase); see equations (7) and (3). At high current levels series resistances affect the propagation delay time seriously. When all series resistances were zero, then the theoretical minimum value of $\tau_p^*/2$ (being 125 ps at room temperature) could be reached when the current level would be increased sufficiently (see dotted line in Fig. 9). Simulations learned that the speed degradation is mainly caused by the relatively high base-series-

-resistance of the n-p-n transistor ($R_{bN1} + R_{bN2}$). This total resistance value is 3 kΩ at room temperature and causes a propagation delay time increase of about 300 ps at 240 μA/gate.

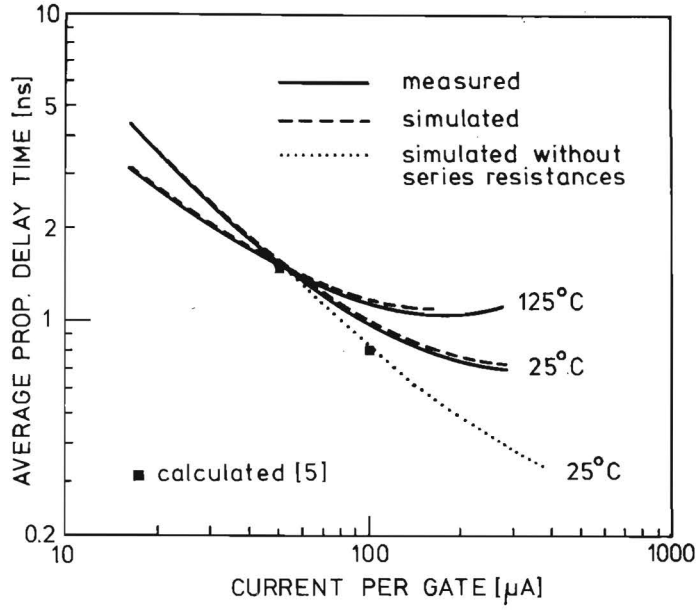

Fig. 9. Measured, simulated and calculated average propagation delay times of oxide-isolated ISL [3]. The calculated values are obtained without series resistances being taken into account [5]. The dotted line corresponds to simulations done with the model in which all series resistances are reduced to zero.

As both the series resitances and capacitances increase with increase of temperature, it turns out that the average propagation delay time is even more RC-time limited at high temperatures; this means that at high current levels the propagation delay times increase with temperature.

At 55 μA/gate the low and high current temperature effects compensate each other, resulting in a temperature independent propagation delay time of 1.3 ns.

10.VIII Conclusions

A 14-node model has been derived which models an oxide isolated p-n-p clamped ISL gate with fan-out = 4. The model includes an n-p-n transistor, a p-n-p transistor, a silicon diode and four Schottky diodes. Special attention is paid to all temperature coefficients of the device parameters. The extrapolated barrier height of the Schottky diode at 0°K is used as modeling parameter.

Very good agreement is obtained with measurements in the temperature range from 25°C to 125°C. The model is obtained for an ISL structure with a walled n-p-n emitter (two sides walled) and a single base conact. This walled emitter causes a relatively high n-p-n base series resistance and affects the speed at high current levels. Non-walled structures and/or the application of double base contact can therefore improve the speed at high current levels.

Due to the p^+ channel-stopper in the process, the collector series resistance of the clamp-p-n-p is relatively small, which means that low doped substrates can be used.

APPENDIX

It is impossible to measure the forward current gain of the p-n-p (β_{fP}) directly with the teststructure of Fig. 1, because when the collector contact of the n-p-n is used as base contact of the p-n-p, two devices are influencing the measurement: a) the parasitic p-n-p in the region where the buried layer is present (TP'), and b) the n-p-n transistor with floating emitter. The total schematic is shown in Fig. 10. It can be calculated that the effective current gain equals

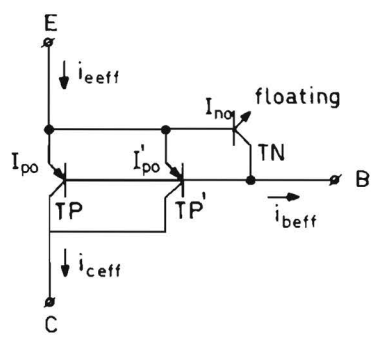

Fig. 10. Complete schematic of the structure of Fig. 4.

$$\beta_{fP\,eff} = \frac{1 + I_{po}'/I_{po}}{1/\beta_{fP} + I_{po}'/(\beta_{fP}' I_{po}) + I_{no}/[I_{po}(\beta_{fN} + 1)]} ,$$

where I_{po}' is calculated over the total region where the buried layer is present (I_{po}' per unit square is known [7]), and consequently i_{bTP}' represents the inverse base current of both the intrinsic and extrinsic base-collector region of the n-p-n.

With $\beta_{fP\,eff} = 40$, $I_{po} = 5.10^{-17}$, $I_{po}' = 16.10^{-20}$, $\beta_{fP}' = 2.4$ [7], $I_{no} = 10^{-17}$ and $\beta_{fN} = 70$, it follows that $\beta_{fP} = 48$.

As the collector current of the parasitic p-n-p is negligible compared with the collector current of the p-n-p, in the eventual ISL model only the base current of the parasitic p-n-p is modeled. This base current is equally devided over the diode and the base-collector junction of the n-p-n. This implies that the saturation current of the diode becomes $I_{ddo} = I_{po}'/(2\beta_{fP}') = 33.10^{-21}$ A and the inverse current gain of the n-p-n becomes $\beta_{rN} = 2\beta_{fP}'I_{no}/I_{po}' = 300$.

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11

Static and Dynamic Noise Margins of Logic Circuits

Abstract—The noise margins of logic circuits are often the subject of confusion. This paper intends to clear up the confusion by explaining four basic types of noise, and by showing the various methods, together with boundary conditions, which can be used to find the worst case noise margins. A flip-flop setup is advised which can be used for measurements and computer simulations, both for static and dynamic noise margins. Also configurations with fan-in and fan-out larger than 1 can be handled with this flip-flop method.

In general, it is found that the dynamic noise margins increase for shorter noise pulses; a first-order explanation of this phenomenon is given.

Also, energy noise margins are considered. It is shown that no characteristic energy can be determined which can disturb a logic circuit. Although energy minima can be found, their values as figures of merit are doubtful.

The theoretical considerations are completed with computer simulations and measurements of the static and dynamic noise margins of integrated Schottky logic (ISL), as an example. The obtained dynamic noise margins and energy noise margins of ISL agree very well with the first-order explanations given in this article.

11.I. Introduction

THE NOISE MARGINS of logic circuits are often the subject of confusion.

When referring to static noise margins, a type of noise is usually meant that is called series-voltage noise in this paper. However, also other types of noise exist, such as parallel-current noise and voltage noise in the power-supply and ground lines, which can exhibit totally different static margins than the series-voltage noise.

The worst case static series-voltage noise margin can be found graphically with the well-known "mirror-and-maximum-

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square method" [1] applied to the voltage transfer characteristic of a gate, but only if the input impedance of the gate is much larger than the output impedance. This boundary condition is frequently disregarded, leading to wrong conclusions (for the static noise margins of integrated injection logic, for instance).

This paper intends to clear up the confusion by explaining the four basic types of noise, and by showing the various methods, together with boundary conditions, which can be used to find the worst case static noise margins. For the cases where the mirror-and-maximum-square method cannot be used, a flip-flop setup is advised which can be used both for measurements and computer simulations. This setup can also be used for fan-in and fan-out larger than 1.

As the static noise margins are already the subject of confusion, the dynamic margins are even more unclearly defined. It

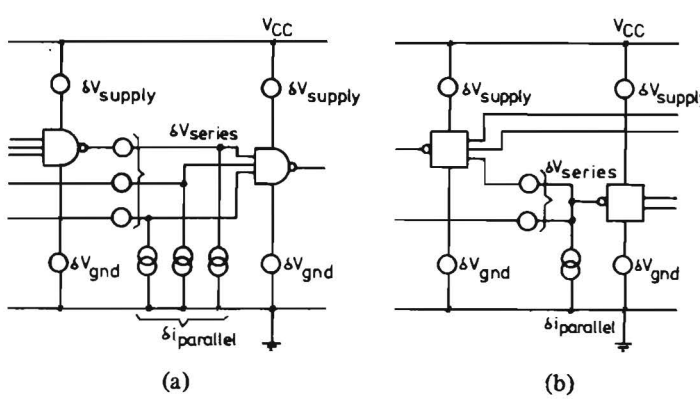


Fig. 1. Basic noise sources in NAND logic (a) and wired AND logic (b).

will be shown in this paper that the four basic noise sources can be considered as pulsing noise sources also. Viewed in this light, static noise is pulsed noise with an infinitely long pulse length. In general, it will be found that the dynamic noise margins are larger than the static ones: during short pulses, higher noise amplitudes may be applied. A first-order explanation of this phenomenon, considering *RC* time delays, will be given. The advised flip-flop method can also be used to find the worst case dynamic noise margins.

An interesting parameter would be "the" energy noise margin of a logic circuit. It will be shown that no specific energy noise margin can be defined because the energy required to deliver to, or withdraw from a circuit, depends heavily on the type of noise source and the length of the noise pulse.

The theoretical considerations will be completed with computer simulations and measurements of the static and dynamic noise margins of integrated Schottky logic (ISL) [2], [3] as an example.

11.II. Four Basic Noise Sources

In both NAND logic (TTL, ECL, NMOS, etc.) and wired AND logic (I^2L, ISL, STL, etc.), there are four basic noise sources: series-voltage noise in the interconnection lines between gates (δV_{series}), parallel-current noise to inputs or outputs of gates (δi), voltage noise at the ground line (δV_{gnd}), and voltage noise at the power-supply line (δV_{supply}). Fig. 1 shows these noise sources in both logic types for arbitrary fan-in and fan-out configurations. All these noise sources can be present at the same time with any amplitude and any sign. This means that the determination of the worst case noise pattern is a multidimensional problem that is almost impossible to solve. A better approach is to isolate δV_{series}, δV_{gnd}, δV_{supply}, or δi and to determine the worst case margin for each type of noise. After that cross relations or cross sensitivities may be examined.

It should be noted that each noise source either delivers power to the circuit or withdraws power from the circuit.

11.III. Worst Case Static Series-Voltage Noise Margin

Fig. 2 shows an infinitely long chain of identical inverters (of the wired AND type) with series-voltage noise $\delta_1 V$ and $\delta_2 V$ in all interconnections. This type of noise may be induced by inductive coupling to a current gradient di/dt. This case can be considered as quasi-static if the time interval in which the current gradient is present is long compared with the switching speed of the inverting gates.

The input voltage levels are indicated by H (high) and L (low). In the adverse situation, $\delta_1 V$ and $\delta_2 V$ have a different sign. The noise margin is defined as the maximum value of

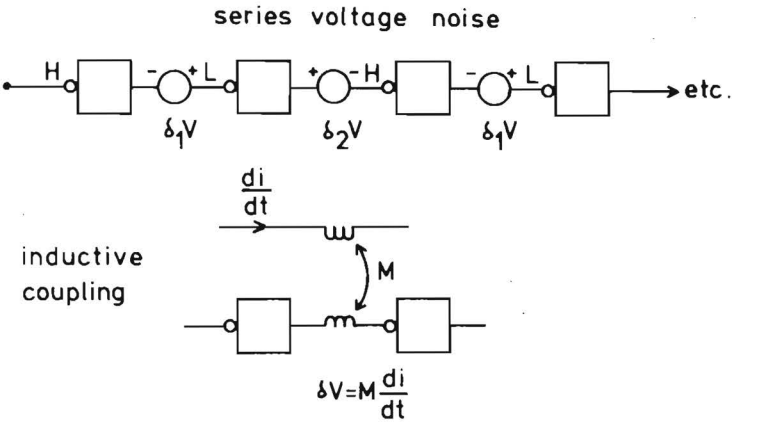


Fig. 2. Series-voltage noise in an infinitely long chain of identical inverters of the wired AND type. The logic voltage levels are indicated by H (high) and L (low). The noise sources have alternating signs in the adverse situation. For the worst case situation, the arbitrary choice $\delta_1 V = \delta_2 V = \delta V$ is made. The noise may be induced by inductive coupling to a current gradient di/dt. The maximum noise amplitude $\Delta V = \delta V_{max}$ for which gates at the end of the chain are on the edge of switching to the wrong state is defined as the worst case noise margin ΔV_{series}.

δV for which gates at the end of the chain are on the ultimate edge of switching to the wrong state [1].

As long as $\delta_1 V$ and $\delta_2 V$ can have different amplitudes, noise margins can be found for all different ratios $\delta_1 V/\delta_2 V$ from zero to infinity. In this paper, the worst case noise margin will be considered for the arbitrary ratio $(\delta_1 V/\delta_2 V) = 1$, which means that $\delta_1 V = \delta_2 V = \delta V$. The worst case static series-voltage noise margin is then defined as $\Delta V_{series} = \delta V_{max}$.

The value of ΔV_{series} can be found graphically with the mirror-and-maximum-square method [1] applied to the *voltage* transfer characteristic of the gate in the case where the gate output impedance is much lower than the gate input impedance ($R_{out} \ll R_{in}$). This impedance condition is required because the mirror-and-maximum-square method is based on the assumption that the input voltage at any stage is given by the summation of the output voltage of the preceding stage and the voltage of the noise signal.

For logic circuits such as ECL, TTL, and MOS, one has indeed $R_{out} \ll R_{in}$, which means that the mirror-and-maximum-square method can be applied to the voltage charac-

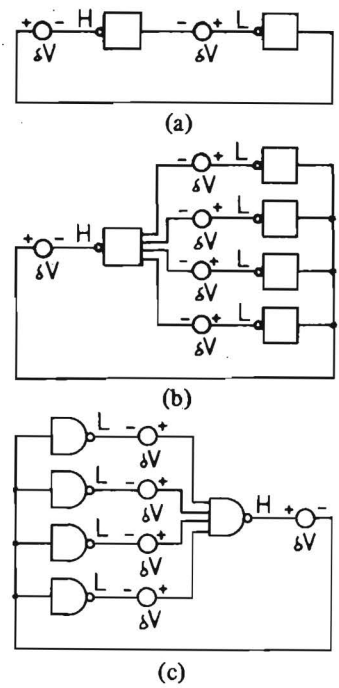


Fig. 3. Worst case series-voltage noise measurement/computer simulation setup for wired AND logic with fan-in = fan-out = 1 ($F = 1$) (a) and $F = 4$ (b), and for NAND logic with $F = 4$ (c). Feedback makes a flip-flop. The noise amplitude at which the flip-flop switches to the wrong state is equal to the noise margin in an infinitely long chain.

teristic. However, for I^2L, ISL, and STL, the impedance condition does not hold, which means that the application of this method to these logic circuits will give wrong values for ΔV_{series}.

In the case of logic circuits where R_{in} is not large compared with R_{out}, the easiest way to find ΔV_{series} is by a direct measurement or a computer simulation.

Depending on the shape of the voltage and current transfer characteristics of the gates, a certain minimum number of gates have to be taken in series for an accurate approximation of the infinitely long chain. As this minimum number is difficult to determine and as a very long chain is uneasy to handle, it is better to take two gates in series and make a feedback to form a flip-flop. This method was proposed earlier in [1] [see Fig. 3(a)]. The value of the ΔV_{series} is found to be $\delta V_{\max}$,

at which value the flip-flop is at the ultimate edge of switching to the wrong state and is exactly the same δV_{max} that would be found in an infinitely long chain. In fact, Fig. 3(a) represents a method that can be used to find ΔV_{series} for the case where fan-in = fan-out = 1 ($F = 1$). A more critical worst case situation will be found for fan-in = fan-out = 4 ($F = 4$). Fig. 3(b) shows how a similar measurement or computer simulation is set up for $F = 4$. This method is, of course, not restricted to wired AND logic but can also be applied to NAND logic, as illustrated in Fig. 3(c).

11.IV. Worst Case Static Parallel-Current Noise Margin

Fig. 4 shows an infinitely long chain of identical inverters with parallel-current noise $\delta_1 i$ and $\delta_2 i$ to all interconnection nodes. This type of noise may be introduced by capacitive coupling to a voltage gradient dV/dt. This case can be considered as quasi-static if the time interval in which the voltage gradient is present is long compared with the switching speed of the inverting gates.

Here, too, in the adverse situation $\delta_1 i$ and $\delta_2 i$ have a different sign, and since the worst case situation will arbitrarily be

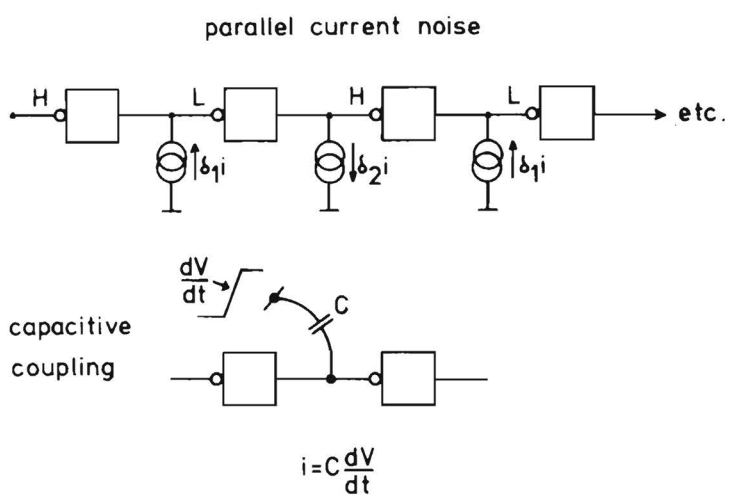


Fig. 4. Parallel-current noise in an infinitely long chain of identical inverters (wired AND logic). The noise may be introduced by capacitive coupling to a voltage gradient dV/dt.

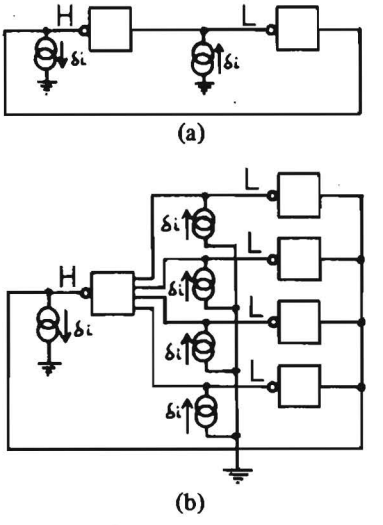


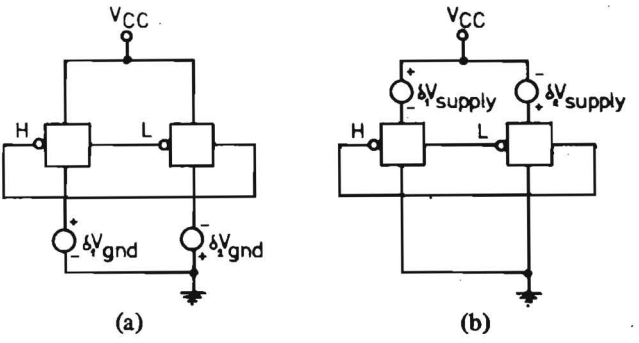
Fig. 5. Flip-flop setup to find the worst case parallel-current noise margin Δi, for $F = 1$ (a) and $F = 4$ (b). This example is made with wired AND logic.

chosen for $\delta_1 i = \delta_2 i = \delta_i$, the worst case static noise margin will be found for $\Delta i_{\text{parallel}} = \delta i_{\max}$. The value of $\Delta i_{\text{parallel}}$ can be found graphically with the mirror-and-maximum-square method applied to the *current* transfer characteristic in the case where $R_{\text{out}} >> R_{\text{in}}$.

This impedance condition holds for I^2L, for instance, and it has been shown [4] that this graphical method can be used to find $\Delta i_{\text{parallel}}$ for this type of logic. For other logic circuits where R_{out} is not large compared with R_{in}, the easiest way to find $\Delta i_{\text{parallel}}$ is by direct measurement or computer simulation with a flip-flop setup as illustrated in Fig. 5. Fig. 5(a) shows for wired AND logic the setup for $F = 1$, and Fig. 5(b) the setup for $F = 4$. Of course, a similar setup can be applied to NAND logic.

11.V. Worst Case Static Margins for Voltage Noise in Ground- and Power-Supply Lines

Voltage noise in the ground- and power-supply lines can be caused by ringing, spikes, voltage drops due to series resistances, etc. Fig. 6 shows the flip-flop setup with $F = 1$ for wired AND logic to determine the static noise margins. Of course, for $F = 4$, and also for NAND logic, setups similar to



(a) (b)

Fig. 6. Flip-flop setup to find ΔV_{gnd} (a) and ΔV_{supply} (b) for $F = 1$ wired AND logic. Of course, a setup similar to that in Fig. 3(b) and Fig. 3(c) can be given for $F = 4$.

those in Fig. 3 can be given. The worst case noise margins are given by $\Delta V_{gnd} = \delta V_{gnd\,max}$ and $\Delta V_{supply} = \delta V_{supply\,max}$, where $\delta_1 V_{gnd} = \delta_2 V_{gnd} = \delta V_{gnd}$ and $\delta_1 V_{supply} = \delta_2 V_{supply} = \delta V_{supply}$.

11.VI. Elucidation of the Influence of Static Noise in a Flip-Flop

To elucidate what happens if static noise is present in a flip-flop, an example of series-voltage noise and parallel-current noise will be given for gates with $R_{in} >> R_{out}$.

Fig. 7 shows such a flip-flop. The input and output impedances are modeled with the resistors R_{in} and R_{out}, respectively. Fig. 7(a) shows series-voltage noise and Fig. 7(b) shows parallel-current noise. Fig. 8(a) shows the voltage transfer characteristics of both gates in the case where no noise is present. There are two stable states A and C and one metastable state B. Assume that the flip-flop is in the stable state A. With noise present, the transfer characteristics will shift into the directions of the two arrows, as indicated in Fig. 8(a). The influences of $\delta_1 V$ and $\delta_1 i$, and $\delta_2 V$ and $\delta_2 i$, are taken into account in the output voltages of gate 1 and gate 2, respectively. Fig. 8(b) illustrates such shifts. As long as the transfer characteristics intersect at three points, the flip-flop will remain in the stable state A. Fig. 8(c) shows larger shifts induced by larger noise amplitudes. Here the characteristics intersect in point C only, which means that the flip-flop is switched over to the other state. The noise amplitudes for which the transfer characteristics just touch each other in

point A (then points B and A will come together) indicate the noise margin(s).

For voltage noise in the ground- and power-supply lines, similar explanations can be given.

Note that in the particular case of Fig. 7 the series-voltage noise sources deliver a very small amount of power to the circuit because of the high input impedance of the gates. For the parallel-current noise sources, it is quite different. Source $\delta_1 i$ delivers a large amount of power to the circuit, and the source $\delta_2 i$ withdraws a large amount of power from the circuit due to the low output impedance of the gates.

For gates where the condition $R_{in} >> R_{out}$ does not hold, the explanation and visualization of the influence of the noise is somewhat more difficult. However, the principle remains the same: as soon as the flip-flop is forced to a condition where the two stable states do not exist anymore, the flip-flop will switch over the other state.

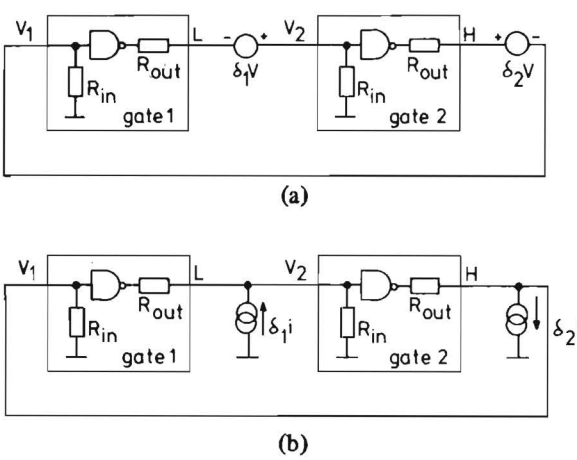
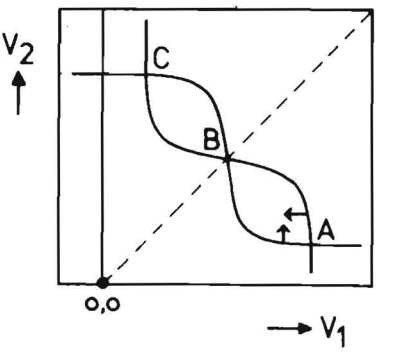
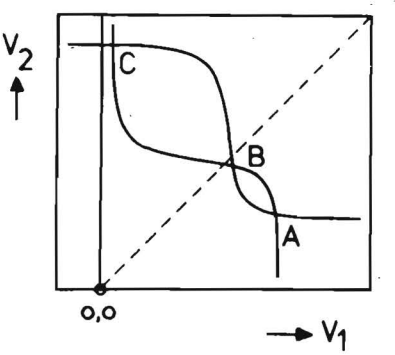


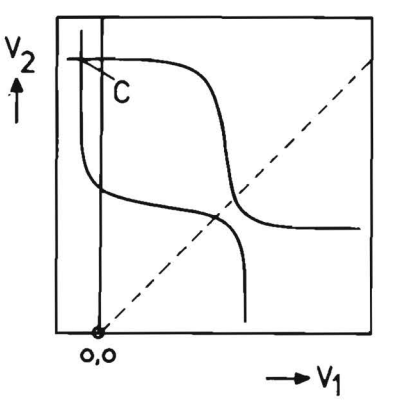
Fig. 7. Series-voltage noise (a) and parallel-current noise (b) in a flip-flop with gates for which $R_{in} >> R_{out}$. Both types of noise cause a shift of the output voltages of the gates.



(a)



(b)



(c)

Fig. 8. Voltage transfer characteristics of the gates from Fig. 7. Without noise (a) there is one metastable state *B* and there are two stable states *A* and *C*. The flip-flop is assumed to be in the stable state *A*. With noise present, the characteristics will shift [see arrows in (a)]. For small shifts stable state *A* will still exist (b). For large shifts, the characteristics do not touch in *A* anymore and the flip-flop is forced to switch to state *C* (c). A maximum sum of shifts can be determined to keep the flip-flop in state *A*.

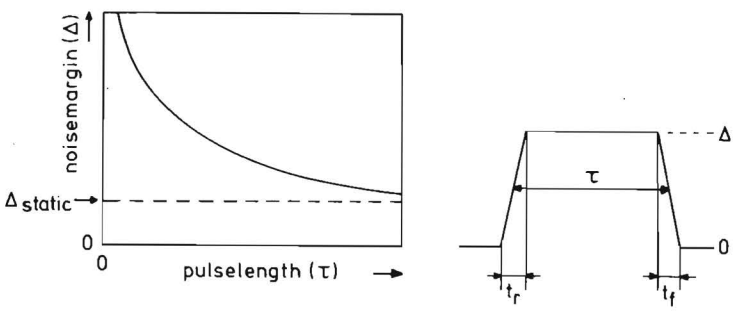


Fig. 9. General behavior of the dynamic noise margins: amplitudes of noise pulses are allowed to be higher for shorter pulsewidths. For very long noise pulses, the situation is quasi-static and the noise margins will reach their minima.

11.VII. Dynamic Noise Margins

The static noise margins indicate the maximum dc noise amplitudes that can be withstood by the logic. This means that the noise may be present during an infinitely long time without bringing gates to the wrong state.

It is very well known that if the noise is present in pulse-form, the noise amplitudes are allowed to be higher than the static margins without affecting the proper logic states. This brings us to the dynamic noise margins.

Fig. 9 shows the phenomenon. For very long noise pulses the situation is quasi-static and the margins are determined by static margins Δ_{static}. For short pulses the noise margins increase. The shapes of the various curves depend, of course, on the switching speed of the gates. For slow gates, the noise margins will increase more rapidly than for fast gates if the pulsewidths decrease.

The increasing margins for shorter pulses have primarily to do with internal *RC* time constants in the gates. The external applied pulses have to induce voltage shifts inside gates and, because of the *RC* time delays, larger amplitudes of the driving noise sources are allowed for shorter pulses. An example of this phenomenon will be given in Section VIII. Exact calculations of dynamic margins are very difficult. Measurements and/or computer simulations, using the flip-flop method, are much more easier to do.

11.VIII. Energy Noise Margins

Although the amplitudes and lengths of the noise pulses are the most important parameters, a boundary condition is that the noise sources can deliver or can sink enough energy to bring the circuit to the wrong logical state.

To obtain a first-order impression of the energy requirements, the same circuit as given in Fig. 7 will be considered. In this case, only noise at the output of gate 1 (which is LOW) will be present, and the gates are assumed to have a specific input capacitance C (see Fig. 10). As is shown in the previous section, the flip-flop will switch to the other state if the transfer characteristic of gate 1 is shifted enough upward. This has to be done by the noise source δV [see Fig. 10(a)].

For the static case the input capacitance of gate 2 plays no role. In the dynamic case, however, the input capacitance has to be charged by the noise source, which has to deliver a certain amount of energy. If the input impedance of gate 2 is neglected, then the time to charge the input capacitance is determined by the amplitude δV of the noise source and the

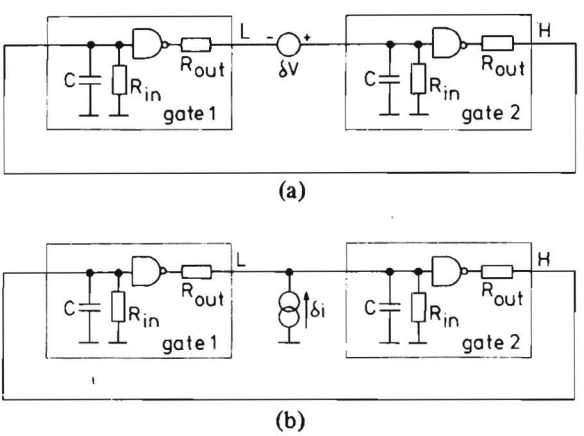


Fig. 10. Same circuits as given in Fig. 7, now considered for dynamic (pulsed) noise. The gates have an input capacitance C. Series-voltage noise (a) or parallel-current noise (b) is present at the output of gate 1.

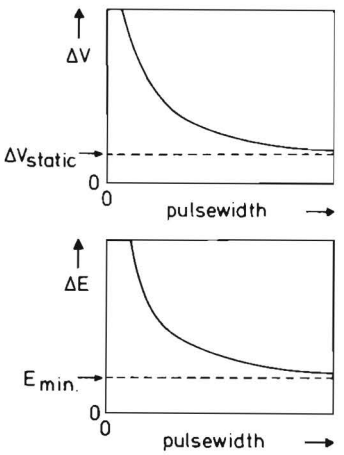


Fig. 11. Series-voltage noise margin and series-voltage noise energy margin of the circuit shown in Fig. 10(a) as a function of noise pulsewidth. The behavior is obtained from a simplified model. The energy margin increases for shorter pulses of the series-voltage noise.

output impedance of gate 1. The time needed to charge the input of gate 2 to a specific voltage will decrease for higher noise voltages. As for higher voltages, the energy efficiency decreases (see Appendix I), the noise source has to deliver more energy during the short pulses with high amplitude. Fig. 11 shows the phenomenon. In the (quasi) static case the required energy is minimal and is given by $E_{min} = C[(V_{in} + \Delta V)^2 - V_{in}^2]$, where V_{in} is the undisturbed input voltage of gate 2 and ΔV the static noise margin.

With parallel current noise [see Fig. 10(b)] the energy aspect is totally different. Here the energy efficiency increases for short pulses with high amplitude (see Appendix II). This means that long pulses with small amplitude require more energy than short pulses with high amplitude; this is also shown in Fig. 12. For infinitely short pulses, the required energy reaches half the value of E_{min} as for the series voltage case (see Appendix II).

For energy-sinking noise sources, similar explanations can be given as for the energy-delivering sources. Also the energy aspects of the noise in the ground- and power-supply lines can be treated in the same way.

It should be stated that this introduced energy explanation is a simplified one because the intrinsic propagation delay times of the gates have been neglected. In fact, an extra

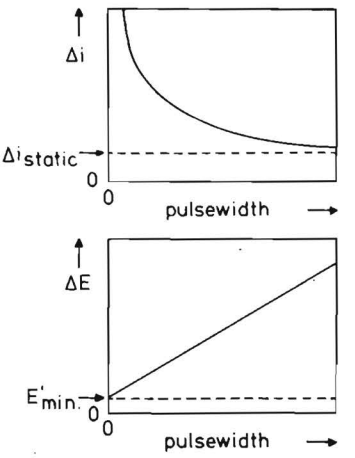


Fig. 12. Parallel-current noise margin and parallel-current noise energy margin of the circuit shown in Fig. 10(b), as a function of noise pulsewidth. The behavior is obtained from a simplified model. For this type of noise the energy margin decreases for shorter pulses of the parallel-current noise.

boundary condition has to be fulfilled which says that the voltage change at the input of gate 2 must be induced long enough to overcome the feedforward delay in the flip-flop. This problem is very complicated and needs more detailed study. The basic message of the simplified explanation is that there will be a great difference concerning the energy margins of the various noise sources.

11.IX. Measured and Computer-Simulated Noise Margins of ISL

Integrated Schottky logic (ISL) is a wired AND logic that can be made in a standard Schottky process [2]. The basic circuit diagram is shown in Fig. 13. The saturation currents of the transistors and Schottky diodes are indicated by I_{n0}, I_{p0}, and I_{d0}. The current source can be either a non-saturated p-n-p transistor or a resistor. Measurements and computer simulations were carried out for series-voltage noise, parallel-current noise, and ground-line voltage noise. No separate measurements and simulations were made for power-supply noise, because the margins for this type of noise can be directly calculated from the parallel current-source margins. This is due to the fact that the power-supply noise only modulates the amplitude of the current source of ISL.

A. Static Noise Margins

Fig. 14 shows the logic swing and the worst case static noise margins of ISL as a function of I_{d0}/I_{p0}, derived with computer simulations. Four cases are shown: $F = 1$ and $F = 4$, both for $\beta_{n\text{-}p\text{-}n} = 20$ and $\beta_{n\text{-}p\text{-}n} = 100$. The simulation setups given in Figs. 3(a), 3(b), 5(a), and 6(a) were used. In all cases, $\alpha_{p\text{-}n\text{-}p} = 0.9$ and the temperature is room temperature. The logic swing equals roughly (kT/q) ln $(\alpha_{p\text{-}n\text{-}p}\ I_{d0}/I_{p0})$, independent of the current per gate [3].

With $F = 4$, the flip-flop is only stable in the case of a voltage swing greater than 100 mV; whereas, with $F = 1$, 35 mV or 45 mV is required for $\beta = 20$ and $\beta = 100$, respectively. For these minimum voltage swings, all noise margins are zero. The worst case series-voltage noise margins ΔV_{series} increase linearly with the voltage swing, whereas the worst case ground-line noise margins ΔV_{gnd} increase linearly with

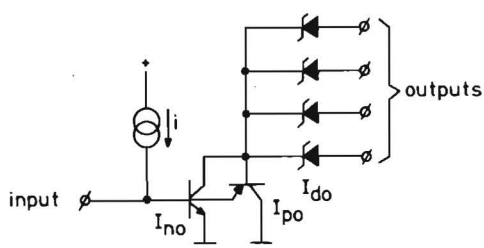


Fig. 13. Basic circuit diagram of an ISL gate [2]. The saturation currents of the transistors and Schottky diodes are indicated by I_{n0}, I_{p0}, and I_{d0}. The current source can be either a nonsaturated p-n-p transistor or a resistor.

the half voltage swing. The difference is caused by the fact that the series-voltage noise source, which is placed in series with the input of the gate that has the input in the HIGH state, is ineffective, because of the very high output impedance of the gate, which is OFF. The ground-line voltage noise sources are effective in both the gates, which means that $\Delta V_{gnd} = \frac{1}{2}\Delta V_{series}$. Similar behavior will be found in SI^2L, I^2L, and STL [3].

The worst case parallel-current noise margins Δi have been normalized to the current i per gate. The values of $\Delta i/i$ increase with increasing $\beta_{n\text{-}p\text{-}n}$. For very large values of I_{d0}/I_{p0}, $\Delta i/i$ increases to $(\beta_{n\text{-}p\text{-}n} - F)/(\beta_{n\text{-}p\text{-}n} + F)$.

Measurements are indicated by the heavy black points in Fig. 14. They fully agree with the computer simulations. The experiments are very easy to carry out; the noise amplitude at which the flip-flop switches to the wrong state is found to be sharply determined. To be sure that the measured margins are really the static margins, it is necessary to stabilize the flip-flop with an extra capacitor (for instance, between the two base

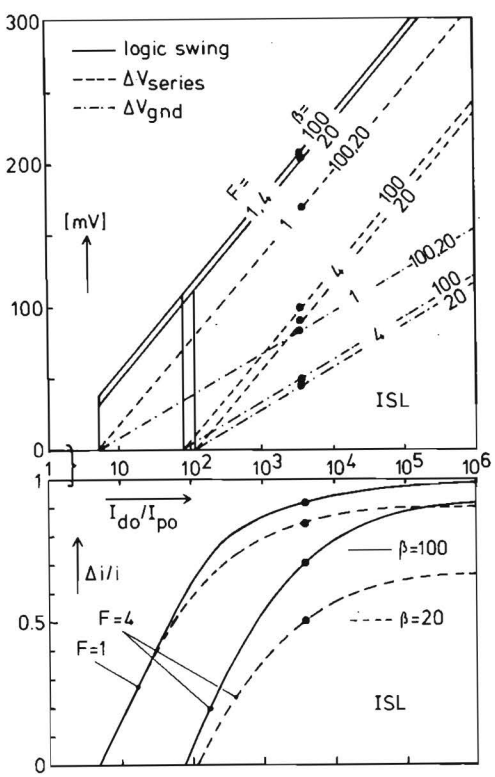


Fig. 14. Logic swing and the worst case static noise margins ΔV_{series}, ΔV_{gnd}, and $\Delta i/i$ for ISL as a function of I_{d0}/I_{p0}, with $\alpha_{p\text{-}n\text{-}p} = 0.9$ for two values of F (1 and 4) and two values of $\beta = \beta_{n\text{-}p\text{-}n}$ (20 and 100). Measurements (heavy black dots) were done for $I_{d0}/I_{p0} = 4.10^3$. No series resistances are taken into account.

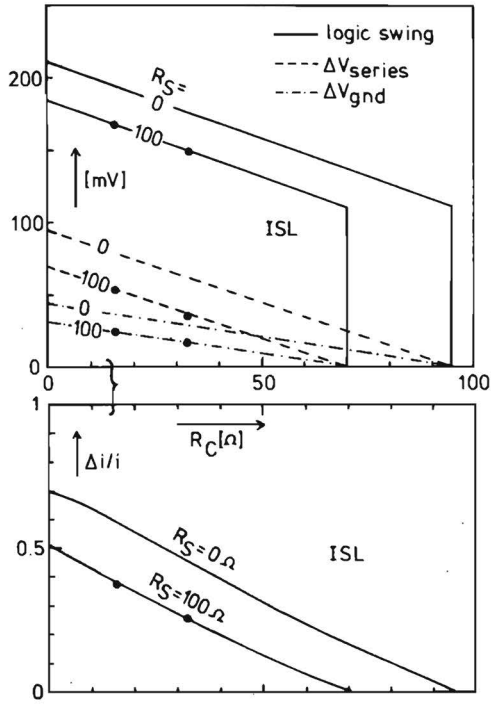


Fig. 15. Logic swing and the worst case static noise margins ΔV_{series}, ΔV_{gnd}, and $\Delta i/i$ for ISL as a function of R_C (n-p-n collector series resistance) with R_S (Schottky diode series resistance) as a parameter, at a current level of 250 μA/gate, with $\beta_{n\text{-}p\text{-}n} = 100$, $\alpha_{p\text{-}n\text{-}p} = 0.9$, and $I_{d0}/I_{p0} = 4.10^3$. Measurements were done for $R_C = 16\ \Omega$ and 32 Ω, with $R_S = 100\ \Omega$.

nodes) to prevent any ac noise from switching the flip-flop. The noise amplitudes then have to be increased very slowly in order to remain (quasi) static.

The noise margins presented in Fig. 14 are independent of the current, and, although worst case, are still optimistic as long as no series resistances are taken into account. By way of example, Fig. 15 shows how series resistances (n-p-n collector series resistance R_C and Schottky diode series resistance R_S) affect both voltage swing and noise margins. In this particular case, $I_{d0}/I_{p0} = 4.10^3$, $\beta_{n\text{-}p\text{-}n} = 100$, $\alpha_{p\text{-}n\text{-}p} = 0.9$, $i = 250\ \mu$A, and $F = 4$. In the case where $R_S = 100\ \Omega$, all noise margins will be zero for $R_C = 70\ \Omega$.

B. Dynamic Noise Margins

By way of example, some computer-simulated dynamic noise margins of ISL will be shown. The most relevant parameters used for the ISL model are as follows. For the n-p-n transistor, $f_T = 1600$ MHz, $\beta_n = 80$; $C_{be} = 0.14$ pF, $C_{bc} = 0.23$ pF: for the p-n-p transistor, $f_T = 16$ MHz, $\alpha = 0.95$; $C_{bc} = 0.6$ pF. The Schottky diode has a series resistance of 43 Ω. The $f_{T_{p\text{-}n\text{-}p}}$ is the most important parameter; with $f_{T_{p\text{-}n\text{-}p}} = 16$ MHz, the ISL-gate turnoff time is about 9 ns, and the average propagation delay time is 4.5 ns [5].

Fig. 16 shows four noise sources (parallel-current noise and ground-line voltage noise) that are investigated for the dynamic noise margins. The noise sources are not applied simultaneously, so non-worst case situations are studied. A current level of 250 μA/gate has been taken for the computer simulations.

Fig. 17(a) shows the simulated noise margins $\Delta_1 i$, $\Delta_2 i$, $\Delta_1 V$, and $\Delta_2 V$ of the four noise sources of Fig. 12 as a function of

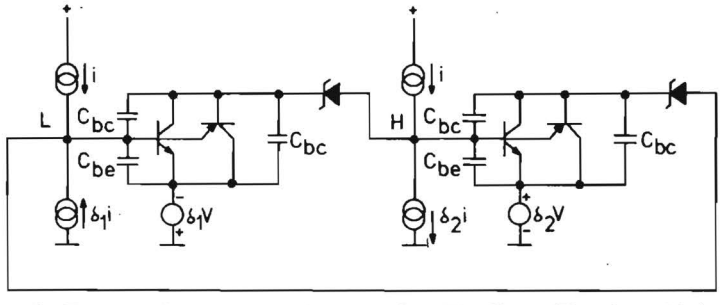


Fig. 16. Four noise sources in an ISL flip-flop ($F = 1$), which are investigated for the dynamic noise margins. The noise sources are not applied simultaneously.

the noise pulsewidth. The general behavior is as expected: for shorter pulsewidths the noise margins increase. The margins $\Delta_1 V$ and $\Delta_2 V$ follow exactly the same curve and have an asymptote at 9 ns. This means that the noise has to be present during the total turnoff time of gate 2. The margins $\Delta_1 i$ and $\Delta_2 i$ do not exhibit an asymptote at 9 ns. This is caused by the fact that the presence of the parallel-current noise decreases the switch OFF time of gate 2. In the case of

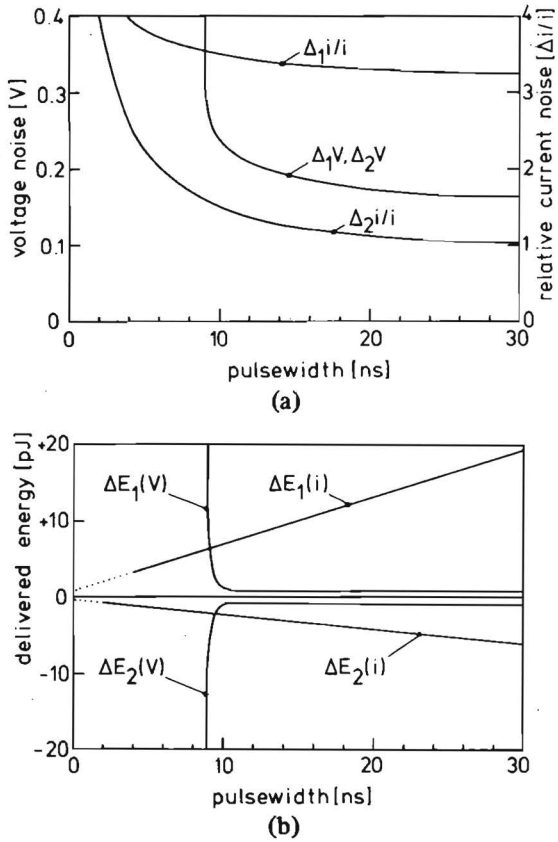


Fig. 17. Computer-simulated dynamic noise margins (a) and dynamic energy noise margins (b) of a typical ISL gate for parallel-current noise and ground-line voltage noise. The flip-flop setup shown in Fig. 16 is used. The margins are non-worst case.

$\Delta_1 i$, the n-p-n collector current of gate 2 is increased, which decreases the turnoff time of this gate [5], [6]. In the case of $\Delta_2 i$, a similar effect is present; with a large current noise at the input of gate 2, the base-emitter voltage of the n-p-n of gate 1 is decreased rapidly, causing an incidentally increased discharge current $(C_{be} + C_{bc})\,(dC_{be}/dt)$ for gate 2 [6].

Fig. 17(b) shows the delivered (positive) or sunken (negative) energy during the applied pulses of Fig. 17(a). The behavior of the curves resembles very much the energy noise margins shown in the Figs. 11 and 12, which were obtained from the simplified model. The energy margins for current

noise decrease for shorter pulses; the energy margins for the voltage noise increase for shorter pulses. The energy minima can be found between 0.5 and 1 pJ.

As the actual energy margins depend heavily on the type of noise source, noise amplitude and noise pulse length, the meaning of the energy minima as figures of merit is doubtful.

For worst case dynamic margins, $\delta_1 i$ and $\delta_2 i$ or $\delta_1 V$ and $\delta_2 V$ have to be applied simultaneously, with the same amplitude, of course. The results will be different from the results shown in Fig. 17.

11.X. Conclusions

It has been shown that four basic types of noise can be considered in logic circuits: series-voltage noise, parallel-current noise, and voltage noise in the ground- and power-supply lines. The noise can be present both in the static and dynamic mode, leading to different noise margins. Further different margins will exist for the various fan-in and fan-out configurations.

It has been shown that the well-known mirror-and-maximum-square method to find the static worst case series-voltage margin or the static worst case parallel-current margin can only be used in some limited cases where fan-in = fan-out = 1 and where the right boundary conditions are fulfilled concerning the input and output impedances of the logic gates. For all other cases, including dynamic noise, a flip-flop method is advised, which can be used both for measurements and computer simulations.

In general, it is found that the dynamic noise margins increase for shorter noise pulses. A first-order explanation of this phenomenon is given; more detailed study is needed.

Although the amplitudes and lengths of the noise pulses are the most important parameters, a boundary condition is that the noise sources can deliver or can sink enough energy to bring the logic circuit to the wrong state. This leads to the introduction of energy noise margin.

It is not possible to find a characteristic energy to disturb a logic circuit due to the fact that the energy efficiency of the various noise sources is quite different. Although energy minima can be found, the actual amount of energy depends on

the type of noise source, noise amplitude, noise pulse length, and input and output impedances of the logic gate. Therefore, the values of the minimal energy noise margins as figures of merit are doubtful.

The theoretical considerations are completed with computer simulations and measurements of the static and dynamic noise margins of integrated Schottky logic (ISL) as an example. The obtained dynamic noise margins and energy noise margins agree very well with the first-order explanations given in this article.

Appendix I
Charging a Capacitor with a Pulsed Voltage Source and a Series Resistor

Fig. 18 shows the electrical diagram of a capacitor C that is charged by a pulsed voltage source δV via a series resistance R. For $t < 0$ the voltage over the capacitor V_C is zero, and the amplitude of the voltage source is zero. At $t = 0$ the voltage source has the amplitude δV. The current through the voltage

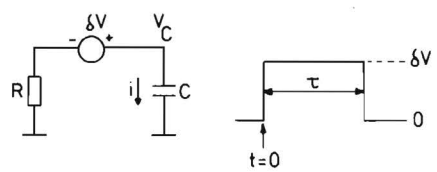


Fig. 18. Charging a capacitor with a pulsed voltage source and a series resistor.

source is given by

$$i = \frac{\delta V}{R} \exp(-t/RC) \tag{1}$$

and the voltage over the capacitor equals

$$V_C = \delta V[1 - \exp(-t/RC)]. \tag{2}$$

The time τ, to reach a voltage ΔV across the capacitor is given by

$$\tau = RC \ln [\delta V/(\delta V - \Delta V)] \tag{3}$$

where, of course, $\delta V \geqslant \Delta V$.

The value of τ indicates the minimum pulsewidth of the noise source. The energy delivered by the voltage source is given by

$$E = \delta V \int_0^{\tau} i\,dt = C \cdot \delta V \cdot \Delta V \tag{4}$$

where $\delta V \geqslant \Delta V$.

This means that the minimum energy equals

$$E_{\min} = C(\Delta V)^2 \tag{5}$$

and that the energy increases for $\delta V > \Delta V$, despite the fact that τ decreases.

In other words, the energy efficiency decreases for shorter pulses with higher amplitude.

Appendix II
Charging a Resistor-Shunted Capacitor with a Pulsed Current Source

Fig. 19 shows the electrical diagram of a capacitor C that is shunted by a resistor R. The capacitor is charged by the current course δi. For $t < 0$ the voltage over the capacitor V_C is zero, and the amplitude of the current source is zero. At $t = 0$ the current source has the amplitude δi. The voltage across the capacitor is given by

$$V_C = \delta iR\,[1 - \exp(-t/RC)]\,. \tag{6}$$

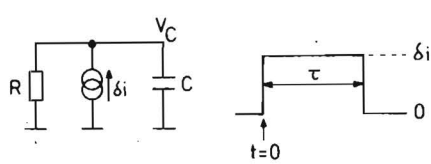


Fig. 19. Charging a resistor-shunted capacitor with a pulsed current source.

The time τ to reach a voltage ΔV over the capacitor equals

$$\tau = RC \ln\,[\delta iR/(\delta iR - \Delta V)] \tag{7}$$

where, of course, $\delta iR \geqslant \Delta V$.

The energy delivered by the current source equals

$$E = i\int_0^{\tau} V_C\,dt = C(\delta iR)^2\,[-\ln(1 - \Delta V/\delta iR) - \Delta V/\delta iR]. \tag{8}$$

Series expansion of the ln function delivers

$$E = \frac{1}{2}C(\Delta V)^2 + \frac{1}{3}C\frac{(\Delta V)^3}{\delta iR} + \frac{1}{4}C\frac{(\Delta V)^4}{(\delta iR)^2} + \frac{1}{5}C\frac{(\Delta V)^5}{(\delta iR)^3} + \cdots \tag{9}$$

where $\delta iR \geqslant \Delta V$.

This means that a minimum energy value of $\frac{1}{2}C(\Delta V)^2$ will be reached for an infinitely high value of δi. The energy increases for smaller values of δi. In other words, the energy efficiency increases for shorter pulses with higher amplitude.

Acknowledgment

The author wishes to thank J. v. d. Crommenacker and R. Hamberg for their help with the computer simulations.

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12

Calculation Method to Obtain Worst-Case Static Noise Margins of Logic Circuits

Indexing terms: Logic, Noise

A relatively simple calculation method is introduced using the flip-flop method, and by using the criterion that, with marginal static noise applied to the flip-flop, the loopgain is 1. As an example, the worst-case static series voltage noise margin of I^2L is calculated.

To determine the worst-case noise margins of logic circuits, a flip-flop method can be used for measurements and computer simulations.[1,2]

It has been stated[2] that analytical calculations of the static noise margins would be very difficult, specifically for those cases where bipolar transistors are in saturation. In this letter, however, a relatively simple calculation method is introduced by using the criterion that, with marginal static noise applied to the flip-flop, both small-signal voltage and current loopgains are equal to 1.

A flip-flop will remain in one of its two stable states if the loopgain in such a stable state is smaller than 1, whereas the loopgain in the metastable state is larger than 1.[3] With marginal noise applied to the flip-flop, one of the stable states coincides with the metastable state (see Fig. 8 in Reference 1) which means that the loopgain (for voltage, current and power) is equal to 1.

As an example of the calculation method, the worst-case static series voltage noise margin of I^2L is calculated for the case that fan-in = fan-out = 1. It will be shown that, by assuming that the loopgain is 1, a loopgain calculation is avoided (which might be very difficult in cases where transistors are in saturation and/or in cases where it is cumbersome to find a convenient point to 'break' the loop, which has to be done at a low-output/high-input impedance interface).

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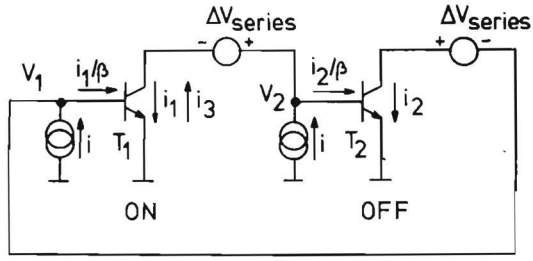

Fig. 1 *Flip-flop arrangement to determine worst-case static noise margin* ΔV_{series} *of* I^2L *for the case that fan-in = fan-out = 1. Noise margin is defined as the value of* ΔV_{series} *for which the flip-flop is at the ultimate edge before switching to the other state*

Fig. 1 shows the flip-flop arrangement[1,2] to determine the worst-case static series voltage noise margin of I^2L, for the case that fan-in = fan-out = 1. For both transistors, it is assumed that $\beta_{up\,eff} = \beta$, and $\beta_{down} = \infty$.

Transistor T_1 is on and T_2 is off; the noise sources try to bring the flip-flop into the other state. The collector current of T_1 is given by

$$i_c(T_1) = I_0\{\exp(qV_{BE}/kT) - \exp(qV_{BC}/kT)\} = i_1 - i_3$$

and the collector current of T_2 by $i_c(T_2) = i_2 - i_4$, where I_0 is the saturation current. The base currents of transistor T_1 and T_2 are i_1/β and i_2/β, respectively.

The Kirchhoff current law yields

$$i_1 - i_3 + \frac{i_2}{\beta} = i \tag{1}$$

and

$$i_2 - i_4 + \frac{i_1}{\beta} = i \tag{2}$$

The Kirchhoff voltage law gives

$$V_{BC}(T_1) + \Delta V_{series} + V_{BC}(T_2) - \Delta V_{series} = 0$$

which means that

$$\frac{kT}{q} \ln \frac{i_3}{I_0} + \frac{kT}{q} \ln \frac{i_4}{I_0} = 0$$

resulting in

$$i_3 i_4 = I_0^2 \tag{3}$$

The fourth equation required to solve for i_1, i_2, i_3 and i_4 is given by the criterion that both the small-signal current and voltage loopgains are equal to 1. This means that

$$\delta i_1 - \delta i_3 + \frac{\delta i_2}{\beta} = 0 \tag{4}$$

and,

$$\delta i_2 - \delta i_4 + \frac{\delta i_1}{\beta} = 0 \tag{5}$$

where

$$\delta i_1 = \frac{q i_1}{kT}\,\delta V_1 \qquad \delta i_2 = \frac{q i_2}{kT}\,\delta V_2$$

$$\delta i_3 = \frac{q i_3}{kT}\,(\delta V_1 - \delta V_2) \qquad \delta i_4 = \frac{q i_4}{kT}\,(\delta V_2 - \delta V_1)$$

Combining eqns. 4 and 5 gives

$$i_1 i_2 \left(1 - \frac{1}{\beta^2}\right) - i_2 \left(i_3 + \frac{i_4}{\beta}\right) - i_1 \left(i_4 + \frac{i_3}{\beta}\right) = 0 \tag{6}$$

With eqns. 1, 2, 3 and 6, i_1, i_2, i_3 and i_4 can be solved; the worst-case noise margin will then be given by

$$V_{CE}(\mathrm{T}_1) + \Delta V_{series} - V_{BE}(\mathrm{T}_2) = 0$$

which yields

$$\Delta V_{series} = \frac{kT}{q} \ln \frac{i_2 i_3}{i_1 I_0} \tag{7}$$

Combining eqns. 1, 2 and 6 gives

$$i_3 + i_4 = \sqrt{(\beta+1)}\sqrt{\left\{\left(\frac{3}{\beta}-1\right)I_0^2 + \left(\frac{\beta-1}{\beta}\right)^2 i^2\right\}} - \left(\frac{\beta-1}{\beta}\right)i \tag{8}$$

With $\beta = 1$, eqn. 8, together with eqn. 3, yields $i_3 = i_4 = I_0$, and further with eqns. 1 and 2 it can be shown that $i_1 = i_2$. This means that, with eqn. 7 it is found that $\Delta V_{series} = 0$ for $\beta = 1$ (as expected).

For $(\beta - 1) \gg I_0/i$, eqn. 8 reduces to

$$i_3 = \frac{\beta-1}{\beta}(\sqrt{(\beta+1)} - 1)i \tag{9}$$

and

$$i_4 \approx 0 \tag{10}$$

Combining eqns. 1, 2, 9 and 10 gives

$$i_1 = \beta\sqrt{\left(\frac{1}{\beta+1}\right)}i \qquad i_2 = \left[1 - \sqrt{\left(\frac{1}{\beta+1}\right)}\right]i \tag{11}$$

So, with eqn. 7, the worst-case noise margin is found to be

$$\Delta V_{series} = \frac{\kappa T}{q}\ln\frac{i}{I_0} - \frac{kT}{q}\ln\frac{\beta^2}{(\beta-1)(\beta+2-2\sqrt{(\beta+1)})} \tag{12}$$

for $\beta - 1 \gg I_0/i$.

As, for normal transistors, $I_0/i < 10^{-8}$, eqn. 12 will be valid for $\beta - 1 > 10^{-6}$.

Note that ΔV_{series} is much larger than the value of $(kT/q)\ln\beta$, quoted in most of the I^2L literature (see Reference 4, for instance). Fig. 2 shows a graphical representation of eqn. 12. The theoretical curve is confirmed by computer simulations and also by measurements.[2] The presented calculation method can also be used in cases where fan-in = fan-out > 1, and also for other types of noise.[1]

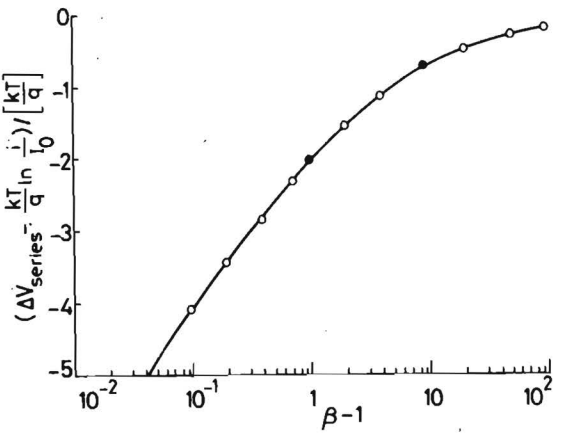

Fig. 2 *Calculated, computer-simulated and measured values of the worst-case static series voltage noise margin of I^2L for fan-in = fan-out = 1, as a function of $\beta = \beta_{upeff}$*

——— eqn. 12
○ computer simulated
● measured (Reference 2)

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26th February 1980

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13

Temperature Behaviour of the Static Noise Margins of ISL and STL

J. Lohstroh and R.M. Pluta

Abstract — **The low current level static ground-line voltage noise margins of ISL and STL as a function of temperature and the fan-out, are derived analytically for gates with and without an internal pull-up current. At high current levels where series resistances play an important role, the noise margins are obtained by computer simulations. It appears that STL has better noise margins than ISL at high temperature, when their logic swings are equal at room temperature, and when no pull-up currents are applied.**

With pull-up currents this difference decreases dramatically, and reasonable noise margins at high fan-outs can be obtained over a large temperature range.

13.I. Introduction

Integrated Schottky Logic (ISL) [1-4] and Schottky Transistor Logic (STL) [5-8] are both promising high speed VLSI candidates. Their basic principles of operation are similar, only their clamp device is different: a p-n-p transistor in ISL and a Schottky diode in STL. STL is a marginally faster than ISL (when the voltage swings are equal), at the cost of higher process complexity [9].

Important properties of both types of logic are their noise margins. In this paper the static noise margins of ISL and STL, will be studied as a function of temperature, both for the standard circuits without pull-up and circuits with pull-up currents (see Fig. 1).

When the voltage swings of ISL and STL are equal at room temperature, their noise margins at room temperature are very similar [10]. It will be shown in this paper that with increasing temperature the noise margins of ISL will decrease faster than the noise margins of STL, due to the large difference between the temperature coefficients of the saturation currents of the Schottky diodes and p-n-p transistors. This effect is even worse when series resistances cannot be disregarded. However, by lowering the barrier height of the ISL Schottky diodes and/or application of internal pull-up currents, the noise margins of ISL can be made as good as the noise margins of STL.

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In Section II the temperature coefficients of the voltage swings of ISL and STL are investigated theoretically and in Section III the theoretical methods and experimental methods (or by computer simulation) of obtaining the worst-case static noise margins are discussed. In Section IV the theoretical method is used to derive analytical worst-case static ground-line voltage noise margins of simplified ISL and STL circuits with the most essential series resistances included, with and without internal pull-up currents. Complete models with all series resistances included for oxide-isolated ISL and STL gates are given in Section V. The logic swing and the worst-case static ground-line

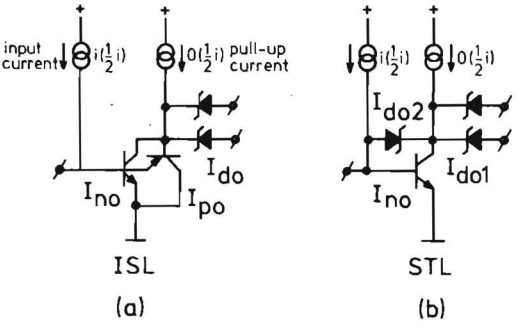

Fig. 1. ISL (a) and STL (b), with and without internal pull-up current. Without pull-up current the input current is i; with pull-up current the input current is $\frac{1}{2}i$ and the pull-up current is $\frac{1}{2}i$.

voltage noise margins of ISL and STL using these complete models are obtained by computer simulations, and the results are discussed in Section VI. Section VII contains a comparison of the static noise margins of ISL and STL, and a discussion about the practical use of the results obtained.

13.II. Temperature coefficients of the voltage swings of ISL and STL

As the voltage swings have a very large influence on the noise margins of ISL and STL, the temperature coefficients of the voltage swings will be considered first.

A. ISL

When the ideality factors of both the p-n-p transistor and the Schottky diode are 1 (n = 1), and when all series-resistances are ignored, then the voltage swing of ISL at reference temperature T_R is given by [1,9]:

$$\Delta V_{ISLR} = \frac{kT_R}{q} \ln \frac{\alpha_p^* I_{doR}}{I_{poR}} , \qquad (1)$$

where α_p^* is the effective forward collector-emitter current ratio of the p-n-p transistor [9], which is close to 1 for practical devices, I_{doR} is the saturation current of the output Schottky diode at reference temperature T_R, I_{poR} is the saturation current of the p-n-p transistor at reference temperature T_R (see Fig. 1(a)). The saturation current of the Schottky diode at reference temperature T_R is given by:

$$I_{doR} = AA^*T_R^2 \exp[-q(\phi_{B0} - \alpha T_R)/(kT_R)] = AA^*T_R^2 \exp(q\alpha/k)\exp[-q\phi_{B0}/(kT_R)], \tag{2}$$

where A is the diode area, A^* is the Richardson constant, ϕ_{B0} is the linearly extrapolated barrier height at 0°K [11], and α the temperature coefficient of the barrier height [11]. The saturation current of the Schottky diode at temperature T is [11]:

$$I_{doT} = I_{doR}\left(\frac{T}{T_R}\right)^2 \exp\left[\frac{q\phi_{B0}}{k}\left(\frac{1}{T_R} - \frac{1}{T}\right)\right]. \tag{3}$$

Further, the saturation current of the p-n-p transistor at temperature T is [11]:

$$I_{poT} = I_{poR}\left(\frac{T}{T_R}\right)^{1.8} \exp\left[\frac{qV_{G0}}{k}\left(\frac{1}{T_R} - \frac{1}{T}\right)\right], \tag{4}$$

where V_{G0} is the linearly extrapolated bandgap voltage at 0°K. Combination of (1), (3), and (4), and differentiation yields:

$$\left.\frac{d(\Delta V_{ISL})}{dT}\right|_{T_R} = \frac{\Delta V_{ISLR} - V_{G0} + \phi_{B0} + 0.2kT_R/q}{T_R}. \tag{5}$$

When a PtNi-silicide Schottky diode is used (with ϕ_{B0} = 0.8 V and α = .066 mV/°C), then in an oxide-isolated process with $I_{doR} = 25.10^{-14}$A, $I_{poR} = 5.10^{-17}$A and $\alpha_p^* = 0.98$, the voltage swing ΔV_{ISLR} is 220 mV. With V_{G0} = 1.205 V for the p-n-p transistor [11] therefore, the temperature coefficient of the voltage swing given by (5) equals – 0.6 mV/°C at room temperature [11].

If in the same lay-out the PtNi-silicide Schottky diode were replaced by a Schottky diode with a lower barrier height (Al for instance with ϕ'_{B0} = 0.74) then the voltage swing would increase by $(\phi_{B0} - \phi'_{B0})$Volt, assuming that $\alpha_{PtNi\text{-}silicide} = \alpha_{Al}$ (see equation (1) and (2)). In equation (5), ϕ_{B0} has to be replaced by ϕ'_{B0}, which means that the temperature coefficients of – 0.6 mV/°C will not change!

The temperature coefficient of the voltage swing of ISL will not depend therefore on the type of metal of the Schottky diode in a given lay-out, when the Schottky diodes have the same α.

B. STL

When the ideality factors of both Schottky diodes are 1, or at least equal, then the voltage swing of STL at reference temperature T_R is given by [6,9]:

$$\Delta V_{STLR} = \frac{kT_R}{q} \ln \frac{I_{do1R}}{I_{do2R}} , \tag{6}$$

where I_{do1R} and I_{do2R} are the saturation currents of the output Schottky diode and the clamp Schottky diode respectively (see Fig. 1(b)); they are given by (2) with A_1, α_1, ϕ_{B01} and A_2, α_2, ϕ_{B02} respectively as parameters.

Combination of (6) and (3) and differentiation yields:

$$\left.\frac{d(\Delta V_{STL})}{dT}\right|_{T_R} = \frac{\Delta V_{STLR} - \phi_{B02} + \phi_{B01}}{T_R} , \tag{7}$$

which can, with (2) and (6), be reduced to

$$\left.\frac{d(\Delta V_{STL})}{dT}\right|_{T_R} = \frac{k}{q} \ln \frac{A_1}{A_2} + \alpha_1 - \alpha_2 , \tag{8}$$

which is either zero (when $A_1 = A_2$ and $\alpha_1 = \alpha_2$) or very small compared with (5).

Thus, as a first-order approximation, the voltage swing of STL is independent of the temperature, when indeed the ideality factors of both diodes are equal.

If the last condition is not satisfied, the voltage swing depends on the current level of the gates, and this could result in a temperature coefficient that cannot be ignored.

Another statement to be made is that both Schottky diodes are assumed to obey the exponential characteristic $i_d = I_{do} (\exp(qV_d/(nkT)) - 1)$ when forward *and* reverse-biased. This may not be the case for the low barrier output diode (often made with TiW), which can exhibit additional leakage current which can dominate the exponential behaviour.

13.III. The static noise margins; methods of determination

As shown in [12], four types of noise can be considered: voltage series noise, parallel current noise, ground-line voltage noise and power supply voltage noise.

The worst-case static noise margins ΔV_{series}, ΔV_{gnd}, ΔV_{supply}, and $\Delta i/i$ are defined as the minimum noise amplitudes which, when applied with alternating sign in an infinitely long chain of inverters, cause the gates to switch to the wrong state. Instead of an infinitely long chain a flip-flop can also be used [12], and provides an easier way of determining the noise margins.

As in all logic gates, the transconductance of the transistors decreases with increasing temperature, the voltage swing should increase with increasing temperature to

obtain temperature-independent noise margins.

When the voltage swing remains constant, or even decreases with temperature (and with increasing fan-out), all static noise margins decrease with increasing temperature and may eventually become zero. All types of static noise margins become zero simultaneously at the same temperature, so only *one* noise margin has to be investigated to find the critical temperature [12].

In this paper we will investigate ΔV_{gnd}, because voltage drops over ground rails in LSI and VLSI chips are one of the biggest concerns in ISL and STL designs.

As shown in the next section, simple analytical expressions for the noise margins can be obtained only when most of the series resistances are ignored. Nevertheless, these calculations show very clearly how the noise margins depend on temperature and fan-in and fan-out.

The method of calculation is to determine the noise amplitude at which the small signal loopgain becomes 1 [13]; under this condition the Jacobian of the Kirchoff equations is zero [14].

When all series resistances are included, the analytical approach becomes too complicated. In this case computer simulations have to be carried out. The most reliable method is to do quasi-static transient simulations by increasing the noise sources in a flip-flop, linearly and slowly with time (slowly compared to the switching speed of the flip-flop) and detect the minimum noise amplitude which causes the flip-flop to switch to the wrong state.

13.IV. First-order analytical expressions for the voltage swing and the worst-case ground-line voltage noise margins of simplified ISL and STL circuits with the most important series resistances included

In this section analytical expressions for the worst-case ground-line voltage noise margins of ISL and STL, with and without pull-up currents, are derived with most of the transistor series resistances ignored, but with the essential series resistances R_c and R_d (n-p-n collector series resistance and Schottky diode series resistance) included; see equations (13), (14), (16) and (18). All the expressions are derived for the condition that the ideality factor of all junctions is 1. The equations (13), (14), (16) and (18) have been verified by computer simulations to be accurate to within 1 mV.

A. ISL without pull-up current

Fig. 2 shows worst-case ground-line voltage noise applied to an ISL flip-flop with F = fan-in = fan-out = 4 [12]. First the circuit without pull-up will be considered (input-currents i, no pull-up currents).

As shown in the appendix, a simple analytical expression can be obtained only

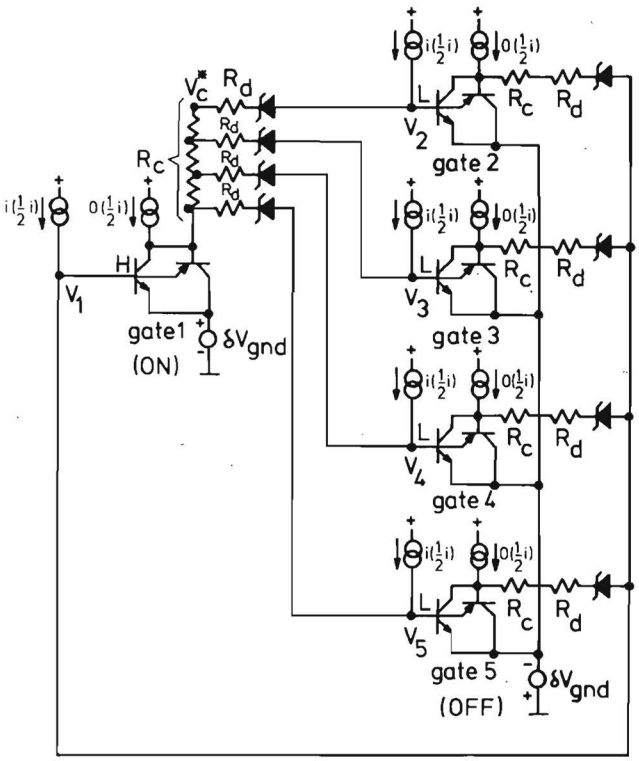

Fig. 2. Worst-case ground-line voltage noise applied to an ISL flip-flop with F = fan-in = fan-out = 4. All series resistances, except R_c and R_d are left out. A simple analytical solution of the noise margin is obtained when all Schottky diodes of gate 1 are connected to V_c^*.

when all transistor series resistances, except R_c and R_d, are ignored, $\beta_{n\text{-}p\text{-}n} = \infty$, $\alpha_p^* = 1$, and when all Schottky diodes are connected to node V_c^* (see fig. 2). Fig. 3 shows the equivalent diagram of Fig. 2; all parallel OFF-gates are replaced by one gate with F-times increased input current, F-times increased saturation currents and F-times reduced series resistance of the Schottky diode. The factor γ is the saturation current ratio of the n-p-n and the p-n-p transisator ($\gamma = I_{no}/I_{po}$). For practical values of I_{do}/I_{po} (> 100), gate 2 is far from saturation when the flip-flop reaches its metastable point (when the noise voltages are increased to the value ΔV_{gnd}). This means that in gate 2 the p-n-p transistor, the collector series resistance of the n-p-n, and the Schottky diode with its series resistance can be disregarded. When $\beta_{n\text{-}p\text{-}n} = \infty$, $\alpha_p^* = 1$ and the ideality factor of all junctions are 1, only one variable (i_1) exists, and has to be determined by finding the condition for which the loop-gain is 1 and consequently the Kirchoff-Jacobian is 0.

Kirchoff's voltage law yields:

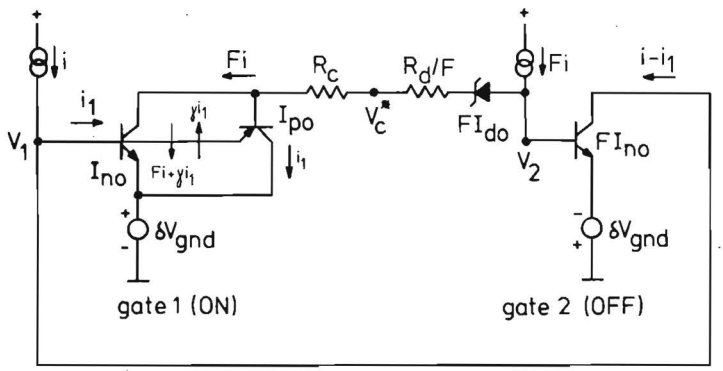

Fig. 3. Equivalent diagram of the ISL flip-flop of Fig. 2 with F as parameter.

$$f_1 = \Delta V_{gnd} + \frac{kT}{q} \ln \frac{Fi + \gamma i_1}{I_{no}} - \frac{kT}{q} \ln \frac{i_1}{I_{po}} + FiR_c + iR_d + \frac{kT}{q} \ln \frac{Fi}{FI_{do}}$$

$$- \frac{kT}{q} \ln \frac{i - i_1}{FI_{no}} + \Delta V_{gnd} = 0,$$

which reduces to:

$$f_1 = 2\Delta V_{gnd} - \Delta V_{ISL} + \frac{kT}{q} \ln \frac{Fi(Fi + \gamma i_1)}{i_1(i - i_1)} = 0, \tag{9}$$

where $\gamma = I_{no}/I_{do}$ and where ΔV_{ISL} is given by:

$$\Delta V_{ISL} = \frac{kT}{q} \ln \frac{I_{do}}{I_{po}} - i(FR_c + R_d), \tag{10}$$

which is $V_2 - V_1$ in Fig. 2 and Fig. 3 when measured for $\delta V_{gnd} = 0$.

The Kirchoff-Jacobian, which contains only one element, is zero when $\partial f_1/\partial i_1 = 0$. Differentiation of f_1 yields:

$$\frac{i_1(i - i_1)}{Fi(Fi + \gamma i_1)} \cdot \frac{Fi[i_1(i - i_1)\gamma - (Fi + \gamma i_1)(i - 2i_1)]}{i_1^2(i - i_1)^2} = 0,$$

which reduces to:

$$F\left(\frac{i}{i_1}\right)^2 - 2F\left(\frac{i}{i_1}\right) - \gamma = 0. \tag{11}$$

Solution of (11) delivers:

$$\frac{i}{i_1} = 1 + \sqrt{1 + \gamma/F} \ . \tag{12}$$

Note that $i_1 = \frac{1}{2}i$ when $\gamma \ll F$. Thus the flip-flop switches as soon as V_{BE} of the n-p-n transistor of the OFF-gate is large enough to cause the OFF-transistor to conduct $\frac{1}{2}i$.

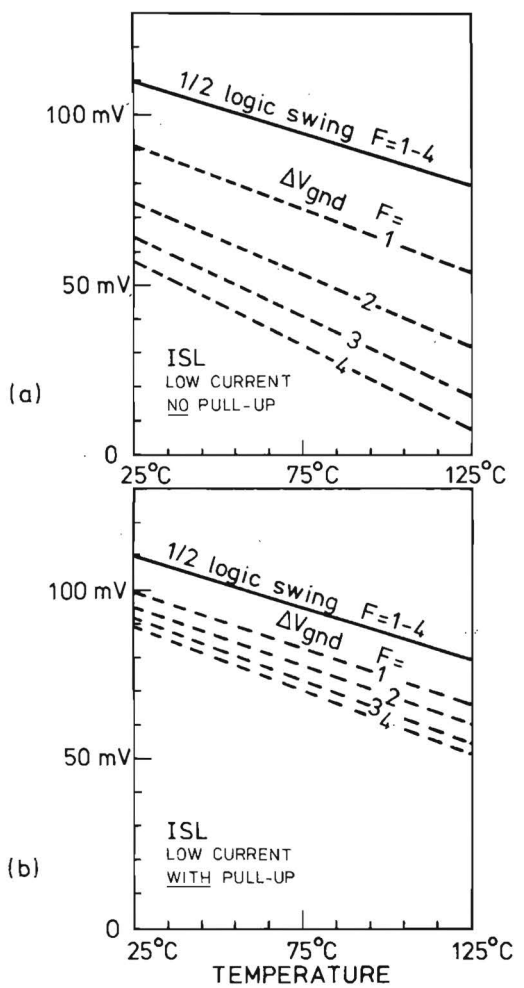

Fig. 4. Half the voltage swing and the worst-case static ground-line voltage noise margins at low current levels of ISL without internal pull-up current (a) and with internal pull-up current (b), with F as parameter. The noise margins are obtained analytically and verified by computer simulations.

The worst-case static ground-line voltage noise margin is now the noise margin given by the combination of (9) and (12):

$$\Delta V_{\text{gnd ISL}} = \frac{1}{2}\Delta V_{\text{ISL}} - \frac{kT}{q}\ln\sqrt{\frac{Fi(Fi+\gamma i_1)}{i_1(i-i_1)}} = \frac{1}{2}\Delta V_{\text{ISL}} - \frac{kT}{q}\ln\left(F+\sqrt{F(F+\gamma)}\right). \quad (13)$$

Equation (13) has been verified with computer simulations with the practical values $\beta_{\text{n-p-n}} = 70$ and $\alpha_{\text{p}}^* = 0.98$; the simulated results are in this case closer than 1 mV to the values obtained by (13), so the influence of $\beta_{\text{n-p-n}}$ and α_{p}^* in practical circuits can be disregarded.

For low current levels the second part of equation (10) can be ignored, and consequently the temperature coefficient of the voltage swing of ISL is -0.6 mV/°C as explained in Section II.

Fig. 4(a) shows $\frac{1}{2}\Delta V_{\text{ISL}}$ and $\Delta V_{\text{gnd ISL}}$ as a function of temperature with F as parameter, according to equation (13) for low current levels, for ISL with a voltage swing of 220 mV at room temperature and $\gamma = 0.2$ (in real devices γ decreases a little with temperature, due to the difference in bandgap-voltage of the n-p-n and the p-n-p). The noise margin decreases considerably with increasing F (with $(kT/q)\ln 2F$ when $\gamma \ll 1$), and when the temperature increases.

With $F = 4$, ΔV_{gnd} decreases from 58 mV to 8 mV when the temperature increases from 25°C to 125°C.

It has been shown [10,12] that measurement results of the static noise margins correspond very well with computer simulated values.

B. ISL with pull-up current

Pull-up currents can be used to decrease the fan-in dependency of the propagation delay time [9]. It appears that the noise margins also improve when pull-up currents are applied.

In this paper the case is studied where half the gate current is used as input current, and the other half is used as pull-up current (see Fig. 2 with pull-up currents and input currents of $\frac{1}{2}i$).

If all series resistances are again ignored, except R_{c} and R_{d}, $\beta_{\text{n-p-n}} = \infty$, $\alpha_{\text{p}}^* = 1$, the equivalent diagram of Fig. 2 is given by Fig. 5. The noise margin improvement is caused by the fact that in this case a threshold effect is built-in before the flip-flop can switch. The OFF-transistor of gate 2 must now conduct at least $\frac{1}{2}Fi$ before the diode D2 is forward biased (when the transistor current is less than $\frac{1}{2}Fi$, node V_{p} is clamped to the power supply voltage and diode D2 is reverse-biased). As soon as $i_{\text{cOFF}} > \frac{1}{2}Fi$ node V_{p} comes down and D2 is forward-biased, and at the same time the loop-gain is larger than 1 and the flip-flop immediately switches to the wrong state.

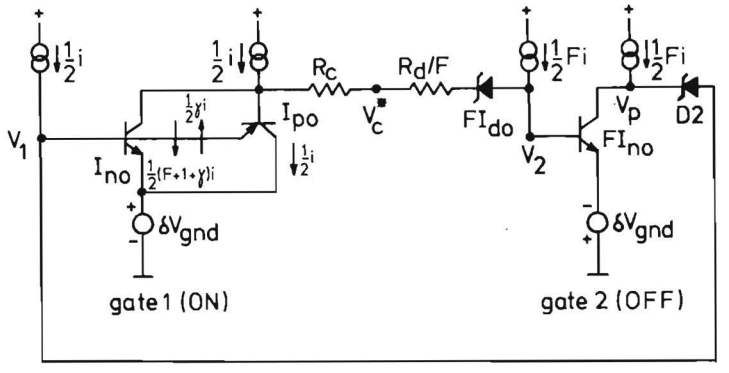

Fig. 5. Equivalent diagram of the ISL flip-flop of Fig. 2 with pull-up currents, with F as parameter.

Thus the noise margin can easily be found as the condition for which i_{cOFF} of gate 2 is $\frac{1}{2}Fi$, with $i_{D2} = 0$.

In this case Kirchoff's voltage law yields:

$$\Delta V_{gnd} + \frac{kT}{q} \ln \frac{\frac{1}{2}(F + 1 + \gamma)i}{I_{no}} - \frac{kT}{q} \ln \frac{\frac{1}{2}i}{I_{po}} + \frac{1}{2}FiR_c + \frac{1}{2}iR_d$$

$$+ \frac{kT}{q} \ln \frac{\frac{1}{2}Fi}{FI_{do}} - \frac{kT}{q} \ln \frac{\frac{1}{2}Fi}{FI_{no}} + \Delta V_{gnd} = 0,$$

$$\text{Thus } \Delta V_{gnd\,ISL\,pull\text{-}up} = \tfrac{1}{2}\Delta V_{ISL\,pull\text{-}up} - \frac{kT}{q} \ln \sqrt{F + \gamma + 1}, \tag{14}$$

where $\Delta V_{ISL\,pull\text{-}up}$ is given by:

$$\Delta V_{ISL\,pull\text{-}up} = \frac{kT}{q} \ln \frac{I_{do}}{I_{po}} - \frac{1}{2}(FR_c + R_d)i, \tag{15}$$

which has also been verified with computer simulations to be correct to within 1 mV for practical values of $\beta_{n\text{-}p\text{-}n}$ and α_p^*.

Fig. 4(b) shows $\frac{1}{2}\Delta V_{ISL\,pull\text{-}up}$ and $\Delta V_{gnd\,ISL\,pull\text{-}up}$ as function of temperature according to equation (14) at low current levels, with the same gates as used in Fig. 4(a).

Compared with Fig. 3(a), the F-independent voltage swing is the same, but the decrease of the noise margin with F is much less (about half as much as in the case without pull-up), so $\Delta V_{gnd\,ISL\,pull\text{-}up}$ is 90 mV at 25°C and 50 mV at 125°C for $F = 4$.

C. STL without pull-up current

STL is treated in the same way as ISL. In Fig. 2 therefore all p-n-p transistors have to be replaced by Schottky diodes (see Fig.1). If all series resistances are ignored, except R_c and R_d, and $\beta_{n\text{-}p\text{-}n} = \infty$, a similar expression as (13) can be found:

$$\Delta V_{gnd\,STL} = \frac{1}{2}\Delta V_{STL} - \frac{kT}{q} \ln (F + \sqrt{(F+1)F}\,), \tag{16}$$

with

$$\Delta V_{STL} = \frac{kT}{q} \ln(I_{do1}/I_{do2}) - (FR_c + R_d)i\,. \tag{17}$$

Equation (16) has been verified with computer simulations with $\beta_{n\text{-}p\text{-}n} = 70$ (1 mV accuracy).

Note that (16) is identical to the ISL case with $\gamma = 1$ (in this case the n-p-n transistor of gate 1 would have to conduct the same current as in ISL).

When both Schottky diodes have indeed an ideality factor of one, and when $A_1 = A_2$ and $\alpha_1 = \alpha_2$ (see Section II), then the temperature coefficients of the first part of equation (17) is zero and consequently the voltage swing of STL at low current levels is temperature independent.

Fig. 6(a) shows $\frac{1}{2}\Delta V_{STL}$ and $\Delta V_{gnd\,STL}$ as a function of temperature with F as parameter for low current levels, according to equation (16), for STL with a voltage swing of 220 mV.

Compared with ISL the influence of F on the noise margin is somewhat smaller, but the initial noise margin for $F = 1$ is larger than that of ISL at 25°C. The decrease of the noise margins with increasing temperature is much less than for ISL because of the temperature-independent voltage swing.

D. STL with pull-up current

With gate input currents of $\frac{1}{2}i$ and pull-up currents of $\frac{1}{2}i$, it can be calculated that the worst-case static ground-line voltage noise margin is:

$$\Delta V_{gnd\,STL\,pull\text{-}up} = \frac{1}{2}\Delta V_{STL\,pull\text{-}up} - \frac{kT}{q} \ln \sqrt{F+2}\,, \tag{18}$$

with

$$\Delta V_{STL\,pull\text{-}up} = \frac{kT}{q} \ln (I_{do1}/I_{do2}) - \frac{1}{2}(FR_c + R_d)i\,, \tag{19}$$

which has also been verified with computer simulations.

Fig. 6(b) shows the low-current level results of equation (18) for the same gate as in Fig. 6(a); the improvement is obvious.

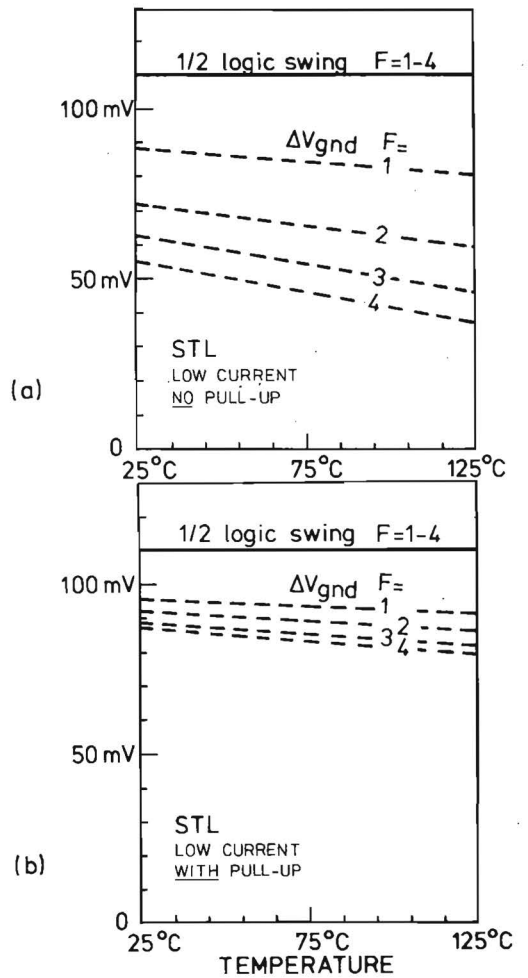

Fig. 6. As Fig. 4, but this time for STL.

13.V. DC models of oxide-isolated ISL and STL gates

Small-size oxide-isolated structures are taken as examples because, in these devices, series resistances tend to be higher than in pn-isolated devices of larger dimensions [11,15]. It will be shown that these series resistances (in particular R_c and R_d) will seriously affect the noise margins.

Fig. 7(a) shows a DC-model (no capacitances included) of an oxide-isolated ISL gate [11]. It contains an n-p-n (TN), a p-n-p (TP), a pn diode (D), four Schottky diodes

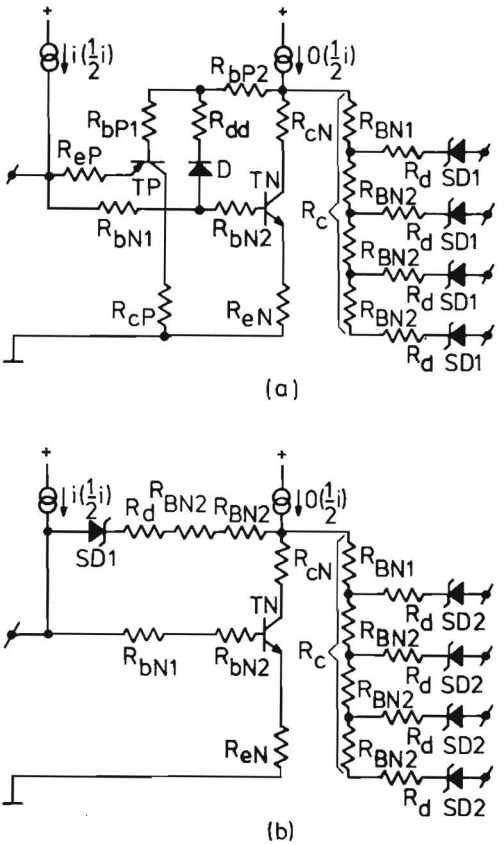

Fig. 7. DC models of minimum-size oxide-isolated ISL (a) and STL (b).

(SD1) and series resistances. The pn diode is introduced in order to model the injection of holes at the extrinsic base-collector junction of the saturated n-p-n [11]. Fig. 7(b) shows a DC model of an STL gate. As the n-p-n transistor does not go into saturation, no pn diode is introduced. The clamp Schottky diode (SD1) is the same type of high-barrier Schottky diode as the output Schottky diode of ISL (PtNi-silicide, $\phi_{B01} = 0.8$V). The output Schottky diodes are assumed to be of TiW ($\phi_{B02} = 0.58$V). All relevant DC parameters and their temperature coefficients of ISL and STL are listed in Table 1 (a) and (b) respectively. The low current level voltage swing is 220 mV both for ISL and STL.

TP	TN	D	SD1	SD2
$n = 1$ $V_{G0} = 1.206V$ $I_{po} = 5.10^{-17}A$ $\beta_{fP} = 48$ $\beta_{rP} = 0.04$ $R_{eP} = 20\Omega$ $R_{bP1} = 6k\Omega$ $R_{cP} = 1.1k\Omega$	$n = 1$ $V_{G0} = 1.16V$ $I_{no} = 10^{-17}A$ $\beta_{fN} = 70$ $\beta_{rN} = 300$ $R_{en} = 10\Omega$ $R_{bN2} = 2k\Omega$ $R_{cN} = 30\Omega$	$n = 1$ $V_{G0} = 1.206V$ $I_{ddo} = 33.10^{-21}A$ $R_{dd} = 40\Omega$ resistors $R_{bN1} = 1k\Omega$ $R_{BN2} = 45\Omega$ $R_{bP2} = 30\Omega$ $R_{BN1} = 100\Omega$	$n = 1$ $\phi_{B01} = 0.8V$ $I_{do1} = 25.10^{-14}A$ $R_d = 70\Omega$	$n = 1$ $\phi_{B01} = 0.58V$ $I_{do2} = 13.10^{-10}A$ $R_d = 70\Omega$

(a)

TP	TN	D	SD1	SD2
$T\beta_{fP} = 2.10^{-3}$ $T\beta_{rP} = 2.10^{-3}$	$T\beta_{fN} = 56.15^{-4}$ $T\beta_{rN} = 27.10^{-4}$	$TR_{dd} = 6.10^{-3}$ resistors	$TR_d = 6.10^{-3}$	$TR_d = 6.10^{-3}$
$TR_{eP} = 2.10^{-4}$ $T^2R_{eP} = 7.10^{-6}$ $TR_{bP1} = 6.10^{-3}$ $TR_{cP} = 8.10^{-3}$	$TR_{eN} = 10^{-3}$ $TR_{bN}2 = 2.10^{-3}$ $T^2R_{bN2} = 6.10^{-6}$ $TR_{cN} = 6.10^{-3}$	$TR_{bN1} = 2.10^{-4}$ $T^2R_{bN1} = 7.10^{-6}$ $TR_{bP2} = 13.10^{-4}$ $TR_{BN1} = TR_{BN2} = 13.10^{-4}$		

(b)

TABLE 1. (a) Room temperature values of the most relevant parameters of the models of Fig. 7, and their temperature coefficients (b).

13.VI. Voltage swings and worst-case static ground-line voltage noise margins of oxide-isolated ISL and STL at 100 μA/gate

This section follows the same lines as Section IV, but this time all voltage swings and noise margins are obtained by computer simulations, using the complete models described in Section V. The main difference between the computer simulations and the analytical calculations of Section IV is that for the computer simulations the Schottky diodes are not all connected to V_c^* (see Fig. 2) and thus V_2, V_3, V_4 and V_5 are not equal at moderate current levels (voltage swing dispersion). For $F > 1$ the logic swing will be somewhat larger than given by (10), (15), (17) and (19) respectively. To obtain worst-case conditions, the last Schottky diodes are always used in gate 1, so for $F = 3$, gate 5 is disconnected; for $F = 2$, gates 5 and 4 are disconnected; and for $F = 1$, gates 5,4 and 3 are disconnected (see Fig. 2).

A. ISL without pull-up current

Fig. 8(a) shows the simulation results of the voltage swings and ground-line noise margins. With $F = 1$ there is no voltage swing dispersion, and in this case equation (10) is correct. With the gate model of Fig. 7(a) we find that, at 25°C, R_c is 235 Ω, and R_d is 70 Ω, so the voltage swing would be about 30 mV less at 100 μA. Comparison of Fig. 8(a) and Fig. 4(a) shows that the difference is 20 mV; this is mainly caused by the voltage drop of about 10 mV across the base-series-resistance of the p-n-p transistor (the last effect is not included in equation (10)). Fig. 8(a) also shows that the logic swing does not decrease linearly with F due to the fact that all Schottky diodes are not connected to the same node (V_c^*).

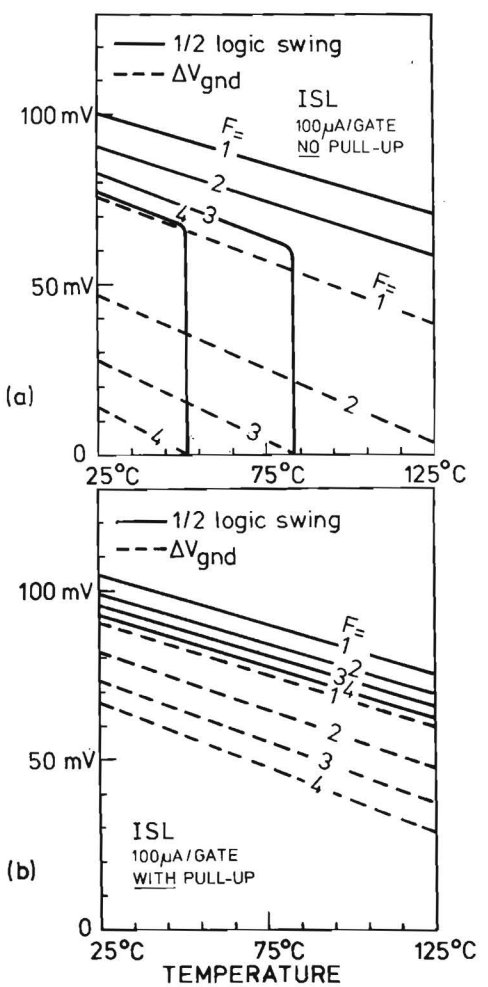

Fig. 8. As Fig. 4 for minimum-size oxide-isolated ISL at 100 μA per gate. All results are obtained by computer simulations, using the model of Fig. 7(a).

The loss of noise margin is somewhat more than half the loss of the voltage swing, when compared with Fg. 4(a); this is mainly due to the high base-series-resistance of the p-n-p which apparently increases the external measured voltage swing, and the base-series--resistance of the n-p-n transistor which decreases the transductance of this transistor. This all ensures that for minimum-size oxide-isolated ISL with $F = 4$, a critical temperature of only 50°C is obtained.

B. ISL with pull-up current

Fig. 8(b) shows that a dramatic improvement is obtained with the application of pull-up currents. This is for two reasons: a) the decrease with the fan-out of the noise margin is better anyway than in pull-up-less circuits, b) the loss of voltage swing is halved

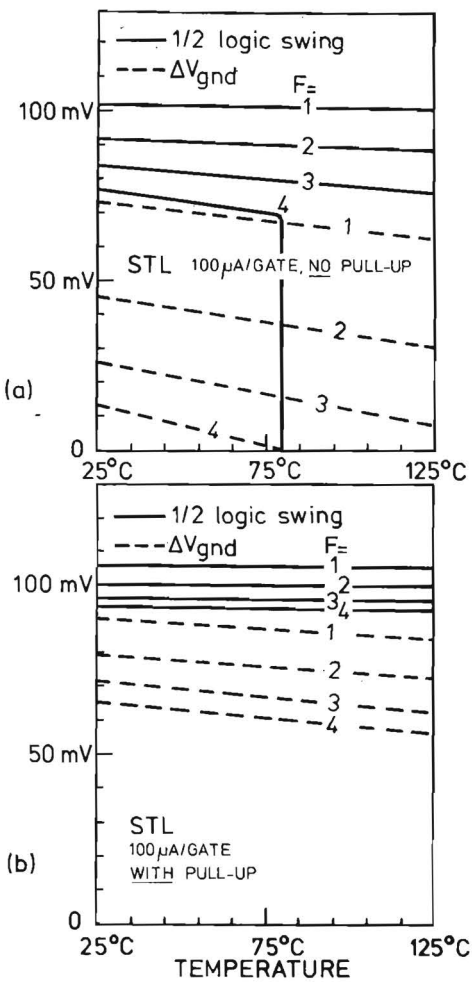

Fig. 9. As Fig. 6 for minimum-size oxide-isolated STL at 100 μA per gate. All results are obtained by computer simulations, using the model of Fig. 7(b).

(when the pull-up current is applied to the most advantageous node; see Fig. 7). The critical temperature when $F = 4$ is now about 200°C.

C. STL without pull-up current

Fig. 9(a) shows the simulation results for STL. Here also the voltage swing losses are somewhat less than indicated by (17), due to the voltage drop across the series-resistance of the clamp-Schottky diode. Note that the temperature coefficient of the voltage swing is slightly negative, due to the positive temperature coefficients of the series resistances.

Compared with ISL (Fig. 8(a)), the noise margins are better, but when $F = 4$ the critical temperature is 80°C, which is only 30°C more than ISL with $F = 4$.

D. STL with pull-up current

In STL also the pull-up currents cause a significant improvement in the noise margins as illustrated in Fig. 9(b).

13.VII. Comparison, conclusions and discussion

In this paper the noise margins of ISL and STL have been studied, based on the assumptions that the ideality factor of all transistors and Schottky diodes is 1, and that no dominating leakage currents are present in the low-barrier Schottky diode in STL.

When the voltage swings of ISL and STL are equal at room temperature, then the room temperature values of the noise margins of ISL are a little better, due to the fact that in ISL the superfluous base-current of the ON-transistor is sinked to ground (by the p-n-p transistor), whereas in STL this current has to flow through the n-p-n transistor. With increasing temperature, however, the noise margins of ISL are very soon smaller than those of STL, mainly because of the high negative temperature coefficient of the voltage swing of ISL (-0.6 mV/°C).

As is shown for minimum-size oxide-isolated ISL and STL gates, series resistances seriously affect the noise margins when the gates are driven at a relative large gate current, because of the large internal voltage drops. Of course, the gate current can be decreased to obtain better noise margins, but then the speed of the logic is lower. An alternative measure is to apply pull-up currents which not only decrease the fan-in dependency of the propagation delay times, but as shown in this paper, improve the noise margins dramatically.

With pull-up currents the noise margins of ISL will also be smaller than of STL at 125°C when the voltage swings are equal at room temperature. Only when the ISL voltage swing is about 60 mV higher at room temperature, will both logic circuits exhibit similar noise margins at 125°C. This can be done by decreasing the barrier height of the Schottky diodes in ISL; the penalty is some speed degradation at room temperature.

In this paper the noise margins have been investigated up to F = fan-in = fan-out = 4 in infinitely long chains of inverters or in flip-flops.

It may be asked how representative the figures obtained are for real logic circuits. The answer depends totally on the type of logic structures used. When for instance flip-flops are used in registers, in most cases F is 2, which means that the critical temperature (= temperature for which all noise margins become zero) for $F = 2$ has to be higher than the maximum operating temperature of the chip. In complex logic structures, where large arrays of gates with high fan-in and fan-out are used (in parallel multipliers for instance), the requirements are more stringent, and therefore pull-up currents for all gates are essential in those cases to avoid signal degradation. In logic circuits where in the logic paths gates with high F-values are succeeded by gates with low F-values, signal regeneration can take place, which means that for the high-F gates a reduced or even negative worst-case noise margin may be acceptable; however, this makes the designers job rather complicated. On the other hand, when the noise margins are positive over the whole temperature range for the maximum used value of F, then the designer has maximum freedom without any risk of mal-functioning circuits.

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Appendix A
ISL Applications

Until now all ISL applications have been made in a pn-isolated process with a 3 μm epitaxial layer and 5 μm minimum details.
The following designs will be discussed:

A. The 3422A, which is a 256 bits shiftregister built-up with D-flip-flops.

B. The OQ4100N1, which is a 16x4 bits pipeline-multiplier, with adders, substractors, rounding logic, timing and system logic: this chip is a part of a fast Fourier transform system.

C. The OQ0040, which is a counter chip that combines ECL, I^2L, ISL and TTL on the same chip.

D. The ISL-CCL library (CCL = Composite Cell Logic), which is a custom IC approach consisting of a predesigned logic-function mask-library from which building blocks can be used to design custom LSI chips with a relatively short turn-around time. As an example the 8X60 (FIFO memory controller) will be discussed.

E. The 8A1200, which is an uncommitted logic gate array (or masterslice) of 1200 NAND-gate equivalents featuring up to 10 inputs and 4 outputs per gate. Each gate is accessable by paths reserved for custum metal interconnection. The turn-around time is very short.

Oxide isolated ISL applications such as high performance gate array, and a 12x12 bit parallel multiplier are in preparation. They will not be discussed in this appendix.

A. The 3422A (designed by J. v.d. Crommenacker).

This chip is a 256 bits shiftregister with 256 D-flip-flops. The total number of equivalent gates is 1674. The load resistances are 8 kΩ, which implies that with a power supply voltage of 2.3 V the current per gate is about 200 μA.

The total power dissipation is 770 mW. Fig. 1 shows the chip (chipsize = 22 mm^2). Each D-flip-flop consists of 6 gates and two separate Schottky diodes (in one island) for the clock-input. The clockpulses are distributed over the chip by repeated fan-out, and remote Schottky diode islands (see Fig. 2). To handle fan-outs larger than 4, ISL gates are used with larger sizes and smaller load resistances. In this design 2 x and 4 x sizes are used (see Fig. 2) to obtain fan-out 8 and fan-out 16. Fig. 3 shows a detail of the chip; indicated is a D-flip-flop, a distributed Schottky clock-input, clockline A (see also Fig. 2), a 4 x size ISL gate with Schottky input and clockline B. The maximum toggle frequency of this shift register has been measured to be 50 MHz.

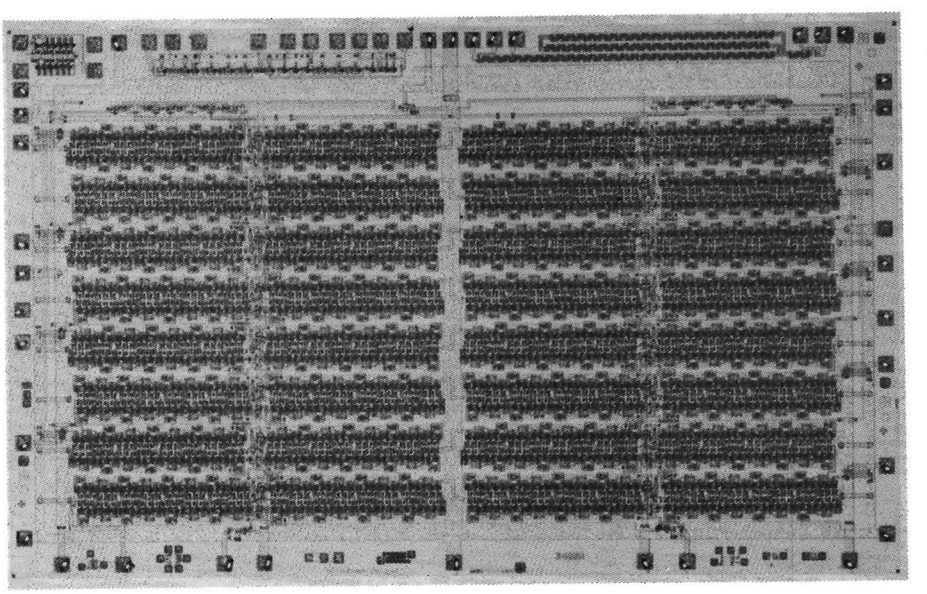

Fig. 1. Chip photograph of the 3422A.

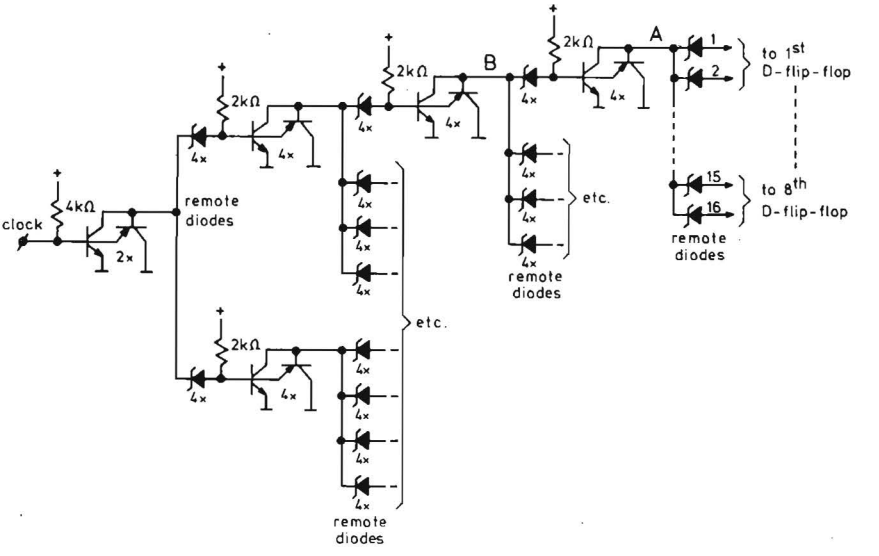

Fig. 2. Clock distribution circuitry on the 3422A.

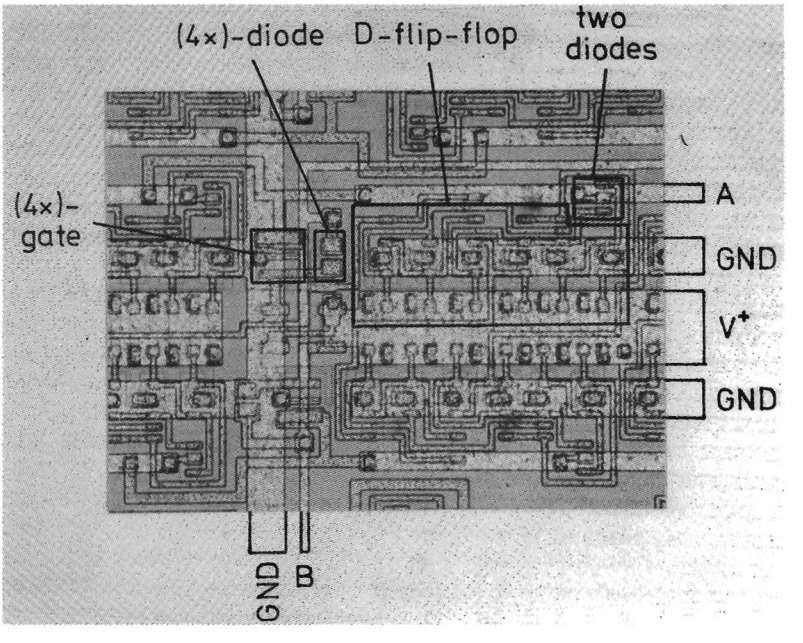

Fig. 3. Detail of the 3422A; indicated is a D-flip-flop, a distributed Schottky clock-input, clockline A (see Fig. 2), a 4x size ISL gate with Schottky input and clockline B.

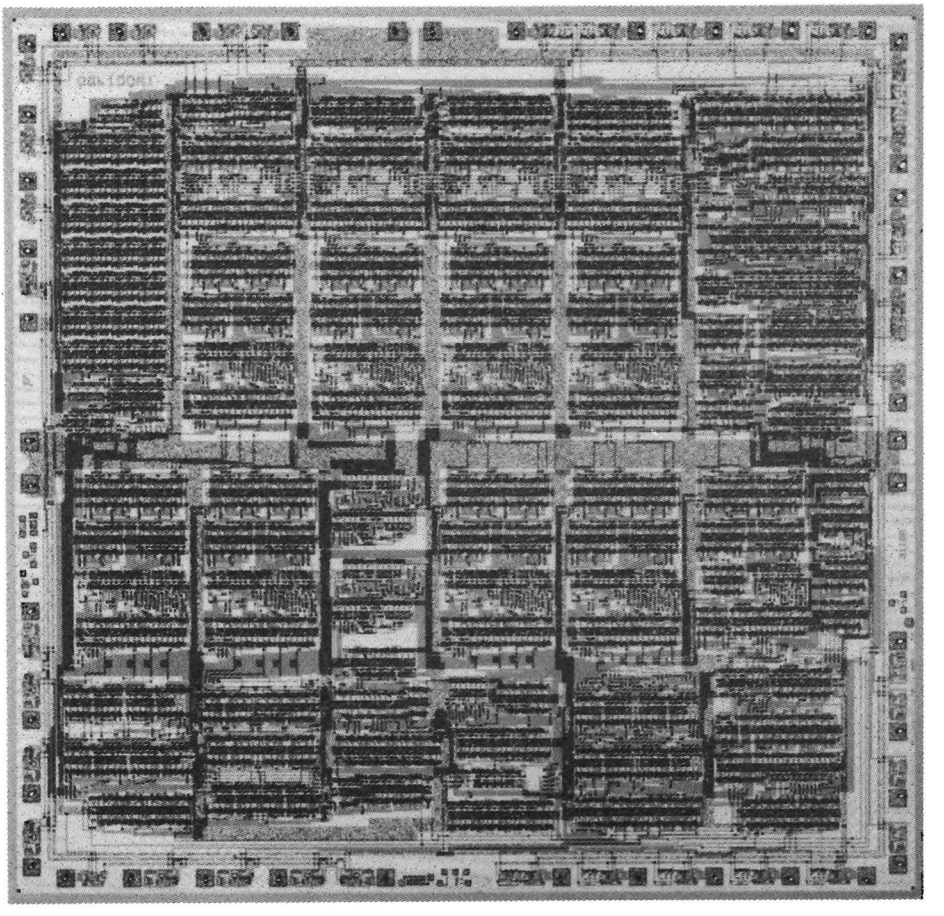

Fig. 4. Chip photograph of the OQ4100N1.

B. The OQ4100N1 (designed by H. Ontrop).

This LSI chip contains a 16x4 bits pipeline-mutiplier, with adders, subtractors, rounding logic, timing and system logic, for application in a fast Fourier transform system. The chip is shown in Fig. 4. The number of gates is 2500; chipsize is 42 mm^2. All internal logic is ISL; input buffers and output buffers make the chips low-power Schottky TTL compatible.

To achieve temperature independent propagation delay times, the current per LSI gate is adjusted to 90 μA (see Fig. 10 in Section 9). The ISL power supply voltage is 1.6 V; the TTL power supply voltage is 5 V. The total power dissipation is 530 mW. The minimum maximal operating frequency over the full ambient temperature range (0° – 70°C) and supply voltage ranges (1.6 V ± 10% V and 5V ± 10%) is 10 MHz, so guaranteed clock periods of 100 ns can be used. In each clock period the signals have to ripple through 11 stages (the logic is 11 stages deep), so the average propagation delay time is about 100 ns/11 = 9 ns for the gates having an average fan-in of 3

and an average fan-out of 3. Only 20 dummy gates are used in the time-critical pathes to prevent excessive delay-increase due to large fan-ins. The typical operating frequency is 13 MHz.

The clockpulses are distributed over the chip by the same repeated fan-out method as in the 3422A.

C. The OQ0040 (designed by B. Nilsson, W.K. Kalkman and J.A. van Nielen).

This LSI chip combines ECL, I^2L and TTL in the same chip. It forms the heart of the Philips nine-digit frequency counter series PM667X [1-3]. Fig. 5 shows the chip-photograph. The chip contains two counting registers, synchronizers and logic-control circuitry needed for such measurement functions as frequency, reciprocal frequency, period average, frequency ratio average, count, time interval, time interval average, phase, duty cycle and multiple burst average. The high frequncy (10 MHz) input data is accepted at ECL level which makes it possible to use ECL prescalers. The command inputs are TTL. Outputs are ECL (for fast triggering) and TTL.

About 1000 highly packed I^2L gates operating at 70 μA/gate are used for the logic functions operating below 1.5 MHz, and about 500 ISL gates (also operating at 70 μA/gate) are used for the 10 MHz functions (counting registers and control logic with maximal 4 gate delays per clockpulse). The frequency specification is 10 MHz; a maximal frequency of 18 MHz was measured. Power supply voltages are 5 V and 1.5 V. Power dissipation is about 100 mA·1.5V + 25 mA·5V = 275 mW. The chip-size is 23.2 mm^2.

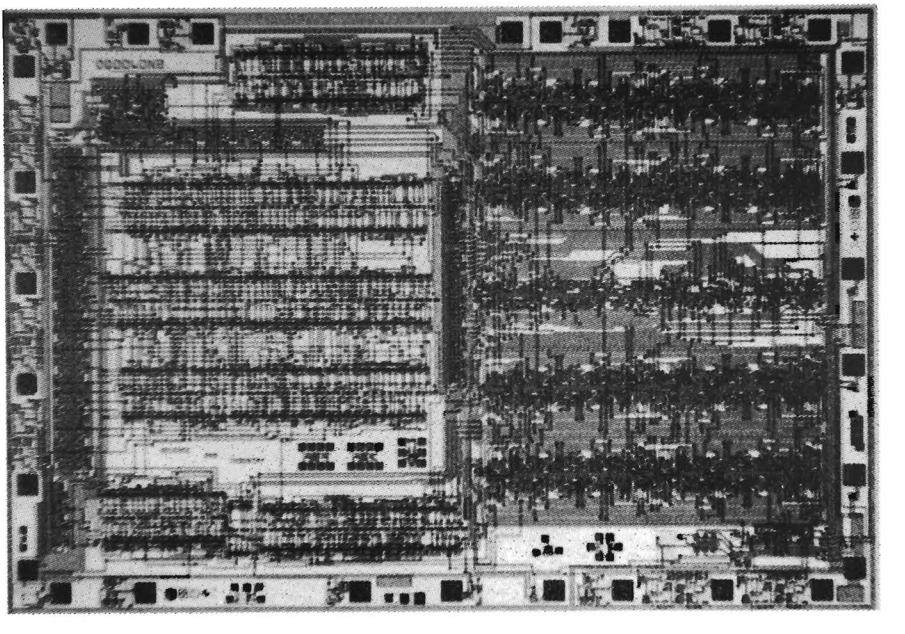

Fig. 5. Chip photograph of the OQ0040.

D. The ISL-CCL library (designed by D. Goddard) with the 8X60 as application.

The ISL-Composite Cell Logic library is a mask-library with predesigned cells, from which selected cells can be combined to form a custom chip which can be made with a short turn-around time [4-6].

The library contains AND gates, NAND gates, OR gates, NOR gates, EXCLUSIVE OR/NOR gates, flip-flops, three-state cells, diode cells, input- and output-buffers, clock buffers, etc.

The CCL approach is particular well suited to design applications where circuit complexities fall within a range of 100- to 1000 gates. The internal cell interconnections are made with a first layer metallization; the cells are interconnected with a second layer metallization on a 32 μm^2 grid. Cell sizes are 128 μm x (n x 32) μm^2, with n = 1, 2, 3, - . . . etc., depending on the particular cell size.

Each cell is described in a manual [6] that specifies the DC and AC characteristics. For instance a NAND gate has a size of 128 μm x 96 μm, consumes a maximum current of 190 μA, and has a maximum propagation delay time of 6 ns at 150°C for fan-in = 1 (10 ns for fan-in = 5).

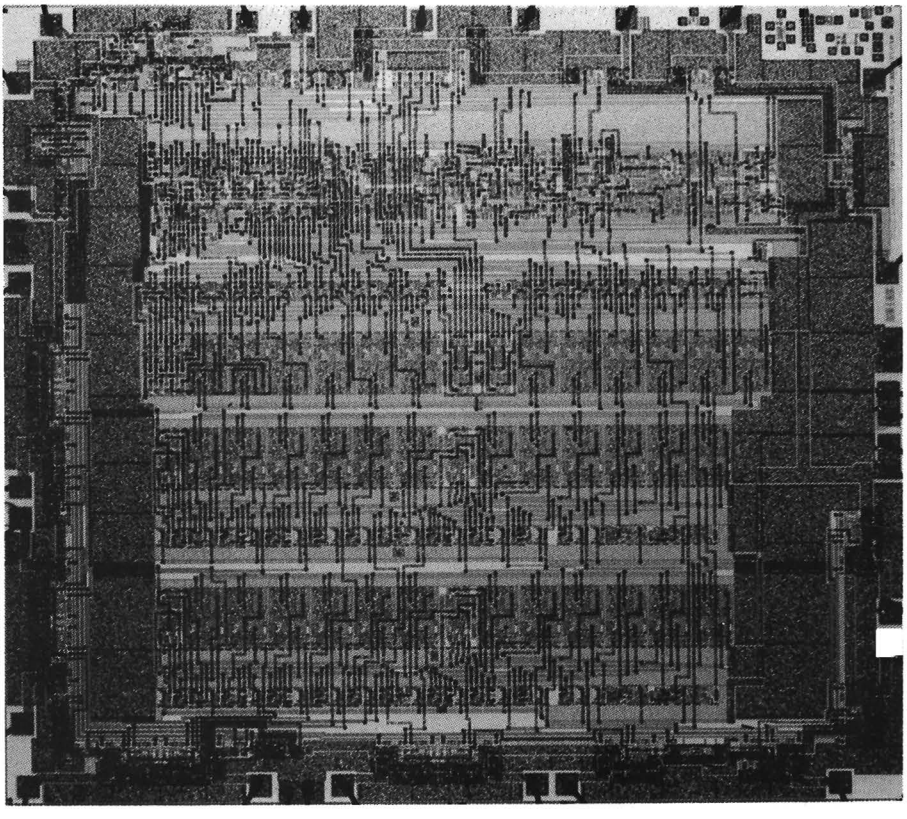

Fig. 6. Chip photograph of the 8X60 (built-up with the ISL-CCL library).

An example of a chip built with the ISL-CCL library is the 8X60 (design: P. Keller) [7], which is an integrated circuit that can convert standard random-access memories into large first-in, first-out buffer memories. With the 8X60 FIFO RAM controller, two asynchronous systems may be interconnected for buffered data-transfer rates exceeding 8 MHz. The 8X60 supplies an address up to 12 bits long to a user-selected RAM of the desired data width. FIFO depth is selectable by two control signals to any of four word values: 64, 256, 1024 and 4096. A four-signal handshake interface is provided for read and write control from the two communicating systems, as well as status signals to indicate the full, half-full, and empty conditions.

The chip inputs and outputs are standard TTL. Fig. 6 shows a photograph. The chip-size is 25 mm^2, the number of ISL equivalent gates is 564. One additional external dropping resistor of 56 Ω connected to the 5V power supply can be used to obtain the ISL power supply voltage of 1.5V. The typical chip power dissipation is
80 mA·5V + 63 mA·1.5V ≈ 500 mW.

E. The 8A1200 (designed by D. Goddard and R. Bindt).

The 8A1200 ISL gate array is an uncommitted logic array (or masterslice) of 1200 NAND-gate equivalents featuring up to 10 inputs and 4 outputs per gate [5,8,9]. This gate array offers circuit designers the ability to create custom LSI circuits of up to 1200 gates, with a short turn-around time.

Each 4-nanosecond gate uses 168 μW of power and the speed-power product of each gate is 0.7 pJ. Logic functions are defined by the user and are implemented by interconnecting 1144 ISL gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 36 LSTTL I/O buffers can be specified.

To realize the groundrail and the power supply rail in the first layer of metallization, the layout of the gate is different from the layout described in section 4 (see Fig. 7).

The wafers are prediffused up to the emitter-diffusion, and stocked. Customization starts with the contact holes for the first layer metallization to form ohmic contacts and Schottky diodes. Fig. 8 shows a detail of the chip just after etching the contact holes; the same detail is shown in Fig. 9 after the etching of the first layer metal. Figs. 8 and 9 show that the packing density of the gates is not maximized; enough space is left around the gates for routing of the metallization to achieve 100% routibility.

All gates have a direct input and a resistor input (see Fig. 7). As shown in Fig. 10 resistor inputs can be interconnected, without current hogging problems, to be driven from an internal Schottky buffer for clock distribution; this is an alternative approach to the clock distribution in the 3422A and OQ4100N1.

Fig. 11 shows an edge of the chip with bonding pads and I/O circuits. The metallization determines whether a buffer is an input or an output circuit (the diffusions allow both types).

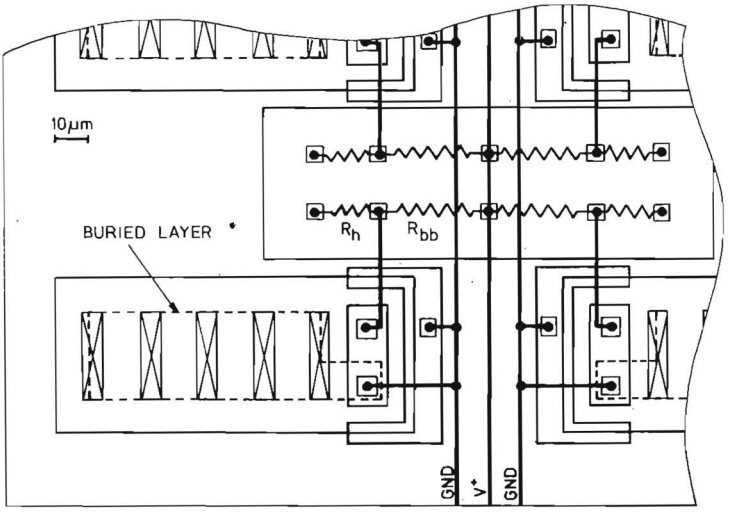

Fig. 7. Lay-out of the ISL gates in the 8A1200 gate array.

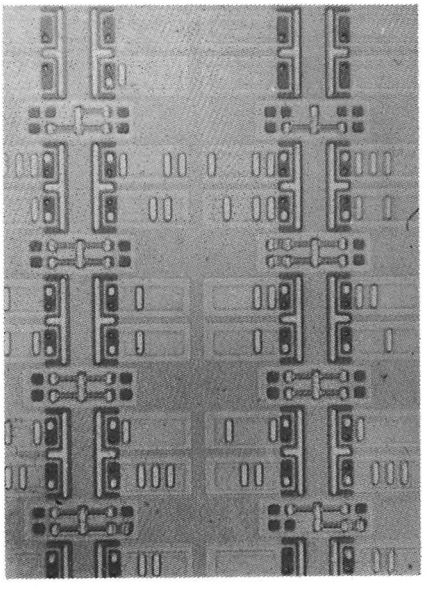

Fig. 8. Detail of the 8A1200 after etching of the contact holes.

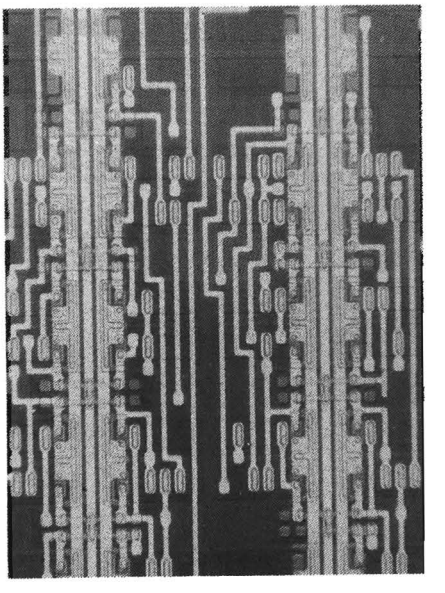

Fig. 9. Same detail as Fig. 8, after etching of the first layer metallization.

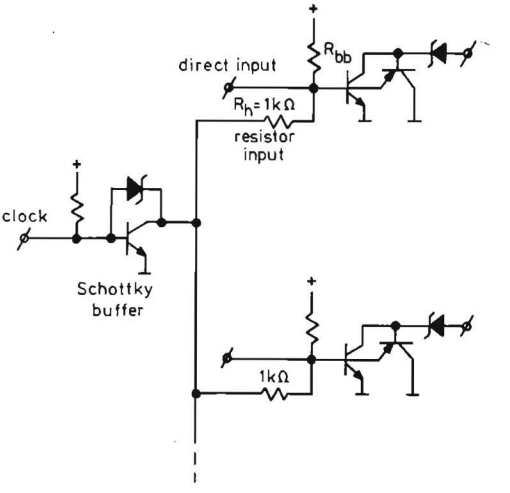

Fig. 10. Clock distribution circuitry on the 8A1200 with Schottky buffers and anti-current-hogging resistor inputs.

Fig. 12 shows a photograph of the total 8A1200 chip (25 mm^2), with an evaluation metallization on top to realize representative logic functions as a 8 to 1 multiplier, a 4-bit adder, a 4-bit universal shift register. Also the following test circuits are made: a D-flip-flop wired as a toggle flip-flop, demonstration of fan-out effects on ISL gates,

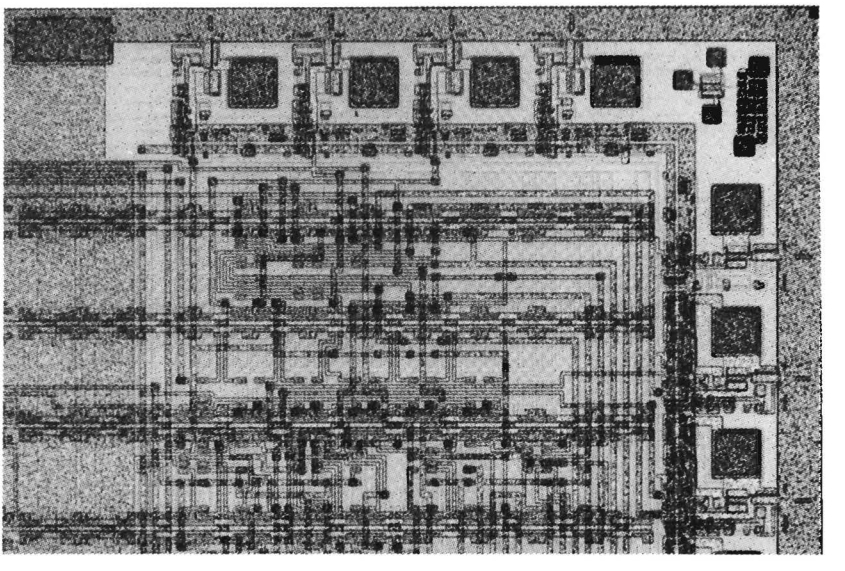

Fig. 11. Detail of the 8A1200 (I/O buffers and part of the ISL gates).

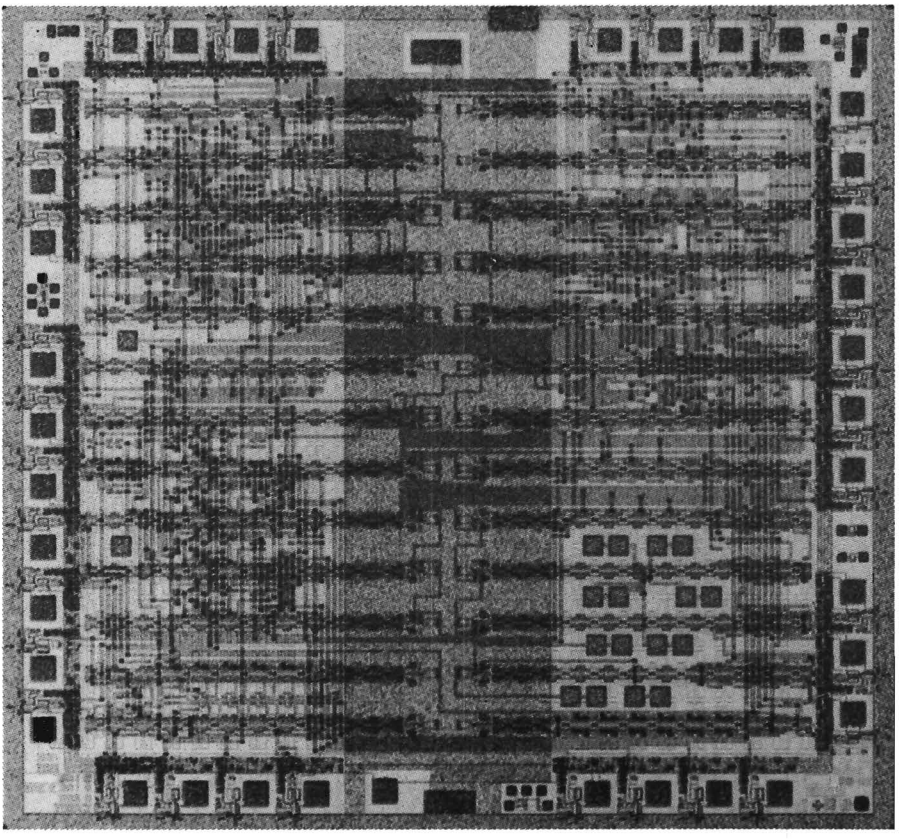

Fig. 12. Chip photograph of the 8A1200 gate array.

test of a fan-in and pattern sensitivity effects on ISL gates, and ring oscillators which show the basic gate delays of ISL gates and Schottky buffers under various lay-out and logical conditions.

In appendix B, the main characteristics and specifications of this gate array are summarized.

REFERENCES

[1] R. Allen, "Input chip sharpens, widens frequency-counter range", *Electronic Design*, March 31, p. 104, 1981.
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[3] J. van der Windt (interview), "Single-chip counter uses two logic types", *Electronics*, June 2, p. 42, 1981.
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[5] J.G. Posa, "Gate arrays, a special report", *Electronics*, pp. 145-158, September 25, 1980.
[6] Signetics CCL design manual.
[7] "8X60 controller converts RAM into first-in, first-out buffer", *Electronics*, July 14, 1981.
[8] S.Y. Landau, "Integrated Schottky Logic gate array", *Microelectronics*, vol. 11, pp. 5-11, 1980.
[9] Signetics 8A1200 gatearray design manual.

Appendix B

PRODUCT DESCRIPTION

The 8A1200 Gate Array (Figure 1) is an uncommitted array of ISL gates (Figure 2), Schottky buffers (Figure 3) and LSTTL-compatible I/O cells (Figures 4 and 5). Thus, up to 1200 gates can be custom interconnected to provide the advantages of both Large Scale Integration (LSI) and proprietary design. The 8A1200 array is based on a technological subset of LSI called ISL (Integrated Schottky Logic). ISL combines the best features of low-power Schottky and I^2L Bipolar technologies.

Designing with the 8A1200 is easy and fast, requiring no more than conventional logic design, logic simulation, and custom coding of metal interconnections among preprocessed logic gates on the array. The design techniques and the implementation processes are analogous to the design of a Printed Circuit Board.

Logic functions are defined by the user and are implemented by interconnecting 1144 ISL NAND gates, using two layers of metal routing. Fifty-two Schottky buffers are provided to drive multi-load internal clock or enable signals. For external interface, up to 36 LSTTL I/O buffers can be specified. As shown in Figure 5, each I/O can be configured to implement any one of 11 different functions: inputs, input/output, totem-pole, open collector, and three-state.

FEATURES

- Customer programmable LSI
- 1144 ISL (NAND) gates
- Two-layer metal interconnection
- 52 Schottky buffers
- 36 I/O buffers
- LSTTL compatible
- Standard PNP inputs
- 8mA output current sink
- -55°C to + 125°C ambient temperature
- 4ns gate speed (typical)
- Speed-power product—0.7 picojoules
- 22, 28, 40, or 44-pin package

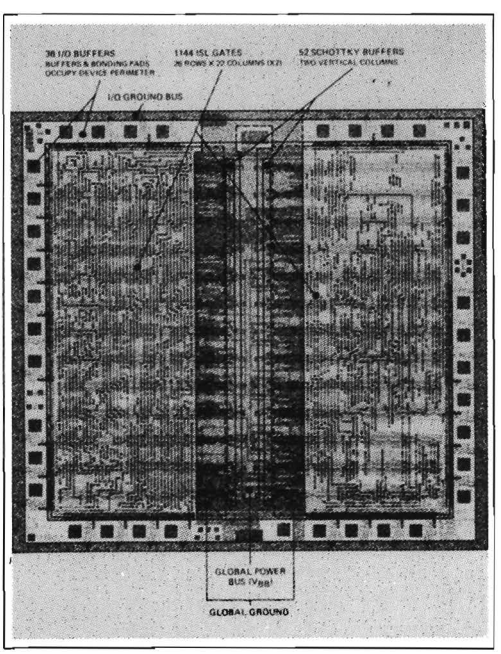


Figure 1. Internal Configuration of 8A1200 ISL Gate Array

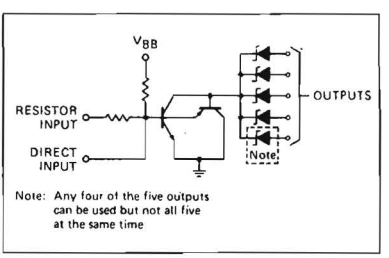


Figure 2. ISL Gate—Schematic Diagram

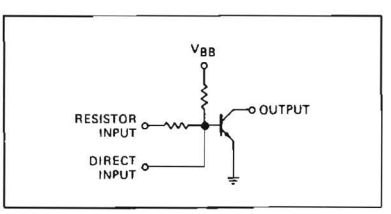


Figure 3. Schottky Buffer—Schematic Diagram

signetics

INPUT/OUTPUT CELLS

All signals within the array interface to external pins via I/O buffers located around the device perimeter. A description of each I/O cell, including the symbolic representation, is shown below. The logic and schematic representation of each I/O cell are shown, respectively, in Figures 4 and 5.

Symbol	Description
INB	Input buffer
AP	Active pull-up output
OC	Open-collector output
EOC	Open-collector output with enable
TS	Three-state output
TOC	Open-collector transceiver
TEOC	Open-collector transceiver with enable
TTS	Three-state transceiver
IOCD	Internal driver to three-state bus
EOCD	External driver to three-state bus
IOD	Internal driver and input driver

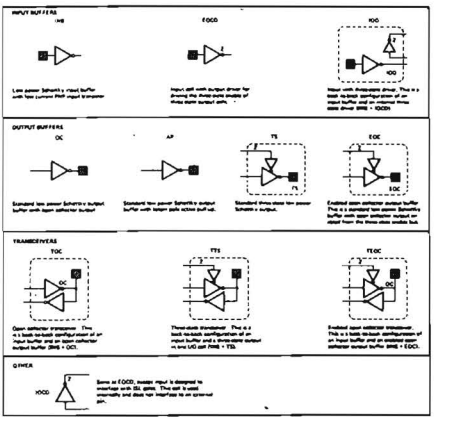


Figure 4. Logic Representations for Eleven I/O Cells

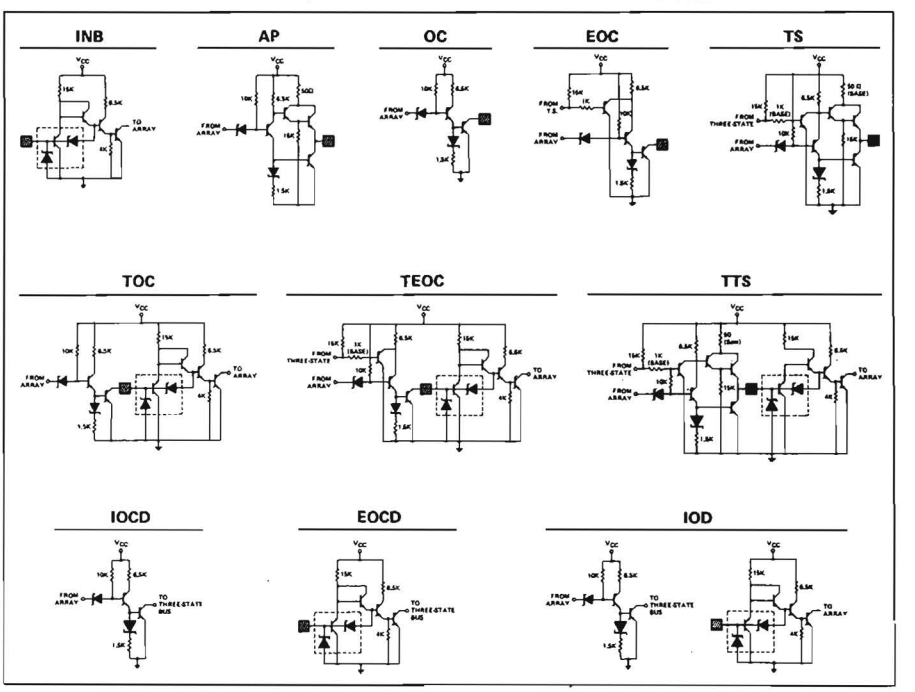


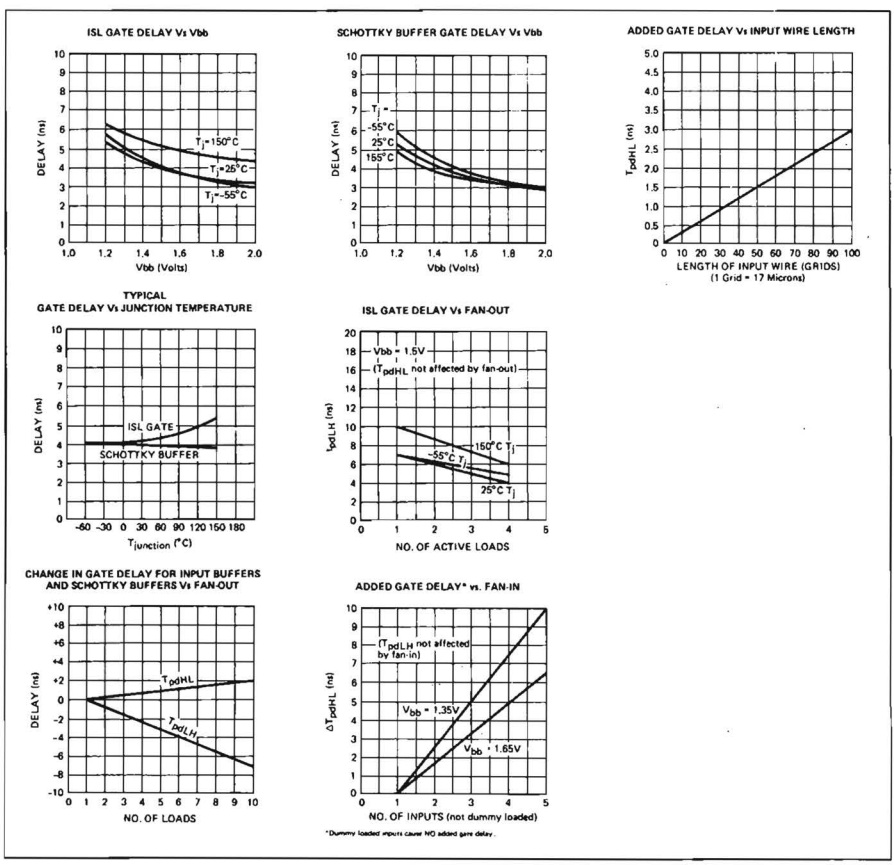
Figure 5. Schematic Representations for Eleven I/O Cells

TYPICAL PERFORMANCE CHARACTERISTICS

Overall performance of the gate array is determined by the following parameters:

- Discrete gate delays
- Gate current (I_{BB}) and gate voltage (V_{BB})
- Junction Temperature (T_J)

Gate delays are subject to several variables, any one of which can affect the overall circuit performance. An analysis of these variables is shown in the accompanying graphs.



POWER DISSIPATION

For the purpose of package selection, the maximum power dissipation for any given implementation of the 8A1200 gate array is given by the following equation.

Maximum Power (in mW) = 0.25 mW x number of ISL
plus, 0.25 mW x number of Schottky buffers used
plus, 12 mW x number of TTS, TOC, and TEOC buffers
plus, 8 mW x number of AP, OC, EOC, TS and IOD buffers
plus, 5 mW x number of EOCD, INB, and IOCD buffers
plus, 0.5)V x load current (in mA) of output buffers

(Note. Load current = maximum I_{OL} for selected temperature range x the total number of output buffers and transceivers that can simultaneously be at a low output state.)

AC AND DC ELECTRICAL CHARACTERISTICS

CONDITIONS:

Commercial—
V_{CC} = 5.0V (±5%)
V_{BB} = 1.5V(±10%)
T_a^1 = 0°C to 70°C

Military—
V_{CC} = 5.0V (±10%)
V_{BB} = 1.5V(±10%)
T_a^1 = -55°C to 125°C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	DESCRIPTION	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V
V_{BB}	ISL gate supply voltage	+7.0	V
E_{IN}	Input voltage, continuous	-0.5 to +5.5	V
I_{IN}	Input current, continuous	-30 to +1.0	mA
V_O	Voltage applied to open-collector output in off-state	-0.5 to +7.0	V
T_A	Ambient temperature, operating	-55 to +125	°C
T_{STG}	Storage temperature	-65 to +150	°C

ISL GATE (Internal)

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{BB}/G	Power supply current per gate		74	112	164	65	112	164	μA
ILF	Input load factor					1		1	Unit load
FO	Fanout							4	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan-in = one (1) ISL gate or Schottky buffer Fan-out = one (1) ISL gate or Schottky buffer				2	4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation					1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay						7	10	ns

SCHOTTKY BUFFER (Internal)

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{bb}/G	Power supply current per gate		74	112	164	65	112	164	μA
ILF	Input load factor					1		1	Unit load
FO	Fanout							10	Unit load
t_{pdAV}	Average gate propagation delay $t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan in = one (1) ISL gate or Schottky buffer Fan out = one (1) ISL gate or Schottky buffer				2	4	6	ns
$t_{pdHL}2$	High-to-low propagation delay	Delay is inferred from circuit simulation					1	2	ns
$t_{pdLH}2$	Low-to-high propagation delay						7	10	ns

[illegible]: IOD, IOCD (Internal)

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	IOCD power supply current	From array = high	0.70	0.95	1.35	0.65	0.95	1.45	mA
	IOD power supply current	VIN = 3V, from array = high	1.30	1.75	2.50	1.20	1.75	2.65	mA
ILF	Input load factor					3			Unit load
FO	Fanout	(drives 3-state inputs only)						16	
t_{pdAV}	Average propagation delay	Fan in = one (1) ISL gate or Schottky buffer					10	14	ns
	$t_{pdAV} = \frac{t_{pdLH} + t_{pdHL}}{2}$	Fan out = one (1) from three state input of an output buffer							

[illegible]: INB, EOCD, TEOC[3] (to array), IOD (to array), TOC (to array), TTS

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	TOC, supply current	V_{IN} = 3V, from Array = L	0.90	1.20	1.75	0.85	1.20	1.80	mA
	INB, EOCD, supply current	V_{IN} = 3V	0.60	.80	1.15	0.55	.80	1.20	mA
	IOD, supply current	V_{IN} = 3V, from Array = H	1.30	1.75	2.50	1.20	1.75	2.65	mA
	TEOC, supply current	V_{IN} = 3V, from TS = H, from Array = L	1.65	2.20	3.10	1.55	2.20	3.30	mA
	TTS, supply current	From Array = L, from TS = H V_{IN} = 3V	1.65	2.20	3.10	1.55	2.20	3.30	mA
VTH	Input threshold voltage					0.80		2.0	V
VCD	Input clamp diode voltage	I_{IN} = –18mA						–1.5	V
I_{IL}	Input low current	V_{IN} = 0.4V						–20	µA
I_{IH}	Input high current	V_{IN} = 2.7V						20	µA
I_I	Max input high current	V_{IN} = 5.5V, Vcc = Max						100	µA
FO	INB & IOD "to array" outputs							10	Unit load
	EOCD & IOD "to three-state" outputs							16	Unit load
t_{pdLH}	Propagation delay, low-to-high F.O. = one (1) ISL load						5	8	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = one (1) ISL load						2	4	ns
t_{pdLH}	Propagation delay, low-to-high F.O. = ten (10) ISL loads	(see fig. 16)					3	4	ns
t_{pdHL}	Propagation delay, high-to-low F.O. = ten (10) ISL loads						4	5	ns

[illegible] BUFFER: AP (Active Pullup)

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current	From array = high	0.70	0.95	1.35	0.65	0.95	1.45	mA
ILF	Input load factor					3			Unit loads
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4mA						400	mV
V_{OH}	Output high voltage	I_{OH} = -400µA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V				-15		-100	mA
t_{pdLH}	Propagation delay, low to high output	R_L = 2K C_L = 15pf					4	8	ns
t_{pdHL}	Propagation delay, high to low output	(see fig. 16)					4	8	ns

OPEN COLLECTOR, OUTPUT BUFFERS: OC, TOC (from array), EOC, TEOC

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	OC power supply current	From array = high	0.70	0.95	1.35	0.65	0.95	1.45	mA
	TOC power supply current	From array = low	0.90	1.20	1.75	0.85	1.20	1.80	mA
	EOC power supply current	From array = low, From T.S. = high	1.05	1.40	1.95	1.00	1.40	2.10	mA
	TEOC power supply current	From array = low From T.S. = high	1.65	2.20	3.10	1.55	2.20	3.30	mA
ILF	Input load factor "from array"					3			Unit load
	Input load factor "from T.S."					3			Unit load
VOL	Output low voltage	I_{OL} = 8mA comm			500				mV
		I_{OL} = 4mA						400	mV
IOH	Output high current	V_{OUT} = 5.5V						20	µA
t_{pdLH}	Propagation delay low to high output	R_L = 2K C_L = 15pf					9	TBD	ns
t_{pdHL}	Propagation delay high to low output	(see fig. 17)					8	TBD	ns

THREE-STATE OUTPUT BUFFERS: TS, TTS (from array)

PARAMETER	DESCRIPTION	TEST CONDITIONS	LIMITS (COMMERCIAL)			LIMITS (MILITARY)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	TS power supply current	From T.S. = high From array = low	1.05	1.40	1.95	1.00	1.40	2.10	mA
	TTS power supply current	From array = low VIN = 3V, from R.S. = high	1.65	2.20	3.10	1.55	2.20	3.30	mA
ILF	Input load factor, either input					3			Unit load
V_{OL}	Output low voltage	I_{OL} = 8mA			500				mV
		I_{OL} = 4MA						400	mV
V_{OH}	Output high voltage	I_{OH} = -400µA	2.7			2.5			V
I_{OS}	Output short circuit current	V_{OUT} = 0V				-15		-100	mA
I_{OLZ}	Three-state off current, output low	V_{OUT} = 0.4V						-20	µA
I_{OHZ}	Three-state off current output high	V_{OUT} = 2.4V						20	µA
t_{pdLH}	Propagation delay, low to high output	R_L = 2K					4	9	ns
t_{pdHL}	Propagation delay, high to low output	C_L = 15pf					6	10	ns
t_{pdZL}	Propagation delay, HI Z to low output	(see fig. 18)					11	14	ns
t_{pdZH}	Propagation delay, HI Z to high output	R_L = 2K, C_L = 15 pf (see fig. 18)					10	13	ns
t_{pdLZ}	Propagation delay, low to HI Z output	R_L = 2K					6	12	ns
t_{pdHZ}	Propagation delay, high to HI Z output	C_L = 15 pf (see fig. 18)					7	7	ns

Notes:

1. Maximum power dissipation limit of circuit is determined by package selection.
2. Guaranteed value is L_{pdAV}.
3. For all input parameters on TEOC and TTS, the "from Three-State" input should be high.

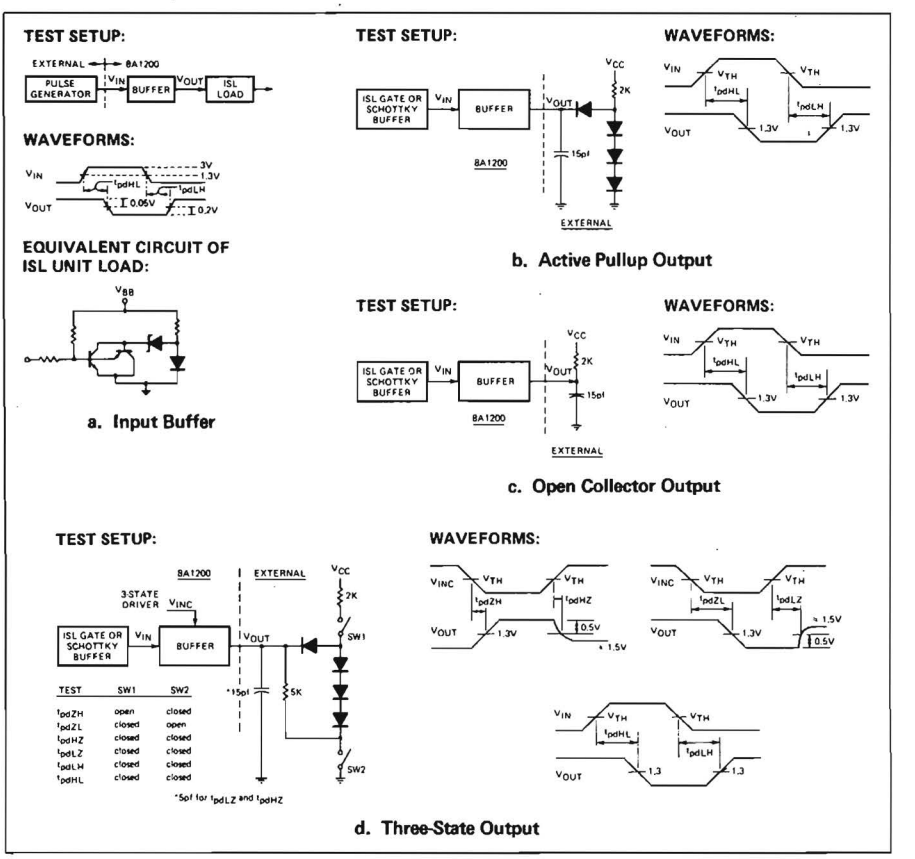


Figure 6. Test Circuits

ORDERING INFORMATION

For additional information on the 8A1200 and other Gate Array products from SIGNETICS, contact your nearest Sales Office.

Summary

Integrated Schottky Logic (ISL) is a new logic gate (with a 200 mV voltage swing) for LSI and VLSI circuits, which can be made in standard bipolar processes. It has been developed to bridge the gap between Integrated Injection Logic (I^2L), which has VLSI capabilities but not a very high speed, and low-power Schottky TTL, which features a good speed but consumes too much chip area and too much power.

The ISL circuit concept is similar to Schottky Transistor Logic (STL) except for the Schottky clamp diode which is replaced by a merged p-n-p transistor, consisting of a combination of a vertical and a lateral p-n-p transistor; the n-p-n transistor is used in the normal downwards mode.

The max. speed of ISL depends strongly on the cut-off frequency of the clamp p-n-p transistor. In a standard pn-isolated buried collector process with a 3 μm epilayer and 5 μm min. details, the cut-off frequency of the combined vertical/lateral p-n-p transistor is about 100 MHz, and the min. propagation delay time of ISL is 2 ns at 500 μA per gate (which is at least five times faster than I^2L made in the same process). At 200 μA per gate the propagation delay time is 2.7 ns.

In a standard oxide-isolated process with 1.2 μm epilayer and 3 μm min. details the relative slow lateral p-n-p transistor is eliminated, resulting in a p-n-p cut-off frequency of about 600 MHz and a min. ISL propagation delay time of 0.6 ns at 500 μA per gate (at 200 μA per gate the propagation delay time is 0.7 ns; at 100 μA per gate 1.0 ns).

Due to the separate load device (resistor or lateral p-n-p transistor in a separate island) the packing density of ISL is about 60% of the packing density of I^2L.

Extended measurements on ISL structures in the pn-isolated process and the oxide-isolated process are carried out. Speed comparisons are made with I^2L and STL.

Analytical expressions of the propagation delay times of ISL and STL are derived. It turns out that oxide-isolated STL is marginally faster than oxide-isolated ISL at the cost of higher process complexity.

First-order models of pn-isolated and oxide-isolated ISL-gates are obtained.

Further the static and dynamic noise margins of logic circuits in general and of ISL in particular are investigated experimentally, by computer simulation, and analytically. Also the temperature behaviour of the static noise margins of ISL and STL structures are derived analytically and by computer simulation.

Finally ISL applications are discussed such as a shift-register chip, a pipeline--multiplier, a counter chip, a custom cell lay-out-library and a gate array.

Samenvatting

Integrated Schottky Logic (ISL) is een nieuwe logische poort (met een 200 mV logische slag) voor LSI en VLSI circuits, en kan gemaakt worden in standaard bipolaire processen. ISL is ontwikkeld om een tussen-oplossing te bieden tussen Integrated Injection Logic (I^2L), dat VLSI-mogelijkheden heeft maar een relatief lage schakelsnelheid heeft, en low-power Schottky TTL, dat een goede schakelsnelheid heeft, maar te veel chip-oppervlak bezet en te veel vermogensdissipatie bezit.

Het ISL circuit-concept is in principe gelijk aan dat van Schottky Transistor Logic (STL), behalve het clamp-device dat in ISL bestaat uit een geïntegreerde p-n-p transistor, bestaande uit de combinatie van een verticale en een laterale p-n-p transistor; de n-p-n transitor wordt op normale wijze bedreven (emitter boven, collector beneden).

De maximale schakelsnelheid van ISL hangt sterk af van de afsnijfrequentie van de clamp p-n-p transistor. In een standaard pn-geïsoleerd proces met een 3 μm dikke epitactische laag en 5 μm minimum lithografische details, is de afsnijfrequentie van de gecombineerde verticale/laterale p-n-p transistor ongeveer 100 MHz, en de minimale poortvertragingstijd van ISL is 2 ns bij 500 μA per poort (dit is ten minste 5 maal korter dan van I^2L gemaakt in het zelfde proces). Bij 200 μA per poort is de poortvertragingstijd 2,7 ns.

In een standaard oxide-geïsoleerd proces met een 1,2 μm dikke epitactische laag en 3 μm minimum lithografische details wordt de relatie langzame laterale p-n-p transistor geëlimineerd, waarmee een afsnijfrequentie van de (verticale) p-n-p transistor van ongeveer 600 MHz wordt verkregen en een minimale poortvertragingstijd van 0,6 ns bij 500 μA per poort wordt bereikt (0,7 ns bij 200 μA per poort en 1,0 ns bij 100 μA per poort).

Door het gescheiden belastingselement (weerstand of laterale p-n-p transistor) is de pakkingsdichtheid van ISL ongeveer 60% van de pakkingsdichtheid van I^2L.

Uitgebreide metingen zijn gedaan aan ISL structuren in het pn-geïsoleerde proces

en het oxide-geïsoleerde proces. Schakelsnelheidsvergelijkingen zijn gemaakt met I^2L en STL. Analytische uitdrukkingen voor de poortvertragingstijden van ISL en STL zijn verkregen. Het blijkt dat oxide-geïsoleerd STL marginaal sneller is dan oxide-geïsoleerd ISL ten koste van een hogere proces-complexiteit.

Eerste orde modellen van pn-geïsoleerde en oxide-geïsoleerde ISL poorten zijn ontworpen.

Verder zijn, d.m.v. experimenten, computer simulaties en berekeningen, de statische en dynamische storingsmarges onderzocht van logische circuits in het algemeen en ISL in het bijzonder. Ook is de temperatuur-afhankelijkheid van de statische storingsmarges van ISL en STL onderzocht d.m.v. computer simulaties en berekeningen.

Ten slotte worden een aantal ISL toepassingen besproken zoals: een schuifregisterchip, een pijplijn-vermenigvuldiger, een teller-chip, een custom lay-out bibliotheek en een gate array.

Curriculum Vitae

11 juli 1946	geboren te 's-Gravenhage.
sept. 1958 – juli 1963	Rijks-HBS "Willem II" te Tilburg.
sept. 1963 – jan. 1970	T.H. Delft, studie technische natuurkunde (afstudeeronderwerp : elektronica voor NMR-apparatuur).
jan. 1970 – juni 1970	Ingenieur-assistent, werkgroep Magnetische Resonantie, afd. Technische Natuurkunde T.H. Delft.
juli 1970	Wetenschappelijk medewerker Philips Natuurkundig Laboratorium te Eindhoven. Onderwerpen: – geïntegreerde magnetische geheugens – digitale silicium-IC imagers voor optische geheugens – ontwerpen, modelleren en toepassen van silicium VLSI componenten en schakelingen t.b.v. digitale logica en geheugens zoals: I^2L, ISL, punch through devices, thysistor devices, etc.
	Het werk beschreven in dit proefschrift vond plaats in de jaren 1976 - 1981.

STELLINGEN

behorende bij het proefschrift van J. Lohstroh

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I

Onder de "punch-through"-spanning van een npn- of pnp-transistor dient de waarde te worden verstaan van de collector-emitterspanning waarbij de collector-basisdepletielaag de emitter-basisdepletielaag raakt, onder de conditie $V_{BE} = 0$.

J. Lohstroh et al., *Solid-State Electronics*, vol. 24, no. 9, pp. 805-814, Sept. 1981.

II

De idealiteitsfactor van het exponentiële deel van de stroom-spanningskarakteristiek van n^+pn^+- en p^+np^+-structuren in de toestand van "punch-through" is groter dan 2.

———, *Solid-State Electronics*, vol. 24, no. 9, pp. 815-820, Sept. 1981.

III

Een "punch-through"-structuur leent zich goed voor toepassing als compact belastingselement in translineaire circuits.

J. Lohstroh, *IEEE J. Solid-State Circuits*, vol. SC-14, no. 5, pp. 840-844, Oct. 1979.

IV

Met het naar standaardsimulatieprogramma's getransformeerde "lumped transistor model" van Linvill kan op relatief eenvoudige wijze het ruimtelijke en dynamische gedrag van minderheidsladingdragers in transistoren worden gesimuleerd.

———, *IEEE J. Solid-State Circuits*, vol. SC-12, no. 2, pp. 176-184, April 1977.

V

De door Poorter als "figure of merit" van een logische poort gedefinieerde energie-storingsmarge is niet noodzakelijkerwijs gelijk aan de energie die nodig is om een logische poort te storen.

T. Poorter, *IEEE J. Solid-State Circuits*, vol. SC-12, no. 5, pp. 440-449, Oct. 1977.

VI

Hoewel er over I^2L enorm veel theorie gepubliceerd is, is het doorbreken van de 1ns-grens voor de poortvertragingstijd bereikt door het toepassen van inzichten die reeds kort na de uitvinding van I^2L bekend waren, zoals:

a) het dunner maken van de epitactische laag en het toepassen van oxide-isolatie,
b) het beperken van het extrinsieke gebied van de inverse npn-transistor,
c) het beheersen van de inverse stroomversterking van de npn-transistor d.m.v. injectie terug in de injector.

D.D. Tang et al., *IEEE IEDM 1979 Dig. Tech. Papers*, pp. 201-204, Dec. 1979.

VII

In alle tot dusver over I^2L gepubliceerde theorie is verzuimd de laterale diffusie te beschouwen van gaten in de emitter van de inverse npn-transistor.

VIII

In het alpinisme kunnen meer mensenlevens worden gespaard door, in aanvulling op de bestaande informatie over de objectieve alpiene gevaren in boeken, tijdschriften en gidsjes, langs de aanlooproutes naar veelbezochte berggebieden borden te plaatsen met informatie over de specifieke objectieve gevaren van het betrokken gebied.

IX

Om vervuiling van de bergen door massarecreatie verder te voorkomen, en om aan de primitiviteitsbehoefte van bergbeklimmers te blijven voldoen, dient men op te houden met het "bewirtschaften" van steeds meer berghutten.

X

Het door luidsprekers ten gehore brengen van – zogenaamd functionele – achtergrondmuziek in winkels, vliegtuigen, liften, hotels, restaurants en andere openbare gelegenheden is een inbreuk op de menselijke vrijheid en dient te worden verboden.

Eindhoven, november 1981.