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A 107GHz LNA in 65nm CMOS with Inductive Neutralization and Slow-Wave Transmission Lines

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Abstract— This paper presents a 107GHz LNA prototype using TSMC 65nm CMOS technology. It explores the limit of the CMOS technology by effectively optimizing the active and passive devices. An improvement of 1.6dB higher maximum stable/available gain (MSG/MAG) on the transistor is achieved around 110GHz by layout optimization and inductor neutralization technique. A high quality factor co-planar waveguide (CPW) transmission line is designed utilizing the slow-wave effect. A quality factor of 23.6 is demonstrated by EM-simulations while taken the consideration of satisfying the stringent layout design rules. Based on the optimization on the active and passive devices, a dual-stage LNA is designed, with a simulated power gain of 10.2dB and noise figure of 8dB at 107GHz, verified by chip-level EM-simulations. The power consumption is 28.2mW.

I. INTRODUCTION

Radio applications, such as high-rate communication links, automotive radars and imaging systems, lead to the use of millimeter-wave (mm-wave) frequencies. Compared to III-V technologies, CMOS has obvious advantages in terms of relatively low cost, high yield, continuous scaling, and potential of full integration with digital circuits. However, the front-end design using CMOS technology in mm-wave range, especially for frequencies above 100GHz, is rather challenging. Firstly, the available gain in the device degrades significantly and becomes very limited beyond 100GHz. Secondly, passive devices have higher loss due to the high frequency resistive loss and the conductive substrate in CMOS technologies. This extra loss in the matching networks further limits the front-end's performance at mm-wave range.

This paper explores the possibility of mm-wave LNA design in CMOS above 100GHz, with solutions to the afore-mentioned challenges. Section II presents the layout optimization; Section III compares four neutralization techniques in terms of gain enhancement; Section IV presents the design of the slow-wave CPW transmission line with high quality factor. In section V, outcomes of the previous two sections are used in a 107GHz two-stage LNA design. Chip-level EM-simulation results will be presented. The paper ends with a conclusion in section VI.

II. TRANSISTOR LAYOUT OPTIMIZATION

Optimizing the active devices used in LNA design starts by

optimizing the two metrics f_{max} and NF_{min} which denote the potential of the devices. Assuming the source resistance is much smaller than the gate resistance, which is reasonable in the used technology, f_{max} can be written as [1]:

$$f_{max} = \frac{f_t}{2\sqrt{r_g (g_{ds} + 2\pi f_t C_{gd})}} \quad (1)$$

where r_g is the total gate resistance and f_t is the unity current gain frequency. We see that f_{max} is sensitive to the layout and more dependent on the resistive parasitic r_g . For a common-source (CS) connected transistor, the minimum noise factor (NF_{min}) for high frequencies can be derived utilizing the ABCD matrix. Based on the hybrid- π model, the minimum noise factor (F_{min}) can be derived as:

$$F_{min} = 1 + 2G \cdot r_g + 2\sqrt{G \cdot r_g (G \cdot r_g + 1)} \quad (2)$$

where,

$$G = \gamma \cdot g_m \cdot \frac{\omega^2 (C_{gs} + C_{gd})^2}{\omega^2 C_{gd}^2 + g_m^2}$$

where $r_g > 0$, and γ is a technology constant relating to the channel noise of the device. At low frequencies, G is a small value, but as frequency approaches the mm-wave region, G can no longer be neglected, and F_{min} becomes a strong function of gate resistance and gate capacitances.

Although C_{gd} is a limiting factor for both f_{max} and NF_{min} shown in the above equations, it is more of an intrinsic property of the transistor, and cannot be improved significantly by the layout. This implies that r_g is the critical parasitic that needs to be minimized for better gain and noise performance. This resistance consists of poly resistance and wiring resistance in the layout. After decreasing the single finger width to 1 μ m and doubling the number of gate contacts, f_{max} and NF_{min} (at 110GHz) are optimized to about 204GHz and 3.8dB respectively. This optimized transistor layout block will be used in the LNA design in Section V.

III. NEUTRALIZATION TOPOLOGIES

Although Mason gain is optimized by the higher f_{max} , the maximum stable/available gain (MSG/MAG) of the device itself may not be high enough. More gain can be expected with

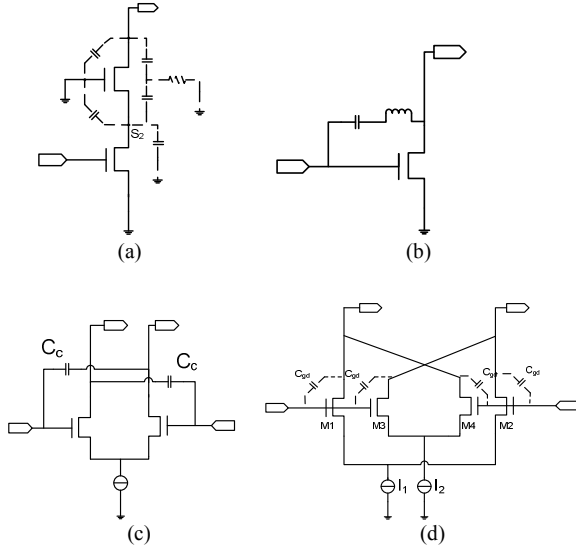


Figure 1. Isolation and neutralization techniques for active devices: (a). Cascode amplifier; (b). Inductor neutralization; (c). Capacitor cross-coupling; (d). Additional differential pair cross-coupling

the help of external circuits for unilateralization. The definition of MSG/MAG suggests that optimization can be done by minimizing S_{12} , i.e. isolating the output and input. This can be done by isolation or neutralizing C_{gd} . Four methods are shown in Fig.1.

In Fig.1(a), the better isolation provided by the common-gate (CG) transistor could increase the power gain and stability factor. But the parasitics of the cascode amplifier become problematic in practical designs. The parasitic capacitors at node S_2 draw current to the ground rather than flowing into the CG transistor. Due to the path through gate capacitance of the CG transistor and the substrate network, the unilateral property of the cascode is no longer valid for mm-wave frequencies. Simulation on a well tuned cascode amplifier shows that the gain improvement only occurs below 100GHz, and the NF is increased significantly by 5dB at 110GHz.

Another method, shown in Fig.1(b), uses an inductor

connected between gate and drain to neutralize C_{gd} . The resonance provides good isolation within a limited frequency range. A capacitor in series with the inductor is added for DC de-coupling. The size of the inductor may be impractically large at lower frequencies (e.g. below 10GHz), but for 110GHz, an inductor of around 120pH is enough for neutralization, which makes this technique reasonable. Simulation shows that there is a 1.6dB increase on the MSG/MAG, although the NF is worsened by 0.9dB. A drawback is that the neutralization may be dependent on the process spread, which will be shown by corner simulations that it only has a minor impact on the performance in Section V.

Neutralization can also be implemented with the use of differential cross-coupling, and two implementations shown in Fig.1(c)(d) are studied. In Fig.1(c), a capacitor pair is cross-coupled connected. In this way, the feedback through C_{gd} in the transistor can be compensated by C_c . To precisely cancel the feedback, C_c must be equal to C_{gd} , which is around 12fF. In the used technology, the small capacitance value is very hard to implement with good precision. This limits the use of this technique. Simulation also shows that the gain improvement only occurs below 110GHz.

The principle of Fig.1(d) is similar to Fig.1(c), while it implements the small capacitor C_c by the additional transistors. If the four transistors share the same size and are biased under the same gate-drain voltage, their C_{gd} will be almost equal. To minimize the current drawn from the output by the extra differential pair, I_2 should be much smaller than I_1 . This implementation achieves the best reverse isolation($S_{12}=-60$ dB). But the gain improvement is only limited to below 90GHz, due to the decrease of the Mason's gain by the extra differential pair. The NF is also deteriorated significantly by 6dB.

The full comparisons of the four techniques are listed in Table.1. We can see that only the inductor neutralization has gain improvement around the wanted frequency, and this will be used in the LNA design. Notice that other three techniques can be useful for lower frequencies, e.g. 60GHz.

TABLE 1. PERFORMANCE COMPARISON ON THE FOUR ISOLATION OR NEUTRALIZATION TECHNIQUES

	SINGLE-ENDED		DIFFERENTIAL	
	Cascode	Inductor neutralization	Capacitor Cross-coupling	Transistor Cross-coupling
Unilateralization range	Wide-band	Within limited frequency range	Wide-band	Wide-band
S_{12} (dB) @ 110GHz	-26	-30	-27	-60
Frequency range for increase of MSG/MAG	Below 100GHz	↑1.6dB @110Ghz	Below 110GHz	Below 90GHz
NF_{min} change(dB) @110GHz	↑↑5 dB	↑0.9 dB	↑1.5 dB	↑↑6 dB
Disadvantages	MSG/MAG decreases at much higher frequencies NF_{min} is greatly increased due to the extra active device	Narrow bandwidth Bias and process spread dependence	Requires very small capacitor, around 12fF No MSG/MAG enhancement at around 110GHz	Mason's gain is decreased, and MSG/MAG enhancement only happens below 90GHz NF_{min} is greatly increased

IV. SLOW-WAVE CPW TRANSMISSION LINE

Transmission lines (TL) are widely used in monolithic high frequency circuits, due to the more predictable performance comparing to lumped elements. While used in matching, a TL of specific electrical length (l_e) is needed to transform the source impedance to certain wanted impedance. So we can derive the total loss in this impedance transformation by:

$$Loss = L \cdot \alpha = l_e \cdot \lambda \cdot \alpha = l_e \cdot \frac{2\pi}{\beta} \cdot \alpha = \pi \cdot l_e \cdot \frac{1}{Q_R} \quad (3)$$

where α and β are the attenuation loss (in dB/mm) and propagation constant (in rad/mm) respectively, and $Q_R = \beta/2\alpha$ is the resonance quality factor. And L (in mm) is the physical length of the TL, which equals to the product of the normalized electrical length (l_e) and the line's wavelength (λ). We see that the total loss in the matching is inversely proportional to Q_R , which is a good metric for the T-line design for matching purpose. In fact, to achieve a higher Q_R , we could decrease the attenuation loss, and/or increase the propagation constant, i.e. decrease the propagation speed.

The floating patterned shields [2] can shield the electric field from penetrating into the lossy substrate, and reduce the attenuation loss. Meanwhile, the patterned shield reduces the signal speed propagating along the line. In total, a high Q_R can

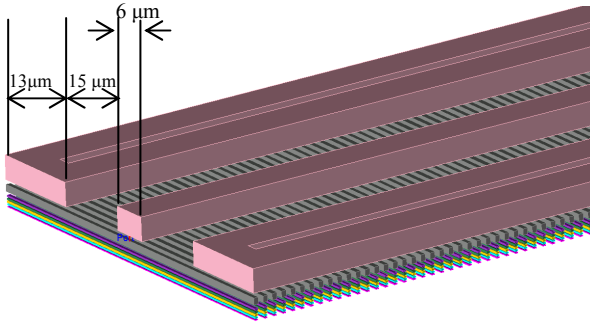


Figure 3. Slow-wave CPW TL with floating patterned shield

be achieved. A 50Ω slow-wave CPW TL with floating patterned shield is designed as shown in Fig.2. The signal and ground plane are in the highest metal layer (M6), while the floating shields are as strips in the next metal layer (M5) to signify the slow-wave effect. The dimensions are shown above the line. Notice that there are dummy slots in the middle of the ground planes and floating dummy strips underneath the M5 strips to satisfy the stringent design rules (metal density) in the used technology and ensure robustness for processing.

The performance is simulated in the EM simulator (ADS Momentum) and results are shown in Fig.3. A characteristic impedance of $48.8\ \Omega$ is achieved around 110GHz . The attenuation loss is 1.56dB/mm , while the wavelength is decreased to 0.74mm from around 1.3mm for a conventional CPW transmission line. Notice that there is a sharp increase in Fig.3(a) after 180GHz . This is due to the simulated length being close to half-wavelength at that frequency, and the extraction method becomes inaccurate. Since the frequency of

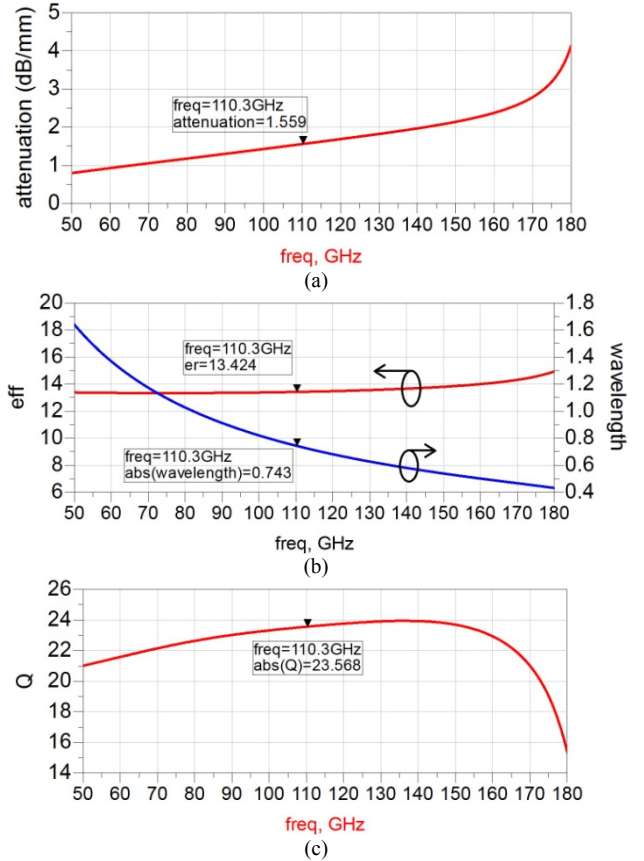


Figure 2. The simulation results on the slow-wave CPW TL. (a). Attenuation loss; (b). Effective dielectric constant and wavelength; (c). Quality factor.

interest is kept away from that range, its influence can be ignored. The quality factor is 23.6 , which makes it a good choice for matching elements in the next section's LNA design.

V. 107GHz TWO-STAGE LNA

Based on the components designed in the last two sections, a two-stage common-source connected LNA is designed, as the schematic shown in Fig.4. Optimized layout and inductor neutralization are used to increase gain in the transistor, and high Q slow-wave CPW TL are used for matching. Basically, a matching network consists of a series line that transfers to the real part of the wanted admittances, and a shunt line further adjusts to the wanted imaginary part. The gate biasing for the first and second stages are optimized for NF and gain respectively, resulting in the biasing shown in Fig.4. The drain biasing of the first transistor and the gate biasing of the second shares the same voltage, i.e. $V_{dd1} = V_{g2}$. This avoids the use of de-coupling capacitor between stages, so eliminating the extra losses and eases the design of matching network.

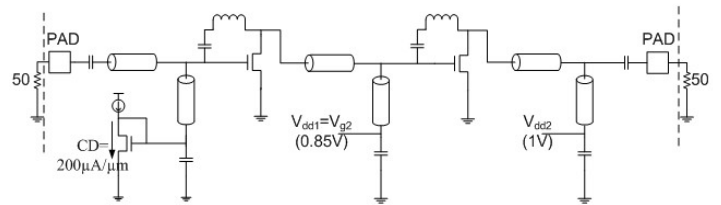


Figure 4. Schematic of the 107GHz two-stage LNA.

In the layout, the connections between components are kept as direct as possible to minimize the parasitics. Meticulous EM-simulations are important to have accurate prediction on the performance [3]. Especially the inductor used for neutralization is adjusted, so that the neutralization functions at the working frequency. The final layout, shown in Fig.5, is adjusted and verified by the chip-level EM-simulation.

The performance based on the chip-level EM-simulation is shown in Fig.6. The power gain is 10.2dB at 107GHz, while

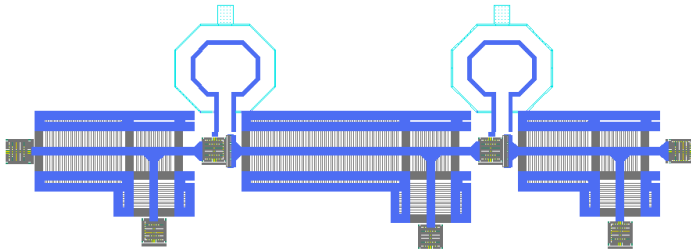


Figure 5. The layout of the two-stage LNA

the return losses at the input and output port are -17.9dB and -28dB respectively. Due to the inductor neutralization, the reverse isolation ($|S_{12}|$) is 41dB. The total noise figure is 8.0dB at 107GHz, and the 1dB compression point is around -5dBm.

The first stage and the second stage draw DC currents of 12mA and 18mA respectively, and the total power consumption is 28.2mW. In Fig.6(a), the corner simulation results are also depicted, to check the performance degradation due to process spread. In the worst case (FF), the gain drops within 1dB and NF increases by only 0.3dB at 107GHz. Enough isolation still exists, since the S_{12} is always below -36dB. Although S_{22} values vary a lot for different corners, they are still well below -15dB around the working frequency. In our design, this influence of the process spread is acceptable.

Comparing to the three recent works at or above 100GHz, shown in Table.2, the LNA in this work provides comparable gain and noise performance, while consuming less power.

VI. CONCLUSIONS

TABLE 2. COMPARISON OF 100GHZ AMPLIFIERS/LNA, IN 65NM CMOS

	[4]	[5]	[6]	This work*
Technology	65nm CMOS	65nm GP CMOS	65nm CMOS	65nm LP CMOS
f_c (GHz)	150	140	100	107
Gain (dB)	8.2	8	13	10.2
NF(dB)	-	-	7.5	8.0
Topology	3CS	3CS+3CG	3CS	2CS
3dB BW (GHz)	27	10	21	16
P_{1dB} (dBm)	1.5	-12	6	-5.0
Matching element	Microstrip	Lumped	CPW	CPW
P_{DC} (mW)	25.5	63	86	28.2

*chip-level EM-simulated results

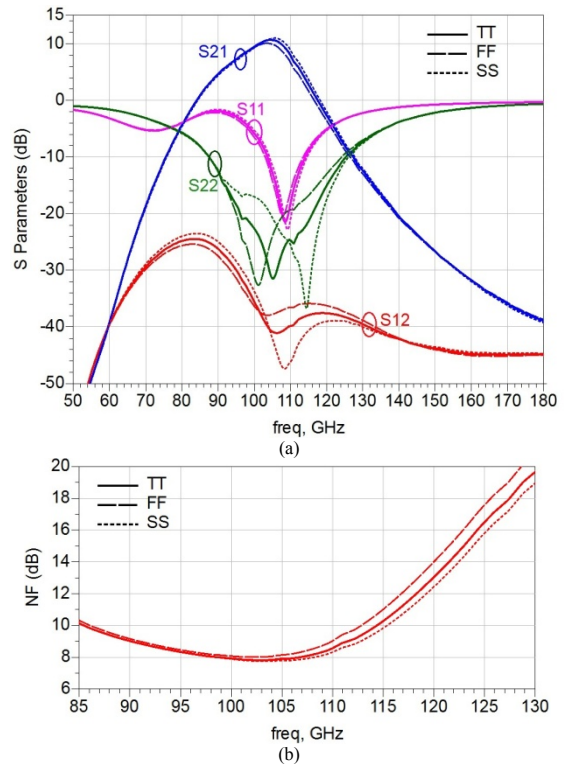


Figure 6. Simulation results of the 107GHz LNA. (a). s-parameters ; (b). noise figure. Corner simulation results are also included.

This paper explored the potential of mm-wave circuit designs above 100GHz in 65nm CMOS technology. It demonstrated useful techniques in the LNA design tackling the challenges in CMOS mm-wave circuits, including: layout optimization which achieved f_{max} of 204GHz and NF_{min} of 3.8dB at 110GHz; inductor neutralization further improves MSG/MAG by 1.6dB; and slow-wave transmission lines with a quality factor of 23.6. Based on these techniques, a 107GHz two-stage LNA is designed achieving 10.2dB power gain and 8dB NF, which are verified by meticulous EM-simulations. The design techniques presented in this paper can be used in the future silicon mm-wave designs above 100GHz.

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