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ON THE DEFINITION OF CRITICAL AREAS FOR IC PHOTOLITHOGRAPHIC SPOT DEFECTS

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Abstract

A closer look at earlier work on IC defect sensitivities reveals that modeling the geometrical patterns only as conductors can be inaccurate in predicting the probability of failure of the circuit. This way of modeling considers also only one layer at a time and neglects any interrelationships, as is the case with transistors. Furthermore, the only kind of faults covered are of the short and break circuit types. We present a generalization that considers the layout as the union of a set of electrical elements and where depending upon the element the patterns have a significance other than simple conductors. This approach models sensitive areas for a larger coverage of faults including stuck-at transistors and possible performance degradations.

INTRODUCTION

The theory of modeling IC photolithographic defect sensitivities has been extensively studied by several authors [1],[2],[3]. In that theory the critical, or sensitive, area was defined as the area where the center of a defect must be situated to cause a fault in the chip. It was found that this area varies as a function of the defect size and of the width and space of the patterns directly involved. This approach neglects those defects which do not cause either a short or a break, yet if the defect falls in the poly-diffusion overlap area of a transistor it can be fatal even if it does not totally break the geometrical pattern.

Missing points in the presentation of the theory up to now are :

+ The calculated critical areas account only for short/break type of faults
+ All the patterns in the layers are considered only as interconnectors, even when in real artworks some portions of those "connectors" are also part of devices like transistors.
+ The effect of layers like the implant-layers of an NMOS process, or the p-well-layers of a CMOS process are not considered.
+ It is a "unilayer" theory, no interdependence between layers is considered, as could be the case of a poly-metal via where three different layers are involved.

Nevertheless the model is good to evaluate the safetiness of the artwork as a function of the probability of failure of its layers, that is, whether the patterns can undesirably be broken or joined. Nowadays, in VLSI yield simulations it is also desirable to find the sensitivity of the electrical circuit as a function of its complete layout, and not only the sensitivity of the layout as a function of its layers.

This paper presents a broader approach to the modeling of sensitive areas. The model that will be presented is a generalization of the existing theory. The sensitive areas that we find are a function of the geometrical patterns in the layers, of their electrical significance, of their relationship to patterns in other layers, and of the defect size. Identifying "composite" sensitive areas gives the ability to predict the probability of failure of special structures like transistors and capacitors, which in turn ease the problem of predicting accurately and realistically the circuit design yield with respect to photolithographic defects.

Finding correctly the critical areas in layouts plays an important role in yield prediction. Several approaches which inherently make use of the concept of critical areas have appeared in the literature [4],[5]. An alternate approach [6] which explicitly uses the critical areas was also presented although the yield prediction (w.r.t. spatial defects) is restricted to shorts and breaks.

SENSITIVE AREAS.

It is convenient to examine briefly the nature of defects and their impact in the ICs. An IC layer is a piece of solid state surface in the wafer usually shaped by one or more masks. The absence or presence of a mask can represent the absence or presence of a certain material in a specific layer. For our purposes a defect is any deviation in the shape of the IC layer from its corresponding mask(s) of the layout. Photolithographic defects are present in the form of line registration errors and spot defects [7]. Defects can introduce faults. A fault is any deviation from the expected behavior of the IC. Some faults are fatal, such as stuck-at outputs or a dc-path change in the topology of the circuit, other faults are only performance failures like undesirable delays.

An electrical element, like a transistor, a capacitor, etc., is a "structure" in which the combination of layers has a special role, and where a defect introduced to any of the involved patterns of the layers makes the entire structure to fail.

The modeling of defects can be done using circles or squares [7]. For clarity purposes of the explanations to follow in the

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paper we prefer to use squares.

We distinguish the "pattern sensitive area" as the area where the center of a defect must fall to cause a fault in the pattern, such as breaking it or joining it with another pattern. The "structure sensitive area", on the other hand, is the area where the center of a defect must occur in order to introduce a fault to the structure.

PATTERN SENSITIVE AREAS FOR SHORTS.

Under the pattern approach all the patterns are considered as interconnectors, and a fault appears only when nonequipotential regions are joined together. Fig. 1 represents the single case of two conductive lines, each of width w, length L and space s between them. Assume that an extra spot of material occurs between the two conductors, if the size of this defect is such that $x > s$ the critical area can be expressed as:

$$A_{PS} = W_{PS} L_{PS} \quad (1)$$

where

$W_{PS} = x - s$
$L_{PS} = L + x$

W_{PS} and L_{PS} represent the critical width and length of the critical area, respectively. The end effects of the defect are also accounted in the length of the critical area.

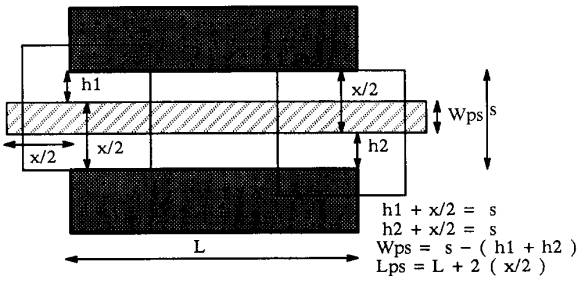

Figure 1. Pattern sensitive area for shorts

PATTERN SENSITIVE AREAS FOR BREAKS.

In this approach a break occurs when an equipotential region is fragmented into two or more nonequipotential regions. Fig. 2 represents a single conductor of width w and length L. Assume that a defect in the form of a missing material occurs. If the size is such that $x > w$ the critical area can be modeled as:

$$A_{PB} = W_{PB} L_{PB} \quad (2)$$

where

$W_{PB} = x - w$
$L_{PB} = L + x$

W_{PB} and L_{PB} represent the width and length of the critical area respectively. The end effects are also consider in the length of the critical area.

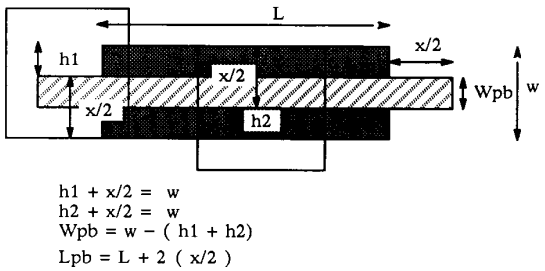

Figure 2. Pattern sensitive area for breaks

UNCOVERED SITUATIONS OF THE PATTERN SENSITIVE AREA APPROACH.

We will point out some cases where the pattern sensitive area fails to detect faults other than shorts and breaks.

Case 1. Consider the case of Fig. 3 where an enhancement transistor is depictured. Both "conductors", poly and diffusion, have a width w. If a defect in the form of missing material appears in the poly layer, two fatal situations may arise: 1) The defect size is x > w and breaks totally the pattern as shown in Fig. 3a, and 2) the defect is of size x < w but it also breaks the pattern as depictured in Fig. 3b. In both cases the transistor's drain and source are short circuited however no sensitive area is computed.

Case 2. Assume now that an extra spot of poly material crosses a diffusion wire which is in its neighborhood, as it is shown in Fig. 4. The undesired crossing creates a parasitic transistor in series with the diffusion wire. However, since the theory is "unilayer" and accounts only for breaks and shorts this situation is never covered.

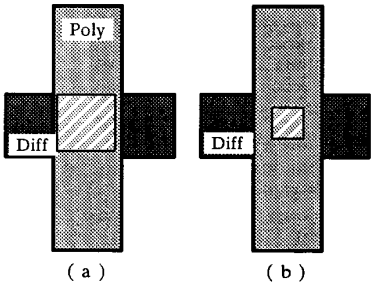

Figure 3. Enhancement transistor. (a) The gate is fully broken. (b) The gate is partially broken

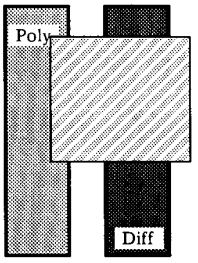

Figure 4. Creation of a parasitic transistor

Case 3. In Fig. 5 a poly-metal via is shown. Assume also that the width of both conductors is w. If a spot of missing material is present in the metal wire exactly on the via, two fatal situations may also arise: 1) The defect size is x > w and breaks totally the pattern, see Fig. 5a, and 2) the defect size is x < w but it occurs precisely on top of the area of the contact hole, see Fig. 5b. In both situations a circuit-break, or a floating line, occurs however no critical area for the last situation is established.

Case 4. Consider once more the via. If an extra spot of material of the contact hole occurs, it is possible that two layers are involuntary connected, as is the case of Fig. 6. Since the theory works only for shorts and breaks any extra contact-hole area is not considered even when a potential fault is present.

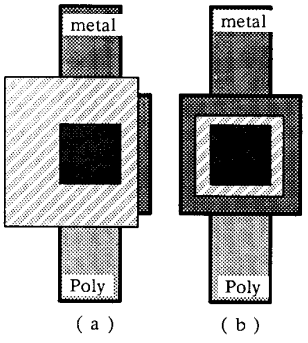

Figure 5. Poly-metal via. (a) Metal wire broken. (b) Metal wire partially broken

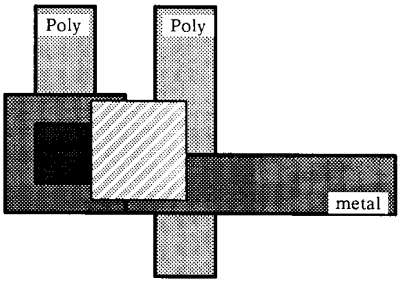

Figure 6. Involuntary via

Case 5. This example does not point out breaks or shorts but it rather projects a possible performance failure. Take in consideration the implant layer of the depletion transistor depictured in Fig. 7. Because the approach accounts only for conductors the layer is discarded from consideration, however the depletion transistor can be turned into a simple enhancement transistor if a spot of missing material of a significant magnitude is present.

STRUCTURE SENSITIVE AREAS.

We outline next a series of requirements necessary to compute multilayer sensitive areas. Since we want to take into consideration the electrical properties of the design it is necessary to identify those electrical elements that have a special meaning in the layout. Therefore, any transistor, via, wire, etc., must be characterized by a unique combination of layers. There is a well known technique that is commonly

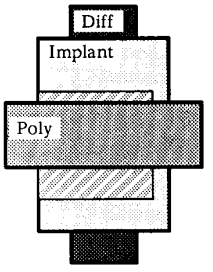

Figure 7. Depletion transistor affected by a spot of missing material in itsimplantation layer.

employed in layout to circuit extractors [8] that does this characterization, see Table 1. The layers are coded as follows: (ni) implant, (nc) contact-hole, (nb) underpassing, (nd) diffusion, (np) poly, (nm) metal. A "1" means that the layer is present, a "0" that the layer is absent and an "X" represents a don't care situation.

TABLE 1. Element vectors of an NMOS process.

Element type	nd	ni	nb	np	nc	nm
metal interconnection	0	X	X	0	X	1
poly/diffusion contact	1	X	1	1	X	0
metal/diffusion contact	1	X	X	0	1	1
metal/poly capacitor	0	X	X	1	0	1
enhancement transistor	1	0	0	1	0	0
depletion transistor	1	1	0	1	0	0

Design rules are necessary to define the boundaries of an electrical element. We mention three cases that may help to visualize this. The overlapping extend of the transistor of Fig. 8a is denoted as O_w and O_l, the mutual extension of poly over diffusion as $E_{w_{PD}}$ and $E_{l_{PD}}$, for the extension width and length respectively. The extension of diffusion over poly is the same except that it is denoted with subscripts DP. It is clear that if the PD extension does not exist the drain and source are joined, the diffusion pattern acts just as a simple wire, and

consequently the intended transistor turned out to be two crossing wires. Fig. 8b shows a capacitor, the overlap width and length is denoted by O_w and O_l but in this case the mutual extension is zero. When defining a capacitor, as an element with electrical purposes for the design, we should define its minimum overlap area otherwise any poly-metal crossing will be considered as a capacitor when in fact it is a parasitic element. As a last example consider a simple conductor wire. It intersects itself thus the overlap width and length are in fact the width and length of the wire, as it is shown in Fig. 8c.

Hence, any pattern area in which the pattern is part of a structure can be expressed as:

$$A_{pattern} = (O_w O_l) + 2(E_w E_l) \quad (3)$$

where

O_w = *overlapwidth*
O_l = *overlaplength*
E_w = *extensionwidth*
E_l = *extensionlength*

and the area of the structure element can be seen as the union of each of the pattern areas involved. Remember that the conductor wires are the simplest structures in which just one layer is involved.

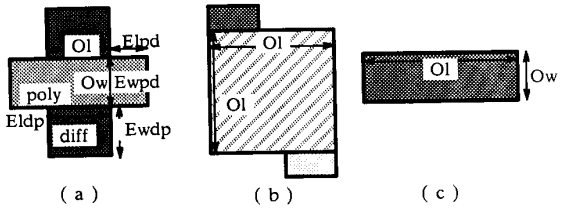

Figure 8. (a) Enhancement transistor. (b) Capacitor. (c) Wire.

It is more appropiate to denote the critical areas as for missing and extra materials instead of as for breaks and shorts because the last two terms are mainly to express the electrical consequences of the former two ones. Besides, we want to find critical areas not only for breaks but also just for a simple missing material that can be fatal to an entire structure.

STRUCTURE SENSITIVE AREAS FOR MISSING MATERIAL.

In every case we use a "cut safe extend Δ" as the minimum portion of the pattern that must be left before it is considered broken, see Fig. 9a.

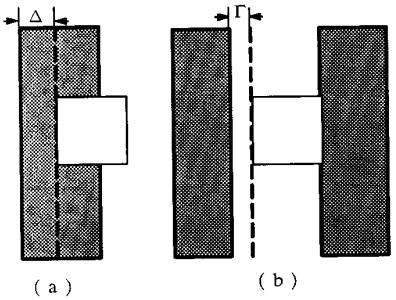

Figure 9. (a)Cut safe extend. (b)Bridge safe extend

Consider now Fig. 10a where a simple conductor wire is shown. The minimum cut extend was set to approximately 0.1 the width w of the pattern, this means that almost the entire pattern has to be cut to consider it broken. Thus, only those defects whose sizes are $x>(w - \Delta)$ are fatal. The figure shows two defects positioned in the uppermost and lowermost locations such that their dimensional extensions leave only the safe extend of the pattern.

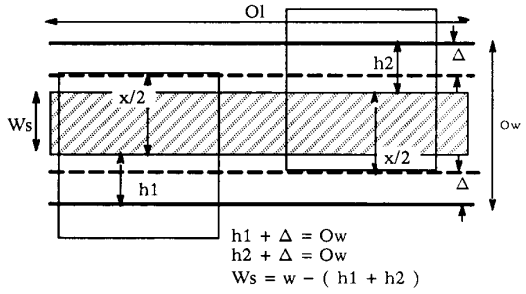

Figure 10. Critical area for the 'wire' structure

The critical area can be written as:

$$A_{S_{cut}} = (W_{S_{cut}} L_{S_{cut}}) \quad (3)$$

where

$W_{S_{cut}} = x - O_w + 2\Delta$
$L_{S_{cut}} = x + O_l$

An exception to the previous formula is when we are dealing with patterns of equal dimensions. If this is the case it is worthwhile asking "which side is the length and which side is the width ?" If we choose one of the sides to be the width we can create critical areas such as the ones of Fig 11b. However, notice that the pattern is fully broken only when the center of the defect is in the middle square of the intersecting critical areas as shown in Fig. 11c.

Thus, the critical area can be expressed as

$$A_{S_{cut}} = W_{S_{cut}} W_{S_{cut}} \quad (4)$$

where

$W_{S_{cut}} = x - O_w + 2\Delta$

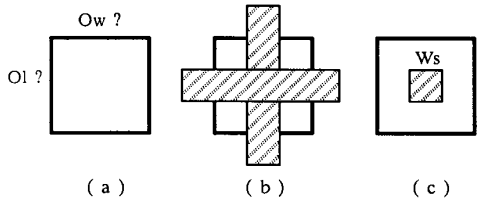

Figure 11. Critical area for square patterns

Consider now Fig. 12 where once more an enhancement transistor is shown. Let us analyze first the poly layer. If a defect occurs in the poly pattern such that its size is $x>(O_w - \Delta)$ the critical area of the poly pattern can be expressed as :

$$A_{S_{cut}} = (W_{S_{cut}} L_{S_{cut}}) + 2(W_{E_{cut}} L_{E_{cut}}) \quad (5)$$

where

$$W_{S_{cut}} = x - O_w + 2\Delta_{overlap}$$
$$L_{S_{cut}} = x + O_l$$
$$W_{E_{cut}} = x - E_{w_{PD}} + 2\Delta_{extension}$$
$$L_{E_{cut}} = x + E_{l_{PD}}$$

A judicious choice of $\Delta_{overlap}$ is to set it to the width of the pattern since any portion cut from the layer can alter the characteristics of the transistor. $\Delta_{extension}$ can be set to $0.9E_w$. This allows to have small cuts in the corners of the gate without fully damaging the transistor. In any case the Δ factor should be specified for each layer of the structure and also for each electrical element defined. The same analysis can be carried on for the diffusion layer, except that the Δs should be now for the diffusion layer, although common sense tells us that they should be the same. Finally, the critical area of the transistor is the union of the critical areas of the poly and diffusion layer. Therefore, the critical area of any structure can be specified as:

$$A_{structure} = \bigcup_{i=1}^{i=N} A_{S_i} \quad (6)$$

where A_{S_i} is the structure critical area of each layer.

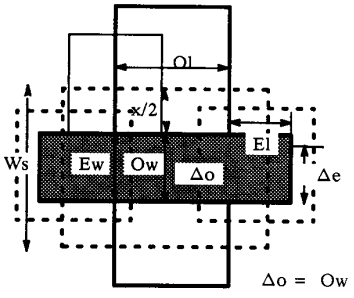

Figure 12. Critical area for the poly pattern in a transistor

We can do a brief summary now. First, equation 5 provides us the means to find the critical area for any pattern in a structure, recall that a wire is the simplest structure with only one layer involved and without mutual extensions. And second, the keywork to this approach is that the "cut safe extend" is variable and depends on the electrical element, as we showed with the last two examples.

A special case arises when two structures of the same kind, like two poly wires intersect each other, as shown in Fig. 13a. In order to satisfy equation (5) we split the two wires in three, such that we obtain two independent patterns plus a third one which is the intersection. The critical areas for each one of the three rectangles can be obtained from equations (4) and (5).

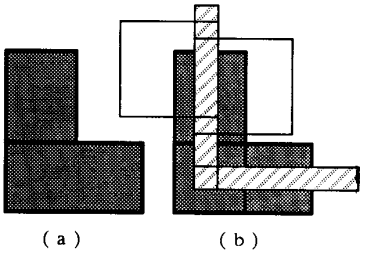

Figure 13. (a) Intersection of two structures of the same kind. (b) Critical areas

A dangling end is a loose structure in the layout. Detecting dangling ends is important because it prevents from calculating more critical area than it should. When a structure does not end in a bonding pad or at least one of its extremes is not attached to another structure then it is considered a dangling end. Consider the case of Fig. 14 where a long wire is used to connect several devices. For instance, the portion A of the wire could be a dangling end, however it is attached to a terminal pad and also intersects another structure of its same kind, now portion B could be the dangling end, however its both extremes are attached, finally portion C is a dangling end since one of its ends is loose.

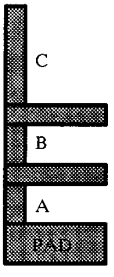

Figure 14. Dangling end

STRUCTURE SENSITIVE AREAS FOR EXTRA MATERIAL.

We also make use of a "bridge safe extend Γ" as the minimum space between two patterns that must be left before they are considered joined, see Fig. 9b.

We will study first the case in which the patterns belong to the same layer. Consider now Fig. 15 where two simple conductor wires are shown. The minimum safe extend was set to approximately 0.1 the nominal space s, this means that almost the entire space has to be covered to consider them joined. Next we determine the critical area for defects whose size are $x>(s - \Gamma)$. For this purpose the figure illustrates two defects such that they are located in the extremes points of the critical belt width.

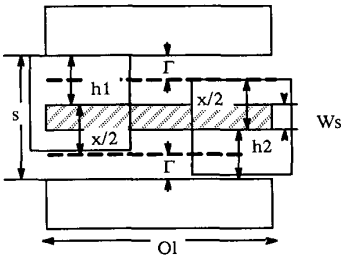

Figure 15. Critical area for two 'wire' structures

The critical area is found to be:

$$A_{S_{bridge}} = (W_{S_{bridge}} L_{S_{bridge}}) \quad (7)$$

where

$$W_{S_{bridge}} = x - s + 2\Gamma$$
$$L_{S_{bridge}} = x + l$$

Consider now Fig. 10 where two patterns are shown. One pattern belongs to the poly layer and the second to the diffusion layer. Assume that an extra material of poly can occur and that it crosses the diffusion line in such magnitude that a parasitic transistor can be made. As in the case of breaks the setting of the extend factor should be done carefully. In this case it is reasonable to set it to a negative value equal to the width of the diffusion pattern. This forces to extract a parasitic transistor only when the poly defect goes beyond the overlapping, as it is depictured. Equation 7 is used again to find the critical area for the structure "parasitic transistor". Critical areas for structures with more than one layer are also the union of each one of the critical areas of the patterns involved in the structure. They can also be represented by means of equation 6.

CRITICAL AREAS AND CIRCUIT SENSITIVITIES

We showed in the last two sections that by appropiately setting the safe extend factors we can take in account the critical areas for different electrical elements, and also we take into consideration a larger number of different fault types.

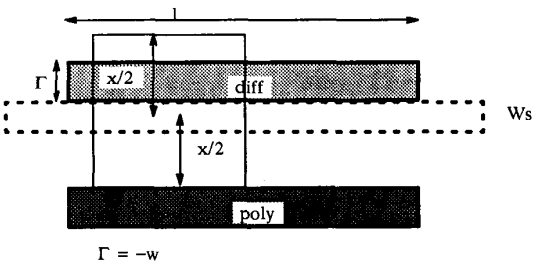

Figure 16. Critical area for a 'parasitic transistor' structure

Critical areas are now not for the ideal case of the conductors but rather for structures that have an electrical significance in the layout.

The sensitivity of the circuit can be seen as the union of the sensitivities of all the electrical components in the layout. The element sensitivity, or probability that an element fails, is related to its structure critical area by:

$$A_{structure} = \Theta_{element} A_{layout} \quad (8)$$

where $A_{structure}$ is the critical area of the element as defined by equation 6, and Θ is the probability of failure of the element.

As opposed to looking at the probability of failure of the element, we can find the probability of occurence of a specific fault if the failure mechanism is known. In this case the failure mechanisms are undesirable spots of extra or missing materials which appear in the normal structure of the electrical element. Tables 2 and 3 show some faults which can be modeled in this way. As an example consider the "parasitic transistor" shown in Fig. 4, the probability of occurrence of this fault is:

$$P_{occurrence} = \frac{A_{str-poly}}{A_{layout}} \cup \frac{A_{str-diff}}{A_{layout}} \quad (9)$$

where $A_{str-poly}$ is the structure critical area of the poly pattern and $A_{str-diff}$ the one of the diffusion pattern.

This suggests also that the probability that an electrical element is faulty depends upon how many fault situations may occur with respect to it. It might be, for instance, in a "transistor structure" that the diffusion pattern is joined to another pattern and also that the poly pattern has a spot of extra material such that it creates a parasitic transistor. Therefore, the sensitivity of the element can also be interpreted as the union of the probability of occurrence of every related fault.

$$\Theta_{element} = \bigcup_{i=1}^{N} P^{(i)}_{occurence} \quad (10)$$

TABLE 2. Element fault vectors for missing material defects. Notations in capital letters represent the spots of missing material of the corresponding layer .

Fault type	nd	ni	nb	np	nc	nm	ND	NI	NB	NP	NC	NM
floating line	1	X	0	0	1	1	0	0	0	0	1	0
poly break	0	X	X	1	0	0	0	X	X	1	0	0
metal break	0	X	X	0	X	1	0	X	X	0	X	1
stuck-on transistor	1	0	0	1	0	0	0	0	0	1	0	0
stuck-off transistor	1	0	0	1	0	0	1	0	0	0	0	0

TABLE 3. Element fault vectors for extra material defects. Notations in capital letters represent the spot of extra material for the corresponding layer.

Fault type	nd	ni	nb	np	nc	nm	ND	NI	NB	NP	NC	NM
Involuntary via	1	X	0	0	0	1	0	0	0	0	1	0
poly short	0	X	X	1	0	0	0	X	X	1	0	0
metal short	0	X	X	0	X	1	0	X	X	0	X	1
stuck-at transistor	1	0	0	1	0	0	0	0	0	1	0	0
parasitic transistor	1	0	0	0	0	0	0	0	0	1	0	0

CONCLUSIONS.

The physical meaning of a defect should be determined not only by its placement in a single layer but rather on the effect that it might have in several layers. Thus, composition of layers with electrical significance must be identified in the layout in order to compute the critical area of the structure.

We presented two general expressions to find the critical areas for extra and missing materials in electrical components. The approach followed makes use of "safe extend" factors which must be set independently for each structure with an electrical significance in the layout.

The ability to find critical areas for structures allows to highlight the probability of failure of the circuit, not of the layout, as a function of its fault models. Therefore, it should be possible to do a classification such as to project the probability of failure due to: stuck-at transistors, floating lines, parasitic devices, shorts, breaks, etc. as well as to find their locations in the layout.

REFERENCES

[1] C. H. Stapper, "Modeling of Integrated Circuit Defect Sensitivities", *IBM J. Res. Develop.*, Vol. 27, No. 6, November 1983, pp. 549-557

[2] C. H. Stapper, "Modeling of defects in integrated circuit photolithographic patterns", *IBM Res. Develop.*, Vol. 28, No. 4, July 1984, pp. 461-475

[3] A. V. Ferris-Prabhu, "Modeling the Critical Area in Yield Forecast",*IEEE Journal of Solid-State Circuits*, Vol, SC-20, No. 4, August 1985, pp. 874-877

[4] J.P. Shen, W. Maly, F.J. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits", *EEE Design and Test of Computers*, December 1985, pp. 13-26.

[5] H. Walker, S. Director, "VLASIC: A Catastrophic Fault Yield Simulator for Integrated Circuits", *IEEE Trans. Computer-Aided Design*, Vol. CAD-5, No. 4, October 1986, pp. 541-556.

[6] I. Chen, A. Strojwas, "Realistic Yield Simulation for IC Structural Failures", *IEEE Int. Conference on Compputer Aided Design*, Nov. 1986, pp. 220-223.

[7] W. Maly, "Modeling of Lithography related yield losses for CAD of VLSI circuits",*IEEE Trans. Computer-Aided Design*, pp. 166-177, 1985

[8] P. Dewilde, Editor, "The Integrated Circuit Design Book", Delft Univ. Press, 1986., pp. 251-293.