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Citation for published version (APA):
Bakopoulos, P., Zakynthinos, P., Kehayas, E., Stampoulidis, L., Fresi, F., Porzi, C., Calabretta, N., Kouloumentas, C., Petrantonakis, D., Maziotis, A., Stamatiadis, C., Apostolopoulos, D., Guina, M., Klonidis, D., Poti, L., Tangdiongga, E., Poustie, A., Maxwell, G., Tomkos, I., ... Avramopoulos, H. (2009). 160 Gb/s all-optical contention resolution with prioritization using integrated photonic components. In *Proceedings of the 35th European Conference on Optical Communication (ECOC 2009) 20 - 24 September 2009, Vienna* (pp. 6.3.5-1/2). Institute of Electrical and Electronics Engineers.

Document status and date:
Published: 01/01/2009

Document Version:
Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

• A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
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160 Gb/s All-Optical Contention Resolution with Prioritization using Integrated Photonic Components

P. Bakopoulos (1), P. Zakynthinos (1), E. Kehayas (1), L. Stampoulidis (1), F. Fresi (3), C. Porzi (3), N. Calabretta (5), Ch. Kouloumentas (1), D. Petrantonakis (1), A. Maziotis (1), C. Stamatiadis (1), D. Apostolopoulos (1), M. Guina (4), D. Klonidis (7), L. Potì (2), E. Tangdiongga (5), A. Poustie (6), G. Maxwell (6), I. Tomkos (7), A. Bogoni (2), H.J.S. Dorren (5) and H. Avramopoulos (1)

1 : National Technical University of Athens – School of Electrical and Computer Engineering
9 Iroon Polytechniou Street, Zografou 15773 – Athens, Greece, Email: pbakop@mail.ntua.gr
2 : Photonic Networks National Laboratory, CNIT, Pisa, Italy, via Moruzzi 1, 56124 Pisa, Italy
3 : CEIIC, Scuola Superiore Sant'Anna, Pisa Italy, 4 : ORC, Tampere University of Technology, Tampere, Finland
5 : COBRA Research Institute, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands
6 : CIP Technologies LTD, Adastral Park, Ipswich, IP5 3RE, UK
7 : Networks and Optical Communications group-Athens Information Technology Center 19002, Athens, Greece

Abstract *We present for the first time 160Gb/s all-optical contention resolution with prioritization using integrated photonic devices. Error-free operation verifies that complex photonic systems are possible and could play a central role in future high-capacity networks.*

Introduction

The realization of advanced photonic integrated components has fuelled new research for realizing more advanced and larger all-optical processing systems [1,2]. Driven by the potential for larger integration scale, smaller footprint and lower power consumption of photonics, research now turns to the design of novel architectures and the implementation of all-optical processing systems. These novel architectures would allow to perform more complex network functionalities serially, on the fly and at bit-rates not possible by electronics. In this paper we present an optical circuit capable of resolving contention in space and wavelength domain between 160 Gb/s packets at the same wavelength λ1, also taking into account priority flags embedded into optical labels. Packet priority information is transmitted alongside with the packets at λ2 (pulse = high, no_pulse = low priority) and can be in-band with the data increasing the overall bandwidth utilization [2]. The system operates at 160Gb/s, does not require any electronics and performs all processing on-the-fly. The circuit was implemented by fiber-interconnecting photonic integrated devices, making the system integrable using hybrid integration of III-V with Silica-on-Silicon platform. Due to the use of packet-level signal processing and high-speed wavelength conversion [3] the bit-rate could be extended to rates >320 Gb/s.

Fig. 1 shows the functional diagram of the circuit, consisting of two 1x2 switches (Switch_1 and 2), an Optical Flip-Flop (OFF), a Packet Envelope Detection circuit (PED) and a 160 Gb/s all-optical Wavelength Converter (WC). Packet A enters the circuit from input 1 and its priority flag is extracted using narrowband optical filtering. The extracted label is fed to the OFF to generate an optical pulse at λ3 with length slightly higher than the data packets. This signal is used to control the state of Switch_1 and route packet B: In the presence of λ3 (i.e. packet A has priority) packet B exits from output_2 of Switch_1 and thus is routed to O/P1 ("contention" port), otherwise packet B exits from output_1 and thus from O/P2 (main output). Output_1 of Switch_1 is split and introduced to the PED circuit generating packet envelope signals at λ4. The PED output is used to control Switch_2 so that packet A is routed to output_3 and exits from O/P1 when the PED is on (ie. packet B exists and packet A has low priority), otherwise packet A is routed to output_4 and exits from O/P2. Outputs 1 and 4 of the 1x2 switches are combined to the circuit output (O/P2) whereas outputs 2 and 3 are combined to point 5 thus resolving the contention in the space domain. Contention resolution in the wavelength domain is performed by wavelength converting the data packets appearing at point 5 to wavelength λ5.

Experimental setup and results

Fig. 2 shows the circuit experimental setup. A 10 GHz mode-locked laser generated 1.8ps pulses that were modulated into data packets containing a 2^7-1 PRBS pattern. This signal was rate-multiplexed to 160Gb/s in a fiber multiplexer and generated a sequence of three data packets with 52ns duration followed by an empty packet slot. This signal was split in 2 parts to provide the 2 incoming packet streams. Packet stream A was combined with the priority flag and was delayed by 90ns with respect to packet stream B (Fig. 3(a,b)). The priority flag was generated in a second modulator and had 1.6ns duration. Packet stream A was separated from the priority flag using an optical filter. The extracted flag was split in 2 parts separated

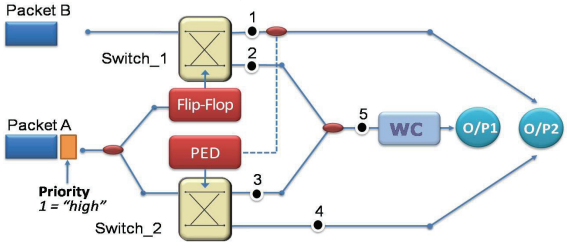

Figure1:Priority-enabled contention resolution concept

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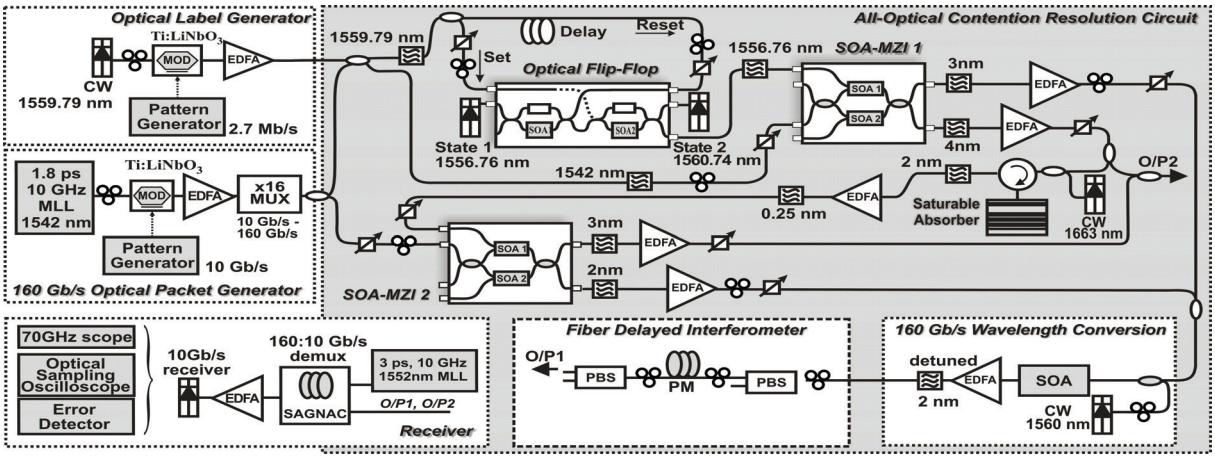

Figure 2: Experimental set-up.

by 60ns to provide the Set and Reset signals for the OFF, which generated 60ns pulses with 1.4dB fluctuation (Fig 3(c)). In parallel, packet streams A and B were introduced to Switch_2 and Switch_1 respectively. Both switches were hybridly integrated SOA – Mach-Zehnder Interferometers and were biased with co-propagating assist CW beams to reduce the SOA ASE. Output_1 of Switch_1 was introduced to the PED circuit, consisting of a passive slow saturable absorber-based vertical-cavity semiconductor gate powered by a 1564nm CW [4]. Output pairs 1,4 and 2,3 were time-synchronized and combined at the main output and contention output respectively (Fig. 3(k,j)). The contention output was combined with a 1560nm CW and was launched in the WC, consisting of a 1.1mm long SOA followed by a 1.5nm filter and a delayed interferometer (Fig 3(i,l)).

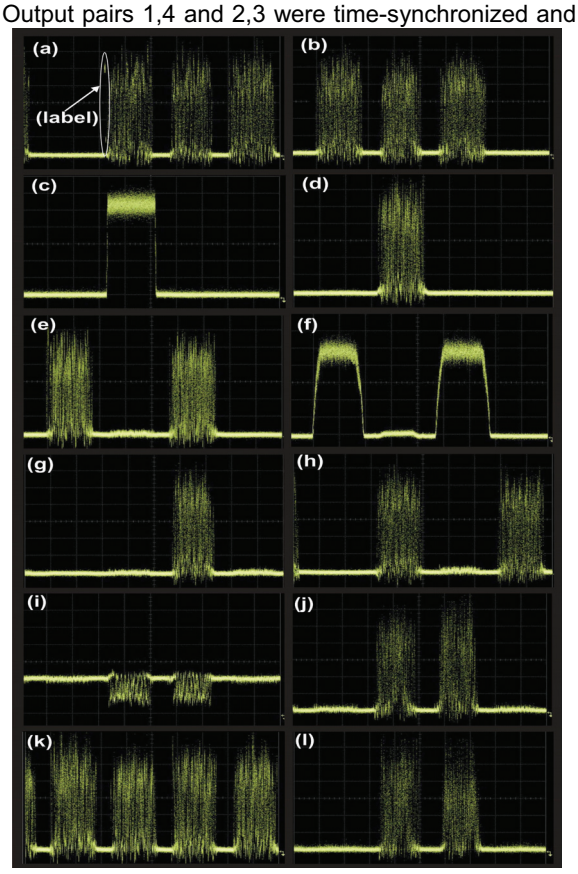

Figure 3 Experimental results. (a) Packet A, (b) packet B, (c) OFF (d) output_2, (e) output_1, (f) PED, (g) output_3, (h) output_4, (j) low-priority contending packets (output_ 5), (k) O/P2, (i) SOA-filter output (inverting WC) and (l) WC output (O/P1). Time scale: 38 ns/div

The 160Gb/s streams were demultiplexed to 10Gb/s in a Sagnac optical switch and the BER performance of the 10Gb/s tributary channels was evaluated. Fig. 4 shows the BER of the input, O/P1 and O/P2 demultiplexed signals as well as the corresponding eye diagrams. The obtained power penalties were 4.5dB and 7.8dB at O/P2 and O/P1 at log(BER)=10-9.

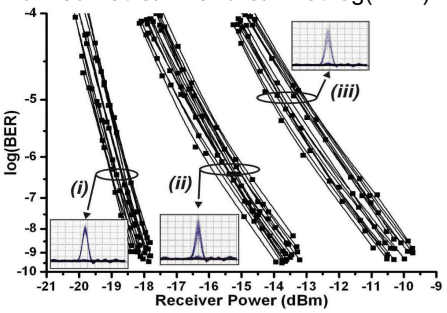

Figure 4 BER performance of the contention resolution circuit i) input data, ii) O/P2, iii) O/P1.

Conclusions

We present 160Gb/s contention resolution in space and wavelength domain with prioritization. The circuit includes photonic integrated devices, verifying the potential of photonics in large-scale systems-on-chip.

Acknowledgements

This work was supported by the European Commission through FP7 project ICT-EURO-FOS Network of Excellence. We gratefully acknowledge HHI, U^{2}t and Alnair Labs for fruitful discussions and hardware/software provided for the experiment.

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