An integral shannon-based view on smart front-ends (invited)

An Integral Shannon-Based View on Smart Front-Ends

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***Abstract*— This paper describes how trends in information society, communication technology, microwave technology, and IC-design technology, ask for a different view on front-ends. The communication channel will be described from a high level, as one 'Shannon channel', comprising a chain of cascaded sub channels. Trends influencing each sub channel will be addressed. From that, we will argue that an integral approach to the design of the communication chain will be a prerequisite for the design of future front-ends. Moreover, the design of the front-end will become dominated by the IC part of the chain, rather than by the transmission channel, which will lead to 'conversion-driven' rather than 'transmission-channel driven' analog front-ends. Finally, it will be shown that future converters will have to be smart. Although applied to wireless, the conclusions are generic and as such can be applied to wired communication channels too.**

I. Introduction

The need for communication is ever growing, as our information society requires more information, anywhere, anytime. Moreover, for communication speed to keep up with digital processing power, we need to facilitate an increase of data rate of about 3 times for every new technology node. The communication should be mobile, wireless and reliable, preferably with just one communication device for all services. Together with the large variety of standards, interference and congestion problems, scarcity of bandwidth, shifts to bands at high frequencies (several tens of GHz), small form factor, long battery life time, etc., this leads to enormous requirements for the front-end (FE) of the transceiver, see Fig. 1a. Traditionally, the communication chain is approached from the transmission channel, which should be used optimally, based on Shannon's fundaments [1]. The FE, and especially the analog FE (AFE), has to provide the required signal 'conditioning' (modulation, in terms of communication theory) according to the standard. We will refer to this as *transmission-channel driven* AFE approach.

For cost and form factor reasons, the FE should be embedded on the digital IC, be compatible with mainstream CMOS, and follow the technology trends. With the higher requirements on the one hand, and the trends in technology on the other hand, the AFE and the converters will then define to a large extent the quality and the resources (power dissipation, chip area, cost) and thus become the bottleneck.

In this paper, we will motivate an integral design approach, extending the Shannon-based view by modelling the chain with three Shannon-channels in series: the transmission channel, the analog channel (including antenna and converters), and the digital channel, and discuss the interrelations between them. We will argue that the AFE, as a signal conditioner, primarily should focus on the overall *conversion* function from analog antenna signals to digital and vice versa, under the constraints of the properties of the silicon/antenna medium (the technology) and the standard-defined EM-waves, and of the costs. In other words, the AFE is primarily a server with the digital IC part as its client. At the same time, the AFE itself should be assisted by the digital core, thus being a client too, with the digital core being the server. The conditioning requirements posed by the transmission channel should be the first responsibility of the digital IC. We will further argue that smart FEs become necessary, like we earlier did for AD and DA converters [2][3]; they incorporate intelligence on chip, and are fed with information from all over the chain.

II. The Front-End in the Transmission Chain

Fig. 1a shows the FE as that part on the chip that takes care for all communication tasks, translating the weak and modulated antenna signals into the (decoded) bits for the application (the backend), and vice versa. In Fig. 1b we see that the FE comprises an analog front-end (AFE) with LNA, mixers, synthesizers, (de)modulators, filters, VGA and power amplifiers; AD and DA converters; digital IF (DIF), if present; digital baseband (DBB) with channel selectivity, demodulation, decoding, decryption; and a digital part that takes care for higher OSI-layer issues, like media-access control (MAC) and network. In the common approach, application specs and transmission-channel properties lead to

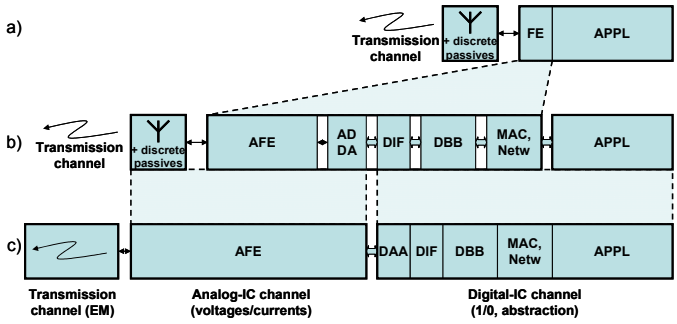

Fig. 1 Communication chain with frontend FE (a), FE expanded (b), and new split up into three sub channels (c)

standards, which enforce specifications for the FE; these are subsequently decomposed into the specifications of the individual blocks. In other words: the transmission channel is a *'client'* and the FE is its *'server'*. Discussions nowadays focus on shifting the conversion step further to the left, so: digitizing more of the FE. Anyhow, this approach is still *transmission-channel driven*. Another issue of research is on-chip antennas. Multi-mode and concurrent operation of the transceivers and silicon properties make this quite complex. Up till now, the design of the antenna, matching networks, etc., is mainly done independently, by microwave designers.

III. Shannon-Hartley-Based View

Let's now take a higher level view to the communication chain. Hartley already formulated a measure for information, linearly proportional to the number of symbols transmitted, and logarithmically to the number of options per symbol. Shannon extended this with statistics, leading, for equal symbol probability and for additive white Gaussian noise, to the Shannon-Hartley channel-capacity formula that states [1]:

$$C = B^{2}log\,(1+SNR)$$

Together with the Shannon coding theorem, stating that there exists a code such that the channel can be used to this maximum, the formula gives a channel capacity that can be seen as an upper bound for the amount of information that can be transmitted, conceptually visualized in Fig. 2.

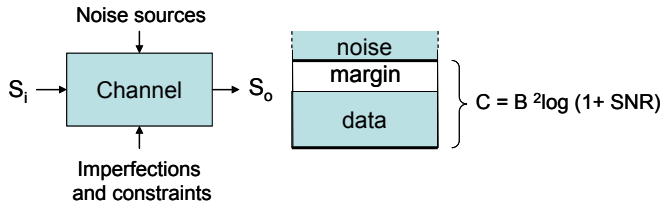

Fig. 2 Shannon-based communication channel model

The capacity is limited by the bandwidth of the channel (maximum symbol rate) and by the SNR (maximum number of symbol options; limited by the resolution in the amplitude domain); without noise the capacity is infinite. This model can be extended for non-equal probabilities (if not taken care for by source coding). Practical imperfections and constraints, like uncertainties (in medium and in 'modulation', in terms of communication theory), and inaccuracies leading to distortion, together with power constraints, further require a certain margin in the design. The rest is available for data transport, if optimally modulation is used.

The common view is to see the transmission channel as a 'Shannon channel', and to assign the task of modulation to the FE, *to achieve optimal use of the transmission channel*. In fact, this is a restricted view that only makes sense if that transmission channel is the bottleneck in the whole chain. Note that, along the same line of thinking, only the 'external' part of the channel is commonly, but wrongfully, referred to as the 'transmission channel'. For the sake of clarity, we will stick to this convention and refer to the whole channel as the communication channel or chain.

IV. A Cascade of Shannon Channels

It was already mentioned that power dissipation is a constraint. In many designs, low power dissipation is even one of the primary goals. Note that both bandwidth and SNR cost power, not only in the sense of transmitted power per bit (where Shannon and others elaborated on), but also on power required to realize the signal conditioning (in our case: power required by the ICs), as the efficiency of the electronics itself is limited, requiring extra power as well. The fundamental reason for that is that the electronic channel, the IC, is as well a physical channel that should be treated quite similarly as a Shannon channel. Consequently, *any power budget restricts both the channel capacity and the utilization for the whole communication path*.

Therefore, we propose a high-level modeling as given in Fig. 3, and in more detail in Fig. 1c: a cascade of three Shannon channels, with 'AFE' used now in a wider sense: all analog electronics, as one sub channel, to be optimized as a whole [4].

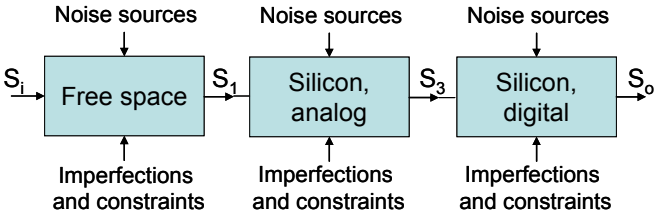

Fig. 3 Communication channel seen as three Shannon channels

The partitioning in sub channels is driven by the change in medium; the split in analog and digital is made because of different constraints. Anticipating strong interaction, the (possibly integrated) antenna or array of antennas, with the associated matching circuitry [5], etc., are included in the analog-IC path and should be designed together with it.

V. Trends

Let's have a look to the trends for those three paths separately and then draw conclusions.

A. Trends for the Transmission Channel

Indeed, it is clear that the first part of the Shannon chain, the transmission channel, still needs signal conditioning. It is also clear that the complexity will further increase here, due to the trend towards higher data rates, the congestion and scarcity in the wireless RF domain, and the shift to several tens of GHz (microwave) carriers.

B. Trends for the Analog-IC Channel

The problems faced by the transmission channel, are similarly faced by the analog IC path. However, *on top of that the analog IC path also faces a deteriorating medium*: the IC medium becomes aggressively worse for analog. This makes the situation for the analog-IC path significantly worse than for the transmission path. The trend in mainstream CMOS technology (smaller scales, lower voltage supplies, and more

digital on the chip) *decreases the capacity* of the silicon medium (Fig. 2). This is due to a reduced SNR both by the lower signal swings (lower supply voltages) and the higher level of noise contributions from the analog parts and from the massively digital processing on the chip. Indeed, transistor speeds, and thus bandwidth, intrinsically go up, but this does not keep pace with the shift to higher carrier frequencies; consequently, for analog it is difficult to exploit this higher inherent bandwidth in full, as parasitics, responsible for uncertainties in the design and modeling and for extra power dissipation, show a growing and significant impact. Thus, for the analog path, the overall channel capacity (given by the technology) decreases substantially, more than for the transmission channel. Combined with the increase in transmission rates, we thus face, see Fig. 2, a significant *decrease in margin* for the analog IC path, faster than for the transmission channel.

And, even worse, the reduced accuracy of the processing (together with the increased interference signals picked up during the transmission due to more crowded channels; a problem for both transmission path and IC path), requires extra margin, further deteriorating the situation for analog.

C. Trends for the Digital-IC Channel

For the digital-IC channel, the situation is quite different, justifying modelling it as a separate channel. B goes up significantly, not only because in digital the parasitics play a less important role than in analog, so that the inherent bandwidths of the transistors can more efficiently be exploited, but also because the scaling allows parallel paths which further increases the bandwidth of the overall channel linearly with the number of parallel paths. As regards the SNR in the capacity C, every gate actually performs a signal conditioning function for the next gate by restoring the electrical signal level to a logic one or zero; however, a reduction in SNR, as introduced by the technology trend, is not such a severe problem as it is for the analog IC path, because the information is coded now including redundancy, and the noise margins in the logic gates are still high enough. For future nanoscale technologies the further reduced SNR might become a problem, but then, still, the analog-path problem is still far larger. (Note that in this nanoscale situation the digital problem is in fact also becoming an analog problem, but for clarity we will refer here only to the analog-IC path when we mention 'analog'.) Thus, the capacity for digital will increase further, whereas power dissipation is reduced both by the reduction in supply voltages, and by the scaling in geometry: higher inherent speeds in the transistors, and less capacitance.

D. Trends for the Complete Channel

From the previous discussion we can conclude that the capacity for digital still increases; the capacity for the transmission channel decreases while the requirements in terms of data rate increase; for the analog IC channel this also holds similarly, but more aggressively, as the medium deteriorates there quite significantly. Extrapolating this trend, it is reasonable to expect that the analog IC path will become the bottleneck in many applications.

VI. Future Client/Server Relations

Defining now a client as a subsystem that needs signal conditioning and as a server a subsystem that provides such conditioning, we will now show the client/server relations in the conventional situation, and those as anticipated for the future.

The conventional view is visualized in Fig. 4a. The AFE is the main server for the transmission path. However, several functions have been taken over by the digital channel, starting from the baseband functions like the channel selectivity function, up to some IF functions. The converters are seen as separate functions that take care for the conversion.

The anticipated situation is depicted in Fig. 4b. Signal conditioning for the IC path up to the conversion, will be the major problem; it can *only* be done, given a predefined transmission standard, by the analog path itself, step by step, and in fact is then part of the signal conditioning for the digital path. This will be discussed in more detail in the next chapter. However, it can and will be assisted by the digital block (DAA in Fig. 4b), by extracting proper information from the signal and the system in the digital domain that can be used to adapt the analog system function. So the AFE is primarily the server for the digital processing path, whereas the digital path is a server (providing digital assistance) for the analog path, see the two arrows forth and back between these two sub channels in Fig. 4b.

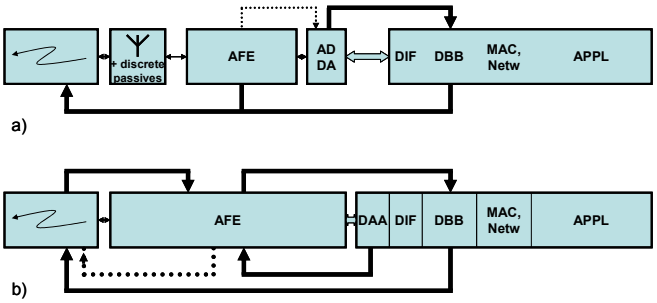

Fig. 4 Client-server relations, conventional view (a) and anticipated situation (b)

In case no standard is predefined, it might well be possible that the transmission scheme is predominantly determined by the analog FE, which on its turn might lead to AFE-driven transmission standards [6]. This makes the transmission path also a server for the AFE path; see the arrow from transmission path to AFE in the figure.

Signal conditioning for the transmission path is also required, of course; this can in principal be done both by the analog-IC path and the digital-IC path. Principally, we expect conditioning for the transmission channel primarily a responsibility of the digital path, see the arrow in the figure, because of three reasons: 1. the IC-conditioning is the dominant concern in the future and can only be done by the analog part; 2. the conditioning for the transmission path can also be done by the digital path; 3. the digital path will steadily grow in capacity in the coming years. Note, however, that the signal conditioning for the IC channel, served by the AFE (arrow from AFE to digital IC), partly overlaps with

what is desired for the signal conditioning required for the transmission channel; as such the AFE at the same time acts already partly as a server for the transmission sub channel. In the figure this is indicated by the dashed arrow (dashed, because it is a positive side effect of another function and not the primary function). The digital part has to take care for all remaining conditioning for the transmission channel. Algorithmic and cost efficiency play an important role and might give preference to analog over digital conditioning. Beamforming is a typical example of optimizing the use of the transmission channel by creating higher SNDR ratios by spatial focusing. If done in the digital domain it requires several parallel analog front-ends; a phase-shifted combination in the analog domain seems then more efficient [7]. However, this choice is motivated by IC conditioning, for efficient use of the *silicon sub channel*, as the single channel after combination is far more efficiently used (in area and capacity) then the combination of parallel channels.

VII. Towards a Conversion-Driven Analog FE

As regards the AFE, we have already drawn two conclusions. First, the antenna must preferably be taken as part of it, at least functionally seen. The emphasis for the AFE is on optimum conversion from EM to bits and vice versa. If possible it will be co-integrated; however, the silicon medium is not optimal for the antenna function. Second, the AFE has to provide the conditioning for the IC channel, for the sake of the conversion to and from the binary signal representation (and performed in the analog part of the channel). Given the trend in technology, the IC channel is indeed best conditioned, when the information is coded in a signal with as few levels as possible, which is the binary signal coding. This relaxes the costly amplitude domain (SNR in the logarithm in Shannon's formula) and instead relies as much as possible on the cheaper bandwidth B in the formula (speed and parallelization; linear relation). As the signals enter the chip (or vice versa have to leave it) in analog continuous-time form, defined by the transmission standard, and have to be translated to the digital form, we need primarily a conversion function including analog signal conditioning and AD/DA conversion. We will therefore call this a *conversion-driven analog FE*.

VIII. Smart Front-Ends

With the AFE becoming the bottleneck in the overall chain, efficiency from an IC-point of view is a prerequisite. Somewhere in time, with ongoing scaling, the margin even will become unsufficient to cover the imperfections, meaning a solution is not realizable anymore within the required specifications and a realistic resources budget (power, chip area, cost). Smart front-ends can 'free' the margin, by using on-chip intelligence to correct imperfections, by adapting the analog conditioning, and/or by (pre or post) correcting it in the digital domain [3]. Extra information can be used from all over the chain, like from the user, from the application, from the IC characterization, from the supply, from the environment, from the input signal (interferers, blockers, congestion, etc.), and from the output signal (like in [5]).

IX. Conclusions

Future communication chains should be optimized in an integral way, with the transceiver considered an integral part of the communication chain in the sense of a Shannon channel. To this purpose, the chain is modeled with three Shannon channels in series: the transmission channel, the analog-IC channel, and the digital-IC channel. Antenna and converters are included in analog FE.

Furthermore, client-server relations have been defined, and changes in them are anticipated. The analog FE should be primarily seen as a server for the digital part, by conditioning the signal: conversion to and from binary signals that are optimal for the IC-channel. Being the bottleneck, the analog FE itself should at the same time be seen as a client with the digital core being the server: digitally assisted analog. The analog FE should thus be primarily designed from the IC-channel point of view, and not from the transmission-channel point of view; in other words: it should follow a 'conversion-driven' FE design, primarily focusing on the conversion of analog signals to digital and vice versa, under the constraints of the properties of the medium (IC technology) and the EM-waves defined by the standard, and of the costs. Partly, this will overlap with the conditioning for the transmission channel. The digital part is primarily responsible for the (remaining) conditioning service for the transmission path.

Smart FEs can 'free' the margin by correcting deterministic imperfections, incorporating intelligence on chip, being fed with information from all over the chain.

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