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Amir Zjajo, Jose Pineda de Gyvez
Philips Research Laboratories
Prof. Holstlaan 4
5656 AA Eindhoven, The Netherlands
E-mail: amir.zjajo@philips.com

Abstract

Due to its low cost, low test time and reduced test complexity, structural testing is preferred to functional whenever possible. The study presented in this paper indicates that the two low-frequency structural test methods considered, power supply current monitoring and the power supply ramping technique, provide a valuable supplement/alternative when one of the functional tests (gain, noise figure and total harmonic distortion) in the test set can be complemented or substituted by structural test and add to or maintain no loss of fault coverage.

1. Introduction

Testing is becoming a substantial barrier to continued RF IC cost reductions because of the additional complexities required by new standards, including multi-band compatibility, higher linearity, lower bit-error rate, and long battery life. In particular, functional bit-error rate testing is the most time consuming operation. RF test costs are projected to take a significant percentage of the manufacturing cost of up to 50% for future RF devices[1]. Moreover, present testing approaches focus on parametric aspects, while actual rejects are functional. This rising cost trend is quite alarming. To reverse this trend, functional testing should be replaced/ complemented with structural testing, offering simpler test patterns, shorter test times and less complex test equipment infrastructure.

A typical test flow allocates test times to wafer test and final test. More traditionally, a wafer test consists primarily of dc tests with current/voltage checks per pin under most operating conditions and with the test limits properly adjusted and in some cases some low-frequency tests to ensure functionality. A wafer test is geared to check open/short circuits, dc biases, charge-pump currents, and logic leakage among other parameters. A final test consists of checking device functionality by exercising tests to cover important circuit parameters. For instance, in the case of RF systems these parameters include the transmitter's power, spectrum and gain steps, or the receiver's IP3, gain, compression, THD, etc. However, with the advent of new packaging techniques, and pressure on test costs, traditional functional tests at package level are being pushed backwards to wafer level. Under this new scenario, wafer testing is performed to determine the true performance of the die independent of the packaging. For more complex System-in-Package modules or Multi-Chip Modules (MCM), only "known good dies" are mounted, provided that the individual dies were wafer-tested to ensure that they were functional and within specifications. Performing RF measurements on wafers may be the most economical production path to market. The challenges of testing RF specifications on wafer come in terms of interference, maintaining power levels, which is greatly affected by return loss, impedance matching, cross-talk..., etc., and obtaining accuracy. These may be overcome by an effective probing setup and calibration procedure.

In this paper we study the role of new low frequency-test methodologies to reduce the use of functional testing. These low-frequency test techniques depart from the traditional role of current/voltage dc checks and are rather applicable for substituting or complementing functional tests. In particular, we concentrate on two techniques, namely power-supply-current monitoring [1-2] and power-supply ramping [3-4]. These two techniques create signatures based on quiescent current measurements. Previous works on power-supply-current monitoring deal with these current signatures in the time domain [1-2]. The immediate drawback of this approach is the complicated testing procedure of direct comparison of supply-current waveforms, especially when the process corners are taken into consideration and when the signature is composed of many points [5]. To avoid this, the spectrum of the power-supply current is preferred to the time-domain supply-current waveform. Although there have been a few investigations in this area in the low-frequency analog circuits [5-7], this approach is completely novel when applied to the high frequency RF world.

The underlying testing approach for both test methods relies on a defect-oriented test analysis that takes into account the spread of the process as well as the presence of resistive defects. Our experiment is based on a Philips

[1] ITRS '04 projections

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Semiconductors Monolithic Microwave IC BGA2712 wideband amplifier [8].

In the course of the paper we will present a brief overview of the wideband amplifier functionality and structural test methodology, propose fault models, give details of the structural and functional tests and a thorough comparison between both techniques.

2. Wideband Amplifier

The design of a constant-gain amplifier over a wide frequency range requires careful design of the matching network, or the feedback network, in order to compensate for the variations of the scattering parameters with frequency. Two commonly used techniques are: (i) the use of a compensated matching network which involves mismatching the input and output matching networks to compensate for the changes with frequency of the forward transmission gain S_{21} [9] and (ii), the use of negative feedback to provide a flat gain response [10].

The typical application diagram of the BGA2712 wideband amplifier is illustrated in figure 1. If input and output stages have a common ground on the chip, a common ground lead inductance provides significant feedback coupling from output to input. This unwanted coupling has a degrading effect on circuit gain and terminal impedances. To reduce this effect, separate ground pads for input and output stages are provided. The DC bias point is maintained internally. When the device is operated below 100 MHz, the value of the input and output DC blocking capacitors should be higher than 100 pF.

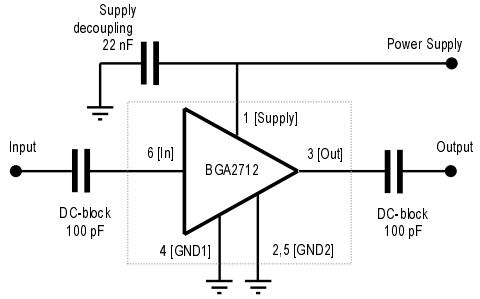

Figure 1: Typical application diagram of the BGA2712.

A general overview of the wideband amplifier specification is given in Table 1 [8]. All of the typical AC parameters specified for RF amplifiers are derived from the S-parameters: S_{11} denotes the input and S_{22} the output reflection coefficient, which is a measure of how well the input and output impedances are matched to the source impedance, respectively, S_{21} denotes the forward transmission coefficient, which is a measure of a fixed gain within a specified frequency range for 0.5dB gain flatness, along with -3dB cut-off frequencies and S_{12} denotes the reverse transmission coefficient, is a measure of how much signal injected into the output port makes it back into the input source. The limits of the dynamic range incorporate non-linearities and noise figure. The non-linearities can be classified into two categories: (i) non-linear distortion effects, which include distortions that occur in the absence of any other signals beside the desired input signals and (ii) non-linear interference effects, which are the results involving one or more undesired input signals. The noise figure of a network is the decrease or degradation in the signal-to-noise ratio as the signal goes through the network.

TABLE I
BGA2712 WIDEBAND AMPLIFIER CHARACTERISTICS AT FIN=2.2 GHZ

Symbol	Parameter	Conditions			Unit
		Min	Typ	Max	
V_S	DC supply voltage	-	5	6	V
I_S	supply current	9	12.3	15	mA
$\|S_{21}\|^2$	insertion power gain	20	22	23	dB
$\|S_{12}\|^2$	isolation	36	39	-	dB
NF	noise figure	-	4.3	4.7	dB
BW	bandwidth	2.8	3.2	-	GHz
K	stability factor	2.5	3	-	-
$CP_{1\,1dB}$	1 dB compression point	-4	-2		dBm
$IP3_{(in)}$	input intercept point	-14	-16	-	dBm
$IP3_{(out)}$	output intercept point	4	6	-	dBm

3. Structural Test Methodology

3.1. Power-Supply-Current Monitoring

The power-supply current of an analog circuit depends on the input signal, the state of the circuit (fault-free or faulty) and the value of the circuit parameters. The power-supply current is a function of the branch currents. If a fault occurs, the current in some branches must have some degree of change. Those changes in branch currents will cause a more or less significant change in power supply current. To avoid direct comparison of the waveforms in the time domain, the spectrum of the power-supply current is employed instead. Figure 2 illustrates difference between harmonics of the fault-free and faulty circuit at 11 MHz input signal, when several single faults, one at the time, are inserted in the circuit. Since such a distinctive behavior is examined and noted across the whole amplifier frequency range of up to 3.2 GHz, our solution would be a less complex, low-cost, low-frequency measurement method eliminating the requirement of expensive RF Automatic Test Equipment (ATE). An essential characteristic of the power-supply monitoring technique is that it can indicate a defect directly, with no requirement to propagate the effects to an output pin. Conversely, under the condition that the ratio of the supply current to the background current is not sufficient to differentiate between a fault-free and a faulty circuit, the main limitation of the supply-current monitoring would be off-chip sensing. However, with development of built-in current monitor on-chip, these constraints have been largely overcome. The criteria for practical on-chip sensor have been summarized in [11]. An important property of any current monitor is to provide

accurate measurements of extremely small current readings in the environment where the current changes are very fast and usually masked with high transients. Several implementations as those depicted in [12-13] have this ability.

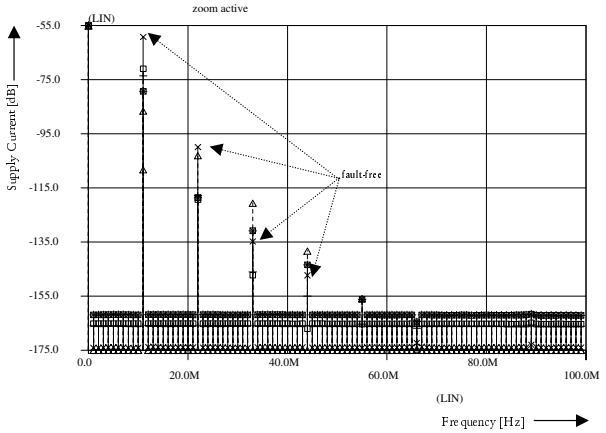

Figure 2: FFT of the amplifier power supply current when 11 MHz signal is offered at the input for fault-free and faulty circuits. The magnitude of the fault-free circuit is denoted with the x sign.

3.2. Power-Supply-Ramp Test Methodology

By applying a ramp signal at the power supply nodes, instead of the usual dc voltage, the majority of the transistors in the circuit are forced into different regions of operation. This has advantage that the detection of faults is done for multiple power-supply voltages and corresponding quiescent currents, enhancing the detectability of faults.

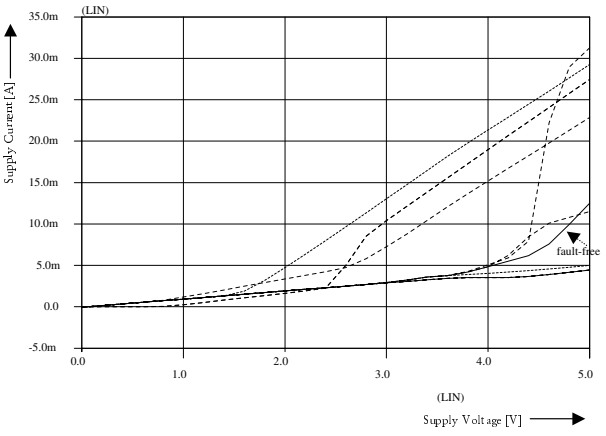

Figure 3: Ramping the power supply voltage and monitoring the supply current for fault-free and faulty circuits. The solid line denotes the fault-free circuit.

The other advantage of a transition from one to the other region is that faults can be detected with distinct accuracy in each of the regions. The power supply voltage is ramped in discrete steps, without paying attention to the speed of the ramp. A clear difference in current signature is obtained between fault-free and faulty circuit as illustrated in figure 3, when, one at the time, several faults are inserted in the circuit. As in the case of the power-supply monitoring, by screening the subsequent behavior of the supply current, there is no need to propagate the effect of the fault to an output pin.

4. Fault diagnosis

4.1. Defect-Oriented Test Process

The defect-oriented test method is based on a fault model that accurately abstracts some fraction (ideally all) of the analog circuit deviations introduced by defects to a set of discrete faults, that can be targeted by a set of tests and detected by production test and measurement equipment. An overview of the defect-oriented test process is given in figure 4. At the first instance, the extracted circuit netlist is simulated without any faults (golden run) and the results of this test are saved. A defect-oriented test starts by generating the fault list. The selected faults are sequentially injected into the circuit and simulated according to test stimuli and the test program.

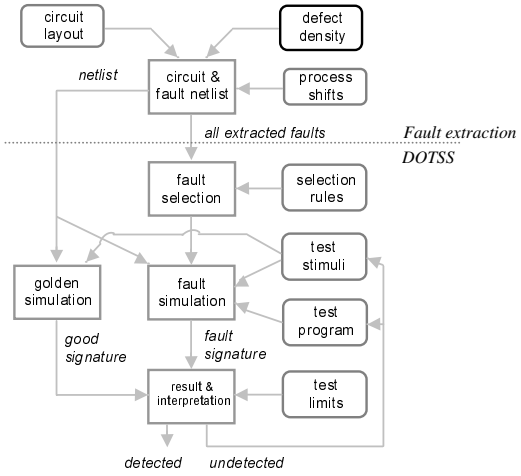

Figure 4: Overview of the Defect-Oriented Test process.

All simulation results are saved in a database, from where the fault coverage can be calculated and the effectiveness of the different individual tests can be established. The detected and undetected faults can be extracted from the database as well. Fault extraction is done on the basis of a Monte Carlo method based on an Inductive-Fault Analysis (IFA) [14-15]. The subject of analog IFA is closely related to realistic analog fault model development. In fact, analog fault modeling has been defined as the critical factor in the success of IFA based analog test methods [16]. Evolved realistic fault models form the basis for test generation and fault simulation.

4.2. The Fault Models and Fault Selection

The fault models are organized according to what defect types can cause that specific circuit fault:

- shorts, which can be formed from extra materials or missing materials,
- opens, where a missing material defect can break a wire on the same layer if it spans the wire or an extra material completely covers a via, which opens the connection,
- size change of devices, where if some shunt transistors are opened, the size of the net transistor is changed instead of forming an open device,
- shorted devices
- non-catastrophic faults, which are evolved from catastrophic shorts and extra contacts.

A catastrophic short in the metal layers was modeled as a resistance inserted between the appropriate nodes, with a value determined by the extra material causing the short: 1 Ω for metal, 10 Ω for polysilicon and 100 Ω for diffusion (ion implantation). Splitting the affected node in two parts and inserting the resistance modeled open faults. A size change of devices was modeled by inserting an extra minimum-size transistor. Shorted transistor devices were modeled as a resistance between the nodes of the affected transistor, while non-catastrophic faults were modeled as a parallel combination of a resistance of 500 Ω and a capacitance of 1 fF [17]. A capacitor short was modeled as a resistance inserted between the nodes of the capacitor and capacitor open by separating the nodes and inserting the resistance. A resistor short and open is modeled in a similar way as a capacitor short and open. Replacing all the transistors, capacitors and resistors with the corresponding fault models all faults are generated. If there are *n* different nodes and there are *m* transistors, *k* capacitors and *l* resistors in the circuit, the number of possible faults is

$$F_{total} = (\sum_{j=1}^{m} 3 + \sum_{j=1}^{k+l} 2)_{opens} + \sum_{i=1}^{n-1} i_{shorts} + m_{sizechange of device} + \sum_{j=1}^{m} 3_{short\ device} + \sum_{j=1}^{m} 3_{non-catastrophic}$$

When applying the previous formula on the wideband amplifier, a total of 189 faults are generated. The tool DOTSS (Defect-Oriented Test Simulation System, a Philips in-house environment for faults simulation, selection, grading and modeling) injects these faults in the fault-free circuit netlist, and passes this modified netlist to the circuit simulator, whose analysis results are then collected by DOTSS and stored in a database.

Since varying the resistance in the model will influence the quiescent current, which will in turn affect the sensitivity of testing method, it is necessary to analyze the impact of weak resistive opens and shorts on fault coverage. Therefore, all individual tests have been conducted for various resistive values. For all individual tests it has been assumed that the circuit can sustain process variations, so the tolerance band can be assumed as well. Any tested signature that falls within $\pm 3\sigma$ spread of the reference value has been assumed to be correct. After setting limits for individual tests and looking at the coverage of a test for a given set of limits, the following step is to group several tests and to determine the total coverage of a number of tests. For each test, DOTSS carries out a test optimization making it possible to choose a combination of tests, which constrains the number of measurements to a couple of points. For the complete analysis at maximum 4 single test points are necessary to achieve the calculated fault coverage.

5. Fault Detection

5.1. Individual Test Methods

Results of the study of the individual tests indicate that 100% fault coverage of all modeled faults except change size of devices is not obtainable when only a single test is applied to the circuit. The tables II and III clearly show a higher percentage of the fault coverage for lower-catastrophic, device-short and higher-open resistive representation, while table IV indicates the fault coverage of non-catastrophic and size change of devices faults.

Often, it is quite likely that a catastrophic fault would change the DC operation point of the circuit and hence will be detected by a DC test stimulus. This may hold for some of the high-impedance non-catastrophic faults as well. The simple DC test is based on a measure of the dc voltage at the output of the circuit. Direct consequence of the injecting of the faults is that the output voltage differs from the nominal value, beyond the $\pm 3\sigma$ spread of the reference value. Depending of the resistor values, which represents catastrophic and devices shorts and opens, each DC analysis will have different fault coverage. Applying DC stimuli will detect around half of the non-catastrophic faults and around one-tenth of the size change of devices faults. Performing a two-port analysis, the forward-transmission-gain coefficient and noise figure (NF) can be determined. Gain analysis detects at the maximum 97.8% of catastrophic and device-shorts, 92.8% opens, 76.2% of the non-catastrophic faults and 87.5% of the size change of devices faults. Fault coverage of the noise figure testing seems to be lowest or one of the lowest for all modeled faults. Applying a pure incremental input tone to the circuit and measuring the total harmonic distortion (THD) values at the circuit output detects most of the open and size change of devices faults. For every type of fault in the circuit, the current in some branches must have some degree of change. Those changes in branch currents will cause a more or less significant change in power-supply current. By applying the sinusoidal signal at the input and then monitoring power-supply current (PSCM) of the faulty

circuit the highest fault coverage of the catastrophic and the devices-shorts are recorded. This method detects at maximum 85.7% of the open and the non-catastrophic faults as well. Applying a ramp signal at the power-supply nodes will provide currents rich in information, capable to differentiate faulty and fault-free circuits in both regions. By monitoring the power-supply current while ramping the supply voltage of the faulty circuit quite comparable results are achieved as with the power-supply monitoring method.

The results indicate that for the strong catastrophic and the device-shorts both structural tests yield a fault coverage comparable, and for both weak shorts even favorable, to functional tests. The power-supply-ramp method is superior to all functional tests for the non-catastrophic faults as well. For the open faults, however, gain and THD tests are advantageous. The THD test reaches 100% coverage of the modeled size change of devices faults, making it not comparable to the other applied tests.

TABLES II – IV INDIVIDUAL TESTS

TABLE II - CATASTROPHIC AND DEVICES SHORTS – MODELED WITH 1-1000 Ω RESISTANCE

Test Type	Fault Coverage [%]			
	1	10	100	1000
DC	93.4	95.6	80.2	36.3
Gain	97.8	95.6	94.5	48.3
THD	82.4	91.2	89.0	84.6
NF	86.8	83.5	61.5	26.3
PSC Monitoring	97.8	97.8	94.5	84.6
PS Ramp	97.8	97.8	95.6	91.2

TABLE III - OPENS – MODELED WITH 1 KΩ-1000 KΩ RESISTANCE

Test Type	Fault Coverage [%]			
	1	10	100	≥ 1000
DC	42.8	52.3	71.4	71.4
Gain	76.2	92.8	92.8	92.8
THD	95.2	95.2	95.2	92.8
NF	76.2	76.2	76.2	76.2
PSC Monitoring	73.8	85.7	85.7	85.7
PS Ramp	64.3	85.7	85.7	85.7

TABLE IV - NON-CATASTROPHIC AND SIZE CHANGE OF DEVICES FAULTS

Test Type	Fault Coverage [%]	
	Non-catastrophic	Size change of devices
DC	52.3	12.5
Gain	76.2	87.5
THD	85.7	100
NF	42.8	25.0
PSC Monitoring	85.7	25.0
PS Ramp	92.8	75.0

5.2. Combined Test Methods

When examining only combinations of the functional tests, the analysis results show that the DC-gain combination is sufficient to detect 100% of the strong catastrophic and the devices shorts as shown in table V. However, for all subsequent resistor values, the highest fault coverage is reached with DC-gain-THD tests combination. Tables VI and VII illustrate that the same test combination detects the highest percentage of the open, 100%, non-catastrophic, 90.4% and size change of devices faults, 100%, as well. Combining the two structural tests alone reaches at the maximum 98.9% of catastrophic and device shorts, 90.4% opens, 93.4% non-catastrophic faults and 87.5% size change of devices faults.

However, when adding the simple DC test to the combination of the two structural tests, 100% fault coverage of size change of devices is obtained.

TABLES V – VII COMBINED TESTS

TABLE V - CATASTROPHIC AND DEVICES SHORTS – MODELED WITH 1-1000 Ω RESISTANCE

Test Type	Fault Coverage [%]			
	1	10	100	1000
DC-PSCM-PS Ramp	**98.9**	**98.9**	**96.7**	**92.3**
DC-Gain	100	98.9	96.7	54.9
DC-Gain-NF	100	98.9	96.7	54.9
Gain-NF	97.8	95.6	94.5	52.7
DC-THD	93.4	100	94.5	84.6
DC-THD-NF	93.4	100	94.5	84.6
THD-NF	86.8	91.2	91.2	84.6
DC-Gain-THD	100	100	97.8	89.0
Gain-THD	97.8	100	96.7	86.8
DC-Gain-NF-THD	100	100	97.8	89.0
DC-Gain-PSCM	100	98.9	97.8	90.1
PSCM-PS Ramp	98.9	98.9	96.7	92.3
Gain-PSCM	100	98.9	97.8	87.9
DC-Gain-PS Ramp	100	98.9	97.8	94.5
Gain-PS Ramp	100	98.9	97.8	93.4
DC-THD-PSCM	98.9	100	97.8	90.1
THD-PSCM	98.9	100	97.8	90.1
DC-THD-PS Ramp	98.9	100	97.8	94.5
THD-PS Ramp	98.9	100	97.8	94.5
DC-Gain-NF-PSCM	100	98.9	97.8	90.1
DC-THD-NF-PSCM	98.9	100	97.8	90.1
DC-Gain-THD-PSCM	100	100	97.8	92.3
DC-Gain-NF-PS Ramp	100	98.9	97.8	94.5
DC-THD-NF-PS Ramp	98.9	100	97.8	94.5
DC-Gain-THD-PS Ramp	100	100	97.8	95.6

TABLE VI - OPENS – MODELED WITH 1 KΩ-1000 KΩ RESISTANCE

Test Type	Fault Coverage [%]			
	1	10	100	≥ 1000
DC-PSCM-PS Ramp	**73.8**	**90.4**	**90.4**	**90.4**
DC-Gain	76.2	92.8	92.8	92.8
DC-Gain-NF	88.1	92.8	92.8	92.8
Gain-NF	88.1	92.8	92.8	92.8
DC-THD	95.2	95.2	95.2	95.2
DC-THD-NF	95.2	95.2	95.2	95.2
THD-NF	95.2	95.2	95.2	95.2
DC-Gain-THD	100	100	100	100
Gain-THD	100	100	100	100
DC-Gain-NF-THD	100	100	100	100
DC-Gain-PSCM	73.8	90.4	90.4	90.4
PSCM-PS Ramp	88.1	100	100	100
Gain-PSCM	88.1	100	100	100
DC-Gain-PS Ramp	88.1	100	100	100
Gain-PS Ramp	88.1	100	100	100
DC-THD-PSCM	100	100	100	100
THD-PSCM	100	100	100	100
DC-THD-PS Ramp	100	100	100	100
THD-PS Ramp	100	100	100	100
DC-Gain-NF-PSCM	95.2	100	100	100
DC-THD-NF-PSCM	100	100	100	100
DC-Gain-THD-PSCM	100	100	100	100
DC-Gain-NF-PS Ramp	95.2	100	100	100
DC-THD-NF-PS Ramp	100	100	100	100
DC-Gain-THD-PS Ramp	100	100	100	100

TABLE VII - NON-CATASTROPHIC AND SIZE CHANGE OF DEVICES FAULTS

Test Type	Fault Coverage [%]	
	Non-catastrophic	Size change of devices
DC-PSCM-PS Ramp	**95.2**	**100**
DC-Gain	73.8	87.5
DC-Gain-NF	73.8	87.5
Gain-NF	64.3	87.5
DC-THD	89.0	100
DC-THD-NF	89.0	100
THD-NF	89.0	100
DC-Gain-THD	90.4	100
Gain-THD	90.4	100
DC-Gain-NF-THD	90.4	100
DC-Gain-PSCM	93.4	87.5
PSCM-PS Ramp	91.2	87.5
Gain-PSCM	91.2	87.5
DC-Gain-PS Ramp	95.2	87.5
Gain-PS Ramp	95.2	87.5
DC-THD-PSCM	93.4	100
THD-PSCM	91.2	100
DC-THD-PS Ramp	91.2	100
THD-PS Ramp	95.2	100
DC-Gain-NF-PSCM	91.2	87.5
DC-THD-NF-PSCM	91.2	100
DC-Gain-THD-PSCM	93.4	100
DC-Gain-NF-PS Ramp	95.2	87.5
DC-THD-NF-PS Ramp	95.2	100
DC-Gain-THD-PS Ramp	95.2	100

For non-catastrophic faults, the same low-frequency test combination has comparable fault coverage to a combination of all examined functional tests. Interesting to note is that for the catastrophic shorts, the device shorts and the non-catastrophic faults, the structural tests, both individually, have a better fault coverage than combined gain and noise figure tests. The supply-ramp method alone has higher fault coverage for the non-catastrophic faults than any combination of the functional tests, except for DC-gain-THD combinations. It is worth to mention that performing individual or combined structural tests alone is not enough; having lower test coverage across the testing range than most combinations of functional tests. However, structural testing provides a useful alternative, where one of the functional tests can be substituted by the structural test maintaining no loss of fault coverage. To examine these possibilities different combinations of the tests have been performed as shown in tables V-VII. Emphasis is placed on replacing the most expensive and time-consuming gain and THD tests. In most cases, substituting the functional with the structural test results in no loss of fault coverage.

6. Conclusions

The fault models presented in this paper are organized according to what defect types can cause that specific circuit fault: shorts, opens, size change of devices, shorted devices and non-catastrophic faults. The results of applying structural and functional test to a study case of a wideband amplifier indicate that for the catastrophic shorts, the device shorts and the non-catastrophic faults both structural tests separately yield a fault coverage, that is favorable to the examined individual functional tests (gain, noise figure and THD). However, the individual tests alone do not have sufficient fault coverage for most of the modeled faults. To reach satisfactory levels of fault coverage different individual tests should be combined. When constructing the test sets emphasis should be placed on replacing the most expensive and time-consuming gain and THD tests and substituting them with the low-frequency structural tests. In most observed cases, this change results in no loss of fault coverage. The test-time, test-cost and test-complexity reduction achieved by this substitution is considerable. When examining only low-frequency test set, 100% fault coverage of size change of devices faults is obtained. For the modeled non-catastrophic faults, the same low-frequency test combination has comparable fault coverage to combination of all examined functional tests.

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