Post-silicon tuning capabilities of 45nm low-power CMOS digital circuits

Post-Silicon Tuning Capabilities of 45nm Low-Power CMOS Digital Circuits

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Abstract

Adaptive circuit techniques enable modification of power-performance efficient circuit operation. Yet it is unclear if such techniques remain effective in modern deep-submicron CMOS. In this paper we examine the technological boundaries of supply voltage scaling and body biasing in 45nm low-power CMOS. We demonstrate that there exists an effective tuning range for power-performance and performance variability control. Our analysis is supported by ring oscillator test-chip measurements.

Introduction

Modern integrated circuits have been equipped with supply voltage scaling (VS) and body bias (BB) tuning approaches for improving power-performance efficient operation [1-3]. Although the benefits of such design technologies are well-established, their effectiveness is strongly process technology dependent. In this paper, we explore the technological boundaries of VS and BB for a state-of-the-art 45nm low-power (LP) CMOS process. In particular, we investigate power-performance trade-offs, leakage power savings, and how far process-dependent performance spread can be tuned. Moreover, we investigate if standard-V_{th} (SVT) with BB-tuning can eliminate the need for low-V_{th} (LVT) and high-V_{th} (HVT) masks.

Test-Chip Design and Tuning Ranges

A test-chip with a size of 1.25x0.44mm^2 has been implemented in 45nm LP-CMOS (Fig.1). It contains two copies of 10 inverter-based ring oscillators (ringos) with different chain lengths which are part of the same core. Layout identical ringo instances are placed at a distance of 125µm.The test-chip contains three cores with different threshold voltage options, namely SVT, LVT, and HVT. Each core has independent power supply voltage (V_{DD}) pads for current measurements. The ground pads, and independent body bias voltage (V_{BB}) pads for PMOS (V_{nwell}) and NMOS (V_{pwell}) devices are common for all cores. Frequency, power, and leakage have been measured for 57 dies on a 300mm wafer. The measurements were performed for 0.6V-1.3V V_{DD}, and for a range of temperatures in between -40^{o}C and 125^{o}C. The nominal V_{DD} setting equals 1.1V. Moreover, a body biasing was applied ranging from 1.1V reverse body bias (RBB) up to 0.5V forward body bias (FBB). In this paper we will use a symmetrical body bias, e.g. V_{BB}=V_{pwell}=V_{DD}-V_{nwell}, and 25^{o}C, unless stated otherwise.

Power-Performance Tuning and Leakage Control

Fig. 2 shows the frequency distributions versus V_{DD} for 57 dies of a LVT, SVT, and HVT 101-stage ringo, respectively. The symbols indicate the frequency of the median sample. We measured a frequency downscaling of 7.8x (LVT), 13.4x (SVT), and 33.3x (HVT) when V_{DD} reduces from 1.1V to 0.6V. Energy and frequency trade-offs for the SVT chip sample are illustrated in Fig.3. Each cloud relates to a unique V_{DD} value, and each dot in a cloud corresponds to a unique V_{BB}. We measured a 44x power reduction, and 3.3x energy savings using VS from 1.1V to 0.6V. The use of BB at V_{DD}=1.1V provided a large frequency tuning range from -19% (1.1V RBB) till 27% (0.5V FBB) w.r.t. the nominal operating point. The frequency tuning index factors are -11% (-31%) up to 17% (41%) for a LVT (HVT) median die sample. The impact of body biasing on energy is small, even for a low circuit activity of 0.3%. For SVT, we obtained 15% energy savings at the same performance w.r.t. the nominal operating point by using combined VS and BB (V_{DD}=1.0V, 0.4V FBB). BB tuning was proposed to eliminate the use of LVT and HVT in 45nm CMOS [3]. At 1.1V V_{DD} our experiments confirm that SVT with 0.5V FBB can achieve LVT performance (Fig.4). However, this gives a 3.6x higher leakage than LVT for the median samples. VS is not preferred for achieving LVT performance due to the associated power penalty. Furthermore, we observed that SVT with RBB alone can not even achieve nominal HVT leakage (Fig.4). This is due to the small body factor (γ) available, and the presence of gate-induced drain leakage at large RBB values. Alternatively, VS alone or combined with RBB enable SVT circuits to effectively achieve HVT leakage (Fig.5). Fig.5 shows the SVT leakage current distributions versus V_{BB} for two V_{DD} values at 25^{o}C. The symbols indicate the results for the median sample. At 1.1V V_{DD} we measured 1.5x-2.8x leakage savings using optimal RBB settings. Reducing V_{DD} from 1.1V down to 0.6V is more effective (4.0x-4.5x). Combined VS+RBB provided 10x-22x leakage savings. The actual leakage savings are strongly temperature dependent (Fig.6). The dominant leakage components determine if VS or RBB is more effective. VS+RBB showed maximum leakage savings around 75^{o}C for the SVT median sample. The location of this maximum depends on process skew, and V_{th} option used.

Performance-Spread Compensation

The impact of systematic and random process variability on ringo timing has been determined by means of a clock-period correlation plot (Fig.7). The clock-period of two closely located layout-identical ringos has been correlated for each die sample. The statistical delay spread of an 11-, 21-, 31-, 41- and 101-stage ringo has been calculated for three BB values at 1.1V V_{DD} (Fig.8). In Fig.8, the solid and open symbols relate to the 3σ systematic and random delay spread, respectively. The trend lines are extrapolated from the 101-stage ringo, which are closely matching the results from the other ringos. Observe that the delay spread reduces consistently when FBB is applied, while it increases for RBB. Fig.9 shows a more detailed analysis for the 21-stage ringo. The total delay spread is about 2x lower for 0.5V FBB w.r.t. the nominal BB case. Contrarily, the spread is about 2x higher for 1.1V RBB. Observe that FBB can significantly reduce both systematic and random delay spread in 45nm LP-CMOS. Fig.10 puts in perspective the clock period mean and 3σ-spread versus V_{BB} for the 21-stage ringo. A ±11% spread was observed at the nominal operating point. This spread could be fully compensated through BB tuning using up to 0.2V FBB for slow die samples, and up to 0.7V RBB for fast die samples. Frequency and leakage was measured for all available samples (Fig.11). For each die sample, it was possible to tune its frequency to the nominal target spec through BB tuning. We required a BB range from 0.1V RBB up to 0.2V FBB. This gives basically an enhancement to 100% parametric yield for our sample set. We measured a 32% frequency increase with 0.5V FBB for the slowest die sample at a 26x leakage penalty. This offers sufficient tuning range for compensating process-dependent performance spread.

Conclusions

Test-chip measurements show that VS and BB remain effective in 45nm LP-CMOS. We demonstrated the presence of large power-performance modification capabilities. For SVT circuits, VS enables 3.3x energy savings when the frequency can be reduced by 13.2x. Combined VS+BB results in 15% energy savings at no frequency penalty, and 10x-22x leakage savings at 25^{o}C. BB tuning offers sufficient range to achieve process-related performance spread compensation. Moreover, FBB can effectively reduce timing uncertainty, e.g. we observe a 2x lower delay spread at 0.5V for a 21-stage SVT ringo. Finally, SVT+FBB can mimic LVT performance, while SVT+RBB can not achieve HVT leakage.

References

[1] Tschanz et.al., *VLSI 2002*, pp. 310-311.

[2] Nomura et.al., *ISSCC 2008*, pp. 262-263.

[3] Gammie et.al., *ISSCC 2008*, pp. 258-259.

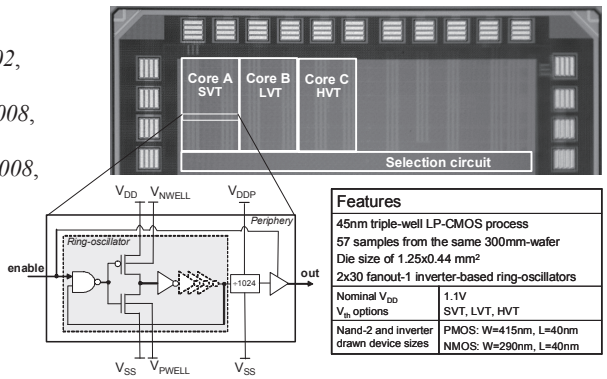


Figure 1. Test-chip photograph and description

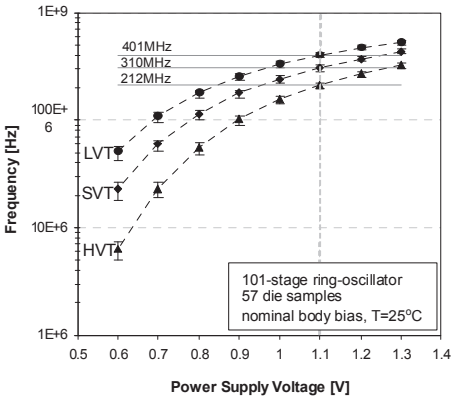


Figure 2. Frequency vs. V_{DD} trends

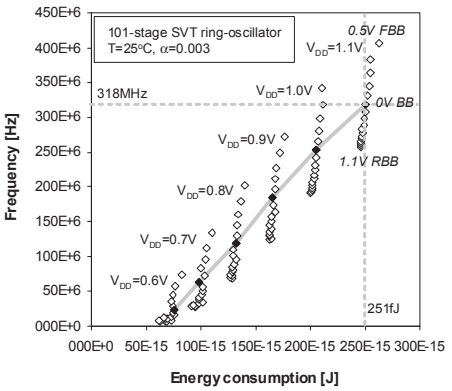


Figure 3. Frequency vs. energy trade-offs for a 101-stage SVT ring-oscillator

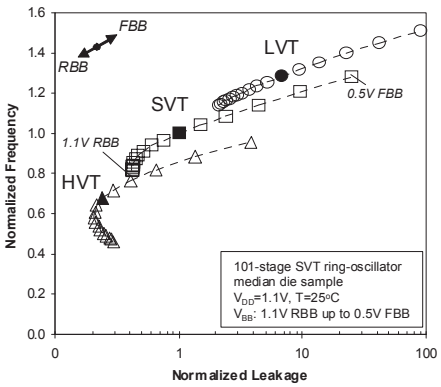


Figure 4. Frequency vs. leakage for a BB-tuned 101-stage ring-oscillator

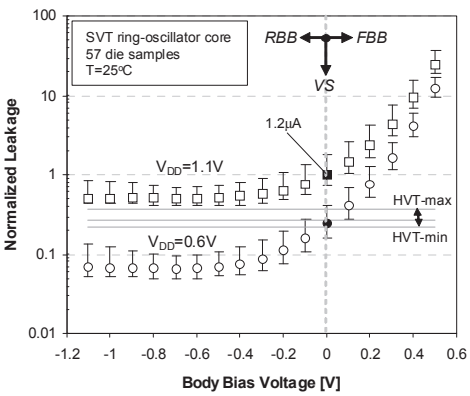
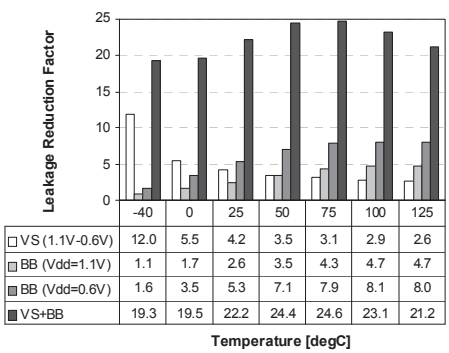


Figure 5. SVT leakage vs. V_{BB} for two distinct V_{DD} values at 25°C



	-40	0	25	50	75	100	125
VS (1.1V-0.6V)	12.0	5.5	4.2	3.5	3.1	2.9	2.6
BB (Vdd=1.1V)	1.1	1.7	2.6	3.5	4.3	4.7	4.7
BB (Vdd=0.6V)	1.6	3.5	5.3	7.1	7.9	8.1	8.0
VS+BB	19.3	19.5	22.2	24.4	24.6	23.1	21.2

Figure 6. VS and BB dependent leakage savings vs. temperature for an SVT ring-oscillator core

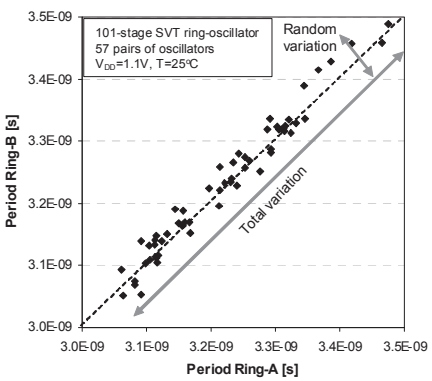


Figure 7. Clock period correlation plot of two layout-identical 101-stage SVT ring-oscillators

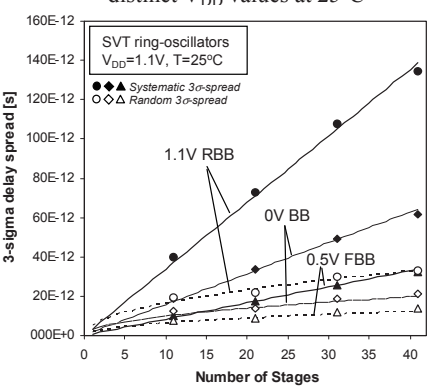
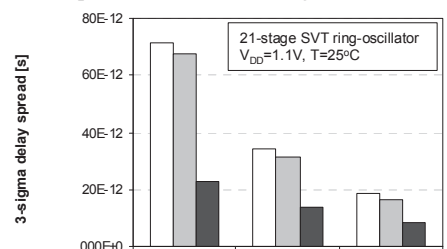


Figure 8. Systematic and random delay spread vs. number of ring-oscillator stages



	-1.1	0	0.5
Total spread	71.50E-12	34.36E-12	18.59E-12
Systematic spread	67.68E-12	31.43E-12	16.52E-12
Random spread	23.05E-12	13.88E-12	8.52E-12

Figure 9. Estimated delay spread for the available 21-stage SVT ring-oscillators

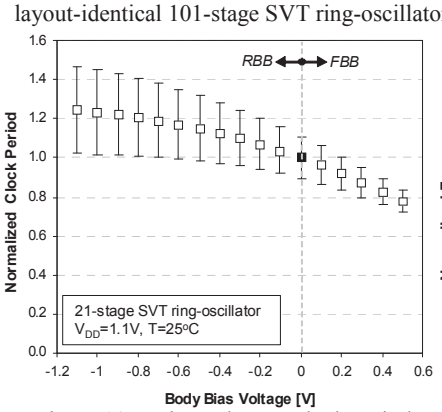


Figure 10. Estimated mean clock period and spread for 21-stage SVT ring-oscillator

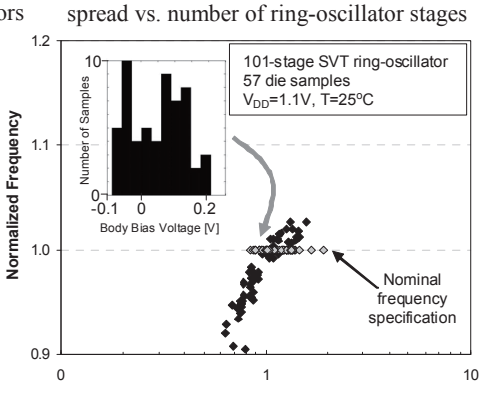


Figure 11. Performance spread compensation