Design, realisation and test of GaAs-based monolithic integrated X-band high-power amplifiers

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Aan Elly en Wesley

Contents

1. Introduction

The use of integrated microwave circuits, for both commercial and military applications, has come to full bloom during the last decade. Military applications, in particular phased-array radar and Electronic Warfare systems, initially stimulated the development of Monolithic Microwave Integrated Circuits (MMICs). Nowadays, further development is mainly driven by the demands of the telecommunication market. Increased demand from the commercial sector has resulted in a further maturing of the existing technology based on MEtal Semiconductor Field Effect Transistors (MESFET). Other technologies based on Heterojunction Field Effect Transistors (HFET) and Heterojunction Bipolar Transistors (HBT) have also emerged during the last decade and are now available for commercial application. The main drive for the use of MMICs is their potential for cost and size reduction. Cost reduction results from the integration of several functions on a single chip. In addition, test and mounting costs are reduced and system reliability is improved. Improved performance is obtained because the on-chip and chip-to-chip component spread is minimal. The cost reduction that is possible through the application of MMICs makes the realisation of systems such as phased-array radar economically feasible; the size reduction makes them technologically feasible. The high-power amplifiers discussed in this thesis are mainly intended for application in phased-array radar antenna systems. For this reason first a short introduction regarding phased-array radar antennas and the Transmit Receive (TR) module, which is used for each antenna element, will be given.

1.1 High-power amplifiers for phased-array radar

The development of phased-array radar originates from the increased demands upon radar systems. An example is the necessity to have multiple antenna beams simultaneously. One antenna beam is then for instance used for tracking a detected object while at the same time another beam is used for missile guidance. An active phased-array radar antenna consists of a number of antenna elements, which each have their own Transmit Receive module. The working principle of a linear phased-array antenna is visualised in figure 1.1. The antenna bundle is steered by giving each antenna element a different relative phase shift when compared to the other elements.

A phased-array antenna can consist of a few to several thousands of TR modules [1.1]. This large amount of TR modules requires the use of cheap highly integrated components to make the realisation of phased-array antennas economically feasible. The use of Monolithic Microwave Integrated Circuits (MMIC) is of vital importance for the realisation of this objective. In figure 1.2, the nowadays most commonly used components in a TR module are shown. The indicated phase shifter (φ) and amplitude regulator (ATT) control the direction and the shape of the antenna pattern. The output power required to achieve a specified detection range is generated with the help of the depicted high-power amplifier (HPA).

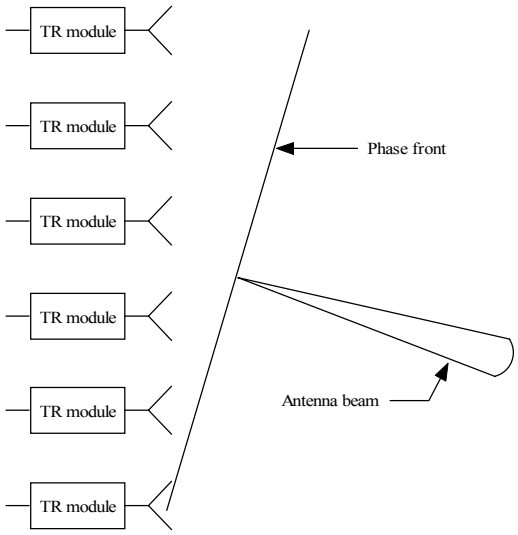

Figure 1.1: Phased-array antenna principle.

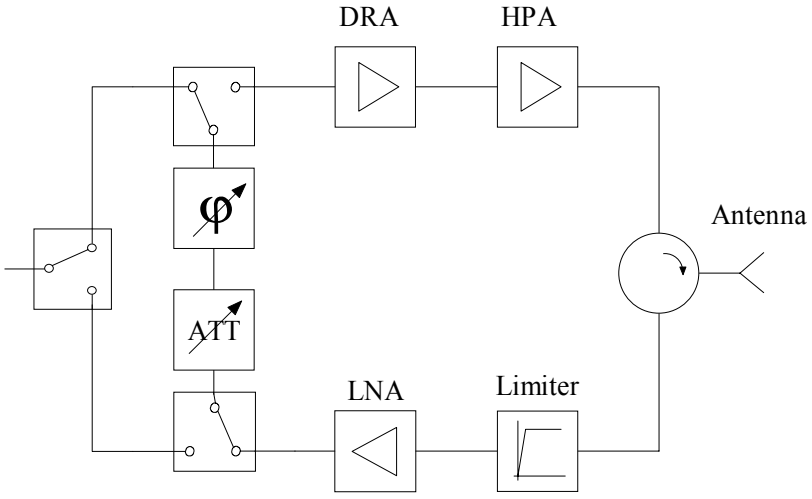

Figure 1.2: Overview of MMICs used in TR module.

In the receive channel a low noise amplifier (LNA) is used to amplify the incoming radar signal. The TR module depicted in figure 1.2, shows the situation commonly encountered at the start of the work in 1992. The TR module topology foreseen for the near future is shown in figure 1.3. Most of the functions are integrated into one multi-function chip (MFC). Examples of such multi-function chips are described in literature [1.2, 1.3]. Probably the LNA and limiter will be integrated into one single chip.

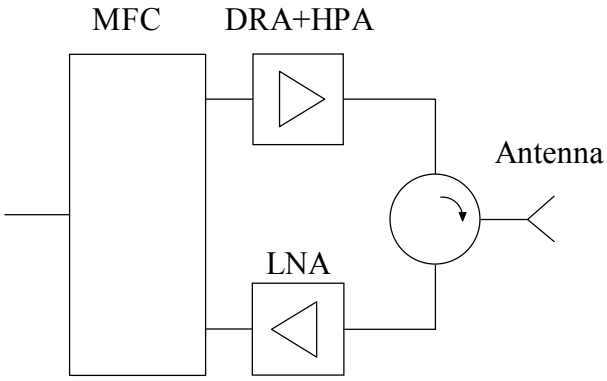

Figure 1.3: TR module architecture for future phased-array radar systems [1.2, 1.3].

The high-power amplifier will be combined with the driver amplifier (DRA) onto a single chip. This indicates that a high-power amplifier is an important separate TR module component at this moment and will stay to be so in the foreseen future. The development of high-power amplifiers as a MMIC is the subject of this thesis. In the next section, the objectives of the work and content of this thesis will be discussed in detail.

1.2 Problem, goal and organisation

1.2.1 Problem and goal

The design of integrated microwave high-power amplifiers at X-band (8.0 - 12.4 GHz), that have both a broad bandwidth and a high efficiency, is the problem investigated in this thesis. These high-power amplifiers will be realised on GaAs wafers in two different transistor technologies, namely a MEtal Semiconductor Field Effect Transistor (MESFET) technology and a pseudomorphic Heterojunction Field Effect Transistor (HFET) technology.

At the start of the work described in this thesis:

- No procedure for the design of microwave integrated high-power amplifiers was available.
- No models for the transistors were available.
- The models for the passive components were inaccurate or even unavailable.
- No measurement systems were available for both the characterisation of high-power amplifiers and active and passive components including transistors, capacitors etc.

The primary goal pursued in this thesis therefore is, to give a systematic overview of all design steps that are necessary to realise a successful wideband high-efficiency microwave high-power amplifier. In addition, the component models and the measurement methods, developed in the scope of this thesis, which form an integral part of the design

methodology, are discussed. The final goal, which is pursued, is an investigation of the feasibility of the realisation of an X-band single chip combined driver and high-power amplifier.

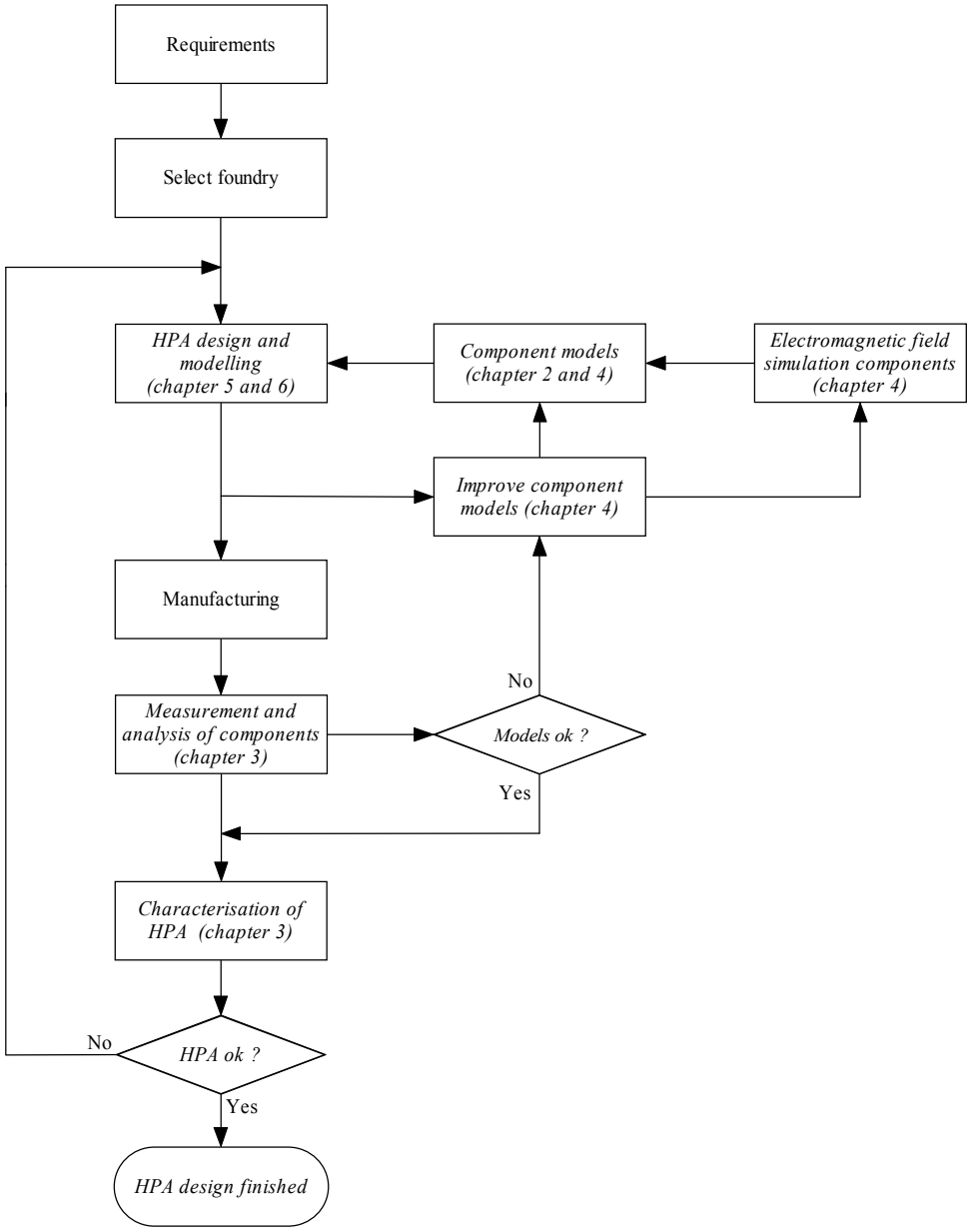

Figure 1.4: High-power amplifier design flow and the relevant chapter numbers.

1.2.2 Organisation

An overview of the dominant factors for the design of high-power amplifiers is shown in figure 1.4. The subjects indicated in *italics* are discussed in detail in this thesis. The design always starts from a set of requirements. Based on the requirements, a foundry is selected that has a technology that is suited to realise the desired specification. After the foundry is selected, the actual high-power amplifier design starts. The procedures developed for the amplifier design will be discussed in detail in chapters 5 and 6. Essential inputs for the design are the active and passive components available in the given technology. In chapter 2 an overview is given of these available components along with their limitations when they are used for high-power amplifier design at X-band. This brings us to an important issue namely the necessity to include the effect of parasitic elements in the component models. The higher the frequency band of interest the more important this becomes. The models used are discussed in chapter 4. The information for both model development and verification comes from two different sources: electromagnetic field simulations and measurements. The measurement systems, developed in the scope of the work described in this thesis, are discussed in chapter 3. Information obtained with the help of these systems is used for component modelling and verification, but is also used for the design of the matching networks that are part of the high-power amplifier. The selection of the transistor layout, operating class and the influence of the selected transistor on the high-power amplifier are discussed in chapter 5. In chapter 6, the design of the high-power amplifiers is discussed. The measurement results of the realised high-power amplifiers are summarised in chapter 7. Finally in chapter 8 a number of conclusions and recommendations will be given.

1.3 References

[1.1] J. Bennett, K. Lewinski, P. Shearing, B. Velsher, J. van Houten and A. Tiesenga, “Quadpack X-band T/R Module for Active Phased Array Radar”, *GAAS’98 Symposium Digest*, pp. 63-67, October 1998.

[1.2] A. de Boer, M.W. van der Graaf, A.P. de Hek and T.C.B. Tieman, “A GaAs Multi-Function X-band MMIC for Space Based SAR Application with 7 bit Phase and Amplitude Control”, *GAAS’98 Symposium Digest*, pp. 215-220, October 1998.

[1.3] A. de Boer and K. Mouthaan, “GaAs Mixed Signal Multi-function X-band MMIC with 7 Bit Phase and Amplitude Control and Integrated Serial to Parallel Converter”, *GAAS’00 Symposium Digest*, pp. 476-479, October 2000.

2. Components

2.1 Introduction

To choose for the right technology is of vital importance for obtaining a good high-power amplifier performance. In this thesis, technology will be used interchangeably with process. The term technology covers the substrate material, the transistor layer stack, the passive components and the possible geometry of these components. The amplifiers discussed in this thesis are realised with the help of two different technologies. The first one is a MESFET technology, which is mature and already allows for the development of high-power amplifiers on a commercial basis. The second one is a HFET technology, which originally was less mature than the MESFET technology. The HFET technology used was optimised by the foundry during the work described in this thesis. This HFET technology makes the development of a combined driver and high-power amplifier on a single chip feasible. The HFET high-power amplifiers were realised on 3" wafers and the MESFET high-power amplifiers were realised on 4" wafers. Today the production of the MESFET process is using 6" wafers [2.1] and the HFET process 4" wafers, clearly demonstrating the rapid development of GaAs related processes. For the work described in this thesis, we had access to the DIOM20HP MESFET process of Infineon and the power HFET process of the Fraunhofer Gesellschaft-Institut für Angewandte Festkörperphysik (FhG-IAF). The choice for these two technologies was a sensible one at the start of the high-power amplifier design work in 1992. At that time, the alternative would have been a technology based on HBTs. However, at that time HBTs suffered from large reliability problems. Nowadays the situation is different and HBTs are an important option for every power amplifier application up to X-band as well. Above these frequencies, HFET technology is now the only viable option due to the available gain of HFETs. Industrial GaAs-based power HBT processes are available that have a reported Mean Time To Failure (MTTF) of more than 10^6 hours at 125 °C and a current density of 25 kA.cm^{-2} [2.2]. The reliability of MESFET or HFET transistors is still better than before quoted MTTF for HBTs. For instance, Triquint quotes at a junction temperature of 150 °C a MTTF of more than 10^6 hours for their PHEMT process and more than 10^8 hours for their MESFET process.

In the remainder of this chapter, the active and passive components available in before mentioned technologies are discussed from a technology point of view. Where relevant also the limitations, such as the breakdown voltage of the transistor, are discussed. This chapter starts with the discussion of the used substrate material Gallium Arsenide (GaAs). The reasons why this substrate material is used are discussed, and a comparison is made with some other substrate materials that have potential for future high-power amplifier design. In section 2.3 and section 2.4 respectively, the active and passive components used for the amplifier design are discussed. The parameter extraction and device modelling of both the active and passive components is discussed in detail in chapter 4 after discussing the necessary measurement systems in chapter 3.

2.2 Gallium Arsenide

The substrate material that is used for the amplifiers described in this thesis is GaAs. This substrate material has been the workhorse for the microwave industry for the development of MMICs, during the last decades. An important advantage of GaAs over Silicon (Si), which is commonly used at lower frequencies, is the fact that substrates as well as epitaxial layers can be made semi-insulating. This semi-insulating property is a prerequisite for monolithic integration of active and passive components and low-loss transmission lines. In table 2.1 the basic properties of GaAs, Silicon, Silicon Carbide (SiC) and Gallium Nitride (GaN) are compared at room temperature.

Table 2.1: Comparison of material properties [2.3]. For the breakdown field $N_D = 1.10^{17}$ cm^{-3} is taken into account. The electron and hole mobility is given for $N_A = N_D = 1.10^{16}$ cm^{-3}.

Material	ε_r	E_G [eV]	Breakdown field [$V.m^{-1}$]	Electron mobility [$m^2V^{-1}s^{-1}$]	Hole mobility [$m^2V^{-1}s^{-1}$]	Saturation velocity [$m.s^{-1}$]	Thermal conductivity [$W.K^{-1}m^{-1}$]
GaAs	12.8	1.43	65.10^6	0.600	0.033	1.10^5	46
Si	11.8	1.11	60.10^6	0.135	0.045	1.10^5	150
4H-SiC	9.7	3.20	35.10^7	0.080	0.012	2.10^5	490
GaN	9.0	3.40	35.10^7	0.100	0.030	15.10^4	130

The materials GaN and SiC are added because they form interesting materials for future high-power amplifier designs. The first reason is their higher breakdown voltage, which gives a higher output power per occupied chip area and a second reason is the better thermal properties of the latter materials. At this moment in time they are, however, not an option to be considered in much detail in this thesis because these technologies are not yet available as a mature process. The thermal conductivity of GaAs is relatively poor when compared to the other materials listed in table 2.1. This is a point of concern for the development of the high-power amplifiers where a lot of heat is generated on a relatively small chip area. Because of this bad thermal conductivity, special countermeasures have to be made to reduce the gate finger temperature as much as possible. This will be discussed in more detail in chapter 5. Note that there is a direct relation between the reliability of the active devices and the temperature of the gate fingers [2.4]. Most failure mechanisms exhibited by semiconductors are due to the diffusion of atoms. Higher temperatures accelerate this diffusion process. The relation between reaction rate R and temperature is given by the Arrhenius equation [2.4]:

$$R = C \cdot e^{\frac{-E_a}{k \cdot T}} . \tag{2.1}$$

In this equation, C is a constant, k the Boltzmann constant, T the absolute temperature in [K], and E_a is the activation energy [eV]. The activation energy is a measure how effectively a failure mechanism utilises thermal energy. The effect of temperature variations can be described with the help of the acceleration factor,

$$AF = e^{\left(\frac{E_a}{k}\left(\frac{1}{T_0}-\frac{1}{T_A}\right)\right)}. \tag{2.2}$$

In this equation, T_0 is the actual operating temperature and T_A is the accelerated temperature. The actual activation energies of the transistors used cannot be given here due to the non-disclosure agreements signed with the foundries. The maximum gate finger temperature that was considered to be acceptable by the foundries was approximately 125 °C. In the remainder of this section, the active and passive components, relevant for high-power amplifier design that can be realised on GaAs will be discussed.

2.3 Active components

2.3.1 Introduction

In this section, the active components used in the high-power amplifier designs are discussed. In section 2.3.2 the working principle of the MESFET, which is used in most of the developed high-power amplifiers, is discussed. In this section also the figures of merit for high-power amplifier transistors, are discussed. The HFET is discussed in section 2.3.3. This section is concluded with a discussion of the various types of transistor layouts and their significance to high-power amplifier design in general will be highlighted.

2.3.2 Metal Semiconductor Field Effect Transistor

The MESFET has been the workhorse of the microwave industry during the last decades. This technology is mature and cheap compared to the HFET technology discussed in the next section. At this moment in time the realisation of high-power amplifiers based on MESFET technology is still attractive because it is a relatively cheap and well-proven technology.

The MESFET technology used is the Self-Aligned Gate (SAG) DIOM20HP high-power technology of Infineon [2.5]. This technology allows the realisation of MMICs with a relatively small number of process steps. A simplified cross section of a MESFET is shown in figure 2.1; the space charge region is indicated beneath the gate contact.

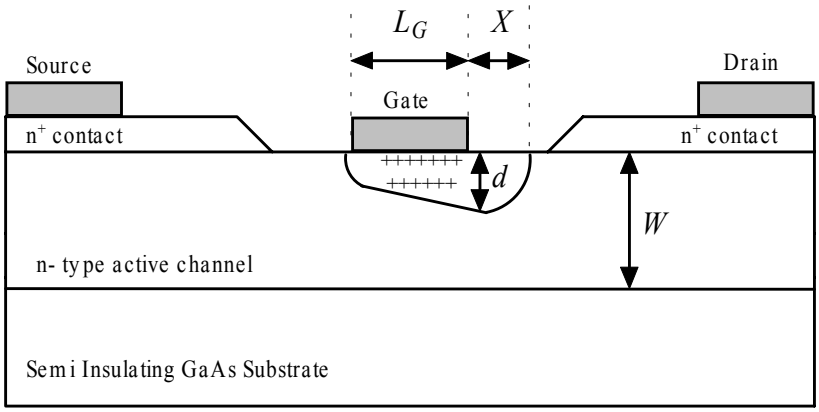

Figure 2.1: Simplified cross section MESFET.

The MESFET consists of three metal electrodes that are connected to the active channel. The drain and source contacts to the active channel are made with the help of ohmic contacts. The current that flows from the drain to the source contact is controlled with the help of the voltage that is applied between the gate and the source electrode. The type of transistor used in this thesis is of the so-called depletion mode. This means that when no gate-source voltage is applied there still will flow a drain-source current. The gate contact is a Schottky barrier. This barrier forms a region beneath the gate that is completely free of charge carriers. Consequently, no current can flow through this region. This region can be further extended into the active channel by applying a more negative gate-source voltage. The voltage, at which the drain-source current ceases to flow through the active channel, is called the pinch-off voltage.

For the discussed MESFET, current saturation occurs for most drain-source voltages due to saturation of the electron drift velocity. The electron drift velocity as a function of the applied electric field E can be calculated with the help of the following equations [2.6]:

$$\upsilon(E) = \mu_0 \cdot E + \left(-2 \cdot \mu_0 \cdot E_C + 3 \cdot \upsilon_{sat1}\right) \cdot \frac{E^2}{{E_C}^2} + \left(\mu_0 . E_C - 2 \cdot \upsilon_{sat1}\right) \cdot \frac{E^3}{{E_C}^3}, \qquad (2.3)$$

when $0 \le E \le E_C$ and ,

$$\upsilon(E) = \upsilon_{sat2} + \left(\upsilon_{sat1} - \upsilon_{sat2}\right) \cdot e^{\left[-\alpha \cdot \left(\frac{E - E_C}{E_C}\right)^n\right]}, \qquad (2.4)$$

if $E > E_C$. In this equation μ_0 is the low-field mobility, E_C the critical electric field, υ_{sat1} the peak velocity and υ_{sat2} the final saturation velocity, υ_{sat2} is in the remainder of this thesis referenced to as υ_{sat}. The factors α and n are fitting factors, which model the transition of the low-field mobility region to the saturated velocity region. In table 2.2, some typical values for GaAs are listed [2.6, experiment 19].

Table 2.2: Parameters for GaAs at T = 300 K used in equations (2.3) and (2.4). The values of the listed parameters are taken from literature [2.6, experiment 19].

μ_0 [$m^2.V^{-1}.s^{-1}$]	E_C [$V.m^{-1}$]	υ_{sat1} [$m.s^{-1}$]	υ_{sat2} [$m.s^{-1}$]	α	n
0.75	36.10^4	216.10^3	114.10^3	1.429759	1.26092

Equations (2.3) and (2.4) are used in combination with the numbers listed in table 2.2 to calculate the velocity as a function of the electric field as depicted in figure 2.2. The depicted results show a peak in the velocity at a low electric field E_C. For small gate lengths, the corresponding drain-source voltage is also low. At electric fields above E_C, the electron-velocity saturates rapidly.

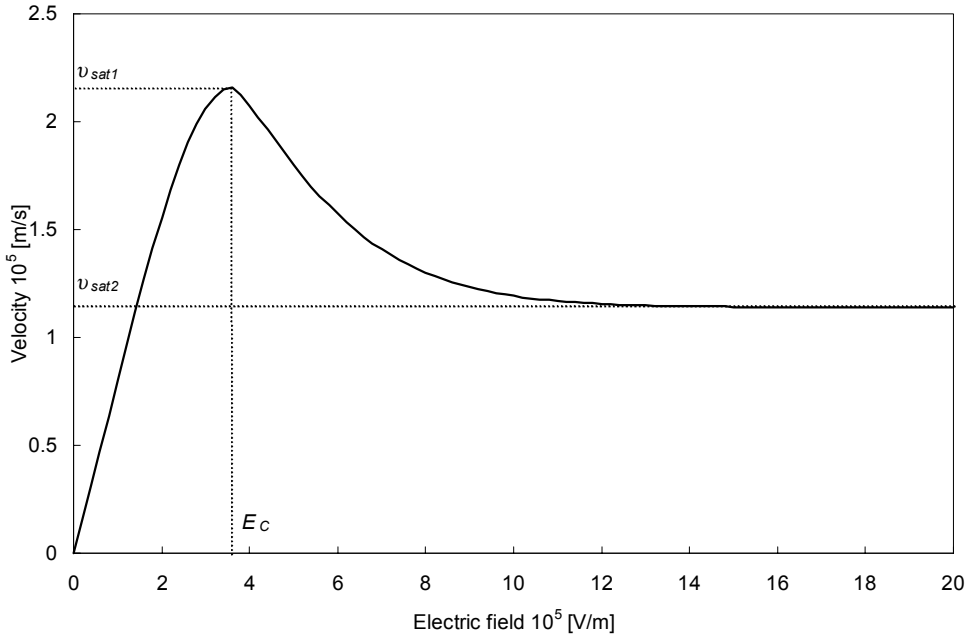

Figure 2.2: Velocity-electric field curve calculated for GaAs with the help of the numbers listed in table 2.2.

The active channel of the MESFET is formed with the help of n-type doped material. For high frequency transistors most of the time an n-type doping is used instead of p-type because n-type material has a higher saturation velocity than p-type material, see table 2.1.

This higher saturation velocity results in a higher cut-off frequency as can be seen from the following equation [2.7]:

$$f_T = \frac{\upsilon_{sat}}{2 \cdot \pi \cdot (L_G + X/2)}. \tag{2.5}$$

The cut-off frequency is defined as the frequency where the magnitude of the current gain of the transistor is reduced to one under the consideration that the output terminal of the transistor is short-circuited. In this equation (2.5), X is the extension of the space-charge layer into the gate-drain space as indicated in figure 2.1. This extension of the space-layer is bias dependent, as can be witnessed from [2.7]:

$$X \leq \sqrt{\frac{2 \cdot \varepsilon_0 \cdot \varepsilon_r}{q \cdot N_D \cdot (V_{B0} - V_{GSI})}} \cdot (V_{B0} - V_{GDI}). \tag{2.6}$$

Consequently, also the cut-off frequency is bias dependent. Another important parameter that limits the highest operating frequency is the length of the gate L_G (figure 2.1), see equation (2.5) for the cut-off frequency of the intrinsic FET [2.7]. This equation shows that the cut-off frequency becomes higher when the gate length L_G becomes smaller. The gate length is 0.5 µm for the DIOM20HP MESFETs. This results, ignoring parasitic or extrinsic FET elements, in a theoretical cut-off frequency of approximately 30 GHz. The parasitic elements of the transistor further reduce the cut-off frequency to approximately 12 GHz, see figure 2.4.

The cut-off frequency can also be written as a function of the equivalent circuit model parameters. A simplified model of an intrinsic FET is depicted in figure 2.3, a more detailed transistor model will be discussed in chapter 4.

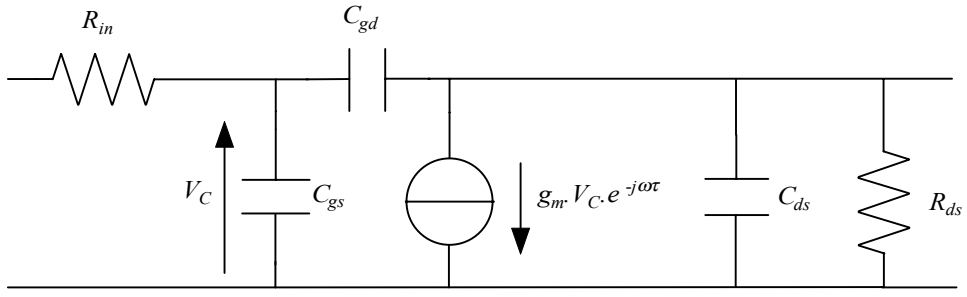

Figure 2.3: Simplified intrinsic transistor model.

For this simplified intrinsic FET model, the cut-off frequency can be calculated with [2.7],

$$f_T = \frac{g_m}{2 \cdot \pi \cdot \left(C_{gs} + C_{gd}\right)}. \tag{2.7}$$

The power gain G_P of a transistor is a very important figure of merit. The power gain of the simplified model depicted in figure 2.3 can be calculated as follows [2.7, page 223]:

$$G_P = \left(\frac{f_T}{f}\right)^2 \cdot \frac{1}{R_{in}} \cdot \frac{\left|Z_{ds}\right|^2 \cdot \left|Z_L\right|}{\left|Z_{ds} + Z_L\right|^2}, \tag{2.8}$$

where C_{gd} is set to zero. This simplifies the calculations and avoids stability problems by enforcing a unilateral device. In this equation Z_{ds} is the parallel impedance of R_{ds} and C_{ds} and Z_L is the load impedance, which is applied to the transistor. From the equation for the power gain, it can be concluded that:

- The cut-off frequency of the transistor should be as high as possible to obtain a high power gain,
- The power gain of the transistors is reduced when the frequency is increased. The consequences of this gain reduction and methods to compensate for it will be discussed in detail in chapter 5 and 6. In the remainder of this thesis this gain reduction as a function of frequency is indicated with the term gain roll-off.

Another figure of merit, which is at least as important as the cut-off frequency, is the maximum frequency of oscillation f_{MAX}. This maximum frequency of oscillation is defined by the frequency where the power gain of the transistor becomes equal to unity. The maximum frequency of oscillation can be calculated with the following equation:

$$f_{MAX} = f_T \cdot \sqrt{\frac{n_L}{\left(1 + n_L\right)^2}} \cdot \sqrt{\frac{R_{ds}}{R_{in}}}, \tag{2.9}$$

with n_L being the ratio between the value of the drain-source resistance and the real part of the load impedance (R_{ds} / R_L). In this equation, it is assumed that the parallel capacitor C_{ds} is resonated out at the frequency of interest with the help of a parallel inductor. The maximum power gain under small-signal conditions is then obtained when the real part of the load impedance is taken equal to the drain-source resistance (R_{ds}) of the transistor (n_L = 1). Under large-signal conditions this is no longer the case because the real part of the load impedance is dictated by the output power required (n_L > 1), see section 5.4. Therefore, under large-signal conditions the power gain and f_{MAX} will be lower than under small-signal conditions.

Equation (2.9) shows that the maximum frequency of oscillation is higher than the cut-off frequency. This is the case because in the saturated region R_{ds} is an order of magnitude larger than R_{in}. In practice, f_{MAX} / f_T is typically 1.5 to 2. The cut-off frequency and the maximum oscillation frequency of a MESFET, which has a total gate width of 1.5 mm and a gate length of 0.5 µm, are depicted in figure 2.4. The cut-off frequency and the maximum

oscillation frequency are calculated with the help of the small-signal equivalent transistor model parameters.

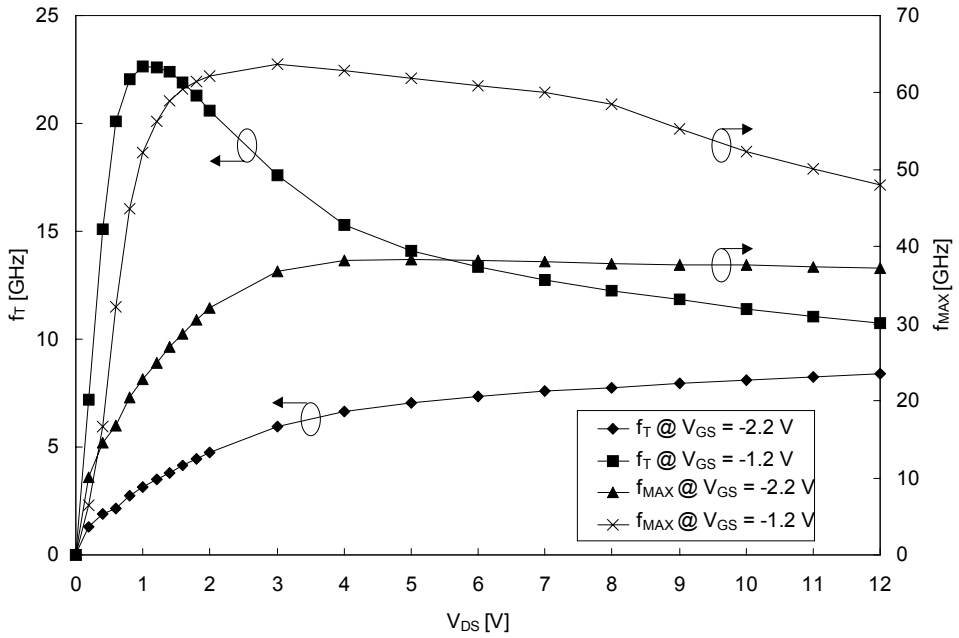

Figure 2.4: Extracted f_T and f_{MAX} of a MESFET as a function of both the drain-source and gate-source voltages. The DIOM20HP transistor has a total gate width of 1.5 mm and a gate length of 0.5 µm.

The results show that both f_T and f_{MAX} are bias dependent as already was concluded from equations (2.5) and (2.6). The cut-off frequency of the transistors discussed in this thesis (typical V_{DS} = 9 V) is close to 12 GHz, which is also the high end of the desired frequency band. On the other hand, the maximum frequency of oscillation is much higher. Therefore, the transistors can still be used for the design of high-power amplifiers at X-band.

Important figures of merit of the used transistors are besides the gain, also the output power and power added efficiency. The idealised IV curves showing the factors that limit the output power are depicted in figure 2.5. The output power (P_{OUT}) capability of the used transistor can be estimated with the help of the following equation:

$$P_{OUT} = \frac{(I_{MAX} - I_{MIN}) \cdot (V_{MAX} - V_{MIN})}{8}. \tag{2.10}$$

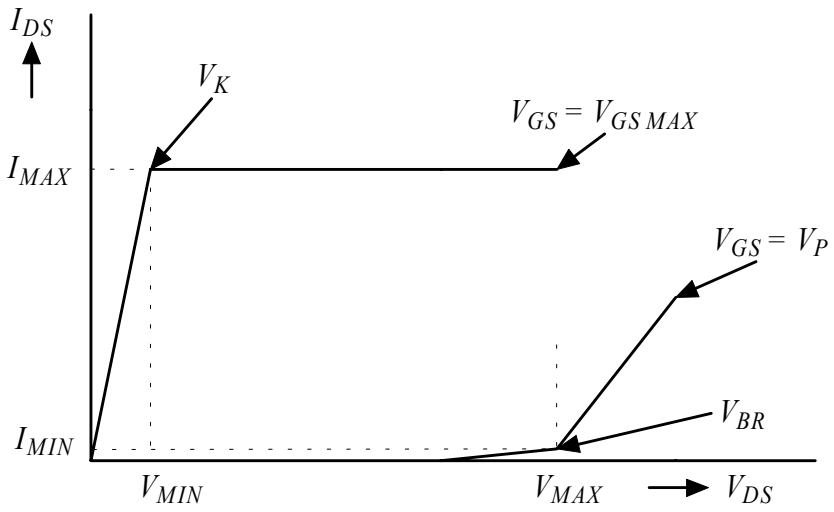

Figure 2.5: Idealised DC IV curves.

The following limiting factors for the output power are observed from the idealised DC IV curves. The maximum open channel current I_F limits the current swing, so $I_{MAX} = I_F$. For simplicity the minimum drain current I_{MIN} is considered to be zero. It is good to note that the maximum open channel current is considerably higher than I_{DSS}, which is some times used. According to [2.7] the maximum open channel current is given by:

$$I_F = q \cdot N_D \cdot Z_G \cdot \upsilon_{sat} \cdot (W - d_{\min}). \tag{2.11}$$

From this equation, it can be seen that the maximum forward current I_F is determined by technology related parameters. These parameters are; the total gate width of the transistor Z_G, the doping density N_D, the saturation velocity υ_{sat} of electrons in the n-doped GaAs, the channel thickness W and the minimum extension of the depletion region into the channel d_{min}, see also figure 2.1. In practice, a lower value has been used for the maximum current I_{MAX} because that current occurs at a gate-source voltage that is higher than the built-in potential of the Schottky diode. Consequently, a large gate current (> 10 mA per finger) starts to flow. This large gate current causes electron migration of the gate metal and results in a reduced reliability of the transistor. Therefore, the gate current per finger was limited for the used transistors to a maximum of 2 mA/finger, see also chapter 6. The resulting maximum drain current is found at a gate-source voltage that approximates the built-in potential of the Schottky diode (≈ 0.8 V).

The load impedances of the transistor should be chosen such that the voltage swing stays within the limits formed by the knee voltage V_K and the breakdown voltage V_{BR}. The knee voltage is determined by the value of the parasitic drain and source resistance, and the drain-source resistance in combination with the maximum current I_{MAX}. The knee voltage is given by the following equation:

$$V_K = (R_s + R_d + R_{ds}) \cdot I_{MAX} \,. \tag{2.12}$$

The voltage swing is limited for higher voltages by the breakdown voltage of the transistor. In equation (2.13) an expression is given for the breakdown voltage [2.7, page 169]:

$$V_{BR} = \frac{1}{2} \cdot \left(\frac{E_B \cdot L_G}{q \cdot N_D \cdot W} \cdot \left(\varepsilon_0 \cdot \varepsilon_r \cdot E_B - q \cdot N_D \cdot W \right) - \frac{q \cdot N_D \cdot W^2}{\varepsilon_0 \cdot \varepsilon_r} \right). \tag{2.13}$$

This simple expression shows the major influence of the material properties on the breakdown voltage. For instance when the doping density increases the breakdown voltage is reduced and the maximum drain current is increased. This kind of relation between the maximum drain current and the breakdown voltage is also observed for the technologies used in the discussed high-power amplifiers. Comparison of equation (2.11) and equation (2.13) shows that there exists a relation between the maximum drain current in the forward direction and the breakdown voltage. When the minimum voltage and current are assumed to be zero the following equation can be found for the output power:

$$P_{OUT} = \frac{1}{16} \cdot \left(\frac{E_B \cdot L_G}{q \cdot N_D \cdot W} \cdot \left(\varepsilon_0 \cdot \varepsilon_r \cdot E_B - q \cdot N_D \cdot W \right) - \frac{q \cdot N_D \cdot W^2}{\varepsilon_0 \cdot \varepsilon_r} \right) \cdot q \cdot N_D \cdot \upsilon_{sat} \cdot \left(W - d_{\min} \right) \tag{2.14}$$

A logical choice for the drain voltage of a transistor would be the middle of the sum of the knee voltage and the breakdown voltage, see equation (2.15). Such a choice guarantees the maximum possible voltage swing without damaging the transistor,

$$V_{DS} = \left(\frac{V_K + V_{BR}}{2} \right). \tag{2.15}$$

Nevertheless this maximum drain voltage was not used for the high-power amplifier designs discussed in this thesis. The reason is the fact that the voltage, calculated with help of equation (2.15), is always higher than the drain voltage that was available from the system in which the amplifiers are used. For the power MESFETs discussed here, the drain to gate spacing is larger than the source to gate spacing. This is done to improve the breakdown voltage of the FET. The measured breakdown voltage under DC conditions is approximately 20 V. Note that the DC breakdown voltage for a MESFET or an HFET is not similar to the RF breakdown behaviour [2.8]. Under RF conditions, the carriers may not achieve sufficient energy to cause avalanche breakdown and therefore a higher breakdown voltage is obtained. For all discussed MESFET amplifiers a drain bias voltage of V_{DS} = 9 V was used. Therefore, the breakdown voltage is not the limiting factor for the voltage swing but the knee voltage is. The knee voltage of the used MESFETs is 1.5 V, and the average measured drain current at V_{GS} = 0.8 V is 365 mA/mm. These values suggest an output power

capability based on DC limits of 0.68 W/mm, output power density results measured under RF conditions will be discussed in chapter 5.

The last figures of merit, which need discussion, are the drain efficiency and the Power Added Efficiency (*PAE*) of the transistor. The drain efficiency is given by:

$$\eta_D = \frac{P_{OUT}}{P_{DC}} . \tag{2.16}$$

In this equation, P_{DC} is the dissipated DC power. A more relevant factor for describing the transistor efficiency is the power added efficiency (*PAE*), because the latter efficiency also considers the gain of the transistor. The power added efficiency is defined with the help of the following equation:

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}} \cdot \left(1 - \frac{1}{G_P}\right). \tag{2.17}$$

This equation shows that the power added efficiency is directly related to the drain efficiency of the transistor and the power gain of the transistor.

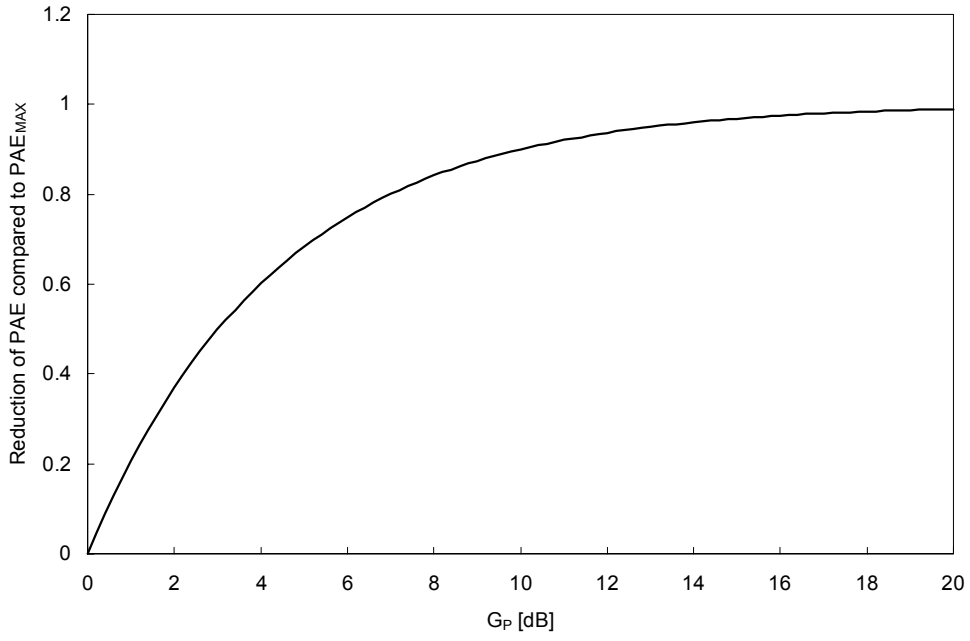

Figure 2.6: Reduction of the PAE of a transistor compared to its maximum value (PAE_{MAX}) as a function of the power gain.

In addition, it can be concluded that the power gain of the transistor (G_P) should be as high as possible to obtain an as high as possible power added efficiency, see figure 2.6. In practice, a power gain below 10 dB is considered unacceptable in terms of power added efficiency reduction. The power gain of a single transistor has, in a multi-stage power amplifier, also influence on the overall power added efficiency of the amplifier. This influence is discussed in more detail in chapter 5.

Other relevant parameters that determine the transistor performance are the number of gate fingers and the width of these gate fingers. These parameters are discussed in more detail in chapter 5.

2.3.3 Heterojunction Field Effect Transistor

For the design of advanced microwave power amplifiers, which can be used for the realisation of combined driver and high-power amplifiers, the HFET technology of FhG-IAF [2.9, 2.10] is used. A simplified cross section of a HFET is shown in figure 2.7. Note that in the literature many different names are encountered for the transistor type that is called HFET in this thesis, examples are High Electron Mobility Transistor (HEMT) and MOdulation Doped FET (MODFET).

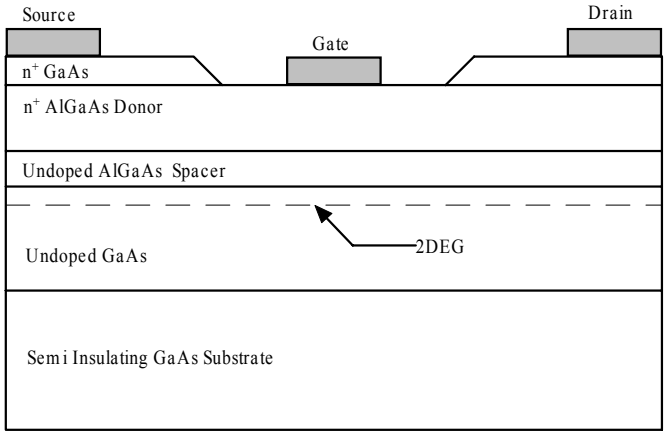

Figure 2.7: Simplified cross section of a HFET.

The HFET technology used, has significant advantages over the MESFET technology presented in the previous section:

- More power gain, 14 dB compared to 10 dB at 12 GHz, see chapter 5 for more details. Due to this increased gain, there is less reduction of the power added efficiency and fewer amplifier stages can be used to realise the combined driver and high-power amplifier discussed in chapter 1.

- More output power per gate width, values up to 0.9 W/mm have been measured at X-band compared to 0.7 W/mm for the MESFET technology, see chapter 5 for more details. Therefore, a higher output power can be realised at the same chip area with the HFET technology, as it will be demonstrated in chapter 7.

Above-mentioned factors make the realisation of a single chip high-power amplifier combined with a driver amplifier with the help of HFET technology possible.

The HFET has, similar to the MESFET, three metal electrodes that respectively are called drain, source and gate. The contact to the active channel is made for the drain and the source with the help of an ohmic contact. The gate is realised with the help of a Schottky barrier. The better high frequency performance of a HFET when compared to a MESFET is due to the existence of a so-called two dimensional electron gas (2DEG). Figure 2.8 shows the energy-band diagram of an $Al_xGa_{1-x}As$-GaAs heterojunction. Note that the bandgap is higher for $Al_xGa_{1-x}As$ compared to GaAs. This heterojunction is in thermal equilibrium when no external voltage is applied. The $Al_xGa_{1-x}As$ is doped n-type, while the GaAs is only lightly doped. To achieve thermal equilibrium electrons will flow from the wide-bandgap $Al_xGa_{1-x}As$ into the GaAs, forming an accumulation layer of electrons in the potential well adjacent to the interface. This accumulation layer is referred to as two-dimensional electron gas. The electrons have quantized energy levels in the plane perpendicular to the interface, in the other two directions the electrons are free to move. The 2DEG is an undoped region, therefore the electrons moving through this gas do not encounter ionised atoms, and therefore high electron mobility is obtained.

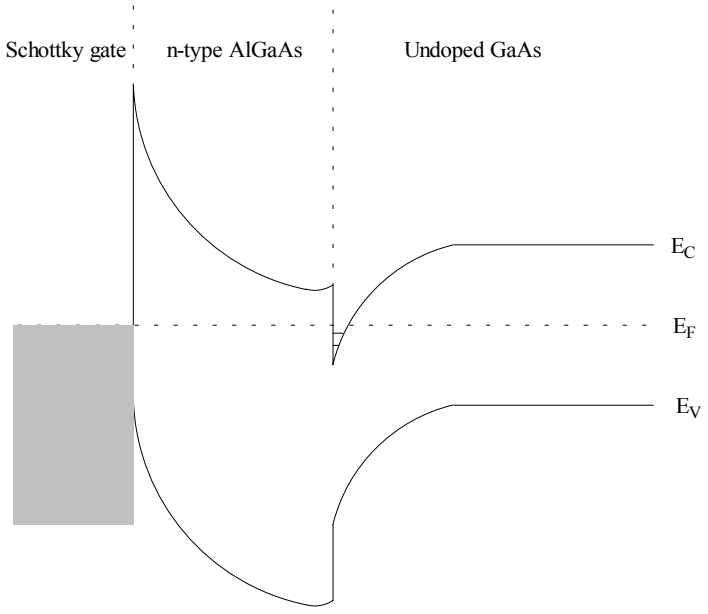

Figure 2.8: Energy band diagram HFET transistor, which is in thermodynamic equilibrium.

The available HFETs are of the depletion mode type. This means that current will flow through the active channel when no gate voltage is applied. The amount of current through the active channel can be controlled with the help of the voltage applied to the gate. Similar to the MESFET there exists a gate voltage denoted pinch-off voltage at which the current through the active channel is reduced to zero. In addition, current saturation will occur at higher drain-source voltages, due to the saturation of the electron velocity at higher field strengths. As in a MESFET, the current flow through a HFET can be controlled by applying a voltage between the gate and source of the transistor. However, in the case of a HFET, not the height of the active channel is varied, as it was the case for the MESFET but the electron density of the electron gas. When the undoped layer on top of the 2DEG is not sufficiently depleted, conduction through this layer will start to occur. The conduction through this layer is similar to the conduction in a MESFET. This so called parasitic MESFET has inferior transport characteristics when compared to the 2DEG and as a result the HFET performance is degraded as parasitic MESFET conduction starts to occur.

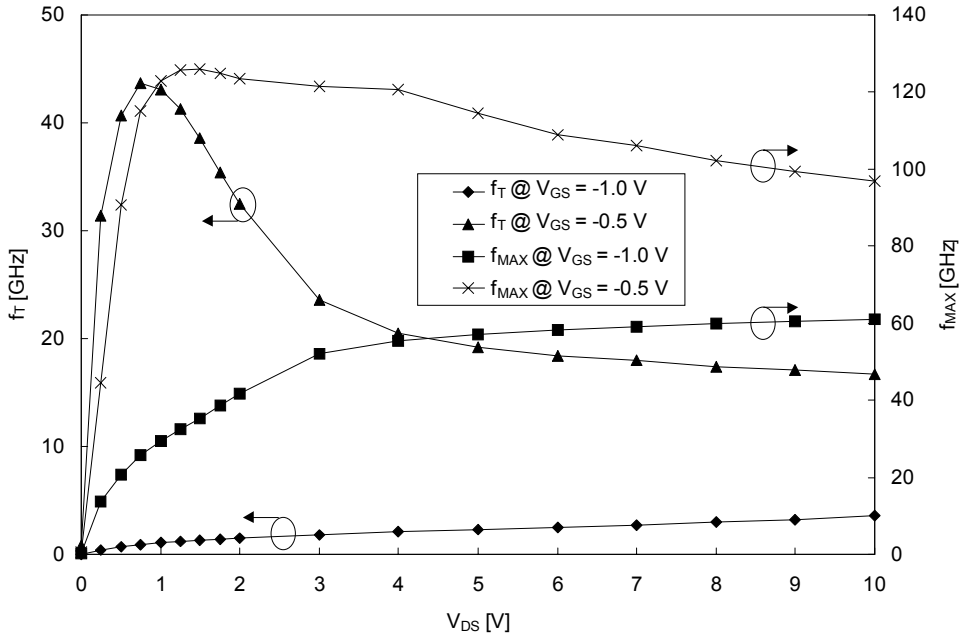

Figure 2.9: Extracted f_T and f_{MAX} of a HFET as a function of both the drain-source and gate-source voltages. The HFET has a total gate width of 1.44 mm and a gate length of 0.3 µm.

The gate length of the HFETs used in this thesis is 0.3 µm. An asymmetric source to gate and drain to gate spacing is used to improve the breakdown voltage. The gate-source spacing is 0.3 µm and the drain-gate spacing is 0.9 µm [2.10]. This large drain-gate spacing is used to improve the breakdown voltage of the HFET. The in this way realised breakdown voltage is > 20 V. For all HFET amplifiers a V_{DS} = 8 V was used. The knee voltage of the

HFETs used is 1.25 V and the average measured drain current at V_{GS} = 0.8 V is 526 mA/mm. The minimum drain current is assumed to be zero. These values suggest an output power capability based on DC limits of 0.89 W/mm, results measured under RF conditions will be discussed in chapter 5.

The cut-off frequency and the maximum frequency of oscillation of the HFET can be described with the same equivalent circuit that was used for the MESFET, see figure 2.3. The frequencies f_T and f_{MAX} extracted from measurements for a HFET with a total gate width of 1.44 mm and a gate length of 0.3 µm are depicted in figure 2.9. The results show a similar bias dependency of the cut-off frequency and maximum oscillation frequency, as it was the case for the used MESFET. The absolute values, however, are significantly higher than was the case for the MESFET. This is quite logical taking into account the smaller gate length of the HFET of 0.3 µm compared to the 0.5 µm gate length of the MESFETs.

The layout of actual power transistors, which connects more than one gate finger in parallel, is more complex than is shown in this section. The layouts of the transistors used for the high-power amplifier design are discussed in the next section.

2.3.4 Transistor Layout

To form a power transistor several gate fingers have to be connected in parallel because the width of the gate finger should not be increased beyond 125 µm for X-band transistors. Above this width, the gain of a transistor becomes unacceptably low. This gain reduction is discussed in more detail in chapter 5. Consequently, more gate fingers have to be connected in parallel to increase the output power of a transistor. The way these gate fingers can be connected in parallel is independent of the transistor type used, i.e. MESFET or HFET, or the foundry used. In fact, the transistor layout is an extra design freedom, which should be considered carefully. The transistor layouts used in the high-power amplifiers described in this thesis are shown in figure 2.10.

It turned out that the fishbone transistor layout gives the highest output power per chip area [2.11]. This is the case because for a large total gate width the fishbone layout results in a squarer layout of the transistor. In a high-power amplifier, a number of transistors must be used in parallel, as it will be discussed in chapter 5, to realise a required amount of output power. When more output power is required, the number of gate fingers in parallel must be increased. In the case of the interdigitated transistor, this will increase the height of the occupied chip area. Consequently, also the height of all matching networks is unnecessarily increased. This is not the case for the fishbone transistor layout where only the width of the bar of transistors that are placed parallel is increased. The width and height of the matching networks, see chapter 6, can stay at their minimal dimensions. The fishbone transistor has the additional advantage of higher gain. This is because more gate fingers with a smaller width are put in parallel than is the case for an interdigitated transistor of the same overall gate width. This is discussed along with the thermal details in much more detail in chapter 5.

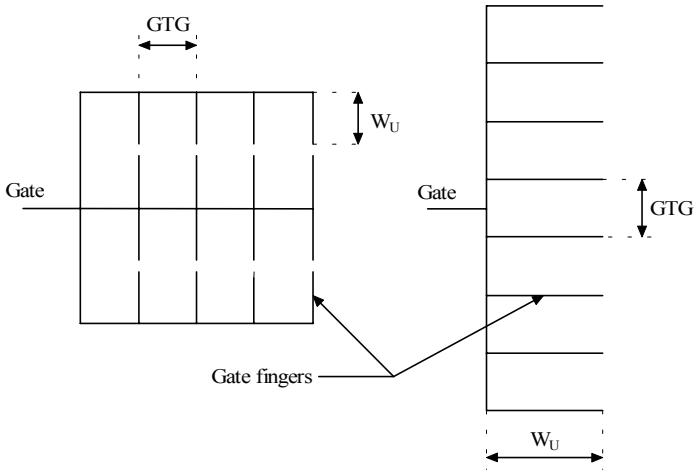

Figure 2.10: Simplified schematic of gate finger connections for a 16 finger fishbone (left) and an 8 finger interdigitated (right) transistor layout. The indicated important parameters are the gate-to-gate spacing (GTG) and the unit gate width of one finger (W_U).

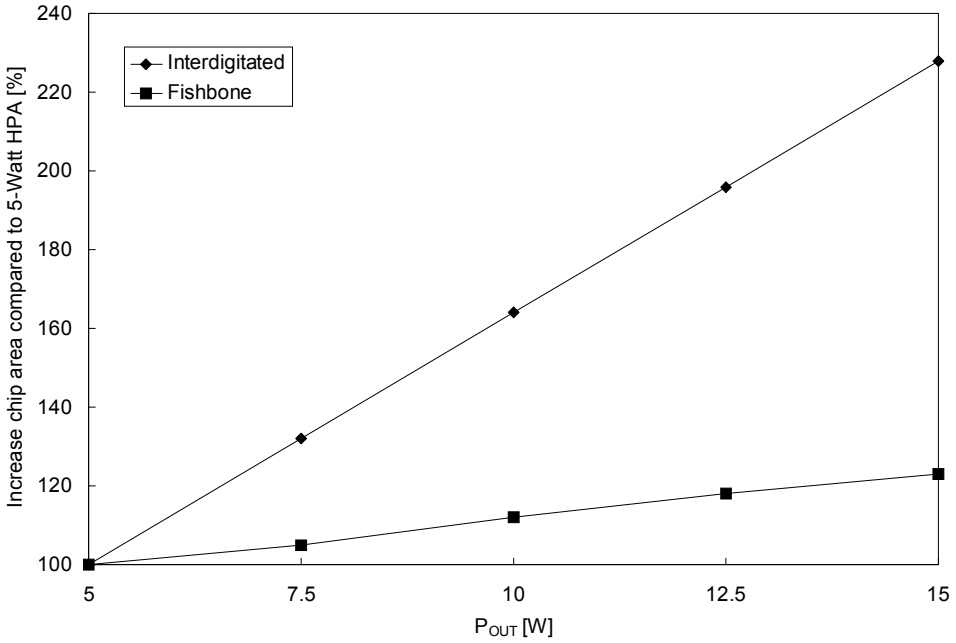

Figure 2.11: Example of the increase in occupied chip area [2.11], when compared to a 5-Watt amplifier, as a function of the required output power.

An example of the chip area increase when going to a higher output power is depicted in figure 2.11. These results clearly show that transistors with a fishbone layout result in a smaller increase in occupied chip area than interdigitated transistor layouts.

Additional layout related factors that limit the performance of a transistor are:

- The minimum width of the gate, drain and source strips which is limited by the maximum current that is allowed to flow through a given microstrip line width.
- The maximum allowable channel temperature limits the spacing between the gate fingers. This is discussed in detail in section 5.3.5.

2.4 Passive components

2.4.1 Microstrip line

The interconnections between the different components can be realised with the help of various types of transmission lines. In figure 2.12, an overview is shown of the most commonly used transmission lines on a MMIC.

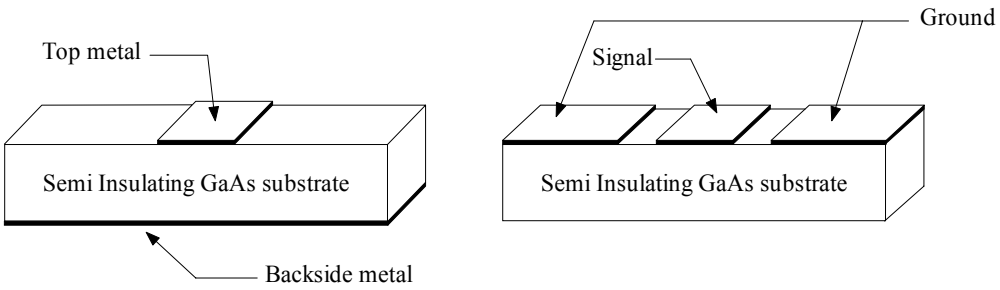

Figure 2.12: Overview of commonly encountered types of transmission lines on GaAs. The microstrip line is depicted left and the coplanar transmission line is depicted right.

Coplanar lines need fewer processing steps than microstrip lines due to the absence of wafer thinning, viahole etching, filling viahole with metal, and metallisation of the complete backside of the chip, which is necessary for a microstrip design. Therefore, a technology based on coplanar lines is potentially cheaper than one based on microstrip lines. At the start (1992) of the high-power amplifier design work, coplanar lines had the following disadvantages when compared to microstrip lines [2.12]:

- Hardly any electrical models for coplanar transmission lines and discontinuities were available.

- Coplanar waveguide supports multiple modes, some of which may be excited at discontinuities. This increases the design risk.
- Coplanar structures are realised on thick substrates, typically >500 µm; therefore, heat transfer becomes a problem for high-power amplifier designs, see also chapter 5.
- Coplanar lines exhibit somewhat higher losses than microstrip lines. A 1 mm long transmission line with a characteristic impedance of 50 Ω, a metal thickness of 5 µm, and a centre conductor width of 68 µm gives a loss of 0.054 dB for the microstrip line case and 0.066 dB for the coplanar line case [2.15].

Therefore, microstrip lines were chosen as transmission lines. In the for this work available MESFET process of Infineon and HFET process of FhG-IAF the microstrip lines are realised on 100 µm thick GaAs substrates. The reasons for this thickness are:

- The range of microstrip line impedances that can be realised with the help of small line widths, 10 – 100 µm, is larger than is the case with thick wafers. Therefore, more compact MMICs can be realised. The microstrip line impedances depicted in figure 2.13 show that an impedance between 40 and 100 Ω can be realised on 100 µm thick GaAs wafers.
- Lower inductance of the viahole to ground. This results for instance in a higher gain of the transistors because there is less frequency dependent feedback caused by the viaholes.
- The thermal properties are better.

The connection to ground is realised with the help of viaholes, see section 2.4.6.

Many of the disadvantages of the usage of coplanar lines mentioned before, have been resolved nowadays [2.13]. Cost savings up to 40% have been reported for a coplanar flip-chip high-power amplifier at X-band [2.14]. The heat is removed for the before mentioned high-power amplifier through the utilisation of thermal bumps at the sources of the used PHEMTs. Therefore in the future, coplanar transmission lines should be seriously reconsidered for high-power amplifier design. Nevertheless for the amplifiers discussed in this thesis only microstrip elements have been used.

The transmission line impedances, shown in figure 2.13, are calculated with the help of Linecalc [2.15]. The impedance levels are limited at the high end by the smallest line width that can be processed and at the low end by the occupied chip area, in practice line widths between 10 and 120 µm are used.

The maximum current that can flow through a cross section of a microstrip line limits the use of microstrip lines, for high-power amplifier design. This is especially important for the microstrip lines that are used to supply the bias currents to the transistors. The amount of current that is allowed to flow, is for a given microstrip line width, determined by the thickness of the microstrip line metal. The metal thickness of the microstrip lines varies between 3 and 5 µm for the used technologies. This results in current density per microstrip line width of 20 mA/µm for the lines directly on the GaAs and a value of 15 mA/µm for the airbridges.

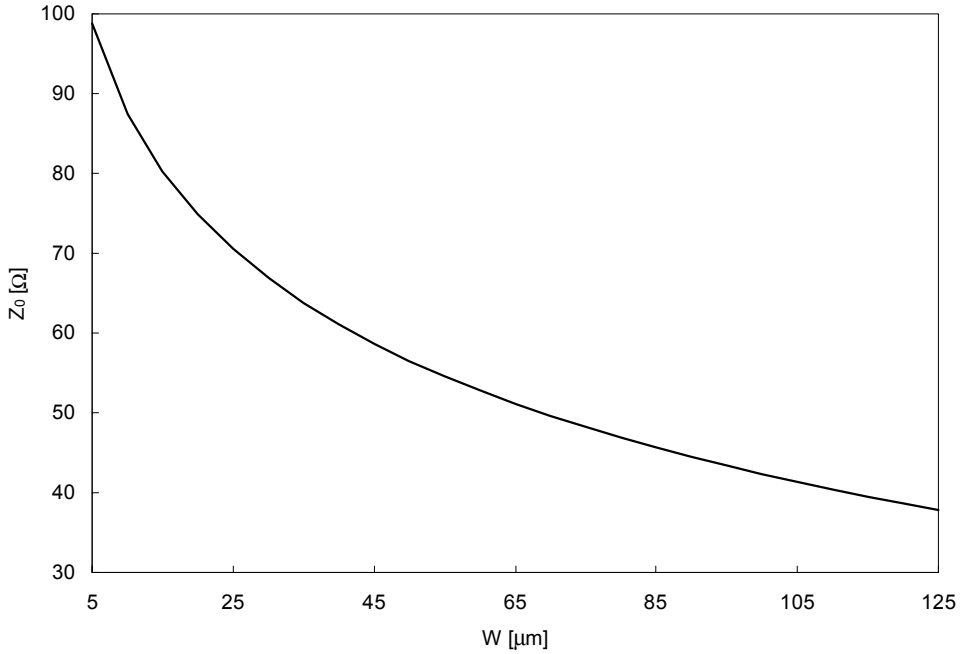

Figure 2.13: Calculated characteristic microstrip line impedance as a function of the line width for a 100 µm thick GaAs wafer [2.15]. The metal thickness of the microstrip line is 5 µm.

The characteristic impedance of the microstrip lines is influenced by process variations. The major process variations are:

- Variation of the thickness of the substrate. The GaAs substrates used have a nominal thickness of 100 µm. For the variation of this thickness a value of ± 10 µm is quoted.
- Variation of the line width. For the variation of the line width a value smaller than ± 1 µm is assumed.
- Variation of the thickness of the line metal. For this, a maximum variation of ± 1 µm is quoted.

These factors lead, besides variations in the characteristic impedance of the lines, also to variations of the effective dielectric constant of the transmission line. The results depicted in figures 2.14 and 2.15 show that the influence of process variations on the characteristic impedance of the line is considerably higher than the influence on the effective dielectric constant. In addition, it is show that for the relevant line widths (> 30 µm) the major influence on the characteristic impedance of the line is the substrate height. The error in the predicted impedance increases when the line width is increased. For a line width of 100 µm, the maximum variation in the characteristic impedance is ± 6%. The maximum variation in the dielectric constant is ± 1.5%.

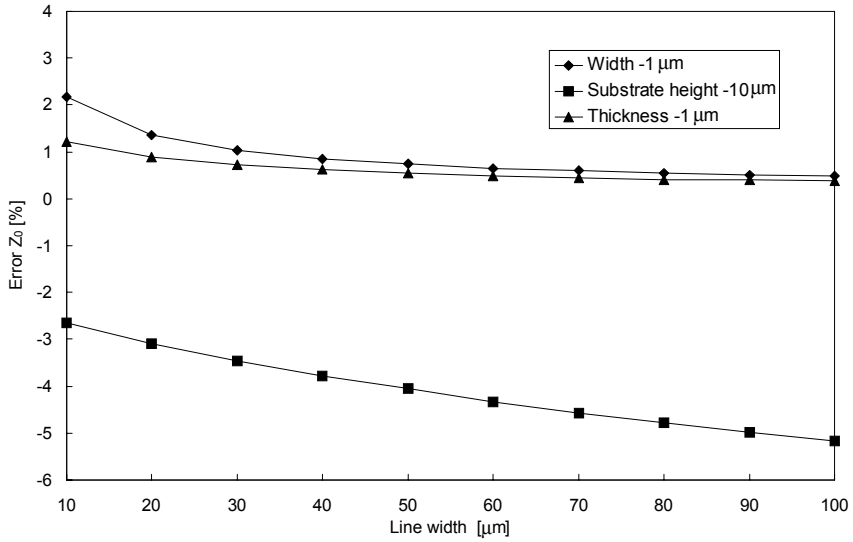

Figure 2.14: Influence of process variations on the characteristic impedance (Z_0) transmission line, values are calculated at 10 GHz and a substrate thickness of 100 µm and a metal thickness of 3 µm.

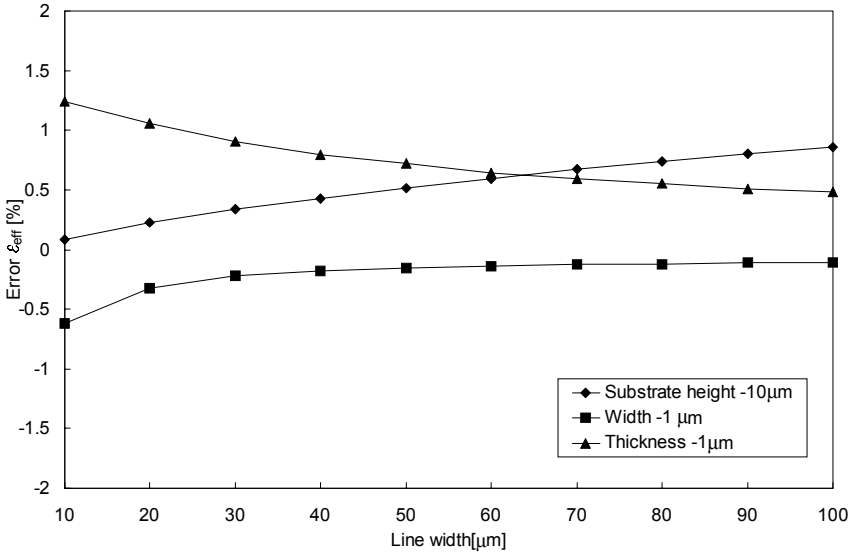

Figure 2.15: Influence of process variations on the effective dielectric constant (ε_{eff}) transmission line, values are calculated at 10 GHz and a substrate thickness of 100 µm and a metal thickness of 3 µm.

2.4.2 Microstrip discontinuities

Microstrip circuits generally require structures like bends, T-junctions, crosses etc., to form matching networks. These junctions result in discontinuities, which no longer can be ignored at X-band frequencies, and therefore accurate models are needed, see chapter 4. The use of the before mentioned junctions is limited by the maximum current that will flow through a given cross section as it is the case for the microstrip lines discussed in the previous section. In addition, the discontinuities are influenced by the same processing variations as the microstrip lines. For the discontinuities, equivalent circuit models mainly consisting of series inductors and parallel capacitors are used. These models will be discussed in detail in chapter 4. The parallel capacitors are mainly influenced by variations of the GaAs substrate. Therefore, a maximum variation of ± 10% can be expected for the parallel capacitor. The series inductors are influenced by variations in the characteristic impedance and the dielectric constant of the discontinuity, see section 4.3.4. For the series inductors, a maximum variation of ± 7% is expected.

2.4.3 Inductor

Inductors are available for application in MMICs. For low power MMICs most of the time spiral or square inductors are used, see figure 2.16.

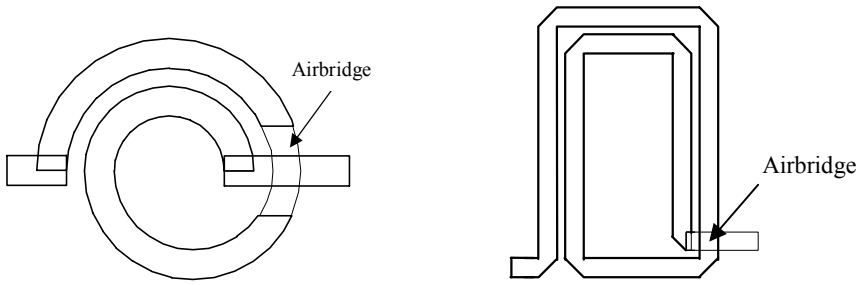

Figure 2.16: Two possible layouts of inductors realisable on a MMIC.

Inductors are used in matching networks and for DC bias de-coupling. The application of spiral or square inductors in high-power amplifiers is problematic due to the high currents that will flow through relative small microstrip line widths. Inductors have line widths up to 15 µm. Consequently the inductors can breakdown under high-power conditions. Therefore, only inductors that are realised with the help of microstrip lines have been used. The use of microstrip lines as inductor with the corresponding model is discussed in section 4.3.4.

The influence of process variations of inductors realised with the help of a microstrip line is the same as was quoted for the microstrip discontinuities discussed in the previous section.

2.4.4 Capacitor

The availability of capacitors is crucial for the realisation of matching networks and DC de-coupling networks. A capacitor can for instance be realised with the help of a parallel stub that is left open. Disadvantages of this method are the fact that only small capacitors can be realised in this way, only parallel capacitors can be realised and DC blocking is not possible. Therefore, this kind of capacitor is not used in the discussed high-power amplifier designs. There are two possibilities to realise lumped capacitors namely Metal Insulator Metal (MIM) capacitors and interdigitated capacitors. A picture of both types of capacitors is shown in figure 2.17.

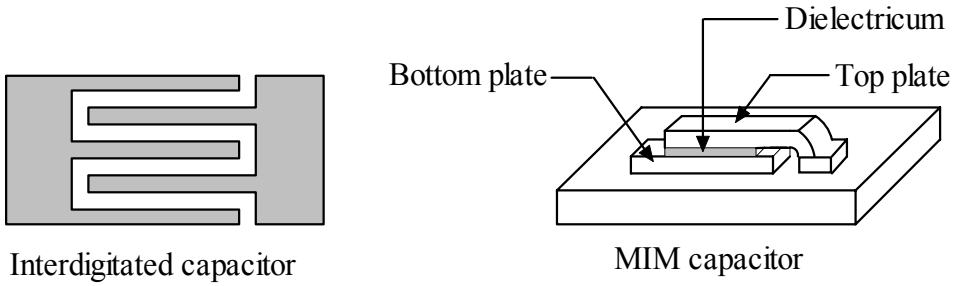

Figure 2.17: Examples of possible layouts of an interdigitated (left) and a MIM capacitor (right).

The interdigitated capacitor is based on the coupling between narrow microstrip lines. With the help of this type of capacitor, only small capacitance values can be realised [2.16]. Due to the low capacitance per area, as shown in figure 2.18, only capacitors < 0.5 pF can be realised. Therefore, this type of capacitor was not used in the discussed high-power amplifier designs. Recently an alternative planar capacitor based on a fractal has been described [2.17] which makes it possible to realise larger capacitance values per area than was possible until now.

The capacitor type that is used for the discussed high-power amplifier designs is the MIM capacitor. This capacitor is formed with two metal plates on top of each other with a dielectric in between. This dielectric is also often used as a passivation layer to protect the MMIC. To be able to realise high capacitance values it is important to use an as thin as possible dielectric with a high permittivity. As dielectric often, Silicon Nitride (Si_3N_4) or Silicon Oxide (SiO_x) is used. Typical values for the capacitance per area vary between 200 and 400 pF/mm^2. These values are considerably higher than the values shown in figure 2.18 for the interdigitated capacitors. In practice, capacitor values up to 5 pF have been realised for the discussed amplifier designs. Larger capacitance values would result in an unacceptable large occupied chip area.

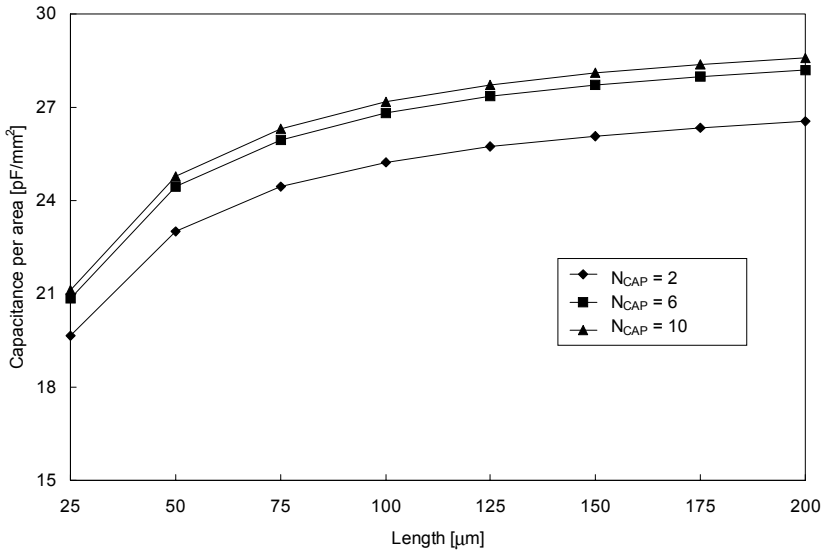

Figure 2.18: Calculated capacitor value per area of an interdigitated capacitor as a function of the number fingers (N_{CAP}) and the length of these fingers [2.16]. The width of each finger is 2 µm and the spacing between the fingers is 2 µm. The thickness of the metal is 0.8 µm.

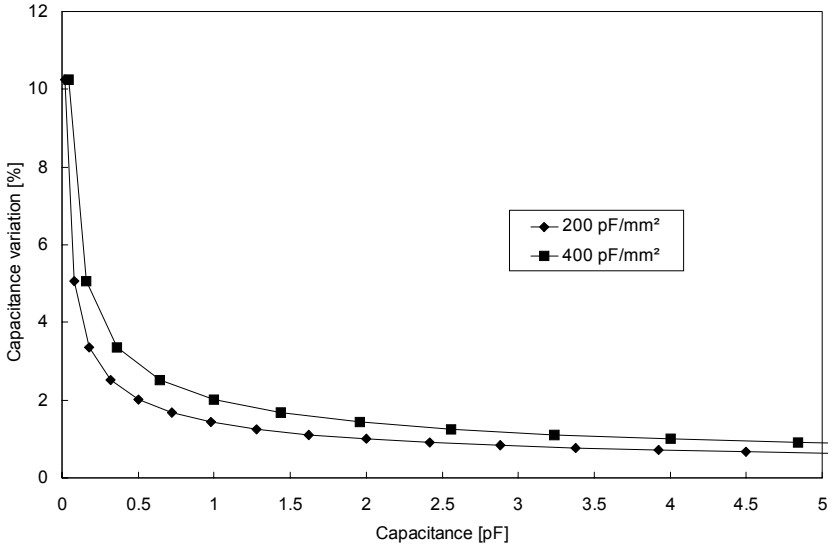

Figure 2.19: Capacitance variation as a function of the required MIM capacitance value for various capacitance values per area. For this calculation a square capacitor layout and a mask accuracy of ± 0.5 µm is assumed.

The use of the MIM capacitors is limited by the breakdown behaviour of the dielectric layer. The maximum voltage, that means the sum of both DC and RF voltage, which can be applied to a capacitor is determined through the thickness of the dielectric layer times the electric breakdown field of the dielectric layer. Due to this limitation capacitors in series have sometimes been used in the output-matching network, see chapter 6 for more details.

The major processing related factors that influence the capacitance value per area are the height of the dielectric layer and the dielectric constant of this layer. A maximum variation between ± 10 – 15% is quoted for the capacitance per area. The value of a MIM capacitor is also influenced by the accuracy of the mask, which is used for the definition of the top plate of the capacitor. In figure 2.19, the influence of a variation of ± 0.5 µm in the dimensions of the top plate of the capacitor is shown as a function of the required capacitor value. The results show that the accuracy decreases rapidly for capacitor values smaller than 0.4 pF. Therefore, only MIM capacitor values larger than 0.4 pF have been used in the amplifier designs discussed.

2.4.5 Resistor

Resistors are used in the discussed power-amplifier designs in the stability improving networks and the slope compensation networks. The resistor is also used for control of the bias currents to improve the reliability of the transistors and to de-couple the influence of the bias circuit from the RF matching networks.

They can be implemented as implanted GaAs resistors or as deposited NiCr resistors. A cross section of both types of resistors is shown in figure 2.20.

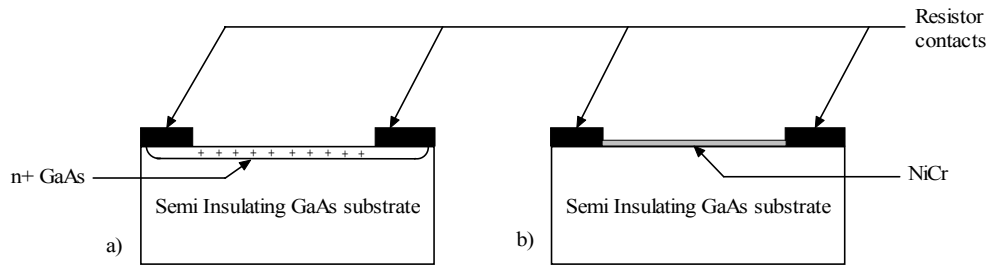

Figure 2.20: Cross-section of a) an implanted GaAs and b) a NiCr resistor.

The usage of the NiCr resistors is limited by the maximum current that is allowed to flow through the resistor before electron-migration in the resistor metal begins to occur. The maximum current, which can flow through a given NiCr resistor width, is in the order of 0.4 mA/µm. The usage of the implanted resistors is limited by the electrical field strength where

the resistor becomes non-linear. This non-linear behaviour is caused by the saturation of the velocity of the electrons for a given electrical field strength. Consequently, the current will not further increase when the applied voltage is increased and the resistor stops acting as a linear resistor.

For the NiCr resistors an accuracy between ± 10 – 15% is quoted and for the GaAs resistors between ± 10 – 40%. The accuracy of the GaAs resistors is considerably lower than for NiCr resistors. Therefore, GaAs resistors have only been used when their absolute value is not critical, e.g. the 1 kΩ stabilisation resistors discussed in section 5.7.2. In the matching networks, only NiCr resistors have been used.

2.4.6 Viahole

Viaholes are used to make electrical ground contacts for the electrical components used in the MMIC. This is of vital importance for the active devices used in a high-power amplifier because reduced inductance to ground will result in improved output power and gain. The viaholes used in conjunction with the active devices also act as thermal short circuits to the ground plane and as such reduce the temperature of the active devices. A viahole is etched through the substrate to the ground plane with its sidewalls covered with gold, see figure 2.21.

The use of viaholes is limited by the maximum current that is allowed to flow before electron migration starts to occur. For the used viahole, a value of several amperes is allowable and there is therefore no problem applying the viaholes in a high-power amplifier.

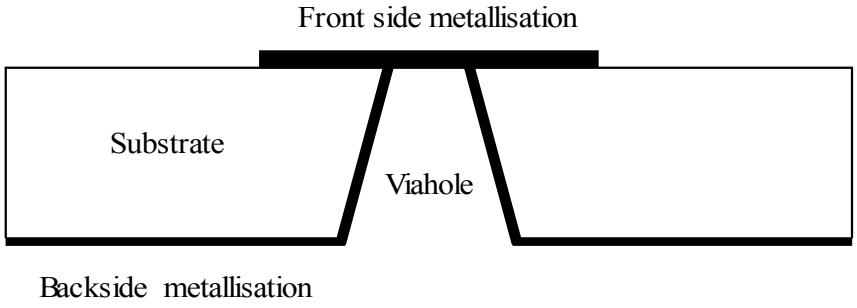

Figure 2.21: Cross section of a viahole.

The viahole can be modelled with the help of series inductors and a parallel inductor to ground, see section 4.3.7. The value of these inductors is mainly influenced by variation of the thickness of the GaAs substrate. Therefore, the parallel inductor to ground has a maximum variation of ± 10% and the series inductors of ± 7%.

2.5 Conclusions

This chapter gives an overview of the technologies that were available for the high-power amplifier designs discussed in this thesis. For each component its limitations from an electrical point of view are given. In addition, an indication of the component value variation as a function of process variations is given.

The active devices that are used are the MESFETs available in the DIOM20HP process of Infineon and the HFETs available in the high-power process of FhG-IAF. Their working principle is discussed and the limiting factors for high-power operation, namely maximum drain current, breakdown voltage and knee voltage, were identified. From these DC values, an output power of 0.68 W/mm was found for the MESFET technology and an output power of 0.89 W/mm was found for the HFET technology. Other figures of merit that were discussed are the cut-off frequency, the maximum frequency of oscillation and the frequency dependency of the power gain. Results show that the HFET technology has a significantly higher cut-off frequency. The HFETs have a cut-off frequency, at a bias setting applicable for power amplifiers, of 17 GHz. The MESFET technology has a cut-off frequency of around 12 GHz. Therefore, the HFET technology will have a higher power gain at X-band. This high power gain is essential for getting an as high as possible power added efficiency. In addition, the degree of freedom a designer has with respect to the transistor layout is discussed. It is shown that high-power amplifiers realised with transistors that have a fishbone layout will occupy less chip area and will have higher gain than the ones realised with an interdigitated layout. Additional factors that influence the layout of the transistors will be discussed in chapter 5.

For the interconnection between the various components, microstrip lines are used. The maximum current that is allowed to flow through a given line width limits the use of a microstrip line. This is also the reason that no use can be made of square or spiral integrated inductors. Microstrip lines are used whenever inductors are needed. Capacitors are realised as Metal Insulator Metal capacitors. The breakdown voltage of these capacitors limits the use of these capacitors. Resistors can be realised as implanted or NiCr resistors; here again the use is limited by the amount of current that is allowed to flow through a given width. The ground connection is made with the help of viaholes. The viaholes are limited in use by the amount of current that is allowed to flow through them. This current limit is not reached for the amplifiers discussed in this thesis due to the large amount of viaholes, which is used in each amplifier design. For each of the passive components values for the worst case component spread are given.

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3. High-power characterisation systems

3.1 Introduction

The availability of accurate component models and model parameters is of vital importance for the successful development of high-power amplifiers. In this chapter, the measurement systems that are developed for the high-power amplifier design and characterisation are discussed. The component models and their parameter extraction methods will be discussed in detail in chapter 4.

All measurement systems that are developed for the design and analysis of high-power amplifiers and components are integrated into one larger fully computer controlled measurement system. This system is developed for the fully automatic characterisation of MMICs, see figure 3.1. The power, load-pull and three-port S-parameter measurement systems were especially developed for the work described in this thesis.

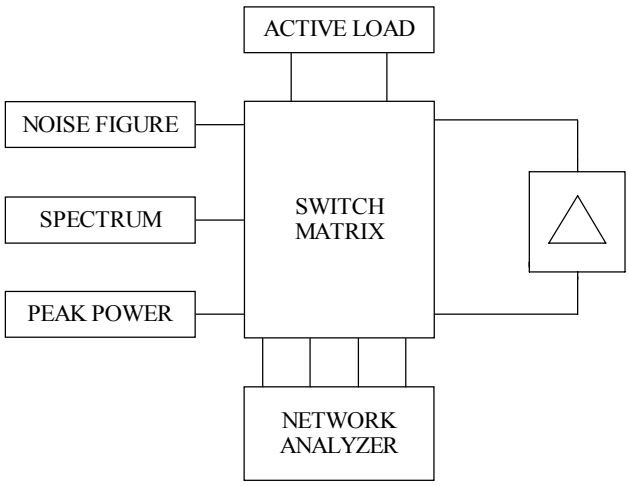

Figure 3.1: Block diagram of integrated TR module and MMIC measurement system.

With the measurement system depicted in figure 3.1, the measurement of a number of different parameters like power, noise figure, third order intermodulation intercept point etc, is possible. In this chapter, only those parts relevant for the characterisation of the components for high-power amplifier design and complete high-power amplifiers are discussed. An overview of all relevant measurement methods and their purpose is summarised in table 3.1. The transition between the various measurement set-ups is controlled with the depicted switch matrix.

Table 3.1: Overview of used measurement methods.

	DC	2-port S-parameter	3-port S-parameter	Power	Load-pull
Passive components		X	X		
Transistors	X	X			X
HPAs	X	X		X	

The DC measurements for the transistor modelling are performed with the help of the HP4142B DC supply. The high-power amplifiers are measured with the help of general purpose DC power supplies. The DC measurement system will not be discussed in any further detail. All measurements discussed in this chapter can be performed under CW and pulsed conditions.

This chapter starts with the discussion of the on-wafer small-signal two-port measurement set-up and the used calibration methods. This measurement system is used for both the characterisation of passive two-port devices and the transistors. In the same section, also the three-port measurement system used for the characterisation of the microstrip T and Y-junctions is discussed. The calibration method that is developed for calibration of measurement ports that are placed under 90° is also discussed in this section. In section 3.3 the high-power measurement system is discussed. The high-power measurement set-up is used for the evaluation of the realised high-power amplifiers. An extension of this measurement set-up is the load-pull measurement system described in section 3.3.3, which is used for the determination of the optimum load impedance and verification of the transistor model.

3.2 Small-signal measurement systems

In this section the small-signal measurements systems used for the characterisation of the components discussed in chapter 2 is described. In section 3.2.1, the two-port measurement system along with the calibration methods and standards used are discussed. The same is done in section 3.2.2 for the three-port measurement system.

3.2.1 Two-port S-parameter measurement system

Microwave circuits are commonly described with the help of S-parameters because these parameters can easily be measured with the help of a network analyser like the HP8510C from Hewlett Packard. The HP8510C network analyser combined with the HP85110A pulsed test-set form the basis of the discussed measurement system.

A two-port is described as follows with the help of S-parameters [3.1]:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{3.1}$$

These parameters are easily determined from the measured ratios of the power waves. This in contrast to for instance Z or Y-parameters, which require the availability of good open and short terminations. These standards are difficult to realise at microwave frequencies, particularly for on-wafer measurements. The S-parameters on the other hand only require the termination of the device under test with the characteristic impedance of the measurement system. For the work described in this thesis, unless otherwise specified, a characteristic impedance of 50 Ω is assumed. This characteristic impedance of 50 Ω has the additional advantage that the active devices are stable at microwave frequencies when terminated with this impedance. This is not always the case when an open or short is presented to the transistor, see section 5.6.

Another essential part of microwave S-parameter measurements is the calibration of the measurement system and the determination of the measurement reference planes. All S-parameter measurements described in this thesis have been calibrated with the help of a Line Reflect Line (LRL) calibration method [3.2]. This method was first described by Engen and Hoer [3.3]. Following their publication a great many so-called self-calibration methods were described in the literature [3.4-3.7]. The multiple line calibration of Marks [3.7] is considered the most accurate on-wafer calibration known today. In the past both on-wafer and coaxial S-parameter measurement systems were calibrated with the help of the so-called Short Open Load Thru (SOLT) method.

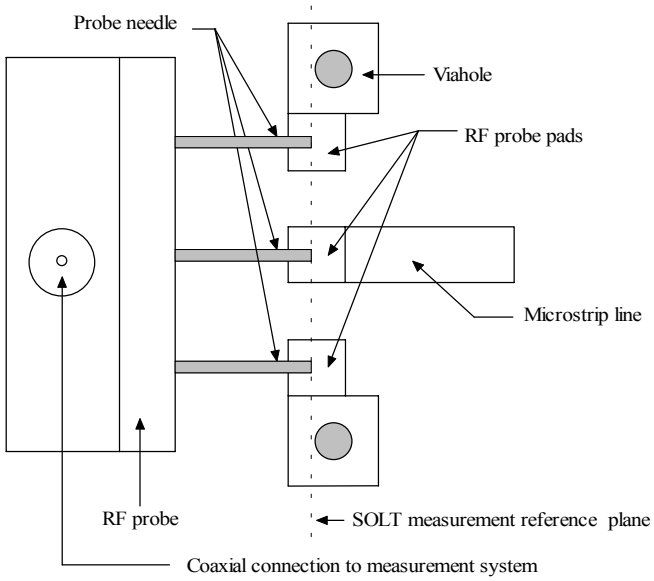

Figure 3.2: Topview of the transition between the measurement system and the device under test.

The LRL calibration method has the following advantages over the classical SOLT calibration method:

- Fewer calibration standards are needed and only a limited amount of information regarding their electrical parameters is needed, e.g. the characteristic impedance of the Line standard.
- It is possible to remove the influence of the coplanar to microstrip transition that exists between the measurement system and the device under test. A picture of such a transition is shown in figure 3.2. The effect of this transition in combination with the calibration method used can be seen in figure 3.3. In this figure, the measurement results of a 1200 µm long 50 Ω microstrip line are compared with Libra [3.8] simulations. The depicted results show that the LRL calibration has a superior performance over the results obtained with the SOLT calibration. Note that for this example the probes have been placed as close as possible to the beginning of the line for the measurement with the SOLT calibration. This has been done to avoid any unnecessary additional phase shift due to the line length of the RF probe pads.

The difference between the measurement results obtained with the SOLT calibration and the ones obtained with the LRL calibration are considerable. As stated before the error in the SOLT calibration is caused by the coplanar to microstrip transition, which is not correctly removed from the measurement results. A numerical example will be given now to get a feeling with respect to the influence of the errors caused by an improper calibration algorithm. For this example, the microstrip line will be considered equivalent to a series inductor. In that case, the inductance value can directly be determined from the measurement of the phase of the S_{21} of the microstrip line with the help of the following equation:

$$S_{21} = \frac{100}{100 + j \cdot \omega \cdot L}. \tag{3.2}$$

The inductance of the microstrip line can be calculated from the phase of the measured S_{21} as follows:

$$L = \frac{-100}{\omega} \cdot \tan\left(\varphi\left(S_{21}\right)\right). \tag{3.3}$$

Suppose this series inductance was used in a low-pass L-matching impedance transformer network, like the one that is described in section 6.2.3.2. Then the centre frequency will shift to a higher value when a SOLT calibration is used to determine the equivalent series inductance of the microstrip line. The reduction of the inductance value that is obtained with the LRL calibration (L_{LRL}) compared to the one found with the SOLT calibration (L_{SOLT}) can be expressed as follows:

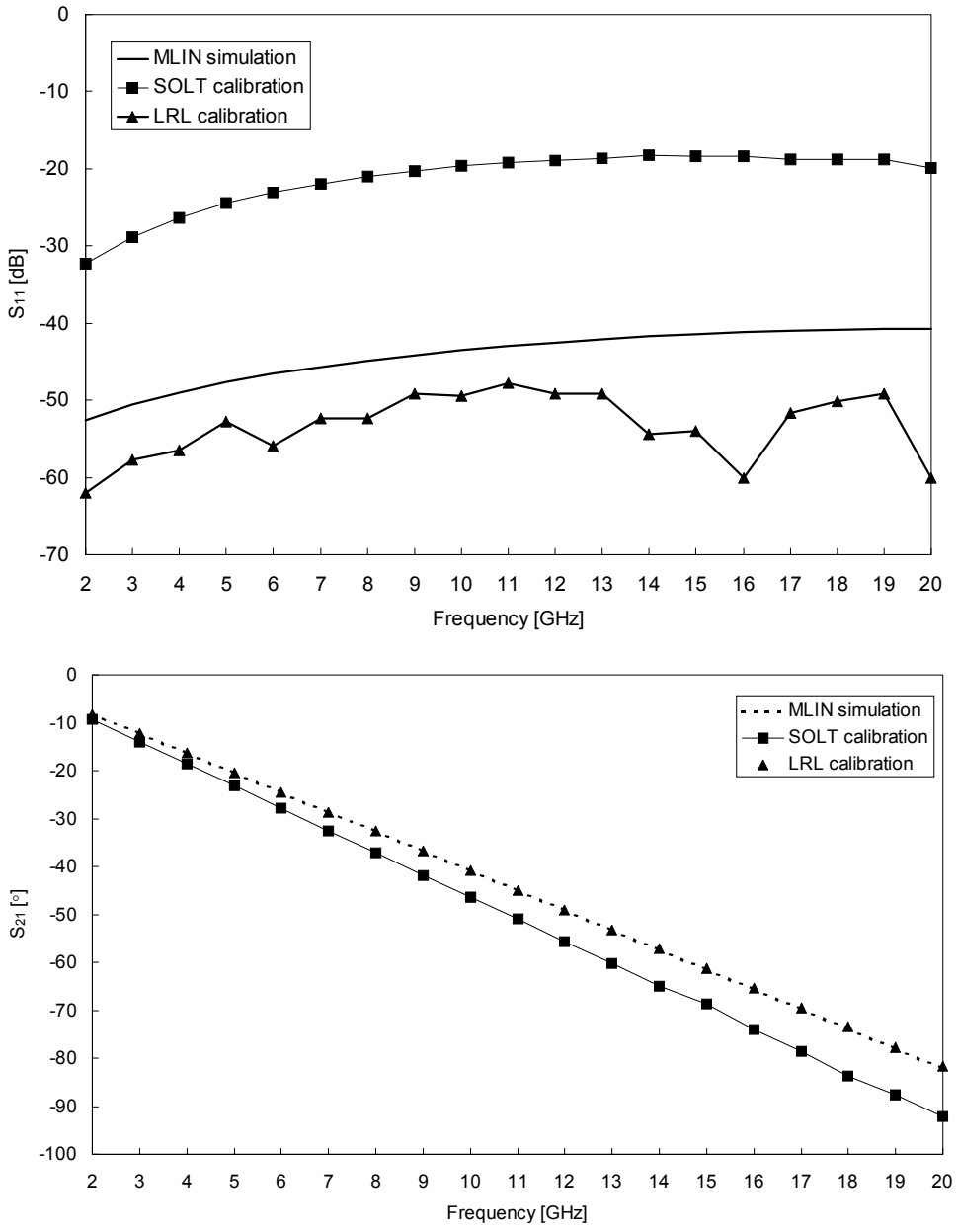

Figure 3.3: Comparison of the simulated S-parameters of a transmission line and the S-parameters measured with a SOLT calibration and with a LRL calibration. MLIN indicates the microstrip line model of Libra [3.8]. The length of the microstrip line is 1200 µm and the width is 70 µm.

$$L_{LRL} = \frac{\tan\left(\varphi\left(S_{21}\right)_{LRL}\right)}{\tan\left(\varphi\left(S_{21}\right)_{SOLT}\right)} \cdot L_{SOLT} \,. \tag{3.4}$$

When the measurement results at 10 GHz are used ($\varphi(S_{21})_{SOLT}$ = -46.4° and $\varphi(S_{21})_{LRL}$ = -40.8°), of the microstrip line depicted in figure 3.3, and a transformation ratio of 4 is assumed, an increase of 14%, see section 6.2.3.2, in the centre frequency of the matching network is found when a SOLT calibration is used. This increase of 14% is totally unacceptable taking into account the relative bandwidth of 30% that is required for the amplifiers discussed in this thesis. Therefore, it can be concluded that the use of the LRL calibration method is essential for obtaining accurate component models. All test structures that have been used for model extraction have been laid out with the help of 50 Ω transmission lines at the input and output of the structure. The influence of these lines can easily be removed from the measurement results by just subtracting the phase of these lines from the measured phase of the S-parameters.

3.2.2 Three-port S-parameter measurement system

A three port S-parameter measurement system is developed for the characterisation of the T-junction and Y-junctions discussed in chapter 4. With this measurement system, it is possible to determine automatically all possible sets of two-port S-parameters between the three ports. The reflection coefficient of the imperfect load connected to the non-measured port is also measured. The three-port S-parameters are extracted from the before mentioned three two-port S-parameter measurements and the knowledge of the impedance of the port that is terminated. The corrected three-port S-parameters are calculated with the help of the algorithm described by Rautio [3.9]. Rautio makes use of so-called Gamma-R parameters, which are similar to S-parameters normalised to an arbitrary impedance. Gamma-R parameters have the advantage that they do not degenerate for short or open circuits. Therefore, the closed-form solution for the determination of three-port S-parameters described by Rautio maintains valid at and near high reflection terminations. The three-port S-parameters are determined from the measured two-port S-parameters and the reflection coefficient of the non-measured port with the following steps:

1. Convert each of the measured two-port S-parameters to Gamma-R parameters with the following equation:

$$R = \left(\Gamma^{*} + S\right) \cdot \left(1 - \Gamma \cdot S\right)^{-1} . \tag{3.5}$$

   In this equation Γ is a diagonal matrix containing the reflection coefficient connected to the specific port when it is not measured.
2. Fill the 3 x 3 Gamma-R matrix with the two-port Gamma-R matrices.
3. Convert the 3 x 3 Gamma-R matrix back to S-parameters, which have the reference impedance required, with the help of the following equation:

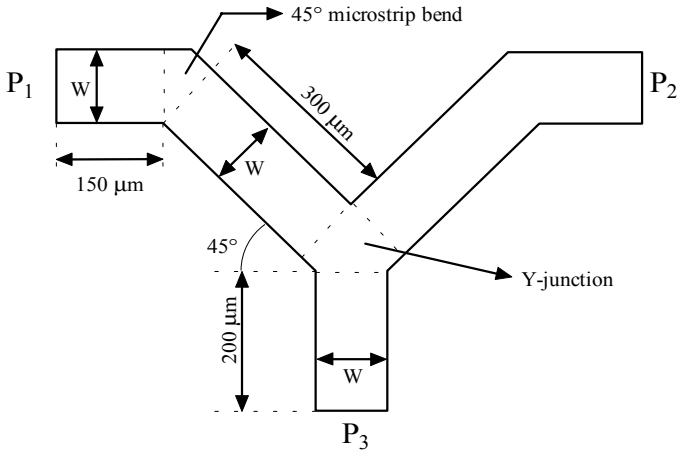

Figure 3.4: Layout Y-junction test structure. The width (W) of both the interconnect lines, bends and the Y-junction is 100 µm. The microstrip line lengths are indicated until the Y-junction reference planes.

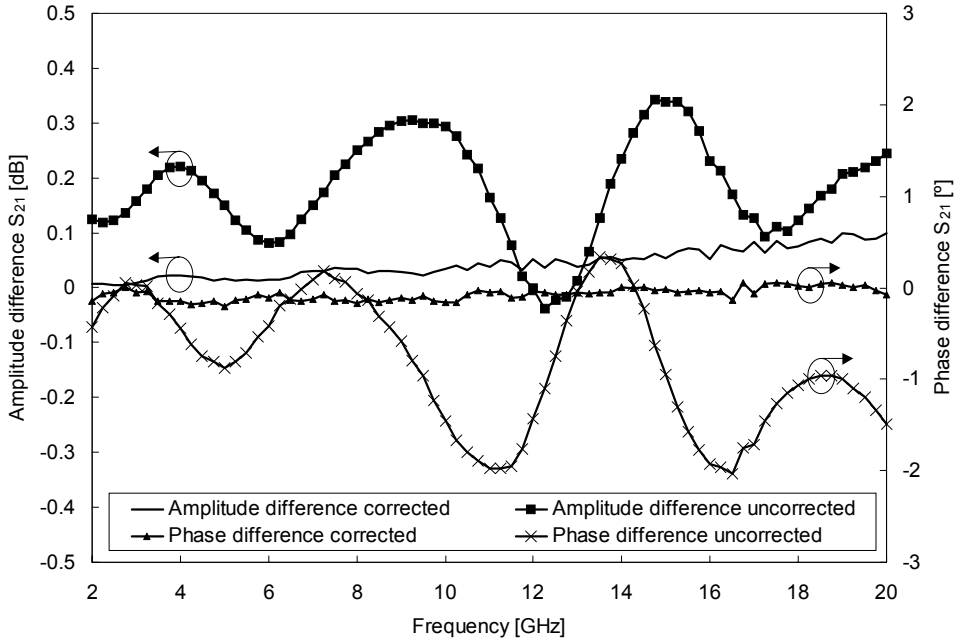

Figure 3.5: Comparison between the measured and simulated results of the Y-junction test structure depicted in figure 3.4. The Y-junction has a width of 100 µm. The corrected results show the situation where the non-ideal character of the terminating impedance is compensated for.

$$S = \left(1 + R \cdot \Gamma\right)^{-1} \cdot \left(R - \Gamma^{*}\right). \tag{3.6}$$

Besides this closed-form solution, also an iterative solution is given by Rautio, which gives a simpler solution when devices with more than 3-ports must be measured. Application of described algorithm will result in more accurate measurement results when compared to the results obtained when an ideal 50 Ω impedance is assumed at the terminated port. This can be clearly seen from the measurement results of the Y-junction test structure depicted in figure 3.5. The layout of the test structure, with port numbering and microstrip line lengths to the reference planes of the Y-junction, is indicated in figure 3.4.

The measurement results from figure 3.5 also show that there is a good agreement between the measurement results and the simulated results obtained with the models for the microstrip lines, the 45° microstrip bend and the Y-junction. These models are discussed in section 4.3.

Another issue that needs careful consideration is the calibration of the two-port measurements that are used for the determination of the three-port S-parameters, especially the calibration of the S-parameters between the measurement ports that are physically not in line. For such ports, it is difficult to design transmission lines that are exactly 50 Ω over a large frequency band. Note that for the three-port measurements it is also necessary to remove the influence of the coplanar to microstrip transition from the measurement results with the help of a LRL calibration. A calibration method has been developed to circumvent these problems using a switch matrix to facilitate calibrating between various combinations of the on-wafer probes as shown in figure 3.6. The same switch matrix is also used for the two-port S-parameter measurements necessary for the three-port S-parameter determination.

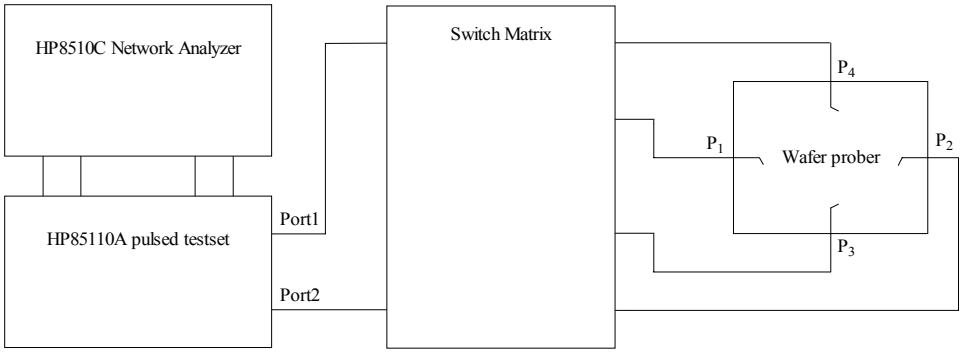

Figure 3.6: Switch matrix and on-wafer measurement system.

First, two in line on-wafer LRL calibrations are performed. The first calibration is performed between probe P_1 and probe P_2. The second calibration is performed between probe P_3 and probe P_4. These are two normal in line LRL calibrations that can be performed with the algorithm available in the network analyzer [3.10]. Suppose a calibration is needed

between probe P_1 and probe P_3 then results of these two calibrations are used as follows. The forward one-port error terms (E_{DF}, E_{RF} and E_{SF}, see [3.10]) are read out of the network analyzer from the LRL calibration between probe P_1 and probe P_2 and used as forward error terms for the new calibration. The reverse one-port error terms (E_{DR}, E_{RR} and E_{SR}) are read out of the network analyzer from the LRL calibration between probe P_3 and probe P_4 and used as reverse error terms for the new calibration. The terms that remain to be determined are the forward and reverse load match and tracking terms (E_{LF}, E_{RF}, E_{TF} and E_{TR}). For the determination of these remaining error terms, the flow graph depicted in figure 3.7 is used. In this flow graph, the terminology for the error terms as given by Marks [3.11] is used.

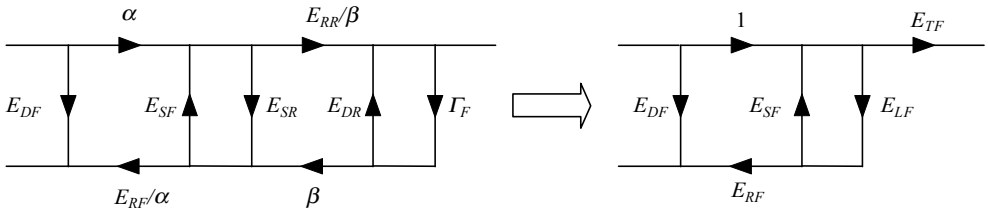

Figure 3.7: Flow graph used for determination error terms in the forward direction.

With the help of this error flow graph, the following equations can be derived for the forward load match and tracking error terms:

$$E_{LF} = E_{SR} + \frac{E_{RR} \cdot \Gamma_F}{1 - E_{DR} \cdot \Gamma_F}, \tag{3.7}$$

$$E_{TF} = \frac{\alpha}{\beta} \cdot \frac{E_{LF} - E_{SR}}{\Gamma_F}. \tag{3.8}$$

The reverse load match and tracking error terms are determined in a similar manner as shown in figure 3.7. The resulting equations for these error terms are:

$$E_{LR} = E_{SF} + \frac{E_{RF} \cdot \Gamma_R}{1 - E_{DF} \cdot \Gamma_R}, \tag{3.9}$$

$$E_{TR} = \frac{\beta}{\alpha} \cdot \frac{E_{LR} - E_{SF}}{\Gamma_R}. \tag{3.10}$$

Unknown are the reflection coefficients of the electronic switch in the test-set in the forward (Γ_F) and reverse (Γ_R) direction and the term α/β. All three terms can be determined when a reciprocal two-port device is connected between probe P_1 and probe P_3. The reflection coefficients of the test-set switch are determined with the help of the measured power waves

(a_1 and a_2) and the uncorrected S-parameter measurements (S_{12M} and S_{21M}), see equation (3.11) and (3.12):

$$\Gamma_R = \frac{\left(\frac{a_1}{a_2}\right)}{S_{12M}} = \frac{a_1}{b_1}, \tag{3.11}$$

$$\Gamma_F = \frac{\left(\frac{a_2}{a_1}\right)}{S_{21M}} = \frac{a_2}{b_2}. \tag{3.12}$$

After these terms have been measured only α/β needs to be determined. This is accomplished through the measurement of a reciprocal two-port device and the method described by Ferrero [3.12]. The effect of the reflection coefficients of the test-set switch, on the measured S-parameters, is removed with the help of the equations given by Marks [3.11]. The measured transmission parameters T_M can in the following manner be expressed as a function of the error terms [3.11]:

$$T_M = \frac{\beta}{\alpha} \cdot \frac{1}{E_{RR}} \cdot \begin{bmatrix} E_{RF} - E_{DF} \cdot E_{SF} & E_{DF} \\ -E_{SF} & 1 \end{bmatrix} \cdot \begin{bmatrix} T_{D11} & T_{D12} \\ T_{D21} & T_{D22} \end{bmatrix} \cdot \begin{bmatrix} E_{RR} - E_{DR} \cdot E_{SR} & E_{SR} \\ -E_{DR} & 1 \end{bmatrix}. \tag{3.13}$$

The transmission parameters have been defined as:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}. \tag{3.14}$$

Equation (3.13) can also be written in a manner similar to that as has be done by Ferrero [3.12]:

$$T_M = \gamma \cdot Y_A \cdot T_{DUT} \cdot Y_B. \tag{3.15}$$

Ferrero [3.12] realised that the determinant of the transmission parameters of a reciprocal two-port device is equal to one. This observation is used to determine γ, see equation (3.16):

$$\det(T_M) = \gamma^2 \cdot \det(Y_A) \cdot \det(Y_B) \Rightarrow \gamma = \pm\sqrt{\frac{\det(T_M)}{\det(Y_A) \cdot \det(Y_B)}}. \tag{3.16}$$

The only thing that is left to solve is the choice of the sign of γ. This is accomplished with the help of the following equations, which are taken from [3.12]:

$$T_{DUT} = \frac{1}{\gamma} \cdot Y_A^{-1} \cdot T_M \cdot Y_B^{-1} = \frac{X}{\gamma}. \tag{3.17}$$

Conversion of the transmission parameters to S-parameters yields:

$$S_{21\,DUT} = \frac{\gamma}{X_{22}}. \tag{3.18}$$

When a microstrip two-port structure is used, the phase of the S_{21} can easily be determined with the help of electromagnetic field simulations. After γ is known the ratio α/β can be calculated. With the help of this ratio, the remaining error terms are calculated. Finally, the resulting error terms are fed back in the network analyzer. The described calibration method has the following advantages:

- The impedance of the thru device does not need to be known. The only condition that must be fulfilled is that the device must be reciprocal.
- The coplanar to microstrip transition can be removed from the measurement results, even when the wafer probes are placed under an angle of 90°.

In summary, it can be concluded that with the on-wafer measurement and calibration method described here the three-port microstrip discontinuities discussed in section 4.3 can be accurately characterised.

3.3 Large-signal measurement system

3.3.1 Introduction

For the verification of the large-signal performance of the transistor models discussed in section 4.2, large-signal measurements are required. For this purpose a load-pull measurement system has been developed. Other interesting large-signal measurement systems are the waveform measurement systems that have for example been described by Demmler [3.13] and Van Raay [3.14]. The reason for the choice for a load-pull measurement system is the fact that besides the model verification additional information regarding the location of the optimum load impedance, the operating class etc. can be obtained. This is described in more detail in chapter 5. A large-signal measurement system is, aside from the model verification, also needed for the characterisation of the realised high-power amplifiers.

The large-signal measurement systems for a fixed load impedance and the calibration algorithms used are discussed in section 3.3.2. In section 3.3.3 this measurement system is extended with an active load and a novel measurement algorithm. This combination makes

it possible to perform load-pull measurements and automatically search for the optimum load impedances.

3.3.2 Power measurement system

The large-signal measurement system that was developed in the framework of this thesis is built around the HP85110A pulsed network analyzer system [3.15]. The choice for this system is based on the following. First, it is possible to perform measurements under both CW and pulsed conditions, which is a requirement for the high-power amplifiers under development. Secondly the test-set can handle up to 20 Watts of RF power when the proper connections and attenuator settings are made [3.15]. A block diagram of the measurement system is shown in figure 3.8.

The input power required is generated with the help of a Travelling Wave Tube Amplifier (TWTA). With the help of this amplifier, a power of 3 Watts can be supplied at the probe tip of the on-wafer measurement system. The device under test (DUT) is terminated at the output of the test-set with the load impedance Z_L. For the characterisation of the power amplifiers, this load impedance is 50 Ω. For the load-pull measurements, this fixed termination is replaced with an active load as it is discussed in section 3.3.3.

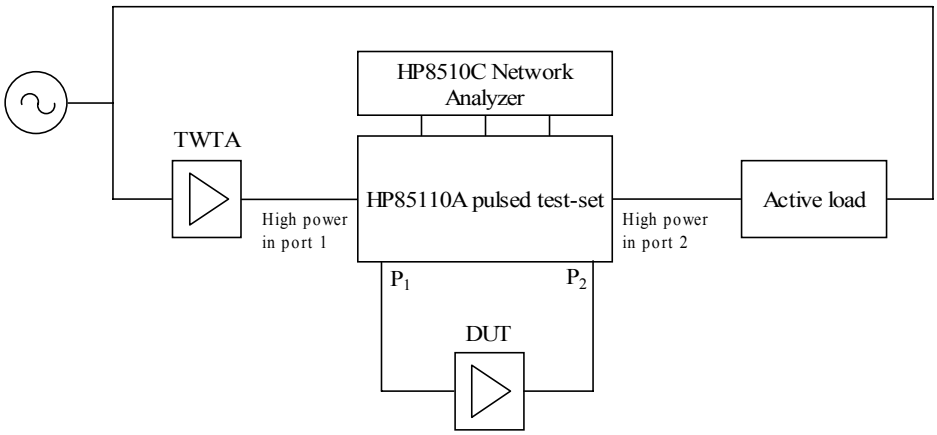

Figure 3.8: Large-signal measurement system.

The characterised transistors have a very low input impedance due to the high value of the gate-source capacitor C_{gs}. To obtain the desired measurement accuracy it is necessary to correct for the mismatch losses that exist between the measurement system and the transistor. To satisfy this condition a fully vector error corrected measurement system is needed. An example of the effect on the measurement result when no vector error correction is applied is shown in figure 3.5. Vector error correction is possible with the measurement system described here because the incident and reflected power waves can be measured separately. It is also possible to measure the absolute value of the power that is present at

the input and the output of the device under test. Finally, the presented measurement system has the ability to measure in real time the load impedance presented at the output of the DUT. This makes it possible to perform load-pull measurements with the described measurement set-up. A more in depth discussion regarding load-pull measurements is presented in the next section.

The development of the necessary calibration and measurement algorithms was started from the ones described by Hecht [3.16]. These equations have been developed for a measurement system where:

- A zero length thru can be applied between the input and the output of the measurement system.
- Absolute power measurement can be performed at the input and output measurement reference planes.

This is not possible with the discussed on-wafer measurement system. To circumvent these problems the possibility to characterise the on-wafer thru standard automatically has been added. Also the S-parameters of the input on-wafer probe were determined and used for the correction of the input power calibration terms. A description of the measurement system and calibration algorithms, which were developed, can be found in literature [3.17]. Later when the measurement system was extended to be able to characterise a complete MMIC, the algorithms discussed in [3.17] were replaced with the ones given by Ferrero [3.18]. The latter algorithms facilitate the use of fewer calibration steps than the ones described in [3.17]. The measurement results are nevertheless the same. The accuracy of on-wafer load-pull measurements was also addressed by Ferrero [3.19]. He showed that it is essential for the measurement accuracy not to use a TWTA during calibration. The noise of a TWTA leads to an unacceptable increase in measurement inaccuracy. Ferrero determined for the load reflection coefficients used for the transistors discussed in this thesis ($|\Gamma_L| < 0.8$) that the accuracy for the output power and power added efficiency is better than 5% when no TWTA is used during the calibration. For the gain measurements, an accuracy of better than 20% was determined.

3.3.3 Load-pull measurement system

Based on the measurement system and calibration method discussed in section 3.3.2 a load-pull measurement system has been developed. This load-pull measurement system is meant to verify the large-signal performance of the transistor models and to obtain experimental information regarding the location of the optimum load impedance of the transistors used in the high-power amplifier designs. This information can be obtained as a function of the selected bias settings, and as a function of a parameter selected, e.g. output power or power added efficiency. An active load is used instead of a passive load because with the former it is possible to correct for the losses between the load and the on-wafer measurement reference plane. This is essential because it must be possible to present large load reflection coefficients (> 0.8) to the output of the DUT. To achieve such high reflection coefficients with a passive load the loss between the load and the measurement reference plane should be less than 0.5 dB, which is difficult to achieve at X-band. Another reason that an active

load was used, is the fact that it can be integrated with the complete measurement system discussed in section 3.1, which would not have been the case if a passive load had been used.

The measurement routines used are the same as the ones described in the previous section. The fixed load described with that measurement set-up is replaced with the active one described in section 3.3.3.1. In section 3.3.3.2 the fast search load-pull algorithm developed in the scope of this thesis is discussed. This algorithm will reduce the necessary measurement time significantly.

3.3.3.1 Active load

The active load that was developed is based on the principle first described by Takayama [3.20], see figure 3.9. The Takayama principle was chosen because it uses simpler hardware due to the absence of possible feedback loop oscillations, as it is the case for the feedback principle [3.21]. The disadvantage of the Takayama principle over the feedback solution is the necessity that for each input power variation the load has to be set again in an iterative, time consuming, manner. To circumvent the long measurement time necessary to find the optimum load impedance with an active load based on the Takayama principle the predictive load-pull algorithm described in section 3.3.3.2 has been developed [3.24].

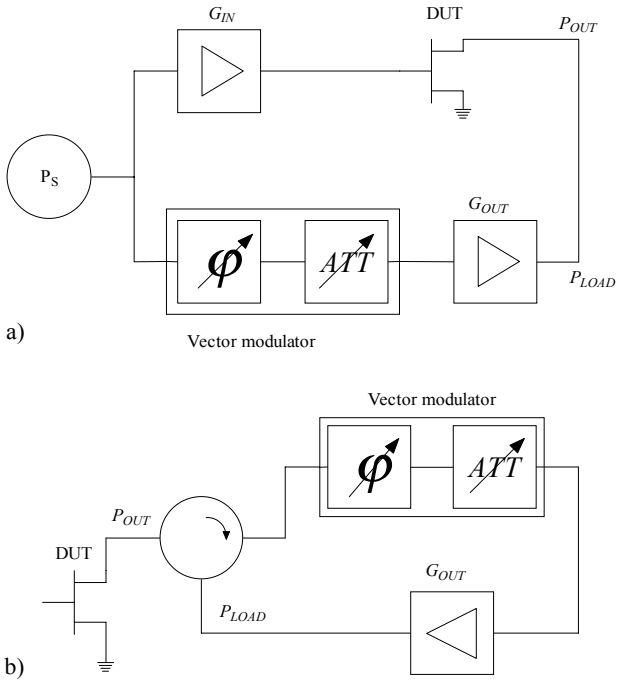

Figure 3.9: Active load principles: a) Takayama principle [3.20], b) feedback principle [3.21].

The load-pull system, based on the Takayama principle, consists of two power amplifiers that are used to generate the power levels required at the input and output of the device under test. The vector modulator [3.22] is used to control the amplitude and the phase of the signal that is fed back into the device under test. This control of amplitude and phase makes it possible to control the load reflection coefficient Γ_L seen at the output of the device under test, see the simplified equation (3.19). In this equation, it is assumed that all components are perfectly matched. When the mismatches are taken into account a similar equation is found [3.23], the equation given here is intended to demonstrate the principle of the active load used in the load-pull measurement system:

$$\Gamma_L = \frac{P_{LOAD}}{P_{OUT}} = \frac{G_{OUT}.ATT_{VM}.e^{j\cdot(\varphi_{vm}+\varphi_{OUT})}}{G_{IN}\cdot G_{DUT}.e^{j\cdot(\varphi_{DUT}+\varphi_{IN})}}. \tag{3.19}$$

The equation given in (3.19) can be further simplified to the one given in (3.20):

$$\Gamma_L = G_{SYS}.e^{j\cdot\varphi_{SYS}}\cdot ATT_{VM}.e^{j\cdot\varphi_{VM}}. \tag{3.20}$$

It can be concluded from equation (3.20) that:

- The amplitude and phase of the load reflection coefficient Γ_L can be controlled with the help of the amplitude setting ATT_{VM} and the phase setting φ_{VM} of the vector modulator.
- The setting of the load reflection coefficient Γ_L must be done in an iterative manner because the phase and gain of the system, G_{SYS} and φ_{SYS}, are power and load reflection coefficient dependent. This is caused by the dependency of the DUT for these parameters.
- Maximum resolution should be obtained for the vector modulator to be able to accurately set the load impedance. It is, therefore, important to dimension the gain of the power amplifiers (G_{IN} and G_{OUT}) carefully. To get better control of the system gain G_{SYS} an extra controllable attenuator has been introduced after the depicted vector modulator, which was lacking in the load-pull measurement system described by Hendriks[3.23].

The load-pull measurement system is fully vector error corrected with the help of the calibration methods described by Ferrero and Pisani [3.18]. The measurement system is configured in such a way that both on-wafer and off-wafer measurements are possible with the same measurement set-up.

3.3.3.2 Fast load-pull search algorithm

In this section, the novel fast search algorithm for finding the optimum load impedance developed in the scope of this thesis will be discussed. Such algorithm is necessary because measuring over an (at first instance) unknown number of different load impedances, at different source powers, to find the optimum load impedance of an active device, for e.g. maximum output power, will result in an unacceptable long measurement time.

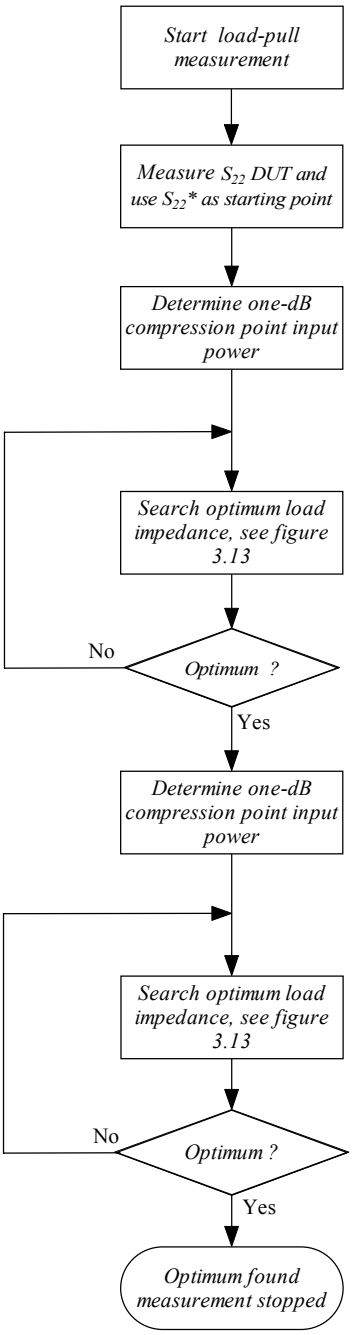

Figure 3.10: Novel active load-pull algorithm for optimum load impedance determination [3.24].

A typical transistor measured in this way has an average measurement time of four hours when measured at one frequency and one bias point. This is much too long taking into account that hundreds of different active devices, at different bias points and frequencies have been characterised for the work described in this thesis.

To reduce the measurement time to less than half an hour for one active device the algorithm depicted in figure 3.10 was developed. The first step is the determination of a start load reflection coefficient at the given frequency and bias point. This start reflection coefficient is found by using the conjugated of the measured output reflection coefficient (S_{22}^*) of the active device. It is well known that this, under small-signal conditions, will give the maximum gain and hence the maximum output power for a given input power. In addition, for other parameters like for instance the power added efficiency this also gives a good start value. The advantage of the selection of this starting point in relation to the number of iterations needed to find the optimum load impedance is shown in table 3.3. The results show that less iterations are needed when the before mentioned starting point is used.

As a next step, the input power at one-dB gain compression point is determined at the selected start load reflection coefficient. This is necessary because the optimum load impedance changes as a function of the input power from a small-signal power to approximately the input power that will give the one-dB compression gain. This can be seen in figure 3.11 and figure 3.12.

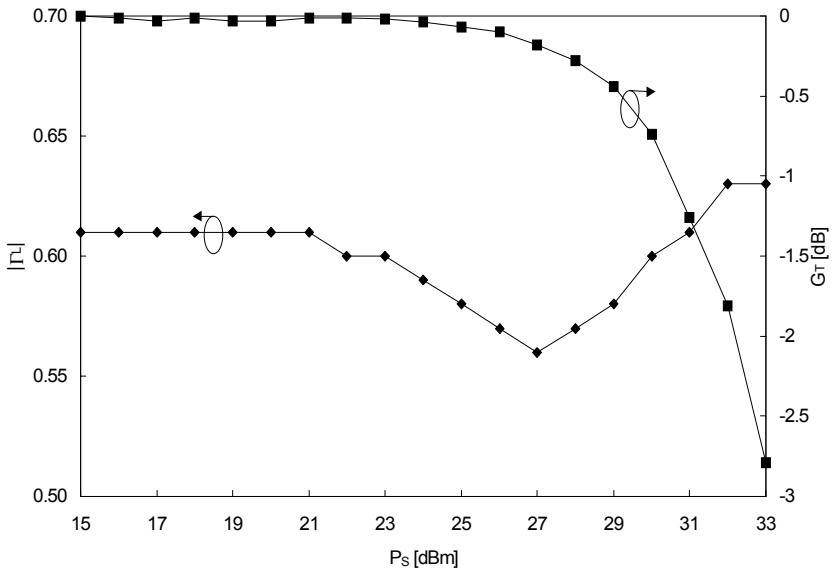

Figure 3.11: Magnitude optimum load reflection coefficient and transducer gain as a function of the applied source power. The optimum is determined for maximum output power at f = 8 GHz, V_{DS} = 9 V and V_{GS} = -0.75 V. The measured MESFET has a total gate width of 2.8 mm.

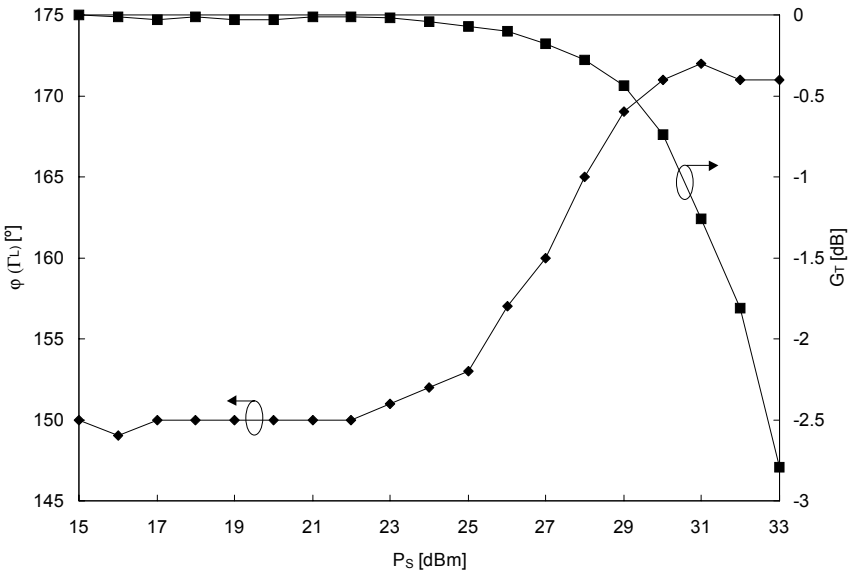

Figure 3.12: Phase optimum load reflection coefficient and transducer gain as a function of the applied source power. The optimum is determined for maximum output power at f = 8 GHz, V_{DS} = 9 V and V_{GS} = -0.75 V. The measured MESFET has a total gate width of 2.8 mm.

The search for the one-dB compression gain is done with the help of the following steps:

1. The transducer gain is measured at the small-signal source power, which is defined at the start of the measurement program.
2. The source power is increased with 3 dB steps and at each step the transducer gain is measured. This is repeated until the one-dB compression point is obtained. A 3 dB power step is used to reduce the time necessary to find the source power that will give the one-dB compression point. The one-dB compression point is defined as the point where the transducer gain is reduced with 1 dB compared to the gain measured at the small-signal source power.
3. The found source power is used to determine the optimum load impedance. This is discussed in more detail in the remainder of this section.
4. At the found optimum load reflection coefficient, the one-dB compression point is determined once again.
5. For the newly found one-dB compression point, the optimum load reflection coefficient is determined. Experiments have shown that it is only necessary to determine the one-dB compression point twice to determine the optimum load impedance.

A flow-graph of the optimum load determination procedure that was developed [3.24], is depicted in figure 3.13.

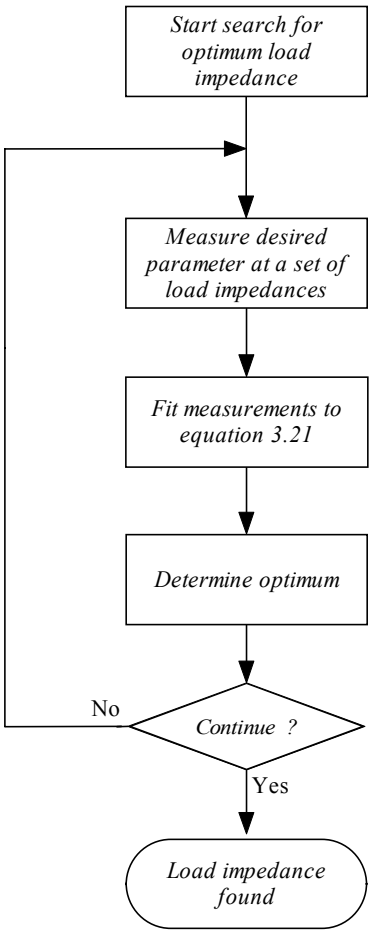

Figure 3.13: Flow chart of the developed optimum load reflection coefficient search algorithm.

As first step in finding the optimum load reflection coefficient the best guess for the location of the optimum, determined in the previous steps, is used as start reflection coefficient. As input power, the one that will result in the previously described one-dB compression point, is used. The steps following these choices are discussed in more detail in the remainder of this section.

The desired parameter, for instance the output power, is measured at a set of different load reflection coefficients. For the location of the load reflection coefficients the so-called Centre Composite Inscribed selection method is used, see figure 3.14. According to [3.25] this selection method is particular appropriate for wafer mapping when the relationship between the measured parameter is no more than second order. In our experience, this assumption is valid, in the neighbourhood of the optimum, for the parameters measured with our active load-pull measurement system.

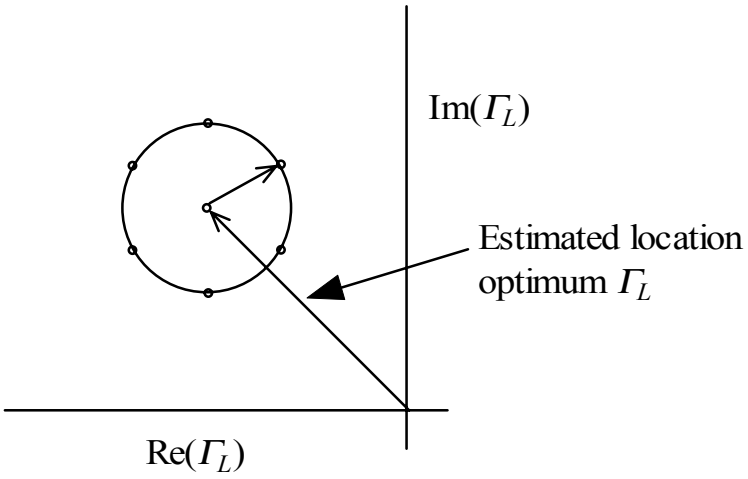

Figure 3.14: Location of the measured load reflection coefficients.

The first measurement will be performed with the load reflection coefficient depicted in the centre of the circle. This is the, at the given moment, best estimation of the optimum load reflection coefficient. After the measurement at this point is done at least five measurements, at a circle surrounding this centre must be performed. For our search algorithm, the radius of this circle is set to 0.1. Experiments have shown that the algorithm works good when six equally spaced reflection coefficients on the circle are measured.

At this point in the search algorithm, the measured parameter is fitted as a function of the load reflection coefficients. The measurement data is fitted with the help of a least square method to the following equation:

$$Z = a_0 + a_1 \cdot X + a_2 \cdot X^2 + a_3 \cdot Y + a_4 \cdot Y^2 . \tag{3.21}$$

In this equation, Z is the measured parameter that must be fitted. X is the real part of the load reflection coefficient, Y is the imaginary part of the load reflection coefficient and a_0 – a_4 are the fitted coefficients. This equation fits the measured parameters very well, see for example the values listed in table 3.2. After the measurement data are fitted to equation (3.21), the location of the optimum load impedance can be determined in two different ways. With the first method, the optimum load impedance is calculated from the derivatives of equation (3.21). This gives the following optimum:

$$X_{OPT} = \frac{-a_1}{2 \cdot a_2}, \tag{3.22}$$

$$Y_{OPT} = \frac{-a_3}{2 \cdot a_4}. \tag{3.23}$$

Table 3.2: Comparison measured and fitted output powers.

$\lvert\Gamma_L\rvert$	$\varphi(\Gamma_L)$	P_{OUT} measured [dBm]	P_{OUT} fitted [dBm]
0.647	151°	28.70	28.70
0.602	143°	28.36	28.27
0.701	144°	27.73	27.75
0.747	151°	28.03	28.09
0.704	158°	28.87	28.85
0.605	159°	29.19	29.18
0.547	151°	28.91	28.94

This method gives excellent results when the optimum lies inside the measured circle of load reflection coefficients. Outside the circle, still a good estimation can be found but sometimes an incorrect estimate of the optimum is found, which leads to unrealisable load impedances, see the first iteration contours indicated in figure 3.15. To circumvent this problem the following method is used. The value of equation (3.21) is evaluated for several thousands of points divided over a circle that has as centre the current best estimation of the location of the optimum load impedance and a radius equal to 0.2. From this set of function evaluations the maximum value is determined and the corresponding load impedance is used as the next estimation of the optimum load impedance. Close to the optimum, both methods will result in the same estimation of the optimum load impedance.

The whole procedure is repeated until one of the following criteria is met:

1. The maximum number of iterations is reached. This number is set to eight but it is seldom reached in practice. The average number of iterations used is three.
2. The difference between two successively determined optimum load reflection coefficients falls inside a specified resolution. The resolution used is 0.02 for the amplitude and 2° for the phase.

In the remainder of this section, two examples are shown, which demonstrate the performance of the discussed load-pull algorithm. The first example shows how the algorithm finds in two steps the optimum load impedance of a MESFET that has a total gate width of 3 mm, see figure 3.15. The results show that for this transistor a good estimation is found for the location of the load impedance for maximum output power. In addition, a reasonable estimation is found for the –0.5 dB contour. The results depicted for the first iteration show that the predicted location of the optimum load impedance has a negative impedance, which is not physical correct because the load impedance should be positive. This demonstrates the necessity of the second method to determine the location of the optimum load impedance.

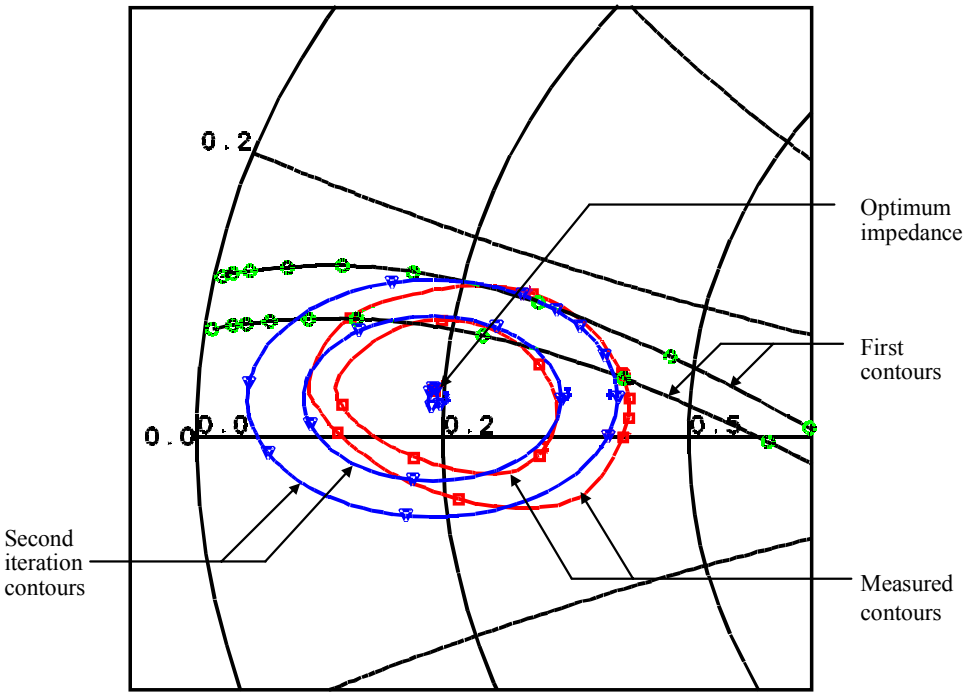

Figure 3.15: Comparison of output power contours of a 3 mm wide MESFET and the contours predicted with the in section 3.3.3.2 discussed load-pull algorithm. For each iteration the location for maximum output power and the –0.5 and –1 dB contours are shown.

Table 3.3: Estimation of the optimum load reflection coefficient of a 3 mm wide MESFET with the described load-pull algorithm for four different starting points.

	#1		#2		#3		#4	
Iteration	$\|\Gamma_L\|$	$\varphi(\Gamma_L)$	$\|\Gamma_L\|$	$\varphi(\Gamma_L)$	$\|\Gamma_L\|$	$\varphi(\Gamma_L)$	$\|\Gamma_L\|$	$\varphi(\Gamma_L)$
1	0.65	165°	0.50	150°	0.30	90°	0.80	-30°
2	0.65	178°	0.63	175°	0.22	153°	0.53	-22°
3	0.66	175°	0.68	176°	0.40	174°	0.29	-6°
4	0.67	175°	0.66	175°	0.60	176°	0.10	23°
5	0.67	175°	0.66	175°	0.72	172°	0.10	169°
6	0.67	175°	0.66	175°	0.67	174°	0.30	174°
7	0.67	175°	0.66	175°	0.67	175°	0.51	175°
8	0.67	175°	0.66	175°	0.67	175°	0.71	177°
9	0.67	175°	0.66	175°	0.67	175°	0.67	175°

In the second example it is shown how the load-pull algorithm converges to the same optimum load impedance independent of the starting position used by the algorithm, see table 3.3. Another conclusion that can be drawn from the depicted results is that the number of necessary iterations depends on the location of the start position in relation with the location of the optimum load impedance. The first example shows the situation where the conjugated of the S_{22} was used as start point for the load-pull algorithm. This choice for the start point leads to the fastest determination of the optimum load impedance.

3.4 Conclusions

In this chapter, the measurement systems used for the characterisation of both the high-power amplifiers and the components used in these amplifiers are discussed.

Two and a three-port S-parameter measurement systems are discussed. It is shown that it is of vital importance for the on-wafer measurement accuracy to eliminate the influence of the coplanar to microstrip transition present at all the ports of the test structures discussed in this thesis. The necessity to remove this transition leads to a Line Reflect Line type of S-parameter calibration.

A three-port measurement system is discussed, which is based on the measurement of three sets of two-port S-parameter measurements and the load impedance of the terminated third port. For the three-port measurement system, a calibration method is developed that allows for the accurate calibration of two-port S-parameter structures whose input and output ports are not in line.

The new large-signal measurement system is built around the HP85110A pulsed Network Analyzer. The developed system allows for both the characterisation of the realised high-power amplifiers as well the characterisation of the used transistors. For the evaluation of the transistors a load-pull measurement system is developed that is controlled with the help of a novel load-pull algorithm. The large-signal measurement system is fully vector error corrected.

3.5 References

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4. Component models

4.1 Introduction

It is essential for the design of X-band high-power amplifiers to have accurate equivalent electrical models available. In this chapter the models which are used and where relevant the method to extract the model parameters is discussed. This chapter starts with a discussion of the electrical models of the active components and the way the model parameters are extracted. Determination of transistor models was necessary because none were available for the transistors that were used in the discussed high-power amplifier designs. In the scope of the work discussed, it also turned out that the microstrip discontinuity models available in the used design software were not accurate enough. In addition, the electrical models of certain components given by the foundry, e.g. the viahole turned out to be inaccurate or unavailable. The electrical models of the passive components are discussed in section 4.3.

4.2 Active components

4.2.1 Transistor model extraction

In this section, the large-signal model used for the both the MESFET and the HFET is discussed. Extraction of our own transistor model parameters is necessary because also the layout of the transistor is considered as a design parameter, see also section 2.3.4 and chapter 5. For the selected transistor size, meaning number of gate fingers, unit gate width, gate to gate spacing and e.g. fishbone layout no transistor model is supplied by the foundry. Therefore, the design work discussed in this thesis was started with the development of a transistor matrix. Such a transistor matrix, although smaller, was added with every high-power amplifier design. The reasons for this are the possibility to check the large-signal performance of the in the design used transistors and the possibility to add larger transistors for future amplifier designs that require a higher output power. An example of such a transistor matrix is shown in figure 4.1. In this picture, a HFET transistor matrix is depicted. The transistors are measured in a two-port configuration where the source of the transistor is grounded with the help of one viahole at each side of the transistor. The common source mode shown here is used for all transistors discussed in this thesis. The transmission lines required to calibrate the measurement system, see section 3.2, can also be seen on the right in figure 4.1. After calibration, the measurement reference plane is shifted from the edge of the probe pad to the input and the output of the transistors. This is possible because the transistors are connected to the input and the output of the test structure with the help of 50 Ω transmission lines, of which the physical and electrical length is exactly known. In this

case, also a one-port viahole test structure and a two-port capacitor test structure are shown in figure 4.1. The extraction of the equivalent circuit of latter components is discussed in section 4.3.

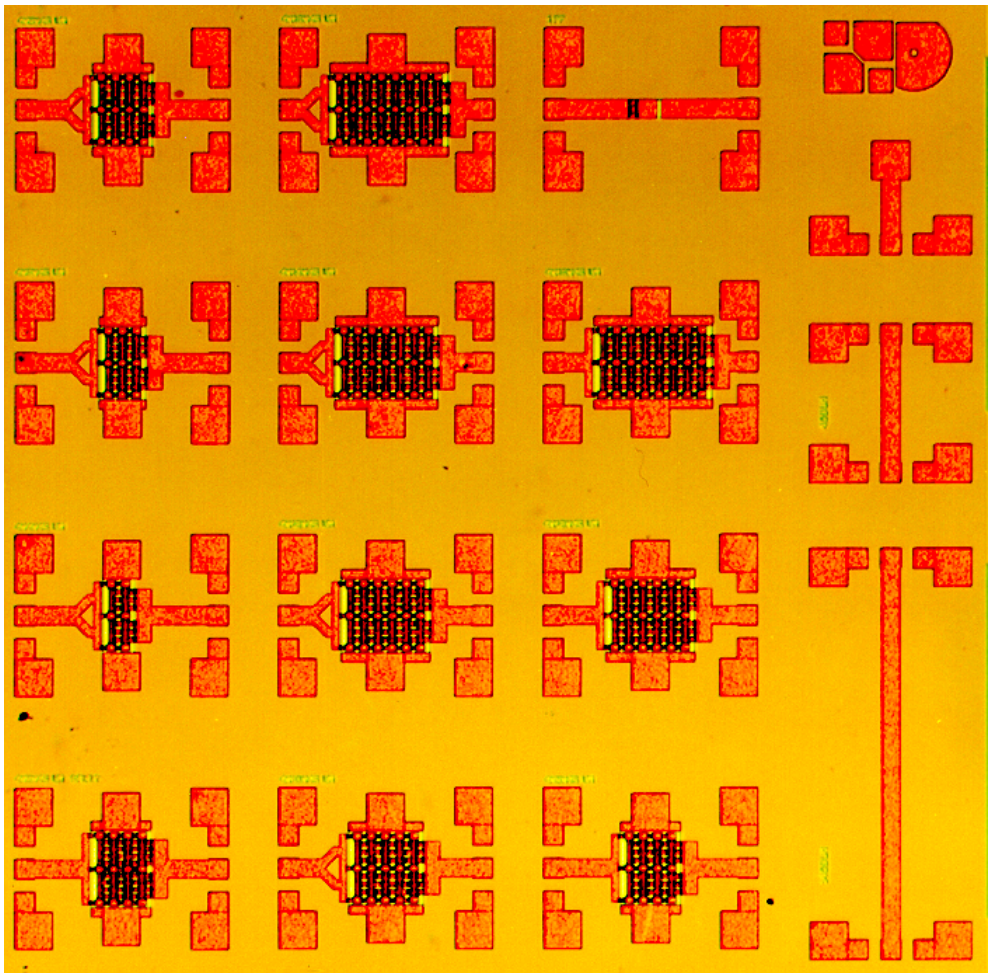

Figure 4.1: Example of a HFET transistor test matrix with LRL calibration structures, a one-port viahole test structure and a two-port capacitor test structure, chip size 4 x 4 mm^2.

Under small-signal conditions the following equivalent intrinsic transistor model is used for both MESFET and HFET transistors, see figure 4.2. This figure shows the relation between the equivalent transistor model parameters and their location in the cross section of the transistor.

Besides the intrinsic transistor model, also the influence of the layout of the transistor has to be included in the model. Figure 4.3 shows the complete small-signal FET model including both the intrinsic and extrinsic FET model parameters. The intrinsic parameters are dependent on the bias voltages. The extrinsic parameters are considered bias independent and are determined by the layout of the transistor.

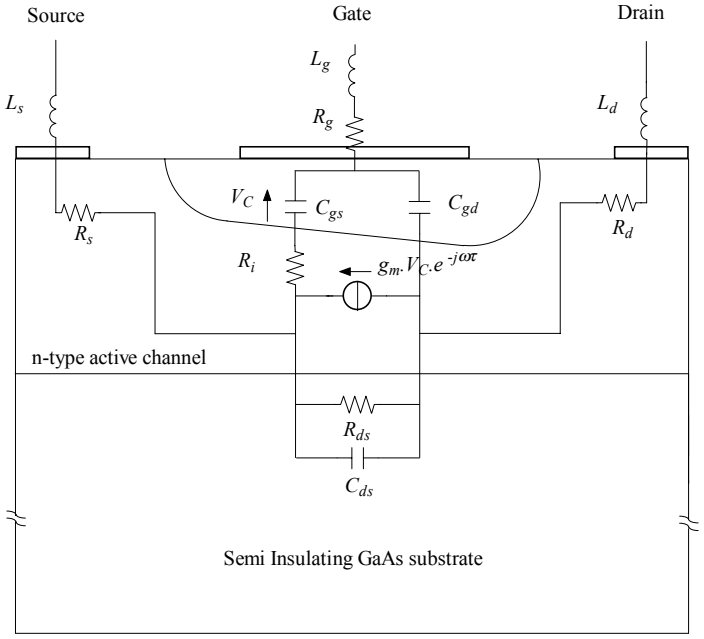

Figure 4.2: Cross section FET with the corresponding equivalent transistor model.

As large-signal transistor model, the EEFET3 model has been used for the MESFET technology and the EEHEMT1 model has been used for the HFET technology. Both models originate from Agilent [4.1] and can be used in our design environment. In this section, the electrical model and the way the model parameters are extracted will be discussed. In the next section, the large-signal performance of the transistor models is compared with large-signal measurement results. The EEFET3 and EEHEMT1 large-signal models incorporate the following important features [4.2]:

- Accurate isothermal drain-source current model, which fits virtually all processes.
- Self-heating correction for drain-source current.
- Charge model that accurately tracks measured capacitance values.
- Dispersion model which permits simultaneous fitting of high-frequency conductances and DC characteristics.
- Breakdown model which describes the gate-drain current as a function of both V_{GS} and V_{DS}.
- Transconductance formulation, which permits accurate fitting of the g_m compression, found in HFETs.

The large-signal FET models were extracted with the help of the program XTRACT from Agilent [4.2]. The transistor model extraction is based on a set of two-port S-parameters measured at a number of bias points. The measurement set-up and calibration methods, discussed in section 3.1 and section 3.2, were used to obtain these S-parameters. The model extraction starts with the determination of the extrinsic parameters. The extrinsic parameters are extracted with the help of so called cold FET measurements [4.3]. This means that the drain-source voltage is set to zero and the gate-source diode is set in forward. Under these conditions the equivalent FET model simplifies significantly, see figure 4.4, and the parasitic inductors are easily extracted from the measurement results [4.3].

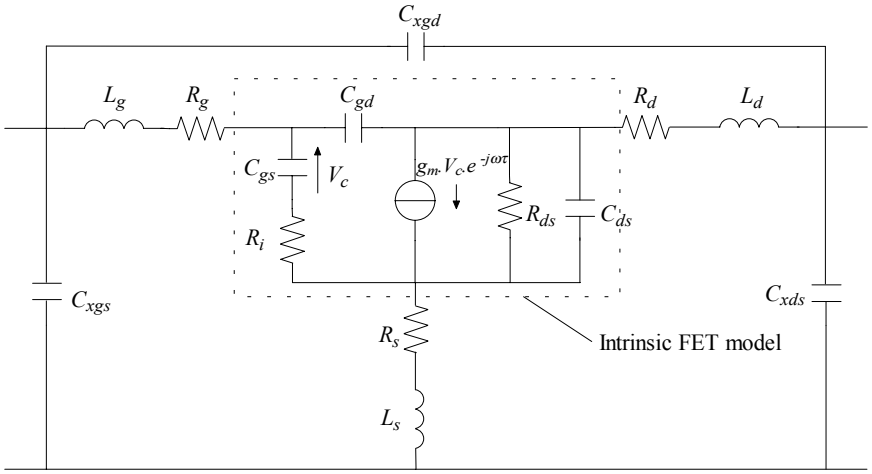

Figure 4.3: FET model topology including both intrinsic and extrinsic parameters.

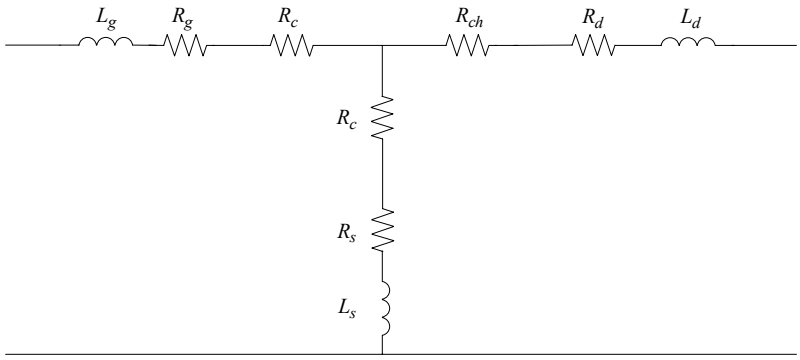

Figure 4.4: FET model under zero bias conditions with the gate-source diode set in forward.

The extrinsic source resistance R_s is determined with the help of the method described by Yang and Long [4.4]. After the value of R_s is known the values of R_g and R_d can easily be

determined from the previously mentioned cold FET measurement results. This is the way it is done in XTRACT, an alternative approach is proposed by Costa et al. [4.5]. Costa determines the extrinsic resistors from three different cold FET measurements with the help of a simple optimisation scheme. According to [4.3], the extrinsic capacitors can be extracted from a cold FET measurement with the gate voltage below the pinch-off voltage. This is not the way it is done in XTRACT; there these capacitors are determined with the help of the optimisation method described by Arnold and Golio [4.6]. From literature, a variety of methods is known for the determination of the extrinsic model parameters some avoid the use of the potential destructive forward gate measurements [4.7]. Others use an optimisation method [4.8] were the flatness of the intrinsic model parameters as a function frequency is used as error criterion for the optimisation of the extrinsic model parameters.

After the extrinsic model parameters are determined, the intrinsic parameters can be determined analytically from the measured S-parameters that have been converted to Y-parameters after removal of the extrinsic model parameters [4.3]. In XTRACT an exact analytical extraction like the one described by Berroth and Bosch [4.9, 4.10] is not used but the approximation described by Dambrine et al. [4.3]. This approximation works well as long as the correct frequencies are used for the determination of the intrinsic model parameters.

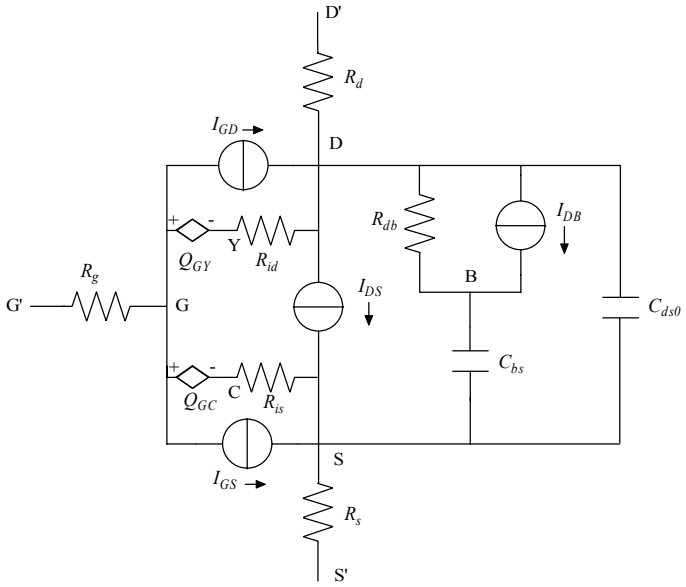

Figure 4.5: Large-signal EEFET3/EEHEMT1 transistor model.

The intrinsic FET model parameters are determined for all measured bias points. The first step in the extraction of the large-signal model is the fitting of the measured DC bias points. After this is accomplished, the intrinsic model parameters are fitted as a function of the measured bias voltages. The first parameter that is fitted is the drain-source current source under AC conditions. Fitting of the IV curves under both DC and AC conditions is

necessary due to the dispersion that can exists between the parameters measured under these conditions [4.11]. The current source I_{DB} that is used to connect these two different current sources is shown in figure 4.5. After the current sources have been fitted as a function of the bias voltages, the capacitors will be fitted.

The following model parameters are treated in the EEFET3/EEHEMT1 model as bias point independent: C_{ds}, R_i and τ. This assumption is certainly inadequate for τ, see for instance [4.12]. The small-signal values, extracted at the operating bias point of the high-power amplifier, are used to circumvent problems arising due to this bias independence of the model.

The breakdown behaviour of the transistor is modelled with the help of the equations given by Taijma [4.13]. In the next section, a comparison will be made between the obtained large-signal simulation results and the measurement results.

4.2.2 EEFET3/EEHEMT1 large-signal transistor model results

In this section, the performance of the large-signal EEFET3/EEHEMT1 simulation results are compared with measurement results. The first verification that is shown is the fitting of the measured DC IV curves as a function of the applied gate-source voltage, see figure 4.6. As can been seen an excellent fit has been obtained.

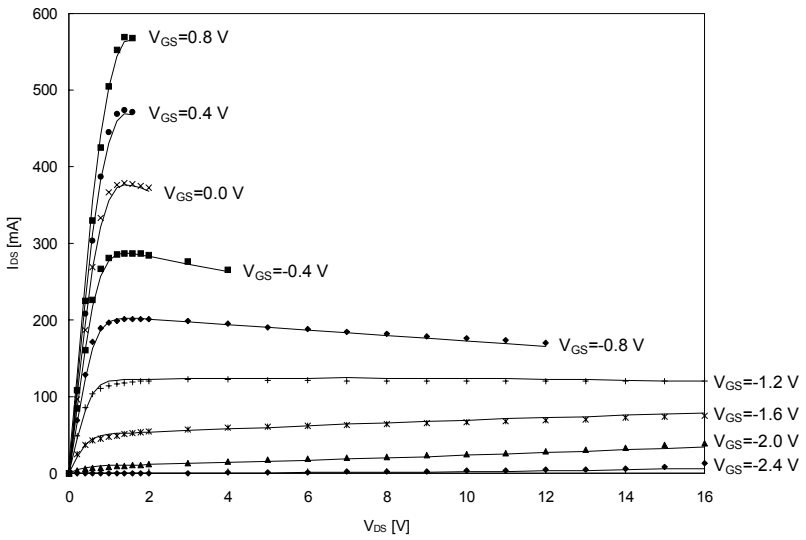

Figure 4.6: Comparison between simulated (solid lines) and measured IV curves (markers) of a MESFET that has a total gate width of 1.5 mm (12 gate fingers).

What is obvious from the depicted results is the fact that not all curves have been measured at the same drain bias points. The reason for this is the DC power compliance that had to be used to prevent the destruction of the transistors. Also the effect of the self-heating of the transistors is visible by the negative slope of the drain current for larger gate to source voltages. As next step the measured optimum load impedances for maximum output power and power added efficiency (PAE), measured with the load-pull measurement set-up described in section 3.3, are compared with the ones predicted using the large-signal FET model. The results of this comparison are listed in table 4.1 for a typical example. These results show that there exists an excellent agreement between the measured and predicted optimum load impedances.

Table 4.1: Comparison between measured and predicted optimum load impedance of a MESFET that has a total gate width of 1.5 mm (12 gate fingers) at f = 10 GHz, V_{DS} = 9 V and V_{GS} = -1.6 V.

	Measured	Simulated
Z_L for maximum P_{OUT}	13.1+j10.4	15.4+j8.8
Z_L for maximum *PAE*	13.1+j10.4	15.2+j10.1

A comparison between the large-signal measurement results at the optimum load impedance for maximum output power and the simulated results is shown as a function of the source power in figure 4.7.

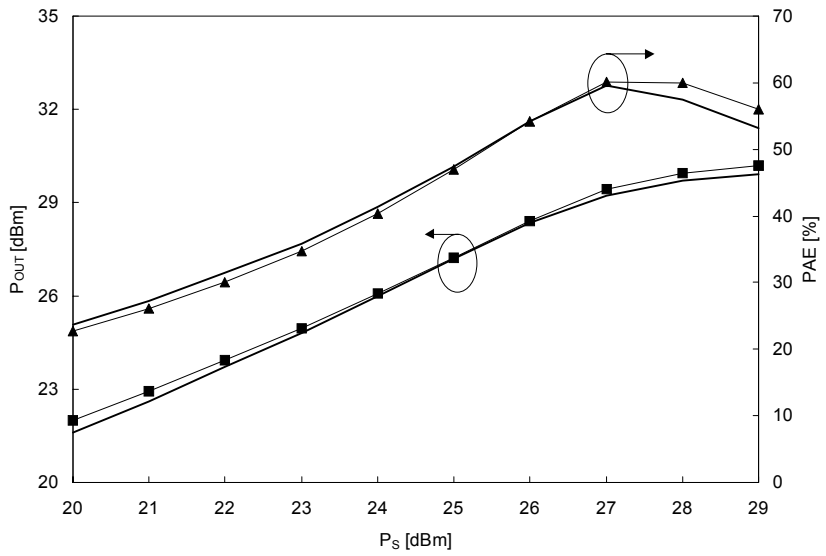

Figure 4.7: Comparison between measured (solid lines) and simulated (lines plus markers) large-signal performance, of a MESFET that has a total gate width of 1.5 mm (12 gate fingers), at f = 10 GHz, Γ_L = 0.6/155°, V_{DS} = 9 V and V_{GS} = -1.6 V as a function of the applied source power.

From the depicted results can be concluded that a good agreement is obtained between large-signal measurement and simulation results with the help of the EEFET3/EEHEMT1 model. One point of concern is the fact that the drain current is not correctly determined with the help of the large-signal transistor model and therefore the power added efficiency is not correctly determined. The simulated power added efficiency results have been calculated with the help of the empirically found factor of 0.9 for the simulated drain current. The drain current corrected in this way, results in a good prediction of the power added efficiency as can be seen in figure 4.7. The reason that the drain current is predicted too high is the way in which the dispersion between the DC and AC performance is solved in the EEFET3/EEHEMT1 models. The increase in drain current as a function of the source power occurs in the AC part of the model. The AC drain-source resistance is lower than the DC drain-source resistance and the model therefore will predict the DC component of the AC current waveform too high. A way out of this problem is the splitting of the large-signal FET model in two separate FET models one for DC and one for AC that are combined with appropriate networks to form one transistor model, see [4.14]. This was not necessary for the transistor models discussed because the drain correction factor mentioned before results in simulations that are accurate enough for high-power amplifier design purposes. In the MESFET example mentioned before a drain correction factor of 0.9 was used, the average correction factor for both MESFET and HFET is 0.85. This factor was found from a comparison between load-pull measurements and large-signal simulations for a large number of transistors with different number of gate fingers and unit gate width.

4.3 Passive components

4.3.1 Introduction

In this section, the models of the passive components are discussed. Whenever possible the verification of the models against measurements is performed. When the models turned out to be inaccurate, as it was the case for the microstrip discontinuities, new models were developed. These new models are based on electromagnetic field simulations. New models were also extracted when foundry models were considered insufficiently accurate for the design of high-power amplifiers at X-band. Examples of such foundry models are the MIM capacitor and the viahole inductance. In addition, an example of the use of electromagnetic field simulations to come to a more compact layout of the matching networks is discussed in this section.

4.3.2 Microstrip line

Microstrip lines are used for interconnection between components and for realising inductors, see also section 2.4.1. A simplified schematic of a transmission line with length l is depicted in figure 4.8.

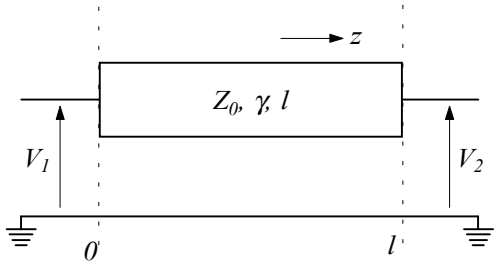

Figure 4.8: Simplified schematic transmission line.

In general, the following equations are used to describe the electrical behaviour of a transmission line:

$$V(z) = V_1 \cdot e^{-\gamma z} + V_2 \cdot e^{\gamma z}, \tag{4.1}$$

$$I(z) = \frac{1}{Z_0} \cdot \left(V_1 \cdot e^{-\gamma z} - V_2 \cdot e^{\gamma z} \right). \tag{4.2}$$

In this equation Z_0 is the characteristic impedance of the transmission line and γ is the propagation constant of the transmission line. The propagation constant γ can also be written as:

$$\gamma = \alpha + j\beta . \tag{4.3}$$

In this equation α is the attenuation constant and β is the phase constant of the transmission line. The model used to describe these transmission line parameters is the one available in Libra [4.1]. This microstrip line model is based on the model described by Hammerstad and Jensen [4.15] for the static impedance Z_0 and the effective dielectric constant ε_{eff}. The attenuation factor α is based on the equations given by Wheeler [4.16]. The dispersion effects are described with the help of the equation given by Kirsching and Jansen [4.17]. A comparison of the Libra microstrip line model with both electromagnetic field simulations and measurement results shows good agreement, see figure 4.9.

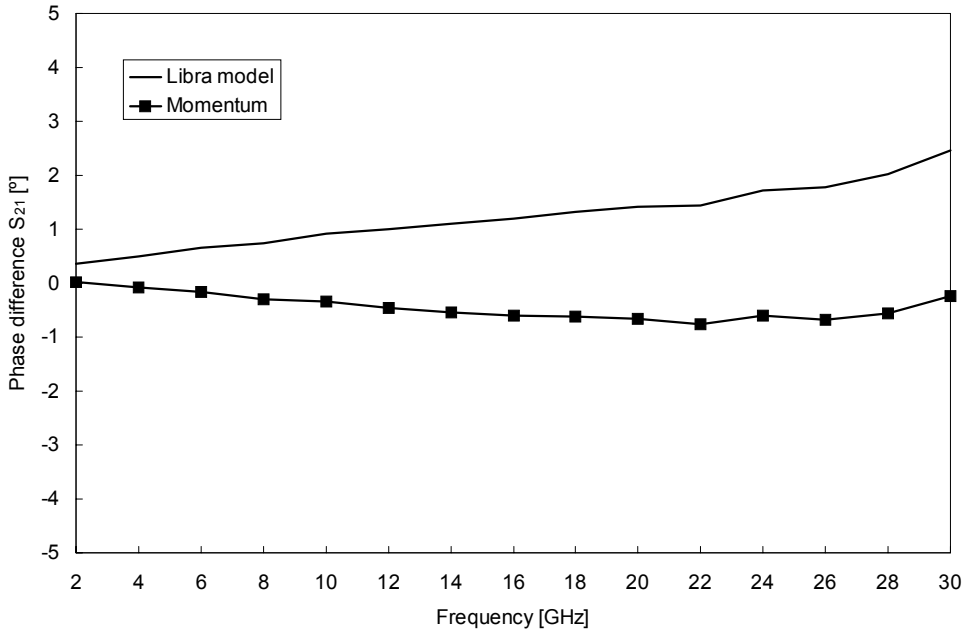

Figure 4.9: Comparison of the phase difference between the measured S_{21} and the one predicted with the help of Libra [4.1] and Momentum [4.18]. The results are obtained for a line with a width of 70 µm and a length of 3000 µm realised on a 100 µm thick substrate (see table 4.2).

The depicted results show that the accuracy of the microstrip line simulated with Libra and the one simulated with Momentum (electromagnetic field simulator) are comparable. The Libra model has been used because its simulation time is only a fraction of that of a Momentum simulation. More details regarding the measurement results of microstrip lines and other microstrip discontinuities can be found in [4.19].

4.3.3 Microstrip discontinuities

During the design of the high-power amplifiers, it turned out that the following microstrip discontinuities were inaccurate or unavailable.

- Microstrip T-junction
- Microstrip Y-junction
- Microstrip crossing
- Microstrip 45° bend
- Microstrip 90° bend

An overview of these microstrip discontinuities is shown in figure 4.10. In this figure, the reference planes of the models (P_1-P_4) and the dimensions that can be varied are shown. Note that the Y-junction model is not available in Libra; the other models turned out to be inaccurate.

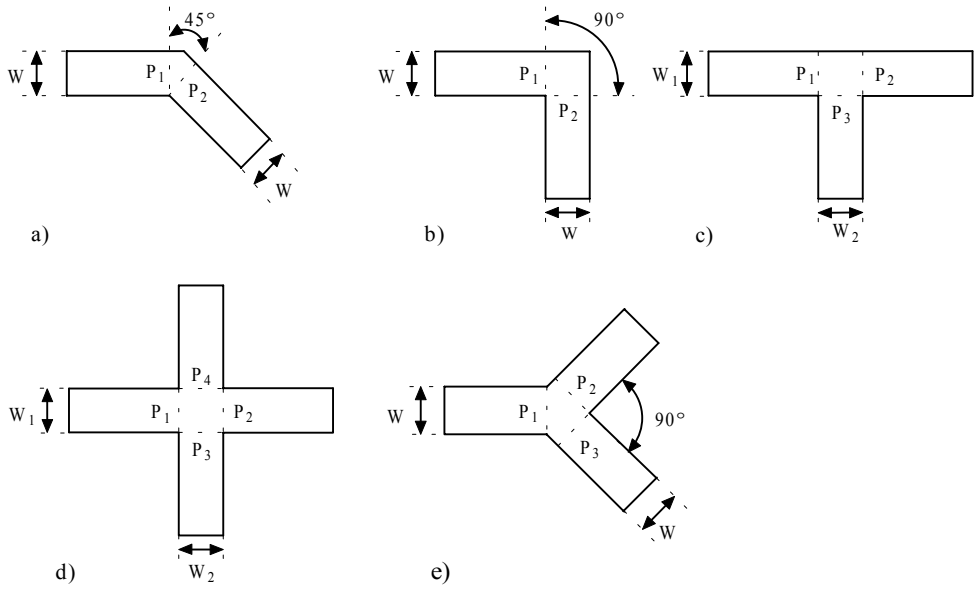

Figure 4.10: Overview of the layout of the modelled microstrip discontinuities, a) 45° microstrip bend, b) 90° microstrip bend, c) microstrip T-junction, d) microstrip crossing and e) microstrip Y-junction.

A comparison of the microstrip discontinuity models available in Libra with electromagnetic field simulations and measurements is shown in [4.19]. From these results, it is concluded that the models in Libra are not accurate enough for use in the high-power amplifiers discussed here. Scaleable models have been extracted for these components based on electromagnetic field simulations. Scaleable models are needed because optimisation of the matching networks, when electromagnetic field simulators are employed is excessively time consuming.

The procedure used for the extraction of scaleable models based on electromagnetic field simulations is depicted in figure 4.11. The first step consists of simulating, a matrix of different sizes with the help of an electromagnetic field simulator. This is done for each discontinuity. The dimensions simulated, depend on the kind of structure, e.g. the width of a 45° microstrip bend is varied between 10 μm and 100 μm, see figure 4.10.

After the simulations have been completed the S-parameters are converted to Y-parameters and the equivalent circuit is determined with the help of the method described in [4.20]. The

approximation, namely that $R << \omega L$, assumed during this extraction turns out to be valid, up to at least 50 GHz, for all discontinuity models described in this thesis. After the model parameters have been determined, taking into account the eventual symmetry in the structure, the model parameters are fitted as a function of their dimensions with the help of a least-square fit routine. Finally, the models are implemented in the design software and verified for both the dimensions used during the extraction and other dimensions inside and outside the extraction range. All discontinuity models discussed in this thesis are valid for widths ranging from 10 to 100 µm.

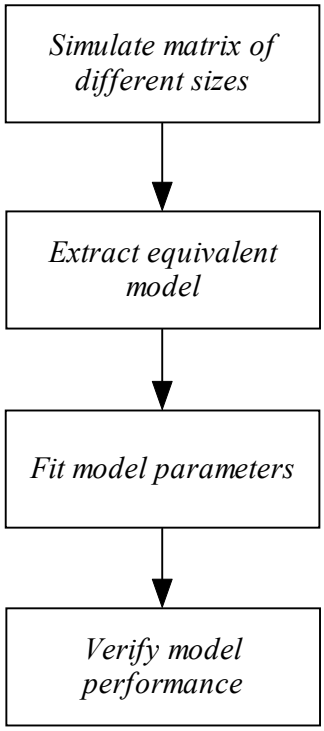

Figure 4.11: Extraction steps based on electromagnetic field simulations.

In the following subsections, the models mentioned before will be discussed. The equivalent circuit is shown for the discussed discontinuities. In appendix A, the equations used to describe the dependence of the model parameters on their geometrical dimensions are given. Where available also a comparison between electromagnetic field simulations, Libra models, measurement results and the new extracted discontinuity models will be shown. The properties listed in table 4.2 have been used for the simulations to obtain the discontinuity models described in the next subsections.

Table 4.2: Substrate and metal definitions used in MOMENTUM [4.18].

ε_r	12.9
tan(δ)	0.001
Height GaAs substrate	100 µm
Thickness metal	5 µm
Conductivity gold	33.10^6 S/m

4.3.3.1 45° microstrip bend

The 45° microstrip bend model used in Libra is based on the model described in [4.21, 4.22]. The shift of the reference planes is calculated with the help of the microstrip line model of Hammerstad and Jensen [4.15]. In the Libra model, dispersion and conductor losses are neglected. In figure 4.12, the equivalent circuit of the 45° microstrip bend is shown. The reference planes of the model are indicated with P_1 and P_2, see also figure 4.10.

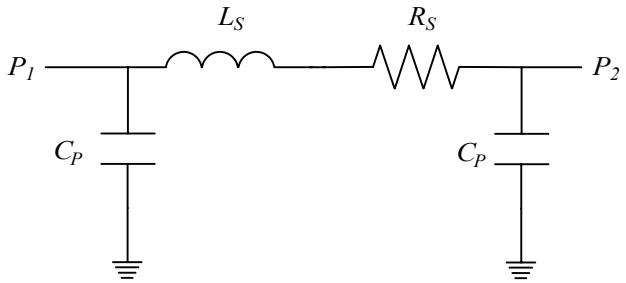

Figure 4.12: Equivalent circuit of the 45° microstrip bend.

In appendix A, the equivalent model equations of the 45° microstrip bend model are given. The results obtained with the help of the model available in Libra, Momentum simulations, and the TNO electromagnetic field simulation based model and measurement results are compared in figure 4.13. The angle of S_{21} is shown because this parameter shows the largest difference between on the one hand the Libra simulations and on the other hand, the electromagnetic field simulations, our own TNO model and the measurement result. From figure 4.13, it is clear that there is a good agreement between the measurement results, the TNO model and the electromagnetic field simulations. The result simulated with Libra is clearly wrong. The phase difference observed for the 45° bends, which are for instance used in the inductors in the output-matching network of a high-power amplifier, results in significant difference in the simulated and realised frequency band, see also section 6.2.3.5. The equivalent inductance predicted with the help of the Libra models will be too small. This in turn results in a reduction of the bandwidth realised at the end of the band. In [4.19], all S-parameters of the 45° microstrip bend for several other bend widths are shown.

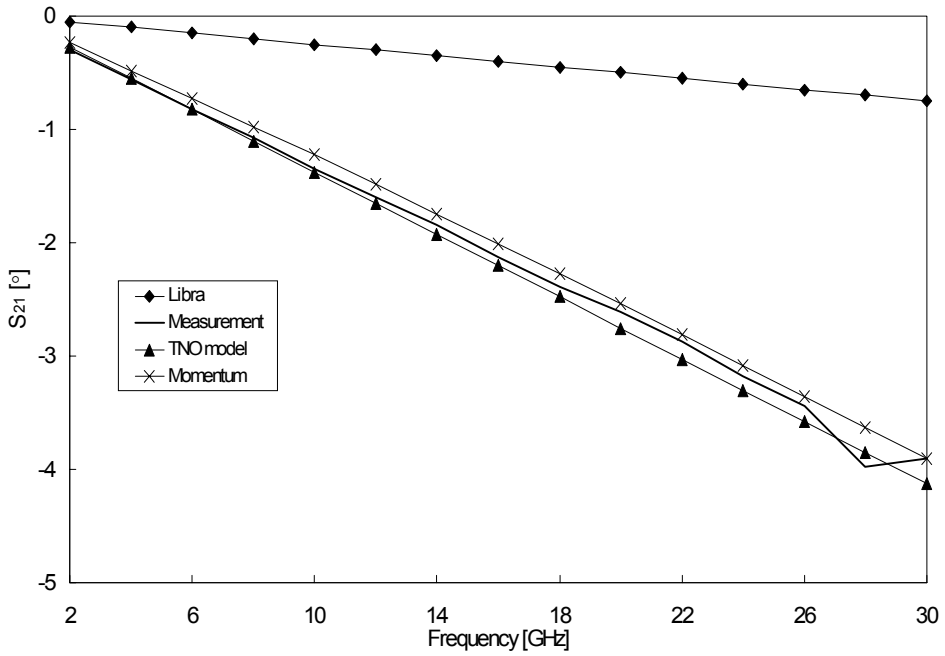

Figure 4.13: Comparison of the angle of S_{21} of a 45° microstrip bend with a width of 100 μm.

4.3.3.2 90° microstrip bend

The model used in Libra is based on the equations given in [4.22]. In figure 4.14, the equivalent circuit of the 90° microstrip bend based on electromagnetic field simulations is shown. In appendix A, the model equations are given. A comparison between the results obtained with the help of the model available in Libra, Momentum simulations, our own electromagnetic field simulation based TNO model and measurement results is shown in figure 4.15. Again, the angle of the S_{21} is shown. It is clear from figure 4.15 that there is a good agreement between the measurement results, the TNO model and the electromagnetic field simulations. The Libra simulation is still wrong but the difference is less than was the case for the 45° microstrip bend.

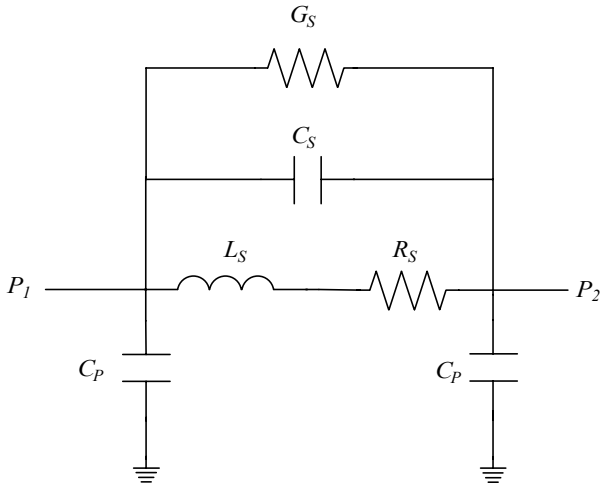

Figure 4.14: Equivalent circuit of the 90° microstrip bend.

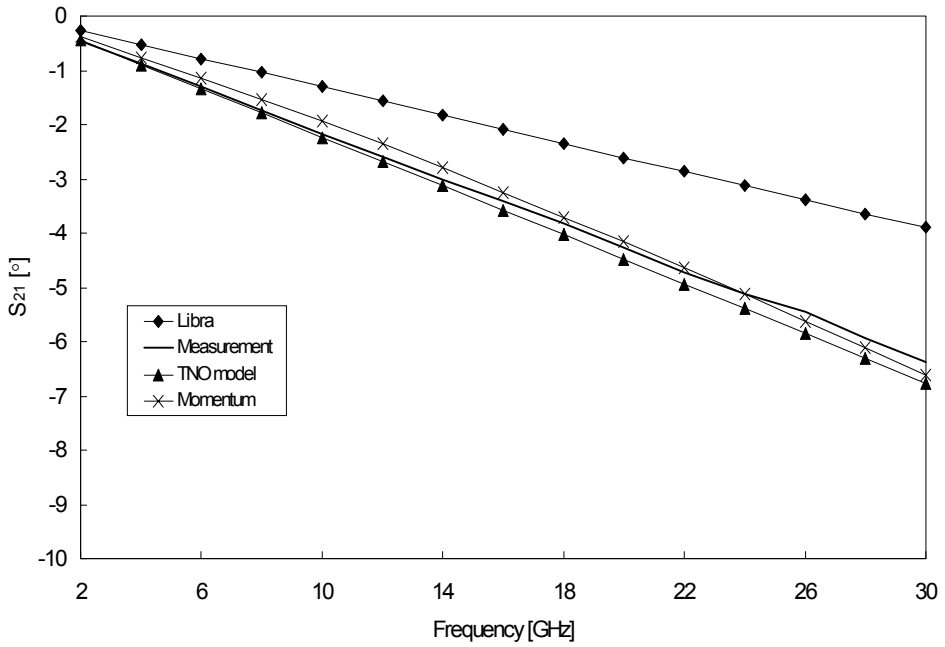

Figure 4.15: Comparison of the angle of S_{21} of a 90° microstrip bend with a width of 100 μm.

4.3.3.3 Symmetrical microstrip T-junction model

The microstrip T-junction model used in Libra is the one described by Hammerstad and Jensen [4.15]. In this model, the dispersion is accounted for using the equations given in [4.17]. In figure 4.16, the equivalent circuit of a symmetric microstrip T-junction, which is based on electromagnetic field simulations, is shown.

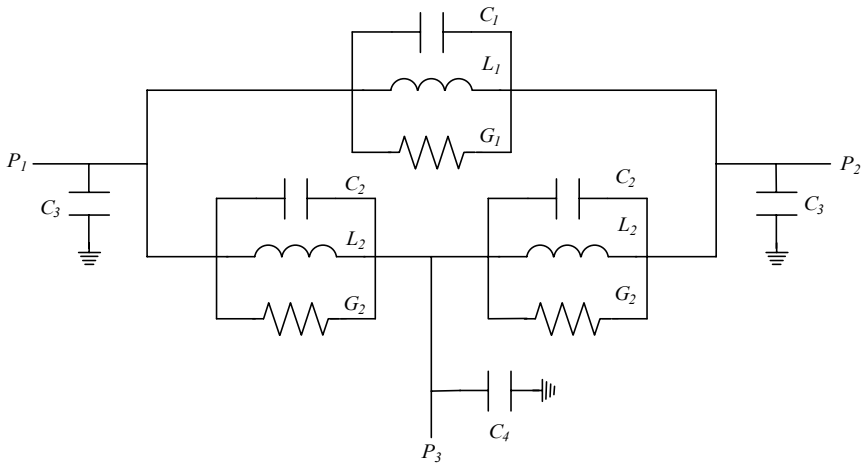

Figure 4.16: Equivalent circuit of the symmetric microstrip T-junction.

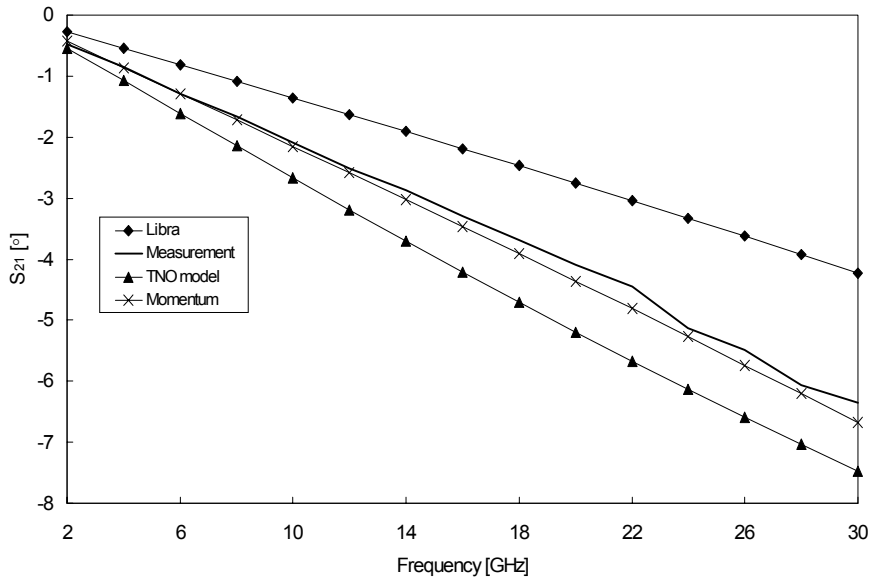

Figure 4.17: Phase S_{21} of a 70 x 70 μm symmetrical T-junction.

The measurement results are compared with the simulation results in figure 4.17. In this figure, the phase of S_{21} for a symmetrical T-junction, with W_1 and W_2 equal to 70 µm, is shown. There is very good agreement between the measurement result and the electromagnetic field simulations for the phase of S_{21}. Both the Libra and TNO model give slightly less accurate results. It should nevertheless be noted that the trend that is predicted with the TNO model is better than the Libra model at high frequencies. Additional results can be found in [4.19, 4.23].

4.3.3.4 Microstrip crossing model

For the microstrip model of a crossing, the one described by Gupta et al. [4.24] is used in Libra. The capacitors in this model are calculated with the help of the equations given in [4.1]. In figure 4.18, the equivalent circuit of a symmetric microstrip crossing is shown. The crossing is termed symmetric because the opposite sides have the same dimensions. This is in contrast to a general crossing that can have four different dimensions. For the high-power amplifier designs discussed here, the symmetric crossing is sufficient for the initial design of the matching networks. The location of the reference planes and the ports are indicated with P_1 - P_4, in figure 4.10.

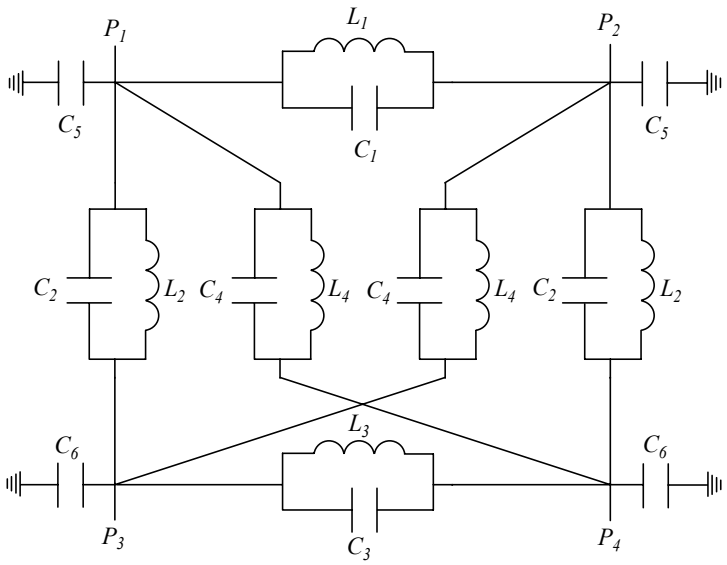

Figure 4.18: Equivalent circuit of the symmetric microstrip crossing.

No test structures were available for the experimental validation of the microstrip-crossing. Therefore, the comparison is limited to the Libra model, the TNO model and the electromagnetic field simulations as shown in figure 4.19. The result shows that performance of these three models is more or less the same.

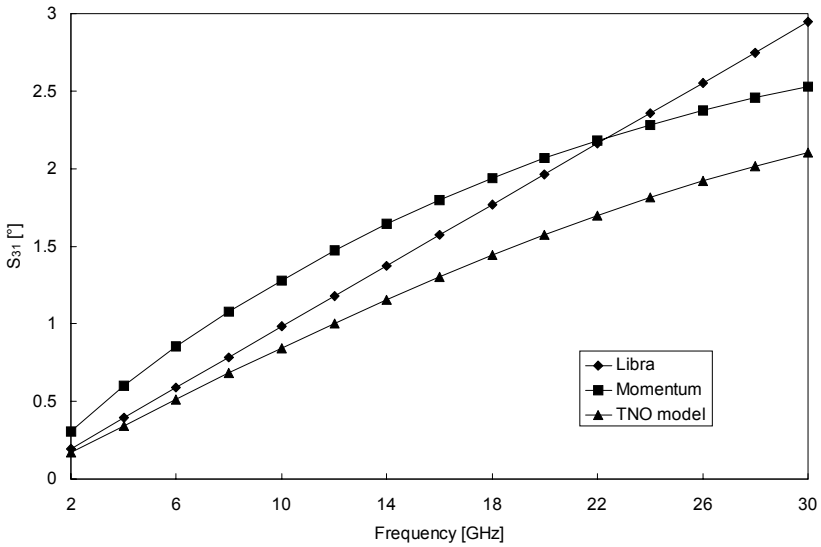

Figure 4.19: Comparison of the simulation results of a 100 x 100 µm symmetric microstrip crossing.

4.3.3.5 Symmetrical microstrip Y-junction model

The symmetrical Y-junction is a microstrip discontinuity of which no model is available in Libra. Nevertheless, it is used very often in high-power amplifier designs because it facilitates the realisation of very compact matching networks. It has turned out to be extremely useful in the output-matching network. The model that is used for the Y-junction is depicted in figure 4.20.

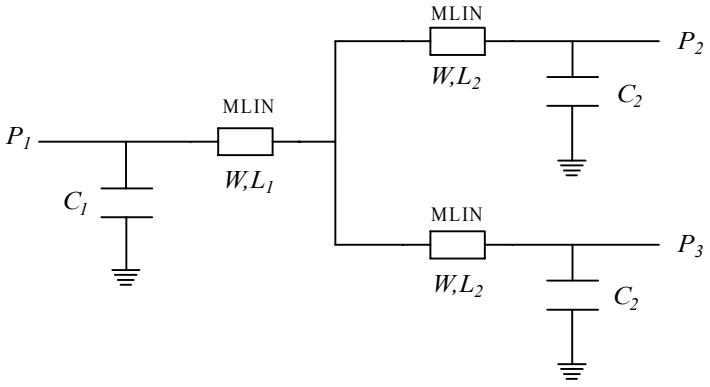

Figure 4.20: Equivalent circuit of a symmetrical Y-junction. MLIN indicates the Libra microstrip line model [4.1].

In order to extract the Y-junction model from electromagnetic field simulations a slightly different approach is used than discussed in the previous sections for the other discontinuities. This is because the parameters [4.20] extracted with the help of the Rautio method are difficult to fit as a function of the physical dimensions. Therefore, the model parameters have been determined via optimisation of simulated S-parameters of the equivalent circuit depicted in figure 4.20.

The parameters that are optimised are L_1, L_2, C_1 and C_2. The width of the microstrip line W is kept fixed to its physical dimension. With the term MLIN the microstrip line model of Libra is indicated. The extracted model parameters are described in [4.25]. The resulting scaleable model equations are listed in appendix A.

The measurement results depicted in figure 4.21 show that there is a good comparison between the Y-junction model extracted on the basis of electromagnetic field simulations and the measurement results of a 100 μm wide Y-junction. The layout of the test structure used for this measurement was already shown in figure 3.4. To obtain this result the complete procedure for the measurement and calibration of a three-port structure as outlined in section 3.2.2 was followed. The S-parameters of the microstrip lines and 45° microstrip bends, depicted in figure 3.4, are de-embedded from the measurement results. The results from figure 4.21 show the validity of both the measurement procedures as are discussed in chapter 3 and the microstrip models based on electromagnetic field simulations, discussed in this chapter.

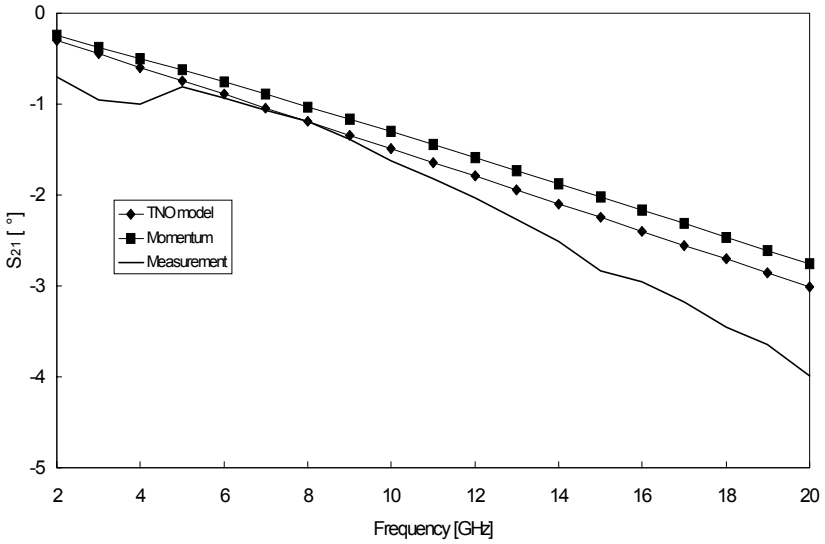

Figure 4.21: Comparison of the measured and simulated angle of the S_{21} of a 100 μm wide Y-junction.

4.3.4 Inductor

Microstrip lines have been used as inductor in the high-power amplifier designs, see section 2.4.3. A shunt inductor to ground can be approximated with the help of a short-circuited transmission line. The input impedance of such a transmission line is given by:

$$Z_{IN} = j \cdot Z_0 \cdot \tan(\beta \cdot l). \tag{4.4}$$

The input impedance of a small short-circuited transmission line can be approximated as follows:

$$Z_{IN} \approx j \cdot Z_0 \cdot \beta \cdot l = j \cdot \omega \cdot \frac{Z_0 \cdot l \cdot \sqrt{\varepsilon_{eff}}}{c}. \tag{4.5}$$

The latter equation shows that a short-circuited transmission line can be used as a parallel inductor to ground. It is also evident that for small inductance values a trade-off can be made between the length l and the characteristic impedance Z_0 of the transmission line. This can be of use when there is for instance a limited chip area available in that case, the impedance of the line can be increased to realise the inductance value required with a smaller line length.

Series inductors can also be realised with the help transmission lines. For this purpose a microstrip line can be approximated with the help of the following equivalent pi-network, see figure 4.22.

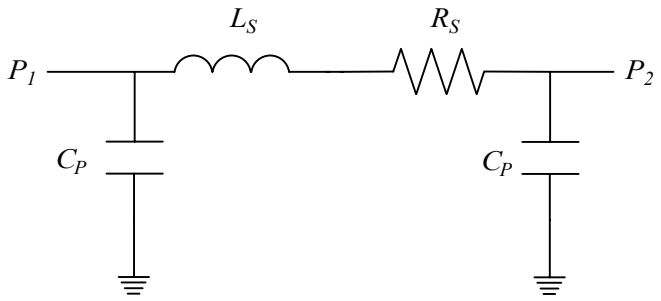

Figure 4.22: Approximation of microstrip line with an equivalent pi-network.

For short transmission lines the capacitors can be neglected, see figure 4.23, and the equivalent circuit in that case reduces to that of an inductor. The parameters of the equivalent pi-network have been fitted as a function of the length and width of these microstrip lines. This equivalent pi-network is used for the translation of a synthesised matching network with ideal components into a layout, see section 6.4. An overview of the equations used for the model components depicted in figure 4.22 is given in appendix A.7.

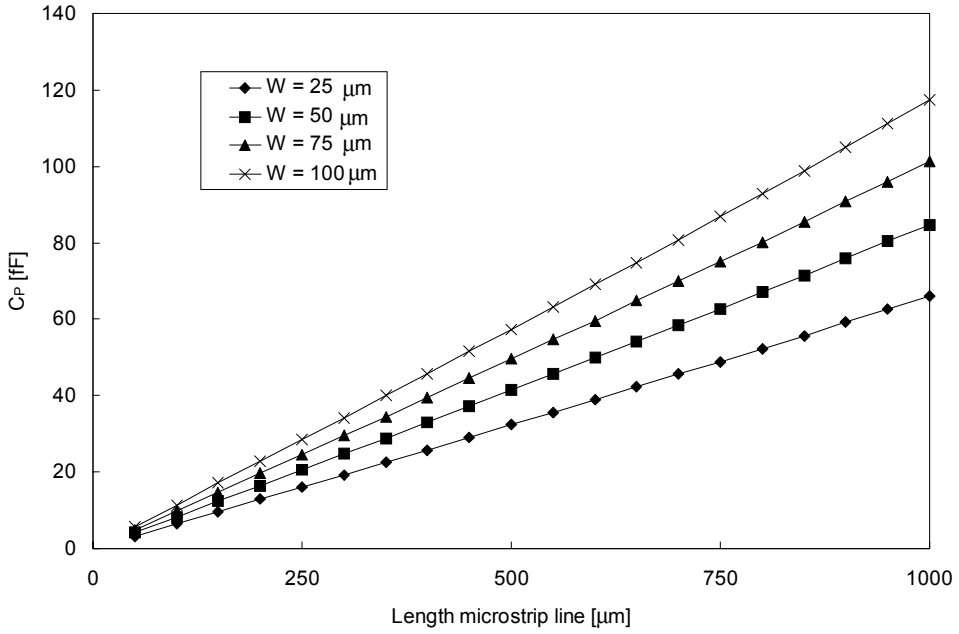

Figure 4.23: Value of parasitic capacitance C_P [fF] of a microstrip line simulated in Libra for different line widths. The line widths are given in µm.

With the help of a microstrip line, with a length up to 1000 µm, an equivalent series inductance of maximal 0.8 nH can be realised.

4.3.5 Capacitor

The capacitor type that is used for the high-power amplifier designs is the MIM capacitor. The value of the capacitor can be modelled to first approximation with the help of equation (4.6), which is the standard equation for a parallel plate capacitor:

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d} \quad . \tag{4.6}$$

At microwave frequencies, it is also necessary to consider the effect of the length of the transmission line present in the capacitor. A comparison of the modelling of a series capacitor, with and without considering the electrical length of the transmission line present in the capacitor with the measurement results, is shown in figure 4.24.

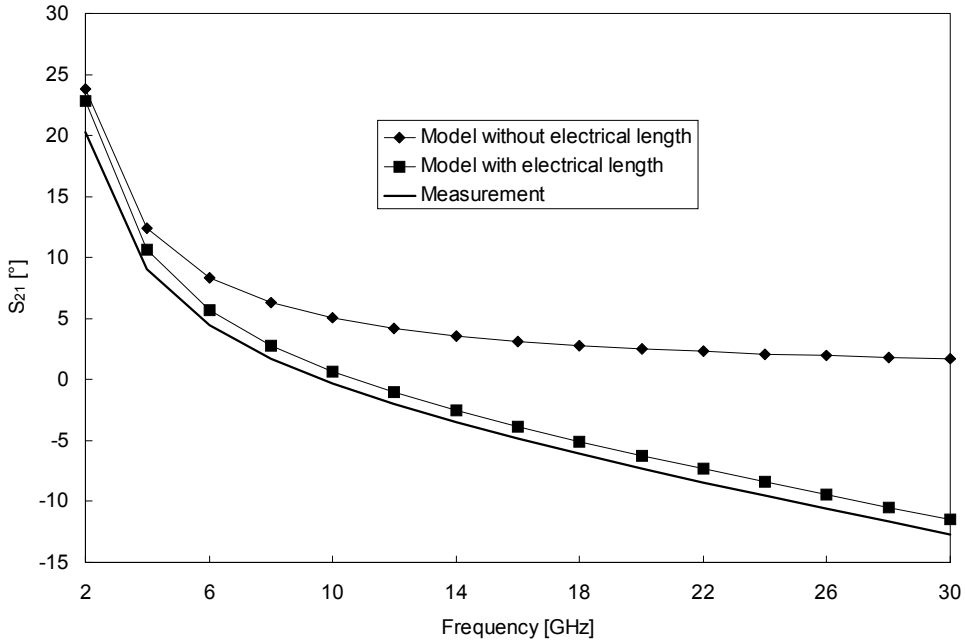

Figure 4.24: Effect of modelling series capacitor (1.8 pF) with and without electrical length of the transmission line present in the capacitor.

The depicted results show a good agreement between the simulations with electrical length and the measured capacitor results. Not considering the length of the capacitor will result in an equivalent capacitance value that is too high. This can be seen from equation (4.7) where the equivalent capacitance is given as a function of both the series capacitance and the series inductance:

$$C_{EQUI} = \frac{C_S}{1 - \omega^2 \cdot L_S \cdot C_S}. \tag{4.7}$$

The equivalent circuit of a series capacitor is shown in figure 4.25. In appendix A.8, equations are given for the calculation of the component values of this equivalent circuit. The use of these equations and the way in which to deal with the parasitic components will be discussed in more detail in chapter 6. The results depicted in figure 4.24 demonstrate the validity of this model when compared with measurements.

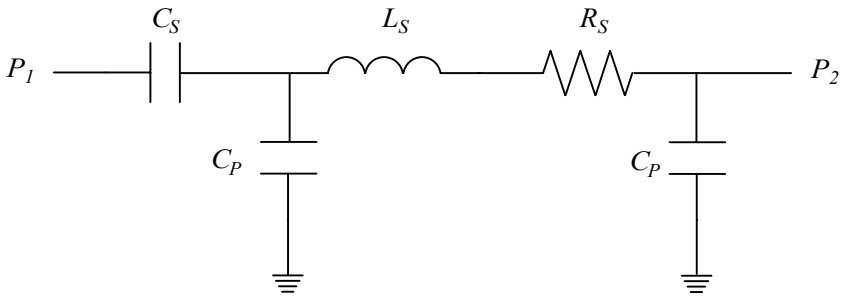

Figure 4.25: Equivalent circuit of a series MIM capacitor.

An electromagnetic field simulator like Momentum [4.18] can also be used to simulate a MIM capacitor. In this section, an application is shown of such electromagnetic field simulation of an MIM capacitor.

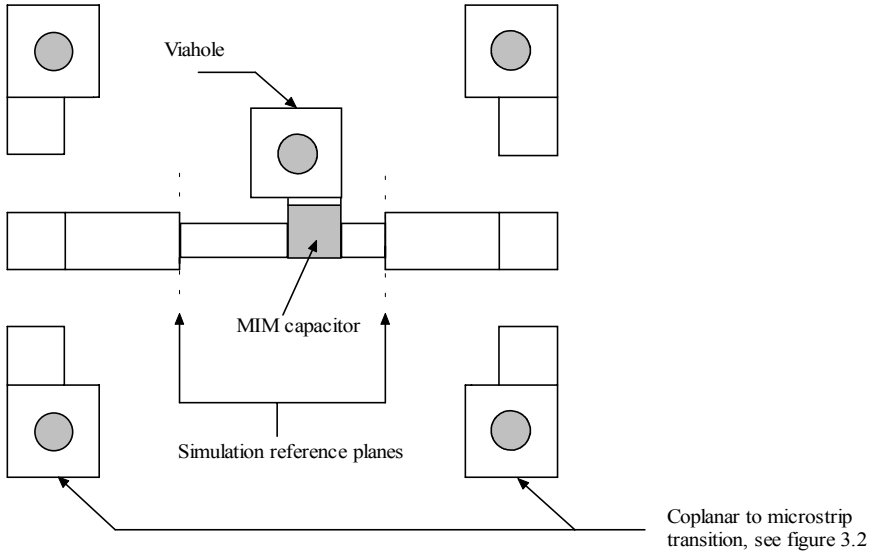

Figure 4.26: Topview of parallel capacitor integrated in microstrip lines test structure.

In figure 4.26 a test structure of a parallel MIM capacitor integrated in a microstrip line is shown. This structure is used many times in the discussed high-power amplifier designs at the input of the transistors. The parallel capacitor is used to perform a first interstage matching step, see chapter 6 for a more detailed discussion regarding matching networks. The capacitor is integrated in the microstrip line to save occupied chip area and to reduce the effect of the parasitic series inductor. The microstrip lines are connected to the top of the capacitor and the viahole is connected to the bottom plate of the capacitor. Consequently, the MIM capacitor becomes a three-port structure of which no model was available.

To circumvent this problem electromagnetic field simulations were used to model the three-port MIM capacitor. With the help of these simulations, the model that is shown between the dotted lines in figure 4.27 is determined. This model consists of a T-junction with at its third port a series capacitor and series microstrip line. For the model of the T-junction, the one that is discussed in section 4.3.3.3 was used. The model discussed in appendix A.8 was used for the capacitor. For the microstrip lines, the Libra model was used. Finally, the viahole model is the one that is discussed in section 4.3.7. A comparison between the measurement and simulation results at the reference planes indicated in figure 4.26 is shown in figure 4.28.

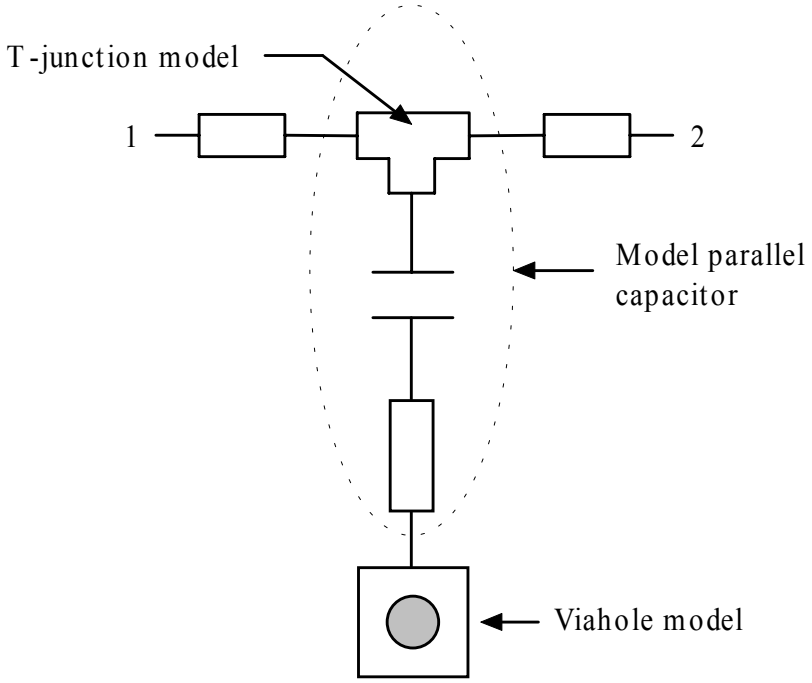

Figure 4.27: Model integrated parallel capacitor.

These results demonstrate an excellent agreement between measurement and simulation results. In addition, the validity of the model of a parallel capacitor found with the help of electromagnetic field simulations is proven. The depicted results also demonstrate the validity of the other used component models, like T-junction, microstrip lines and viahole, as were discussed in this chapter.

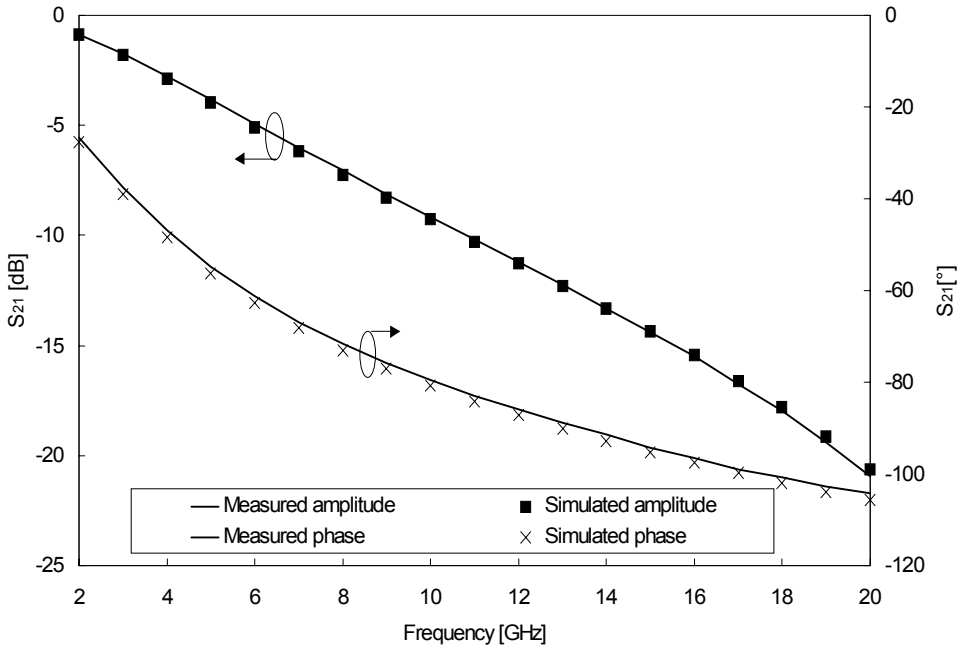

Figure 4.28: Comparison between measured (solid lines) and simulated (markers) results of parallel capacitor embedded in microstrip lines, see figure 4.26 and figure 4.27.

4.3.6 Resistor

The resistor model used in this thesis is depicted in figure 4.29. The model topology is very similar to the one that is used for the inductor and capacitor.

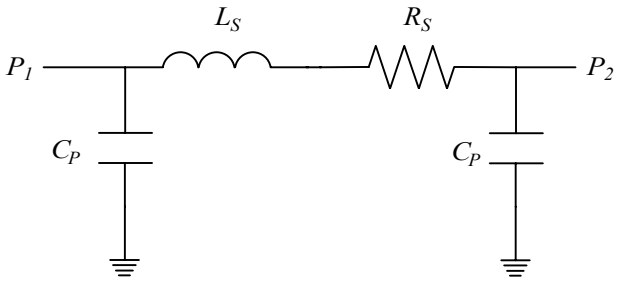

Figure 4.29: Resistor model.

The resistance R_S can be calculated with the help of the following equation:

$$R_S = R_{SHEET} \cdot \frac{L}{W} + 2 \cdot \frac{R_{CONTACT}}{W} . \tag{4.8}$$

The series resistance is a function of the sheet resistance R_{SHEET}, the contact resistance $R_{CONTACT}$, and the width W and length L of the resistor. In appendix A.8, the equations for L_S and C_P can be found. They are identical to the ones used for the capacitor. Use of the model depicted in figure 4.29 results in accurate simulation results as can be seen from the results depicted in figure 4.30. From these results can also be concluded that at microwave frequencies it is not acceptable to neglect the influence of the parasitic inductance L_S. Different approaches that yield similar results are the use of the Thin Film Resistor (TFR) model available in Libra [4.1] or a combination of the series resistance R_S and a microstrip line that has a length L and a width W.

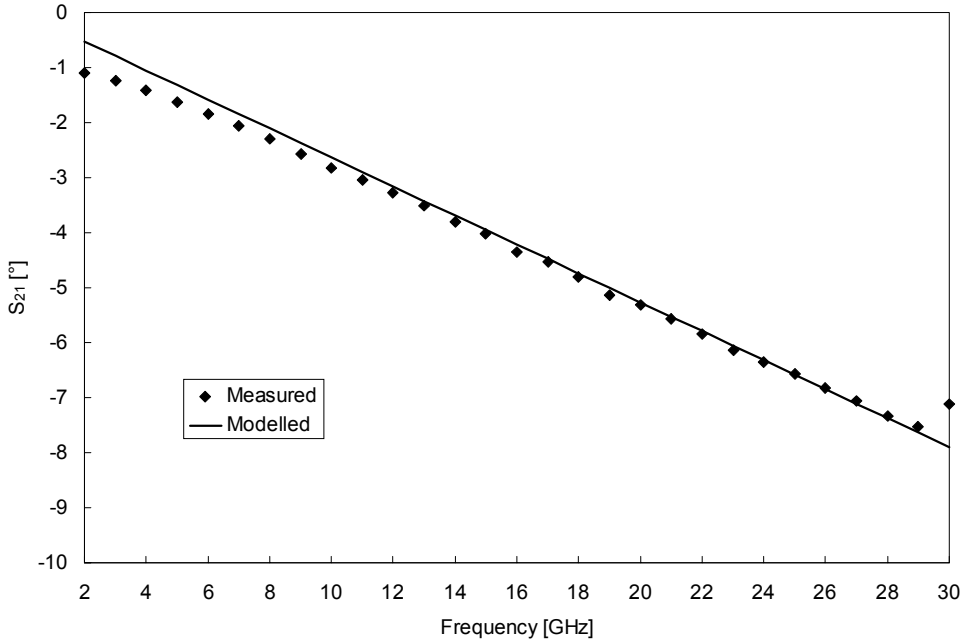

Figure 4.30: Comparison between the measured and simulated phase of the S_{21} of a 120 Ω resistor. This resistor has a length of 88 μm and a width of 38 μm.

4.3.7 Viahole

The connections to the ground plane at the backside of the wafer are made with the help of viaholes, see also chapter 2. A viahole model is determined for the two-port configuration depicted in figure 4.31. This viahole configuration and the one-port case are among the most encountered configurations in high-power amplifier designs. The equivalent circuit of

the determined viahole model is depicted in figure 4.32. The viahole forms a cone to the ground plane, see figure 2.21. This cone has a diameter of 50 µm at the top of the substrate. The metal top plate covering the viahole has a size of 150 x 150 μm^2. It is assumed that the bottom side of the cone has a diameter of 150 µm.

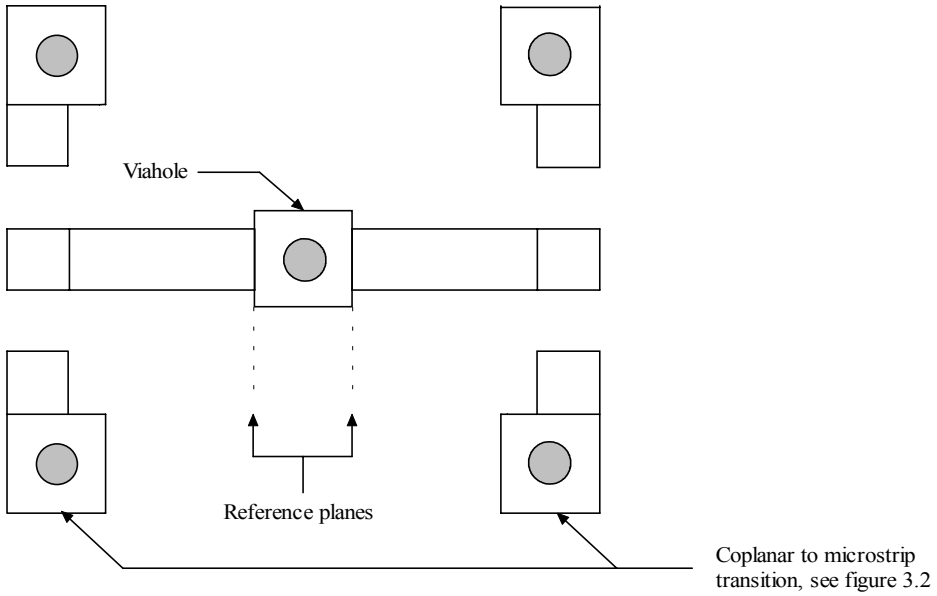

Figure 4.31: Topview of a two-port viahole test structure.

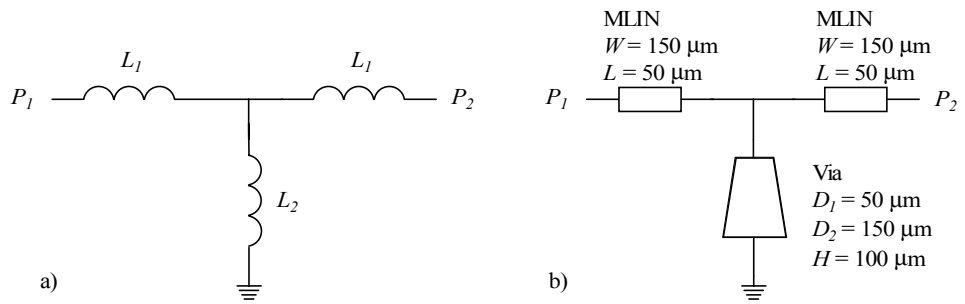

Figure 4.32: Two-port equivalent circuit viahole model, a) model extracted from measurements, b) based on Libra models.

The two-port viahole structure with ports connected in opposite directions is often encountered in structures where FETs have been placed in parallel, see for instance the output stage in section 6.3.2.

The values for the model components can directly be determined from the measured two-port S-parameters that have been converted to Z-parameters, see the following equations:

$$L_1 = \frac{\mathrm{Im}(Z_{11} - Z_{12})}{\omega}, \tag{4.9}$$

$$L_2 = \frac{\mathrm{Im}(Z_{12})}{\omega}. \tag{4.10}$$

In figure 4.33, the values of the viahole model parameters obtained from measurements, electromagnetic field simulations and simulation with the components available in Libra are shown.

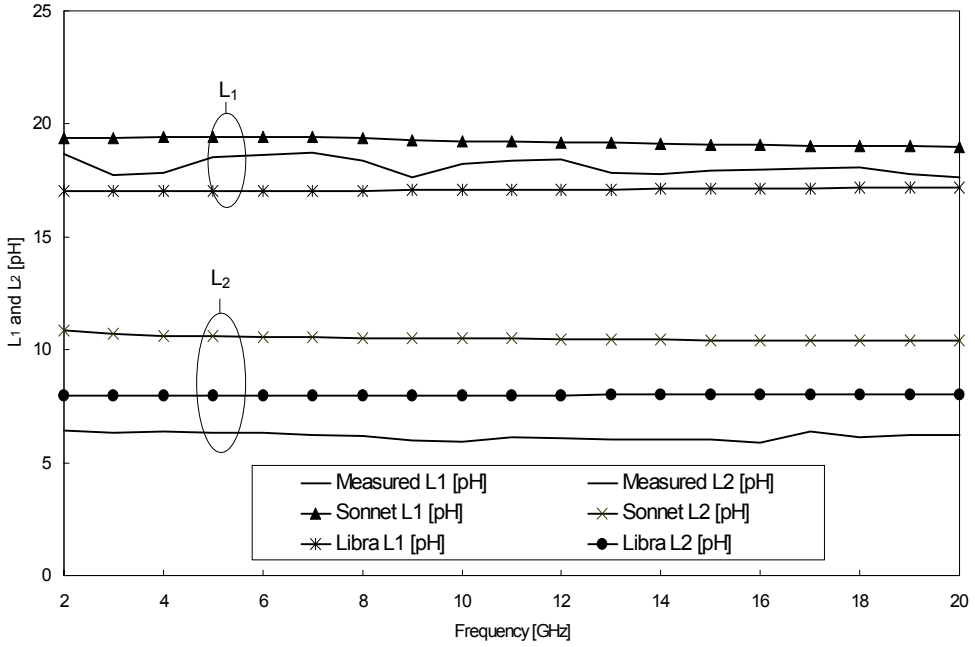

Figure 4.33: Two-port viahole model parameters extracted as a function of frequency from measurements, electromagnetic field simulations [4.26] and Libra simulations. Measurement results are the averaged results of 14 samples measured on the same wafer. (Standard deviation on L_1 is 2 pH and on L_2 is 0.4 pH)

The first observation that can be made is that the extracted model parameters are flat as a function of frequency, showing the validity of the chosen model topology. The simulation and measurement results of L_1 are close together. In the case of the Libra simulation, a microstrip line model (MLIN) is used to model L_1. This microstrip line has the same width

as the top plate of the viahole. The length of this line is equal to the length between the edge of the viahole top plate to the edge of the viahole itself. The agreement between the measured and simulated values of L_2 is less than the agreement between the measurement and simulation results of L_1, but is still considered good enough for design at X-band. The electromagnetic field simulation shows a relative large deviation with the measured results. This is due to the way the viahole itself is subdivided. The staircase structure used to approximate the cone is shown in figure 4.34. Experiments show that a subdivision of at least five steps is needed for L_2 to converge to a constant value. The values found from both simulation and measurement results are lower than the values quoted by the foundry.

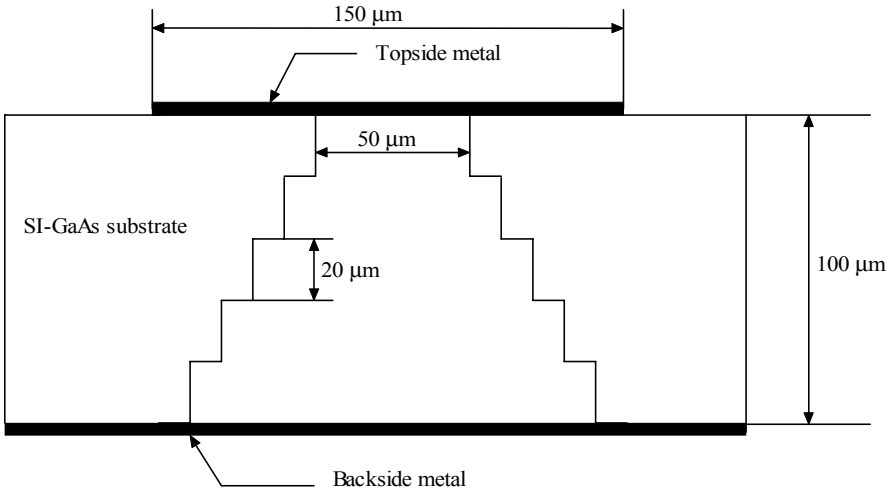

Figure 4.34: Cross section of viahole used for electromagnetic field simulations. For the given example, the substrate is divided in five layers.

4.4 Conclusions

In this chapter the equivalent circuit models of both the active and passive components used in the high-power amplifier designs are discussed.

The extraction and the performance of the large-signal transistor models used for both the MESFET and the HFET technology are discussed in this chapter. As large-signal models, the EEFET3 and the EEHEMT1 model from Agilent are used. It is shown that an excellent agreement for the DC IV curves is found. In addition, the large-signal performance under optimum load conditions is good enough for the discussed high-power designs. It was also discussed that there is a structural difference between the power added efficiency measured as a function of the source power and the simulated one. A correction factor of 0.85 for the simulated drain current was found to give good results under large-signal conditions. An

explanation for the drain current, which is predicted too high, is found in the way the dispersion model is implemented in the EEFET3 and EEHEMT1 model.

The microstrip line model as it is available in the used design software is shown to be accurate enough for design purposes at X-band. The same is not true for the available microstrip discontinuity models. For the 45° and the 90° microstrip bend, the symmetrical microstrip T-junction and the symmetrical microstrip crossing an improved scaleable electrical model is determined based on electromagnetic field simulations. It is shown when compared with measurements that these models give more accurate results than the models that are available in the RF design package Libra. The fact that these models are scaleable is of vital importance for the reduction of the simulation time necessary for the optimisation of the performance of the matching networks. Besides the before mentioned discontinuities also a model is extracted for a symmetrical Y-junction. This discontinuity model is not available in the design software used. In addition, the Y-junction model turns out to be in good agreement with the measurement results.

Inductors in the discussed high-power amplifier designs are realised with the help of microstrip lines. Based on the microstrip line model available in Libra a scalable inductor model is extracted. This model is a function of both the width and the length of the microstrip line. The usage of this model is discussed in more detail in chapter 6.

For the MIM capacitors available in both discussed technologies, an electrical model is extracted. It is shown that especially the electrical length of the capacitor can no longer be neglected at X-band. For the components of the capacitor model scaleable equations are determined. These equations are derived from simulations with the available microstrip line model. Again, as it was the case for the inductor, the electrical performance of a microstrip line is approximated with the help of a pi-network. This pi-network consists of a series resistor and inductor and at the input and the output a capacitor to ground. In this chapter, it is also shown that simulation of capacitor structures with the help of an electromagnetic field simulator is possible and necessary. These MIM capacitor simulations result in an improved insight in the modelling of such structures and in a more compact design of the matching networks.

A resistor can also adequately be modelled with the help of a pi-network. This pi-network consists of a series resistor, a series inductor, and two equal parallel capacitors to ground.

A model for a two-port viahole structure is shown based on measurements and electromagnetic field simulations. There is a good agreement between both if the substrate is subdivided in five or more sections for the electromagnetic field simulation.

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5. High-power amplifier topology and transistor cell size

5.1 Introduction

In the previous chapters, the available on-chip components, their limitations and models and the way in which they are characterised, were discussed. In this and the following chapter, the high-power amplifier design with all its aspects will be discussed. The power amplifier design flow, which is followed, is depicted in figure 5.1. The first part of the design flow namely the determination of the amplifier topology, the selection of the unit transistor cell size, the operating class with the load impedance, and the reliability and stability enhancement measures will be discussed in this chapter. The design of the matching networks, the overall power amplifier simulation and optimisation and the stability analysis of the complete high-power amplifier will be discussed in the next chapter.

As first step in the design flow, the topology of the power amplifier will be determined. The number of transistors used in parallel in the output stage, also called unit transistor cells, is determined with the help of the expected output power density of the transistors and the specified output power of the amplifier. A first estimation regarding the output power density of the transistors can be obtained from the knee voltage, breakdown voltage and maximum drain-source current of the transistors as it was already discussed in section 2.3.2. Based on the gain of the unit transistor cell used in the output stage of the power amplifier the size of the transistors in the stage preceding the output stage can be determined. These aspects and the way the figures of merit of the chosen transistor cells influence the performance of the complete high-power amplifier will be discussed in section 5.2.

The figures of merit of the unit transistor cell are influenced by the layout of the transistor namely, the width of the gate fingers, the number of gate fingers used in parallel, and the temperature of the gate fingers. All these aspects will be discussed in detail in section 5.3. The performance of the power amplifier is also strongly influenced by the selected operating class and the corresponding load impedance of the unit transistor cells. These aspects will be discussed in section 5.4.

Another aspect that needs careful attention is the reliability of the used unit transistor cells. The reliability of the transistors is influenced by the maximum gate finger temperature, as will be discussed in section 5.3. The reliability is also influenced by electron migration of the gate finger metal, which is caused by the large gate currents that can flow under non-linear operating conditions of the high-power amplifier. The use of a series gate resistor to prevent the occurrence of large gate currents and its effect on both output power and power added efficiency of the unit transistor cell, will be discussed in section 5.5. Before the design of the matching networks can start the stability of the used unit transistor cells must be analysed and if necessary be improved.

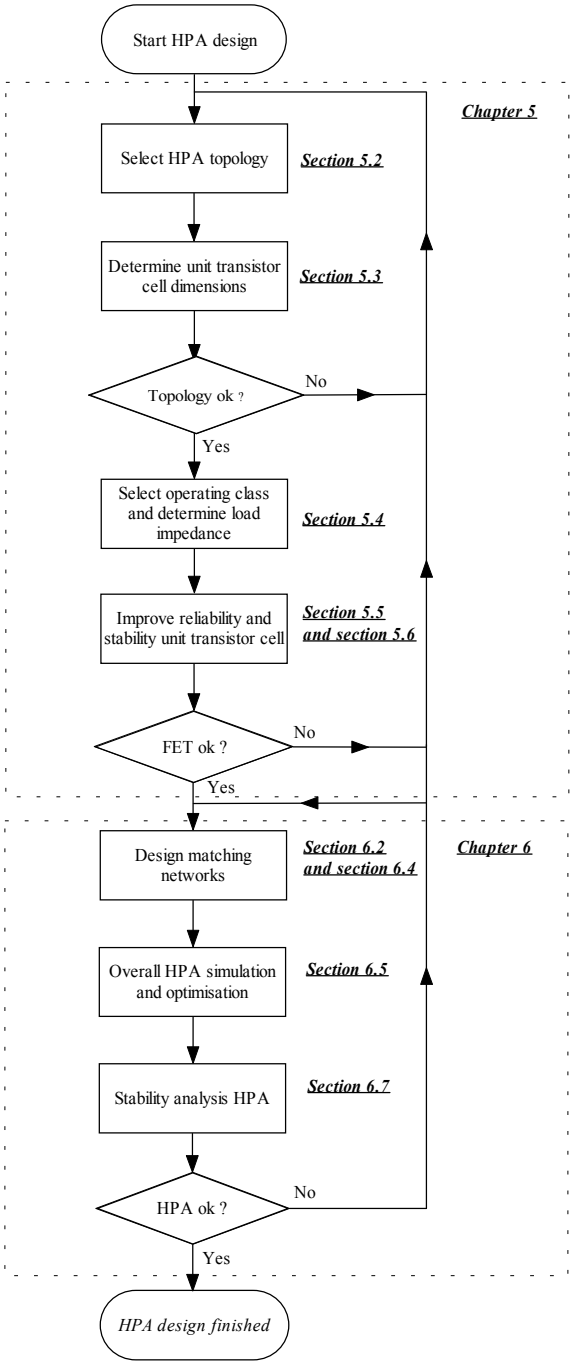

Figure 5.1: High-power amplifier design flow that is discussed in chapter 5 and 6.

The stability analysis of a transistor and stability improvement networks are discussed in section 5.6. Finally, in section 5.7 an overview is given of the dimensions, bias point, load impedance, the stability analysis and size of the unit transistor cells, used in the amplifiers discussed in chapter 7 of this thesis.

5.2 Amplifier topology

The first step in designing a high-power amplifier is the selection of the amplifier topology and the dimensions of the unit transistor cell. Factors that influence the dimensions of the unit transistor cell are discussed in detail in section 5.3. A number of transistors must be used in parallel because there is a limit to the maximum dimensions of the transistor, i.e. number of gate fingers and unit gate width. The available technology and the amount of output power required determine the number of transistors that must be used in parallel. For the amplifiers discussed in this thesis 2^n (n=1,2,3,…) transistors in parallel are used. This helps to avoid odd-mode oscillations [5.1] and the matching networks are kept as symmetrical as possible from both an electrical and a layout point of view. This symmetry is not easy to achieve when an odd number of transistors are used in parallel. For the amplifiers discussed in this thesis most of the time eight transistors in parallel have been used.

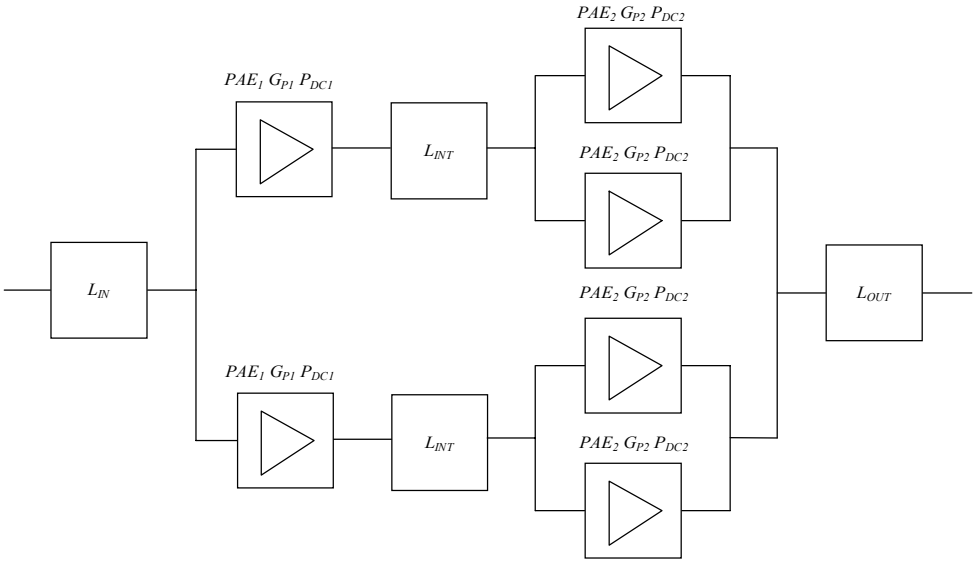

Figure 5.2: Block diagram of a two-stage high-power amplifier. Indicated are also the relevant figures of merit of the transistors and the losses of the matching networks.

The influence of the selected unit transistor cell on the overall high-power amplifier performance is considerable as will be discussed in the remainder of this section. The

discussion is based on the simplified block diagram of a two-stage high-power amplifier, which is shown in figure 5.2. In this figure, L_{IN}, L_{INT} and L_{OUT} represent the losses of respectively the input, the interstage and the output-matching networks. A two-stage example is shown here because all important conclusions regarding the high-power topology can be drawn from this case. It is easy to extend the results obtained to amplifiers having three or more stages. The transistors are characterised by their figures of merit, see also chapter 2. The relevant figures of merit for this discussion are the output power (P_{OUT}), the power added efficiency (PAE), the power gain (G_P) and the dissipated DC power (P_{DC}) of each transistor.

As already mentioned before the number of transistors used in the output stage is determined by the amplifier output power required and the output power that is available from a unit transistor cell. The latter factor is technology and layout dependent as will be discussed in section 5.3 and section 5.4. The required output power of the transistors used in the output stage of the amplifier can be calculated with the following equation:

$$P_{OUT\_FET2} \geq \frac{P_{OUT\_HPA}}{N_{FET} \cdot L_{OUT}} \cdot C_{POUT} \cdot C_{TEMP} \,. \tag{5.1}$$

In this equation N_{FET} is the number of transistors used in parallel, P_{OUT_HPA} the output power required of the amplifier, P_{OUT_FET2} the output power of the second stage transistor and L_{OUT} the loss of the output-matching network. Typical values for the loss of the output-matching network are 0.5 – 1.0 dB. Besides these obvious factors, also the output power variation of the transistors C_{POUT} caused by process variations should be taken into account. Measurements have shown that for both discussed technologies the worst case output power variation is ± 0.5 dB. In addition, the variation of the output power of a transistor as a function of temperature C_{TEMP} should be taken into account. The variation of the output power as a function of temperature is discussed in section 5.3. The output power is reduced when the temperature increases. Therefore, for the calculation of the number of transistors used in parallel, the highest specified temperature should be used.

The size of the first stage transistors is determined by the number of output stage transistors used in parallel, the expected losses of the interstage-matching network and the power gain of the output stage transistors. The output power required for the first stage transistors P_{OUT_FET1} can be calculated with the following equation:

$$P_{OUT\_FET1} \geq \frac{N_{FET} \cdot P_{OUT\_FET2}}{G_{P2} \cdot L_{INT}} \cdot C_{POUT} \cdot C_{TEMP} . C_{COMP} \,. \tag{5.2}$$

In this equation, N_{FET} is the number of output stage transistors that are combined in the interstage-matching network. For the amplifiers discussed in this thesis most of the time two transistors are combined. This will result in a more compact layout of the interstage-matching networks, see chapter 6, and therefore, the chip size of the complete power amplifier is reduced. Other factors that must be taken into account are the power gain of the output stage transistors G_{P2} and the loss of the interstage-matching network L_{INT}. Similar to

the output stage transistor also for this transistor extra margins for output power variation C_{POUT} and the temperature variations C_{TEMP} must be taken into account. Besides these factors an additional margin C_{COMP} must be taken into account to prevent the first stage transistors from going into compression before the second stage transistors. For the amplifiers discussed in this thesis an output power margin for the first stage transistors of at least one dB is taken into account.

For the calculation of the total power added efficiency PAE_{TOT} of the amplifier, it is convenient to assume that the losses in each branch of the matching networks are equal. In addition, the power added efficiencies of the individual transistors in each amplifier stage are considered equal. With the help of equation (5.3), the overall power added efficiency of a two-stage high-power amplifier can be calculated. This equation is valid unless there are differences in the branch losses or in the power added efficiencies of the transistors. Then the worst-case branch loss of the matching networks and power added efficiency of the transistors can be used to derive the worst case power added efficiency of the high-power amplifier. The derivation of this equation is given in appendix B:

$$PAE_{TOT} = \frac{PAE_1 \cdot PAE_2 \cdot (L_{IN} \cdot L_{INT} \cdot L_{OUT} \cdot G_{P1} \cdot G_{P2} - 1)}{PAE_1 \cdot G_{P1} \cdot L_{IN} \cdot L_{INT} \cdot (G_{P2} - 1) + PAE_2 \cdot L_{IN} \cdot (G_{P1} - 1)}. \tag{5.3}$$

In this equation PAE_1 is the power added efficiency of the first-stage transistors that have a power gain G_{P1} and PAE_2 the power added efficiency of the second-stage transistors that have a power gain G_{P2}. For the case where $G_{P2} >> 1$ equation (5.3) reduces to:

$$PAE_{TOT} = PAE_2 \cdot L_{OUT}. \tag{5.4}$$

The effect of the power added efficiency of the input and output stage transistors on the overall power added efficiency of the high-power amplifier is shown in figure 5.3. The numbers that are used are typical for a 5-Watt high-power amplifier developed in the MESFET process. The power added efficiency of the second stage transistors is close to 55%. Therefore, an overall power added efficiency of the complete amplifier between 30 and 40% can be expected. This estimation is in good agreement with the measured power added efficiency as reported in [5.2]. These results demonstrate the validity of the approach used to estimate the overall power added efficiency of a complete amplifier based on the losses of the matching networks and the power gain and power added efficiency of the transistors. A close inspection of equation (5.3) reveals that for the overall high-power amplifier performance it is of vital importance that:

1. The loss of the output-matching network L_{OUT} should be as low as possible, see also equation (5.4).
2. The gain G_{P2} and the power added efficiency PAE_2 of the last stage transistors should be as high as possible. From this point of view, it is beneficial to use the HFET instead of the MESFET technology, see chapter 2, because this technology has a higher power gain.

3. The power added efficiency and gain (PAE_1 and G_{P1}) of the first stage transistors and the losses of the input and interstage-matching networks (L_{IN} and L_{INT}) can not be neglected.

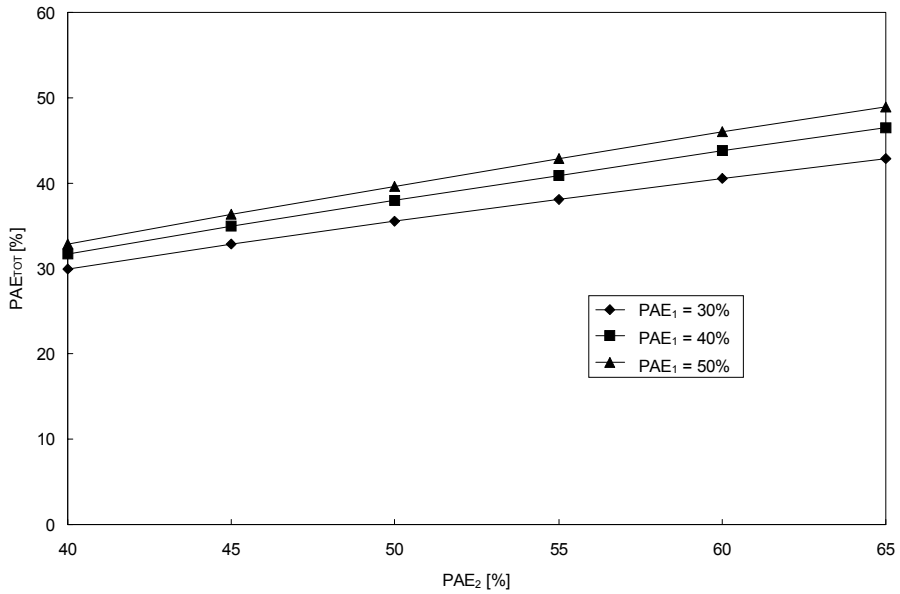

Figure 5.3: Power added efficiency calculation results of two-stage high-power amplifier. For this calculation the following settings are used: G_{P1} = 10 dB, G_{P2} = 8.5 dB, L_{IN} = 1.5 dB, L_{INT} = 1.5 dB and L_{OUT} = 0.7 dB.

5.3 Transistor size and layout

5.3.1 Introduction

The output power required for a high-power amplifier is realised by designing a number of transistors in parallel. For a given technology and a chosen number of transistors in parallel, the total gate width of the transistor is determined. After the total gate width of the transistor is known it is necessary to decide what kind of transistor layout will be used, see section 2.3.4. For the high-power amplifiers discussed in this thesis both transistors with an interdigitated and a fishbone layout have been used. After the layout of the transistor is selected, it is time to choose the width of one gate finger. When this width is known also the number of gate fingers is selected. An additional degree of freedom is the spacing used between the gate fingers. A reduction of this spacing results in a reduction of the size of the transistor layout but also in an increase of the maximum gate finger temperature and as a

result in a decrease of the reliability of the transistor. Therefore, there is a minimal value for the gate-to-gate spacing from a thermal point of view. This and all the other mentioned factors are the subjects discussed in the following sections.

For different output powers of the amplifier, examples of the calculated total gate width of unit transistor cell sizes are listed in table 5.1. For these calculations, equation (5.1) is used. Eight transistors in parallel are assumed, which is the case for almost all amplifiers discussed in this thesis, and an output-matching loss of one dB is assumed. For this calculation, both the factors C_{POUT} and C_{TEMP} have been set to one. For this calculation, the following output power densities are used: MESFET 0.6 W/mm and HFET 0.7 W/mm. These output power densities are more realistic than the one's based on the DC parameters mentioned in chapter 2, as will be shown in section 5.7.

The results listed in table 5.1 give an idea for the discussion in the next sections regarding the expected transistor sizes.

Table 5.1: Calculated gate width transistors for different amplifier output powers. Eight transistors in parallel are assumed with one dB of loss in the output-matching network and $C_{POUT} = C_{TEMP} = 1$.

$P_{OUT\ HPA}$ [W]	MESFET size [µm]	HFET size [µm]
2.5	656	562
5.0	1311	1124
7.5	1967	1686
10.0	2623	2248

5.3.2 Influence of unit gate width on transistor gain

The parameter that can be changed the easiest in the layout of a transistor is the unit gate width. The width of the gate finger is directly related with the power gain of the transistor. If the width of the gate finger increases the gain of the transistor will decrease because the attenuation and the phase shift of the signal along the gate finger will increase. An impression regarding the power gain reduction G_{PR} can be obtained with the help of the following equation [5.3]:

$$G_{PR} = \frac{1}{W_U} \cdot \left[\frac{2\alpha^2 + \beta^2}{4\alpha \cdot \left(\alpha^2 + \beta^2\right)} - \frac{e^{-2\alpha W_U}}{4\alpha} - \frac{e^{-2\alpha W_U}}{4 \cdot \left(\alpha^2 + \beta^2\right)} \cdot \left(\alpha \cdot \cos 2\beta W_U - \beta \cdot \sin 2\beta W_U\right) \right]. \tag{5.5}$$

The α and β in equation (5.5) represent the attenuation and phase shift of the transmission line formed by the gate finger and the active region underneath the gate finger, see figure 5.4, W_U is the unit gate width.

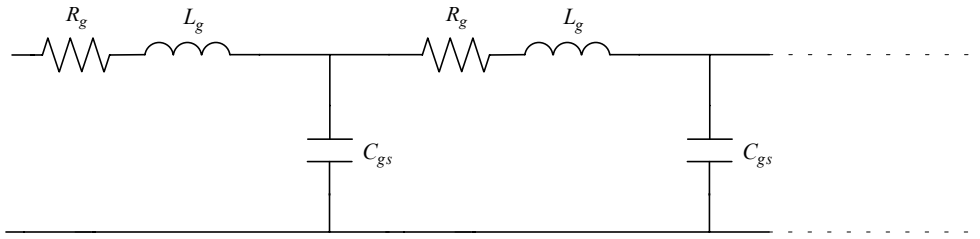

Figure 5.4: Model of transmission line formed by the gate finger and the active region underneath it.

The following equations are derived for α and β based on the equivalent circuit shown in figure 5.4:

$$\alpha = \omega \cdot C_{gs} \cdot \sqrt{-\frac{L_g}{2 \cdot C_{gs}} + \frac{1}{2} \cdot \sqrt{\left(\frac{L_g}{C_{gs}}\right)^2 + \left(\frac{R_g}{\omega \cdot C_{gs}}\right)^2}}\ , \tag{5.6}$$

$$\beta = \omega \cdot C_{gs} \cdot \sqrt{\frac{L_g}{2 \cdot C_{gs}} + \frac{1}{2} \cdot \sqrt{\left(\frac{L_g}{C_{gs}}\right)^2 + \left(\frac{R_g}{\omega \cdot C_{gs}}\right)^2}}\ . \tag{5.7}$$

These equations show that the gate resistance R_g should be as low as possible. Then the attenuation α becomes zero and the phase shift β is minimal. The value of R_g increases when the gate length decreases. To lower R_g for small gate lengths and to increase the gate current density that is allowed to flow through a gate finger, mushroom or T-gates have been used. When R_G is zero, equation (5.5) reduces to:

$$G_{PR} = \frac{1}{2 \cdot W_U} \cdot \left[W_U + \frac{\sin 2\beta W_U}{2 \cdot \beta} \right]. \tag{5.8}$$

The results of the application of equations (5.5) and (5.8) for some typical DIOM20HP MESFET values are depicted in figure 5.5. The propagation constant is bias dependent because C_{gs} is bias dependent as it was discussed in chapter 4.2. The value for C_{gs} that is used in before mentioned calculation was determined at V_{DS} = 9 V and V_{GS} = -1.25 V. The results depicted in figure 5.5 show that the gain of a transistor is reduced when the unit gate width is increased or the frequency is increased. As maximum gain degradation, a value of one dB is considered acceptable. Consequently, at X-band a maximum unit gate width of approximately 125 µm can be used. For this reason the amplifiers designed with an interdigitated transistor layout used unit gate widths of 125 µm. In addition, it can be

concluded from figure 5.5 that the phase shift is the dominant factor in the power gain reduction.

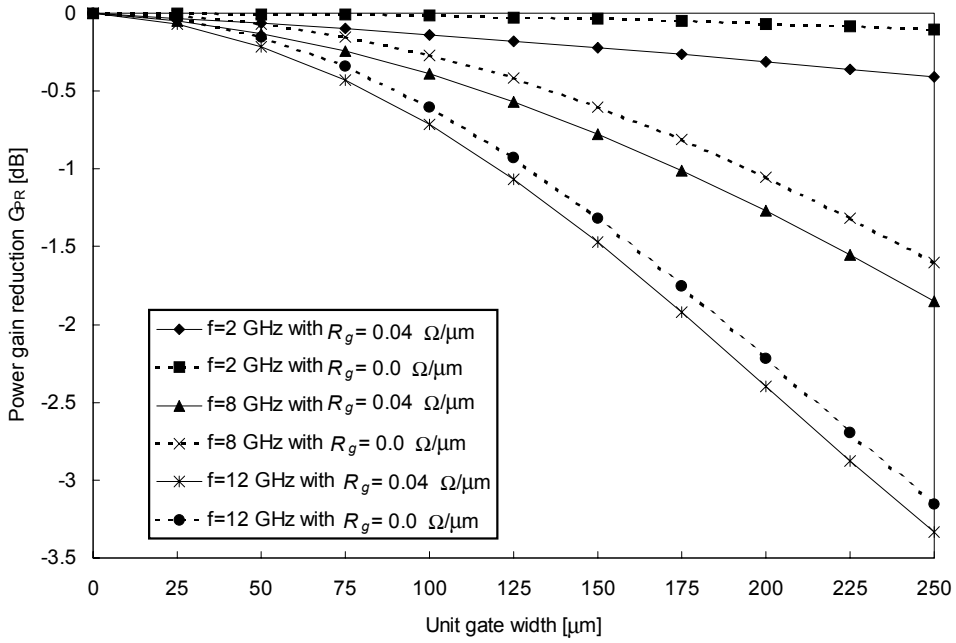

Figure 5.5: Calculated power gain reduction based on equations (5.5) and (5.8). For this calculation the following input values have been used: L_g = 6 pH/µm, R_g = 0.04 Ω/µm, C_{gs} = 1.235 fF/µm, R_g = 0.0 Ω/µm (dotted lines) and R_g = 0.04 Ω/µm (solid lines).

For the transistors that have a fishbone layout the situation is more complex because the gate feed structure is different and the spacing between the gate fingers is smaller. Consequently, the gate fingers become hotter and an additional gain reduction will occur when the unit gate width is increased. In figure 5.6, the measured power gain reduction obtained for a matrix of fishbone MESFETs is shown. These results also show that the gain of a transistor is reduced as a function of the width of the gate finger. The depicted results show a large gain reduction as a function of the gate width. The reduction is more than the one that is predicted with the help of equation (5.5). This is because the real situation is much more complex than is described with equation (5.5). A better prediction of the gain reduction would be possible with the help of electromagnetic field simulations of the entire transistor layout, like the one described by Cidronali [5.4]. However, at the time the transistor size and layout was designed, no electromagnetic tools were available to perform such kind of simulations. Therefore, the selection of the transistor size and layout was done on an experimental basis. It is shown in figure 5.6, that the power gain will be reduced as the unit gate width increases. The output power on the other hand is more or less constant as a function of the unit gate width as long as the number of gate fingers is kept constant. This is because the drain and source connections have a much larger width and the capacitance to

ground is less. Consequently, the attenuation and phase shift is not an issue for the before mentioned unit gate widths. The effect of the number of gate fingers on both the gain and the output power of a transistor is discussed in more detail in the next section.

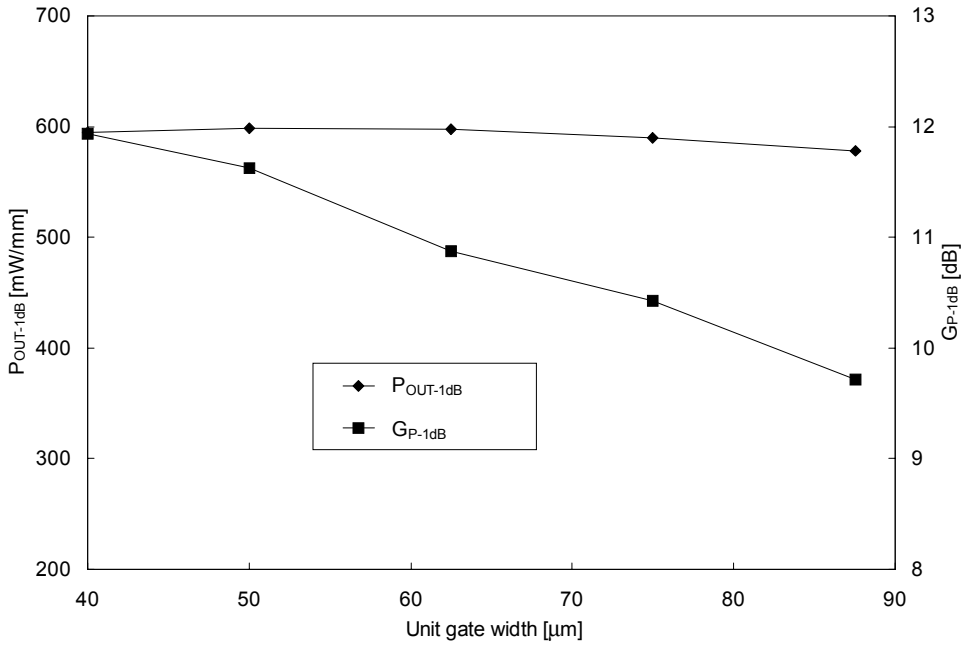

Figure 5.6: Measured 1dB compression output power and power gain at 8 GHz as a function of the unit gate width of fishbone MESFETs that have 16 gate fingers. Measured at V_{DS} = 9 V and V_{GS} = -1.25 V.

5.3.3 Number of gate fingers

Besides the unit gate width, also the number of gate fingers used in parallel is an important parameter. The influence of the number of gate fingers is also determined by the transistor layout. We have used, as already discussed in section 2.3.4, both interdigitated and fishbone types of transistor layouts for the power amplifiers discussed in this thesis.

For the interdigitated transistor layout the maximum number of gate fingers is determined by the maximum allowed phase shift to the outer gate fingers of the transistor. In literature [5.3] a value of one sixteenth of the wavelength is mentioned as an acceptable distance between the inner and the outer gate fingers, above this value the transistor no longer can be looked upon as a lumped element. Other factors that play a role are:

- The input impedance of the transistor, which decreases when the number of gate fingers is increased. As a result the matching losses will also increase, see chapter 6 for a more in depth discussion.
- The channel temperature is not uniformly divided over the gate fingers. Therefore, the gate fingers in the middle of the transistor will become hotter than at the outside. This is discussed in more detail in section 5.3.4.

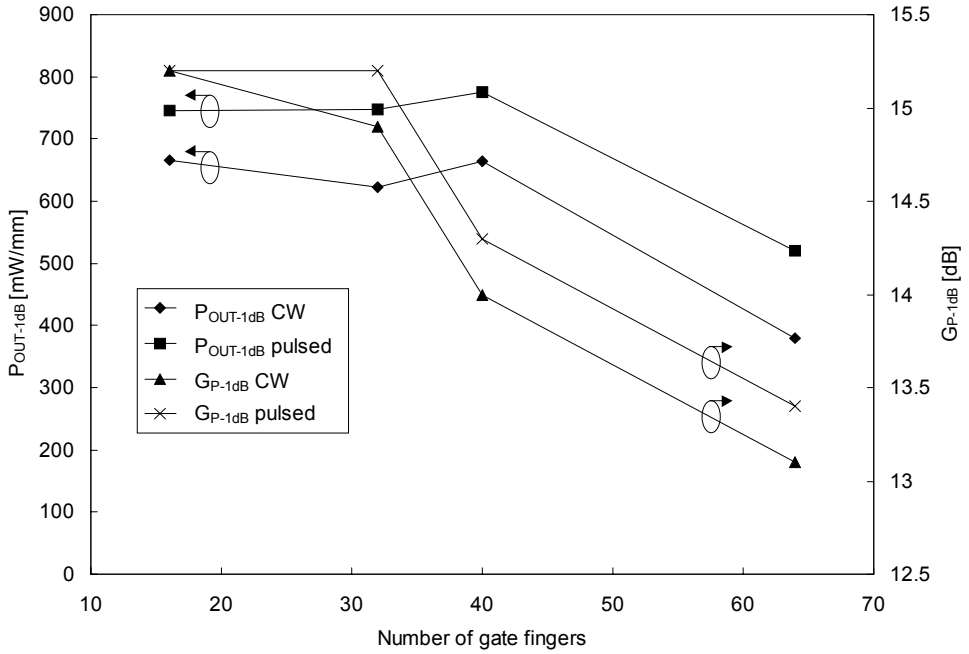

Figure 5.7: Influence of number of gate fingers of a HFET fishbone transistor layout on output power and power gain. The unit gate width of these transistors is 45 μm. Load-pull measurement performed at: V_{DS} = 8 V, V_{GS} = -0.4 V and f = 8 GHz. For the pulsed measurements a duty cycle of 10% and a pulse width of 10 μs are used.

When fishbone transistors are used similar problems occur. The only difference is the distance to the first gate fingers, which is longer than is the case for the interdigitated transistor layout. From this point of view, less gate fingers can be used in parallel with a fishbone transistor layout. The effect of the number of gate fingers has been investigated experimentally for both the MESFET and the HFET technology. Some typical results are depicted in figure 5.7 for the HFET technology.

The results as have been depicted in figure 5.7 show that both the output power and the gain decrease when the number of gate fingers is increased. From the depicted results can be concluded that the output power significantly decreases when more than 48 gate fingers are used in parallel.

Load-pull measurement results of a MESFET fishbone transistor matrix with a different number of gate fingers and unit gate widths are listed in table 5.2.

Table 5.2: Summary of CW load-pull measurement results of a MESFET fishbone matrix measured at f = 8 GHz, V_{DS} = 9 V and V_{GS} = -1.25 V.

FET	N_{GF}	W_U [µm]	P_{SAT} [mW/mm]	P_{OUT_1dB} [mW/mm]	G_{P_1dB} [dB]	$PAE_{\_1dB}$ [%]
1	32	48	586	512	12.4	54
2	32	67	578	510	11.3	56
3	40	50	596	538	12.1	54
4	32	94	612	574	10.6	56
5	48	63	570	539	11.0	57
6	60	48	469	424	10.6	48

The results listed show the same trends as observed before namely the saturated output power per total gate width is more or less constant and independent of the unit gate width until more than 48 gate fingers in parallel are used. The gain decreases for a constant number of gate fingers in parallel, see sample 1, 2 and 4, as the unit gate width increases. This is an extra confirmation of the behaviour observed in the previous section.

The fishbone topology, sizes of the feed network, gate-to-gate spacing etc. is the same for both the MESFET and HFET example discussed before. Four branches of gate fingers are used in parallel. This means that where e.g. 40 gate fingers are mentioned 10 gate fingers are used in parallel for each branch.

The output power decreases because the power of the gate fingers is no longer combined in phase, as it was the case when only the width of the gate fingers was varied. This out of phase summation of the output power is also caused by the travelling wave effect that is caused by both the drain and gate manifold. This effect can be minimised by putting the gate fingers as close together as possible. The effect of the gate-to-gate spacing on amplifier performance from a thermal and reliability point of view is the subject of the next section.

5.3.4 Thermal analysis transistor

A good estimate of the maximum gate finger temperature is of vital importance for the estimation of the reliability of the transistors. In addition, the output power and power gain of the transistors are reduced with increasing temperature. Most failure mechanisms exhibited by semiconductors are due to the diffusion of atoms. Higher temperatures accelerate this diffusion process. The relation between reaction rate *R* and temperature is given by the Arrhenius equation [5.5]:

$$R = C \cdot e^{\frac{-E_a}{k \cdot T}} . \tag{5.9}$$

In this equation C is a constant, k the Boltzmann constant, T the absolute temperature in [K], and E_a is the activation energy in [eV]. The activation energy is a measure how effectively a failure mechanism utilises thermal energy. The effect of temperature variations can be described with the help of the acceleration factor,

$$AF = e^{\left(\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_A}\right)\right)} . \tag{5.10}$$

In this equation T_0 is the actual operating temperature and T_A the accelerated temperature. The actual activation energies of the transistors used cannot be given here due to the non-disclosure agreements signed with the foundries. The maximum gate temperature that was considered acceptable by the foundries was approximately 125 °C. The acceleration factor can be used to calculate the reduction of the Mean Time To Failure when the temperature is changed.

For the thermal analysis of the power transistors the TXYZ30 program developed by Albers [5.6] is used. According to [5.6, 5.7] this program solves the heat-flow problem by expanding a series of basis functions satisfying the boundary conditions at the surface of the material. The following assumptions are made:

- The heat generators are rectangular plates at the surface of the chip.
- No heat loss from the top or sides of the chip.
- No heat loss in the electrical connections.
- The heat sink is considered ideal.

Heat transfer in power transistors is mainly due to heat conduction. The heat conduction equation that must be solved is given in (5.11):

$$\frac{\partial}{\partial x} \cdot \left(\kappa \cdot \frac{\partial T}{\partial x} \right) + \frac{\partial}{\partial y} \cdot \left(\kappa \cdot \frac{\partial T}{\partial y} \right) + \frac{\partial}{\partial z} \cdot \left(\kappa \cdot \frac{\partial T}{\partial z} \right) + g(x, y, z, t) = \rho \cdot c \cdot \frac{\partial T}{\partial t} . \tag{5.11}$$

In this equation, T is the temperature [K]. The thermal conductivity is κ [W/m.K], the specific heat is c [J/kg.K] and the material density is ρ [kg/m³]. The rate of the energy generation per unit volume is given by $g(x,y,z,t)$ [W/ m³]. Of these values, the thermal conductivity and the specific heat are strongly temperature dependent for GaAs. The temperature dependence of the thermal conductivity can be accounted for with the help of the Kirchhoff transformation [5.8, 5.9]. This transformation shifts the non-linearity from the heat-flow equation to the boundary conditions. Therefore, this transformation relates the "linear" temperature θ with the actual temperature T, see equation (5.12):

$$\theta = T_0 + \frac{1}{\kappa(T_0)} \cdot \int_{T_0}^{T} \kappa(T) \cdot dT \quad . \tag{5.12}$$

In this equation, T_0 is a reference temperature at which the thermal conductivity is determined. Substituting equation (5.12) in equation (5.11) and assuming CW operating conditions gives the linear heat equation that is solved in the TXYZ30 program:

$$\kappa(T_0) \cdot \left(\frac{\partial^2 \theta}{\partial x^2} + \frac{\partial^2 \theta}{\partial y^2} + \frac{\partial^2 \theta}{\partial z^2} \right) + g(x, y, z, t) = 0 \; . \tag{5.13}$$

In literature [5.10], it is shown that for RF power transistors operated in the CW mode it is sufficient to solve only the DC portion of the heat conduction. After this equation is solved, a linear temperature θ is available. The actual temperature can be calculated with the help of two Kirchhoff transformations as given in equation (5.12). The first one is used to relate the ambient temperature T_A to the reference temperature T_0. This transformation was removed for each calculation performed in this thesis by choosing $T_0 = T_A$. A second transformation is needed to relate the calculated temperature θ to the actual temperature T. This can be done analytically when the temperature dependence of the thermal conductivity is known. The following equation was used to account for the temperature dependency of the thermal conductivity:

$$\kappa(T) = \kappa(T_0) \cdot \left(\frac{T}{T_0} \right)^n \; . \tag{5.14}$$

For n different values can be found in literature [5.7]. We decided to use n = -1.25 for our calculations [5.11, 5.12]. With the help of equation (5.12) and equation (5.14), the following analytical equation is found for the actual temperature T:

$$T = T_0 \cdot \left(1 + \frac{(n+1) \cdot (\theta - T_0)}{T_0} \right)^{\frac{1}{1+n}} \; . \tag{5.15}$$

In this equation $(\theta - T_0)$ is the term that is available from the TXYZ30 program. For the calculations, it is necessary to define the area of the heat generators. These heat generators are considered rectangular. For the length, the unit gate width of the transistor is used. For the width, the situation is somewhat more complex. For recessed etched transistors according to Anholt [5.7] the heat is generated over an area that is smaller than the gate length. For planar transistors, this area is more spread out over the gate to drain distance. Therefore, it is difficult when the exact geometry of the transistor is not known to give an accurate estimate of the width of the heat region. Because this is the case for the transistors used, it was decided to use the gate length as the width of the heat region. The temperature that is predicted with the help of the TXYZ30 program is in general too high. The following

factors [5.12] contribute to a higher calculated thermal resistance when compared to the actual thermal resistance:

- The passivation layer covering the transistor acts as a heat spreader in upward direction.
- The electrical interconnections radiate temperature.
- The available viaholes will lower the thermal resistance.

This higher calculated resistance is no problem because only an estimation is needed for the maximum gate finger temperature. For the processes used, there will not be any reliability problems as long as the calculated temperature stays below 125 °C.

The temperature under pulsed conditions will be lower because the dissipated average power is less and therefore, at least the ambient temperature will be at a lower value than in the CW case. The temperature rise that occurs under a step response of the DC power can be calculated with the help of the following equation [5.13]:

$$T = T_A + P_{DC} \cdot \theta \cdot \left(1 - \frac{8}{\pi^2} \cdot \sum_{n=1,3,5,\ldots}^{\infty} \frac{e^{\frac{-t}{\tau_n}}}{n^2} \right). \tag{5.16}$$

For the thermal time constant τ_n in equation (5.16) the following equation is used [5.13]:

$$\tau_n = \left(\frac{2 \cdot h}{n \cdot \pi} \right)^2 \cdot \frac{1}{\alpha}. \tag{5.17}$$

In this equation, h is the height of the substrate, which is 100 µm for the amplifiers discussed in this thesis. For the thermal diffusivity α of GaAs, a value of 0.24 [cm^2/s] [5.3] at room temperature is used. With the help of equations (5.16) and (5.17), the thermal time constant of GaAs can be calculated. The thermal time constant is defined as the time where the temperature has reached 63.2% of its steady state value. With the numbers and equations mentioned before, a thermal time constant of 133 µs is found for 100 µm thick GaAs. In practice much lower time constants (< 1 µs) have been observed. A more accurate calculation of the thermal time constant of GaAs can be found in [5.14]. In this reference, the heat equations are solved in all three dimensions, where it is done in only one direction in [5.13]. Therefore, the results from [5.14] will more closely approximate the reality. Equations (5.16) and (5.17) have been given here anyway because they show that the thermal time constant is independent from the dissipated power P_{DC}, a result that is confirmed in [5.14]. From the results presented in [5.14], it can be concluded that the thermal time constant of GaAs is approximately 0.3 µs. Therefore, it can be concluded that for the pulse widths used in radar systems (typically > 10 µs) the gate fingers are already at their maximum temperature. The only difference then between CW and pulsed operation comes from the fact that in the latter case the dissipated power in the surrounding of the gate finger is lower. Therefore, the ambient temperature will be lower when adequate heat removal is present.

The calculated temperatures with the TXYZ30 program are compared with infrared measurements performed at TNO-FEL [5.15]. A comparison between the measured and calculated temperatures is shown in figure 5.8. These results show that the predicted maximum gate temperature compares well with the measured results. For the TNO-FEL measurement results an accuracy of 5° C was calculated.

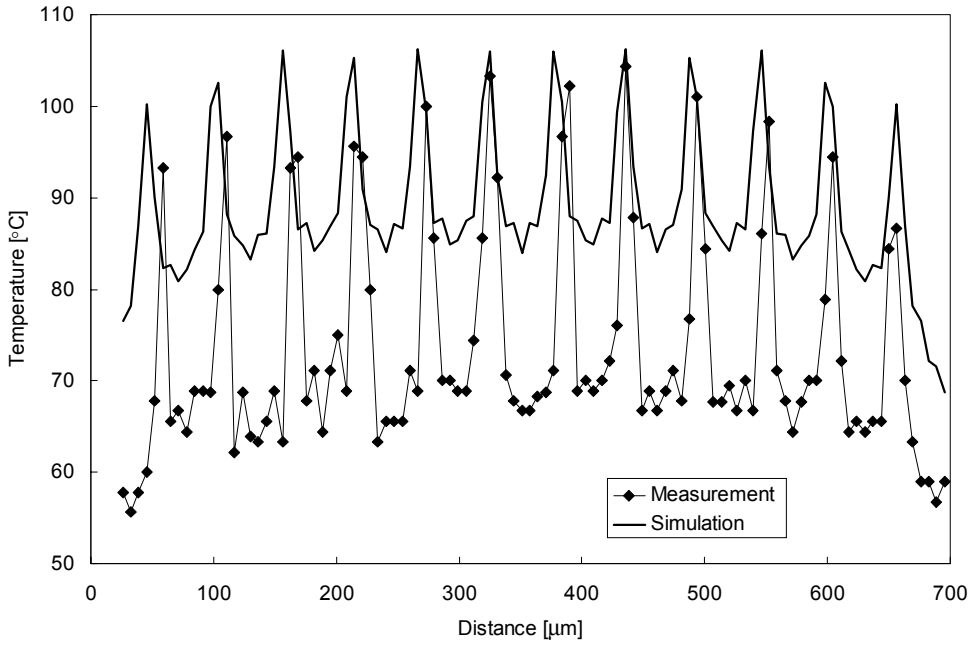

Figure 5.8: Comparison between measured [5.15] and calculated temperature as a function of the distance. The calculation is performed for a transistor that has 12 gate fingers with a width of 125 µm. The dissipated power is 1.37 W. Ambient temperature is 60 °C. The calculated results are shown in the middle of the gate finger width.

A second verification is a comparison made with the thermal calculations given by Marsetz [5.16, example 2]. These calculations have been performed as a function of both the dissipated power and the gate-to-gate spacing. The by Marsetz [5.16] calculated temperatures compare well with the measurement results. A comparison of the TXYZ30 simulation results with the results obtained by Marsetz is depicted in figure 5.9. The results show that:

- The gate-to-gate spacing has a strong influence on the gate temperature. The depicted results indicate that a spacing of approximately 30 µm is a minimum else the gate temperature becomes too high for higher ambient temperatures. (Maximum expected dissipated power is around 1 W/mm and T_A = 60 °C.)

- The temperature increases as the dissipated power increases. There is for a given maximum gate finger temperature and ambient temperature also a limit to the dissipated power.
- The results show that there is a reasonable agreement between measurement and simulations. These results show that the TXYZ30 program is accurate enough for our thermal calculations, which have only an indicative character anyway.

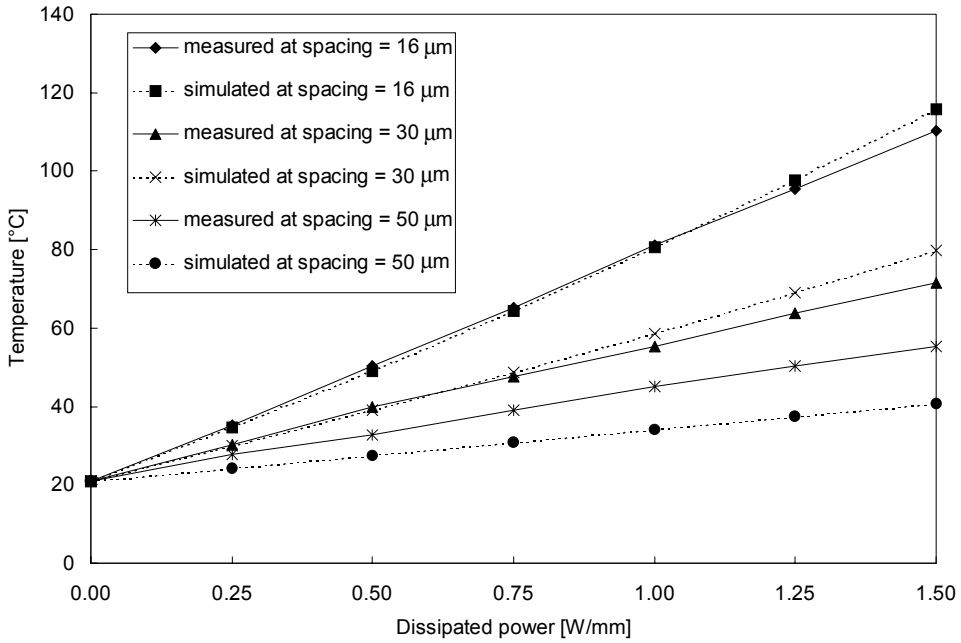

Figure 5.9: Comparison between measured [5.16, figure 2] and calculated temperature as a function of the dissipated power and the gate-to-gate spacing. The calculation is performed for a transistor that has 7 gate fingers with a width of 100 µm. Ambient temperature is 21 °C and thickness substrate is 630 µm.

The output power and power gain are reduced as the ambient temperature is increased, as can been seen from the measured results depicted in figure 5.10. This negative temperature dependency is an advantage that FETs have over bipolar transistors. In the bipolar transistor case, thermal runaway and destruction of the transistor when no counter measures for the existing positive thermal feedback are taken, is a well-known phenomenon. The MESFET results depicted in figure 5.10 show an output power variation of –0.006 dB/°C as a function of temperature. The power gain varies with –0.013 dB/°C. The output power and the power gain vary, for the given temperature interval, more or less linear as a function of temperature. The depicted temperature range is for the kind of application, where the discussed power amplifiers are designed for, the most important range.

If it is assumed that the temperature variation of the output power and power gain is mainly caused by the temperature dependency of the saturation velocity of the electrons, an estimation of the temperature dependency can be made with the help of the equations given by Nosal [5.17]. In appendix C, the calculation of the temperature dependency of a MESFET is given based on the physically based MESFET model of Ladbrooke [5.18]. From these results a power gain variation as a function of temperature of –0.014 dB/°C can be found for the 25 to 125 °C temperature range. For the output power variation, half of this value, -0.007 dB/°C, was found. The power gain variation calculated in appendix C and the measurement results as have been depicted in figure 5.10 are in good agreement with the results that have been summarised by Lardizabal et al [5.19]. They compared reference data from different sources. From these sources, an average gain variation of –0.015 dB/°C was found.

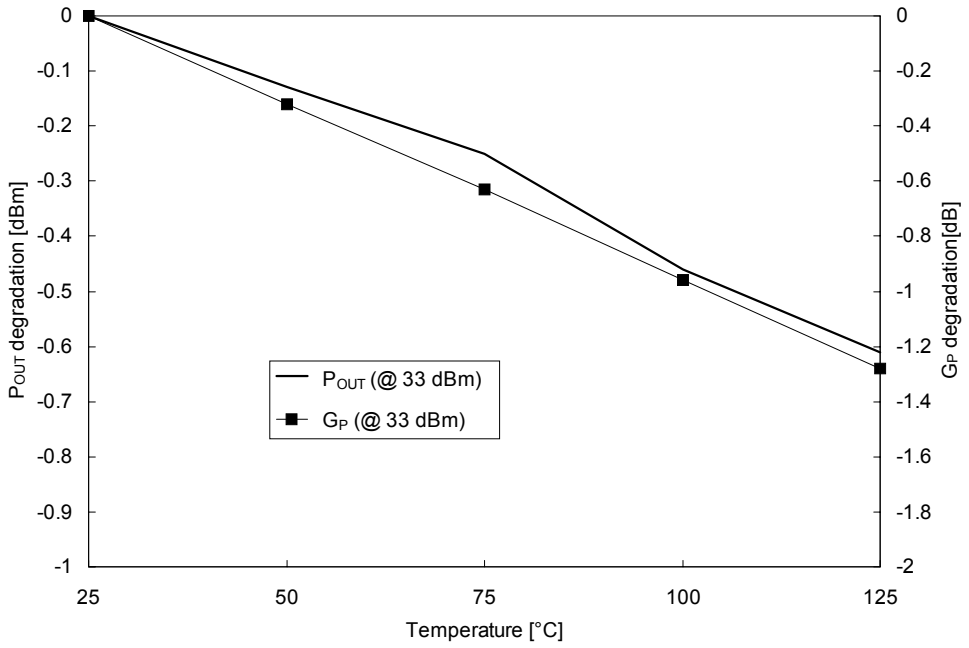

Figure 5.10: Degradation of the measured output power and the power gain of a MESFET with a total gate width of 3 mm and a gate-to-gate spacing of 30 µm. Load-pull measurements are performed at: V_{DS} = 9 V, V_{GS} = -1.25 V, P_S = 33 dBm, f = 8 GHz and Γ_L = 0.7/175°.

The temperature dependency of the HFET technology was only experimentally investigated. The results of this experiment are depicted in figure 5.11. From the measurement results a power gain reduction of –0.0275 dB/°C and an output power reduction of –0.0175 dB/°C is found. The temperature dependency of the HFET transistor is considerably higher than the temperature dependency of the MESFET transistor. For both transistor technologies, the

degradation of the power gain as a function of temperature is considerably higher than the output power degradation.

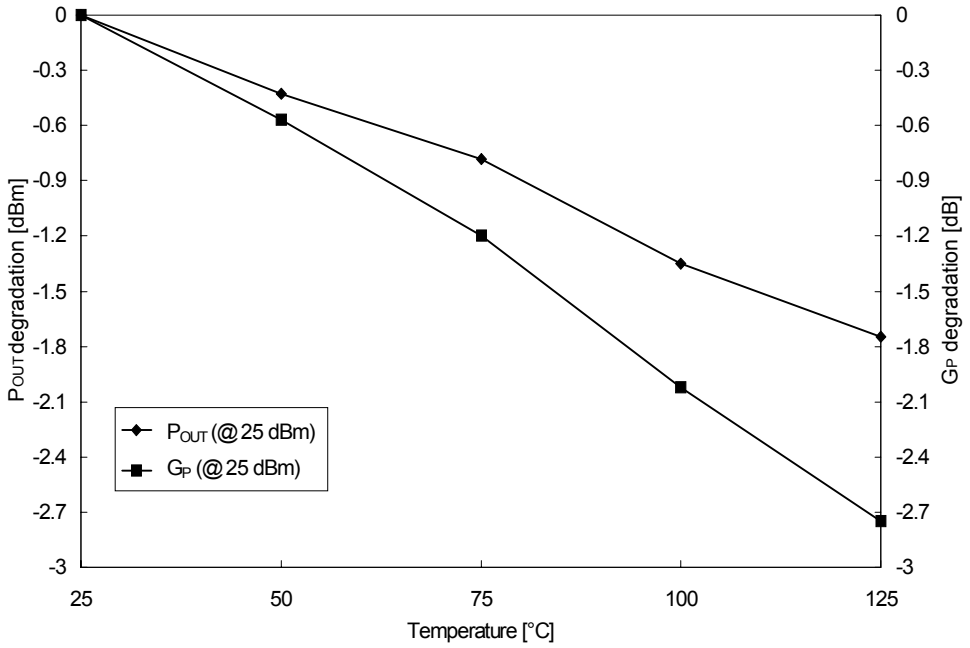

Figure 5.11: Degradation of the measured output power and power gain of a HFET with a total gate width of 1.44 mm and a gate-to-gate spacing of 25 µm. Load-pull measurements are performed at: V_{DS} = 8 V, V_{GS} = -0.2 V, P_S = 25 dBm, f = 8 GHz and Γ_L = 0.37/180°.

5.3.5 Gate-to-gate spacing

An additional degree of freedom for both, interdigitated and fishbone, transistor types is the gate to gate spacing. For an as compact as possible transistor layout this distance should be minimised while keeping at the same time the gate finger temperature below the value that will guarantee an acceptable reliability of the transistor. The power amplifier design work was started with interdigitated transistors that had a gate-to-gate spacing of 55 µm. For the 3 and 5-Watt MESFET high-power amplifiers, this spacing was reduced to 30 µm [5.2]. This reduction was necessary to keep the occupied chip area acceptable small. With the help of thermal simulations, it was verified if the resulting increase in maximum gate finger temperature was acceptable. In figure 5.12, the results of this analysis are shown, for a transistor with an interdigitated layout, as a function of the gate-to-gate spacing.

The thermal analysis software used to obtain these results was discussed in section 5.3.4. These results show that the maximum temperature stays below the 125 °C for a 55 µm gate-

to-gate spacing, which is considered to be a safe limit for the used process from a reliability point of view. Later the gate-to-gate spacing was reduced to 30 μm. For this spacing a maximum temperature, which is slightly larger than 125 °C is predicted. This was not considered a reliability problem because the calculated temperature is too high, see section 5.3.4. In addition, the dissipated power used is higher than the one that occurs in the power amplifiers.

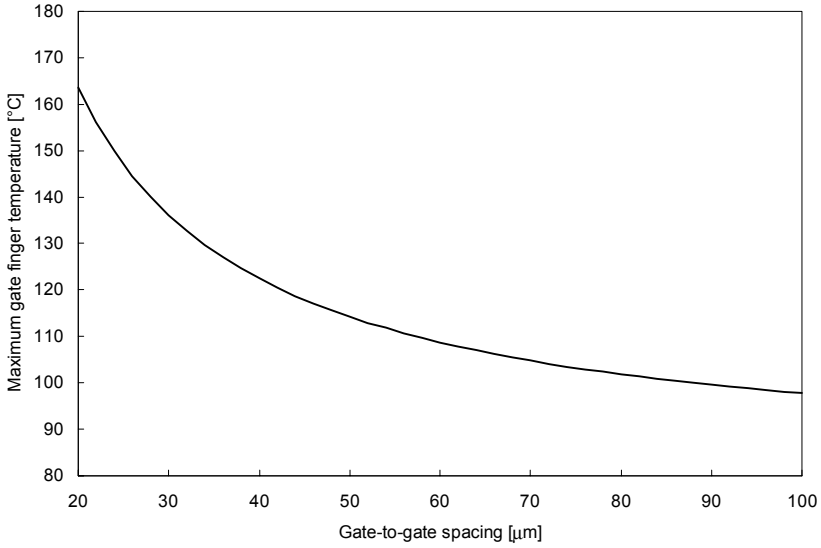

Figure 5.12: Simulated maximum gate finger temperature of a 12-finger interdigitated transistor with 125 μm wide gate fingers as a function of the gate-to-gate spacing. The ambient temperature is 60°C, the substrate thickness is 100 μm and the dissipated DC power is 1 W/mm.

5.4 Selection operating class and determination load impedance transistor

5.4.1 Introduction

The number of transistors used in parallel and their layout and size are selected now. The next step in the design process is the selection of the operating class. In this section the effect of the selected operating class and the effect of the load impedance on the power added efficiency, the gain and the output power of a transistor is discussed, see section 5.4.2. The determination of the optimum load is discussed in section 5.4.3.

5.4.2 Selection operating class

The discussion regarding the selection of the operating class starts with the help of idealised transistor characteristics. From this ideal case, the effect of the bias point selected and the effect of harmonic terminations on output power and power added efficiency are studied. In addition, the effect of non-idealities, like the knee voltage, the finite drain-source resistance and the bias dependent gain of the transistor will be discussed.

For reasons of convenience a number of relevant figures of merit, which were discussed in chapter 2, is briefly repeated here. The simplified small-signal equivalent circuit of a biased transistor and the corresponding DC-IV curves are shown in figure 5.13. A more detailed equivalent circuit model for the transistor was given in section 4.2.

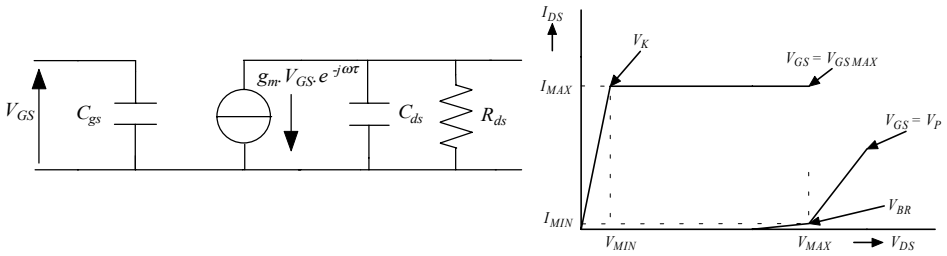

Figure 5.13: A simplified transistor model with idealised DC-IV curves.

The available output power is determined by the voltage and current limits expressed in the following equation see section 2.3.2:

$$P_{OUT} = \frac{(I_{MAX} - I_{MIN}) \cdot (V_{MAX} - V_{MIN})}{8}. \tag{5.18}$$

The minimum voltage V_{MIN} is determined by the knee voltage of the used transistors, see also section 2.3.2. The maximum voltage V_{MAX} that can be obtained is in principle determined by the breakdown voltage of the transistor. With these values the supply voltage, which will give the maximum voltage swing, can be calculated, see equation (2.15) in section 2.3.2. For the amplifiers discussed in this thesis a supply voltage of 8 - 9 V is used. These values are lower than the ones that can be calculated with help of equation (2.15). For the amplifiers discussed in this thesis the drain voltage is determined by the system in which the amplifiers are used. In addition, it is sensible to use lower supply voltages to create a safety margin so that the breakdown voltage will not be reached. Consequently, the voltage swing is limited by the knee voltage V_K. The maximum drain-source current I_{MAX} is determined by the gate current limit of 2 mA per gate finger.

The choice of the operating class has a direct influence on both the output power and the efficiency of the transistor. A measure for the efficiency of a transistor is the drain efficiency η_D, which is defined as:

$$\eta_D = \frac{P_{OUT}}{P_{DC}}. \tag{5.19}$$

Another, more useful measure for the efficiency of a transistor, because having a transistor with a high drain efficiency but no gain makes no sense, is the power added efficiency (*PAE*):

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}} \cdot \left(1 - \frac{1}{G_P}\right). \tag{5.20}$$

This equation shows that the power added efficiency is directly related to the drain efficiency of the transistor. It can also be concluded that the power gain of the transistor (G_P) should be as high as possible to obtain maximum power added efficiency, see section 2.3. A high power gain of a single transistor is also beneficial for the overall power added efficiency of the complete high-power amplifier as already discussed in section 5.2.

An overview of commonly used operating classes with their harmonic terminations is listed in table 5.3.

Table 5.3: Overview of commonly encountered "linear" operating classes and their harmonic terminations for the 2nd and 3rd harmonic frequency.

Class	η_D [%] [1)]	$Z_{L\ 2fo}$ [Ω]	$Z_{L\ 3fo}$ [Ω]	α_2 [°] [2)]
A	50	-	-	180
AB	50-78.5	0	0	90 - 180
B	78.5	0	0	90
C	78.5-100	0	0	0 - 90
F	88.4	0	∞	90

[1)] The maximum obtainable drain efficiency is given in reality this number will be lower.
[2)] The definition of the conduction angle α_2 is shown in figure 5.14.

In this overview, only single ended solutions are considered. As operating class, only A, B and AB was considered during this work. Class C was not considered because of its reduced output power capability and the difficult if not impossible way to realise harmonic load impedances. Class F was not considered because it is difficult to realise the necessary harmonic terminations over a broad bandwidth [5.20]. Class D and E type of amplifiers were not considered due to the switching speed required of the transistors and the necessary harmonic terminations that are not realisable over a broad bandwidth. An overview of before mentioned operating classes is given in [5.20-5.22].

The amplitude of the input voltage and the DC current setting determines the drain current waveform and the drain voltage waveform. In figure 5.14, a drain current waveform and a drain voltage waveform are shown which are driven into compression. The amount of drain current, which is driven into compression, is indicated with the angle α_1. In this figure I_F is the maximum current and I_P is the amplitude of the clipped cosine wave. The conduction

angle α_2 defines the operating class of the amplifier, see table 5.3. The drain current is zero between α_2 and 360°-α_2. The amount of drain voltage, which is driven into compression, is indicated with the angle α_3. It is assumed that the voltage is symmetrically driven into compression between zero and twice the supply voltage. Consequently, the average value of the voltage wave is equal to the supply voltage V_{DS}. The drain current waveform is described with the help of the following Fourier series:

$$I_{DS}(t) = I_{a0} + \sum_{n=1}^{\infty} I_{an} \cdot \cos(n \cdot \omega \cdot t) + \sum_{n=1}^{\infty} I_{bn} \cdot \sin(n \cdot \omega \cdot t), \tag{5.21}$$

where,

$$I_{a0} = \frac{I_F}{\pi \cdot (\cos\alpha_1 - \cos\alpha_2)} \cdot [\alpha_1 \cdot \cos\alpha_1 - \alpha_2 \cdot \cos\alpha_2 + \sin\alpha_2 - \sin\alpha_1], \tag{5.22}$$

and,

$$I_{a1} = \frac{I_F}{\pi \cdot (\cos\alpha_1 - \cos\alpha_2)} \cdot [\cos\alpha_1 \cdot \sin\alpha_1 - \cos\alpha_2 \cdot \sin\alpha_2 + \alpha_2 - \alpha_1], \tag{5.23}$$

and,

$$I_{bn} = 0 \qquad n = 1, 2, ..., \infty . \tag{5.24}$$

These equations describe the DC and first harmonic component of the drain-source current waveform depicted in figure 5.14. The higher harmonic components are considered to be short-circuited. This is a reasonable assumption as will become clear in the remainder of this section.

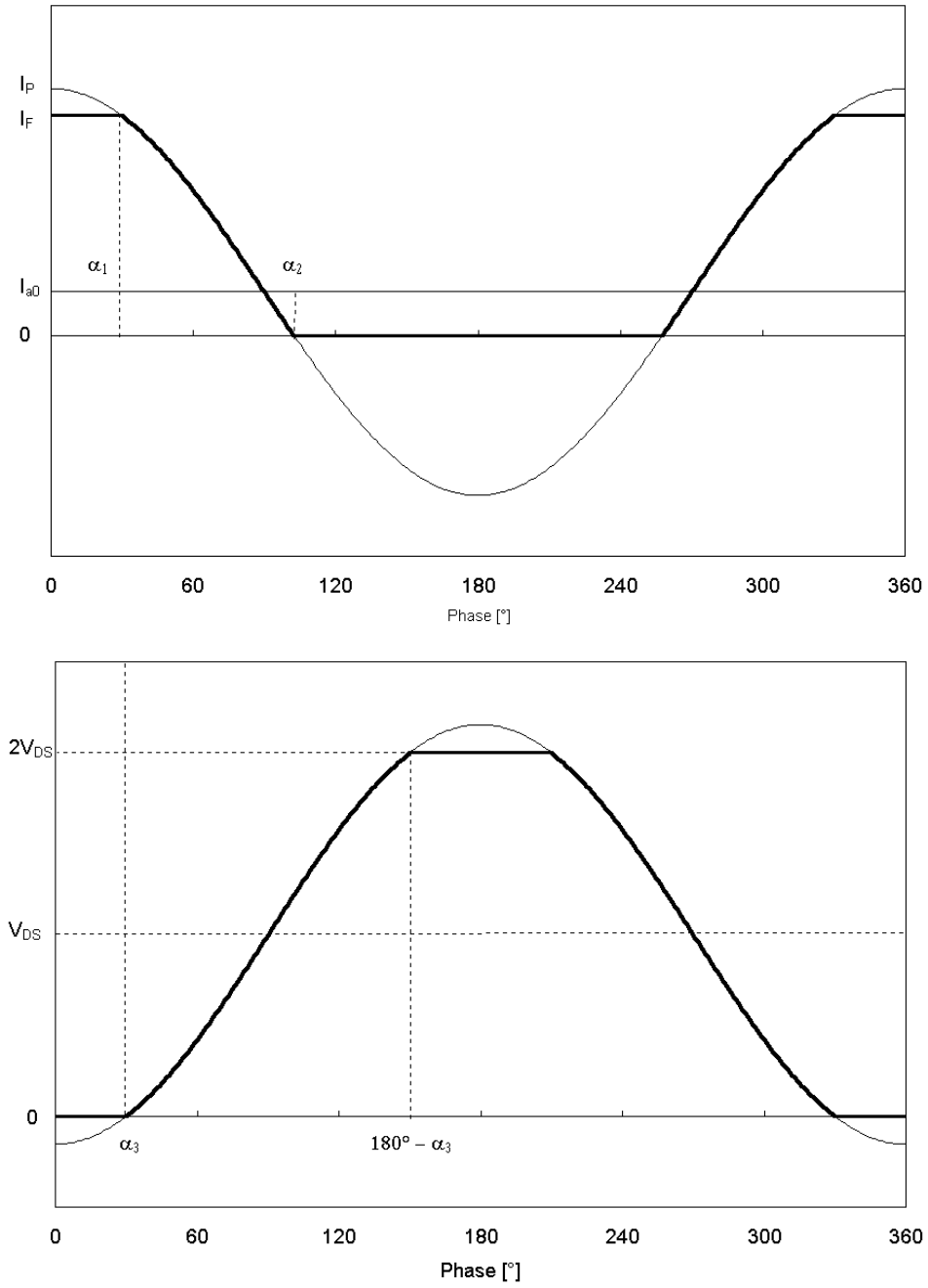

Figure 5.14: Drain current and drain voltage (thick lines) of an ideal FET. The angles α_1, α_2 and α_3 indicate where the current and voltage starts to clip.

In the following, the focus will be on the effect of single side clipping caused by the fact that the gate source voltage becomes smaller than the pinch-off voltage. The drain-current waveform is considered to reach the maximum drain-source current ($\alpha_1 = 0°$). The drain-source voltage is not clipped ($\alpha_3 = 0°$) and considered to be limited by the knee voltage of the transistor and not by the breakdown voltage. The latter assumption is valid for all amplifiers discussed in this thesis. The DC power consumption and the RF output power are given with the following equations:

$$P_{DC} = V_{DS} \cdot \frac{I_F}{\pi} \cdot \left(\frac{\sin\alpha_2 - \alpha_2 \cdot \cos\alpha_2}{1 - \cos\alpha_2} \right), \tag{5.25}$$

$$P_{OUT} = \frac{(V_{DS} - V_K) \cdot I_F}{2 \cdot \pi} \cdot \left(\frac{\alpha_2 - \cos\alpha_2 \cdot \sin\alpha_2}{1 - \cos\alpha_2} \right). \tag{5.26}$$

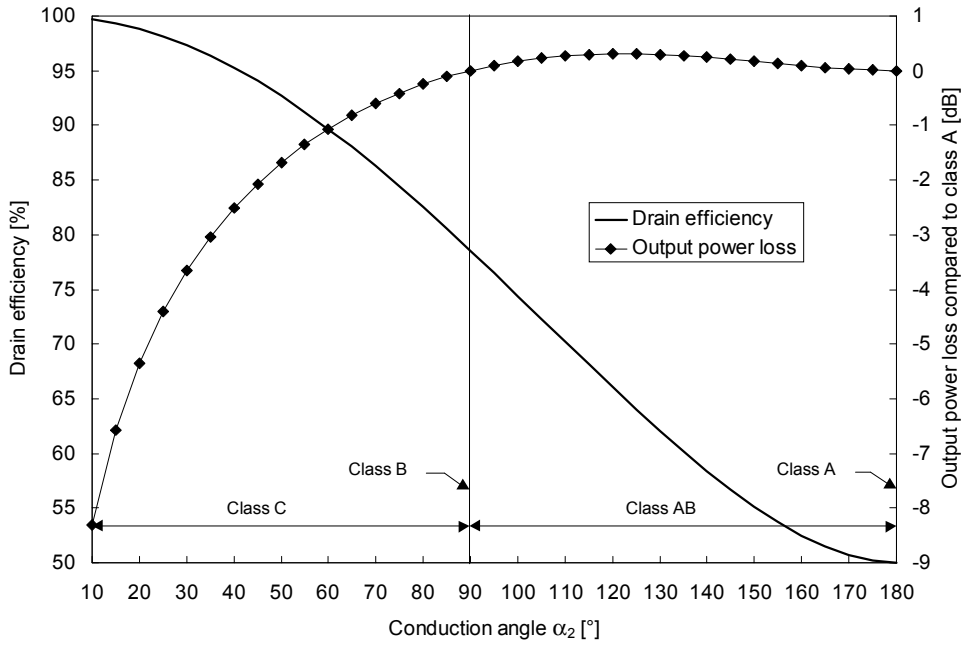

Figure 5.15: Effect of bias point selection on output power and drain efficiency.

The drain efficiency is then defined as follows:

$$\eta_D = \frac{P_{OUT}}{P_{DC}} = \frac{1}{2} \cdot \left(\frac{V_{DS} - V_K}{V_{DS}} \right) \cdot \left(\frac{\alpha_2 - \cos\alpha_2 \cdot \sin\alpha_2}{\sin\alpha_2 - \alpha_2 \cdot \cos\alpha_2} \right). \tag{5.27}$$

When the knee voltage V_K is set to zero, the classical text book efficiencies are found. For class A ($\alpha_2 = 180°$) the efficiency is 50% and for class B ($\alpha_2 = 90°$) the efficiency is $\pi/4$. In addition, it is clear that the efficiency is reduced when the knee voltage > 0.

In figure 5.15, the effect of the class selection is shown on both output power and drain efficiency. The results show that the drain efficiency increases with decreasing conduction angle α_2. The output power on the other hand is more or less constant between a class A and B operating point (a conduction angle between 90° and 180°). When an operating point is selected in the direction of class C the output power rapidly decreases. For the amplifiers, all the power that a transistor can deliver is needed. For this reason, operating a transistor beyond class B was not considered to be an option. As stated before a more realistic number for the efficiency is the power added efficiency, see equation (5.20). For the power added efficiency calculation, also the effect of the power gain G_P is taken into account. In [5.23] the following equation for the power added efficiency is given which relates the conduction angle α_2 with the class A power gain G_A:

$$PAE = \frac{G_A \cdot (1 - \cos\alpha_2) \cdot (\alpha_2 - \sin\alpha_2 \cdot \cos\alpha_2) - 2 \cdot \pi}{2 \cdot G_A \cdot (1 - \cos\alpha_2) \cdot (\sin\alpha_2 - \alpha_2 \cdot \cos\alpha_2)} . \tag{5.28}$$

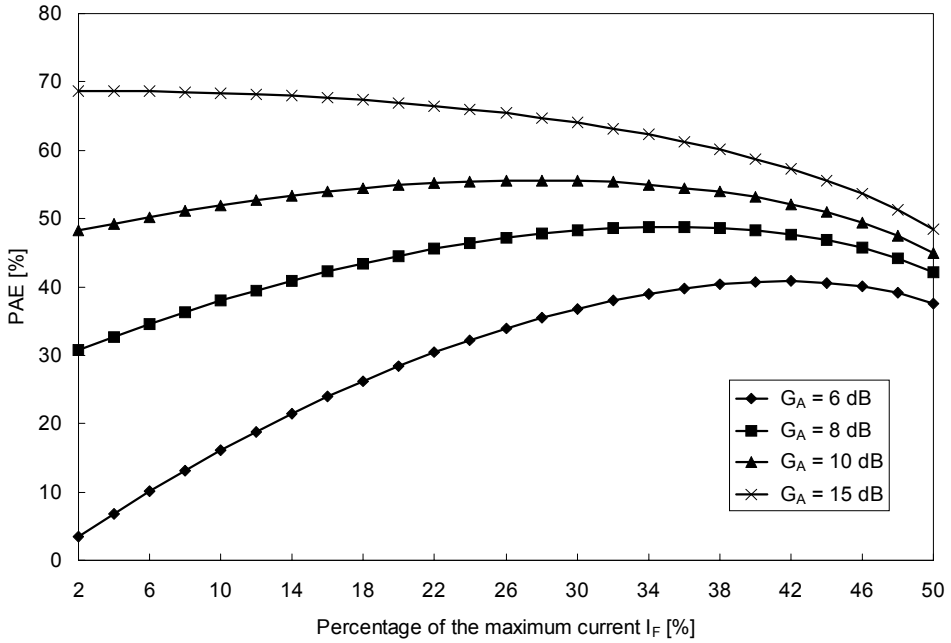

Figure 5.16: The calculated power added efficiency as a function of the drain-source current setting as percentage of the maximum current and the gain of the transistor in Class A, see equation (5.28).

In literature, normally the discussion regarding the optimum bias point for maximum power added efficiency is not based on the conduction angle but is based on a current setting as a function of the maximum current I_F. The relation between the percentage of the maximum current setting X and the conduction angle α_2 is given by the following equation:

$$X = \frac{-\cos\alpha_2}{1-\cos\alpha_2}. \tag{5.29}$$

The power added efficiency as a function of the current setting as a percentage of the maximum current, is plotted for several different power gains in figure 5.16. The results show that when the power gain is decreasing the percentage of the maximum drain current that will give the maximum power added efficiency moves from a class B (0% of I_F) operating point to a class A (50% of I_F) operating point. The available power gain should be considered at, at the highest frequency of interest. For the used MESFET process and depending on the transistor layout used, the gain varies between 8 and 10 dB. Therefore, a drain current setting between 25 and 30% of the maximum drain current seems optimal. The HFET process used has a minimum gain of 12 dB. In the latter case, a 25% drain current setting seems optimal. These numbers derived from idealised transistor characteristics are comparable with the numbers found in literature [5.25].

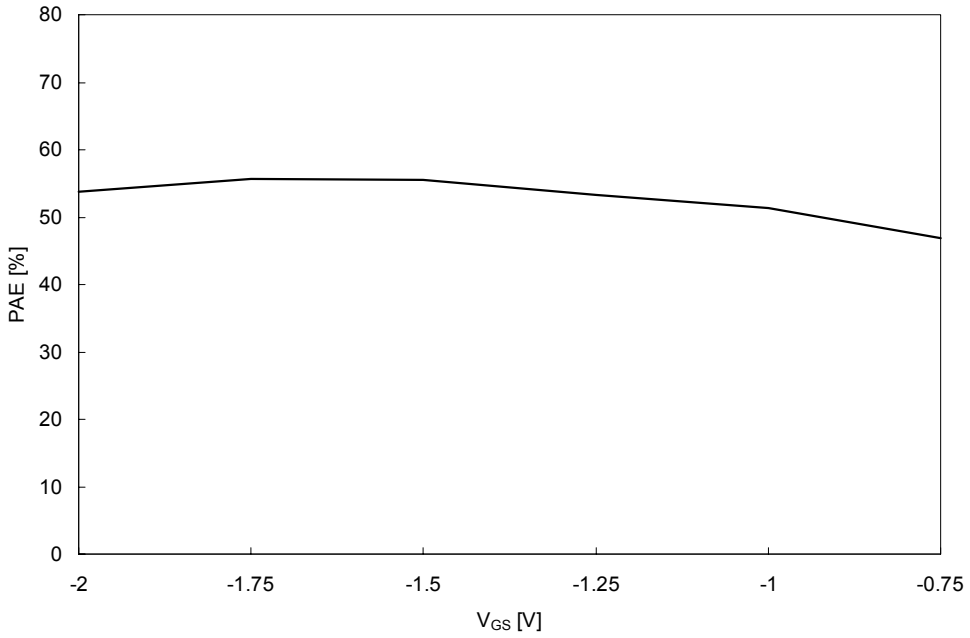

Figure 5.17: Measured effect of gate bias on power added efficiency. The results are obtained for a fishbone MESFET with a total gate width of 2.4 mm. Measured at 8 GHz, V_{DS} = 9 V and Γ_{LOAD} = 0.63/164°.

The gain reduction used in equation (5.28) between class A and B is 6 dB. In reality, this gain reduction will be less [5.3] and the resulting power added efficiency would be higher. The power added efficiency variation as a function of the bias setting is illustrated by a measured power added efficiency versus bias voltage, see figure 5.17. In class A, the gain of the transistor is approximately 10 dB. A gate voltage of –0.75 V corresponds with a class A bias point. A gate voltage of –2 V corresponds with a bias point close to class B. The results that are depicted show once again that the maximum power added efficiency is found at a class AB bias point.

The calculations mentioned before are all given up to the point where the drain current starts to be clipped by the maximum obtainable drain current. Beyond this point when the proper harmonic terminations are utilised a further increase in output power and power added efficiency can be obtained by further overdriving the transistor as has been shown by Snider [5.24]. To analyse what will happen when the transistor is driven into compression, it is assumed that the drain voltage will go into compression at the same input power level as the drain current, see figure 5.14. The proper harmonic terminations are assumed present, so that the voltage wave will be symmetric around the bias voltage V_{DS}. Under the assumption that the knee voltage V_K = 0 V the first harmonic component of the voltage wave can be calculated as follows:

$$V_{a1} = \frac{V_{DS}}{\pi} \cdot \frac{\left(\pi - 2 \cdot \alpha_3 + \sin 2 \cdot \alpha_3\right)}{\cos \alpha_3} . \tag{5.30}$$

When the voltage and current wave are driven into compression at the same conduction angle ($\alpha_1 = \alpha_3$) then the dissipated DC power and the RF output power can be calculated with the help of the following equations:

$$P_{DC} = \frac{V_{DS} \cdot I_F}{\pi} \cdot \frac{\left(\alpha_1 \cdot \cos \alpha_1 - \alpha_2 \cdot \cos \alpha_2 + \sin \alpha_2 - \sin \alpha_1\right)}{\left(\cos \alpha_1 - \cos \alpha_2\right)}, \tag{5.31}$$

$$P_{OUT} = \frac{V_{DS} \cdot I_F}{2 \cdot \pi^2} \cdot \frac{\left(\pi - 2 \cdot \alpha_1 + \sin 2 \cdot \alpha_1\right)}{\cos \alpha_1} \cdot \frac{\left(\sin \alpha_1 \cdot \cos \alpha_1 - \sin \alpha_2 \cdot \cos \alpha_2 + \alpha_2 - \alpha_1\right)}{\left(\cos \alpha_1 - \cos \alpha_2\right)} . \tag{5.32}$$

The drain efficiency can be calculated with the help of equation (5.19) and the power added efficiency can be calculated with the help of equation (5.20) provided that the gain can be calculated. For the calculation of the gain, the method described by Snider [5.24] is used. The power gain G_P in the non-linear operating region can be expressed as a function of the linear output power, the compressed output power and the linear gain G_{P_LIN} :

$$G_P = G_{P\_LIN} \cdot \cos^2 \alpha_1 \cdot \frac{P_{OUT}\ \alpha_1 \neq 0}{P_{OUT}\ \alpha_1 = 0} . \tag{5.33}$$

The compression level C_L is calculated with the following equation:

$$C_L = \frac{1}{\cos^2 \alpha_1}. \tag{5.34}$$

The calculated power added efficiency results and the increase in output power compared to the linear case (α_1 = 0) are shown in figure 5.18. The results show that both the output power and the power added efficiency will increase when the transistor is driven into compression. When the maximum power added efficiency point is considered the optimum, then an increase in absolute sense of 3.4% in power added efficiency and 0.73 dB in output power is observed. This optimum is found in this case for a power compression level of 1.5 dB, which compares well with the compression levels found from measurements performed on the transistors used in the amplifiers discussed in this thesis.

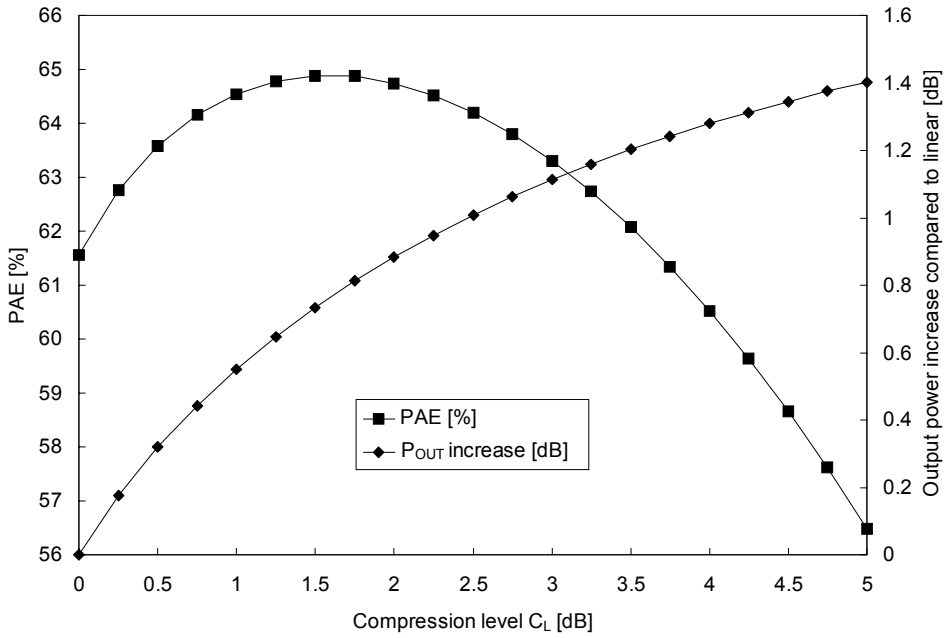

Figure 5.18: Calculated output power and power added efficiency as a function of the compression level. The results are calculated at a Class AB operating point (X = 0.25) and G_{P_LIN} = 9 dB.

In figure 5.19, it is shown that the compression level that will give the maximum power added efficiency mainly depends on the gain of the transistors used and not that much on the operating class of choice. The results from figure 5.19 also show that the optimum power added efficiency point for the transistors used, is found between (linear transistor power gain is 7 – 12 dB) the one and two dB compression point.

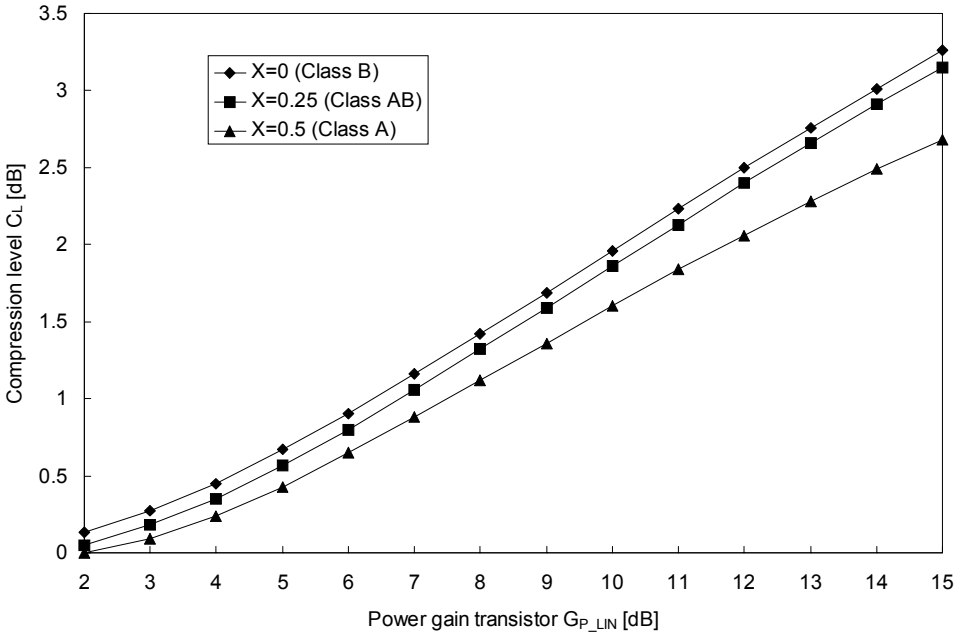

Figure 5.19: Calculated compression level that results in the maximum power added efficiency as a function of the transistor gain. The calculation is performed for three different operating classes.

The calculated ideal output power and power added efficiency are influenced by the following factors:

1. The drain-source resistance which has a finite value.
2. The drain-source capacitance which has a significant influence at X-band and higher frequencies.

The influence of these factors on the performance of the transistor will be discussed in the remainder of this section. The finite drain-source resistance causes a reduction in the amount of power that can be delivered to the load impedance by the transistor. The ratio between the real part of the optimum load impedance and the drain-source resistance determines the amount of power that is dissipated in this resistance. The current that flows through the substrate underneath the active channel determines the value of R_{ds}. This current should be minimised as much as possible. The amount of output power reduction N_{DS} due to the finite value of R_{ds} can be calculated with the help of the following equation:

$$N_{DS} = \frac{R_{ds}}{R_{ds} + R_S}. \tag{5.35}$$

In this equation R_S is the real part of the optimum load impedance as will be discussed in chapter 6. In table 5.4, calculated average output power reduction figures for the MESFET and HFET transistors used at a typical bias point are given.

Table 5.4: Average output power reduction N_{DS} due to finite value of drain-source resistance R_{DS}.

	V_{DS} [V]	V_{GS} [V]	R_{DS} [Ω.mm]	R_S [Ω.mm]	N_{DS}
MESFET	9.0	-1.25	145.0	55.1	0.72
HFET	8.0	-0.30	190.0	41.0	0.82

The results show a considerable reduction of the output power due to the finite value of the drain-source resistance. Therefore, the expected output power values based on DC limitations, which are mentioned in chapter 2 will be reduced. On the other hand the output power will be increased again because the transistors will be used in their non-linear region, typically with a factor of 1.17 (0.7 dB). Based on this number and the values listed in chapter 2 and table 5.4, an output power of 570 mW/mm is estimated for the MESFET transistors and 850 mW/mm for the HFET transistors. These numbers are close to the measured ones that are listed in section 5.7.1, which shows the validity of the used approach to estimate the expected output power under RF conditions.

The drain-source capacitor C_{ds} has a significant influence at X-band and higher frequencies. Therefore, a complex load has to be presented to the output terminal of the transistor in order to obtain a real load impedance at the current source inside the transistor. The design of such complex load impedance will be discussed in detail in chapter 6. At the higher harmonic frequencies, C_{ds} presents already more or less a short circuit at the output of the transistor. Consequently, the effect of harmonic tuning at the output of the FET is less than expected from values found in the literature [5.25 - 5.27]. Power added efficiency improvements of more than 15% are reported with the help of harmonic tuning.

The result of a harmonic load-pull simulation of a 1.5 mm MESFET at 10 GHz is shown in figure 5.20. These results show that an absolute power added efficiency improvement of only 6.5% is obtained with the help of harmonic tuning. This is clearly less than the cited 15% improvement. The effect of neglecting the C_{ds} for a Infineon DIOM20HP MESFET with a total gate width of 1.5 mm, in combination with harmonic tuning is shown in figure 5.21. The drain-source capacitor has been left out of the simulation by applying a capacitor at the output of the transistor that has a negative value equal to C_{ds}. Although this way to remove the influence of C_{ds} is not entirely correct, still the effect of C_{ds} on harmonic tuning is demonstrated.

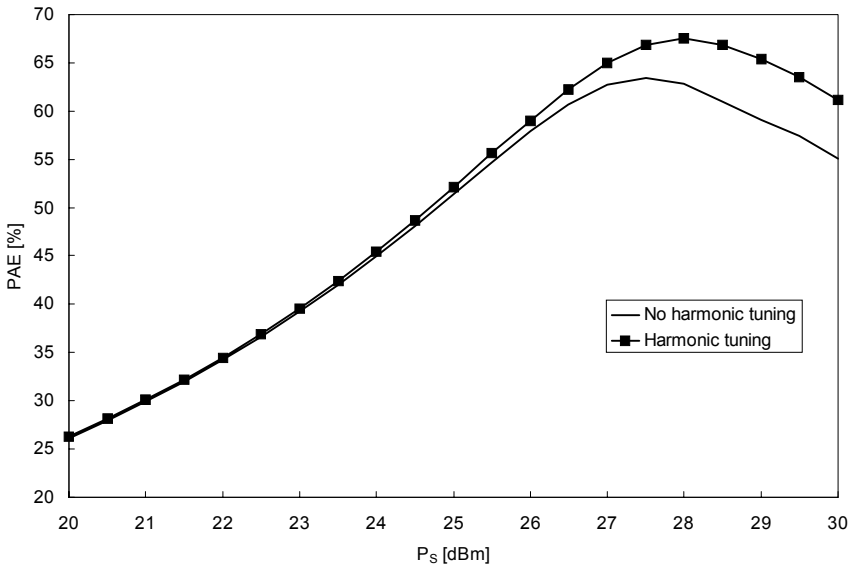

Figure 5.20: Power added efficiency with and without harmonic matching for a MESFET with a total gate width of 1.5 mm. The results are calculated at 10 GHz, V_{DS} = 9 V and V_{GS} = -1.6 V.

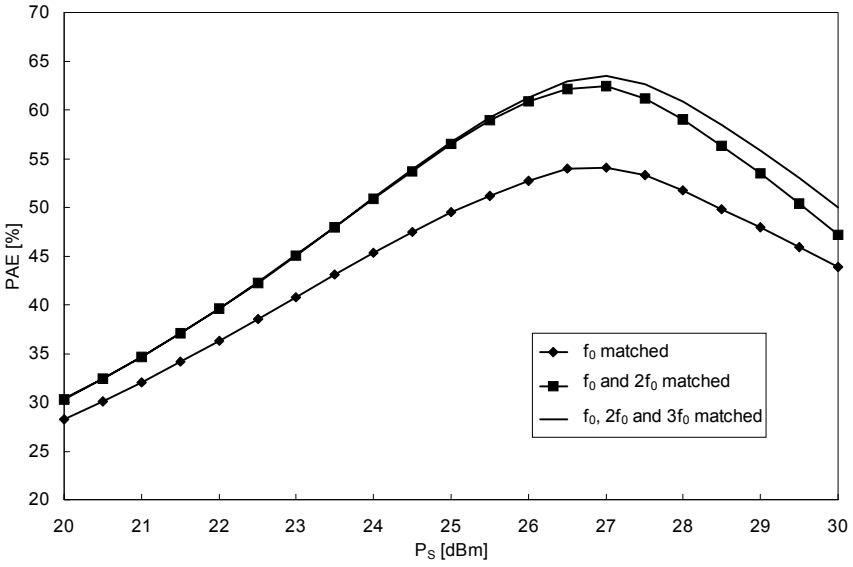

Figure 5.21: Power added efficiency with and without harmonic matching for a MESFET without C_{ds}. A MESFET with a total gate width of 1.5 mm is used. The results are calculated at 10 GHz, V_{DS} = 9 V and V_{GS} = -1.6 V.

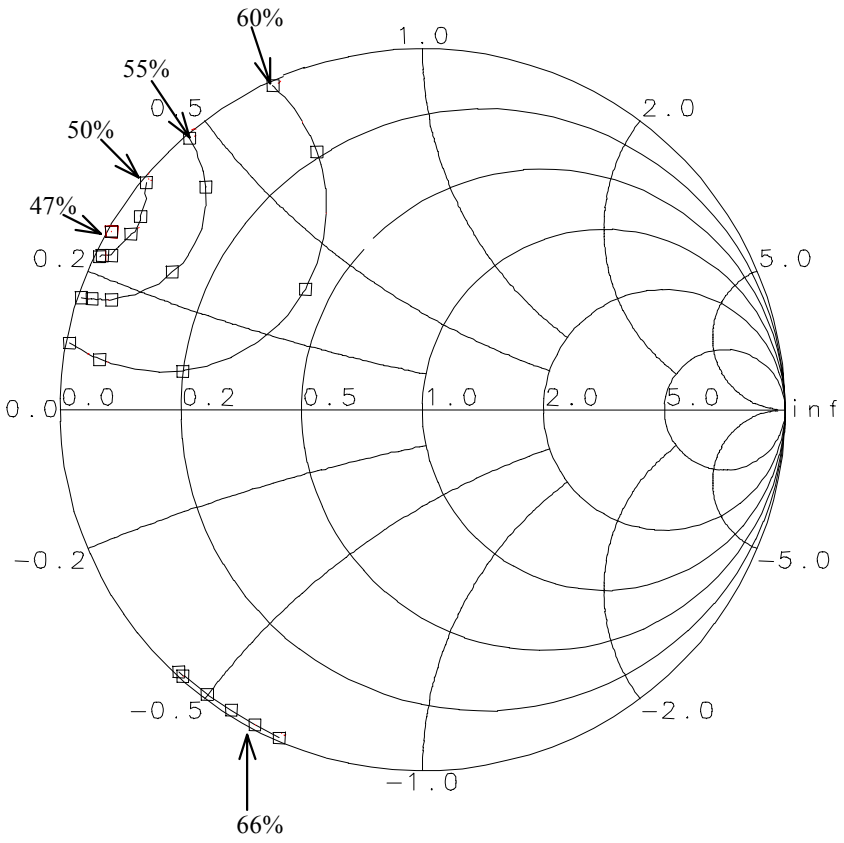

Figure 5.22: Power added efficiency contours (the values are indicated with arrows) when a load-pull simulation at the second harmonic frequency is performed. (Γ_{f0} = 0.62/142°, Γ_{3f0} = 0.0/0.0°, V_{DS} = 9 V, V_{GS} = -1.6 V, f0 = 9.3 GHz and P_S = 27 dBm).

The results clearly show that harmonic tuning is also effective at X-band when the influence of C_{ds} is neglected. In that case, a power added efficiency improvement of 17% is achieved. This is comparable to the power added efficiency improvement numbers cited in literature. Therefore, it can be stated that C_{ds} already acts as a harmonic pre-match at X-band. When the same transistor would have been used, at for instance 900 MHz, a significant power added efficiency improvement would have been obtained with the help of harmonic tuning. Therefore, for the given transistor harmonic tuning would not result in a large power added efficiency improvement. Nevertheless, it is important to check at least the impedance at higher harmonic frequencies to prevent a reduction of the power added efficiency. This can occur if the imaginary part of the load impedance presented to the transistor resonates out the C_{ds} of the transistor. An example of such a situation is shown in figure 5.22 where the

simulated power added efficiency contours as a function of the second harmonic load impedance are shown. Most of the second harmonic load impedances result in a similar power added efficiency. The output-matching network tends to result in an open circuit for higher harmonic frequencies, see chapter 6. More details regarding the effect of C_{ds} on power added efficiency could be found in [5.28].

5.4.3 Determination optimum load impedance

The effect on the output power, gain and power added efficiency of the load impedance presented at the output of the transistor is discussed in this section. First, in short a number of different methods that can be used for the determination of the optimum load impedance will be reviewed.

The following methods to determine the optimum load impedance were considered:

- The use of the so-called Cripps method [5.29, 5.30]. This method uses a simplified model of the transistor, which can be obtained from small-signal S-parameter measurements at the bias point of interest and knowledge of the DC IV curves. With the help of this information it is possible to construct load-pull contours and the optimum load impedance can be determined. The Cripps method was not used because of the following limitations:
  1) The DC IV curves are not always similar to the AC IV curves.
  2) Other essential information for the high-power amplifier design is missing e.g. the input impedance of the transistor under large-signal conditions when it is loaded with the optimum load impedance.
  3) Modelling of the external part of a transistor with only the drain to source capacitance is too simplistic. Certainly for large transistors, as it is the case for the discussed high-power amplifiers, the influence of the drain-source resistance and the parasitic inductances on the external optimum load impedance can no longer be neglected.

  However, if no large-signal transistor model or load-pull measurement set-up is available it can give a reasonable estimation of the optimum load impedance.

- The use of load-pull simulations performed with the help of the large-signal transistor model and the contour test bench available in the Agilent Series IV simulation software [5.31]. Comparison with load-pull measurements shows, as already discussed in section 4.2, that the transistor model will give a good estimation of the location of the optimum load impedance in the case of maximum output power. This becomes more difficult if an optimum load impedance for maximum power added efficiency is searched. This is due to the overestimation of the drain current by the transistor model.

- The use of load-pull measurements is still the preferred method to determine the optimum load impedance. When this type of measurements is performed with a system like the one that is described in section 3.3, information becomes available regarding the load impedance of the interstage-matching network.

Determination of the optimum load impedance based on load-pull measurements is the method, which is discussed, in the remainder of this section. First, we will concentrate on the optimum load impedance of the output transistor stage of the amplifier. The load impedance, which must be presented at the output of the transistors, is dependent on the input power. Under small-signal conditions, the optimum load impedance for maximum output power, power added efficiency and power gain is the same. The load that is found for this case is the conjugated of the output impedance of the transistor when the input is simultaneously conjugated matched with the source impedance. When the input power is increased, the real part of the load impedance starts to change from R_{ds} to a load that will guarantee maximum voltage and current swing. An example how the load impedance varies as a function of the input power can be seen in figures 3.11 and 3.12 in chapter 3. In the amplifiers discussed in this thesis, the output stage transistors have been driven a few dB into compression. This is done to get an optimum performance of the high-power amplifiers with respect to output power and power added efficiency, see section 5.4.2. Under these non-linear conditions the optimum load for maximum output power and the one for maximum power added efficiency are unequal. For a number of amplifiers, a compromise between these two impedances is used. The real part of the load impedance R_L can be calculated by combining equation (5.23) and equation (5.30) into:

$$R_L = \frac{V_{DS}}{I_F} \cdot \frac{(\pi - 2\alpha_3 + \sin 2\alpha_3)}{\cos\alpha_3} \cdot \frac{(\cos\alpha_1 - \cos\alpha_2)}{(\cos\alpha_1 \cdot \sin\alpha_1 - \cos\alpha_2 \cdot \sin\alpha_2 + \alpha_2 - \alpha_1)} . \quad (5.36)$$

For simplicity reasons the knee voltage is considered to be zero. The current waveform that will result in maximum drain efficiency and consequently also in maximum power added efficiency is found from:

$$\frac{\delta \eta_D}{\delta \alpha_1} = 0 \quad \Rightarrow \alpha_1 = 0 . \quad (5.37)$$

This solution ($\alpha_1 = 0$) for the maximum drain efficiency is identical to the one found by Snider [5.24]. In figure 5.23, the results of the real part of the load impedance R_L for the maximum efficiency case ($\alpha_1 = 0$) and the maximum output power case ($\alpha_1 = \alpha_3$) are compared.

The results show that the real part of the load for maximum efficiency is higher than the one for maximum output power. The load for maximum output power is almost constant as a function of compression level. This is as expected not the case for the maximum efficiency load. At the two-dB compression level, there is already a difference of 10% between the real part of both load impedances. The imaginary parts of both load impedances are equal, as it will become clear from the discussion in the next chapter and appendix F.

The optimum load impedance for all other transistors used in the power amplifier depends on the fact whether they are used in their linear region and how much output power margin there is before they are driven into compression. If there is sufficient margin, to guarantee

that the transistors will only operate in their linear region then the optimum load is the one, which maximises the power gain of the transistor. In the amplifiers discussed in this thesis most of the time, one transistor is used to drive two transistors in the next stage, see also section 5.2. In combination with the low gain of the transistors used and the losses in the interstage-matching network this leads to the conclusion that there will not be much margin before these transistors will be driven into compression. Load-pull simulations have been performed [5.32] to find the optimum load impedance as a function of frequency. The simulated results showed at the low end of the band an optimum load impedance that will result in maximum power gain. At the high end of the frequency band, an optimum load impedance for maximum output power was found. This combined with the fact that the load impedances of the interstage-matching networks are difficult to realise led to the conclusion to use the load for maximum output power over the entire frequency band. This choice gives more guarantees that the output stage will be the first amplifier stage that goes into compression.

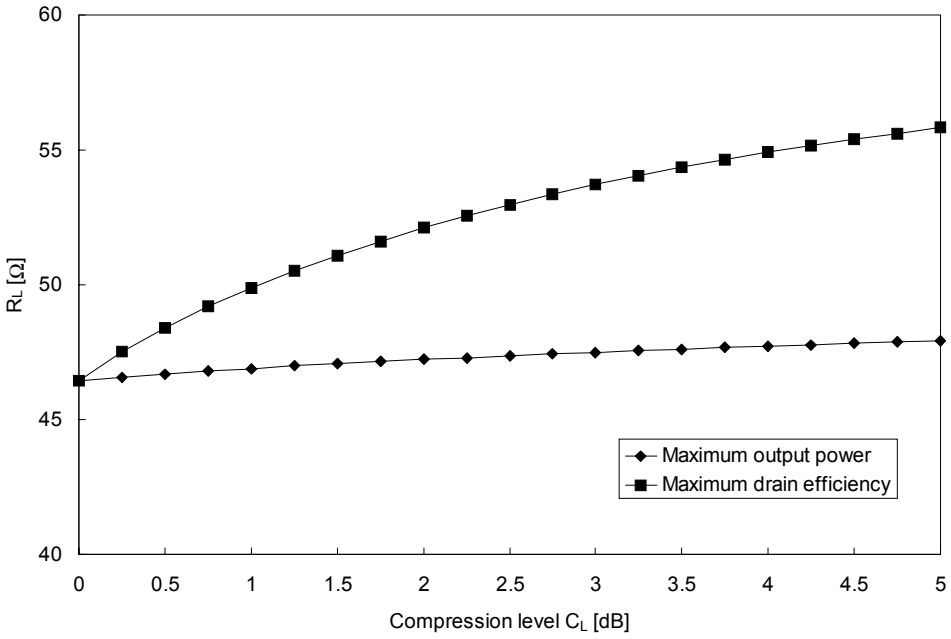

Figure 5.23: Calculated real part load impedance R_L for the maximum drain efficiency and output power case at X = 0.25. For this calculation some typical MESFET values have been taken: V_{DS} = 9 V and I_F = 365 mA.

5.5 Reliability improvement

The reliability of a high-power amplifier is directly related to the reliability of the transistors used. Factors that influence the reliability of a transistor are temperature and electrical stress caused by for instance gate current. The problem of temperature can be minimised by selecting a proper transistor layout. This was discussed in detail in section 5.3.4. Excessive current densities are harmful to the long-term reliability of the transistor due to the electron-migration, which will start to take place. These high current densities start to occur when large-signal input power levels are applied to the transistor. The problem starts to occur first for the gate current, due to the small cross section of the gate fingers. Although this problem is a bit reduced when so-called mushroom gates are used it is still a problem under large-signal conditions. The gate current density under large-signal conditions can be reduced with a series resistor in the gate bias circuit, see figure 5.24.

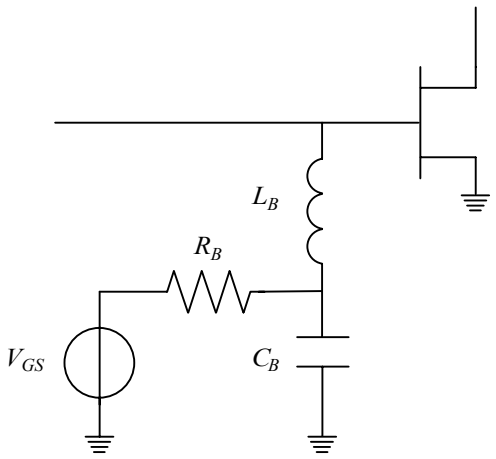

Figure 5.24: Biasing of the transistor gate with the help of a series resistor.

The use of gate bias resistors causes a reduction of the gate voltage when gate current starts to flow at the moment the transistor is driven into compression. Application of gate bias resistors results in a disadvantage for the output stage only. In that case, the maximum obtainable output power is reduced. For the other amplifier stages, sufficient output power margin is available. The output power is reduced because the maximum drain current swing is limited. For the discussed technologies the output power is reduced with 0.5 - 1.0 dB when a series resistor is applied in the gate bias supply lines, see the results listed in table 5.5.

Table 5.5: Large-signal simulation results at the 2 dB compression point of a 3 mm MESFET (N_{GF} = 48, W_U = 63 μm) simulated for different values of the gate resistance R_B. All simulations are performed at V_{DS} = 9 V, V_{GS} = -1.25 V and Γ_L = 0.753/169.38°.

R_B [Ω]	P_{OUT} [dBm}	PAE [%]	I_D [mA]	I_G [mA]
0	33.57	55.3	380	34.9
25	33.07	55.9	337	20.7
50	32.92	56.0	324	13.8
75	32.84	56.1	318	10.3
100	32.76	56.0	313	8.3
125	32.72	55.9	310	7.0
150	32.68	55.8	307	6.0
175	32.64	55.7	305	5.3
200	32.62	55.6	304	4.7

The results listed in table 5.5 show that the gate current is reduced when a gate resistor is applied in the bias circuit. The power added efficiency is not reduced by the application of the gate resistor. For the simulation results listed in table 5.5, the transistor was terminated with the optimum load impedance found for the situation where no gate resistance was applied. The question arises if for instance for a gate resistance of 100 Ω a different optimum load impedance will be found. Simulations show that this is hardly the case. For the 100 Ω example an optimum load reflection coefficient of Γ_L = 0.763/167.20° is found, which is more or less the same as the one found for the situation without gate resistor. The output power is only 0.02 dB higher with this new load impedance. The fact that the optimum load impedance hardly changes when a gate resistance is applied is also confirmed by the load-pull measurements described in [5.33]. The behaviour of the results discussed in [5.33] show a similar influence of the gate resistance on both the output power, power added efficiency and gate current as it is observed from the simulation results listed in table 5.5. Therefore, it can be concluded that simulations can be used to give a reliable prediction of the influence of the gate resistor on large-signal performance of the transistor. The results as listed in table 5.5 show that there is hardly any difference between the results obtained for 100 and 200 Ω. This seems to indicate that any large resistor might be used, which is convenient from a matching point of view, see section 6.3. This is not the case, because as pointed out by Constantin [5.33], there can be a problem with thermal runaway of the transistor when a large resistor is applied. Therefore, for the designs discussed in this thesis, the value of the gate resistor is limited to a maximum of 50 Ω for the transistors used in the output stage. For this value, no problem with thermal runaway is observed for the used transistors. The thermal runaway problem is caused by the positive feedback of the leakage current between the gate and source of the transistor.

5.6 Transistor stability analysis

The selection of the unit transistor cell and the operating class along with the determination of the optimum load impedance was discussed in the previous sections. After the transistor size is selected, the stability of this transistor must be checked up to the maximum frequency of oscillation f_{MAX}. The most desirable situation is the one in which the transistor is unconditional stable for all frequencies of interest. Unfortunately, this is almost never the case in practice. It is certainly not the case for the transistors used in the high-power amplifier designs discussed in this thesis. Unconditional stability is desirable because in that case all passive terminations can be presented to the input and output of the transistor without the risk of starting an oscillation. If the transistors are not unconditional stable, they must be made stable with the help of passive networks that make the combination of transistor and network stable. These stabilisation networks are an integral part of the matching networks and therefore have influence on microwave frequencies. It is thus essential to check if such a network is necessary before the design of the matching networks is started. If stabilisation networks are necessary, their topology and component values have to be established.

The stability of the transistor can be analysed with the help of the so-called *K*-factor first described by Rollet [5.34]:

$$K = \frac{2 \cdot \mathrm{Re}(\gamma_{11}) \cdot \mathrm{Re}(\gamma_{22}) - \mathrm{Re}(\gamma_{12} \cdot \gamma_{21})}{\left|(\gamma_{12} \cdot \gamma_{21})\right|}, \tag{5.38}$$

where, γ is any of the immittance *z*, *y*, or hybrid *h* or *g* matrix parameters. The *K*-factor can also be expressed with the help of the S-parameters of the transistor,

$$K = \frac{1 + \left|S_{11} \cdot S_{22} - S_{12} \cdot S_{21}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2}{2 \cdot \left|S_{12} \cdot S_{21}\right|}. \tag{5.39}$$

The latter definition of the *K*-factor is the one that was mainly used for the design of the amplifiers. The *K*-factor itself is not sufficient to guarantee unconditional stability. For this, an additional factor is necessary. In [5.35], an overview is given of a number of factors that can be used. For this work the following additional condition is used:

$$B_1 = 1 + \left|S_{11}\right|^2 - \left|S_{22}\right|^2 - \left|S_{11} \cdot S_{22} - S_{12} \cdot S_{21}\right|^2. \tag{5.40}$$

Unconditional stability of the transistor is guaranteed if the *K*-factor is larger than one and the factor B_1 larger than zero. As stated before unconditional stability is not guaranteed for the transistors used in this thesis, see for an example the results depicted in figure 5.25.

At this point in the discussion, it is good to point at the condition, formulated by Rollet [5.34], which states when the *K*-factor may be used for the determination of the stability of a

linear two-port. This condition states that at least one set of immittance parameters of the two-port must have no right half plane poles. The author fully agrees that this factor as stated in [5.36] often is overlooked by microwave designers. In practice, the condition given by Rollet is difficult to obtain from measurements because it is difficult to measure directly immittances at microwave frequencies. For this reason, Ohtomo has given a more general condition based on S-parameters [5.36]. Ohtomo states that at least one set of S-parameters of a two-port terminated with arbitrary positive reference impedances must have no right-plane poles. In practice this is guaranteed when the S-parameters can be measured. This is the case for all transistors used in the high-power amplifiers discussed in this thesis.

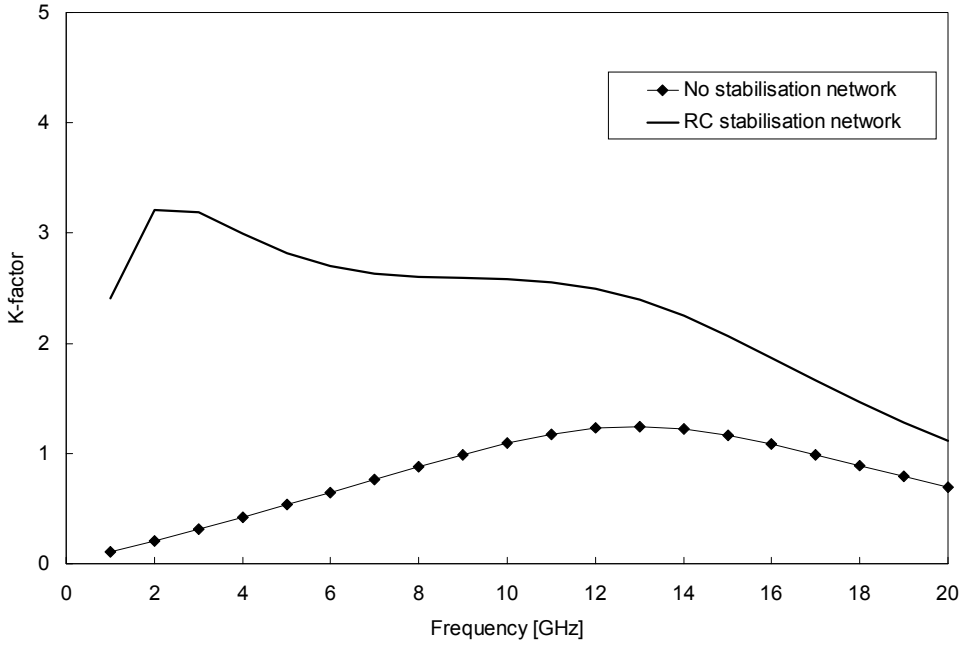

Figure 5.25: K-factor of a 2.16 mm HFET (48 fingers with W_U = 45 µm) with and without stabilisation network simulated at V_{DS} = 8 V and V_{GS} = -0.3 V.

For two-ports that have multiple active devices other stability analysis methods must be used. Examples of other types of analysis methods are given in [5.37, 5.38] where the Normalised Determinant Function is used to analyse the stability of a given circuit. The stability analysis of multi-device structures is discussed in more detail in section 6.7. For the moment, we go back to the results that have been depicted in figure 5.25. There it is shown that the given transistor is not unconditional stable below 9 GHz. This frequency is already very close to the frequency band of interest. Nevertheless, it should be noted that it is not certain that when the *K*-factor is smaller than one, the transistor will start to oscillate. That depends on the source and load impedance presented to the transistor. In this case a better insight can be gained with the help of so-called stability circles, see for instance [5.39] for a

derivation of these circles. An example of the use of the stability circles is shown in figure 5.26.

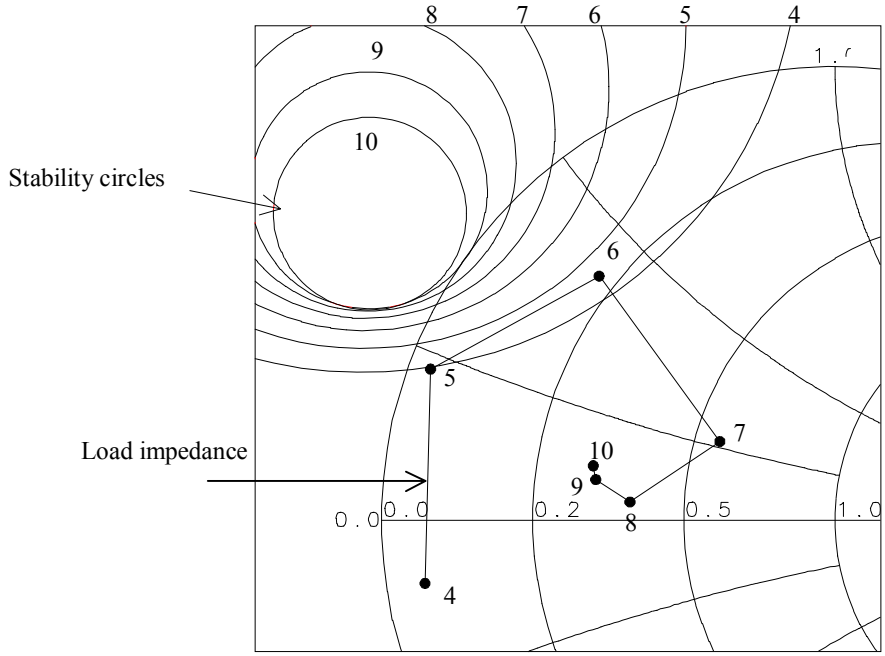

Figure 5.26: Output stability circles of a 2.16 mm HFET (48 fingers with W_U = 45 µm) at V_{DS} = 8 V and V_{GS} = -0.3 V and the reflection coefficient of the output-matching network. The bold numbers indicated the simulated frequency points in GHz.

The results depicted in figure 5.26 show that below 9 GHz the given transistor is conditionally stable because in that case the stability circles fall partially inside the depicted Smith chart. In this case, the transistor is stable outside the stability circles. The results also show that the transistor becomes unstable for more load impedances when the frequency becomes lower. These frequencies are in general the major cause of concern because:

- The impedance, which the bias circuitry will present to the transistor below 1 GHz is unknown.
- The gain of the transistors is high for low frequencies.

This is a problem because it is not possible to realise sufficiently large on-chip bias decoupling capacitors. For these purpose large capacitors > 1 nF would be needed, which are not realisable on-chip. Therefore, off-chip bias decoupling circuitry has to be added to the high-power amplifier to ensure stability. For the microwave frequencies of interest, there is not a large stability margin. For five GHz the realised output load impedance almost touches the stability circles, see figure 5.26. In this case, there are two choices. The first one is to accept that the transistor is only conditional stable. An example of a design

methodology based on this approach is given in [5.40]. The second option would be to increase the *K*-factor to a value larger than one by adding some passive resistive circuitry to the transistor. The stability of a transistor can be improved by applying series or parallel feedback, or a series- or parallel- impedance at the input or the output of the transistor, see figure 5.27. In the case of high-power amplifiers, series or parallel feedback is not a real option because of the amount of gain and output power that would be lost. The options that are left are the application of a series and or parallel impedance at the input and/or the output terminals of the transistor. When this series or parallel impedance has a resistive part the stability margin can be improved as can be easily seen from the definition of the *K*-factor, see equation (5.38).

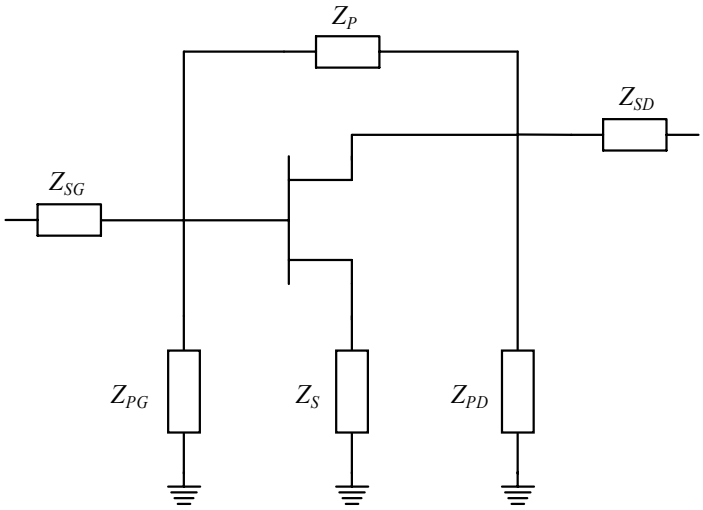

Figure 5.27: Possibilities to enhance the stability margin of a transistor.

Equation (5.38) shows that when a series or parallel impedance is added at the input of the transistor the stability of the whole is improved because the real part of the Z_{11} or Y_{11} has become larger. For the amplifiers discussed in this thesis both networks in series and parallel with the transistor have been used to enhance the stability. In figure 5.25, the improvement that can be obtained with the application of a parallel RC network in series with the input of the transistor was demonstrated. For the RC network a resistance of 25 Ω and a capacitance of 3 pF is used. The improvement in the *K*-factor comes at the price of reduced maximum available gain, as can been seen for the given example in figure 5.28. The maximum available gain is defined with the help of he following equation:

$$G_{MAX} = \frac{|S_{21}|}{|S_{12}|} \cdot \left(K - \sqrt{K^2 - 1} \right). \tag{5.41}$$

In figure 5.28 only the results between 10 and 16 GHz are shown because the maximum available gain (G_{MAX}) is only defined for a K-factor > 1, see equation (5.41). The maximum available gain reduction can be lowered by using a lower resistance value or a higher capacitance value. Both result in a higher frequency where the K-factor will become larger than one. The unconditional stable region should at least reach 500 MHz. Below this frequency, it becomes easier to apply off-chip stabilisation networks to the high-power amplifier.

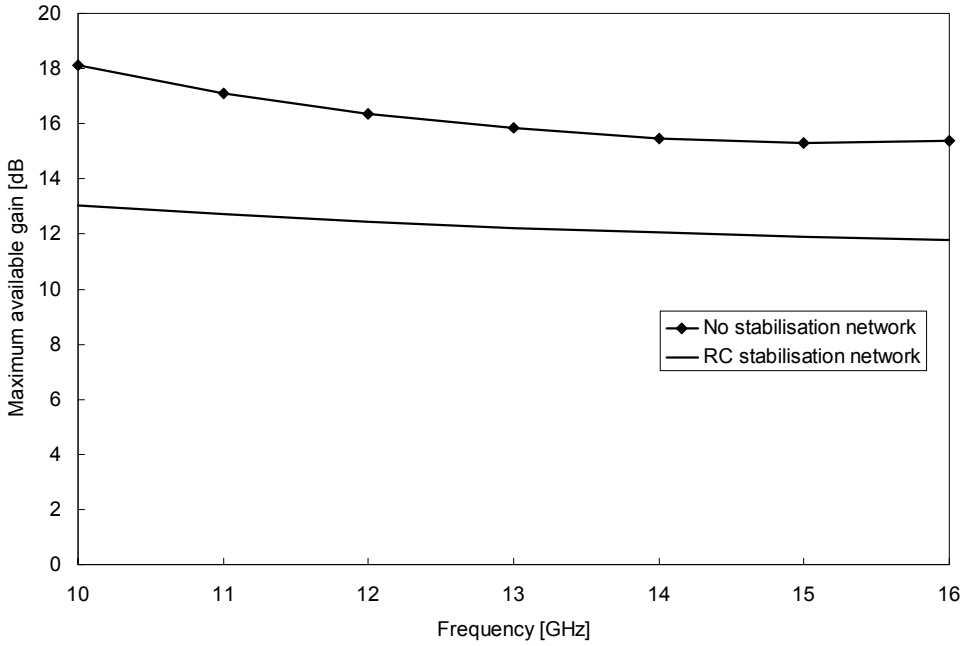

Figure 5.28: Effect of stability network on maximum available gain of a 2.16 mm HFET (48 gate fingers with a W_U = 45µ m) at V_{DS} = 8 V and V_{GS} = -0.3 V.

Application of a series network at the input of the transistor is the preferred method to stabilise the transistor for the following reasons:

- No network at the output needs be used and consequently no output power is lost in such a network.
- Realisation of Z_{SG} by a parallel RC network effectively also prevents parametric oscillation [5.41].
- This RC network is ideally suited to compensate for the frequency dependent gain role-off of the transistors, this issue is discussed in more detail in section 6.3.4.

At the start of the design, this stability analysis is performed under small signal conditions. However, under large-signal conditions the S-parameters of the transistor will change. Therefore, the stability analysis has to be repeated with the load impedances and power

levels that are present in the power amplifier. This issue will be discussed in more detail in chapter 6, where the overall stability analysis of the complete power amplifier is covered.

5.7 Unit transistor cells used in amplifier designs

5.7.1 Selected unit transistor cell sizes

The selection of the unit transistor cell sizes, used for the power amplifiers described in this thesis, is discussed in this section. The choice of a given transistor size, meaning number of gate fingers, width of the gate fingers and layout, is based on the discussions as they have been presented in the previous sections and in section 2.3.4. In the MESFET technology, power amplifiers with a targeted output power between 3 and 12 Watt have been designed. For the HFET technology, power amplifiers with a targeted output power between 5 and 10 Watt have been designed. The choice of transistor cells is based on the large-signal performance measured with the load-pull measurement system discussed in section 3.3.3. The equations that are given in section 5.2 were used to determine the number of transistors used in parallel. For these calculations, a loss of 1 dB is assumed in the output-matching network and an output power variation due to process variations of 0.5 dB. There is no need to take into account a factor for temperature variations because all amplifiers are specified at T_A = 25 °C, which is the same ambient temperature as at which the load-pull measurements are performed. A summary of the load-pull measurement results of the selected unit transistor cells is listed in table 5.6.

Table 5.6: Summary load-pull measurement results of unit transistor cells used in discussed high-power amplifier designs. All measurements are performed at f = 8 GHz. The results are obtained at the load impedance that will give maximum output power.

FET	Wafer	N_{GF}	W_U [µm]	V_{DS} [V]	V_{GS} [V]	P_{OUT_2dB} [mW/mm]	$PAE_{\_2dB}$ [%]	G_{P_2dB} [dB]
1	YC201.5	12	125	9	-1.60	581	49.7	7.7
2	YI505.6	48	63	9	-1.25	562	56.2	10.0
3	YC602.24	48	83	9	-1.25	467	49.3	9.2
4	YC602.24	32	75	9	-1.25	630	54.4	8.0
5	ASYL5C	32	45	8	-0.30	816	51.9	13.2
6	ASYL5C	48	45	8	-0.30	717	47.3	13.4

The first four transistors mentioned are MESFETs and the last two mentioned are HFETs. All transistors have a fishbone layout except for the first one, which has an interdigitated layout. As mentioned before the fishbone layout will result, for higher output powers, in a smaller chip area. The listed results also show that the HFET technology has a higher output power density than the MESFET technology. Therefore, smaller transistors can be used in HFET amplifiers and consequently these amplifiers will be smaller. In addition, the

power gain of the transistors is also considerably higher for the HFET technology. Consequently, the overall performance of the amplifier with respect to power added efficiency will be better, see section 5.2. Again the results show that the power gain depends on the width of the gate finger. This is another advantage of the fishbone transistor layout, where many gate fingers with a small width are used in parallel, over the interdigitated transistor layout. The number of gate fingers chosen is the maximum before the rapid degradation of the output power of the transistors occurs, as discussed in section 5.3.3. The operating class selected for all transistors is class AB. For the 3 and 5 Watt amplifiers a gate-source voltage was selected that guaranteed the maximum power added efficiency, see figure 5.17. Later on it became clear that the gain of the last stage transistors also plays a crucial role in the overall power added efficiency of the complete amplifier, see section 5.2. Therefore, for all other amplifiers a bias point more in the direction of class A is used. This bias point has only slightly less power added efficiency but considerably higher gain.

An overview of the amplifier designs made in both MESFET and HFET technology is given in table 5.7. In this table for each amplifier is indicated which transistor unit cell is used, how many transistors in parallel are used and what the expected minimum, nominal and maximum output power will be. The calculations show that for all amplifiers under nominal conditions (P_{OUT_NOM}) the targeted output power (P_{OUT_TARGET}) can be achieved with the selected unit transistor cell and number of transistors in parallel, except for the first amplifier. For the three-watt amplifier, more transistors in parallel could have been used. This was not considered to be an option because in that case eight transistors in parallel should have been used to keep the amplifier symmetrical, see section 5.2. In addition, the resulting output power would have exceeded the target and the chip size of the amplifier would have been increased unnecessarily. An alternative would have been increasing the number of gate fingers of the transistor or the width of the gate fingers. This was not possible at that time due to the absence of suitable transistor test structures to extract a large-signal model for a transistor with a larger total gate width. Therefore, it was decided to aim at an output power that is slightly below the specification.

Table 5.7: Overview of the transistor cells used in the output stage of the realised high-power amplifiers. For the calculation of the expected output power, a loss of one dB in the output-matching network and a output power variation, due to process variations, of ± 0.5 dB is assumed.

HPA#	P_{OUT_TARGET} [W]	FET	N_{FET}	P_{OUT_MIN} [W]	P_{OUT_NOM} [W]	P_{OUT_MAX} [W]
1	3	1	4	2.46	2.77	3.10
2	5	1	8	4.43	5.54	6.20
3	7 - 10	2	8	9.61	10.80	12.10
4	10 - 12	3	8	10.52	11.82	13.24
5	5 - 7	5	8	6.65	7.47	8.37
6	9 - 10	6	8	8.76	9.84	11.02

For the majority of the amplifiers, the same transistor unit cell that is used in the output stage is also used in the other amplifier stage(s). Exceptions are amplifier #4 where transistor #4, see table 5.6, is used in the first 2 stages and amplifier #6 where transistor #5 is used in the first 2 stages. An extracted equivalent model for the optimum load impedance used in the amplifier designs is discussed in chapter 6.

5.7.2 Stability unit transistor cells

The analysis and the way to stabilise the unit transistor cells have been discussed in section 5.6. Based on these methods the stability of the selected unit transistor cells is discussed in this section. An overview of the simulated *K*-factor with and without stabilisation networks is listed in table 5.8. In this table also an overview of the used stabilisation network is given.

Table 5.8: Overview of stable frequency range of used unit transistor cells with and without stabilisation network, also the network used is indicated. The stability of the transistor is tested between 0.1 - 50 GHz.

FET	Wafer	N_{GF}	W_U [µm]	Frequency [GHz] without network K > 1 and B_1>0	Frequency [GHz] with network K > 1 and B_1>0	Stabilisation network (figure 5.29)
1	YC201.5	12	125	6.5 – 19.8	-	-
2	YI505.6	48	63	6.7 – 20.1	0.1 – 50	a)
3	YC602.24	48	83	5.6 – 17.3	0.1 – 50	a)
4	YC602.24	32	75	8.9 – 18.2	0.1 – 50	a)
5	ASYL5C	32	45	-	0.1 – 50	a) / b)
6	ASYL5C	48	45	9.1 – 16.8	0.1 – 50	a) / b)

The results show that without stabilisation networks the unit transistor cells are only unconditional stable over a limited frequency range and in one case, FET #5, not at a single frequency. For the 3 and 5-Watt amplifier designs no stabilisation networks were applied. This gave no problem for the 3-Watt design, but for the 5-Watt design, it turned out to be complicated to stabilise the amplifier under all conditions. For this reason it was decided to use stabilisation networks in all other discussed high-power amplifier designs. As stabilisation networks the ones depicted in figure 5.29 are used. Stabilisation network a) is a parallel network used both at the gate and at the drain of the transistor (Z_{PG} and Z_{PD} in figure 5.27). Stabilisation network b) is a series network used at the gate of the transistor (Z_{SG} in figure 5.27).

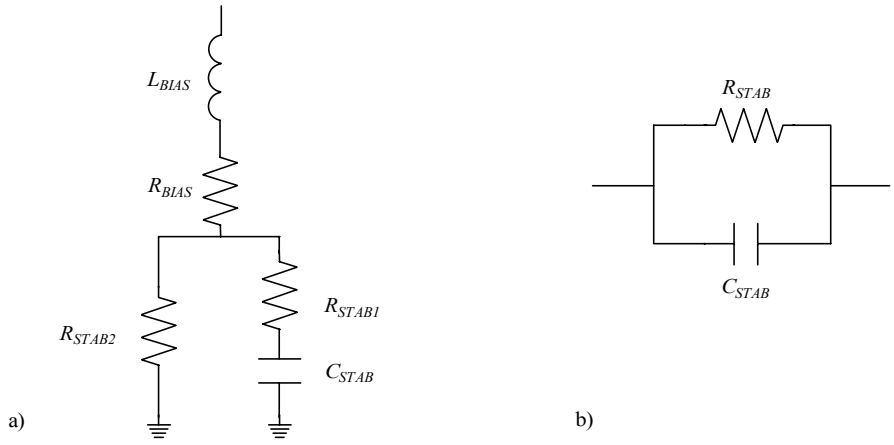

Figure 5.29: Stabilisation improvement networks.

The inductor L_{BIAS} does not enhance the stability of the transistor but is added to model that at the drain side the stabilisation network is connected at the end of the bias stub, see section 6.3. The end of the bias stub is used to ensure that in the frequency band of interest the insertion loss caused by adding of the stabilisation network will be minimal. At the gate side, no inductor is present but the biasing is done via the resistor R_{BIAS}. The resistor R_{STAB1} is added at the drain side to ensure that no parallel resonant circuits to ground that have a high quality factor will exist. For low frequencies the resistance R_{STAB2} will reduce the transistor gain and thus will improve the stability margin of the transistor. Typical values used for stabilisation network a) are listed in table 5.9.

Table 5.9: Typical range of the component values used in stabilisation network a).

	Gate side	Drain side
L_{BIAS} [nH]	0	0.5 – 2.0
R_{BIAS} [Ω]	50 – 100	0
R_{STAB1} [Ω]	0	10 – 30
R_{STAB2} [Ω]	1000	1000
C_{STAB} [pF]	5	5

For the stabilisation capacitance C_{STAB} for each network, a value of 5 pF is used. From table 5.9, it can be concluded that the value of L_{BIAS} varies strongly. This is because the stabilisation network a) is only connected to the bias stubs at the edge of the chip. Therefore, the length to the transistors is variable. This gives a problem for the transistors that are in the middle of the high-power amplifier depending on the total gate width of the transistor. For instance for the 10 – 12 Watt MESFET amplifier unconditional stable behaviour for the transistors in the middle of the amplifier was no longer guaranteed. A better solution in that case, is the application of network b). This network has the advantage that it only has to be applied at the gate side of the transistor, which is possible without any

problem. Other advantages are, as discussed in section 5.6, the fact that the network can be used to create a frequency dependent loss, which can be used to compensate for the frequency dependent gain role off of the transistor. Application of network b) also helps in suppressing odd-mode and parametric oscillations [5.41]. For these reasons, network b) is considered the preferred solution to guarantee unconditional stable behaviour of the unit transistor cells used in high-power amplifier designs. A typical value for R_{STAB} = 25 Ω and for C_{STAB} = 3 pF.

5.8 Conclusions

The selection of the amplifier topology and the size and layout of the unit transistor cell was discussed in this chapter. It was decided to use 2^n transistors in parallel, with n an integer number. This has the advantage that the design of the matching networks is simpler because the existing symmetry can be used. An additional advantage of the symmetry is that the risk of the occurrence of odd-mode oscillations is reduced. Based on simplified calculations the following crucial factors for the amplifier performance were derived:

- The loss of the matching networks should be as low as possible, especially the loss of the output-matching network.
- The power added efficiency and power gain of the output stage transistors must be high.

These requirements are better fulfilled with the HFET technology, where the maximum power added efficiency is comparable to that of the MESFET technology, with considerably higher power gain.

The output power and gain of a transistor are also influenced by the following factors:

- The width of the gate finger. It was shown that the power gain decreases rapidly as the width of the finger is increased. On basis of a theoretical model, a maximum gate width of 125 μm was found. For this gate width, a power gain reduction of one dB is found. In practice, even more gain reduction is observed. Therefore, it was concluded that the unit gate width should be as small as possible. Consequently, transistors with a fishbone layout are the preferred choice over the transistors with an interdigitated layout. An advantage of the used fishbone layout over the interdigitated layout is the fact that four rows of gate fingers are used in parallel instead of two. Therefore, the unit gate width in a fishbone layout is only half that of an interdigitated layout. Consequently, for the same gate width the gain of the fishbone transistor is higher.
- The number of gate fingers used in parallel. For the fishbone layout load-pull measurements show, that in case more than 40 fingers are used in parallel, the output power density decreases rapidly.
- The gate-to-gate spacing. The spacing between the gate fingers influences the maximum temperature of the gate fingers. There is a direct relation between the maximum gate finger temperature and the reliability of the transistor. For both the MESFET and HFET technology, a maximum gate finger temperature of 125 °C is considered acceptable by the foundries. The thermal calculation software used is discussed and it is shown that the temperature dependency of the thermal conductivity

of GaAs can be accounted for with the help of the Kirchhoff transformation. Verification of the thermal calculations with measurements shows a good correlation. Based on the thermal calculations, a minimum gate-to-gate spacing of 30 μm is found. For the MESFET technology, a good correlation between the output power and power gain reduction as a function of temperature between the measured and calculated results is found.

The operating class used determines the output power, power gain and power added efficiency of the used unit transistor cells. It is shown that for the transistors cells, used at X-band, the drain-source capacitor already acts as a short circuit at higher harmonic frequencies. It was also argued that it is not possible to use harmonic terminations over broad frequency bands. For this reason only classes A, B and AB are considered viable options for the operating point selection. Based on both measurements and calculations performed with a simplified transistor model it was shown, that the optimum operating point for the transistors used, is a class AB operating point. A value of approximately 25% of the maximum drain current seems optimal for the used technologies. It is shown that by using the transistor in its non-linear region both the output power and power added efficiency can be increased. An optimum for the used transistors is found around the 1.5 dB compression level.

A number of different methods for the determination of the optimum load impedance are discussed. It was shown that for our purpose load-pull measurements are the most suited way to determine these values. It was also discussed that under large-signal conditions, there is a difference between the load impedance that will give maximum output power and the load impedance that will give maximum power added efficiency. For most of the amplifiers discussed in this thesis a load close to the one for maximum output power is used. This choice was made to keep the unit transistor cells as small as possible for the specified output power.

The stability of the unit transistor cells was also discussed. It was shown that the stability of a transistor can be analysed with the help of the *K*-factor. Results of this analysis show that the transistor unit cells used are only unconditionally stable. Methods to ensure unconditional stability of the unit transistor cells over a large frequency band were also discussed.

At the end of this chapter, an overview of the transistor cells used in the amplifier designs was given including the applied stabilisation networks. It was concluded that the parallel RC network at the gate of the transistor was the preferred choice for future high-power amplifier designs.

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6. High-power amplifier design

6.1 Introduction

The high-power amplifier topology, the determination of the size and the stability of the unit transistor cell, the operating class of the power amplifier and the corresponding optimum load impedance of the transistors were discussed in chapter 5. In this chapter, the remaining topics relevant for the design of a high-power amplifier are discussed.

As first topic, the design of the matching networks is discussed. The design-flow that is followed is shown in figure 6.1. After the optimum load impedance is known an equivalent circuit of the source and load impedances of the matching networks is determined. The component values are used to determine the theoretically maximum bandwidth over which the load can be matched with a specified minimum reflection coefficient. This analysis will show that for both the HFET and MESFET transistors it is possible to realise matching networks over the 8 – 12 GHz bandwidth. Both these topics will be discussed in section 6.2. As final point, a number of prototype matching networks is discussed in section 6.2. For these networks, the obtainable frequency bandwidth is determined. These prototype networks are used as starting point for the design of the matching networks as it is discussed in section 6.3. The design of the matching networks is done from the output to the input of the amplifier and is in this order therefore discussed in section 6.3. In the approach discussed, the choice how the bias is applied to the transistors is the first point that needs to be resolved before the matching network is designed. Whenever possible the bias networks are used to make the source and load impedance real at the centre frequency. After the bias network is known the matching network is designed, different methods are discussed in section 6.3. The design methods discussed in section 6.3 result in matching networks with ideal components. These ideal components must be converted into a layout. The way this can be done is discussed in section 6.4.

The second topic that will be discussed in this chapter is the overall simulation of the high-power amplifier. Problems occur due to the strong non-linear behaviour of the transistors in combination with the number of transistors used. In section 6.5 a method is discussed that enables the simulation of a complete high-power amplifier in an efficient way.

The third topic, which is discussed in section 6.6, is the effect of bias supply variations on high-power amplifier performance. An on-chip bias generation circuit is discussed which circumvents several of the problems related to bias voltage variations.

The final topic is the overall stability of the high-power amplifier. In section 6.7, the different possible oscillation modes and the way to analyse and prevent them are discussed.

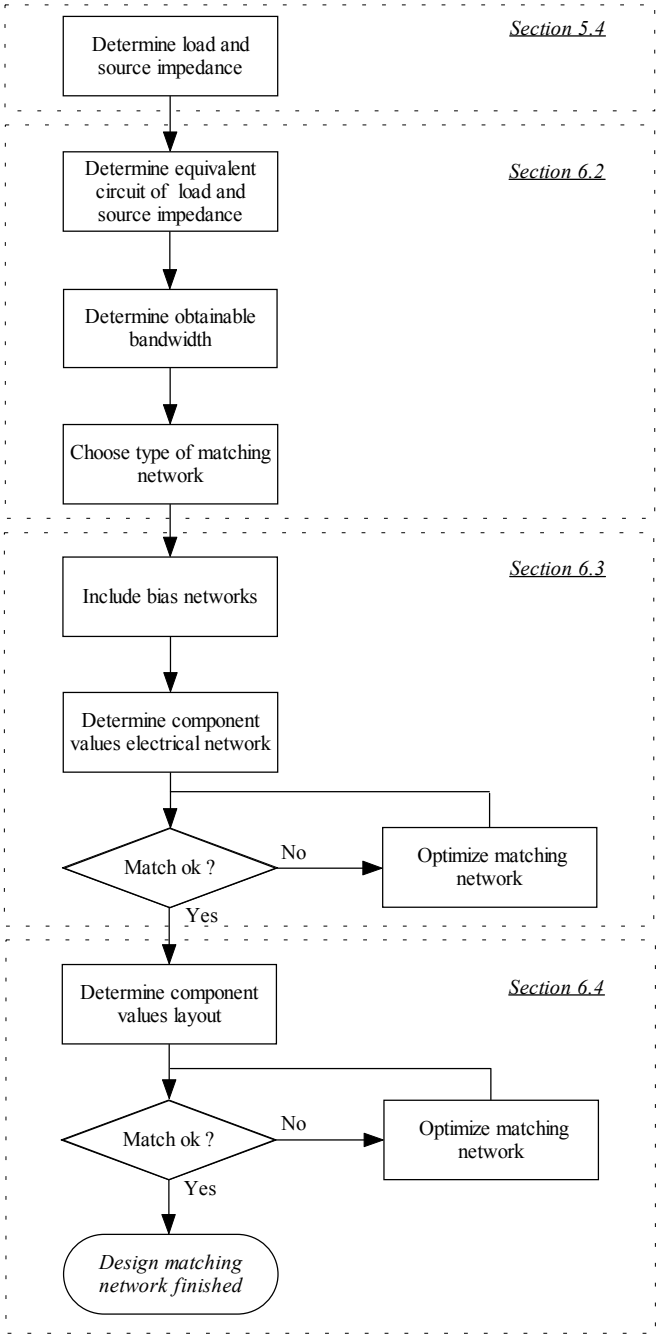

Figure 6.1: Design-flow-matching networks. For each item is indicated in which section it is discussed.

6.2 Matching network principles

6.2.1 Introduction

At this point, after the high-power amplifier topology is selected and the stability of the transistors is assured, it is time to start the design of the matching networks. The general problem that must be solved is depicted in figure 6.2. A complex source impedance must be matched to a complex load impedance. This matching must be accomplished with the help of a passive network with minimised losses. In addition, the matching network must have a prescribed frequency dependent loss to compensate for the frequency dependency of the power gain of the transistors. The losses of the matching networks consist of:

- Mismatch losses, which are caused by the fact that the realised input and output impedance of the matching network are not exactly equal to the presented load and source impedance of the matching network.
- Loss due to dissipation in the constituent components, e.g. the series resistance of a microstrip line.

In this section, a number of basic items relevant for the design of matching networks are discussed. The first item that will be discussed is the modelling of the load and source impedances. This, together with the maximum bandwidth that can be obtained when the Bode-Fano limit [6.1, 6.2] is used, will be discussed in section 6.2.2. The design of some prototype matching networks and their performance is the subject of section 6.2.3. In principle, these prototype networks are narrow-band matching networks. Nevertheless, they provide a useful starting point for the design of wideband matching networks.

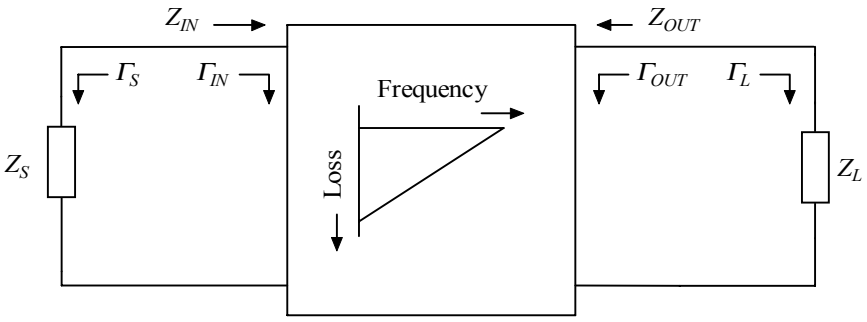

Figure 6.2: Generalised matching problem.

The input (Γ_{IN}) and the output (Γ_{OUT}) reflection coefficient, which are depicted in figure 6.2, are a measure that indicates how well the realised input and output impedance matches with the source and load impedance. The input reflection coefficient of the network depicted in figure 6.2 can be calculated with:

$$\Gamma_{IN} = \frac{Z_{IN} - Z_S^*}{Z_{IN} + Z_S}. \tag{6.1}$$

The output reflection coefficient of the network depicted in figure 6.2 can be calculated with:

$$\Gamma_{OUT} = \frac{Z_{OUT} - Z_L^*}{Z_{OUT} + Z_L}. \tag{6.2}$$

6.2.2 Wideband matching limitations

In this subsection, the wideband matching limitations are discussed. The point that has to be investigated is whether the given load and source impedances can be matched over the required frequency band. This can be done in at least three different manners as indicated by Abrie [6.3]. First of all the Bode-Fano limit can be determined [6.1, 6.2]. As a second method, the series expansion given by Youla [6.4] can be used. As a third method, the impedance can be fitted with the help of an iterative procedure like the one given by Carlin [6.5]. For the analytical techniques [6.1, 6.2 and 6.4] an equivalent circuit that fits the load impedance over the bandwidth required must be determined. This is not necessary for the iterative technique proposed by Carlin [6.5]. Nevertheless, to gain a thorough understanding of the matching problem and to investigate the frequency band limitations, the determination of the equivalent network of the load and source impedances will be discussed before that the actual matching network is designed.

All amplifiers have been realised with networks that have a source and load impedance that can be represented with the help of a 3 element network in the frequency band of interest see appendix F, or are matched to a real impedance of 50 Ω. The equivalent source and load networks are depicted in figure 6.3. The depicted source and load impedances closely follow the equivalent circuit of a transistor, as has been discussed in section 4.2. Element values for the various transistor sizes used, are listed in appendix F.

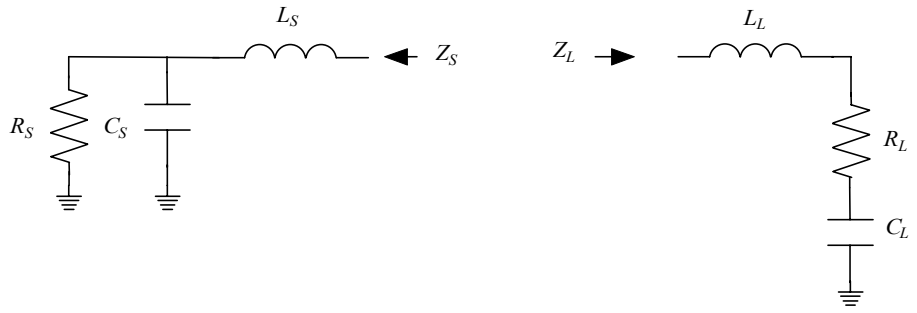

Figure 6.3: Equivalent circuit of source (left) and load impedance (right) of the matching networks.

Before the actual frequency limits of the used MESFET and HFET technology are determined, first the effect of the input impedance of the matching network on the realised output power will be discussed. A mismatch of the matching network causes a reduction of the output power that is delivered by the transistor. For an input impedance that results in a larger real part than the real part of the source impedance the following equation can be used for the calculation of the output power [6.6]:

$$P_{OUT} = \frac{\mathrm{Re}(Z_S)}{\mathrm{Re}(Z_{IN})} \cdot P_{OUTMAX} \,. \tag{6.3}$$

For the case where the real part of the input impedance (Z_{IN}) is lower than the optimum load resistance, the following equation can be used:

$$P_{OUT} = \frac{\mathrm{Re}(Z_{IN})}{\mathrm{Re}(Z_S)} \cdot P_{OUTMAX} \,. \tag{6.4}$$

The magnitude of the load reflection coefficient is given by:

$$|\Gamma_{IN}| = \sqrt{\frac{(\mathrm{Re}(Z_{IN}) - \mathrm{Re}(Z_S))^2 + (\mathrm{Im}(Z_{IN}) + \mathrm{Im}(Z_S))^2}{(\mathrm{Re}(Z_{IN}) + \mathrm{Re}(Z_S))^2 + (\mathrm{Im}(Z_{IN}) + \mathrm{Im}(Z_S))^2}} \,. \tag{6.5}$$

When the sum of the imaginary part of the input and source impedance is set to zero the worst case situation for the reflection coefficient is found which results in a maximum output power reduction. The resulting output power reduction factor N_P is than found as a function of the magnitude of the load reflection coefficient, for the situation that the real part of the input impedance is larger than the real part of the source impedance, as:

$$N_P = \frac{P_{OUT}}{P_{OUTMAX}} = \frac{1 - |\Gamma_{IN}|}{1 + |\Gamma_{IN}|} \,. \tag{6.6}$$

For the situation where the real part of the source impedance is larger than the real part of the input impedance the following equation must be used:

$$N_P = \frac{P_{OUT}}{P_{OUTMAX}} = \frac{1 + |\Gamma_{IN}|}{1 - |\Gamma_{IN}|} \,. \tag{6.7}$$

With the help of these equations, the worst-case output power reduction as a function of the magnitude of the input reflection coefficient can be calculated. The calculated worst-case output power loss as a function of the match between the load impedance required and the realised one is depicted in figure 6.4. An acceptable limit for the output power reduction is 0.5 dB. From the depicted results can be seen that the matching in that case must be better

than –25 dB. In practice, the sum of imaginary parts of the source and input impedance is not equal to zero over the frequency band of interest. Therefore, a matching criterion of better than 20 dB is used for the design of the output-matching network.

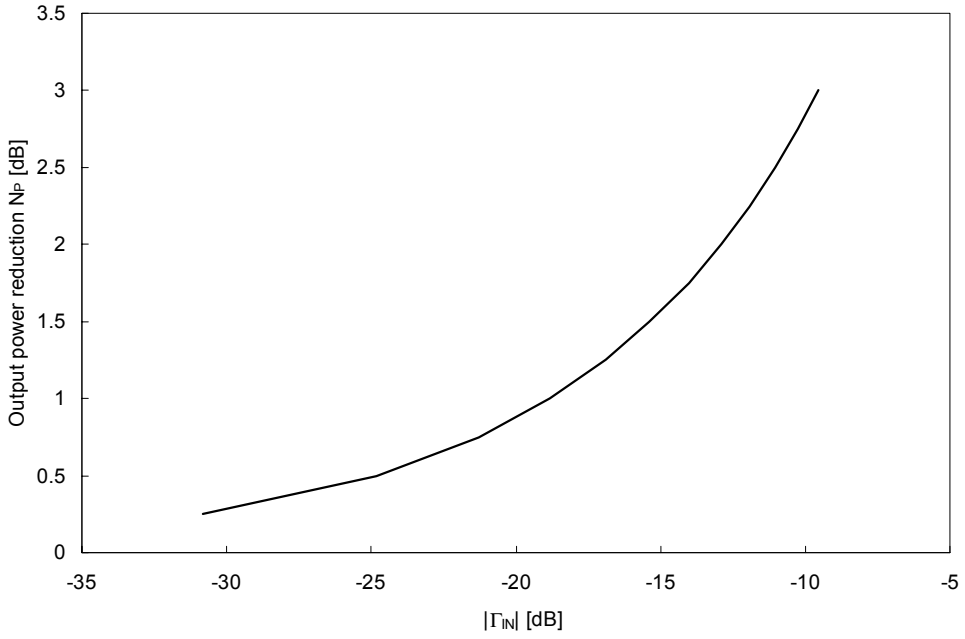

Figure 6.4: Calculated worst-case output power reduction N_P as a function of the amplitude of the source matching reflection coefficient Γ_{IN}.

The maximum bandwidth that can be obtained with a 20 dB matching can be evaluated with the help of the integral equations given by Bode and Fano [6.1, 6.2]. The equivalent circuit of the source impedance of the output-matching network is depicted in figure 6.3. The derivation of this equivalent load model is discussed in detail in appendix F. For the matching networks discussed in this thesis the series inductance is considered to be absorbed in the output-matching network. In the latter case the following integral equation due to Bode [6.1] can be used:

$$\int_0^\infty \ln\left(\frac{1}{|\Gamma_{IN}(\omega)|}\right)\cdot d\omega \;\le\; \frac{\pi}{R_S \cdot C_S}\,. \tag{6.8}$$

A derivation where also the influence of L_S is taken into account is given by Kerr [6.7]. The solution of equation (6.8) is optimal for the frequency dependency of $\Gamma_{IN}(\omega)$ depicted in figure 6.5.

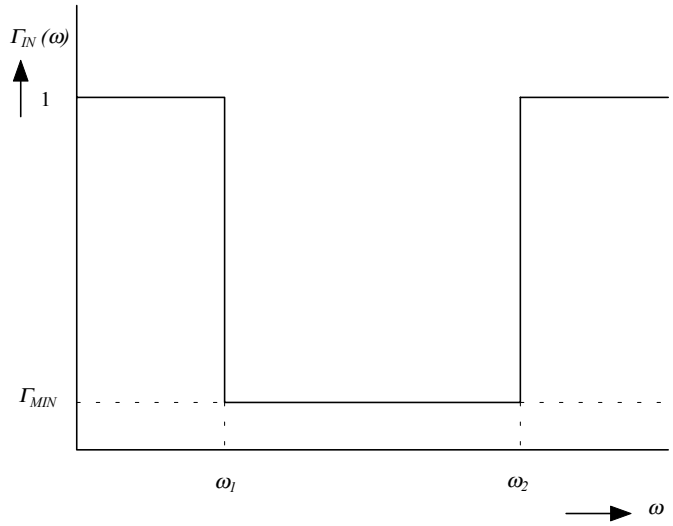

Figure 6.5: Idealised frequency dependency of $\Gamma_{IN}(\omega)$.

The solution for the depicted frequency response is given by:

$$\ln\left(\frac{1}{|\Gamma_{MIN}|}\right) = \frac{\pi}{R_S \cdot C_S \cdot (\omega_2 - \omega_1)}. \tag{6.9}$$

This equation shows the well-known trade-off between the degree of matching and the frequency band that can be matched, i.e. the better the matching the smaller the frequency band that can be matched.

In the previous part of this section it was already shown that a matching of better than 20 dB ($\Gamma_{MIN} = 0.1$) is required for obtaining a good output power. For the MESFET process the following values where found as a model for the source impedance (see appendix F): R_S = 55.1 Ω.mm and C_S = 0.299 pF/mm. With the help of equation (6.9) a maximum theoretical obtainable bandwidth of 13.2 GHz is calculated. For the HFET process the following values where found (see appendix F): R_S = 41.0 Ω.mm and C_S = 0.468 pF/mm. In this case, a theoretical bandwidth of 11.3 GHz is calculated. The theoretical bandwidth that can be obtained with the HFET technology is smaller than the one that can be obtained with the MESFET technology. This smaller bandwidth is the result of the higher value of C_S, which is more than 1.5 times larger. For both the MESFET and the HFET technology it can be concluded, that for the output-matching network, there is no problem in meeting the 4 GHz bandwidth required at X-band from a theoretical point of view.

The matching of the load impedance is less critical than the previously discussed matching of the source impedance. A mismatch will result in a power gain reduction of the matching network. This gain reduction N_G can be expressed as follows:

$$N_G = 1 - \left|\Gamma_{OUT}\right|^2 . \tag{6.10}$$

The calculated gain reduction as a function of the matching of the load reflection Γ_{OUT} is depicted in figure 6.6. The results show that indeed the matching of the load impedance is less critical than the source impedance. When a gain reduction of 0.5 dB is considered acceptable then the matching should be better than -10 dB.

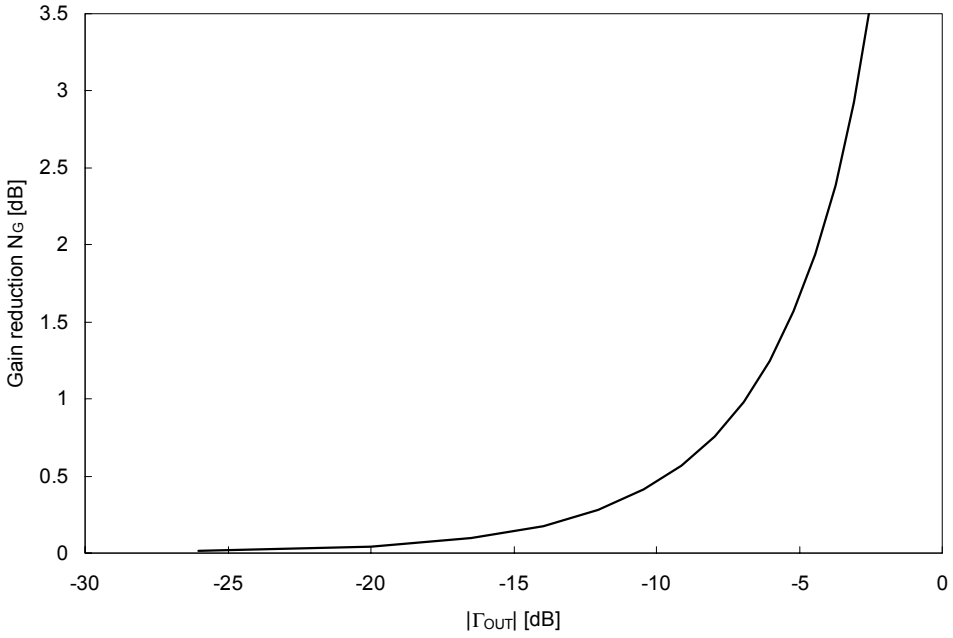

Figure 6.6: Gain reduction N_G as a function of the load matching reflection coefficient Γ_{OUT}.

The bandwidth over which the load impedance can be matched can be determined, in a similar way as the source impedance was determined, with the help of the following equations [6.2]:

$$\int_0^{\infty} \frac{1}{\omega^2} \ln\left(\frac{1}{\left|\Gamma_{OUT}(\omega)\right|}\right) \cdot d\omega \;\le\; \pi \cdot R_L \cdot C_L , \tag{6.11}$$

$$\ln\left(\frac{1}{\left|\Gamma_{MIN}\right|}\right) = \frac{\pi \cdot R_L \cdot C_L \cdot \omega_2 \cdot \omega_1}{(\omega_2 - \omega_1)} . \tag{6.12}$$

In appendix F the following typical values are found for the MESFET process: R_L = 4.9 Ω.mm and C_L = 1.243 pF/mm. With the help of equation (6.12) a minimum reflection coefficient of Γ_{MIN} = 0.056 is found for the 8 – 12 GHz frequency band. For the HFET process R_L = 2.1 Ω.mm and C_L = 2.134 pF/mm are found. These values result in a minimum reflection coefficient of Γ_{MIN} = 0.120 for the 8 - 12 GHz frequency band. These results show that the bandwidth over which the transistors can be matched with a low reflection coefficient is much lower at the input of the transistor than at the output of the transistor. The bandwidths found with equation (6.9) and equation (6.12) in theory are independent of the size of the transistor. This transistor size independence is caused by the scaling of the value of R_S and R_L, which is compensated, by the scaling of the value of C_S and C_L. In practice, however, this is not the case because it is not possible to realise loss-less components. Therefore, it is much more difficult to match a large transistor than a small transistor, see also Walker [6.8, pp. 38]. To obtain an impression with respect to the matching that can be obtained for a given frequency-slope compensation, the work of Ku and Peterson can be used [6.9].

6.2.3 Prototype matching networks

6.2.3.1 Introduction

The subject of this section is the design and performance of a number of prototype matching networks. These networks are in general, depending on the matching ratio, narrow-band solutions. The matching networks discussed are of importance for narrow-band high-power amplifier designs and they can be used as building blocks to form wideband matching networks, as discussed in section 6.3. In this section the relevant building blocks used in the high-power amplifier designs are discussed. For this discussion, it is assumed that at the centre frequency an impedance transformation will take place between two real impedances. In the approach discussed, the imaginary part of the load and source impedance are compensated, before the impedance transformation will be performed, see also section 6.3. In addition, the sensitivity of the prototype matching to component variations will be discussed.

6.2.3.2 L-type matching networks

The first two matching networks that will be discussed are the low-pass and high-pass L-type matching networks. The other two L-type matching networks, namely the one with two inductors and the one with two capacitors, are not considered here because it is not possible to transform between two real impedances with these networks. L-type matching networks are the networks with the least number of lumped components with the help of which an impedance transformation can be performed. The schematic of the low-pass and high-pass L-type matching networks is depicted in figure 6.7. For each pair of transistors placed in

parallel, one such network is used. For the amplifiers discussed in this thesis, most of the time eight transistors in parallel are used, resulting in three matching steps.

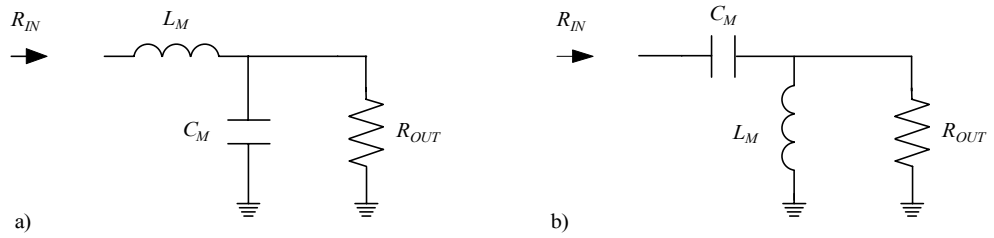

Figure 6.7: Low-pass L-type matching network (a) and high-pass L-type matching network(b).

The transformation ratio n between the input and output resistance is given as:

$$n = \frac{R_{OUT}}{R_{IN}} . \tag{6.13}$$

The element values of the low-pass matching network can, at the centre frequency f_C, be calculated with the help of the following equations:

$$C_M = \frac{1}{\omega_C \cdot R_{IN}} \cdot \sqrt{\frac{n-1}{n^2}} , \tag{6.14}$$

$$L_M = C_M \cdot n \cdot {R_{IN}}^2 . \tag{6.15}$$

Note that equation (6.14) shows, that only a larger output resistance ($n > 1$) can be transformed to a lower input resistance with the help of the depicted low-pass network. Although the before mentioned low-pass networks are very simple, still relatively large bandwidths can be matched with such a network provided that the ratio between the input and output resistance is not too large.

The matching between the required and realised input impedance is independent of both the frequency and the impedance levels as can be seen from the following equation:

$$\Gamma_{IN}(\omega) = \frac{n - 1 - \left(\frac{\omega}{\omega_C}\right)^2 \cdot (n-1)}{n + 1 - \left(\frac{\omega}{\omega_C}\right)^2 \cdot (n-1) + 2 \cdot j \cdot \left(\frac{\omega}{\omega_C}\right) \cdot \sqrt{n-1}} . \tag{6.16}$$

With the help of equation (6.16) the relative bandwidth over which a given reflection coefficient can be obtained, can be calculated as a function of the matching ratio *n*. The results of such a calculation are depicted in figure 6.8.

The results show that for a relative frequency bandwidth of 30% the matching ratio must be smaller than 3. In that case, an input reflection coefficient of 0.15 must be taken into account, which is too big, as discussed in section 6.2.2. When the required input reflection coefficient of 0.1 must be met, more than one low-pass matching network in series must be used when the matching ratio is larger than 2. The relative bandwidth depicted in figure 6.8 is defined as:

$$BW = \frac{f_H - f_L}{\sqrt{f_H \cdot f_L}} \cdot 100\% . \tag{6.17}$$

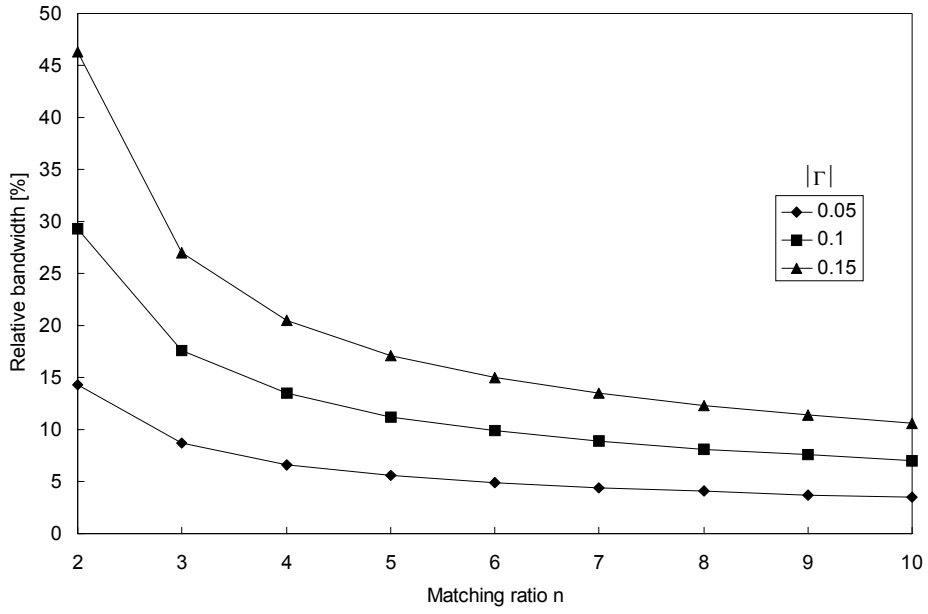

Figure 6.8: Matching of a low-pass network as a function of the magnitude of the reflection coefficient and the transformation ratio n. The results are calculated with the help of equation (6.16).

For the high-pass network depicted in figure 6.7, similar equations can be derived for the element values of the matching network:

$$C_M = \frac{1}{\omega_C \cdot R_{IN}} \cdot \sqrt{\frac{1}{n-1}}\,, \tag{6.18}$$

$$L_M = C_M \cdot n \cdot {R_{IN}}^2\,. \tag{6.19}$$

The reflection coefficient of the high-pass network can be calculated as follows:

$$\Gamma_{IN}(\omega) = \frac{n-1-\left(\frac{\omega}{\omega_C}\right)^2 \cdot (n-1)}{n-1-\left(\frac{\omega}{\omega_C}\right)^2 \cdot (n+1) + 2 \cdot j \cdot \left(\frac{\omega}{\omega_C}\right) \cdot \sqrt{n-1}}\,. \tag{6.20}$$

The relative frequency bandwidth as a function of the matching ration n that can be calculated with the help of equation (6.20) is similar to the one, which is depicted for the low-pass matching network in figure 6.8.

The low-pass and high-pass L-matching networks are sensitive to variations in the inductor and capacitor values. This variation can be expressed with the help of the following equations:

$$K_L = \frac{L_2}{L_1}\,, \tag{6.21}$$

$$K_C = \frac{C_2}{C_1}\,, \tag{6.22}$$

where K_L is the inductor variation and K_C is the capacitor variation. The original value is indicated with a one, the modified value is indicated with a two. The component variations result in both a change of the centre frequency of the matching networks and a change in the impedance transformation ratio. The modified centre frequency f_2 of a low-pass L-matching network can be expressed as a function of the required centre frequency f_1 and the component variations with the help of the following equation:

$$f_2 = f_1 \cdot \sqrt{\frac{K_C \cdot N_1 - K_L}{K_L \cdot {K_C}^2 \cdot (N_1 - 1)}}\,. \tag{6.23}$$

The modified centre frequency of a high-pass matching network is given with the following equation:

$$f_2 = f_1 \cdot \sqrt{\frac{N_1 - 1}{K_L \cdot K_C \cdot N_1 - {K_L}^2}} \,. \tag{6.24}$$

Both equations show that the modified centre frequency f_2 is also a function of the originally required impedance transformation ratio N_1. Besides the centre frequency, also the impedance transformation ratio changes. The new impedance transformation ratio N_2, can be calculated for both low- and high-pass L-matching networks, with the help of the following equation:

$$N_2 = \frac{K_C}{K_L} \cdot N_1 \,. \tag{6.25}$$

6.2.3.3 Pi-type matching networks

Impedance matching is also possible with the help of T and pi-networks instead of the before mentioned L-type matching networks. In this paragraph, only the low-pass pi-matching network will be discussed, see figure 6.9.

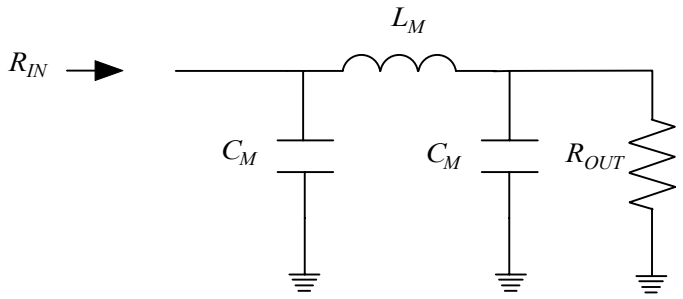

Figure 6.9: Pi impedance matching network.

The component values can be calculated at the centre frequency with the help of the following equations:

$$C_M = \frac{1}{\omega_C \cdot R_{IN} \cdot \sqrt{n}} \,, \tag{6.26}$$

$$L_M = C_M \cdot n \cdot {R_{IN}}^2 \,. \tag{6.27}$$

Depending on the value of *n* this network topology can be used to transfer the output resistance to a higher or a lower value at the input of the matching network. The amount of matching that can be reached is depicted in figure 6.10.

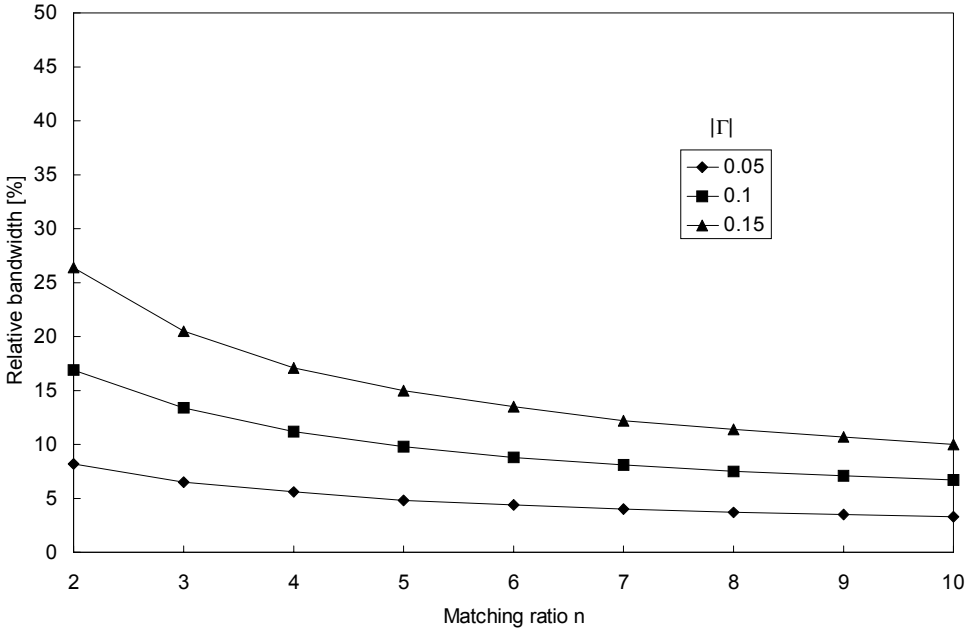

Figure 6.10: Matching of a pi-matching network as a function of the relative frequency bandwidth and the transformation ratio n. The results are calculated with the help of equation (6.28).

In this case, the matching is also independent of both the actual frequency and the actual impedance levels as can be seen from the following equation:

$$\Gamma_{IN}(\omega) = \frac{(n-1)\cdot\left(1-\left(\frac{\omega}{\omega_C}\right)^2\right) - j\cdot\left(\frac{\omega}{\omega_C}\right)\cdot\sqrt{n}\cdot\left(1-\left(\frac{\omega}{\omega_C}\right)^2\right)}{(n+1)\cdot\left(1-\left(\frac{\omega}{\omega_C}\right)^2\right) + j\cdot\left(\frac{\omega}{\omega_C}\right)\cdot\sqrt{n}\cdot\left(3-\left(\frac{\omega}{\omega_C}\right)^2\right)}. \tag{6.28}$$

The results depicted in figure 6.10 show that even less bandwidth is obtained, as was the case with the L-type low-pass network, see figure 6.8. This is caused by the fact that only at the centre frequency a real impedance is matched from the output to the input. This could also have been achieved with L-matching networks discussed in the previous chapter. Adding an additional element introduces in this case a larger frequency dependency.

Consequently, the obtainable bandwidth is reduced. In general, a broader bandwidth can be matched when more elements are used, as shown in section 6.3.

The sensitivity of the centre frequency to component variations is expressed with the help of the following equation:

$$f_2 = f_1 \cdot \sqrt{\frac{1}{K_L \cdot K_C}} \,. \tag{6.29}$$

The impedance transformation ratio at the new centre frequency f_2 can be calculated with the help of equation (6.25).

6.2.3.4 Distributed element matching networks

It is also possible to use distributed elements instead of lumped elements for the impedance matching. A well-known example is a series transmission line that has an electrical length of 90°. This type of impedance transformer has been used in cases where the series inductance of the other networks becomes too high. Then an inductor that is laid out with the help of a microstrip line, see section 4.3.4, no longer can be considered as a lumped element. In addition, the capacitors to ground become too small to be realised in an, from a modelling point of view, accurate enough way. This is the case in the last matching step of the output-matching networks discussed in this thesis. The characteristic impedance of the transmission line used for a λ/4 impedance transformer is given by the following equation:

$$Z_0 = \sqrt{R_{IN} \cdot R_{OUT}} = \sqrt{n} \cdot R_{IN} \,. \tag{6.30}$$

The obtainable reflection coefficient as a function of frequency and impedance transformation ratio n is given by the following equation:

$$\Gamma_{IN}(\omega) = \frac{n-1}{n+1+j \cdot 2 \cdot \sqrt{n} \cdot \tan\left(\frac{\pi}{2} \cdot \frac{\omega}{\omega_C}\right)} \,. \tag{6.31}$$

Equation (6.30) shows that there is a problem when this type of impedance transformer is used to transform to a low impedance, e.g. 50 Ω to 8 Ω. In that case, a characteristic impedance of 20 Ω is needed. From the characteristic impedance values given in section 2.4.1 it is clear that this value cannot be realised with the help of a microstrip line on 100 µm thick GaAs wafers. A solution to this problem is the application of shunt capacitors to ground at the input and the output of the transmission line, see figure 6.11. This solution also can be used in case the needed transmission line length becomes unacceptable long.

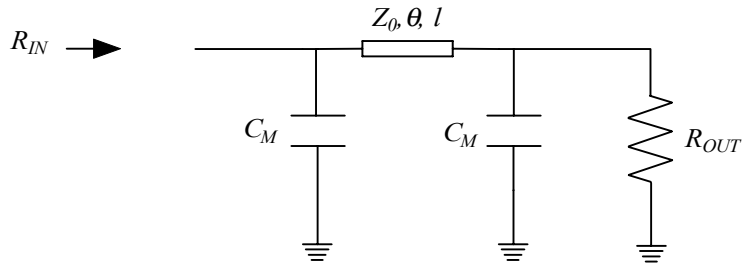

Figure 6.11: Impedance transformation realised with the help of a transmission line terminated with shunt capacitors at the input and the output.

The characteristic impedance of the transmission line can be calculated at the centre frequency with the help of the following equations:

$$Z_0 = \frac{\sqrt{n} \cdot R_{IN}}{sin\theta_C}, \tag{6.32}$$

$$C_M = \frac{1}{\omega_C \cdot Z_0 \cdot \tan\theta_C}. \tag{6.33}$$

In figure 6.12, the values that are calculated for various transmission line lengths are depicted for the before mentioned example of the 50 Ω output resistance that is transformed to 8 Ω at the input. The results are calculated for a frequency of 10 GHz. The results show the trade-off, which can be made, between the characteristic impedance and the electrical length of the transmission line. The matching of the transmission line terminated with shunt capacitors can be calculated with the help of the following equation:

$$\Gamma_{IN}(\omega) = \frac{n-1-(n-1)\cdot\left(\frac{\omega \cdot tan\theta}{\omega_C \cdot tan\theta_C}\right) - j\cdot\sqrt{n}\cdot\left(2\cdot\left(\frac{\omega}{\omega_C}\right)\cdot cos\theta_C - tan\theta\cdot\left(\frac{cos\theta_C}{tan\theta_C} + \left(\frac{\omega}{\omega_C}\right)^2\cdot\frac{sin\theta_C}{tan^2\theta_C}\right)\right)}{n+1-(n+1)\cdot\left(\frac{\omega \cdot tan\theta}{\omega_C \cdot tan\theta_C}\right) + j\cdot\sqrt{n}\cdot\left(2\cdot\left(\frac{\omega}{\omega_C}\right)\cdot cos\theta_C + tan\theta\cdot\left(\frac{1+sin^2\theta_C}{sin\theta_C} - \left(\frac{\omega}{\omega_C}\right)^2\cdot\frac{sin\theta_C}{tan^2\theta_C}\right)\right)} \tag{6.34}$$

with

$$tan\theta = tan\left(\frac{\omega}{\omega_C}\cdot\theta_C\right). \tag{6.35}$$

Equation (6.34) and equation (6.35) show that the matching in this case depends on the impedance ratio n, the relative frequency f/f_C, and the electrical length θ_C. For an electrical

length of the transmission line of 90°, equation (6.34) reduces to the one that was found for the λ/4 impedance transformer, see equation (6.31).

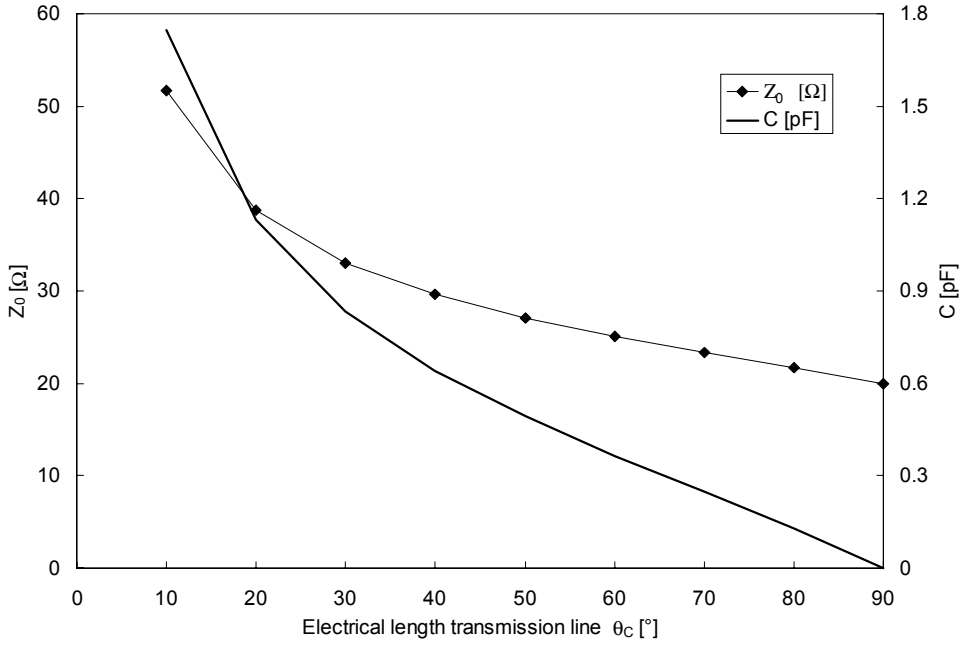

Figure 6.12: Characteristic impedance of the transmission line and value shunt capacitors as a function of the electrical length of the transmission line. The output impedance of 50 Ω is transformed to an input impedance of 8 Ω at 10 GHz.

The depicted results show that it is possible to use a transmission line shunted with capacitors for the given example. The electrical length of this transmission line has to be reduced to a value that is lower than 20° to make the characteristic impedance realisable, see section 2.4.1. For the given example in fact, one falls back to the pi-matching network that has previously been discussed. For situations where higher impedance levels are matched, as it is for instance the case for the output-matching networks, the trade-off between electrical length and shunt capacitor length is of interest. In a situation, where a physical long transmission line is undesirable, its length can be reduced with the help of shunt capacitors or one of the other previously discussed matching networks must be used.

The variation in the centre frequency of the distributed matching networks is caused by variation in the characteristic impedance of the line K_Z, a variation in the effective dielectric constant K_E and a variation of the capacitor value K_C. The first two variations are defined with the help of the following equations:

$$K_Z = \frac{Z_{02}}{Z_{01}}, \tag{6.36}$$

$$K_E = \frac{\varepsilon_{eff2}}{\varepsilon_{eff1}}. \tag{6.37}$$

The capacitor variation is defined with the help of equation (6.22). For a λ/4 impedance transformer the new centre frequency f_2 and the new impedance transformation ratio N_2 can be calculated with the help of the following equations:

$$f_2 = \frac{f_1}{\sqrt{K_E}}, \tag{6.38}$$

$$N_2 = \frac{N_1}{K_Z{}^2}. \tag{6.39}$$

In both equations, it is assumed that the characteristic impedance of the line and the effective dielectric constant of the transmission line vary independently. Although in reality this is not entirely the case, this assumption is accurate enough for the current purpose. The new centre frequency and impedance transformation ratio of the matching network formed with the help of a transmission line that is terminated with capacitors can be calculated with the help of the following equations:

$$f_2 = f_1 \cdot \frac{\tan(\theta_1)}{K_C \cdot K_Z \cdot \tan\left(\frac{f_2}{f_1} \cdot \sqrt{K_E} \cdot \theta_1\right)}, \tag{6.40}$$

$$N_2 = N_1 \cdot \frac{\sin^2(\theta_1)}{K_Z{}^2 \cdot \sin^2\left(\frac{f_2}{f_1} \cdot \sqrt{K_E} \cdot \theta_1\right)}. \tag{6.41}$$

In these equations, θ_1 is the electrical length of the transmission line.

6.2.3.5 Summary prototype matching networks

In this section, some conclusions will be drawn regarding the discussed prototype matching networks. First, we will have a look at the relative bandwidth that can be obtained with one prototype matching network. In figure 6.13 a comparison is shown for $\Gamma_{IN} = 0.1$. The results show that the transformer realised with the help of a transmission line that has an electrical length of 90° has the largest relative bandwidth. The relative bandwidth of the low-pass and

high-pass L-matching networks is the same. The bandwidth obtained with the pi-matching network and transmission line terminated with parallel capacitors is the lowest of all. In the latter case, the transmission line has an electrical length of 30°. Further reducing the electrical length to be able to increase the characteristic impedance of the transmission line would result in an even worse relative bandwidth. In summary, it can be stated that for small band matching networks the relative bandwidth decreases as the number of components of the matching network increases.

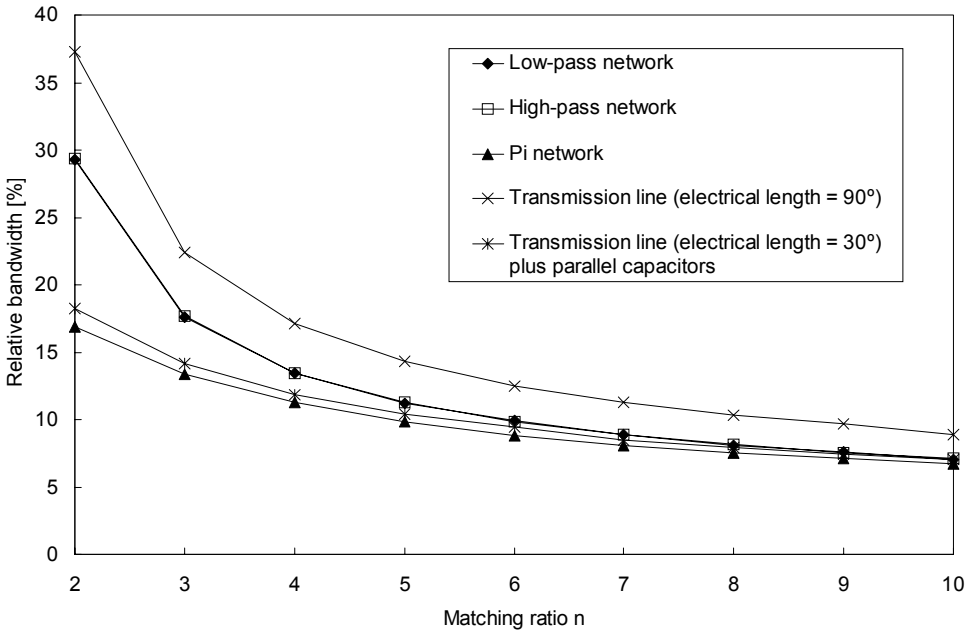

Figure 6.13: Relative bandwidth as a function of the matching ratio for Γ_{IN} = 0.1 and various prototype matching networks.

Another conclusion that can be drawn is that the relative bandwidth required of the high-power amplifiers, which is more than 30%, cannot be met with the help of only one prototype matching network. The way a larger relative bandwidth can be obtained will be discussed in section 6.3.

The next problem that needs attention is the value of the components used in the prototype matching networks. In figure 6.14, the capacitance and inductance values of the lumped matching networks are shown. It can be concluded from the depicted results that:

- The low-pass matching network will give the lowest component values.
- The component values below 3 GHz become large. Therefore, for frequencies below 3 GHz off-chip matching should be considered.
- At higher frequencies (> 20 GHz) the component values become small. Therefore, the influence of variations and modelling inaccuracies becomes larger at these frequencies.

In summary it can be stated that it is possible to realise on-chip lumped matching networks in the 3- 40 GHz frequency band. The low-pass matching network is, due to its low component values, the preferred prototype matching network.

The necessary line lengths for distributed matching networks are depicted in figure 6.15. These results show that even at 10 GHz the necessary line lengths are long (> 2.6 mm). Therefore, the use of distributed matching networks is considered an option for frequencies > 20 GHz.

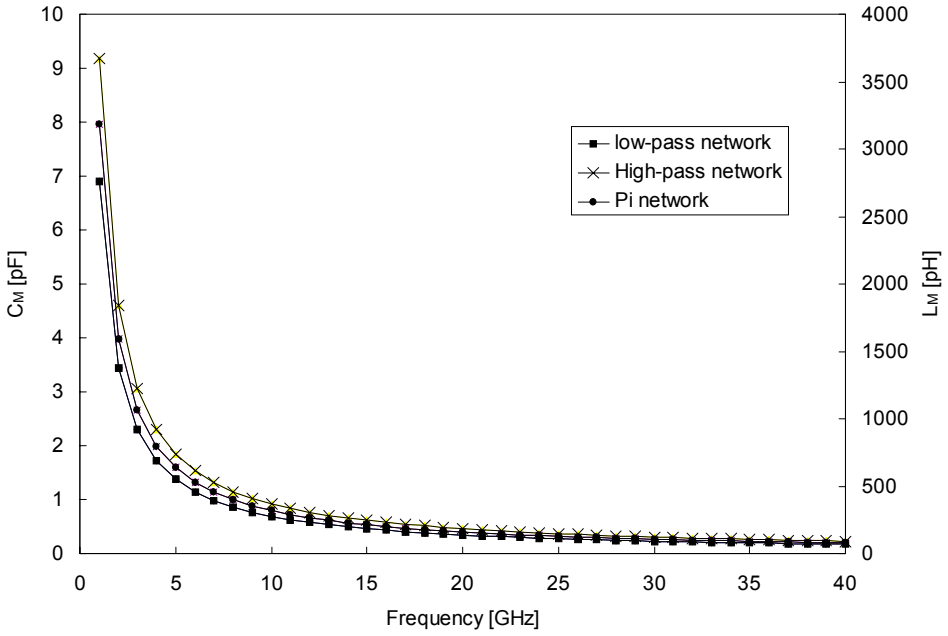

Figure 6.14: Component values of lumped prototype-matching networks. The values are calculated for an input resistance R_{IN} = 10 Ω and a matching ratio n = 4.

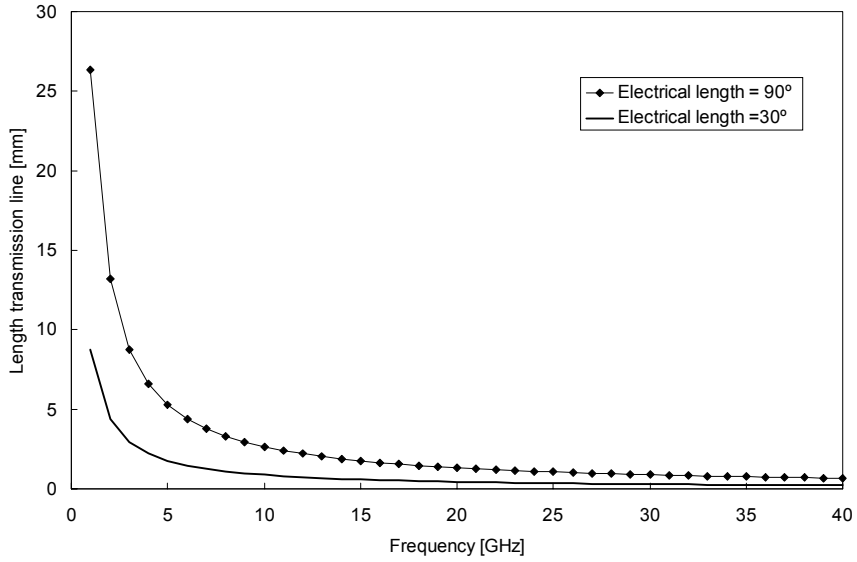

Figure 6.15: Length of transmission line of distributed prototype matching networks. The values are calculated for an input resistance R_{IN} = 10 Ω and a matching ratio n = 4, used relative dielectric constant ε_{eff} = 8.1.

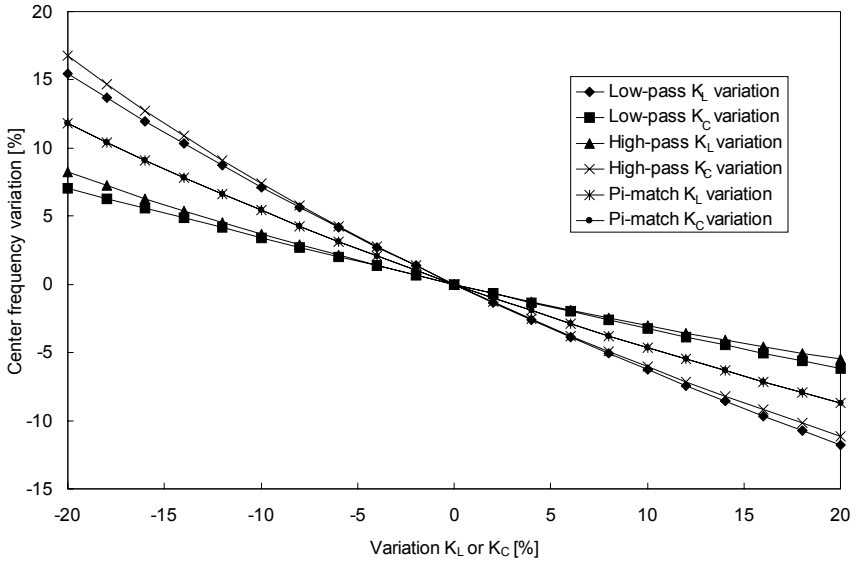

Figure 6.16: Variation centre frequency of lumped matching networks as a function of the component spread. The matching ratio N_1 = 4 is used for this calculation.

To gain a better understanding of the sensitivity of the matching networks for component spread one parameter at a time is varied. The results for the lumped matching networks are depicted in figure 6.16. The results show that the inductor variations have a larger effect on the performance of a low-pass L-matching network than capacitor variations. For high-pass matching networks, capacitor variations result in a larger variation of the centre frequency of the matching network than is the case for inductor variations. The sensitivity for capacitor and inductor variations is equal for pi-matching networks. All results are calculated for a realistic impedance ratio of four. Smaller transformation ratio will result in even larger errors. Higher transformation ratios will give similar results to the ones depicted in figure 6.16. The effect of component spread in the case of a distributed network is depicted in figure 6.17. The results show that the distributed matching networks are less sensitive to component spread, than the lumped matching networks. For inductor variations, a value of ± 7% and for capacitor variations a value of ± 15% was given in chapter 2. With the help of these numbers a maximum frequency shift (N_1 = 4) of 10.7 % for a low-pass matching network and 14.7% for a high-pass matching network can be calculated. From a point of component spread it is better to use low-pass networks instead of high-pass networks. Consequently, a frequency band, which has at both sides an overlap, must be designed. In practice, an overlap of 5% was used. The frequency shift of a distributed network is lower namely less than ± 1%.

Besides a frequency shift, also an output power loss can be observed. The results depicted in figure 6.18 show that the distributed matching networks result in a larger output power loss than the lumped matching networks.

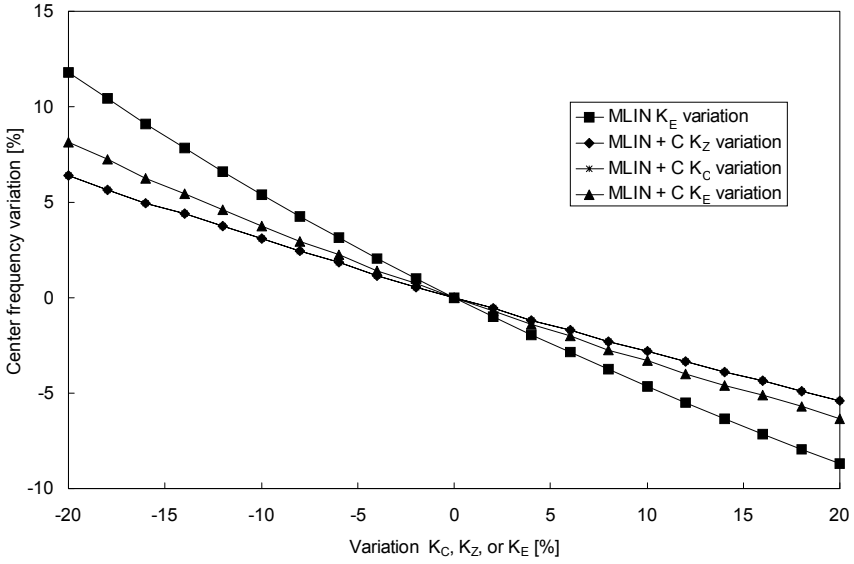

Figure 6.17: Effect of component spread on centre frequency of distributed matching networks. The microstrip line (MLIN + C) plus capacitor has an electrical length of 60°.

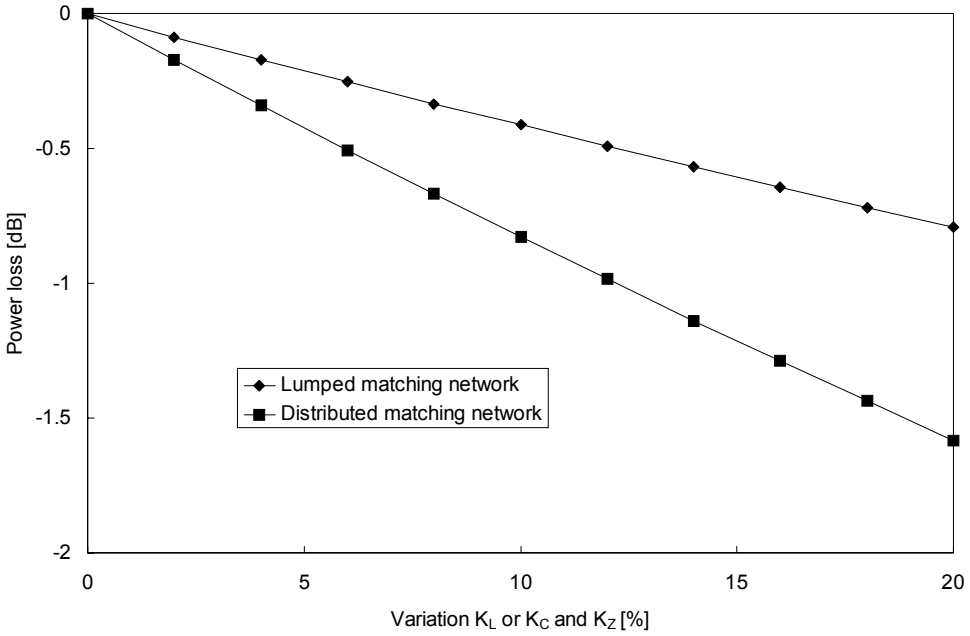

Figure 6.18: Output power loss as a function of component variations. The electrical length of the microstrip line in the distributed matching network is 90°.

6.3 Matching network design

6.3.1 Introduction

Application of the prototype matching networks discussed in the previous section and the constraints the layout poses on the realisation of the matching networks will be discussed in sections 6.3.2 to 6.3.4. In section 5.2, it was discussed that the output-matching network is the most crucial, since the performance of this network directly determines both the output power and power added efficiency of the complete high-power amplifier. Therefore, the design of the matching networks starts with the design of the output-matching network, see section 6.3.2. The realised performance of this network in combination with the output stage transistors determines the load impedance of the interstage-matching network. The source impedance used for the interstage-matching network is discussed in section 5.4 and section 5.7. After establishing the source and load impedances, the interstage-matching network is designed, as it is discussed in section 6.3.3. In a similar way, the load impedance of the input-matching network is determined. The design of the input-matching network is discussed in section 6.3.4.

6.3.2 Output-matching network design

In this section, the design of the output-matching network is discussed. As indicated in the introduction of this section the design of the matching networks is started with the output-matching network. This is necessary because information resulting from this design is needed for the other matching networks.

The output-matching network must provide the following functions:
- Present the optimum load impedance to the output of the transistor.
- Combine the output power of all transistors to the output of the amplifier with as low as possible losses.
- Provide the bias supply to the transistors.
- Provide DC decoupling to the output.

There are several different methods to realise the necessary output power combination, as for instance described by Marsh [6.10]. Only methods with minimum loss, excluding e.g. Lange couplers [6.11], have been considered in this thesis.

For all output-matching networks discussed in this thesis low-pass matching networks are used with at the input a parallel inductor to ground, which makes the load impedance real. This inductor can also be used for the supply of the bias voltages to the output of the transistors, see figure 6.19.

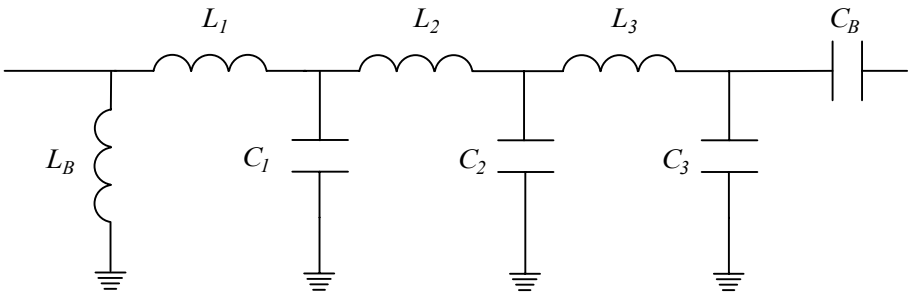

Figure 6.19: Topology of output-matching network.

A low-pass network can easily be converted into a layout, see figure 6.26. The series inductors can be used to connect the transistors in parallel in a quite natural way. The capacitor C_B is added at the output of the matching network as a DC block. This capacitor is not intended for impedance transformation. As a first step for the design of the output-matching network a narrow-band matching network design will be performed. This first step is used to get an impression of the order of magnitude of the lumped component values used and to see if these component values are realisable.

The drain biasing of the transistors needs to be taken into account from the start of the design. There are at least three ways to bias the drain, namely:

1. The use of bias resistors that have a high value, so its influence on the matching networks can be neglected. This is not a viable option for the drain-source supplies both from a point of DC power loss with as a result decreasing power added efficiency and from a point of needed level of supply voltage. As we will see in the next sections, the use of bias resistors for the gate voltage supplies in the interstage and input-matching networks is certainly an option that must be taken into account.
2. The use of a large inductor, which is put in parallel with the matching network. This inductor should have such a value that its influence on the matching network can be neglected in the frequency band of interest. To be able to neglect such an inductor at X-band a value of several nano-Henries is required. Despite the advantage that the matching network and biasing can be designed separately, this approach is not applicable due to the low current handling capability of on-chip inductors, as already discussed in section 2.4.3.
3. The use of bias stubs realised with the help of a microstrip line. These microstrip lines also have an inductive character as discussed in section 4.3.4. A disadvantage of the use of a microstrip line as an inductor is the fact that no high inductance values can be realised. Therefore, the influence of the bias stubs cannot be neglected during the design of the output-matching network. In the remainder of this section is discussed how the influence of the bias stub is incorporated in the design.

The third method has been used to supply the bias to the drain of the transistors for the amplifiers discussed in this thesis. For all the amplifiers discussed in this thesis it was decided to place the bias stub as close as possible to the output of the transistor. The reason for this choice is the fact that at this point the impedance level has its lowest value. Consequently, the influence of the off-chip bias circuitry is minimised. The bias inductor is also used to compensate for the effect of the reactive part of the source impedance (parasitic absorption), see figure 6.20.

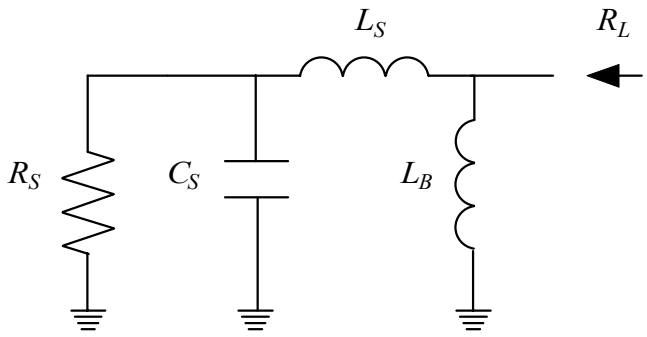

Figure 6.20: Overview source impedance and bias inductor L_B.

For the case where L_S is absent, it is very simple to calculate the value of L_B with the help of the following equation:

$$L_B = \frac{1}{\omega_C^2 \cdot C_S}, \tag{6.42}$$

in this equation, ω_C is the centre frequency of the amplifier bandwidth. Unfortunately, L_S is not zero, as can been seen from the numbers presented in appendix F. The inductance of L_S is further enlarged by the fact that the inductor L_B cannot be directly connected in parallel to the transistor. This is not possible because in that case a part of the inductor would be short-circuited by the drain feed network of the transistor. In practice, a minimum distance of 50 μm between transistor and bias stub was used for all discussed amplifiers. This extra microstrip line increases the value of L_S with approximately 20 pH, see appendix A.7.

The value of L_B when the influence of L_S is taken into account can be calculated with the help of the following equations:

$$L_B = \frac{-R_S{}^2 - \omega_C{}^4 \cdot C_S{}^2 \cdot R_S{}^2 \cdot L_S{}^2 - \omega_C{}^2 \cdot L_S{}^2 + 2 \cdot \omega_C{}^2 \cdot C_S \cdot R_S{}^2 \cdot L_S}{-\omega_C{}^2 \cdot C_S \cdot R_S{}^2 + \omega_C{}^4 \cdot C_S{}^2 \cdot R_S{}^2 \cdot L_S + \omega_C{}^2 \cdot L_S}, \tag{6.43}$$

$$R_L = \frac{\left(L_B - \omega_C{}^2 \cdot C_S \cdot L_S \cdot L_B\right) \cdot R_S}{L_S + L_B}. \tag{6.44}$$

Because of the non-zero value of L_S the required resistance R_S is also transformed by the network formed by L_S and L_B to a lower value R_L. Consequently, the matching ratio increases, and therefore the bandwidth is decreased.

The effect of L_S on both the values of L_B and R_L is shown for different transistor sizes in figure 6.21. The results are given at a frequency of 10 GHz for the average values of the MESFET process, R_S = 55.1 [Ω.mm] and C_S = 0.299 [pF/mm], as it is discussed in section 6.2.2. From the depicted results, it can be concluded that the value of the bias stub L_B increases with increasing value of L_S. The impedance R_L on the other hand becomes lower than R_S when the value of L_S increases. As an example, a transistor with a total gate width of 3 mm is chosen. A value of 60 pH is chosen for L_S, which is a reasonable assumption, see appendix F. With these values L_B becomes 317 pH and R_L = 12.16 Ω. The next step, is the further reduction of the influence of the off-chip circuitry. This is realised by placing a bias decoupling capacitor C_B at the end of the bias stub, see figure 6.22. This capacitor should have a value that is as high as possible. In practice 5 pF decoupling capacitors are used. Note that this decoupling capacitor is also needed for the necessary DC blocking, only at microwave frequencies the stub must be connected to ground.

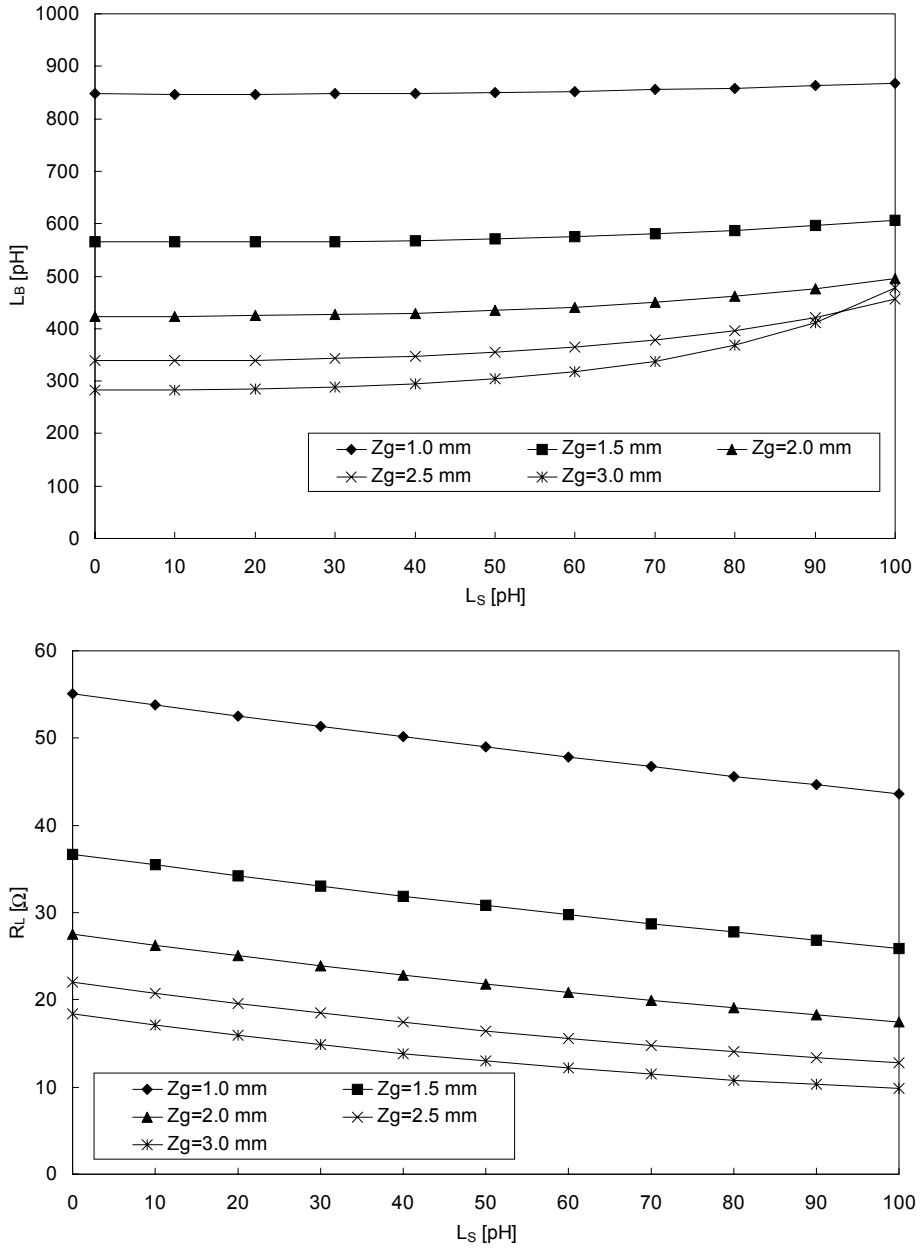

Figure 6.21: Calculated values for both L_B and R_L as a function of the value of L_S at f_C = 10 GHz for different transistor sizes (Z_g). The average values of the MESFET process, R_S = 55.1 Ω.mm and C_S = 0.299 pF/mm, as discussed in section 6.2.2, are used to perform these calculations.

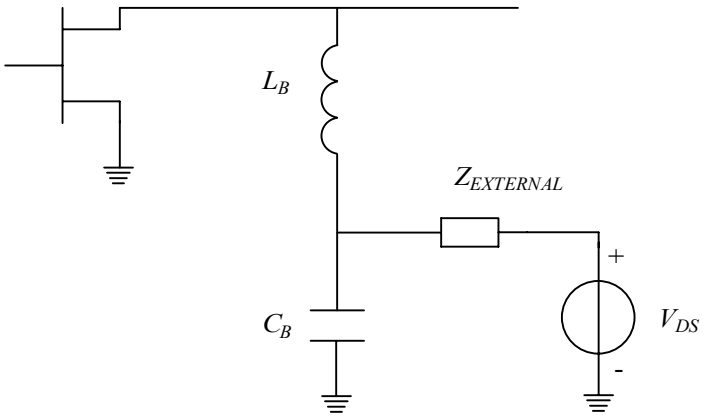

Figure 6.22: Bias decoupling output-matching network.

The use of this bias decoupling capacitor is essential because it is unknown what the value of $Z_{EXTERNAL}$ will be at microwave frequencies. At these high frequencies, it is almost impossible to take off-chip precautions because it is difficult to realise off-chip components that will work properly at microwave frequencies. The bias decoupling capacitor value is not high enough to ignore its influence on the inductance L_B. The resulting inductor value L_{BE} is reduced at the centre frequency as can be seen with the help of the following equation:

$$L_{BE} = L_B \cdot \left(1 - \frac{1}{\omega_C{}^2 \cdot L_B \cdot C_B} \right). \tag{6.45}$$

Therefore, a higher value of L_B is needed to realise the required inductance at the centre frequency. With a bias decoupling capacitor of 5 pF an inductor of 368 pH is required to realise at 10 GHz the equivalent inductance of 317 pH that was earlier mentioned.

Now before discussing the design of the remainder of the matching network, first a brief look at the layout of the bias stub. It was already stated that it would be realised with the help of a microstrip line. The question is, what are the dimensions of this line and which factors influence the choice of the dimensions. The most important selection criterion is the amount of DC current that is expected to flow through the microstrip line. It was already discussed in section 2.4.1 that the current is limited to a maximum per line width. Depending on the number of transistors used in parallel and the choice whether single side or double side biasing is allowed, the amount of DC current flowing through the bias stub can be calculated. Another factor that is of interest is the width of the line, wider lines need to become longer to realise the same inductance value as can be seen from the equation listed in appendix A.7. Therefore, from a point of efficient use of chip area it is sensible to

choose the line width in such way that its maximum current limit is being approached, of course with a sensible safety margin taken into account. When a line width of 100 µm is selected, a line length of 904 µm is needed to realise an inductance of 368 pH. The line length is calculated for a substrate thickness of 100 µm with the help of equation (A.6) given in appendix A.7.

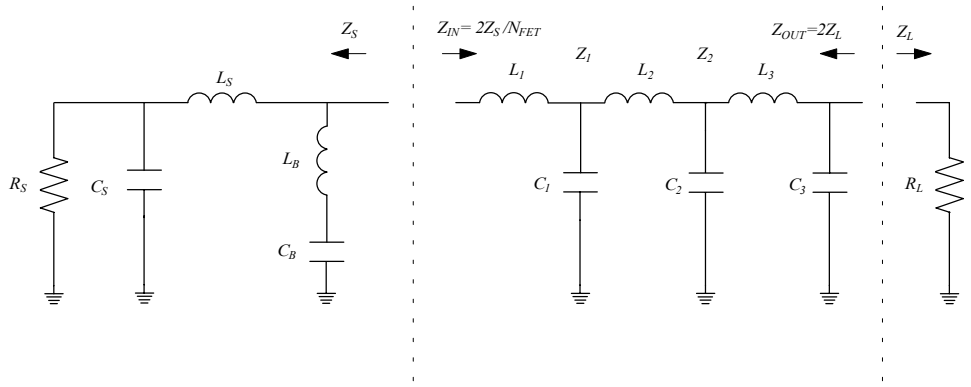

Figure 6.23: Output-matching network reduced to a two-port with the corresponding source and load impedance.

In the next step, the real impedance of 12.16 Ω will be transformed to 50 Ω at the output of the matching network. This is done, as already indicated in figure 6.19, with a low-pass matching network. The number of inputs of this matching network depends on the number of transistors used in parallel. For the amplifiers discussed in this thesis most of the time eight transistors in parallel are used. To make the electrical design of the output-matching network simpler the number of input ports is reduced to one. This is possible because the output-matching network is completely symmetrical. How this conversion of an n-port matching network to a two-port matching network is accomplished is explained in appendix E. For the current example the bias stub and the decoupling capacitor are added to the source impedance, see figure 6.23. The combination is done in a tree-like structure, see e.g. appendix E were an example is discussed. The factor 2 depicted by the source and load impedance in figure 6.23 originates from the symmetry of the matching network that is being used. Therefore, the load impedance of the output-matching network becomes 100 Ω. The influence of the DC blocking capacitor as depicted in figure 6.19 is neglected for the moment.

To determine the component values of the matching network a number of different approaches can be followed. Analytical approaches like the one described by Chen [6.12] or the real frequency matching technique described by Carlin [6.5] can be used. In practice, it turned out that the approach outlined in the remainder of this section also gives acceptable results, but is more easily implemented. In the end the electrical network has to be converted to a layout. The conversion to a layout introduces parasitic components that have to be compensated for. Furthermore, it is sometimes impossible to layout parts of the matching networks due to design rules formulated by the foundry. This is discussed in more

detail in section 6.4, where the electrical circuit to layout conversion is discussed. The limitations mentioned before make a complete analytical solution very difficult and therefore at some stage in the design the use of optimisation to determine the dimensions of the components becomes unavoidable. The best that can be done in such case is to come up with starting values that are close to the optimum solution. This increases the chance that an optimum matching over the frequency bandwidth required will be found with the help of optimisation. Other advantages of the use of optimisation techniques, for the design of the output-matching network, are:

- The possibilities to change the topology of parts of the matching network, e.g. a low-pass network into a λ/4 impedance transformer.
- Dimensions of some components can be kept fixed. This is sometimes necessary due to layout constraints, e.g. the minimum distance between viaholes is reached.

The procedure that was followed to design the output-matching network is the following:

1. As already discussed the imaginary part of the source impedance is compensated for by the inductor L_B, using parasitic absorption. Inductor L_B is also used for biasing.
2. The intermediate impedance levels are determined at the centre frequency. Besides the source and load impedance of the matching network also the number of transistors used in parallel determine the impedance levels.
3. The element values of the low-pass matching networks are calculated at the centre frequency.
4. The centre frequencies, at which the element values of the low-pass matching networks are calculated, are optimised to obtain an as good as possible matching over the entire frequency band.

The last three points will now be discussed in more detail. The intermediate impedance levels are arranged in such a way that the impedance matching steps will become equal. Equal impedance matching steps will result in the maximum relative bandwidth that can be obtained for each matching step, see also the results discussed in section 6.2.3. The majority of the high-power amplifiers discussed in this thesis use eight transistors in parallel in the output stage. In all amplifiers, the matching is done with the help of three matching networks. The resulting intermediate impedance steps can be calculated in the following way:

$$\frac{Z_{IN}}{Z_1} = \frac{Z_1}{Z_2} = \frac{Z_2}{Z_{OUT}}, \tag{6.46}$$

this results in the following intermediate impedance levels:

$$Z_1 = \sqrt[3]{Z_{IN}{}^2 \cdot Z_{OUT}}, \tag{6.47}$$

$$Z_2 = \sqrt[3]{Z_{IN} \cdot Z_{OUT}{}^2}. \tag{6.48}$$

In the current example, eight transistors in parallel are combined. Due to the existing symmetry, only half of the matching network needs to be designed. The real part of the

output impedance of one transistor at the centre frequency is 12.16 Ω. This then becomes for the four transistors in parallel 3.04 Ω (note that only four branches have to be taken into account due to the existing symmetry). The output impedance of the matching network is 100 Ω. The intermediate impedance levels are easily calculated with the help of equation (6.47) and equation (6.48). For Z_1, a value of 9.74 Ω and for Z_2, a value of 31.21 Ω is found. The equations given in section 6.2.3.2 for the low-pass matching network are now used to calculate the component values at the centre frequency of 10 GHz. The result of this calculation is listed in table 6.1, as method 1. For interpretation of the real component values, one should keep in mind that there are in this case four branches in parallel. This means that the inductors of the first matching network have to be multiplied by four, for the second matching network by two and for the third matching network by one. In appendix E this multiplication factor is derived. For the capacitors, the same is valid only there the values have to be divided by instead of multiplied by the same factor.

The results of the calculated matching network is depicted in figure 6.24. The in this figure indicated input-matching reflection coefficient is calculated with the help of equation (6.1). In this equation, Z_{IN} is the simulated input impedance of the matching network. The source impedance Z_S is in this case completely real and has a value of 3.04 Ω.

Table 6.1: Calculated values components output-matching network.

	L_1 [pH]	C_1 [pF]	L_2 [pH]	C_2 [pF]	L_3 [pH]	C_3 [pF]
Method 1	72	2.43	230	0.76	737	0.24
Method 2	73	2.47	250	0.82	750	0.24
Method 3	72	3.13	305	1.00	951	0.24
Method 4	73	3.12	305	1.00	947	0.24

The results for method 1, which are depicted in figure 6.24, show that a matching of better than –20 dB is obtained over a relative bandwidth of 20%. This bandwidth is not sufficient for the amplifiers discussed in this thesis. The method used is now refined by releasing the constraint that all impedance transformations are calculated at the same centre frequency, and will be referred to as method 2. The centre frequencies of the matching networks have been optimised with the help of Libra [6.13]. The transformation ratio has been kept constant. The resulting component values are listed in table 6.1 as method 2. The obtained matching is depicted in figure 6.24. These results show that a broader bandwidth of approximately 30% is obtained. However, the maximum value of the matching is increased to –20 dB, which is almost acceptable. For the output-matching network design, a larger frequency bandwidth and a better matching are required to be able to account for process variations. Therefore as next step, method 3, both the transformation ratio and the centre frequency of the low-pass matching networks are optimised. The optimisation has been performed for the 7.75 – 12.25 GHz bandwidth. The results, as depicted in figure 6.24, show that a significant improvement is obtained over the two before mentioned methods. With the help of this optimisation, a bandwidth of more than 45% is obtained that has a matching better than –24 dB. This result is good enough for realising the output load impedance as discussed in the previous section, see the results depicted in figure 6.4. The

results determined with method 3 are obtained with the help of an optimisation of the low-pass matching networks with the help of the optimiser available in Libra.

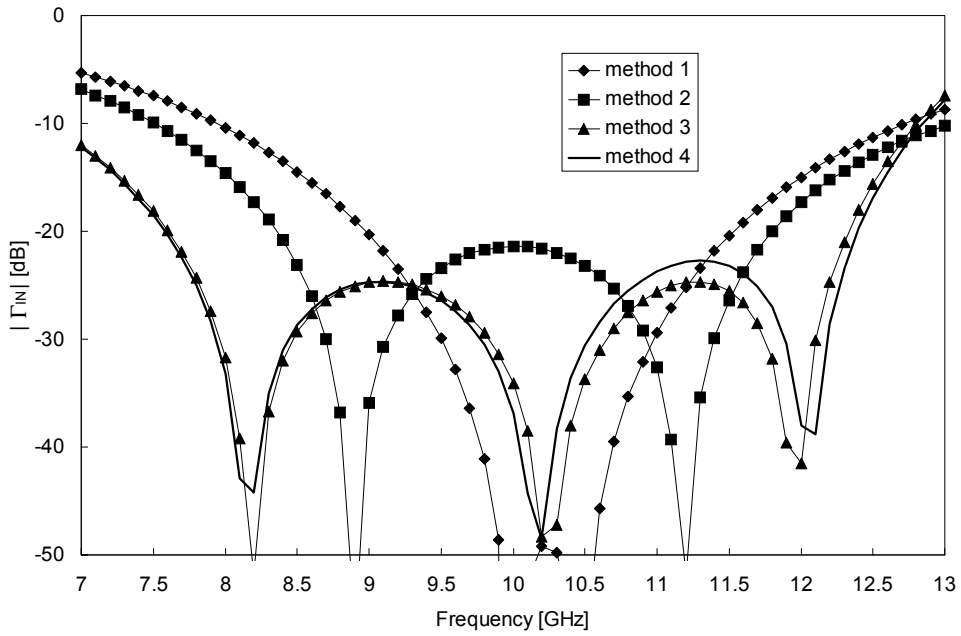

Figure 6.24: Comparison of calculated results of different matching methods.

The question arises if it is possible to obtain better results when a pure analytical approach would have been used to calculate the element values. An overview of a number of wideband matching approaches based on the work of Fano [6.2] is given by Cuthbert [6.14]. A synthesis method to match a complex load to a real impedance was given by Cottee and Joines [6.15]. They present a method that optimises the performance of L-type matching networks over a given frequency band. Zhu and Chen [6.16] have derived equations that allow the direct calculation of the component values of a network that matches two real impedances. These equations were used to calculate the element values of the matching network depicted in figure 6.23. The results of this matching network are also depicted in figure 6.24. They are indicated as method 4. The value of the calculated element values is listed in table 6.1. The results of method 3 and 4 are nearly identical. Therefore, it can be concluded that in this case also the maximum obtainable matching is achieved with the help of optimisation. The global optimum was reached, in this case, due to the fact that good starting values were obtained by first calculating the element values of the low-pass matching networks at the centre frequency with method 1. The calculated element values are already relatively close to their optimum values as can be seen from the values listed in table 6.1.

The question arises why not always use synthesis methods as the ones discussed by Cuthbert [6.14]. The reason for this is the fact that quick solutions are obtained for simple low-pass matching networks. Nevertheless, the situation becomes much more complex as parts of the low-pass matching networks have to be replaced when their component values are not realisable. In [6.17] a comparison is made between results obtained with the help of analytical methods and the ones obtained with the help of an optimisation based approach. As an optimisation method the "real frequency matching" technique is used [6.17]. It is shown [6.17] that analytical methods generally yield sub-optimal performance and the "real" frequency technique has superior performance. Next, it is shown that also the realisation of the component values required poses a problem for the utilisation of pure analytical techniques. Nevertheless, the analytical techniques are valuable in accessing the obtainable limits of a given matching approach as it was shown in this section.

Based on the analytical design some conclusions can be drawn about the problems that will occur when this electrical network is converted into a layout. The first conclusion is that the components of the first and second matching network seem to be realisable. This is different for the third matching step where an inductance of 947 pH and a capacitance of 0.24 pF must be realised. For a line width of 50 µm, a line length of 2318 µm is needed according to appendix A.7 to realise an inductance of 947 pH. This inductor has a parallel capacitor of 0.2 pF at both ends. This capacitance value has to be subtracted from the values listed for C_2 and C_3 in table 6.1. The resulting capacitance for C_3 of 0.04 pF is considered too small for accurate realisation with the help of an MIM capacitor, see section 2.4.4. The minimum MIM capacitance value that was allowed is 0.4 pF, see section 2.4.4. The reason is the fact that the modelling uncertainties are considered too high for lower capacitance values. An alternative for the MIM capacitor would be the use of an interdigitated capacitor. This was also rejected from a modelling accuracy point of view. Fortunately, the large line length which is needed for the realisation of the inductor is also the clue to the solution of this problem namely the use of a λ/4 transmission line impedance transformer.

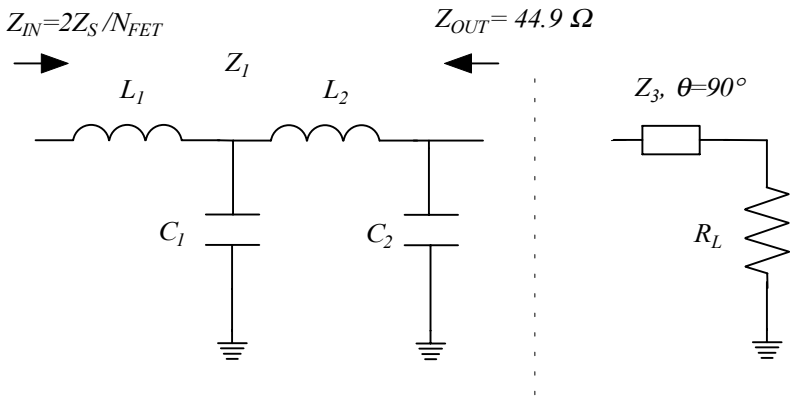

Figure 6.25: Modified output-matching network. In the last stage an impedance line transformer has been applied, that has a width of 30 µm.

The characteristic impedance of the transmission line can be calculated with the help of equation (6.30). With the help of this equation, a value of 56.2 Ω is found. The corresponding line width is approximately 50 µm, see figure 2.13. When this line width is inconvenient, because e.g. it takes to much space in the layout, it is also very simple to change its width. As an example the line width is changed to 30 µm the corresponding, characteristic impedance is 67 Ω. The component values of the resulting two low-pass sections have to be recalculated see figure 6.25. Note that the load impedance R_L = 100 Ω. First, the intermediate impedance level Z_1 must be determined. This is done with the help of the following equation:

$$\frac{Z_{IN}}{Z_1} = \frac{Z_1}{Z_{OUT}} \Rightarrow Z_1 = \sqrt{Z_{IN} \cdot Z_{OUT}} \ . \tag{6.49}$$

With 3.04 Ω at the input and 44.9 Ω at the output, a value of 11.68 Ω is found for Z_1. The recalculated element values are listed in table 6.2.

Table 6.2: Calculated values components output-matching network.

L_1 [pH]	C_1 [pF]	L_2 [pH]	C_2 [pF]	Z_3 [Ω]	θ_3 [°]
82	2.30	313	0.60	67.000	90.000

At this point, it is good to note what has been accomplished here. Due to layout constrains the initial lumped low-pass matching network has been replaced by a network which combines a lumped low-pass part with a distributed transmission line impedance transformer. In addition, the impedance transformation ratios have been adapted in such way that a physical realisation of the component values is possible.

At this point in the design, the topology and component values of the output-matching network are known. As a next step, the dimensions of the layout of the used components must be determined. The procedure used for the conversion of an ideal matching network into a layout is discussed in section 6.4.

An example of the realisation of an output-matching network is shown in figure 6.26. The depicted layout is typical for almost all amplifiers that are discussed in this thesis, see chapter 7 and appendix I for the pictures of the realised amplifiers.

The first thing that is remarkable is the width of the bias inductor L_B and the position of the bias decoupling capacitor C_B. As already discussed, wide microstrip lines are needed for the realisation of the bias inductor L_B because a lot of DC current will flow through it. For the discussed output-matching network a maximum current of 2 A is expected, so a linewidth of 100 µm is chosen. The reason for the slightly odd placement of the bias decoupling capacitor is also this large DC current. For amplifiers that have a lower output power, and thus a lower DC current, the DC current is normally supplied via the top plate of the MIM

capacitor. That is not possible in this situation because the airbridges connecting the top plate of the capacitor cannot support the expected amount of DC current.

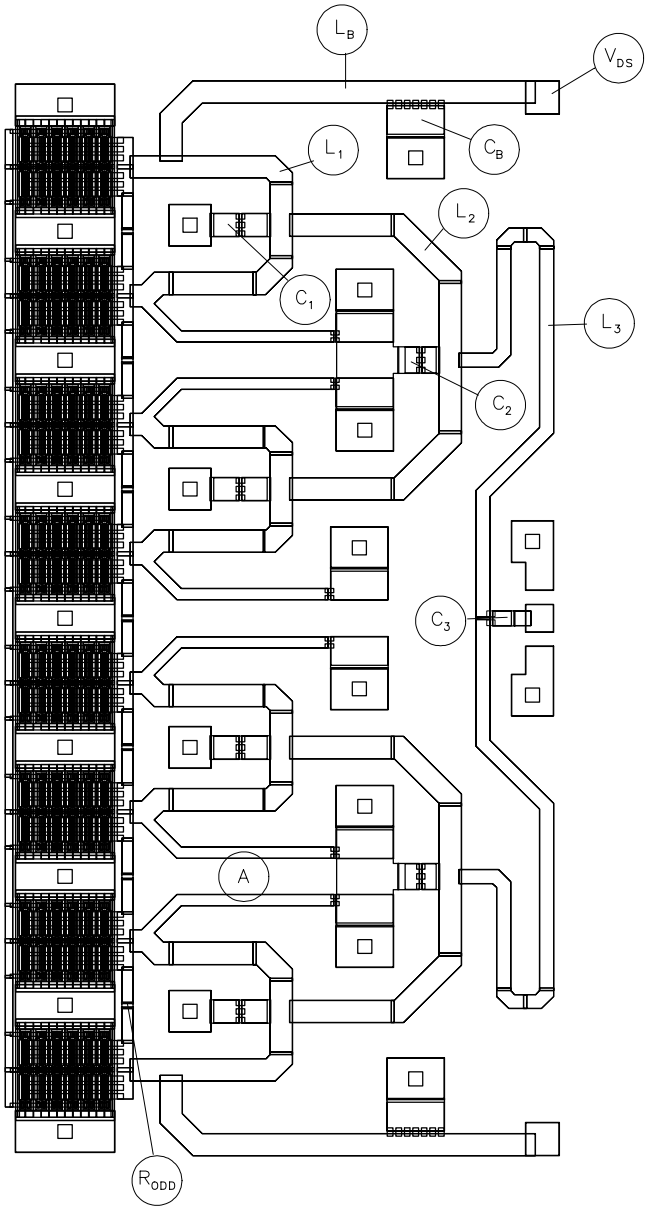

Figure 6.26: Layout of the output-matching network of the 10-Watt HFET power amplifier. This amplifier will be discussed in detail in section 7.3.

The second point that needs explanation is the use of series capacitors for the realisation of C_1 and C_2. The reason for this series capacitor is the high peak voltage at the combination points. This peak voltage in combination with the DC supply voltage easily reaches the maximum allowed value of 15 V, see also section 2.4.4. The high peak voltage V_P is caused by a combination of high output power and impedance levels, as can be seen from the following equation:

$$V_P = \sqrt{2 \cdot P_{OUT} \cdot R_{OUT}} \ . \tag{6.50}$$

The output power of the transistors depicted in figure 6.26 is approximately 1.5 W. The impedance over the capacitor C_2 is 44.9 Ω, see figure 6.25. With these values, a peak voltage of 23.2 V can be calculated. This value in combination with a DC supply voltage of 8 V, leads to a total voltage of 31.2 V, which is too high. In addition, the total voltage over capacitor C_1 is slightly too high namely 16.4 V. The solution for this problem is lowering the voltage for each capacitor by using two capacitors in series. Nevertheless, it will become a serious problem if the output power of the transistors will be further increased. In this case doubling the output power will remove the benefit reached by using two capacitors in series. There is also a potential problem for transistors based on new materials such as GaN. For these materials supply voltages of over 50 V can be used. These high supply voltages call for a redesign of the MIM capacitor with respect to the maximum voltage that may be applied to a MIM capacitor.

The third point that needs discussion is the coupling between the various microstrip lines. An explicit example hereof is indicated with A in figure 6.26. These lines must have the same impedance as the bias stubs. There are two problems with these lines. The first problem is the fact that the lines are close together. Consequently, there is electromagnetic coupling between these lines. This coupling causes both a change of the characteristic impedance of the line and a reduction of the electrical length of the line. These changes result in a wrong input impedance of these stubs, see equation (4.4). The second problem is the length of the line, which cannot become as long as the length of the bias stub, as it is clear from the layout depicted in figure 6.26. The solution to both problems is changing the characteristic impedance of the line to a higher value. Then the length of the stub can become smaller and it will fit nicely in the layout.

The fourth and last item that will be addressed here is the resistor, R_{ODD}, which is placed in between the transistors. The position of these resistors is essential for the prevention of the occurrence of odd-mode oscillations [6.18]. This subject will be discussed in detail in section 6.7.4.

At this point, the influence of modelling accuracy on the performance of the output-matching network discussed in this section will be analysed. As an example, the effect of the 45° microstrip bend model used (see section 4.3.3.1) on the total value of inductance L_1, see figure 6.26, is analysed. The Libra model predicts an inductance of ≈ 2 pH for a 100 µm bend and the model discussed in this thesis gives an equivalent inductance of ≈ 12 pH. The layout contains two of these microstrip bends. From table 6.1, can be seen that a total

inductance of 300 pH must be realised. Design of this 300 pH based on the Libra models will results in an equivalent inductance of 320 pH. The impedance transformation ratio of this matching network is 3.165. The resulting decrease in the centre frequency of the matching network, which can be calculated, with the help of equation 6.23, is 4.7%. This example again proves the necessity of the development of the microstrip discontinuity models discussed in chapter 4

6.3.3 Interstage-matching network design

The design of the interstage-matching network is the subject of this section. The interstage-matching network must perform the following functions:

- Present the optimum load impedance to the first stage transistors.
- Transport the output power of the first stage transistors to the input of the second stage transistors with a minimised loss.
- Provide bias supplies to the transistors and separate gate from drain bias.
- Optional is the possibility to compensate for the gain role-off of the transistors.

The points mentioned before are for a two-stage amplifier but the functions required are also valid for a multi-stage amplifier. In this section, a procedure for the design of an interstage-matching network will be discussed. This procedure focuses on the design of a matching network with minimised loss. The inclusion of the bias supply for the transistors is taken into account from the start. Issues involving stability will be discussed in this section. Methods for the realisation of a frequency dependent loss, which are used for the compensation of the gain roll-off of the transistors, will be discussed in the next section.

The selected transistor sizes and amplifier topology are the starting points for the design. The selection of these was discussed in detail in chapter 5. In most of the two-stage amplifiers discussed in this thesis:

- The output power of one transistor in the first stage is divided into two in the second amplifier stage.
- The same transistor size is used in both the first and the second stage.

The choice of a one to two division results in a reduction of the required chip area needed for RF matching networks because parts of the network are shared. The extra chip area that becomes available can be used for bias and oscillation suppression networks. Consequently, the overall required chip area is reduced. Another consequence of the choice mentioned before is the need for large transistors in the first stage of the amplifier.

The load impedance of the interstage-matching network is determined from a simulation of the input impedance of the second stage transistor loaded with the output-matching network discussed in the previous section. The isolation of the second stage transistors is low due to the large total gate width. Consequently, the influence of the impedance of the output-matching network on the load impedance of the interstage-matching network cannot be neglected. This is also the reason that the output-matching network is designed before the interstage-matching network. The selection of the source impedance of the interstage-matching network was discussed in detail in section 5.4.3. In practice, the source reflection

coefficient for the interstage-matching network is the conjugate of the optimum load reflection coefficient used for the output-matching network. The reason for this is the fact that the same transistor size is used. In addition, these transistors are used close to saturation due to the loss of the interstage-matching network and the relative low gain of the transistors used in the output stage. The topology depicted in figure 6.27 forms the starting point for the discussion of the design of the interstage-matching network.

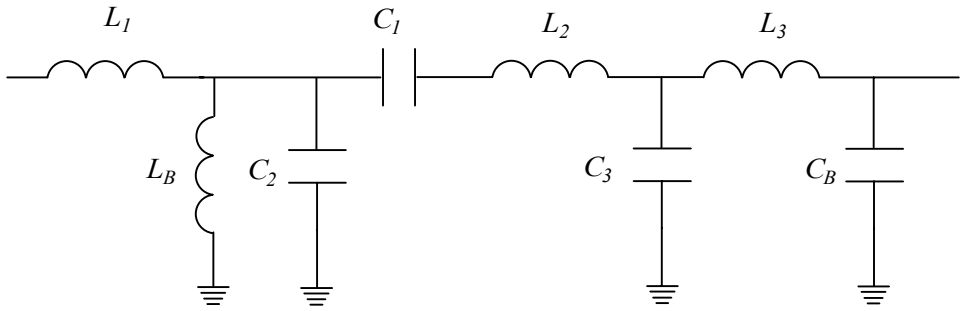

Figure 6.27: Topology interstage-matching network.

The design of the interstage-matching network is more complicated then the output-matching network because the impedance levels to be matched are much lower. The real part of the input impedance of the second stage transistor is in the order of 1 Ω. A second complicating factor is the fact that both the source and load impedance of the interstage-matching network consist of real and imaginary parts. A third difference is the DC blocking required between the drain biasing of the first stage and the gate biasing of the second stage. For this reason, the capacitor C_1 is added in the low-pass matching networks depicted in figure 6.27. The last difference is the direction of impedance transformation. For the interstage-matching network, the impedance has to be transformed to a lower value when looking from the input to the output. This is the other way around for the output-matching networks discussed in this thesis.

The same procedure, as outlined for the output-matching network, will be used to get an idea about the required component values and the level of impedance matching that can be obtained. This procedure consists of:

- Making the source and load impedance real at the centre frequency.
- Matching the resulting real impedances with the help of a low-pass matching network. Again, a low-pass matching network is chosen because two transistors in parallel in the second stage have to be connected to one transistor in the first stage. For this line length is needed, which is provided by the inductors of the low-pass matching network.

The realisation of a real impedance at the input of the matching network can be done with the help of inductor L_B. The value of L_B is calculated in a similar way as was done for the output-matching network, see equations (6.43) and (6.44). For the interstage-matching network, see figure 6.27, an additional series inductor L_1 is used to transform the real part of

the input impedance to a lower value. This improves the resulting impedance transformation ratio and less matching steps are needed. Again, as it was the case for the output-matching network, the inductor L_B is also used for the biasing of the first stage transistors. The realisation of a real impedance at the output of the interstage-matching network is more complex. The situation where the impedance is made real with the help of a parallel inductor is depicted in figure 6.28.

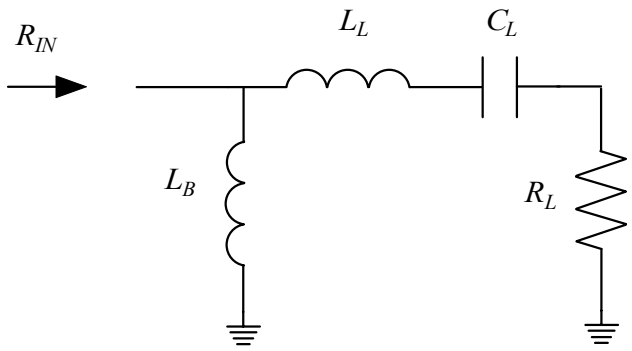

Figure 6.28: Overview of load impedance interstage plus first matching capacitor.

The value of L_B that will make the input impedance R_{IN} completely real at a given centre frequency f_C is calculated with the help of the following equation:

$$L_B = \frac{1 - 2 \cdot \omega_C{}^2 \cdot L_L \cdot C_L + \omega_C{}^4 \cdot L_L{}^2 \cdot C_L{}^2 + \omega_C{}^2 \cdot C_L{}^2 \cdot R_L{}^2}{\omega_C{}^2 \cdot C_L - \omega_C{}^4 \cdot L_L \cdot C_L{}^2}. \tag{6.51}$$

The resulting real part of the input impedance is calculated with the help of the following equation:

$$R_{IN} = \frac{L_B \cdot \left(1 - \omega_C{}^2 \cdot C_L \cdot L_L\right)}{C_L \cdot R_L}. \tag{6.52}$$

As an example, the value L_B is calculated for a MESFET that has a fishbone layout. As input parameters for this calculation the following values (appendix F) are used: R_L = 4.26 Ω.mm and C_L = 1.54 pF/mm. The calculations are performed for different values of L_L and different transistor gate widths. The result of these calculations is depicted in figure 6.29.

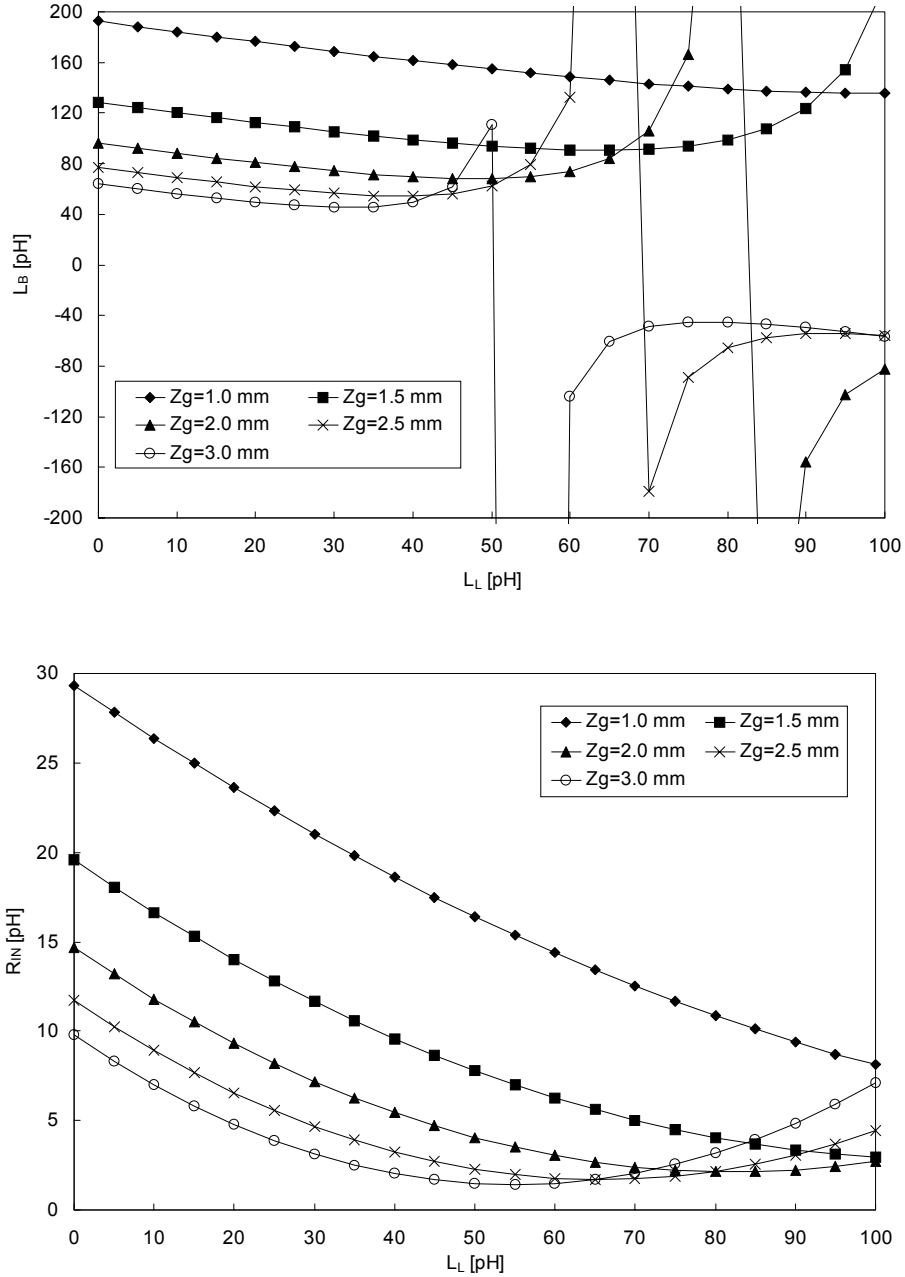

Figure 6.29: Calculated values for both L_B and R_{IN}, for different transistor sizes (Z_g), as a function of the value of L_L at f_C = 10 GHz. The following values are used R_L = 4.26 Ω.mm and C_L = 1.54 pF/mm. These values are extracted for the MESFET process as discussed in appendix F.

The result shows that the value of L_B decreases as the transistor size increases. In practice, this way to compensate for the imaginary part of the load impedance cannot be used for transistors that have a total gate width larger than 2.0 mm. For this transistor width, the inductance L_L is approximately 60 pH. This inductance value is further increased by the transmission line, which is connected in series between the bias stub and the transistor. This additional transmission line has an equivalent inductance of approximately 20 pH. For larger transistor widths the value of L_L will further increase and will resonate with the capacitor C_L in the frequency band of interest. When this happens, the input impedance of the transistor changes from capacitive to inductive behaviour. The inductance values that will result in a resonance of L_L and C_L within the frequency band of interest should be avoided. In that case the matching becomes too dependent on process variations. A better approach in that case would be to use some additional series inductance and use a capacitor instead of an inductor to make the input impedance real. This will be discussed next but first a remark regarding the value of R_{IN}. The value of R_{IN} is transformed to a higher value, which is in combination with the already discussed reduction of the source resistance resulting in a lower transformation ratio, which is beneficial for the obtainable bandwidth.

So far, we have seen that an inductor can be used to make the impedance real at the load side of the interstage-matching network. We have also seen that this approach can be applied for relatively small transistors only. For transistor sizes, where the inductance L_L starts to resonate with capacitance C_L inside the frequency band of interest, a different approach has to be used. In that case the input impedance R_{IN} is made real with the help of a capacitor C_B, see figure 6.30.

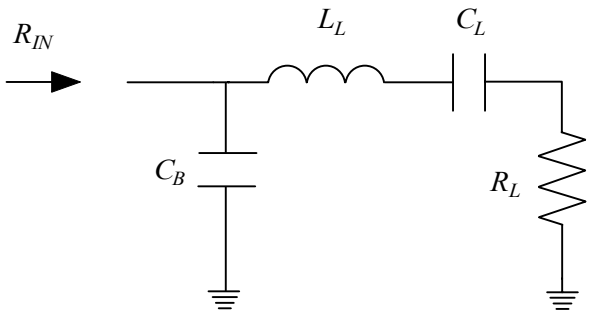

Figure 6.30: Overview of load impedance interstage plus first matching capacitor.

The value of C_B that will make the input impedance R_{IN} real at a given centre frequency f_c is calculated with the help of the following equation:

$$C_B = \frac{C_L \cdot \left(1 - \omega_C{}^2 \cdot L_L \cdot C_L\right)}{-\omega_C{}^4 \cdot L_L{}^2 \cdot C_L{}^2 - \omega_C{}^2 \cdot R_L{}^2 \cdot C_L{}^2 + 2 \cdot \omega_C{}^2 \cdot L_L \cdot C_L - 1}. \tag{6.53}$$

The resulting real part of the input impedance is calculated with the help of the following equation:

$$R_{IN} = \frac{C_L \cdot R_L}{(C_L + C_B) - \omega_C{}^2 \cdot L_L \cdot C_L \cdot C_B}. \tag{6.54}$$

As an example, the value of C_B is calculated for a MESFET that has a fishbone layout. As input parameters for this calculation the following values (appendix F) are used: R_L = 4.26 Ω.mm and C_L = 1.54 pF/mm. The calculations are performed for different values of L_L and different transistor gate widths. The result of before mentioned calculations is depicted in figure 6.31. The calculations show that a value of around 5 pF is required for a transistor with a total gate width of 3 mm. The corresponding values of R_{IN} have not been depicted here because they are similar to the ones in figure 6.29.

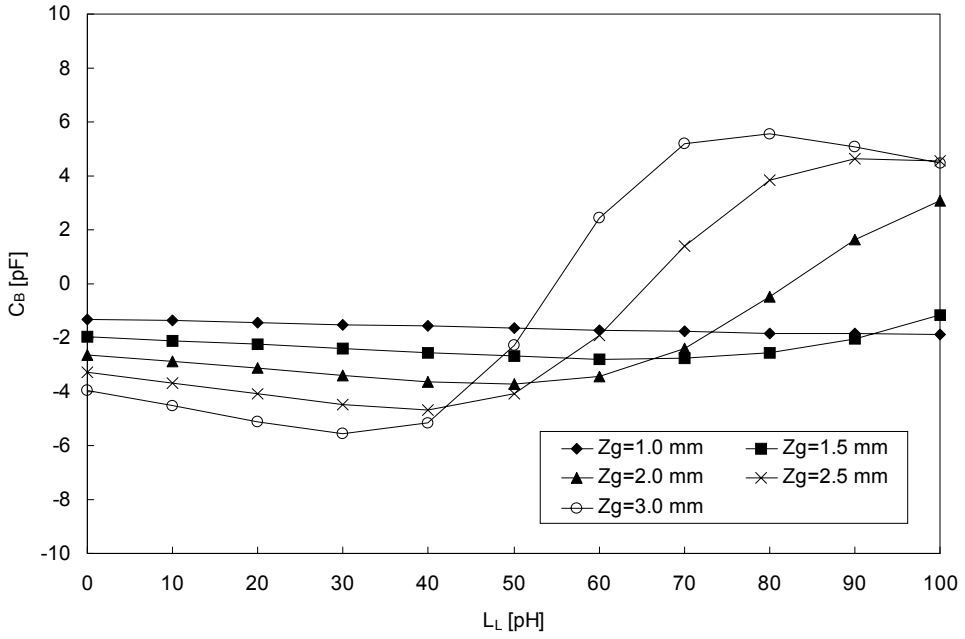

Figure 6.31: Calculated values for C_B, for different transistor sizes (Z_g), as a function of the value of L_L at f_C = 10 GHz. The following values are used R_L = 4.26 Ω.mm and C_L = 1.54 pF/mm. These values are extracted for the MESFET process as discussed in appendix F.

It is thus shown that for large transistors a capacitor must be used to make the impedance real at the output of the interstage-matching network. The use of a capacitor instead of an inductor means that a different way must be used to realise the supply of the gate voltage of

the last stage transistors. Methods that can be used for this purpose, see figure 6.32, with their advantages and disadvantages will be discussed now.

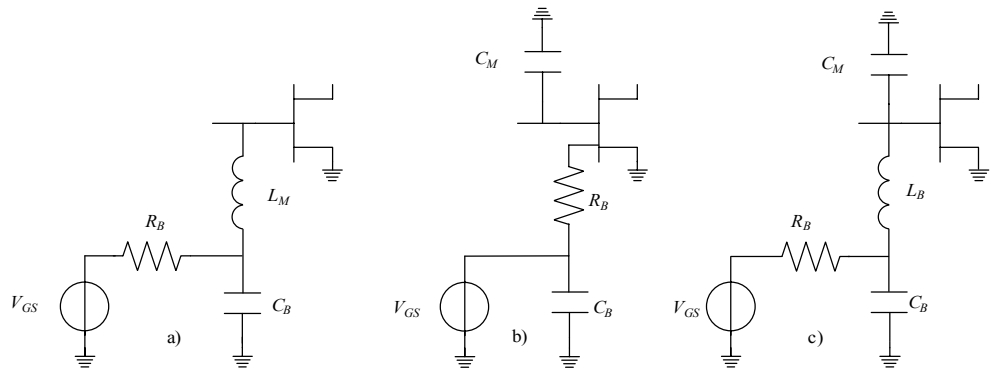

Figure 6.32: Realisation of gate biasing via interstage-matching network.

The first method, indicated with a), is the one that can only be applied for small transistors (gate width < 2 mm). The second method, indicated with b), consists of a resistor directly connected to the gate metal of the transistor. This connection is made outside the RF path. The resistor R_B should have a value that is large enough so it has only a minimal influence on the RF behaviour of the matching network. For this reason, this biasing method is only applicable for large transistors that have low input impedance. The resistor R_B is also necessary to limit the gate and drain current under large-signal conditions, this is necessary to enhance the reliability of the amplifier as discussed in section 5.5. A disadvantage of this method is the fact that the resistor R_B is connected inside the reference plane of the transistor model. Electromagnetic field simulation of the gate feed structure is needed to account for this. This is also important for the incorporation of the coupling effects between transistor and the matching elements in the simulation. Methods to perform the necessary electromagnetic field simulation are described in [6.19, 6.20]. Due to the complexity of the simulations, coupling between transistor and matching elements and the influence of elements connected inside the reference planes of the transistors, were not taken into account for the amplifiers discussed here. Nevertheless, measurement results [6.21] of various test structures showed a relevant influence between the transistors, biasing resistors and matching structures used. The third method, indicated as c) in figure 6.32, is a more elegant solution, which avoids the connection of a bias network inside the reference plane of the transistor model. In addition, the need for a bias inductor, which is also used in the RF matching network, is avoided by placing an inductor in parallel with a matching capacitor. The resulting admittance of a parallel LC circuit to ground is as follows:

$$Y_{LC} = j \cdot \omega \cdot C_M \cdot \left(1 - \frac{1}{\omega^2 \cdot L_B \cdot C_M} \right). \tag{6.55}$$

The resonant frequency of this circuit should be outside the frequency band of interest. In that case, adding an inductor will result in the reduction of the equivalent capacitor value. When a relatively large value for the bias inductor is chosen, only a slight modification to the capacitor value has to be made, to realise the required value inside the frequency band of interest. At the border of the chip there is always room to place an inductor that has a value of at least 0.5 nH. Note that there is not always place for a very large inductor (> 1 nH). Therefore, the effect of this inductor on overall capacitance value should always be taken into account.

At this point in the design of the interstage-matching network the following has been accomplished:

- The load and source impedance has been made real at the centre frequency.
- The bias supply for the transistor is integrated in the design of the matching network.

The next point that must be realised is the impedance transformation. For this the same techniques, as discussed for the output-matching network design, are used. First, we have a look at the matching ratio required. This is an indication for the number of matching sections that are needed. Then the component values of this matching network will be determined in a similar manner as it was done for the output-matching network. As a final step, the DC separation between the two bias supplies has to be realised. This can be accomplished by one of the following two methods:

- Add a series capacitor, see figure 6.27, to one of the series inductors. When a sufficiently large series capacitor is used, which resonates with the matching inductor outside the frequency band of interest only a slight modification of the matching network is necessary.
- A second option, which is also interesting from a layout point of view, is the conversion of a part of the matching network from a low-pass network into a high-pass network.

A typical example of a layout of an interstage-matching network in which all of the items discussed before have been applied, is depicted in figure 6.33. The equivalent circuit of this matching network is depicted in figure 6.34. At the input of this network a transformer formed by inductor, L_1 and L_2 can be seen. As explained earlier this transformer is used to make the source impedance real and to supply the drain voltage to the first stage transistors. At the output of the matching network, the load impedance is made real with the help of capacitor C_5. The parallel RC network formed by C_4 and R is used to make the output stage transistors unconditional stable above 0.5 GHz as already discussed in chapter 5. The impedance transformation is accomplished with the help of two low-pass matching networks formed by C_1, L_3, C_3 and L_5. The depicted capacitor C_2 is used to separate the bias supplies of the input and output stage transistors. Finally, the biasing of the output stage transistors is done with the help of inductor L_4. This biasing method was already discussed in this section as method c).

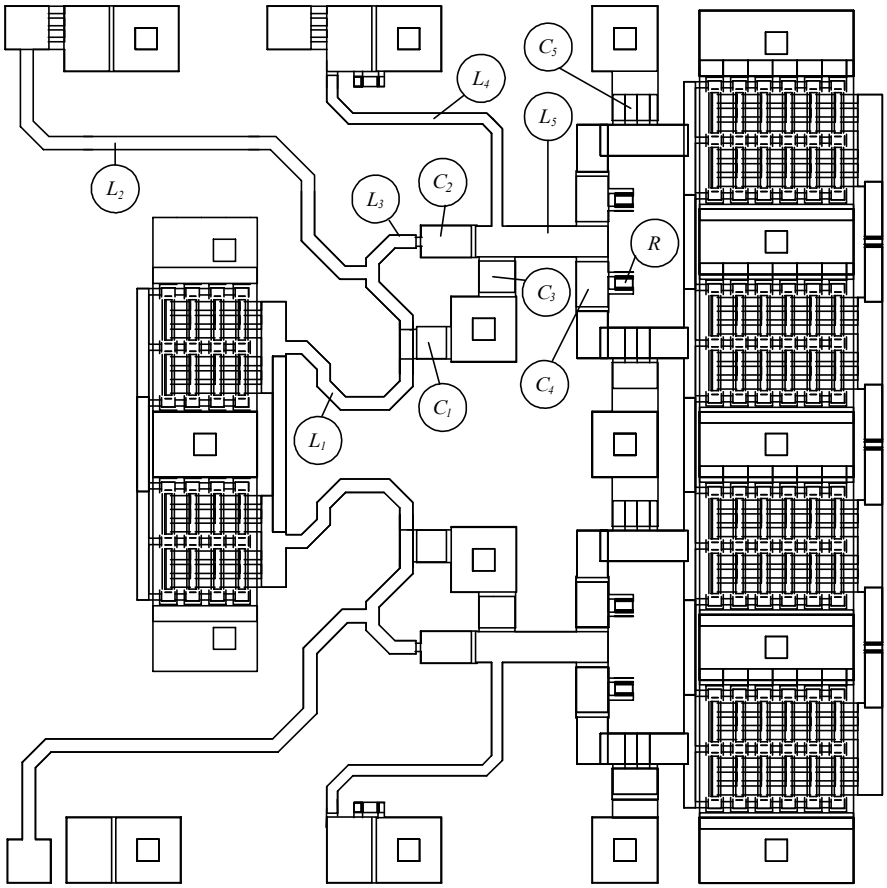

Figure 6.33: Layout of the interstage-matching network of the 10-Watt HFET power amplifier discussed in section 7.3.

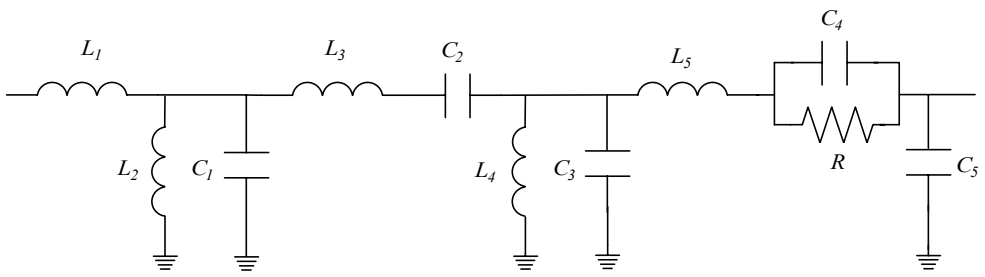

Figure 6.34: Equivalent circuit of the interstage-matching network depicted in figure 6.33.

6.3.4 Input-matching network design

The design of the input-matching network is discussed in this section. This matching network must perform the following functions:

1. Divide the power present at the input of the amplifier to the transistors of the first stage with minimised losses. The number of transistors in the first stage depends on both the number of amplifier stages and the number of transistors used in the output stage, see section 5.2.
2. Provide a compensation for the frequency dependent gain role-off of the transistors used.
3. Match the transistors to 50 Ω at the input of the amplifier.
4. Provide the gate bias supply to the first stage transistors.

Again, before the actual design of the input-matching network is started one should carefully consider how the biasing should be applied. The options that are available to solve this problem are similar to the ones discussed for the interstage-matching networks. One additional option is available for the input-matching network namely the application of a very large bias resistor, e.g. 1 kΩ. This is possible because the transistors will be used in their linear region and therefore no gate current is expected to flow. This resistor can be virtually used everywhere in the matching network. If this option is used the biasing and matching problem can be solved separately. However, care must be taken to prevent thermal runaway problems, see section 5.5.

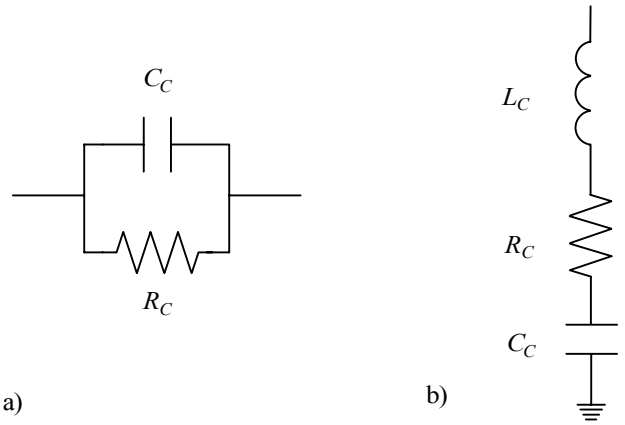

Figure 6.35: Slope compensation networks used in input-matching network.

In addition, the way the gain roll-off compensation is realised should be considered before the actual matching network is designed. In the classical matching theory, this slope compensation problem is solved by giving the input a frequency dependent mismatch. This means a high mismatch at the low end of the frequency band and no mismatch at the high end of the frequency band. This approach is not acceptable in this case due to the required input match of 50 Ω. In figure 6.35, two examples of slope compensation networks are shown.

If the use of mismatch is not acceptable, the only alternative to realise slope compensation is the introduction of dissipating elements. The frequency dependency is introduced in case a) by the parallel capacitor. This type of network is also very suitable for the enhancement of the stability of the used transistors as it was discussed in section 5.6. In the second case, the frequency dependency is introduced by a series inductance. The series capacitor shown is necessary for DC blocking in many cases. The use of resistive elements to realise the slope compensation is also helpful in releasing the required matching because they mask the mismatch loss at the input of the high-power amplifier. Of course, the use of dissipating elements comes at the price of increased loss at the highest frequency of interest of the matching network. For the high-power amplifiers with a high output power (> 5 Watt), this loss has a value between 2 and 3 dB.

The design of the input-matching network is similar to that of the interstage-matching network, except for the source impedance, which is real. Another difference is the increased impedance transformation ratio. The transformation ratio is higher because the resistive part of the source impedance is higher for the input-matching network. This input impedance is 50 Ω, resulting in an input impedance of 100 Ω, compared to 27 Ω for a 2 mm DIOM20HP MESFET used in the interstage-matching network. In addition, as it is the case for a two-stage amplifier, two transistors are combined in parallel, which will lower the load impedance with a factor of two and increase the transformation ratio with a factor of two. The latter point is not an issue for the three and four stage amplifiers discussed in this thesis where only one transistor per amplifier half is used.

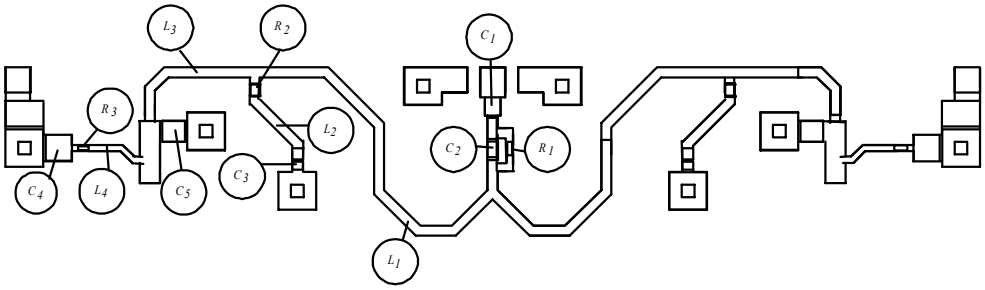

Figure 6.36: Layout of the input-matching network of the 10-Watt HFET amplifier discussed in section 7.3.

The layout of the input-matching network of the HFET high-power amplifier is depicted in figure 6.36.

The equivalent circuit of this input-matching network is depicted in figure 6.37. Again, the capacitor C_5 is used to make the load impedance real. At the source side capacitor, C_1 acts as DC blocking capacitor. The parallel RC network formed by R_1 and C_2 is used to create a frequency dependent slope in the matching network. The resistive part is also used to improve the matching of the high-power amplifier by masking the mismatch losses in the

matching network. The impedance matching has been accomplished here with the help of two impedance transformers formed by the inductors L_1, L_2, L_3 and L_4. The resistors R_2 and R_3 are added to increase the slope of the frequency dependent loss of the input-matching network. The capacitors C_3 and C_4 are mainly added for DC blocking. The gate voltage of the transistor is supplied via the top plate of capacitor C_4.

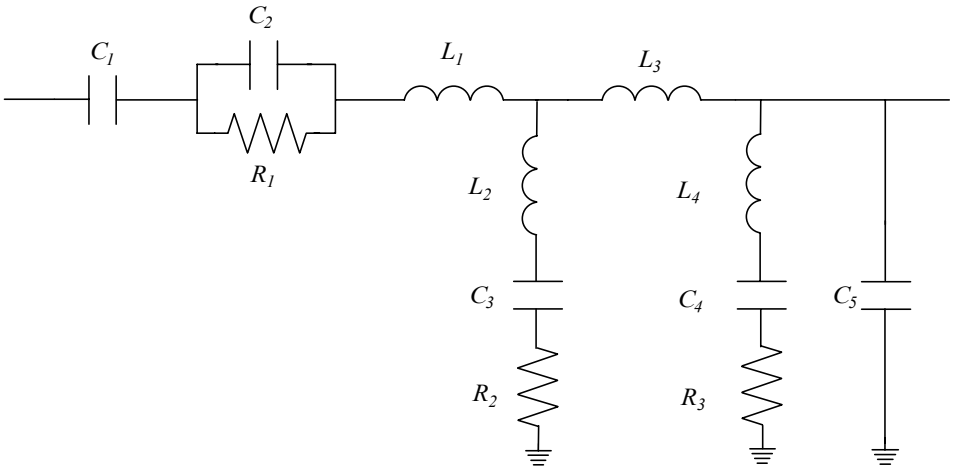

Figure 6.37: Equivalent circuit of the layout of the input-matching network depicted in figure 6.36.

The network described before is the one that was used for the 10-Watt HFET amplifier discussed in the next chapter. This matching network made use of two L-type matching networks that consist of a series inductor and a parallel inductor. The advantage of these networks is the ability to realise large slope compensation by placing resistors in series with the parallel inductors. For the other amplifiers discussed in this thesis the slope compensation was divided over the input and the interstage-matching networks. In the latter case, often the matching network depicted in figure 6.38 was used, in appendix I some examples have been shown. The blocking capacitor C_1 and the parallel RC network have the same function as it was already discussed before. The load impedance is made real with the help of capacitor C_4. Note, that for smaller transistors, this capacitor is replaced by a parallel inductor, see the previous section. The resulting real impedances are transformed with the help of a λ/4 impedance transformer in combination with a low-pass matching network. Similar as it was the case for the output-matching network a λ/4 impedance transformer had to be used because the component values of a low-pass matching network would have become too small.

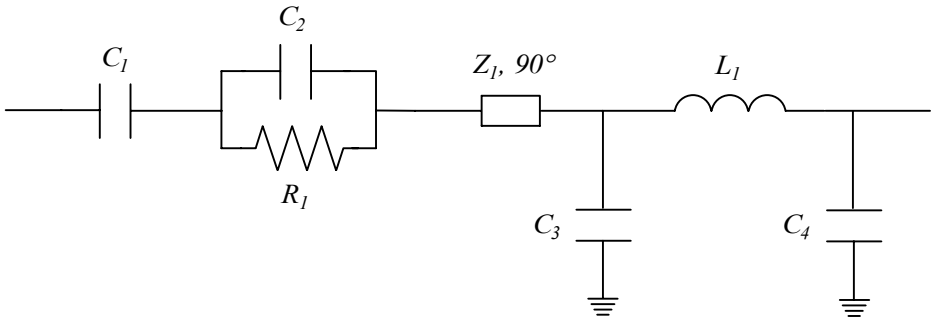

Figure 6.38: Alternative input matching topology.

6.4 Circuit to layout conversion

After having determined an electrical network with ideal components, which performs the impedance transformation between a given source and load impedance, the layout of this network must be generated. The conversion of the ideal equivalent circuit to a layout is the subject of this section. Guidelines will be given enabling the designer to stay as close as possible to the initial electrical performance of the ideal matching network. However, it should be noted that a final optimisation of the network with a tool such as Libra [6.13] is inevitable to reach the best possible performance. The conversion will be discussed with the help of an example. For this example a 5 Ω input impedance is transformed to a 30 Ω impedance at the output of the matching network. A low-pass impedance matching network has been used, see figure 6.39. The component values have been determined with the help of a Chebychev approximation [6.16] of the required matching over the frequency band of interest, see also section 6.3.2.

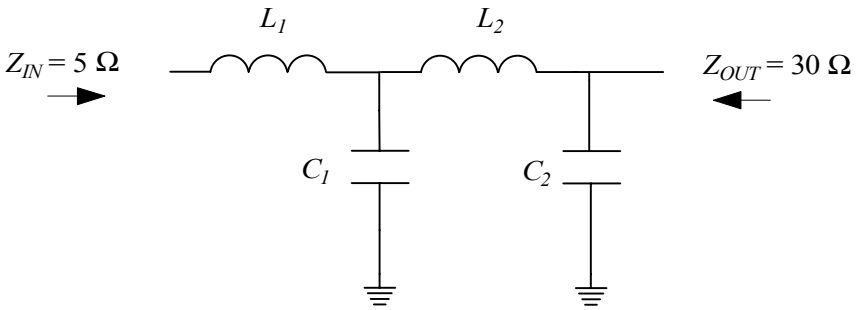

Figure 6.39: Circuit to layout conversion example.

The calculated component values of the ideal matching network are listed in table 6.3.

Table 6.3: Calculated component values schematic to layout example.

L_1 [pH]	C_1 [pF]	L_2 [pH]	C_2 [pF]
112	2.068	310	0.745

Each component has two degrees of freedom when it is converted into a layout, namely its width and its length. The width of a microstrip line that is used to realise an inductor is limited by the amount of DC current that must be able to flow through the line, see also chapter 2. Therefore, often the width of the lines is fixed and the only degree of freedom that is left is the length of the line. The situation is different for the capacitors there both the width and the length can be chosen freely. Nevertheless, it is not advisable to use capacitors that have small width and that are long. In that case, the parasitic inductance and resistance of the capacitor are maximised. This situation has to be avoided. For this reason, in practice, often the width of the capacitor is chosen and with the help of this width, the length can be calculated. For this example, the width of both the capacitors and the microstrip lines has been chosen. An overview of the selected widths and lengths is given in table 6.4.

The resulting S_{11} and S_{21} for six different situations are depicted in figure 6.40. The first result depicted is the one that is obtained with the ideal components that have been listed in table 6.3. The results show that an excellent match < -20 dB is obtained over the 8 – 12 GHz frequency band. The second situation depicted, is the one where the ideal components are directly converted to a layout without considering the influence of the parasitic elements of these components. The obtained results are disastrous as can be seen from figure 6.40. These bad results are caused by the influence of the parasitic elements, for instance the inductance in capacitors and viaholes, which are not compensated for.

Table 6.4: Dimensions of the components that have been converted into a layout. The ideal components values are listed in table 6.3.

Situation	L_1		C_1		L_2		C_2	
	W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]	W [µm]	L [µm]
#2	80	254	80	129	80	728	50	74.5
#3	80	254	1)	1)	80	728	1)	1)
#4	80	254	80	80	80	728	50	51.5
#5	80	214	80	80	80	648	50	51.5
#6	80	169	80	91	80	552	50	67.0

1) Ideal capacitors have been used in this case. The used values are C_1 = 1.968 pF and C_2 = 0.670 pF.

At this point, it is clear that the influence of the parasitic elements is considerable. In the following, the compensation of these parasitic elements is discussed in a stepwise manner. In appendix G, the equations that have been used to compensate for the parasitic elements are discussed. In this section, only the results will be discussed.

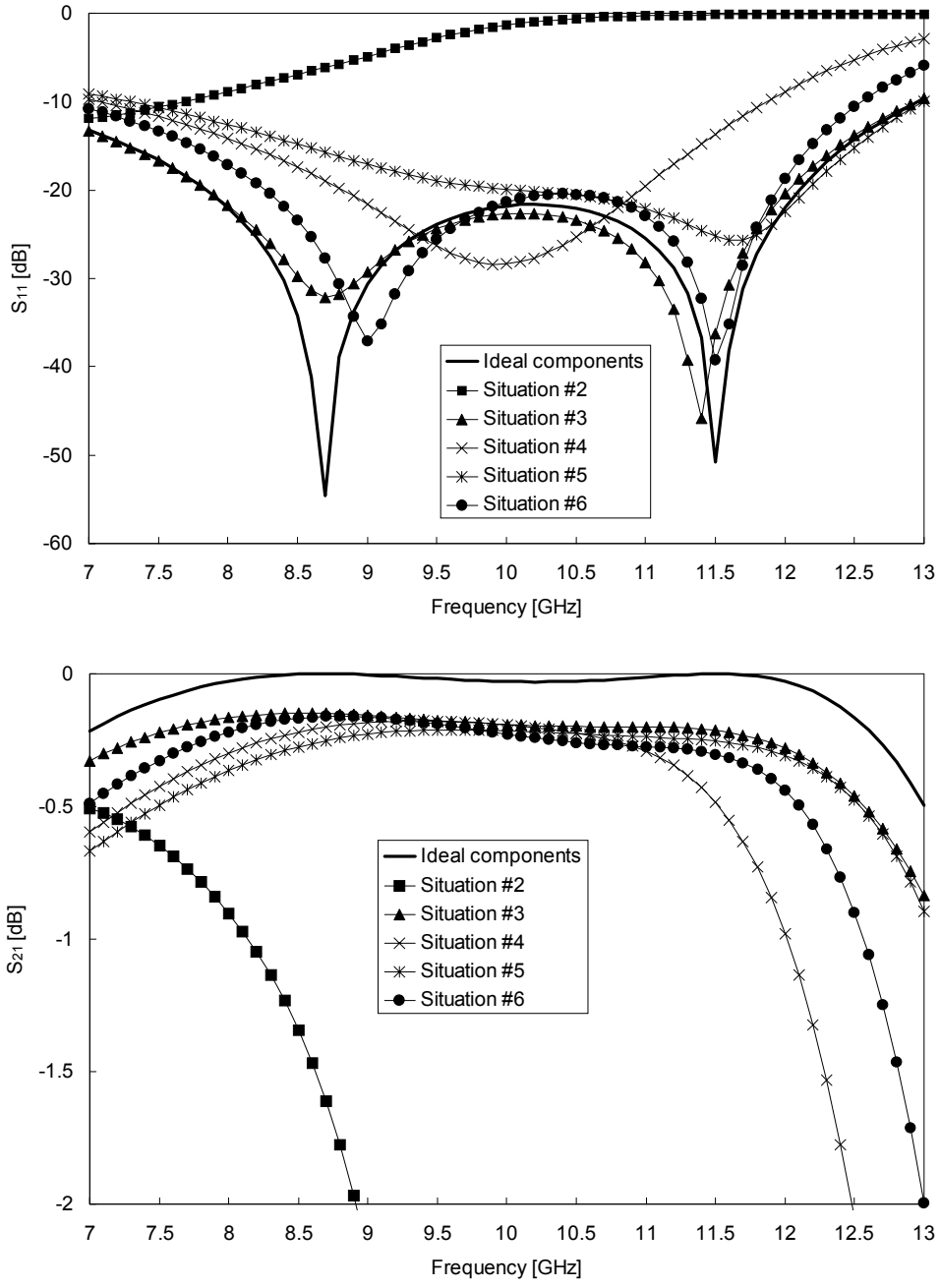

Figure 6.40: Response of the circuit to layout conversion example calculated for 6 different situations.

As a first step, the dimensions of the layout of the series elements are calculated. At this point, it is good to note that the highest order of the equations used for the inductor realised with the help of a microstrip line and the MIM capacitor is two. The order of the equations has been limited to two to make simple analytical equations for the calculation of the dimension of the layout of these components possible. In appendix G, it is shown that by limiting the highest order of the component models to two results in a highest order of the equations, that can be used to calculate the element values, to three. This order of equations can still be solved analytically. As stated before the width of the microstrip lines was chosen. Therefore, the length of the lines must be calculated. The resulting lengths are listed in table 6.4 as situation #3. When both the length and the width of the microstrip line are known the value of the parasitic capacitors to ground is also known. The value of these capacitors is subtracted from the values required for C_1 and C_2, which have been listed in table 6.3. The results of situation 3 that are depicted in figure 6.40 show that the matching (S_{11}) is excellent. Therefore, it can be concluded that this compensation step works very well. Only the loss (S_{21}) has increased to approximately 0.2 dB due to the losses in the microstrip lines.

As a next step, the dimensions of the capacitors have to be calculated. In this case, the width is selected to be 80 µm for capacitor C_1 and 50 µm for capacitor C_2. The lengths are calculated taken into account these widths. In addition, the influence of the viahole inductance, see chapter 4, and the parasitic inductance of the capacitor are accounted for. In appendix G, the used equations are discussed. The calculated dimensions of the capacitors and microstrip lines are listed in table 6.4, as situation #4. The results for this situation are also depicted in figure 6.40. The results show a matching that is still good in the middle of the desired frequency band but it is not good enough over the entire frequency band. For narrow-band applications up to a relative frequency bandwidth of 20% the discussed schematic to layout procedure gives already satisfactory results.

For good wideband results, an additional optimisation step is needed. Before this is done the influence of the microstrip T-junctions, which are necessary to connect the capacitors to ground, will be discussed. For the compensation of the influence of the T-junction, a simplified model is used. In this case, the T-junction is approximated with the help of two microstrip lines that have a width of 80 µm and a length that is equal to half of the width of the capacitor that is connected to ground. The capacitor is connected in the middle of these two microstrip lines. The results as are depicted as situation #5, in figure 6.40 show that results are slightly worse. The results after that the dimensions of the components have been optimised is shown as situation #6 in figure 6.40. The results show that the resulting matching (S_{11}) is close to the one that is obtained with the help of the ideal components listed in table 6.3. The loss (S_{21}) is comparable to the one that was obtained for situation #2. Therefore, it can be concluded that for this example the loss is dominated by the losses of the microstrip lines.

In the scope of the work described in this thesis a computer program was developed, which performs the calculation of the dimensions of the layout of the matching network automatically. In the end still, a final optimisation step is necessary to compensate in a more exact way for the parasitic elements of the used components. In addition, also coupling

between various parts of the layout should be taken into account. Nevertheless, the dimensions found with the methods discussed in this section and appendix G, form a good starting point for the determination of the dimensions of the layout of the matching networks.

6.5 Overall high-power amplifier simulation

In the previous sections, the design of the matching networks was discussed. The overall simulation of a high-power amplifier is the topic discussed in this section. This is not as trivial as it might look at first sight. The reason for this are the number of transistors, most of the time eight in the output stage of the amplifier, that are used in their non-linear region. This results for the Libra harmonic balance simulator [6.13] in long simulation times and often in convergence problems, in which case no simulation result at all is obtained. As already indicated this is caused by the large number of transistors that are simulated in their non-linear region. A solution for the before mentioned problem is the reduction of the number of transistors that is needed in the simulation. The symmetry that exists in the amplifier makes a reduction of the number of transistors needed for a simulation to one per amplifier stage, possible.

In the remainder of this section, a method to simulate the amplifier performance with only one transistor per amplifier stage is discussed. In figure 6.41, an example of a one-stage amplifier is depicted. In this figure, the incident and reflected power waves at the input and the output of the transistors are depicted.

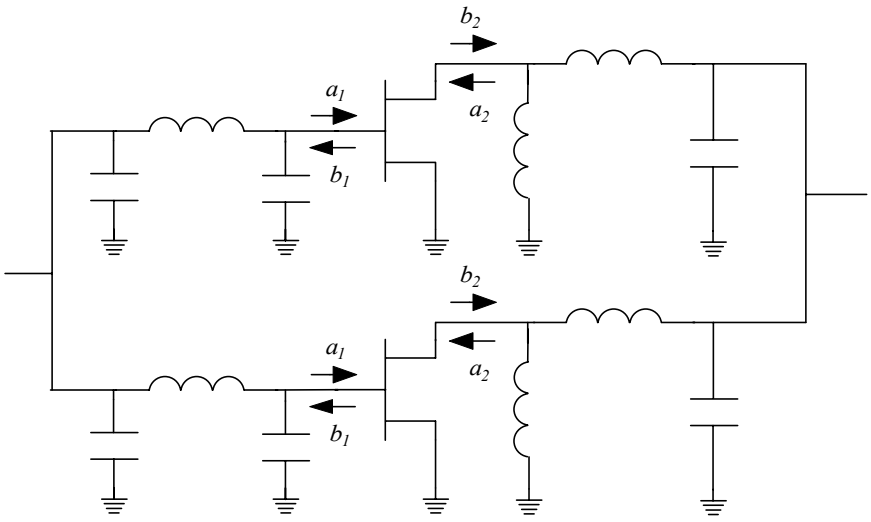

Figure 6.41: Example of a one-stage high-power amplifier with in and output-matching networks.

The depicted power waves (a_1, b_1, a_2 and b_2) are equal at both branches of the matching networks. This symmetry is used to reduce the number of transistors that has to be simulated per amplifier stage to one. This reduction is achieved with the application of an ideal power sampler. Its symbol is depicted in figure 6.42. An ideal power sampler has at each frequency the following S-parameters:

$$S_{21} = S_{12} = S_{31} = 1\,, \tag{6.56}$$

and

$$S_{11} = S_{22} = S_{33} = S_{13} = S_{23} = S_{32} = 0\,. \tag{6.57}$$

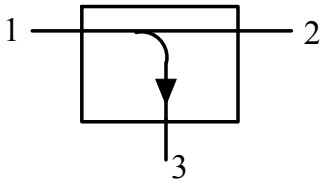

Figure 6.42: Symbol of an ideal power sampler.

This power sampler is a standard component available in Libra [6.13]. It is also easily defined with the help of the S-parameters given in equations (6.56) and (6.57) for simulation packages, like ADS [6.22], where this component is unavailable. The power sampler is used to generate the incident and reflected power waves required at the input and output of the matching networks as it is shown in figure 6.43.

At the input of the transistor, the power sampler is connected in the reverse direction. By doing this the reflected wave, b_1 that is coming back from the transistor is also injected in the second branch of the input-matching network. The incident wave a_1 is absorbed in the power sampler. The use of the power sampler results in the same set of power waves at the outputs of the matching network as would have been the case when two transistors where used in the simulation. The same reasoning is valid for the output-matching network only there the incident wave b_2 is injected and the reflected wave a_2 is absorbed by the power sampler. It is easily seen that by using more power samplers this principle can be expanded to any number of transistors in parallel.

The method described in this section solves the convergence problems encountered with the amplifiers discussed in this thesis. In addition, a significant simulation speed improvement has been obtained. The actual number is difficult to exactly quantify, because it depends on the actual amplifier topology, i.e. the number of transistors in parallel. In practice, speed improvements with a factor of more than 10 have been obtained. This speed improvement in combination with the reduced number of convergence problems makes an overall

optimisation of the high-power amplifier performance under large-signal conditions feasible.

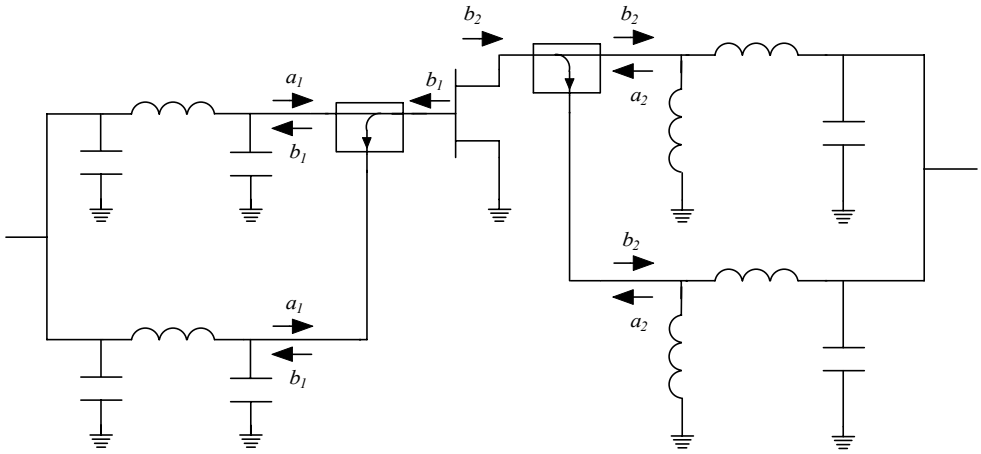

Figure 6.43: Simulation of high-power amplifier with only one transistor per amplifier stage.

6.6 Biasing circuit

The way the gate bias voltages are applied to a high-power amplifier needs additional consideration. Points of concern are:

- The influence of fluctuations in the bias supplies voltages.
- The effect of process variations.
- The effect of temperature variations.

When the gate bias voltages are directly obtained from the bias supplies the effect on the performance of the high-power amplifier is considerable. Unacceptable output power and insertion phase variations may occur due to gate bias variations. Due to the random nature of these variations, no compensation can be applied. Another disadvantage of the use of a gate voltage directly obtained from the bias supplies is the fact that process variations, e.g. pinch-off variations, will result in considerable gain variations. The same is valid for the effect of temperature variations. To circumvent or at least reduce the effect of before mentioned problems it is necessary to generate the gate voltages with the help of a gate bias circuit. Examples of gate bias circuits are depicted in figure 6.44.

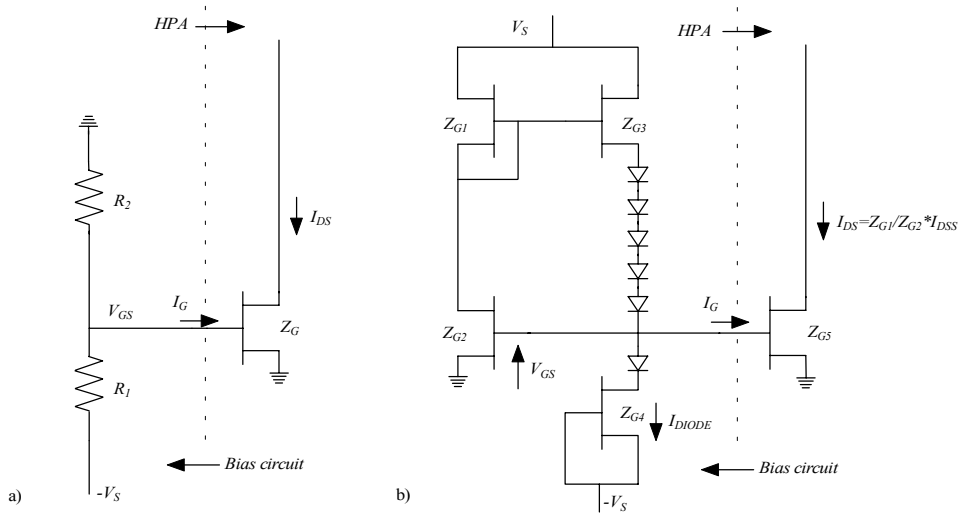

Figure 6.44: Examples of gate bias generation circuits.

To analyse the behaviour of the gate bias circuits, the equation for the drain-source current given by Curtice [6.23] will be used:

$$I_{DS}(V_{GS}, V_{DS}, Z_G) = Z_G \cdot \beta \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \cdot \tanh(\alpha \cdot V_{DS}). \tag{6.58}$$

This equation shows that the drain-source current is dependent on the bias voltages applied to the transistor, the size of the transistor and the threshold voltage of the transistor V_T. For the analysis of the behaviour of the gate bias circuit the following is assumed:

- The transistors are used in their saturated region ($\tanh(\alpha.V_{DS})=1$).
- The output conductance is assumed to be zero ($\lambda = 0$). This is a reasonable assumption for the small transistors used in the discussed gate bias circuit.

Equation (6.58) is then simplified to:

$$I_{DS}(V_{GS}, Z_G) = Z_G \cdot \beta \cdot (V_{GS} - V_T)^2. \tag{6.59}$$

The transconductance of the transistor is found as:

$$g_m(V_{GS}, Z_G) = \frac{\delta I_{DS}}{\delta V_{GS}} = 2 \cdot Z_G . \beta \cdot (V_{GS} - V_T). \tag{6.60}$$

The transconductance can also be expressed as a function of the drain-source current with the help of the following equation:

$$g_m(V_{GS}, Z_G) = 2 \cdot \sqrt{Z_G \cdot \beta \cdot I_{DS}(V_{GS}, Z_G)}. \tag{6.61}$$

The transconductance g_m is directly related to the gain of the transistors as was already discussed in section 2.3. The drain-source current setting is related to both the gain of the transistor, see equation (6.61), and the operating class of the transistor, see section 5.4. The effect of gate-source voltage variations is described with the help of the following equations:

$$\frac{\Delta I_{DS}}{I_{DS}}(V_{GS}) = 2 \cdot \left(\frac{\Delta V_{GS}}{V_{GS} - V_T} \right) + \left(\frac{\Delta V_{GS}}{V_{GS} - V_T} \right)^2, \tag{6.62}$$

$$\frac{\Delta g_m}{g_m}(V_{GS}) = \frac{\Delta V_{GS}}{V_{GS} - V_T}. \tag{6.63}$$

When a simple gate bias circuit is used like the one depicted in figure 6.44 a), a considerable influence of supply voltage V_S variations is observed on the gate-source voltage applied to the transistors in the power amplifier. Consequently, there is also a direct influence on the drain-source current setting and gain of the transistor,

$$V_{GS} = \frac{R_2}{R_1 + R_2} \cdot V_S = K_R \cdot V_S. \tag{6.64}$$

There is a linear relationship between supply voltage variations and gate source variations, although the supply voltage variations are reduced with a factor K_R. If a supply voltage of – 5 V is assumed a typical value of $K_R = 0.25$ is found for the MESFET amplifiers and a value of $K_R = 0.06$ is found for the HFET amplifiers discussed in this thesis. The situation changes when the power transistors start to draw gate current. In that case, the gate-source voltage is reduced,

$$V_{GS} = \frac{R_2}{R_1 + R_2} \cdot V_S - \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot I_G. \tag{6.65}$$

The situation is similar to the one described in section 5.5, where a gate resistor is used to improve the reliability of the transistors by reducing the gate current. There is no disadvantage from the point of varying gate source voltage due to gate current when each amplifier stage uses its own gate bias circuit.

The influence of supply voltage variations is absent for circuit b) shown in figure 6.44. The gate bias voltage that is generated with that circuit is directly determined by the ratio of the gate width of the transistor indicated with Z_{G1} and the gate width of the transistor indicated with Z_{G2}. The gate-source voltage is directly related to the threshold voltage of the transistor via the following relation:

$$V_{GS} = \left(\sqrt{\frac{Z_{G1}}{Z_{G2}}} + 1 \right) \cdot V_T \,. \tag{6.66}$$

The current through and the transconductance of the transistors used in the high-power amplifier is then given by:

$$I_{DS}(V_{GS}, Z_G) = \frac{Z_{G1}}{Z_{G2}} \cdot Z_G \cdot \beta \cdot {V_T}^2 = \frac{Z_{G1}}{Z_{G2}} \cdot I_{DSS}(Z_G), \tag{6.67}$$

$$g_m(V_{GS}, Z_G) = 2. \sqrt{\frac{Z_{G1}}{Z_{G2}}} \cdot Z_G \cdot \beta \cdot V_T \,. \tag{6.68}$$

Under large-signal conditions, the gate bias circuit must be able to supply gate current in both positive and negative direction. To make this possible a buffer stage has been added to the gate bias circuit. The amount of gate current that can be delivered in the forward direction is determined by the size of the transistor indicated with Z_{G3}. The amount of gate current that can flow in the negative direction is limited by the current that flows through the current source realised with the transistor that has a gate width Z_{G4}. This current source is also used to set the level shift diodes in forward and to reduce the influence of the negative supply voltage.

In figure 6.45, the layout of the realised gate bias circuit is shown. The necessary diodes are realised with the help of transistors which drain and source connections are connected together. A comparison between the simulated and the measured gate voltage as a function of the gate current that is flowing is depicted in figure 6.46. The results show that a constant voltage is obtained over a 0 to 25 mA gate current range. In figure 6.46 also the gate voltage as a function of varying supply voltages is shown. In addition, it is shown that the gate bias current can supply some negative gate current.

An additional point of concern is, as was mentioned in the introduction of this section, the influence of process variations on high-power amplifier performance. The major influence, which can be compensated for is the gain variation of the amplifier. This gain variation is directly related to variations in the threshold voltage of the used transistors. The effect of threshold voltage variations on the drain-source current and transconductance when biased with circuit a) figure 6.44, is given by:

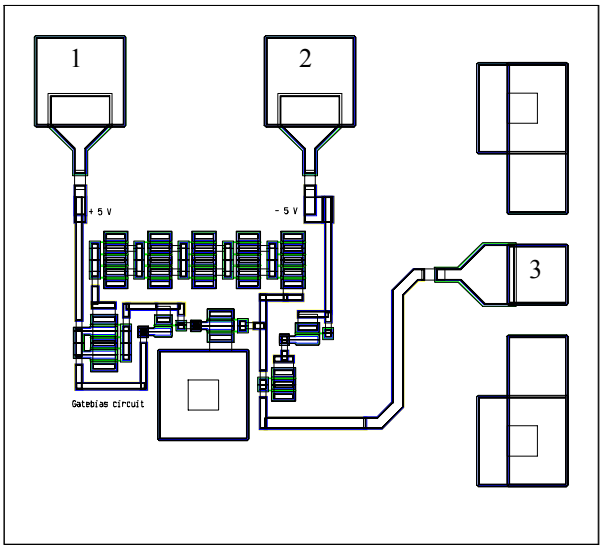

Figure 6.45: Layout of the realised gate bias circuit.

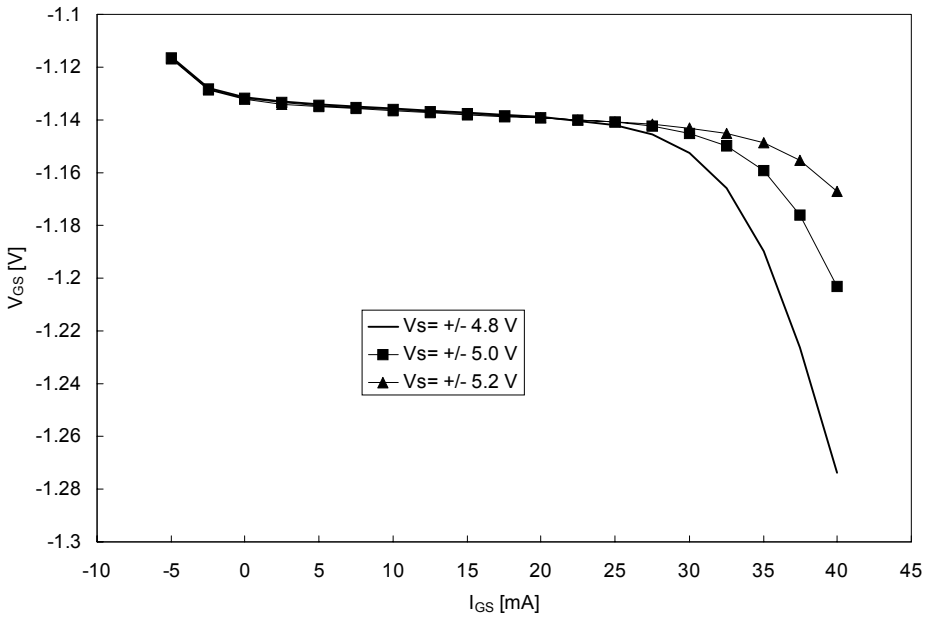

Figure 6.46: Calculated gate-source voltage generated with the help of gate bias circuit shown in figure 6.44 b) as a function of the gate bias current and the bias voltages.

$$\frac{\Delta I_{DS}}{I_{DS}}(V_{GS}) = -2 \cdot \left(\frac{\Delta V_T}{V_{GS} - V_T} \right) + \left(\frac{\Delta V_T}{V_{GS} - V_T} \right)^2, \tag{6.69}$$

$$\frac{\Delta g_m}{g_m}(V_{GS}) = -\frac{\Delta V_T}{V_{GS} - V_T}. \tag{6.70}$$

The dependence of gate bias circuit b) for threshold voltage variations is given by the following equations:

$$\frac{\Delta I_{DS}}{I_{DS}}(V_{GS}) = 2 \cdot \left(\frac{\Delta V_T}{V_T} \right) + \left(\frac{\Delta V_T}{V_T} \right)^2, \tag{6.71}$$

$$\frac{\Delta g_m}{g_m}(V_{GS}) = \frac{\Delta V_T}{V_T}. \tag{6.72}$$

The equations show that circuit b) is less sensitive to process variations than circuit a). The variations are only equal for V_{GS} = 0 V, for the amplifiers discussed in this thesis $V_{GS} \approx 0.5V_T$. Equation (6.61) shows that transconductance variation as a function of process variation is minimised when a constant current setting is used. A constant current setting can be realised with the help of a current mirror. An example of a current mirror realised on GaAs is discussed in [6.24]. A disadvantage of the in [6.24] depicted current mirror is its dependency on supply voltage variations. Therefore, the gate bias circuit depicted as b) in figure 6.44 was the preferred solution.

The last point that needs attention is the temperature dependency of the power amplifier. As discussed in section 5.3.4 and appendix C the major factor contributing to the temperature dependency of the transistor gain is the temperature dependency of the electron saturation velocity. Therefore, the transconductance fitting factor β will decrease with increasing temperature. Equation (6.61) shows that for increasing temperature the drain-source current and consequently the gate-source voltage should increase also to get a constant transconductance and therefore a more or less constant transistor gain. In [6.25, 6.26] some off-chip circuits are discussed that control the gate-source voltage as a function of temperature. In [6.27] a very simple on-chip gate-source voltage control circuit is discussed. Excellent temperature control was achieved with this circuit. A disadvantage of the circuit discussed in [6.27] is its dependency on variations in bias supply voltage and process variations.

The high-power amplifiers discussed in this thesis were developed for application in the TR module of a phased-array radar. The specified temperature range of this TR module was 30 °C, for this reason not very large gain and output variations due to temperature variations are expected. Application of the bias circuit as shown in figure 6.44 b) is acceptable for this reason because it has no bias supply dependency and the process variations are partly compensated for. For power amplifiers that combine a wide temperature range, with large

process variations and the need to minimise the effect of bias supply voltage variations further investigations are needed for the development of an on-chip gate bias circuit, which compensates for all three mentioned aspects.

6.7 High-power amplifier stability

6.7.1 Introduction

After the amplifier design is completed, the stability of the amplifier must be analysed. This analysis is more complex than the one discussed in section 5.6 for a single transistor. This is due to the fact that there exist multiple loops for a complete amplifier, which all can give rise to instabilities. Besides these loop oscillations, also instability can exist for certain load impedances applied to the input, the output and the bias connections of the amplifier. This is specifically a problem at low frequencies where it is not possible to take sufficient on-chip counter measures. At microwave frequencies the loading is still important but can easily be analysed with the existing tools. It is also relatively easy to take on-chip precautions to prevent oscillations at these frequencies. Another class of oscillation is formed by the so-called odd-mode type of oscillations that can occur because the used transistors are not equal or the matching networks are not completely symmetrical. The last type of oscillation that is important for high-power amplifier design is the so-called parametric oscillation. In the following sections, the different types of oscillations and the methods that are used to analyse them are discussed in detail.

6.7.2 Loop oscillations

All oscillations that can exist in high-power amplifiers can be subdivided in oscillations that are caused by a feedback loop or oscillations that are caused by incorrect loading of the transistors. In section 5.6, the effect of the load impedances applied to a transistor is analysed with the help of the *K*-factor. In this section, the analysis of loop gain oscillations will be discussed.

In literature different methods are described that can be used to analyse the effect of feedback that exists in an amplifier. One of the first contributions in this area regarding the analysis of microwave high-power amplifiers is due to Freitag [6.18]. Although it is an elegant method, it is not sufficient for the problem at hand here. The reasons for this are the following: 1) the circuit discussed in this thesis is not entirely symmetrical, 2) the mode of instability is not a priori known. These requirements are not necessary for the method used for the analysis of the stability of the discussed high–power amplifiers. This analysis method is based on the work described by Ohtomo [6.28]. This method is based on splitting the amplifier in an active and a passive part as it is shown in figure 6.47.

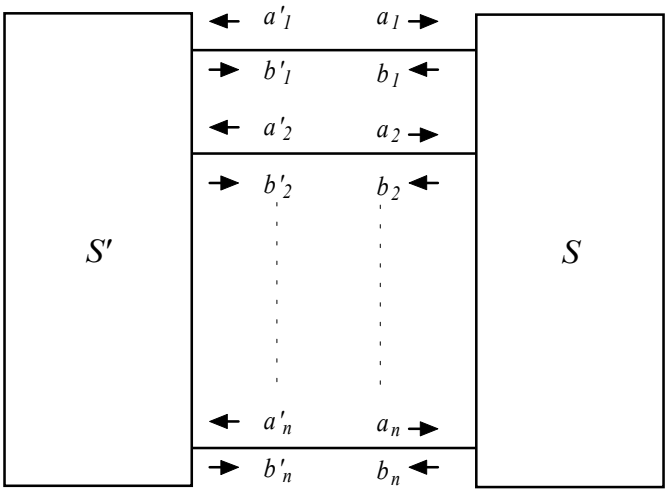

Figure 6.47: Generalised equivalent circuit of a high-power amplifier (The S-parameters for passive part are indicated with S' and for active part with S).

Based on this generalised equivalent circuit the following generalised oscillation condition can be derived in terms of the S-parameter of the active and passive part of the power amplifier [6.29]:

$$\Delta = \left| [S'] \cdot [S] - [I] \right| = 0 , \tag{6.73}$$

in this equation I is the identity matrix and S' and S are the S-parameter matrix of the passive part and the active part of the amplifier respectively. Mason and Zimmerman have shown [6.30] that an arbitrary linear flow graph is stable only if the zeros of the graph determinant function Δ lie in the left half plane. This under the consideration that all branch transmissions themselves are stable. This means that the active devices must be stable, see section 5.6. Mason and Zimmerman have also shown that rewriting the determinant function as a product of return differences gives a convenient way for the analysis of the stability,

$$\Delta = \Delta_1 \cdot \Delta_2 \cdots \Delta_n , \tag{6.74}$$

the return differences in equation (6.74) can also be written as:

$$\Delta_k = 1 - \tau_k , \tag{6.75}$$

in this equation τ_k is the loop transmission of node k where all higher order nodes are split or erased [6.30]. Nyquist plots of Δ_k or τ_k can be used to judge if an amplifier is stable. Ohtomo [6.28] has given a convenient way to analyse all relevant loop transmissions with the help of a commercial available simulator like e.g. Libra [6.13]. Another approach

originates from Platzker et al. [6.31] where the stability is analysed with the help of the normalised determinant function. Implementation of this method in a commercial available simulator is described for a linear n-port in [6.32] and for the non-linear case in [6.33].

Performing the stability analysis with the help of the Ohtomo method in a commercial simulator is convenient, as long as the number of active devices and different load impedances at the input, the output and the bias ports of the amplifier, are small. This is not the case for most of the amplifiers discussed in this thesis. For this reason, a stability analysis program based on the method of Ohtomo is written which uses the S-parameters files of both the active and passive part of the amplifier as input only. The termination on different ports can be varied automatically. This last point is an important feature, certainly at the output of a power amplifier that is used in a TR module of a phased-array radar, which is not sufficiently isolated from the antenna. In this case, the load impedance of the amplifier varies as a function of the scan angle of the phased-array antenna. This varying load impedance can lead to instabilities and therefore burn-out of the power amplifier. So the stability analysis mentioned before must be carried out for a variety of load impedances. The outcomes of this program are Nyquist plots of all relevant loop gains and an automatic warning is given if instability is detected.

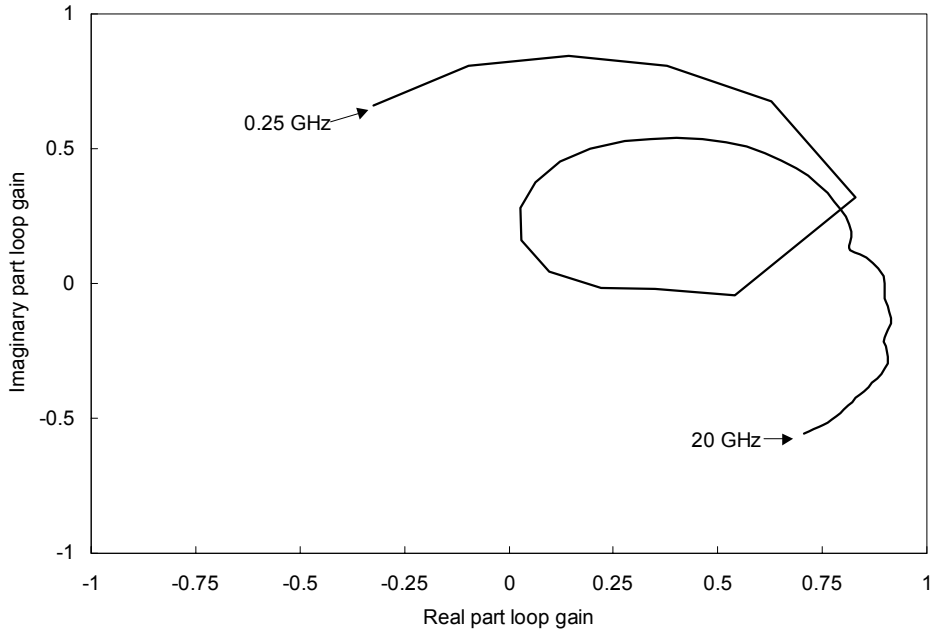

Figure 6.48: Loop gain of 10-Watt HFET amplifier, see section 7.3. For this calculation, none of the existing loops has been deactivated.

The stability analysis should be performed under both small-signal and large-signal conditions. Consequently, the S-parameters of the transistors used in a power amplifier must be determined under large-signal conditions. For this purpose, a multi-tone simulation method was developed, which is discussed in detail in appendix D. This method is used in the high-power amplifier design under different input power and bias conditions. It is clear that the accuracy of this method entirely depends on the accuracy of the transistor models used, see section 4.2. In figure 6.48 an example of a Nyquist plot of a loop gain of one of the discussed amplifiers is shown.

6.7.3 Low-frequency oscillations

The circuitry that is connected to a power amplifier off-chip can also cause oscillations. Such oscillations can be caused by off-chip loops or impedances presented to the input or the output of the transistors. The analysis of the loop oscillations is discussed in the previous section. The method to analyse the effect of the load impedance on the stability of the transistor was presented in section 5.6. The reason that there can exist oscillation problems because of off-chip connections is the inability to realise sufficient on-chip decoupling, see section 2.4.4. Therefore, the influence of the off-chip connections is seen at the input and output of the transistors inside the amplifier. The frequency range where these kinds of problems have been observed varies from ≈ 1 MHz to 2 GHz.

The solution to this problem is the application of sufficient decoupling as close as possible to the chip. This decoupling can be realised with the help of a bank of SMD capacitors connected to ground. Different capacitor values are needed to guarantee stability over the complete frequency range. This is necessary because the resonance frequency where the behaviour of the capacitor changes to that of an inductor depends on the value of the capacitor. The larger the capacitor values the lower the resonant frequency. In series with these capacitors, certainly for the small values, a series resistance must be used to prevent the occurrence of a short circuit at the input and the output of the transistor. Analysis has shown that this will result in an oscillation for frequencies below a few GHz.

The decoupling mentioned before can be realised, when the power amplifiers are mounted in their application, e.g. a TR module for a phased-array radar. It is more difficult to realise sufficient decoupling when there is a need for on-wafer testing of the power amplifiers. In the latter case, the inductance of the probe needles makes a sufficient decoupling for high frequencies difficult. The inductance of a probe needle is approximately 10 nH. This high value can cause problems in the GHz frequency range because the influence of the decoupling capacitors is masked by the inductance of the probe needle. As a result an inductor is presented at the input and the output of the transistor, which on its turn might result in an oscillation.

6.7.4 Odd-mode oscillations

Until this moment, all signals entering and leaving the transistors that are placed in parallel are considered to have equal amplitude and phase. In addition, also the divider and combiner networks are considered to be symmetrically. In reality, both the transistors and the divider and combiner networks are not equal for all branches due to process variations and electromagnetic coupling. These inequalities can give rise to another type of oscillation, which. is known as odd-mode oscillation. One of the firsts to give an analysis method for this kind of oscillations was Freitag [6.18]. His analysis method indicates which mode is involved if such an oscillation problem exists (but not exactly). Recently a method is proposed [6.34] that circumvents this problem. The proposed method gives a very simple solution for symmetrical networks.

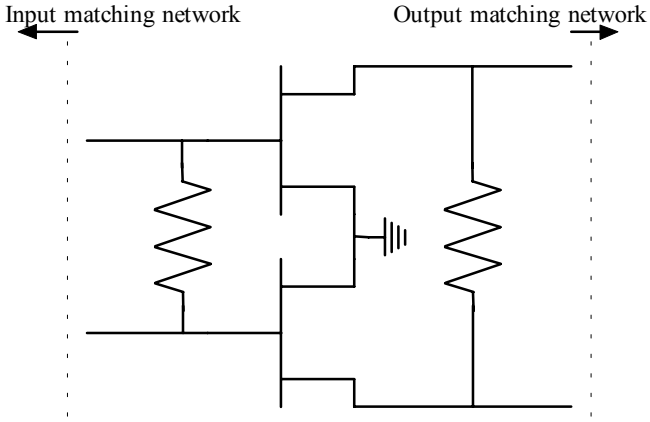

Figure 6.49: Used odd-mode suppression network.

For the amplifiers discussed in this thesis no in depth odd-mode stability analysis was performed. Instead, from the start of the amplifier design, networks have been utilised to suppress odd-mode oscillations. The suppression networks consist of a stabilising resistors that is placed in between each pair of transistors whenever possible, see figure 6.49. The value of the resistor varies from 0 to 10 Ω.

Note that the odd-mode oscillations can also exist in the frequency band of interest. Therefore, it is not possible to take other precautions like e.g. the utilisation of a parallel resistor capacitor network, which is introduced to reduce the loop gain. The use of odd-mode suppression networks works well and no odd-mode related oscillation problems were detected for the amplifiers discussed in this thesis.

6.7.5 Parametric oscillations

The last category that is discussed in this thesis is the group of oscillations that are input power and bias dependent. This group of so-called parametric oscillations can be subdivided in spurious and subharmonic oscillations [6.35]. The existence of parametric oscillations cannot be analysed with the help of the methods discussed so far. A method that is able to detect the existence of subharmonic oscillations is described in [6.36]. In practice, the application of such a method is very time consuming because it must be performed at every possible frequency, input power level, temperature, bias point etc. Therefore, practical application of methods that can be used for the analysis of parametric oscillations is mainly restricted to the explanation of a detected oscillation. Of course for a limited number of cases the analysis must be performed before the amplifier is processed. This point of view that parametric oscillations only can be analysed if the oscillation frequency is known is also shared by the authors of [6.37]. They state that the order of the subharmonic must be known prior to running a stability analysis with a harmonic balance simulator like Libra [6.13]. A solution to this problem would be the application of a time domain simulator like PSPICE. The problem with such a time domain simulator is the unavailability of microstrip model for transmission lines and discontinuities. At this point, it is good to note that the models that have been discussed in this thesis directly can be used in a time domain simulator. This is even true for the Y-junction model where the microstrip line models can be replaced by the model given for the capacitor for the inductance L_S, see appendix A.7.

Parametric oscillations can have a destructive effect due to the increased voltage stress on the transistors. For this reason and the fact that they at least increase the spurious level, it is necessary to look at means to prevent these oscillations. For this, it is necessary to have some insight in the nature of the mechanism that causes the parametric oscillations. The subharmonic oscillation is believed to be caused by the non-linear gate capacitances C_{gs} and C_{gd} [6.35, 6.37]. These non-linear capacitances can give rise to subharmonic frequency components, as it is the case with pumped varactor diodes [6.38]. The time dependent variation of these capacitors can be described with the following equation:

$$C(t) = C_0 \cdot \left(1 + 2 \cdot \sum_{N=1}^{\infty} \gamma_N \cdot \cos\left(N \cdot \omega_0 \cdot t\right) \right). \tag{6.76}$$

In this equation γ_N is a factor which is increased when the amplitude of the voltage over the capacitor increases at frequency f_0. A stable subharmonic f_{SH} repeats exactly as:

$$f_{SH} = f_0 \cdot \frac{n}{m}. \tag{6.77}$$

In this equation, f_0 is the pump frequency and n and m are integer numbers. Subharmonic generation is directly related to the memory of the circuit [6.37]. The carrier lifetime in the case of a Field Effect Transistor is low. It is in the order of a few pico-seconds. Therefore, it

is unlikely that for the amplifiers discussed in this thesis the subharmonics will be more than two or three times lower than the pump frequency [6.37]. According to [6.35], the following equation describes the f_0 / 2 oscillation condition:

$$\left| Z_L(\omega_{SH}) + R_S + \frac{1}{j \cdot \omega_{SH} \cdot C_0 \cdot \left(1 - \gamma_1{}^2\right)} \right| < \frac{\gamma_1}{\omega_{SH} \cdot C_0 \cdot \left(1 - \gamma_1{}^2\right)}. \tag{6.78}$$

In this equation, Z_L is the load impedance at the subharmonic frequency and R_S is the series resistance. In appendix H the derivation of this equation is given. This equation shows the ways that can be used to prevent subharmonic oscillations. The first method is increasing the value of R_S with the help of the RC network that was discussed in section 5.6. This network is also useful for providing unconditional stability for the transistors. For some of the amplifiers discussed in this thesis this network is used in front of the transistors. In [6.35], it was proposed to integrate these networks directly in series with each gate finger. A second method to prevent subharmonic oscillations from occurring is influencing the value of Z_L. When Z_L has an inductive character C_0 can be resonated out by this inductance as can be seen from equation (6.78). Application of for instance a short in parallel with the gate at the subharmonic frequency, see [6.37], prevents this from happening. Disadvantages of the latter method compared to the first one are the fact that the necessary LC circuit to create the short circuit at the subharmonic frequency takes a relative large amount of chip area. In addition, the subharmonic frequency must be known in advance. This is necessary because it is difficult if not impossible to realise the short over the broad frequency range, which else would be required. A third method is the one described in [6.36] where a stabilising resistor is used between the transistors that are placed in parallel, see figure 6.49. This method was used for all amplifiers discussed in this thesis. For none of these amplifiers, subharmonic oscillations were detected.

The prediction of the occurrence of parametric spurious oscillations is difficult. These oscillations are caused by a change of the transistor parameters under large-signal conditions. The influence in the frequency band of interest can be analysed with the method discussed in section 6.7.2. For this analysis, the large-signal S-parameters of the transistors are determined with the method discussed in appendix D. For the parametric spurious analysis a similar method can be used. In the latter case, the offset between the large-signal frequency and the second frequency must be changed in such way that the S-parameters at the spurious frequency can be simulated. This is in principle possible but, as already stated at the beginning of this section, very time consuming without priory knowledge of the oscillation frequency. In [6.35] it was stated that the use of a RC network at the input of the transistor also prevent spurious oscillations from occurring at low frequencies. To prevent spurious oscillations for the amplifiers discussed in this thesis the methods given in section 6.7.4 were used.

6.8 Conclusions

In this chapter, the design of the matching networks is discussed in detail. The design procedure used in this thesis starts with the determination of the source and load impedance of the matching networks. For the load impedance of the input and interstage-matching networks a series inductor, capacitor and resistor network is found. The source impedance found for the interstage and output-matching network is formed by a series inductor terminated with a parallel resistor capacitor network. In both networks, the values for the capacitors and resistors scale as a function of the total gate width of the transistor cell. The value of the series inductor is determined by the layout of the transistor cell.

With the help of the integral equations due to Bode and Fano [6.1, 6.2] it is shown that the realisation of matching networks with a sufficient degree of accuracy is possible over the X-band frequency range. For the source impedance an impedance matching of better than 20 dB can be obtained over the entire frequency band. For the load network, a lower bandwidth is found for the same mismatch loss. Therefore, it is expected that it will be more difficult to get a good match for the input and interstage-matching networks than for the output-matching network.

An overview is given of a number of simple networks, which can be used for the realisation of the matching networks. For each network, equations are derived for the calculation of the element values and the input reflection coefficient. This reflection coefficient is shown to be dependent on the matching ratio and relative frequency bandwidth only. On the other hand, the element values of the matching network are dependent on the matching ratio and the frequency of interest. The equations show that the component values become large for frequencies below 3 GHz. For frequencies above 20 GHz the component values become small. Therefore, normally at low frequencies, parts of the matching networks need to be realised off-chip and at high frequencies, mainly distributed elements must be used. Lumped on-chip components have reasonable values at X-band. Therefore, for the realisation of the matching networks in the amplifiers discussed in this thesis lumped components have been used. In addition, for each type of matching network the sensitivity for component spread was analysed. It turned out that:

- The distributed matching networks are less sensitive to component spread than the lumped matching networks.
- For the used technologies, the lumped high-pass matching networks are more sensitive to component spread than the lumped low-pass matching networks.

The matching networks must perform the following functions:

- Present the load and source impedance required at the input and output terminals of the transistors.
- Combine or divide the power from or to the transistors to the required load impedance or source impedance as has been defined in chapter 5. The input and the output of the amplifier are loaded with the system impedance, which is 50 Ω.
- Provide where necessary a frequency dependent loss to compensate for the gain roll-off in the transistors.

- Provide the bias supply to the transistor.
- Enhance the stability of the used transistors.

For the matching networks that have been used in the amplifiers, the influence of the bias supply connections has been taken into account. The drain bias is supplied via an inductor. This inductor is also used to make the source impedance of the matching networks real at the centre frequency. The gate biasing is done via a bias resistor. For the discussed amplifiers, it was not always possible to supply the gate bias via an inductor because its value became too small to realise. The use of a resistor in series with the gate of the transistor results in a lower output power and an increased reliability of the transistor, as discussed in section 5.5. Two different methods have been used to determine the element values of the matching networks. For both methods, first the load and source impedance is made real. The source impedance is made real with the inductors that are used for the biasing. The load impedance is made real with the help of a parallel capacitor to ground or in the case of a small transistor with a parallel inductor to ground. Analysis has shown that for the transistors used in the discussed amplifier the value of the capacitor or inductor is critically influenced by the value of the gate inductance. Therefore, it is recommended for future designs, to include extra series inductance with the gate to make the resulting capacitor value less critical. As a second step, the component values of the network, which matches the resulting real source and load impedances, are determined. A low-pass matching network is used as the basis for the input, interstage and output-matching network design. A low-pass matching network is used because it contains the required series inductances, which can be used to connect the transistors in parallel. The component values of the low-pas matching network can be determined in different manners. The first way to determine them is to make use of closed form expressions that can be used to calculate the element values. A second method is making use of the elementary impedance transformers discussed in section 6.2.3. When these impedance transformers are optimised for centre frequency and matching ratio, the same component values and performance are found as with the first method. The advantage of the second method is that different types of elementary matching networks can be combined to form the required matching network. The compensation of the frequency dependent gain roll-off of the transistors is realised with the introduction of a frequency dependent loss in the matching networks. This loss is introduced by placing resistors at strategic places in parallel or in series with the matching elements.

The conversion of the ideal matching network into a layout is also discussed in this chapter. It is shown that a good first approximation is obtained if the parasitic effects of the used components are compensated for at one frequency e.g. the centre of the desired frequency band. In the end, the use of an optimiser is still unavoidable. For this reason software was developed to find good initial values for the layout of the used components.

For the overall simulation of the power amplifiers a method has been developed, which makes it possible to simulate the performance under large-signal conditions. The developed method uses the available symmetry in the amplifier. The incident and reflected power waves are presented to the matching networks with the help of ideal power samplers. In this way, the number of transistors needed for a large-signal simulation is reduced to one per

amplifier stage, which on its turn removes the convergence problems that are encountered in a simulation when all transistors are used.

The generation of the gate bias voltage of the amplifier is also discussed. It is shown that the influence of the supply voltages on the gate voltage can be reduced with the help of the gate bias circuit discussed in this chapter. In addition, the effect of threshold voltage variations is partly compensated for. The developed gate bias circuit does not compensate for temperature variations. Further investigations are needed for the realisation of a gate bias circuit, which compensates for supply voltage variations, component spread and temperature variations.

As last point, the different types of oscillation and ways to analyse and suppress them were discussed. The influence of the load and source impedance on the stability of the unit transistor cells was already discussed in section 5.6. In this chapter a method is given that makes it possible to analyse oscillations caused by on-chip and off-chip loops. Another type of oscillation that is discussed is the so-called low-frequency oscillation. In general, low-frequency oscillation is caused by the off-chip circuitry because not sufficient on-chip decoupling can be realised. This problem is solved with the use of off-chip decoupling capacitors with a resistor in series. In addition, also odd-mode oscillation can cause problems. This type of oscillation is suppressed by adding resistors between the gates and the drains of the transistors that are placed in parallel. The last types of oscillation that are discussed are the so-called parametric oscillations. A complete analysis of this kind of oscillations during the design phase is difficult if not impossible. For this reason, isolation resistors in between the gate and the drain of the transistors are used as a precaution. In addition, the use of a parallel resistor and capacitor network at the input of the transistor helps to avoid parametric oscillations. For future designs, integration of such a network per gate finger as proposed in [6.35] is advisable.

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7. High-power amplifier results

7.1 Introduction

In the previous chapters, the ingredients that are necessary for a successful high-power amplifier design are discussed. In this chapter the results obtained with the application of the discussed models and design methods will be presented. For both MESFET and HFET technology, one example will be discussed in detail. A comparison between the measurement and simulation results will be shown and discussed. All amplifiers that are discussed in this thesis are steps towards the realisation of the targets that are listed in table 7.1.

Table 7.1: Final high-power amplifier design goals.

Specification	Goals
Frequency band	8.5 – 11.5 GHz
Output power	9 – 10 Watt
Power added efficiency	> 25%
Transducer gain	30 dB

The amplifiers must be able to operate under both pulsed and CW operating conditions. For the realisation of the combined driver and high-power amplifier, discussed in section 1.1, a transducer gain G_T of 30 dB is needed. The required gain and output power are realised with a number of amplifier designs. Each amplifier, discussed in the next sections, has a higher output power and if possible a higher gain than the previous one. In section 7.2, the high-power amplifiers developed with the help of the DIOM20HP MESFET process of Infineon are discussed. The results of the amplifiers developed in the HFET process of FhG-IAF are given in section 7.3. A comparison between the results obtained with both technologies and the results, which can be found in literature, is presented in section 7.4.

7.2 MESFET amplifier results

In this section, the realised MESFET amplifiers are discussed. The first designs realised in the DIOM20HP process were one-stage amplifiers that aimed at an output power of 2-Watt [7.1]. The results of one of these amplifiers (HPA #1) are listed in table 7.2. The results show that the obtained gain is very low. Therefore, from that point in time only amplifiers with two or more stages were designed. As a next step 3-Watt and 5-Watt high-power amplifiers (HPA #2 and #3) were designed, manufactured and tested. The measurement results [7.2, 7.3] are also listed in table 7.2. These results were at that moment in time (1994 - 1995) actual state-of-the-art. All high-power amplifier designs mentioned before were

based on transistors that have an interdigitated layout, see section 2.3.4. Only the gate-to-gate spacing was varied. For the 2-Watt designs, a 50 µm gate-to-gate spacing was used and for the 3 and 5-Watt designs a 30 µm gate-to-gate spacing. A reduction of the gate-to-gate spacing to 30 µm is still acceptable from a reliability point as it was discussed in section 5.3.5. For the 7 - 10 and 10 - 12 Watt high-power amplifiers (HPA #4 and #5) so-called fishbone transistor layouts were used, see section 2.3.4. This type of transistor layout was used to keep the chip area as small as possible while at the same time the output power is increased with the help of larger transistors. The 7 - 10 Watt and 10 - 12 Watt high-power amplifier designs also focused on the design of amplifiers that have both state-of-the-art output power and at the same time also have a high gain. For this reason, also the number of amplifier stages was increased from two to three for the 7 - 10 Watt high-power amplifier and to four stages for the 10 - 12 Watt high amplifier. The measurement results of the 7 - 10 Watt amplifier [7.4] and 10-12 watt amplifier [7.5] are summarised in table 7.2. Photographs of the first four amplifiers can be found in appendix I.

Table 7.2: Summary of the measured performance under pulsed conditions of the high-power amplifiers that are realised in the Infineon DIOM20HP MESFET process. A pulse width of 10 µs and a pulse repetition frequency of 20 KHz have been used.

HPA	P_{OUT} *target* [W]	Frequency band [GHz]	P_{OUT} [W]	*PAE* [%]	G_T [dB]	# stages	Chip size [mm^2]
#1	2	8.5 - 10.5	2.5 – 2.9	30 - 41	4.0-4.6	1	16.0
#2	3	8.0 - 11.3	2.8 – 4.1	30 - 43	9.3-11.1	2	9.0
#3	5	7.8 - 10.6	5.0 – 7.1	30 - 40	12.0-13.5	2	22.0
#4	7 - 10	8.0 - 10.0	6.9 – 11.2	18 - 27	12.4-14.5	3	25.0
#5	10 - 12	8.5 - 10.5	8.5 – 10.5	27 - 32	19.3-20.2	4	32.5

In the remainder of this section, the results of the 10 - 12 Watt amplifier see figure 7.1, will be discussed in more detail. A comparison will be shown between small-signal measurement and simulation results and an explanation for the measured output power level will be given.

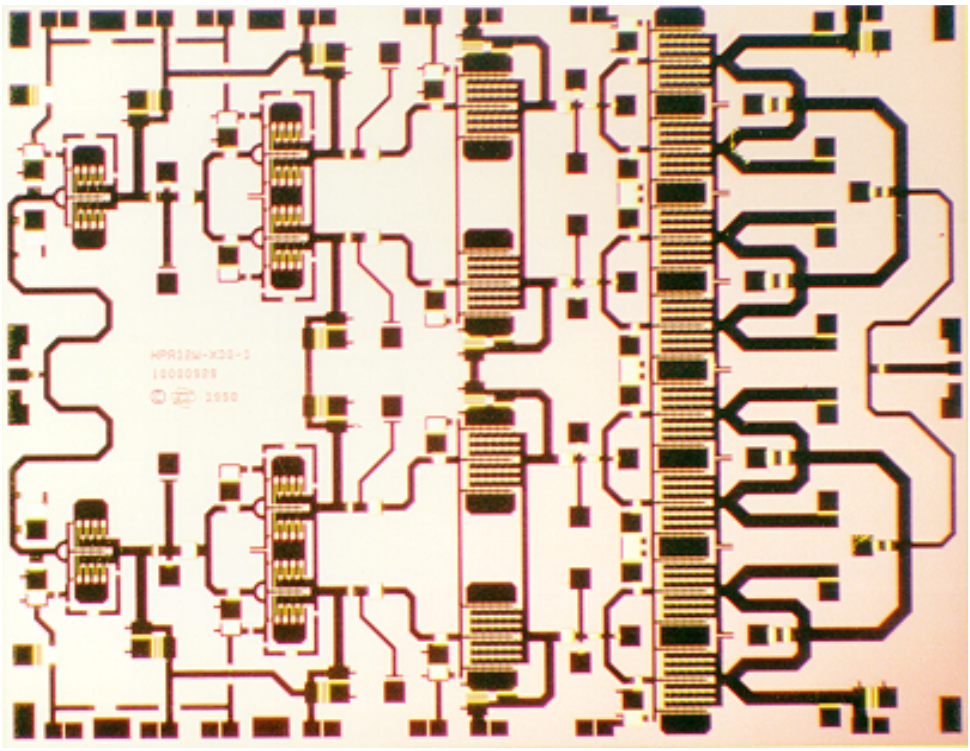


Figure 7.1: Photograph of the 10 - 12 Watt high-power amplifier that is realised in the Infineon DIOM20HP MESFET process. Chip size is 6.5 x 5.0 mm^2.

This amplifier aimed at the realisation of the target specifications that are mentioned in table 7.1. To realise the high-gain requirement four amplifier stages have been used. This is necessary due to the relatively low power gain of the MESFETs used, see also section 2.3.2. Nevertheless, the specified gain target can not be reached in simulation or in measurement as it can be seen from the results depicted in figure 7.2. The use of five or more amplifier stages was not considered as an option due to the increase in chip size. It can be concluded that an amplifier based on the used MESFET technology is not suitable for use in a two or three chip TR module, in which a gain of 30 dB is required.

In figure 7.2, a comparison is made between the simulated and measured S-parameters of the amplifiers. For this simulation, the S-parameters that are measured for unit transistor cells from the same wafer have been used. In addition, measured S-parameters have been used for some parts of the matching networks. More details regarding the comparison between the simulation and measurement results of the test structures can be found in [7.5].

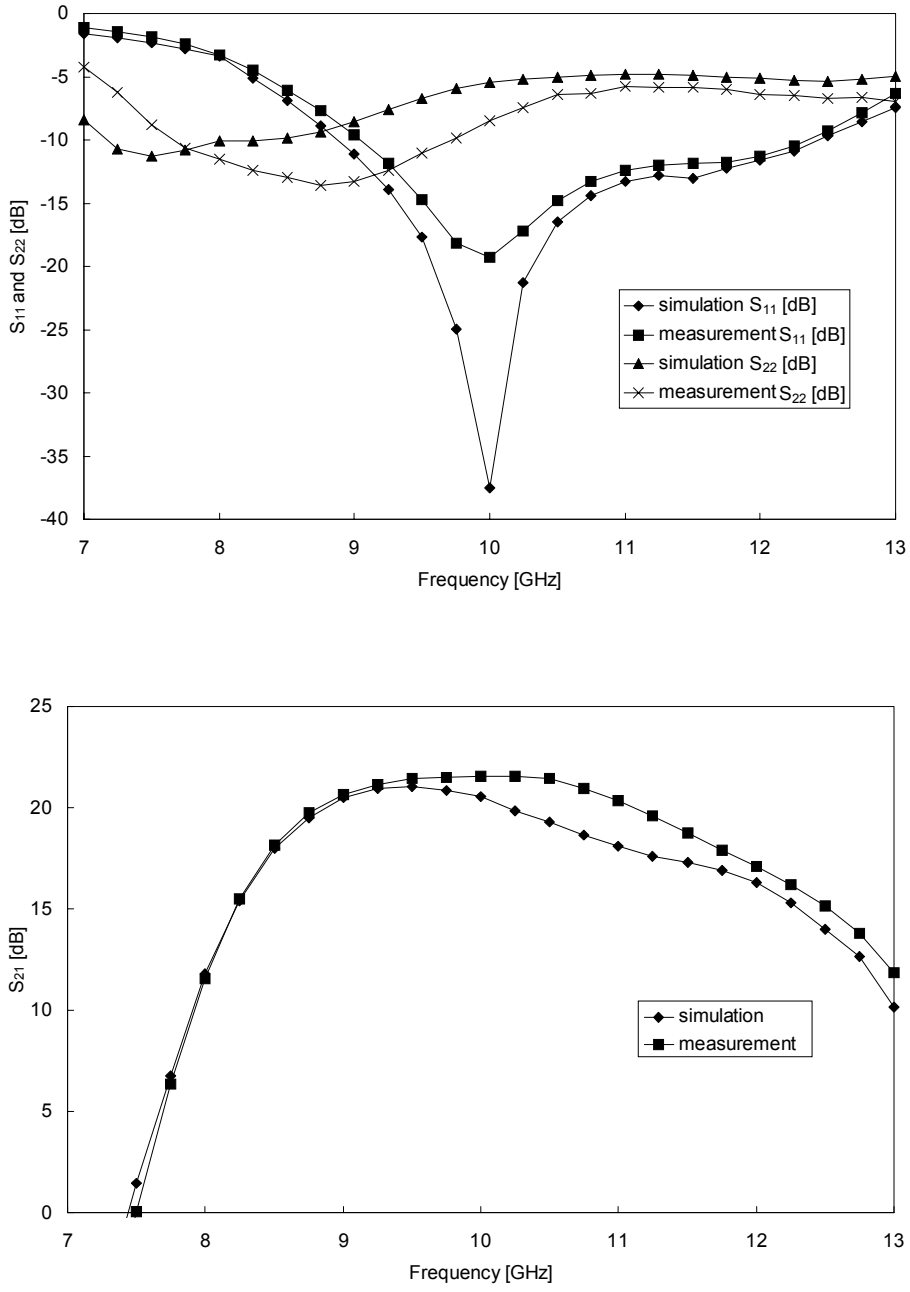


Figure 7.2: Comparison between measured and simulated S-parameters at V_{DS} = 9 V and V_{GS} = -0.8 V, T_A = 25 °C, PW = 10 µs and PRF = 20 kHz.

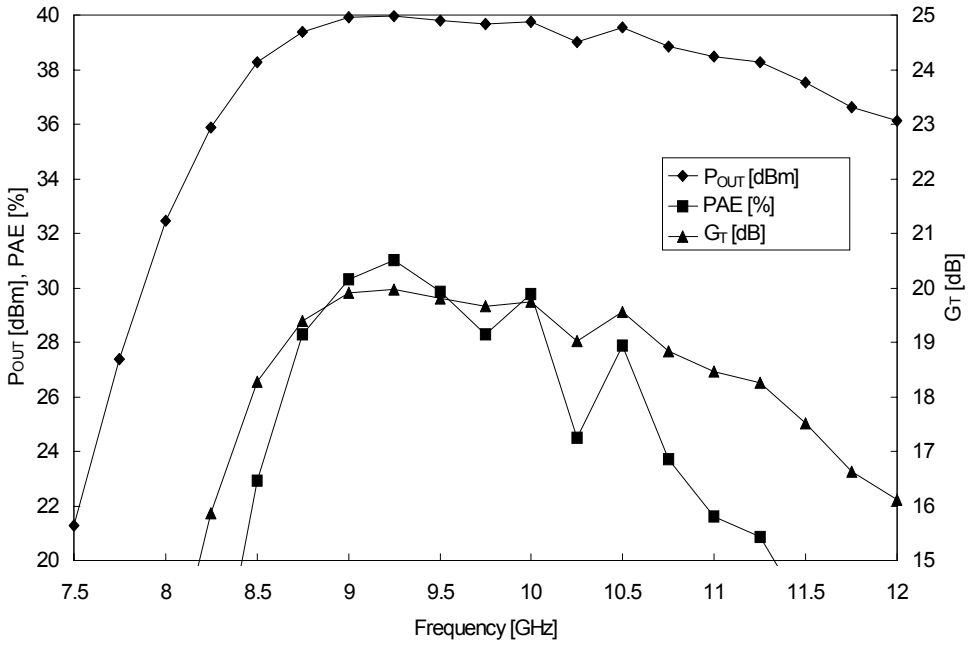


Figure 7.3: Large-signal measurement results at V_{DS} = 9 V, V_{GS} = -0.8 V, T_A = 25 ° C, PW = 10 μs and PRF = 20 kHz.

The results from figure 7.2 show that there is a good agreement between the S-parameters measured and simulated as a function of frequency. For the S_{21} a slope can be observed in both the simulation and measurement results for frequencies above 10.5 GHz. This slope is caused by changes in the gate inductance and/or modelling of the matching networks at the input of the transistors. The value of the gate inductance for the transistors used in this amplifier are around 65 pH as was discussed in section 6.3.3. For this value of the gate inductance in combination with a 4 mm gate width transistor the behaviour of the interstage-matching network is critical as it was shown in section 6.3.3. It is advisable to increase the value of the gate inductance by putting more line length in series with the gate. In this way, the influence of the gate inductance on the overall amplifier performance as a function of frequency is reduced. This approach is successfully demonstrated in an 8 - 10 Watt MESFET amplifier, which cannot be discussed here due to the non-disclosure agreement with the customer.

The measured large-signal performance of the amplifier is depicted in figure 7.3. The measured bandwidth is similar to the small-signal results but smaller than expected. Nevertheless, an output power between 39.3 and 40.2 dBm has been measured over the 8.5 - 10.5 GHz frequency band. This output power is approximately one dB lower than expected. This can be explained by a change in the performance of the transistor cells when compared to the ones on which the design was based. Evidence of this can be seen from the

results of a load-pull measurement of the current transistor cell and the one that was used during the design of the amplifier.

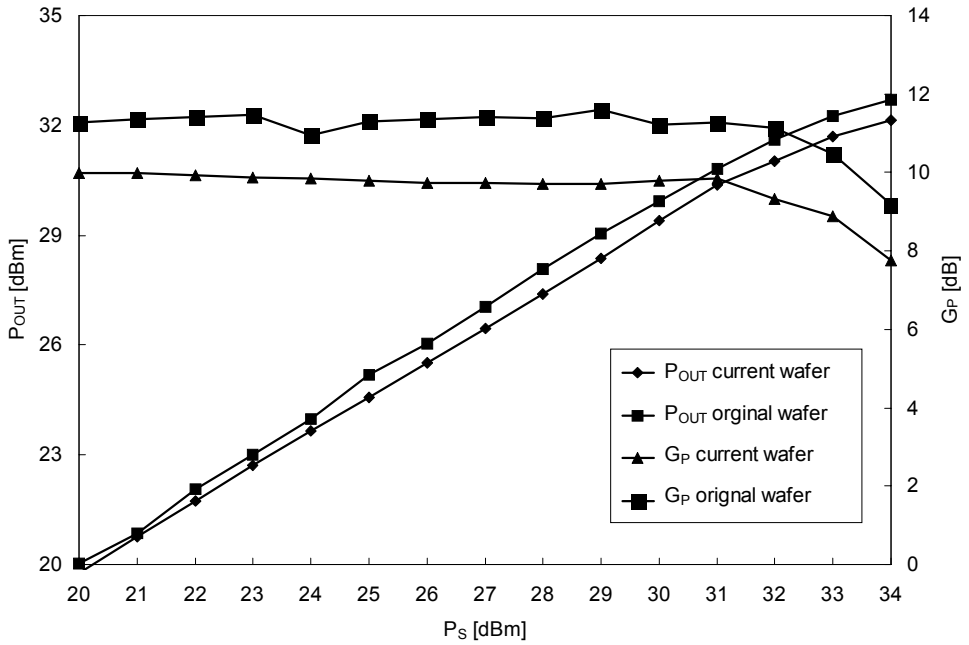


Figure 7.4: Comparison of output power and power gain, of the transistor used in the output stage of the amplifier (N_{GF} = 48, W_U = 83 μm), measured on the current wafer and the wafer on which the transistor model was based on. Measurements are performed at V_{DS} = 9 V, V_{GS} = -1.25 V, f = 8 GHz and Γ_L = 0.7/180°.

The load-pull measurement results from figure 7.4 show that both the output power and the power gain are reduced by approximately one dB. This reduction explains both the reduced output power and gain that has been measured. To increase the gain of the amplifier a higher gate voltage has been used. The measured power added efficiency is still better than specified. The measurement results show that it is difficult to achieve the goals that have been listed in table 7.1. Especially the gain is a difficult specification to meet. To achieve this specification more than one additional amplifier stage has to be added, which will result in an unacceptable larger occupied chip area. Nevertheless, the obtained results demonstrate that it is possible to realise a single chip high-power amplifier at X-band that has an output power of 10 Watt combined with an acceptable power added efficiency and gain. Additional results of MESFET amplifiers not discussed in this thesis can be found in [7.6 - 7.8].

7.3 HFET amplifier results

In this section, the measured performance of the high-power amplifiers that are designed using the FhG-IAF high-power HFET process is discussed. The design of the amplifiers realised in the HFET process was done in parallel with the amplifier designs discussed in the previous section. The HFET technology used has an output power of 0.7 – 0.8 W/mm, as it was discussed in section 5.7. This technology is used in combination with a fishbone transistor layout for the development of 5 - 10 Watt power amplifiers that combine high output power and high gain with a small-occupied chip area. A summary of the obtained results is listed in table 7.3. These amplifier results clearly demonstrate that, with the help of the used HFET technology, it is feasible to combine both the driver amplifier and the high-power amplifier on a single chip.

Table 7.3: Summary of the measured performance of the in the FhG-IAF high-power HFET process realised high-power amplifiers under pulsed conditions. Note that the results are summarised at V_{DS} = 8 V. A pulse width of 10 μs and a pulse repetition frequency of 20 kHz has been used.

HPA	P_{OUT} *target* [W]	Frequency band [GHz]	P_{OUT} [W]	*PAE* [%]	G_T [dB]	# stages	Chip size [mm^2]
#1	5 - 7	7.0 – 11.0	5.2 – 7.6	32.3 - 40.8	20.2 - 21.8	2	16.0
#2	9 - 10	8.0 – 11.0	5.4 – 7.4	23.1 - 33.8	28.4 - 29.7	3	20.0

The first amplifier (HPA #1) listed in table 7.3 aimed at an output power between 5 and 7 Watt. The purpose of this design was to investigate whether it was feasible to realise a single chip power amplifier, which combines high-gain with high output power. From the start of the design, it was decided to fix the width of the amplifier chip to 4 mm. This in combination with the choice for transistors that have a fishbone layout led to an amplifier topology that has eight transistors in parallel. Consequently, the unit gate width of the used transistors was fixed to 45 μm, see section 5.7. The number of gate fingers that was used is 32. Therefore, a nominal output power of 7.5 Watt is expected, see section 5.7. It was decided to design a two-stage amplifier taking into consideration that this was a first step in the realisation of the goals that are mentioned in section 7.1.

A photograph of the realised high-power amplifier is depicted in figure 7.5. As can be seen a very compact high-power amplifier was designed. A lot of electromagnetic coupling is present which must be accounted for. Also the use of accurate models for both transistors and passive components, as described in chapter 4, is essential in obtaining a good result. Very good agreement between the measured and the simulated results over almost the entire frequency band is found and demonstrated with the small-signal measurement results depicted in figure 7.6. The only exception is found between 6.5 and 7.0 GHz where a peak in the S_{21} is visible, see figure 7.6 b). This peak indicates that transistors are used in the neighbourhood of their unstable region. Nevertheless, no oscillations were detected during the measurements of this amplifier.

The measured large-signal performance at a nominal drain voltage of 8 V is shown in figure 7.7. The depicted results show that the 5 - 7 Watt output power target is reached over a relative frequency band of more than 40%. Over the 7.0 to 11.0 GHz frequency band an average output power of 6.1 Watt, a power added efficiency of 36% and a gain of 20.8 dB is measured. The breakdown voltage of the used process is > 20 V. Therefore, it was possible to operate the amplifier at a higher drain voltage. The results when a drain voltage of 10 V was used are depicted in figure 7.8. Over the 7.0 - 11.0 GHz frequency band an average output power of 9 Watt, a power added efficiency of 35% and a gain of 20 dB were measured. These excellent results demonstrate the potential of the used HFET technology for the realisation of power amplifiers that combine a high output power with a high gain on a small chip area.

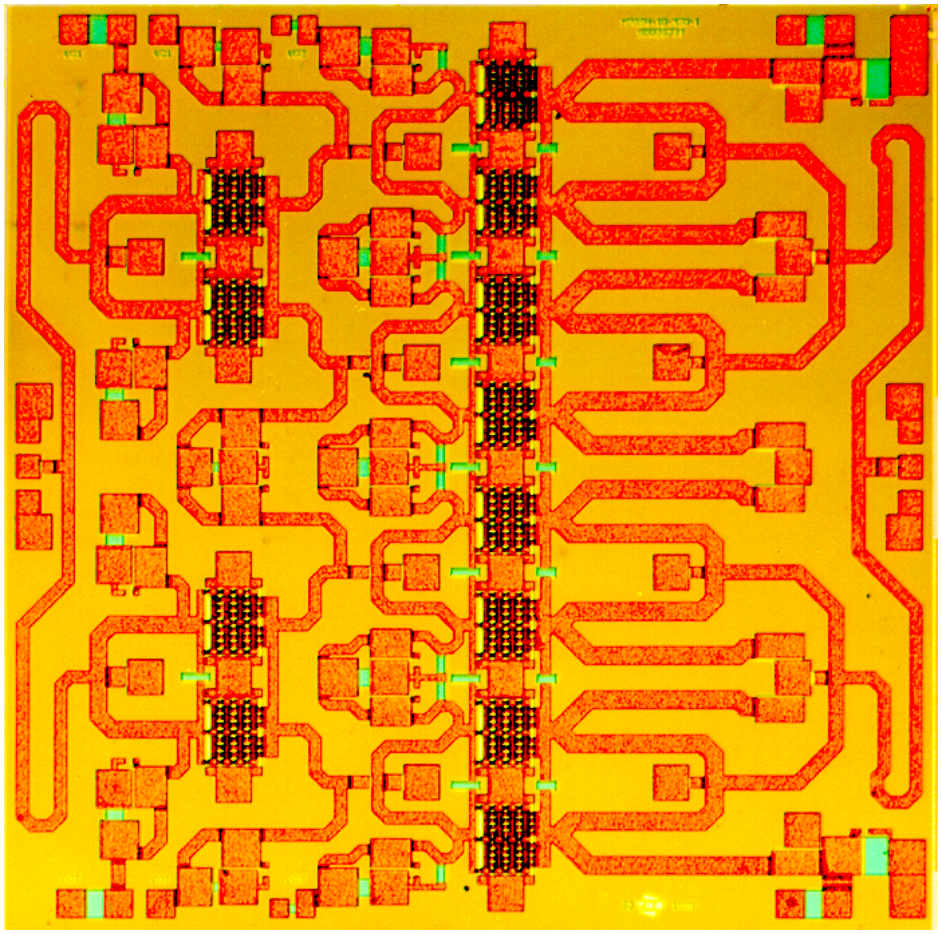
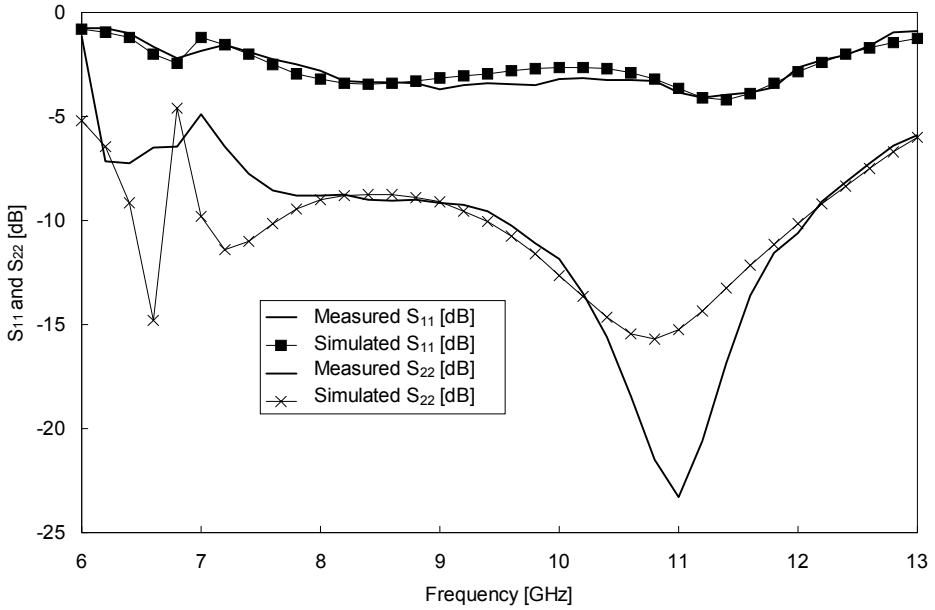
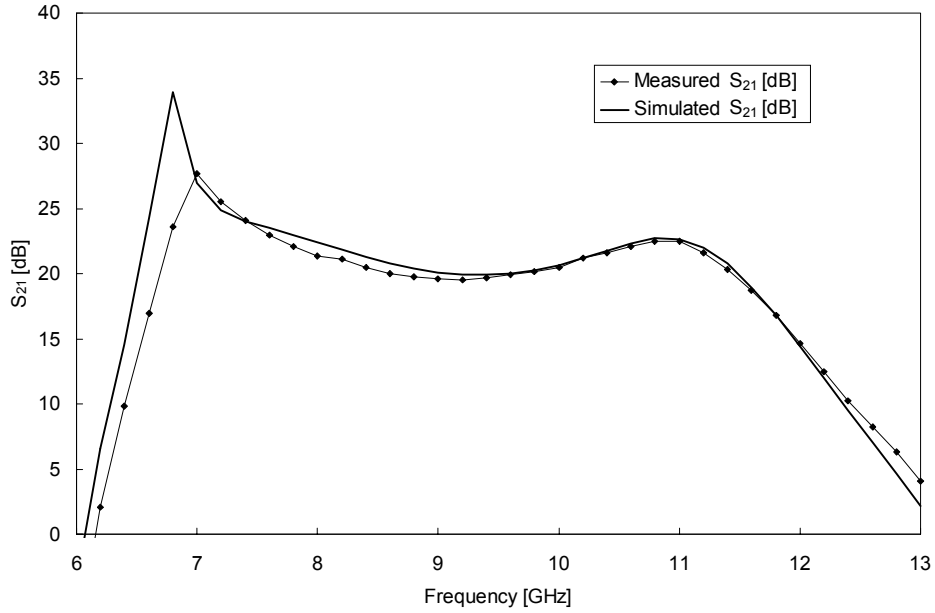


Figure 7.5: Photograph of the 5 - 7 Watt high-power amplifier that is realised in the FhG-IAF HFET process. Chip size is 4 x 4 mm^2.



a)



b)

Figure 7.6: Comparison between measured and simulated S-parameters at V_{DS} = 8 V and V_{GS} = -0.3 V, T_A = 25 °C, PW = 10 µs and PRF = 20 kHz.

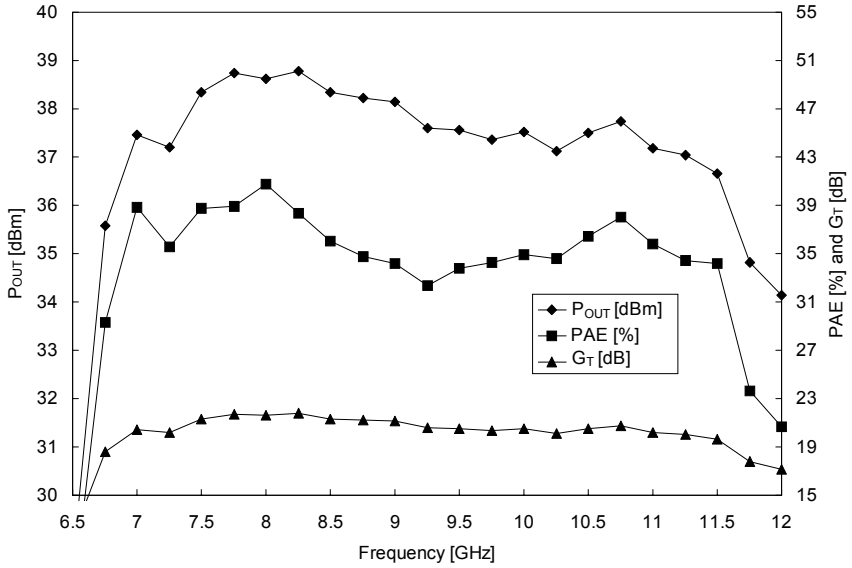


Figure 7.7: Large-signal measurement results 5 - 7 Watt HFET amplifier at V_{DS} = 8 V, V_{GS} = -0.3 V, P_S = 17 dBm, T_A = 25 °C, PW = 10 µs and PRF = 20 kHz.

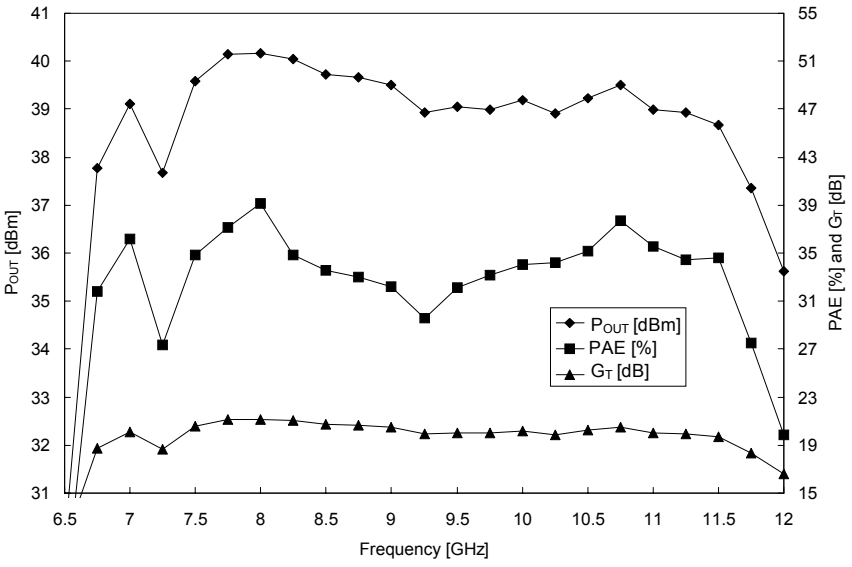


Figure 7.8: Large-signal measurement results 5 - 7 Watt HFET amplifier at V_{DS} = 10 V, V_{GS} = -0.3 V, P_S = 19 dBm, T_A = 25 °C, PW = 10 µs and PRF = 20 kHz.

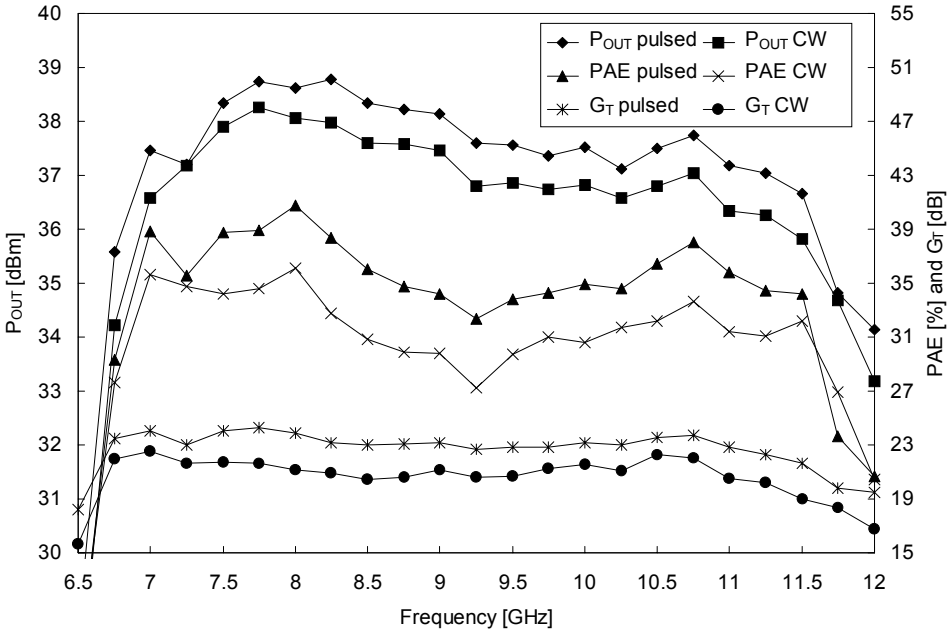


Figure 7.9: Comparison pulsed and CW large-signal measurement results 5 - 7 Watt HFET amplifier at V_{DS} = 8 V, V_{GS} = -0.3 V, P_S = 17 dBm pulsed and P_S = 18 dBm CW, T_A = 25 °C, PW = 10 μs and PRF = 20 kHz.

A comparison of the amplifier performance when operated under pulsed and CW conditions is shown in figure 7.9. The pulsed results are obtained at an ambient temperature of 25 °C. No external cooling was applied during the CW measurements of the amplifier. Consequently, the ambient temperature of the chuck on which the amplifier was mounted increased to 55 °C. Thermal calculations with the values and program discussed in section 5.3.4 show a temperature increase, of the gate fingers in the CW mode, of 82 °C. This temperature increase results as expected in both a reduction of the output power and the gain. Consequently, also the power added efficiency is reduced. The measured performance under CW conditions is excellent. More measurement results are presented in [7.9, 7.10]. In these references, also the amplifier design is discussed in more detail.

The next step that was taken was the design of a two-stage amplifier with larger transistors in the output stage. The size of the transistors was increased to realise a higher output power. The results of this amplifier can be found in reference [7.11].

The last amplifier discussed in this thesis is a three-stage amplifier, which also uses a transistor with an increased size in the final amplifier stage. This amplifier is intended as demonstrator of the feasibility of a single chip combined driver and high-power amplifier that has sufficient gain to realise the two-chip or three-chip TR module which was

mentioned in section 1.1. A picture of the realised amplifier is shown in figure 7.10. The amplifier is realised on a very small chip area of only 20 mm^2. The large-signal measurement results are depicted in figure 7.11. A summary of these measurement results is listed in table 7.3. The output power is lower than expected. This is caused by a change of the C_{ds} of the transistors when compared to the one on which the design was based. Consequently the location of the optimum load impedance is changed and the obtainable output power for the designed load is reduced. Nevertheless the results [7.12] demonstrate that it is feasible to realise a power amplifier that combines both a high output power and a high gain on a small chip area. The results show, for a drain voltage of 8 V, from 8.0 to 11.0 GHz, an average output power of 6.5 Watt, an average power added efficiency of 29%, and a gain of more than 29 dB.

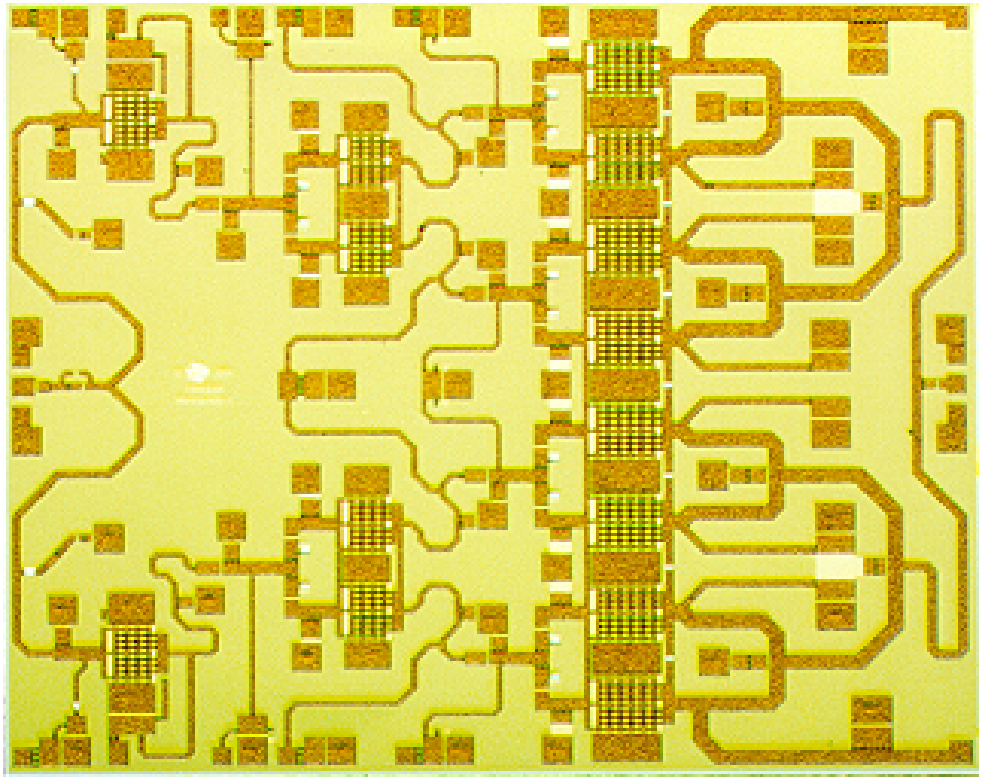


Figure 7.10: Photograph of the 9 - 10 Watt high-power amplifier that is realised in the HFET process of FhG-IAF. Chip size 5 x 4 mm^2.

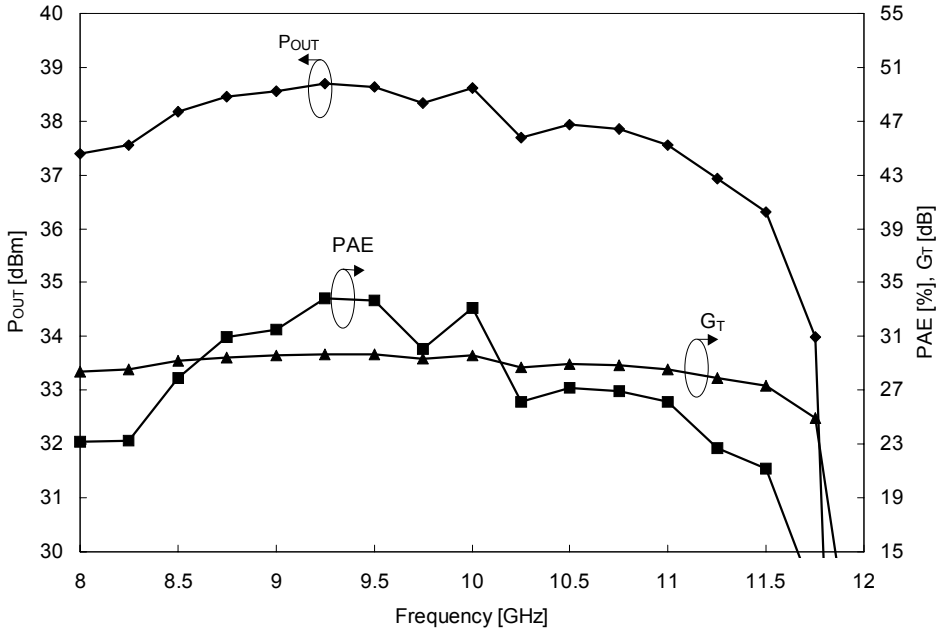


Figure 7.11: Large-signal measurement results 3-stage HFET power amplifier. Measured at V_{DS} = 8 V, V_{GS} = -0.15 V, PW = 10 μs and PRF = 20 kHz.

7.4 Comparison with published X-band HPA results

In the previous sections, the results of the MESFET and HFET high-power amplifiers developed in the scope of this thesis are discussed. In this section, a comparison will be made with the performance of amplifiers that can be found in literature. In addition, it will be investigated, which transistor technology shows, at this moment in time, the largest potential for the realisation of X-band high-power amplifiers. For this purpose a literature search of amplifier results published during the last decade, realised with MESFET, HFET and HBT technology, is performed. The HBT results are included in this section to see which of the before mentioned three transistor technology has the largest potential. The results discussed in this thesis [7.13 - 7.27] are selected based on the following criteria; a relative frequency bandwidth of at least 20% at X-band, a gain of at least 9 dB and all matching networks are included on the chip.

The numbers given in the remainder of this section are the average values obtained over the frequency band of interest. A summary of the measured performance is given in appendix J. In figure 7.12, the realised output power density per chip area is shown as a function of the

measured output power. These results show that the highest output power densities are obtained with the HFET technology. This is remarkable considering the higher output power density per transistor quoted for HBT technology (2 - 3 W/mm compared to 0.7 - 1 W/mm for HFET). In addition, also one MESFET amplifier [7.16] has a measured output power of 12 Watt. This demonstrates that MESFET technology used for X-band high-power amplifier is not only a relatively cheap option but also amplifiers with a high performance can be realised. The results also show that the obtained output power for the in this thesis discussed high-power amplifiers are among the highest quoted for monolithic integrated X-band power amplifiers.

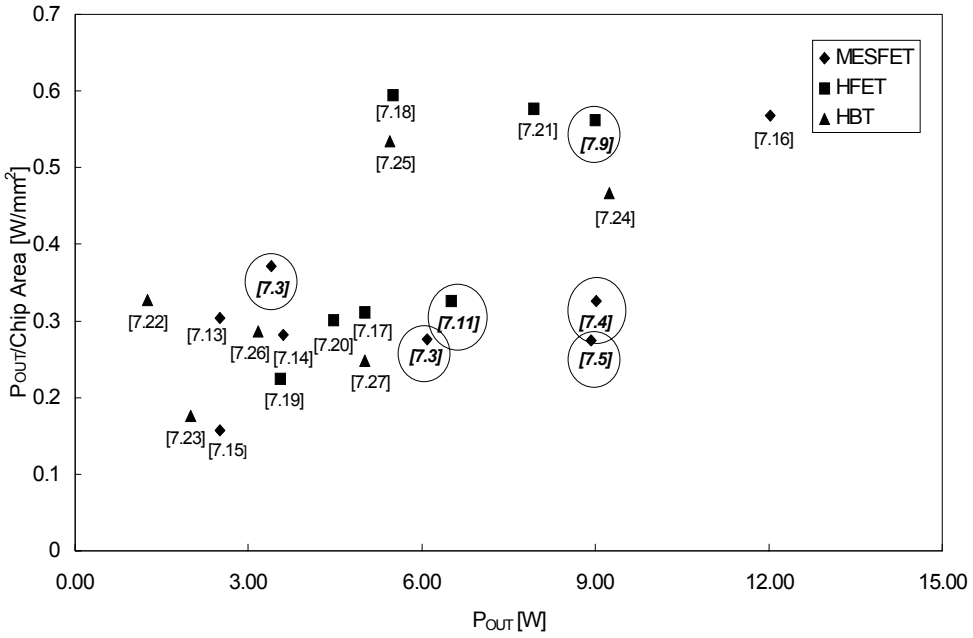


Figure 7.12: Measured output power density per chip area as a function of the measured average output power. The amplifiers designed in the scope of this thesis are indicated with bold italics and circles.

Of course output power and output power density, are not the only relevant figures of merit for analysing the performance of a high-power amplifier. Other relevant factors are the obtained gain, power added efficiency and bandwidth. To analyse the performance of a power amplifier with respect to these factors a new figure of merit is introduced:

$$C_{HPA} = \frac{P_{OUT} \cdot G_T}{Chip\_area}, \tag{7.1}$$

in this equation the output power is given in [W], the gain in [dB] and the chip area in [mm^2]. The measured C_{HPA} as a function of the measured power added efficiency is shown in figure 7.13. The results show that the best performance is obtained with HFET

technology. The majority of the depicted power amplifiers has a power added efficiency between 35% and 40%. The majority of the amplifiers discussed in the scope of this thesis have an average power added efficiency between 30% and 35%. At this point it is good to note that the discussed amplifiers are mainly optimised for maximum output power. Load-pull measurements show that the power added efficiency would have been 5% higher when the performance of the amplifier would have been optimised for maximum efficiency. On the other hand the output power would have been ≈ 0.5 dB lower.

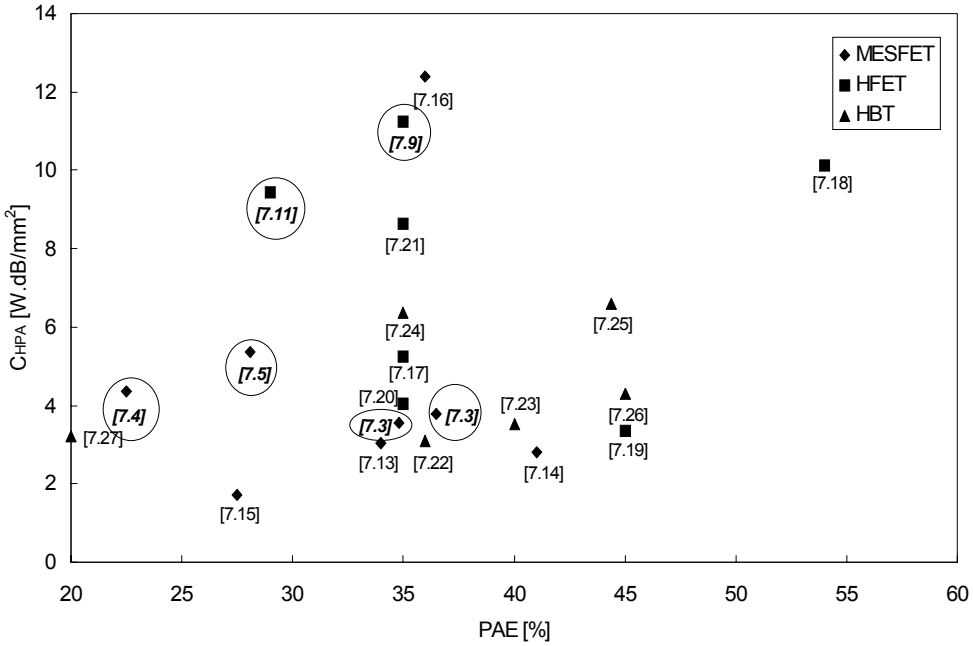


Figure 7.13: Measured figure of merit C_{HPA} as a function of the measured average power added efficiency. The amplifiers designed in the scope of this thesis are indicated with bold italics and circles.

The measured C_{HPA} as a function of relative frequency bandwidth is shown in figure 7.14. The largest relative bandwidths, up to 60%, are obtained with the help of HFET and HBT technology. With the help of MESFET technology relative bandwidths up to 40% are realised. The results of the amplifiers discussed in this thesis show an average bandwidth between 30% and 40%, which was to be expected regarding the fact that this was the targeted frequency bandwidth.

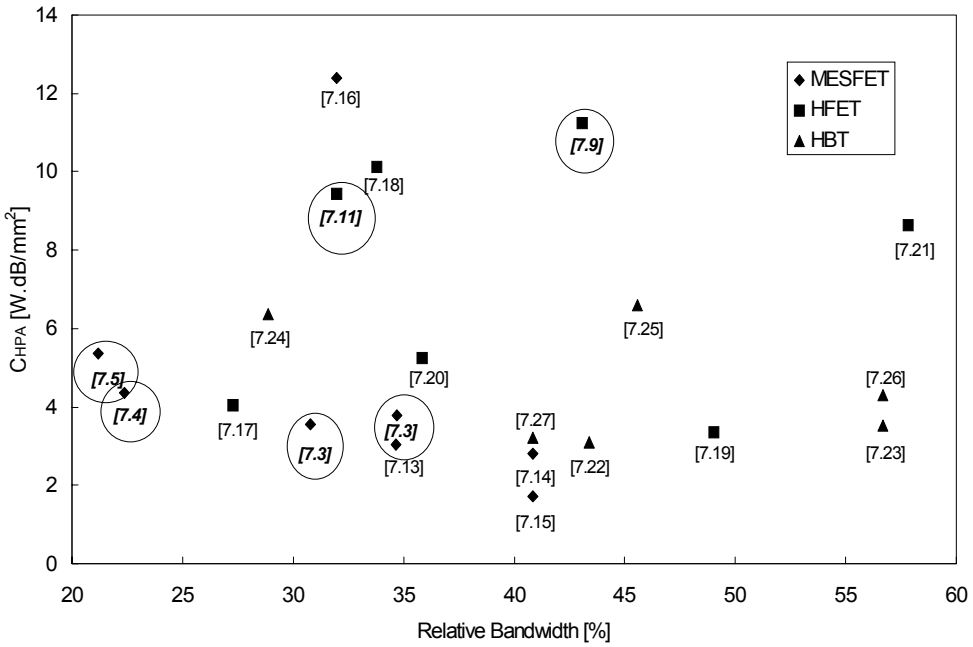


Figure 7.14: Measured figure of merit C_{HPA} as a function of the measured relative frequency bandwidth. The amplifiers designed in the scope of this thesis are indicated with bold italics and circles.

It can be concluded from the results shown in figures 7.12 - 7.14 that at this moment in time the best results are obtained with the help of HFET technology. The better performance of the HFET technology over the HBT technology can be explained by the higher gain of the HFET technology at X-band. Consequently, smaller HBT unit transistor cells can be used when compared to HFET transistor cells to get sufficient gain at X-band for the HBT transistor cells. Therefore, the HFET amplifiers have a higher output power density than the HBT amplifiers. In addition, also the gain of the complete amplifier will be higher when HFET technology is used.

7.5 Conclusions

In this chapter, the results of the amplifiers designed with the models and design techniques discussed in the previous chapters are presented. From a comparison between the simulated and measured small-signal results of amplifiers designed in both MESFET and HFET technology, it can be concluded that there is an excellent agreement. This demonstrates that with the models that are discussed in this thesis excellent results are obtained. For most of the discussed amplifiers the targeted output power is reached or at least approached. In both

technologies, peak output powers of 10 Watt are realised. In table 7.4 a comparison is given between the 10 - 12 Watt MESFET amplifier and the 5 - 7 Watt HFET amplifier. The first amplifier is biased at 9 V and the latter amplifier is biased at 10 V to make a realistic comparison of the output power possible.

Table 7.4: Comparison of measurement results 10 - 12 Watt MESFET HPA with 5 - 7 Watt HFET HPA.

HPA	Technology	Frequency band [GHz]	P_{OUT} [W]	*PAE* [%]	G_T [dB]	# stages	Chip size [mm^2]
#5	MESFET	8.5 - 10.5	8.5 – 10.5	27.0 - 32.0	19.3 - 20.2	4	32.5
#1	HFET	7.5 - 11.0	7.8 – 10.5	29.6 - 37.7	19.9 - 21.2	2	16.0

The results as listed in table 7.4 clearly show that similar results with respect to gain and output power are realised in both technologies. The big advantage of the discussed HFET amplifier is the occupied chip area, which is only 50% of the MESFET chip area. This reduced occupied chip area is made possible by the higher output power density and gain, see section 5.7, of the HFET process when compared with the MESFET process.

The results of the second HFET amplifier that are listed in table 7.3, demonstrate the feasibility of realising the single chip combined driver and high-power amplifier that was mentioned in chapter 1.

A comparison of the amplifiers discussed in this thesis with the ones that are described in literature shows that:

- State-of-the-art output power of 10 Watt is realised in both MESFET and HFET technology.
- The performance with respect to power added efficiency is average.
- The average relative bandwidth that is obtained is between 30% and 40%, which is quite logical considering the fact that this is bandwidth, for which the amplifiers were designed.
- A unique gain of 29 dB has been measured for a high-power amplifier designed with HFET technology.

A comparison of the amplifier results measured for the various transistor technologies shows that the best performance with respect to output power, gain, power added efficiency, bandwidth and chip area is obtained with HFET technology. The better performance of the HFET technology is due to the higher gain of the transistors at X-band.

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8. Conclusions

8.1 Introduction

The steps necessary for a successful design of high-power amplifiers for use in phased-array radar are discussed in this thesis. In this final chapter, the developed design methodology and the results obtained will first be summarised. Then the applicability of the techniques discussed in the design of power amplifiers for both higher as well as lower frequency ranges, and other applications and operating classes, is considered.

8.2 Summary of high-power amplifier design procedure and results

The discussion of the design procedure of high-power amplifiers started with the flow graph given in the introduction. The first points shown in this flow graph are the selection of a technology and a foundry to produce the amplifiers. For the work described in this thesis a MESFET and a HFET process were chosen. The choice for the MESFET process was based on the expectation that it could produce high performance amplifiers that can be used in a commercial application. As MESFET process, the DIOM20HP process of Infineon is used. This process was optimised by Infineon for X-band performance. This has been achieved by reducing the gate length from 0.8 to 0.5 μm and optimising the doping profile. The capability of the FhG-IAF HFET process used in this thesis progressed during this work from low-power to high-power applications. HFETs were taken into consideration due to the inherent better performance of these transistors. It was expected, and demonstrated in this thesis, that this process would enable the development of small-sized combined driver and high-power amplifiers for phased-array radar applications. The use of HBT technology was, at the beginning of this work in the early 1990's, not considered an option from a reliability point of view [8.1, 8.2]. Nowadays most of the reliability problems are solved [8.3, 8.4, 8.5] and HBT technology is a serious alternative for the above mentioned technologies.

The relevant figures of merit for the transistors used for high-power amplifier design are; output power, gain and power added efficiency. It is shown in this thesis that the transistor gain is crucial for both the performance of the transistors and the performance of the complete high-power amplifier. The gain of the transistors should be as high as possible. Therefore, it is expected that the HFET technology, which has both a higher output power density and a higher gain, will result in better more compact power amplifiers, than the MESFET technology.

An overview of the available active and passive components and their limitations is given in chapter 2. Limiting factors are identified for the output power of a transistor. In addition, it

is shown, which passive components can be used. The limiting factor for the transmission lines and the spiral inductors are the maximum current density that can flow through a given line width. For the MIM capacitors, the breakdown voltage is the limiting factor. Therefore, the capacitors to ground used in the output-matching network of the amplifier are realised with the help of two capacitors in series.

Before the high-power design is started, the availability and accuracy of the models for both active and passive components should be evaluated. For the technologies applied here, no transistor model was available for the gate widths used. In addition, the accuracy of the MIM capacitor model turned out to be insufficient for use at X-band. The same was the case for some of the important discontinuity models, e.g. T-junctions, available in the commercial design software. These factors led to the development of the integrated measurement system and calibration algorithms discussed in chapter 3. The measurement system developed is capable of performing the following measurements:

- DC measurements necessary for transistor modelling.
- Two and three-port S-parameter measurements. These measurements are used for both the modelling of transistors and passive components. It is also shown that the influence of the transition of the coplanar probes to the measurement system must be removed from the measurement results. For this purpose, self-developed on-wafer Line Reflect Line calibration standards and calibration algorithms are used.
- The active load-pull measurement system is used to determine the accuracy of the transistors models. This measurement system is also used to obtain the load impedances to be used for the design of the matching networks. The measurement time of a single measurement with the load-pull system was long. To reduce this measurement time a novel load-pull search algorithm was developed.
- For the characterisation of the high-power amplifiers the load-pull measurement system is used with the active load replaced by a fixed 50 Ω termination.

Integration of all these measurements into one system has led to more accurate and repeatable measurement results.

The Agilent EEFET3/EEHEMT1 large-signal transistor model has been adopted. With the help of load-pull measurements it is shown, that the large-signal prediction of this model is acceptable for the design of high-power amplifiers. Only the drain current and consequently the power added efficiency are predicted incorrectly. A simple correction factor of 0.85 times the simulated drain current, yields good results for the various transistor sizes used in this thesis. Electromagnetic field simulations have been used to develop models of five different microstrip discontinuities (45° bend , 90° bend, T-junction, Y-junction and crossing.) Comparison of these models with measurements shows good agreement. In chapter 4, additional models are presented for an MIM capacitor, a microstrip line that is used as inductor, and one and two-port viahole models. Again good agreement between modelled and simulated results is demonstrated. In all cases, the use of an electromagnetic field simulator to accurately simulate the electrical behaviour is demonstrated. This opens the way to the design of very densely packed matching networks.

The information summarised above is necessary for the design of high-power amplifiers. The first step in the design of an amplifier, after the technology is chosen, is the selection of

the topology. The number of amplifier stages to be used is determined by the gain required of the high-power amplifier, the gain of individual transistor cells and the estimated losses in the matching networks. The performance of the transistors used in the output stage significantly influences the overall amplifier performance, as it is shown in chapter 5. In this chapter, it was also demonstrated that for the technologies used, the influence of the amplifier stage driving the output stage, on overall performance (PAE) could not be neglected. The loss of the output-matching network must also be as low as possible from both an output power and a power added efficiency viewpoint. In chapter 5, it is shown that the layout of the transistors has a paramount influence on both the RF performance and chip area of the total power amplifier. Parameters influencing the performance of the transistors, which can be modified by the designer, include:

- The width of the gate fingers. In general the wider the finger the lower the gain of the transistor. This aspect becomes more important for higher frequencies but is already visible at X-band. The results show that the width of the gate finger should be less than 100 μm to limit gain loss to 0.5 dB.
- The number of gate fingers used in parallel. The results show that based on a fishbone layout the number of gate fingers should be limited to 40.
- The spacing between the gate fingers. From a reliability viewpoint the minimum gate spacing should be ≥ 30 μm when a maximum gate temperature of 125 °C is considered to be acceptable.

These factors give limits for the transistor unit cell. The only variable that is left which is considered in this thesis, is the form of the gate feed network. It is shown that a fishbone layout gives a better result than the normal interdigitated layout for power amplifiers that have an output power > 5 Watt. The fishbone transistor is advantageous from both an electrical and a chip area viewpoint.

Once the topology and the dimensions of the unit cell are selected, it is time to determine the bias point and optimum load impedance. The bias point must be chosen to satisfy the requirement of an as high as possible power added efficiency combined with a high output power. In this thesis, it is shown that class AB biasing leads to optimum results for wideband X-band amplifiers. Operating classes that require harmonic termination are not considered in this thesis due to the 30% to 40% bandwidth required of the amplifiers. This makes the physical realisation of harmonic impedances over the entire bandwidth difficult if not impossible. It is also shown that the large drain to source capacitor at the output of the transistor already forms a short circuit at the higher harmonic frequencies. Care must be taken to ensure that the output capacitance is not parallel resonated at higher harmonic frequencies. Open circuits at these frequencies will reduce the power added efficiency.

The optimum load impedance is determined by both the operating class selected and the choice of an optimum for output power or power added efficiency. There is, as shown in this thesis, a distinct difference between both optima. For most of the amplifiers discussed here, an optimum load impedance for maximum output power was used. As next step, the stability of the transistors has to be investigated. All transistors discussed in this thesis are conditional stable only. This means that additional elements have to be added to guarantee conditional stable behaviour at microwave frequencies. It is not possible to realise this stability on-chip down to low frequencies (< 1 MHz). For this very large decoupling

capacitors greater than 1 nF would have been needed. These are impossible to realise on the same chip as the power amplifier. The network promising the largest stable frequency range for use in the matching networks is a parallel resistor capacitor network at the input of the transistor.

At this point in the design, the unit transistor cells, the operating point and the optimum load impedance are selected. In addition, the stability of the transistors is improved with the help of stabilisation networks. The next point that is considered is the design of the matching networks. First, a model for the source and load impedance of these matching networks is determined. At X-band the model of the source impedance is formed by a series inductor terminated with a parallel capacitor resistor network. It is shown that this is a better representation of the reality than the commonly used parallel capacitor resistor network. The load impedance of the matching networks is formed by a series inductor, resistor and capacitor network. The Bode-Fano limit for this network shows that realising the frequency band required for the output-matching network is no problem. This is also the case for the input and interstage-matching networks although less bandwidth can be realised. However, in practice difficulties arise in realising a good match over the frequency band required for these networks. This is due to the low real part of the input impedance of the transistors used in combination with the losses in the matching elements.

The matching networks must provide the following functions:

- Present the optimum source and load impedances to the transistors.
- Divide or combine the RF power.
- For the input and interstage-matching network, realise a frequency dependent loss.
- Supply the DC bias to the transistors.
- Enhance the stability of the amplifier.

In chapter 6, it is shown that realisation of the networks in the form of low-pass matching networks works well. Different approaches to determine the element values are discussed. A combination of the calculation of the component values of L-matching networks at the centre frequency, in combination with an optimisation of these values, gives results equivalent to the element values calculated on the basis of a theoretical Chebychev approach. This result leads to the conclusion that the matching networks can be designed with the help of elementary networks, like L or pi-networks. The required bandwidth and the physical realisation can then further be improved with the help of optimisation. This approach also makes a simple combination of low and high-pass matching networks possible. After the matching networks are designed, the overall high-power amplifier performance must be optimised. In section 6.5, a method was discussed that makes this possible by using a set of ideal couplers in combination with only one transistor per amplifier stage. The use of only one transistor per amplifier stage is necessary to avoid simulation problems under large-signal conditions.

The generation of the gate bias voltage of the amplifier is discussed. It is shown that the influence of the supply voltages on the gate voltage can be reduced with the help of the gate bias circuit discussed in chapter 6. In addition, the effect of threshold voltage variations is partly compensated for with this bias circuit. The developed gate bias circuit does not

compensate for temperature variations. Further investigations are needed for the realisation of a gate bias circuit, which at the same time compensates for supply voltage variations, component spread and temperature variations.

Finally, after the performance of the amplifier is optimised the stability must be investigated. First, the stability at microwave frequencies is investigated. The stability of the transistors themselves was ensured with the help of stability improvement networks, see section 5.6. Therefore, the amplifier can only become unstable through the existence of on-chip and/or off-chip feedback. The existence of such feedback loops that cause oscillations is automatically investigated by analysing all possible loop transmissions, see section 6.7. Secondly, the existence of odd-mode and parametric oscillations is prevented by using stabilising resistors between the transistors at both the gate and the drain side. The last point that must be taken into consideration is potential low frequency instability caused by the bias supplies. This can be suppressed sufficiently using off-chip-decoupling capacitors.

An overview of the high-power amplifier results obtained is given in chapter 7. A comparison of the performance of these amplifiers with the ones that are described in literature shows that:

- Actual state-of-the-art output power of 10 Watt is realised in both MESFET and HFET technology.
- The performance with respect to power added efficiency is average.
- The average relative bandwidth that is obtained is between 30% and 40%, which is quite logical considering the fact that, this is bandwidth, for which the amplifiers were designed.
- A unique gain of 29 dB has been measured for a high-power amplifier designed with HFET technology. This amplifier demonstrates the feasibility of realising a combined driver and high-power amplifier for phased array radar applications.

A comparison of the amplifier results measured for the various transistor technologies shows that the best performance with respect to output power, gain, power added efficiency, bandwidth and chip area is obtained with HFET technology. This good performance is due to high X-band gain of the HFET transistor cells. This high gain makes the use of relatively large transistor cells possible and consequently amplifiers that combine a high output power density with a high gain can be realised.

8.3 Applicability of techniques and models to other applications

The usability of the models and design techniques, presented in this thesis, for other frequency ranges and applications is assessed in this section. Three different frequency ranges can be distinguished namely: RF frequencies (< 3 GHz), microwave frequencies (3 – 30 GHz) and millimetre frequencies (> 30 GHz). At this moment, the most important lower frequency range, from a commercial point of view is 0.9 – 3.0 GHz. This frequency range is especially important for mobile telephone applications like GSM, DECT, PCS, and CDMA. At millimetre frequencies, systems like MVDS/LMDS are of growing importance [8.6].

From this point of view, it is important to see if and how the techniques presented in this thesis can be applied to other applications.

First, an overview will be given of the techniques discussed in this thesis that can be used for all three different frequency ranges:

1. The same on-chip active and passive components as discussed in chapter 2 can be used. It should be noted that the gate length at millimetre frequencies must be smaller than at RF frequencies to guarantee sufficient power gain for the transistor cells.
2. Similar measurement equipment and measurement techniques as have been discussed in chapter 3, can be used. Although at millimetre frequencies, a different S-parameter test-set is needed.
3. Most of the component models presented are valid to at least 30 GHz. The only exception is the model for an inductor formed with the help of a microstrip line. This model is valid up to approximately 15 GHz. For higher frequencies, the inductance can be realised with the help of a number of pi-networks in series, as are discussed in section 4.3.4.
4. The matching networks can be designed in a manner similar to that discussed in chapter 6. In addition, the overall amplifier simulation, optimisation and stability analysis is the same.

Different at the three frequency ranges is:

1. The amplifier topology and the unit transistor cell size. At RF frequencies in general no transistors are used in parallel; this is possible because unit transistor cells with a large unit gate width and a large number of gate fingers in parallel can be used. Large unit transistor cells can be used because the dimensions of the transistor remain small compared to the wavelength, see section 5.3. The situation is the reverse at millimetre frequencies where only small unit transistor cells can be used. Therefore, a number of transistors have to be used in parallel to realise the output power required. The calculation of the sizes of the unit transistor cells can be done for all three different frequency ranges in a manner similar to the one discussed in section 5.2. For all three frequency ranges the stability of the unit transistor cell must be analysed and ensured, see section 5.6.
2. The operating class and load impedance. For the amplifiers discussed in this thesis the class AB without external harmonic tuning was the optimum operating class, see section 5.4. At RF frequencies, also other operating classes are of interest. For example, RF power amplifiers for mobile telephones (e.g. GSM) are battery supplied. They require long talk and standby times, therefore, it is essential to have a high power added efficiency. An advantage of this type of application is the small bandwidth (< 5%) required. Therefore, excellent results can be obtained with class F and inverse class F harmonic matching schemes [8.7 - 8.9]. At millimetre frequencies, the gain of the transistors is low. Consequently, only class AB can be used. The load impedance of the transistor is lower at RF frequencies and will become higher towards millimetre wave frequencies because the size of the transistors will decrease towards higher frequencies. Additionally for mobile applications the supply voltage will be lower, typically 3.5 V, compared to the voltages used for the amplifiers discussed in this thesis (8 - 9 V). This results, for a given output power, in a lower load impedance.

3. The component values of the matching network. In section 6.2.3.5, it is shown that the component values will decrease with increasing frequency. At RF frequencies, especially the inductors become too large to be realised on-chip. Therefore, off-chip matching with the help of SMD components must be combined with on-chip matching. Another consequence of the large component values is the prevalence of high-pass matching networks over low-pass networks. Then the large inductors can be realised off-chip. In addition, the bandwidth required at RF frequencies is in general lower than the ones discussed in this thesis. Therefore, in general a one section L-type matching network is sufficient to realise the required impedance matching. At millimetre frequencies, the distributed effects starts to increase and it becomes more difficult to use e.g. a capacitor as a lumped element. On the other hand, the wavelength becomes smaller. Therefore, distributed matching networks can be used without unnecessarily increasing the chip area.

At this moment, the techniques discussed in this thesis have been successfully used for the design of high power amplifiers at; 900 MHz, 1800 MHz, 5 - 6 GHz [8.3] and 36 - 43 GHz. For the first three amplifiers extensive use of inverse class F harmonic matching has been made. Resulting for the 5 - 6 GHz amplifier [8.3] in a state-of-the-art high-power amplifier, which combines a 10 Watt output power with a power added efficiency of 50%. The obtained results clearly demonstrate the usability of the models and design methods discussed in this thesis. The models and design procedures discussed are ideally suited for implementation in an automatic design procedure of an expert system. It is expected that implementation of such an automatic design procedure can reduce the design time for X-band microwave power amplifiers from several months to approximately one month.

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List of symbols

α	Attenuation constant	[Np.m^{-1}]
	Calibration factor	[-]
	Fitting factor electron velocity curve	[-]
	Thermal diffusivity factor	[m^2.s^{-1}]
	Empirical current saturation factor	[V^{-1}]
α_1	Conduction angle indicating maximum drain current clipping	[°]
α_2	Conduction angle indicating operating class	[°]
α_3	Conduction angle indicating drain voltage clipping	[°]
a_i	Incident power wave (i = 1,2, ….)	[W$^{0.5}$]
A	Area	[m^2]
AF	Acceleration Factor	[-]
ATT_{VM}	Amplitude setting vectormodulator	[-]
b_i	Reflected power wave (i = 1,2, ….)	[W$^{0.5}$]
B_1	Stability factor	[-]
β	Phase constant	[rad.m^{-1}]
	Calibration factor	[-]
	Empirical transconductance factor	[A.V^{-2}]
BW	Band width	[%]
c	Specific heat	[J.kg^{-1}.K]
	Speed of light	[m.s^{-1}]
C	Constant used for reaction rate	[-]
C_B	Bias decoupling capacitor	[F]
C_{bs}	Capacitor used for modelling high frequency dispersion FET	[F]
C_C	Capacitor used in slope compensation network	[F]
C_{ds}	Drain-source capacitor	[F]
C_{gd}	Drain-gate capacitor	[F]
C_{gs}	Gate-source capacitor	[F]
C_{COMP}	Gain compression correction factor	[-]
C_{EQUI}	Equivalent capacitor value	[F]
C_{EP}	Equivalent capacitance parallel inductor and capacitor network	[F]
C_{ES}	Equivalent capacitance series inductor and capacitor network	[F]
C_{HPA}	Figure of merit HPA performance	[W.dB.mm^{-2}]
C_L	Compression level	[-]
	Capacitor used to model load impedance	[F]
C_M	Capacitor used in matching network	[F]
C_P	Parallel capacitance 45º and 90º bend models, capacitor model, resistor and microstrip line model	[F]
C_{POUT}	Output power correction factor	[-]
C_S	Series capacitance 90º bend models and capacitor model	[F]
	Capacitor used in source impedance model	[F]
C_{STAB}	Stabilisation capacitor	[F]
C_{TEMP}	Temperature correction factor	[-]
C_X	Capacitor used in matching networks (X= 1,2,3, ….)	[F]
C_{xds}	Parasitic drain-source capacitor	[F]
C_{xgd}	Parasitic gate-drain capacitor	[F]
C_{xgs}	Parasitic gate-source capacitor	[F]
Δ	Oscillation condition	[-]

Δ_X	Return ratio (X= 1,2,3, ….)	[-]
d	Depletion depth	[m]
	Thickness dielectric MIM capacitor	[m]
D_1	Diameter top viahole	[m]
D_2	Diameter bottom viahole	[m]
d_{min}	Depth of depletion for forward gate current	[m]
ε_0	Permittivity of free space	[$F.m^{-1}$]
ε_{eff}	Effective permittivity of microstrip line	[-]
ε_r	Relative permittivity	[-]
E	Electric field strength	[$V.m^{-1}$]
E_a	Activation energy	[eV]
E_B	Breakdown field strength	[$V.m^{-1}$]
E_C	Conduction band energy	[eV]
	Critical electric field strength	[$V.m^{-1}$]
E_F	Fermi energy level	[eV]
E_G	Band gap energy	[eV]
E_{DF}	Forward directivity error term	[-]
E_{DR}	Reverse directivity error term	[-]
E_{LF}	Forward load match error term	[-]
E_{LR}	Reverse load match error term	[-]
E_{RF}	Forward error term	[-]
E_{RR}	Reverse error term	[-]
E_{SF}	Forward source match error term	[-]
E_{SR}	Reverse source match error term	[-]
E_{TF}	Forward tracking error term	[-]
E_{TR}	Reverse tracking error term	[-]
E_V	Valence band energy	[eV]
f	Frequency	[Hz]
f_0	Fundamental frequency	[Hz]
	Pump frequency	[Hz]
$2f_0$	Second harmonic frequency	[Hz]
$3f_0$	Third harmonic frequency	[Hz]
f_1	Large-signal simulation frequency S-parameter determination	[Hz]
	Centre frequency matching network without component spread	[Hz]
f_2	Small-signal simulation frequency S-parameter determination	[Hz]
	Centre frequency matching network with component spread	[Hz]
f_C	Centre frequency	[Hz]
f_H	High end frequency band	[Hz]
f_L	Low end frequency band	[Hz]
f_{LRL}	Centre frequency matching network found with LRL calibration	[Hz]
f_{MAX}	Maximum frequency of oscillation	[Hz]
f_T	Cut-off frequency	[Hz]
f_{SH}	Subharmonic frequency	[Hz]
f_{SOLT}	Centre frequency matching network found with SOLT calibration	[Hz]
γ	Propagation constant	[m^{-1}]
	Calibration constant	[-]
γ_{ij}	Immittance parameters (i,j = 1,2)	[Ω, or S or -]
Γ	Reflection coefficient	[-]
Γ_2	Reflection coefficient seen from output DUT to input	[-]
Γ_{IN}	Input reflection coefficient	[-]
Γ_F	Reflection coefficient test-set switch in forward direction	[-]

Γ_L	Reflection coefficient load impedance	[-]
Γ_{OSC}	Product reflection coefficients (> 1 indicated oscillation)	[-]
Γ_{OUT}	Output reflection coefficient	[-]
Γ_R	Reflection coefficient test-set switch in reverse direction	[-]
Γ_S	Reflection coefficient source impedance	[-]
G_A	Power gain in Class A	[-]
G_{IN}	Gain at input load-pull measurement system	[-]
g_m	Transconductance	[S]
G_{MAX}	Maximum available gain	[-]
G_{OUT}	Gain at output load-pull measurement system	[-]
G_P	Power gain	[-]
$G_{P\text{-}1dB}$	Power gain at one dB compression point	[-]
$G_{P\text{-}2dB}$	Power gain at two dB compression point	[-]
G_{P1}	Power gain first stage transistor	[-]
G_{P2}	Power gain second stage transistor	[-]
G_{P_LIN}	Power gain in linear region	[-]
G_{PR}	Power gain reduction factor	[-]
G_S	Series admittance used in 90º bend model	[S]
G_{SYS}	Gain active load-pull measurement system	[-]
G_T	Transducer gain	[-]
GTG	Gate-to-gate spacing	[m]
h	Height substrate	[m]
I_D	Drain current	[A]
I_{DB}	Dispersion correction current	[A]
I_{DIODE}	Diode current	[A]
I_{DS}	Drain-source current	[A]
I_{DSS}	Saturated drain-source current at V_{GS} = 0 V	[A]
I_F	Maximum drain current	[A]
I_G	Gate current	[A]
I_{GS}	Gate-source current	[A]
I_{MAX}	Maximum drain current	[A]
I_{MIN}	Minimum drain current	[A]
I_P	Peak current	[A]
κ	Thermal conductivity	[W.m^{-1}.K]
k	Boltzmann constant	[J.K^{-1}]
K	Rollet stability factor	[-]
K_C	Ratio indicating capacitor process variations	[-]
K_E	Ratio indicating effective dielectric constant variations	[-]
K_L	Ratio indicating inductor process variations	[-]
K_R	Ratio resistors for gate bias setting	[-]
K_Z	Ratio indicating characteristic impedance variations	[-]
λ	Empirical output conductance factor	[S]
L	Length (microstrip line, capacitor, resistor and discontinuities)	[m]
	Inductance	[H]
L_{BE}	Equivalent inductance of a series inductor and capacitor	[H]
L_{BIAS}	Inductor used for supplying a bias voltage	[H]
L_C	Inductor used in slope compensation network	[H]
L_X	Inductor used in matching networks (X= 1,2,3, …)	[H]
L_{IN}	Loss input-matching network	[-]
L_{INT}	Loss interstage-matching network	[-]
L_L	Inductor used to model the load impedance	[H]

L_M	Matching inductor	[H]
L_{OUT}	Loss output-matching network	[-]
L_B	Bias inductor	[H]
L_d	Parasitic drain inductance	[H]
L_g	Parasitic gate inductance	[H]
L_{EP}	Equivalent inductance parallel inductor and capacitor network	[H]
L_{ES}	Equivalent inductance series inductor and capacitor network	[H]
L_G	Gate length	[m]
L_{LRL}	Inductance value found with LRL calibration	[H]
L_s	Parasitic source inductance	[H]
L_S	Series inductance 45º and 90º bend models, capacitor model, resistor model and microstrip line model	[H]
	Inductor used in model source impedance	[H]
L_{SOLT}	Inductance value found with SOLT calibration	[H]
μ_0	Low-field mobility	[$m^2.V^{-1}.s^{-1}$]
n	Fitting factor electron velocity curve	[-]
	Matching ratio between input and output impedance	[-]
	Thermal conductivity reduction factor	[-]
N_1	Impedance matching ratio before process variation	[-]
N_2	Impedance matching ratio after process variation	[-]
N_A	Acceptor doping density	[m^{-3}]
N_{CAP}	Number of fingers interdigitated capacitor	[-]
N_D	Donor doping density	[m^{-3}]
η_D	Drain efficiency	[%]
N_{DS}	Output power reduction due to finite value R_{ds}	[-]
N_{FET}	Number of transistors used in parallel	[-]
N_G	Power gain reduction factor	[-]
N_{GF}	Number of gate fingers	[-]
n_L	Ratio between drain-source impedance and real part load impedance	[-]
N_P	Output power reduction factor due to mismatch	[-]
ϕ_b	Schottky barrier height	[V]
φ_{IN}	Insertion phase input load-pull measurement system	[°]
φ_{OUT}	Insertion phase output load-pull measurement system	[°]
φ_{SYS}	Insertion phase load-pull measurement system	[°]
φ_{VM}	Insertion phase vectormodulator	[°]
PAE	Power Added Efficiency	[%]
PAE_{-1dB}	Power Added Efficiency at one dB compression point	[%]
PAE_{-2dB}	Power Added Efficiency at two dB compression point	[%]
PAE_1	Power Added Efficiency first stage transistor	[%]
PAE_2	Power Added Efficiency second stage transistor	[%]
P_{DC}	Dissipated DC power	[W]
P_{DC1}	Dissipated DC power first stage transistor	[W]
P_{DC2}	Dissipated DC power second stage transistor	[W]
P_i	Port numbers component models (i = 1,2, …)	[-]
P_{IN}	Input power	[W]
P_{LOAD}	Output power active load	[W]
P_{OUT}	Output power	[W]
$P_{OUT-1dB}$	Output power at one dB compression point	[W]
$P_{OUT-2dB}$	Output power at two dB compression point	[W]
P_{OUT_FET1}	Output power first stage transistor	[W]
P_{OUT_FET2}	Output power second stage transistor	[W]

P_{OUT_MAX}	Maximum output power	[W]
P_{OUT_MIN}	Minimum output power	[W]
P_{OUT_NOM}	Output power under nominal conditions	[W]
P_{RF}	RF output power	[W]
PRF	Pulse repetition frequency	[Hz]
P_S	Source power	[W]
P_{SAT}	Saturated output power	[W]
P_{OUT_TARGET}	Targeted output power	[W]
PW	Pulse width	[s]
q	Electron charge	[A.s]
Q_{GC}	Gate-source charge	[A.s]
Q_{GY}	Gate-drain charge	[A.s]
ρ	Material density	[kg.m^{-3}]
R	Reaction Rate	[-]
	Gamma-R parameters	[-]
R_B	Bias resistor	[Ω]
R_{BIAS}	Bias resistor	[Ω]
R_c	Channel resistance at gate and source side	[Ω]
R_C	Resistor used in slope compensation network	[Ω]
$R_{CONTACT}$	Contact resistance	[Ω.m]
R_{ch}	Channel resistance	[Ω]
R_d	Drain resistance	[Ω]
R_{db}	Resistor used for modelling high frequency dispersion FET	[Ω]
R_{ds}	Drain-source resistance	[Ω]
R_g	Gate resistance	[Ω]
R_i	Charging resistance at gate	[Ω]
R_{id}	Charging resistance at drain	[Ω]
R_{is}	Charging resistance at source	[Ω]
R_{IN}	Input resistance	[Ω]
R_L	Resistor used to model load impedance	[Ω]
R_{LOAD}	Real part realised load impedance	[Ω]
R_s	Source resistance	[Ω]
R_S	Series resistor 45º and 90º bend models, capacitor model, resistor model and microstrip line model	[Ω]
	Resistor used in model source impedance	[Ω]
R_{SHEET}	Sheet resistance	[Ω]
R_{STAB}	Stabilisation resistor	[Ω]
R_0	System resistance	[Ω]
R_{ODD}	Odd-mode suppression resistor	[Ω]
R_{OPT}	Optimum load resistance	[Ω]
R_{OUT}	Output resistance	[Ω]
S_{ij}	Scattering parameters (i,j = 1,2,3, …)	[-]
S_{ijM}	Measured scattering parameters (i,j = 1,2,3, …)	[-]
θ	Linear temperature	[K]
	Electrical length transmission line	[°]
θ_C	Electrical length transmission line at the centre frequency	[°]
τ	Time delay current generator in equivalent transistor circuit	[s]
τ_X	Return difference (X=1,2,3,…..)	[-]
T	Time	[s]
	Temperature	[K]

$tan(\delta)$	Loss tangent dielectric material	[-]
T_A	Ambient temperature	[K]
	Accelerated temperature	[K]
	Transmission matrix error coefficients input measurement system	[-]
T_B	Transmission matrix error coefficients output measurement system	[-]
T_M	Measured transmission matrix	[-]
τ_n	Thermal time constant	[s]
T_0	Reference temperature	[K]
	Operating temperature	[K]
υ_{300}	Saturated electron velocity at 300 K	[$m.s^{-1}$]
$\upsilon(E)$	Electron velocity as a function of applied electrical field	[$m.s^{-1}$]
υ_{sat1}	Peak electron velocity at $E = E_C$	[$m.s^{-1}$]
υ_{sat2}	Saturated electron velocity	[$m.s^{-1}$]
υ_{sat}	Saturated electron velocity	[$m.s^{-1}$]
V_{B0}	Zero-bias barrier potential	[V]
V_{BR}	Breakdown voltage	[V]
V_C	Voltage over gate-source capacitor	[V]
V_{DS}	Drain-source voltage	[V]
V_{GDI}	Intrinsic gate-drain voltage	[V]
V_{GS}	Gate-source voltage	[V]
V_{GSI}	Intrinsic gate-source voltage	[V]
V_K	Knee voltage	[V]
V_P	Peak voltage	[V]
V_{MIN}	Minimum drain-source voltage	[V]
V_{MAX}	Maximum drain-source voltage	[V]
V_S	Supply voltage	[V]
V_T	Threshold voltage	[V]
ω	Angular frequency	[Hz]
ω_C	Angular centre frequency	[Hz]
W	Channel thickness	[m]
	Width (microstrip line, capacitor, resistor or discontinuities)	[m]
W_U	Unit gate width	[m]
X	Extension of the space-charge layer in the gate-drain space	[m]
	Percentage of maximum drain-source current	[%]
	Real part load reflection coefficient	[-]
X_{LOAD}	Imaginary part load impedance	[Ω]
X_{OPT}	Real part optimum load reflection coefficient	[-]
Y	Imaginary part load reflection coefficient	[-]
Y_{ij}	Admittance parameters (i,j = 1,2, …)	[S]
Y_{LC}	Admittance parallel inductor and capacitor network	[S]
Y_{OPT}	Imaginary part optimum load reflection coefficient	[-]
Z	Parameter to be fitted during load-pull measurement	[-]
Z_{ij}	Impedance parameters (i,j = 1,2,3, ..)	[Ω]
Z_0	Characteristic impedance	[Ω]
Z_{ds}	Drain-source impedance	[Ω]
$Z_{EXTERNAL}$	Impedance of external bias network of HPA	[Ω]
Z_G	Total gate width transistor	[m]
Z_{IN}	Input impedance	[Ω]
Z_L	Load impedance	[Ω]
Z_{OUT}	Output impedance	[Ω]

Z_P	Parallel impedance used for stabilisation FET	[Ω]
Z_{PD}	Stabilisation impedance in parallel with drain FET	[Ω]
Z_{PG}	Stabilisation impedance in parallel with gate FET	[Ω]
Z_S	Source impedance	[Ω]
Z_{SD}	Stabilisation impedance in series with drain FET	[Ω]
Z_{SG}	Stabilisation impedance in series with gate FET	[Ω]

List of abbreviations

2DEG	Two Dimensional Electron Gas
AC	Alternating Current
ADS	Advanced Design System
AlGaAs	Aluminium Gallium Arsenide
ANG	Angle
ATT	Attenuator
CCI	Centre Composite Inscribed
CDMA	Code Division Multiple Access
CPW	CoPlanar Waveguide
CW	Continuous Wave
DC	Direct Current
DCS	Digital Communication Services
DIOM20HP	Double Ge/Si contact Implantation One Metallisation High-power process Infineon
DRA	Driver Amplifier
DUT	Device Under Test
FET	Field Effect Transistor
FhG-IAF	Fraunhofer Gesellschaft-Institut für Angewandte Festkörperphysik, Freiburg im Breisgau, Germany
GaAs	Gallium Arsenide
GAAS	Gallium Arsenide and related III-V compounds Applications Symposium
GaN	Gallium Nitride
Ge	Germanium
GSM	Global System for Mobile communication
HBT	Heterojunction Bipolar Transistor
HFET	Heterojunction Field Effect Transistor
HEMT	High Electron Mobility Transistor
HP	Hewlett Packard
HPA	High-Power Amplifier
Im	Imaginary
InGaP	Indium Gallium Phosphide
IV	Drain-source current-voltage characteristic
LCR	Impedance model consisting of an inductor, capacitor and resistor
LNA	Low Noise Amplifier
LMDS	Local Multipoint Distribution System
LRL	Line Reflect Line
MAG	Magnitude
MESFET	Metal Semiconductor Field Effect Transistor
MIM	Metal Insulator Metal
MFC	Multi Function Chip
MLIN	Microstrip line model available in Libra

MMIC	Monolithic Microwave Integrated Circuit
MODFET	Modulation Doped Field Effect Transistor
MTTF	Mean Time To Failure
MVDS	Microwave Video Distribution System
NiCr	Nickel Chrome
PCS	Personal Communication System
PHEMT	Pseudomorphic HEMT
RC	Parallel resistor and capacitor network
Re	Real
RF	Radio Frequency
RMS	Root Mean Square
SAG	Self Aligned Gate
SAR	Synthetic Aperture Radar
Si	Silicon
SI	Semi-Insulating
SiC	Silicon Carbide
SiGe	Silicon Germanium
Si_3N_4	Silicon Nitride
SiO_2	Silicon Oxide
SMD	Surface Mounted Device
SOLT	Short Open Load Thru
TFR	Thin Film Resistor
TNO-FEL	Netherlands Organisation for Applied Scientific Research - Physics and Electronics Laboratory
TR	Transmit Receive module
TRL	Thru Reflect Line
TWTA	Travelling Wave Tube Amplifier

Appendix A Parameters of electrical models used for HPA design

A.1 Introduction

In this appendix the electrical models of microstrip discontinuities, inductors realised with the help of a microstrip line, and MIM capacitors are discussed. The model topology used for these components was discussed in chapter 4. Each model has been made scaleable as a function of its dimensions. This is of vital importance for the optimisation of the matching networks, which are discussed in chapter 6. Except for the inductor, no comparison between modelled results and/or simulation results is shown in this appendix. A more detailed comparison between the extracted models and the electromagnetic field simulations is reported elsewhere [A.1, A.2]. A comparison with measurement results is shown in [A.3] and [A.4]. For all models, except the Y-junction, equivalent circuits have been used that are built up out of resistor, inductors and capacitors. The dependency of the values of these lumped elements, on the dimensions of the components, has been fitted with the help of polynomials that have a maximum order of three. A polynomial fit is used because this gives an easy analytical method to calculate the dimensions of the elements when an electrical circuit is converted into a layout, see the discussion in appendix G and chapter 6. The fact that these models can be used in time domain simulators is an additional advantage of the use of lumped elements for the modelling of microwave components.

The content of this appendix is as follows. In appendix A.2 and A.3, the 45º and 90º microstrip bend model parameters are presented. The model parameters of the symmetrical T-junction are presented in appendix A.4. In appendix A.5, the parameters of the symmetrical microstrip crossing are presented. The model parameters of the symmetrical Y-junction are presented in appendix A.6. This appendix is concluded with the inductor model in A.7 and the capacitor model in A.8.

A.2 Model parameters 45° microstrip bend

In this section, the equations and the coefficients of the model parameters of the 45° microstrip bend as a function of the microstrip line width are given. The model topology used for the 45° microstrip bend was shown in section 4.3.3.1. The equation used to fit the model parameters as a function of the microstrip line width is given in equation (A.1). The coefficients used in this equation are listed in table A.1.

$$\{L_S, C_P, R_S\} = \sum_{i=0}^{3} a_i \cdot W^i \ . \tag{A.1}$$

In this equation W is the width of the microstrip line in µm. The model parameters tabulated are valid for line widths varying between 10 and 100 µm. The model parameters a_i are fitted as a function of the width of the microstrip line with the help of a least squares routine.

Table A.1: Model parameters and coefficients of a 45° microstrip bend.

	L_S [pH]	C_P [fF]	R_S [mΩ]
a_0	-48.10^{-1}	42.10^{-2}	420.10^{-2}
a_1	28.10^{-2}	32.10^{-4}	0
a_2	-18.10^{-4}	62.10^{-5}	0
a_3	68.10^{-7}	-18.10^{-7}	0

A.3 Model parameters 90° microstrip bend

In this section the equations and the coefficients of the model parameters of the 90° microstrip bend as a function of the microstrip line width are given. The used model topology is shown in section 4.3.3.2. The equation used to fit the model parameters as a function of the microstrip line width is given in equation (A.2). The coefficients used in this equation are listed in table A.2.

$$\{L_S, C_S, R_S, G_S, C_P\} = \sum_{i=0}^{3} a_i \cdot W^i \ . \tag{A.2}$$

In this equation W is the width of the microstrip line in µm. The model parameters tabulated are valid for line widths varying between 10 and 100 µm. The model parameters a_i are fitted as a function of the width of the microstrip line with the help of a least squares routine.

Table A.2: Model parameters and coefficients of a 90° microstrip bend.

	L_S [pH]	C_S [fF]	R_S [mΩ]	G_S [mS]	C_P [fF]
a_0	-398.10^{-1}	619.10^{-1}	487.10^{-2}	-546.10^{-4}	230.10^{-3}
a_1	120.10^{-2}	587.10^{-2}	427.10^{-3}	532.10^{-3}	208.10^{-4}
a_2	-186.10^{-4}	-315.10^{-4}	-123.10^{-4}	-102.10^{-4}	732.10^{-6}
a_3	109.10^{-6}	183.10^{-5}	973.10^{-7}	160.10^{-6}	212.10^{-8}

A.4 Model parameters symmetrical T-junction

The equation to fit the model parameters of a symmetrical T-junction as a function of the width of the connecting microstrip lines is given in equation (A.3). The coefficients used in this equation are listed in table A.3. The model topology itself is shown in section 4.3.3.3.

$$\{L_1, C_1, G_1, L_2, C_2, G_2, C_3, C_4\} = \sum_{i=0}^{3}\sum_{j=0}^{3} a_{ij} \cdot W_1^j \cdot W_2^i \,. \tag{A.3}$$

In this equation W_1 and W_2 are the widths of the T-junction in µm. The model parameters tabulated are valid for line widths varying between 10 and 100 µm. The model parameters a_{ij} are fitted as a function of the widths of the microstrip lines with the help of a least squares routine.

Table A.3: Model parameters and coefficients symmetrical microstrip T-junction.

	L_1 [H]	C_1 [F]	G_1 [S]	L_2 [H]	C_2 [F]	G_2 [S]	C_3 [F]	C_4 [F]
a_{00}	194.10^{-14}	-102.10^{-15}	368.10^{-04}	-781.10^{-13}	182.10^{-16}	-501.10^{-05}	-270.10^{-18}	217.10^{-17}
a_{10}	128.10^{-14}	-272.10^{-17}	-900.10^{-06}	793.10^{-15}	-132.10^{-17}	159.10^{-06}	931.10^{-19}	-398.10^{-18}
a_{20}	-140.10^{-16}	767.10^{-19}	739.10^{-08}	-855.10^{-17}	119.10^{-19}	-410.10^{-09}	-173.10^{-20}	616.10^{-20}
a_{30}	505.10^{-19}	-447.10^{-21}	-209.10^{-10}	440.10^{-19}	474.10^{-22}	-339.10^{-11}	155.10^{-22}	-316.10^{-22}
a_{01}	-110.10^{-15}	-496.10^{-17}	-156.10^{-05}	102.10^{-14}	376.10^{-17}	787.10^{-06}	-518.10^{-18}	738.10^{-18}
a_{11}	-148.10^{-16}	310.10^{-18}	264.10^{-07}	-119.10^{-16}	151.10^{-18}	-137.10^{-07}	408.10^{-21}	177.10^{-19}
a_{21}	161.10^{-18}	-542.10^{-20}	-212.10^{-10}	708.10^{-19}	-167.10^{-20}	-828.10^{-10}	919.10^{-22}	-362.10^{-21}
a_{31}	-327.10^{-21}	266.10^{-22}	-852.10^{-12}	-370.10^{-21}	491.10^{-24}	152.10^{-11}	-781.10^{-24}	158.10^{-23}
a_{02}	248.10^{-17}	-325.10^{-19}	352.10^{-07}	-655.10^{-17}	-125.10^{-18}	-241.10^{-07}	106.10^{-19}	-174.10^{-19}
a_{12}	508.10^{-19}	933.10^{-21}	-579.10^{-09}	622.10^{-19}	-143.10^{-20}	511.10^{-09}	-103.10^{-21}	323.10^{-22}
a_{22}	122.10^{-24}	241.10^{-25}	354.10^{-15}	519.10^{-23}	705.10^{-25}	-140.10^{-14}	-121.10^{-26}	530.10^{-26}
a_{32}	-625.10^{-23}	-262.10^{-25}	224.10^{-13}	235.10^{-23}	218.10^{-24}	-301.10^{-13}	532.10^{-26}	104.10^{-25}
a_{03}	-138.10^{-19}	546.10^{-22}	-213.10^{-09}	241.10^{-19}	139.10^{-20}	244.10^{-09}	-109.10^{-21}	212.10^{-21}
a_{13}	417.10^{-22}	-852.10^{-23}	218.10^{-11}	-249.10^{-21}	-992.10^{-23}	-549.10^{-11}	161.10^{-23}	-323.10^{-23}
a_{23}	-441.10^{-23}	374.10^{-25}	283.10^{-13}	155.10^{-23}	378.10^{-24}	232.10^{-13}	-167.10^{-25}	545.10^{-25}
a_{33}	500.10^{-25}	-110.10^{-28}	-299.10^{-15}	-288.10^{-25}	-342.10^{-26}	120.10^{-15}	547.10^{-28}	-357.10^{-27}

A.5 Model parameters symmetrical microstrip crossing

The equation used to fit the model parameters of a symmetrical microstrip crossing as a function of the width of the connecting microstrip lines is given in equation (A.4). The coefficients used in this equation are listed for each model parameter in table A.4 and table A.5. The model topology itself is shown in section 4.3.3.4.

$$\{L_1, C_1, L_2, C_2, L_3, C_3, L_4, C_4, C_5, C_6\} = \sum_{i=0}^{3}\sum_{j=0}^{3} a_{ij} \cdot W_1^{\,j} \cdot W_2^{\,i} \,. \tag{A.4}$$

In this equation W_1 and W_2 are the widths of the microstrip crossing in µm. The model parameters tabulated are valid for line widths varying between 10 and 100 µm. The model parameters a_{ij} are fitted as a function of the widths of the microstrip lines with the help of a least squares routine.

Table A.4: Model parameters and coefficients symmetrical microstrip crossing.

	L_1 [H]	C_1 [F]	L_2 [H]	C_2 [F]	L_3 [H]
a_{00}	587.10^{-14}	-302.10^{-15}	-152.10^{-12}	263.10^{-16}	640.10^{-14}
a_{10}	761.10^{-15}	784.10^{-17}	707.10^{-15}	-109.10^{-17}	-285.10^{-15}
a_{20}	-818.10^{-17}	-938.10^{-19}	-620.10^{-18}	221.10^{-19}	498.10^{-17}
a_{30}	351.10^{-19}	375.10^{-21}	-257.10^{-20}	-113.10^{-21}	-269.10^{-19}
a_{01}	-228.10^{-15}	-458.10^{-17}	725.10^{-15}	-140.10^{-18}	734.10^{-15}
a_{11}	-258.10^{-17}	174.10^{-18}	-785.10^{-17}	324.10^{-19}	-137.10^{-17}
a_{21}	821.10^{-19}	-185.10^{-20}	344.10^{-19}	-522.10^{-21}	-778.10^{-19}
a_{31}	-571.10^{-21}	630.10^{-23}	-344.10^{-21}	239.10^{-23}	605.10^{-21}
a_{02}	331.10^{-17}	692.10^{-19}	-438.10^{-18}	-158.10^{-20}	-775.10^{-17}
a_{12}	-418.10^{-19}	-151.10^{-20}	-786.10^{-20}	-776.10^{-22}	821.10^{-19}
a_{22}	456.10^{-24}	201.10^{-25}	266.10^{-23}	784.10^{-26}	123.10^{-23}
a_{32}	280.10^{-23}	728.10^{-25}	560.10^{-23}	880.10^{-26}	-320.10^{-23}
a_{03}	-153.10^{-19}	-708.10^{-21}	-797.10^{-20}	286.10^{-22}	323.10^{-19}
a_{13}	348.10^{-21}	190.10^{-22}	185.10^{-21}	-109.10^{-23}	-607.10^{-21}
a_{23}	-299.10^{-23}	-117.10^{-24}	167.10^{-24}	292.10^{-25}	436.10^{-23}
a_{33}	280.10^{-26}	121.10^{-28}	-333.10^{-25}	-206.10^{-27}	-777.10^{-26}

Table A.5: Model parameters symmetrical microstrip crossing.

	C_3 [F]	L_4 [H]	C_4 [F]	C_5 [F]	C_6 [F]
a_{00}	-253.10^{-15}	-151.10^{-12}	280.10^{-16}	245.10^{-18}	-249.10^{-17}
a_{10}	-814.10^{-17}	792.10^{-15}	-135.10^{-17}	-103.10^{-18}	-232.10^{-19}
a_{20}	435.10^{-19}	-288.10^{-17}	291.10^{-19}	501.10^{-20}	-148.10^{-20}
a_{30}	-141.10^{-21}	106.10^{-19}	-159.10^{-21}	-282.10^{-22}	397.10^{-23}
a_{01}	471.10^{-17}	873.10^{-15}	-421.10^{-18}	-241.10^{-18}	104.10^{-18}
a_{11}	393.10^{-18}	-137.10^{-16}	431.10^{-19}	726.10^{-20}	-278.10^{-20}
a_{21}	-127.10^{-20}	839.10^{-19}	-688.10^{-21}	-134.10^{-21}	677.10^{-22}
a_{31}	-233.10^{-23}	-371.10^{-21}	318.10^{-23}	653.10^{-24}	-177.10^{-24}
a_{02}	-472.10^{-19}	-493.10^{-17}	503.10^{-20}	226.10^{-20}	150.10^{-20}
a_{12}	-521.10^{-20}	101.10^{-18}	-206.10^{-21}	-389.10^{-22}	-258.10^{-22}
a_{22}	173.10^{-25}	505.10^{-24}	126.10^{-25}	272.10^{-28}	-117.10^{-26}
a_{32}	173.10^{-24}	-154.10^{-23}	169.10^{-25}	421.10^{-26}	-243.10^{-26}
a_{03}	178.10^{-21}	201.10^{-19}	-845.10^{-23}	-126.10^{-22}	-125.10^{-22}
a_{13}	213.10^{-22}	-327.10^{-21}	-807.10^{-24}	-797.10^{-25}	461.10^{-24}
a_{23}	780.10^{-25}	-385.10^{-23}	418.10^{-25}	843.10^{-26}	-489.10^{-26}
a_{33}	-134.10^{-26}	345.10^{-25}	-336.10^{-27}	-784.10^{-28}	358.10^{-28}

A.6 Model parameters Y-junction

The parameters of the symmetrical Y-junction model are listed in table A.6. The model equation is shown in (A.5):

$$\{L_1, L_2, C_1, C_2\} = \sum_{i=0}^{3} a_i \cdot W^i \,. \tag{A.5}$$

In this equation, W [µm] is the width of the Y-junction. The model parameters tabulated, are valid for line widths varying between 10 and 100 µm. The model parameters a_i are fitted as a function of the widths of the microstrip lines with the help of a least squares routine.

Table A.6: Model parameters and coefficients symmetrical Y-junction.

	L_1 [µm]	L_2 [µm]	C_1 [fF]	C_2 [fF]
a_0	11.336	-17.204	17.645	-8.552
a_1	0.3758	0.0654	0.3103	0.1352
a_2	-0.000918	0.002871	0.004082	-0.001879
a_3	0.0000025	0.000013	-0.0000171	0.0000078

In the Y-junction model the microstrip line models that are available in Libra are used. An alternative for the Libra microstrip line models is the microstrip line model given in appendix A.7.

A.7 Model parameters of an inductor realised with the help of a microstrip line

As explained in section 4.3.4 microstrip lines can be used to realise inductors. In this appendix, the coefficients of equation (A.6) and equation (A.7) have been listed in table A.7,

$$L_S = \sum_{i=0}^{2}\sum_{j=0}^{2} a_{ij} \cdot W^i \cdot L^j , \tag{A.6}$$

$$C_P = \sum_{i=0}^{1}\sum_{j=0}^{1} a_{ij} \cdot W^i \cdot L^j . \tag{A.7}$$

The resistance R_S is fitted with following equation:

$$R_S = \frac{1}{W} \cdot \sum_{i=0}^{2}\sum_{j=0}^{2} a_{ij} \cdot W^i \cdot L^j . \tag{A.8}$$

In these equations, W [µm] is the width of the microstrip line and L [µm] the length of the microstrip line.

Table A.7: Coefficients series inductance L_S [pH], parallel capacitance C_P [fF] and the series resistance R_S [Ω] (note the line length L and the line width W are in [μm]).

	L_S [pH]	C_P [fF]	R_S [Ω]
a_{00}	-27.10^{-1}	-27.10^{-2}	-76.10^{-3}
a_{10}	20.10^{-3}	-60.10^{-4}	-31.10^{-4}
a_{20}	-94.10^{-6}	-	14.10^{-6}
a_{01}	88.10^{-2}	47.10^{-3}	13.10^{-3}
a_{11}	-90.10^{-4}	73.10^{-5}	42.10^{-5}
a_{21}	47.10^{-6}	-	-22.10^{-7}
a_{02}	-65.10^{-6}	-	-18.10^{-7}
a_{12}	48.10^{-8}	-	-78.10^{-9}
a_{22}	-22.10^{-10}	-	36.10^{-11}

The model components L_S, R_S and C_P have been directly determined from the Y-parameters of the microstrip lines simulated in Libra, see equation (A.9) - (A.11). Their value at 10 GHz has been used:

$$L_S = -\frac{1}{\omega} \cdot \mathrm{Im}\left(\frac{1}{Y_{12}}\right), \tag{A.9}$$

$$R_S = -\mathrm{Re}\left(\frac{1}{Y_{12}}\right), \tag{A.10}$$

$$C_P = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega}. \tag{A.11}$$

For microstrip lines with lengths up to 1000 μm these parameters are frequency independent to at least 12 GHz. Evidence of this can be witnessed from figure A.1. The model components L_S and C_P have been determined for line widths varying between 30 and 100 μm. As an input for this model the microstrip line model available in Libra is used.

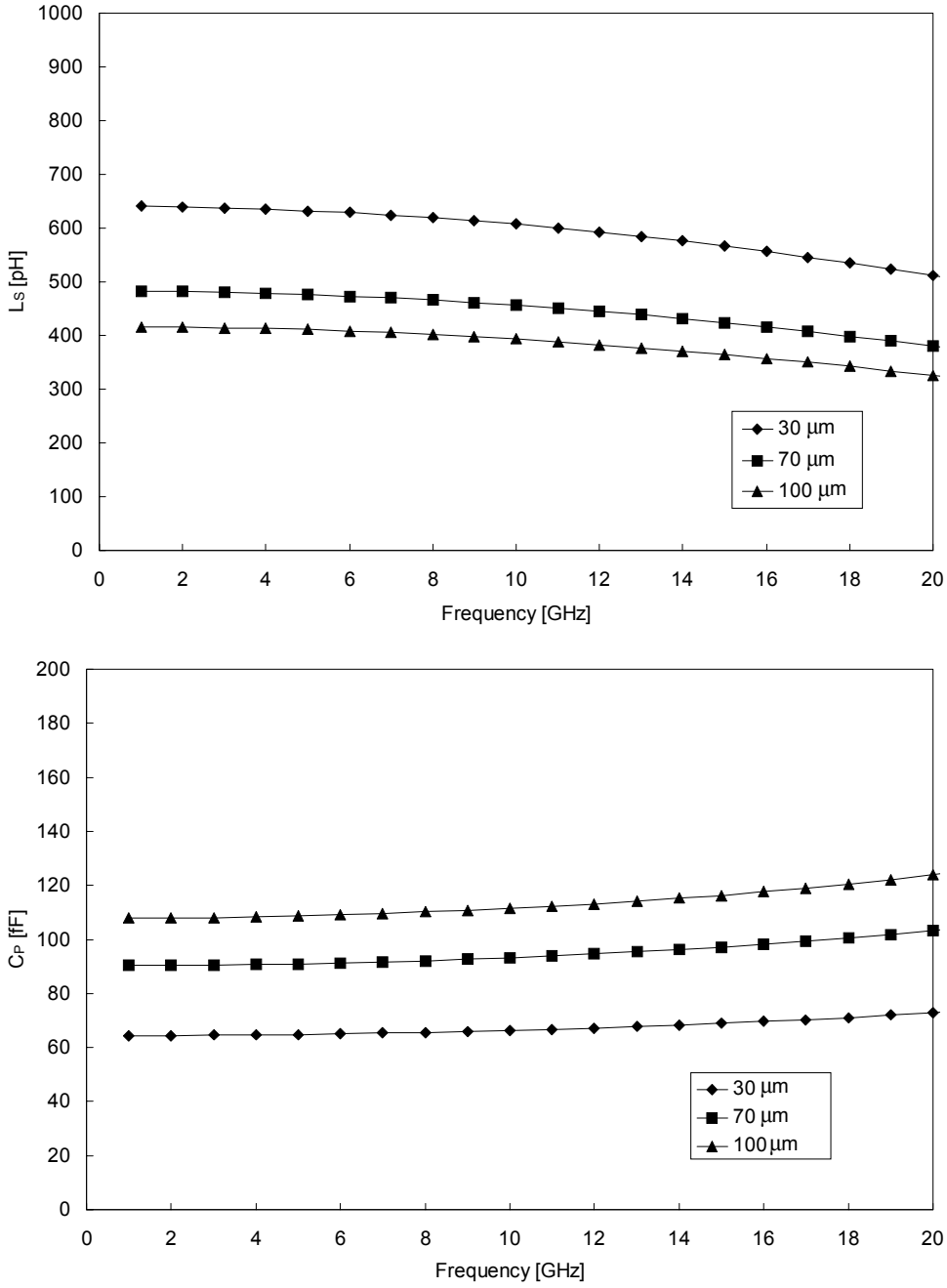

Figure A.1: Calculated L_S and C_P as a function of frequency for microstrip lines with various microstrip line widths W and a line length of L = 1000 µm.

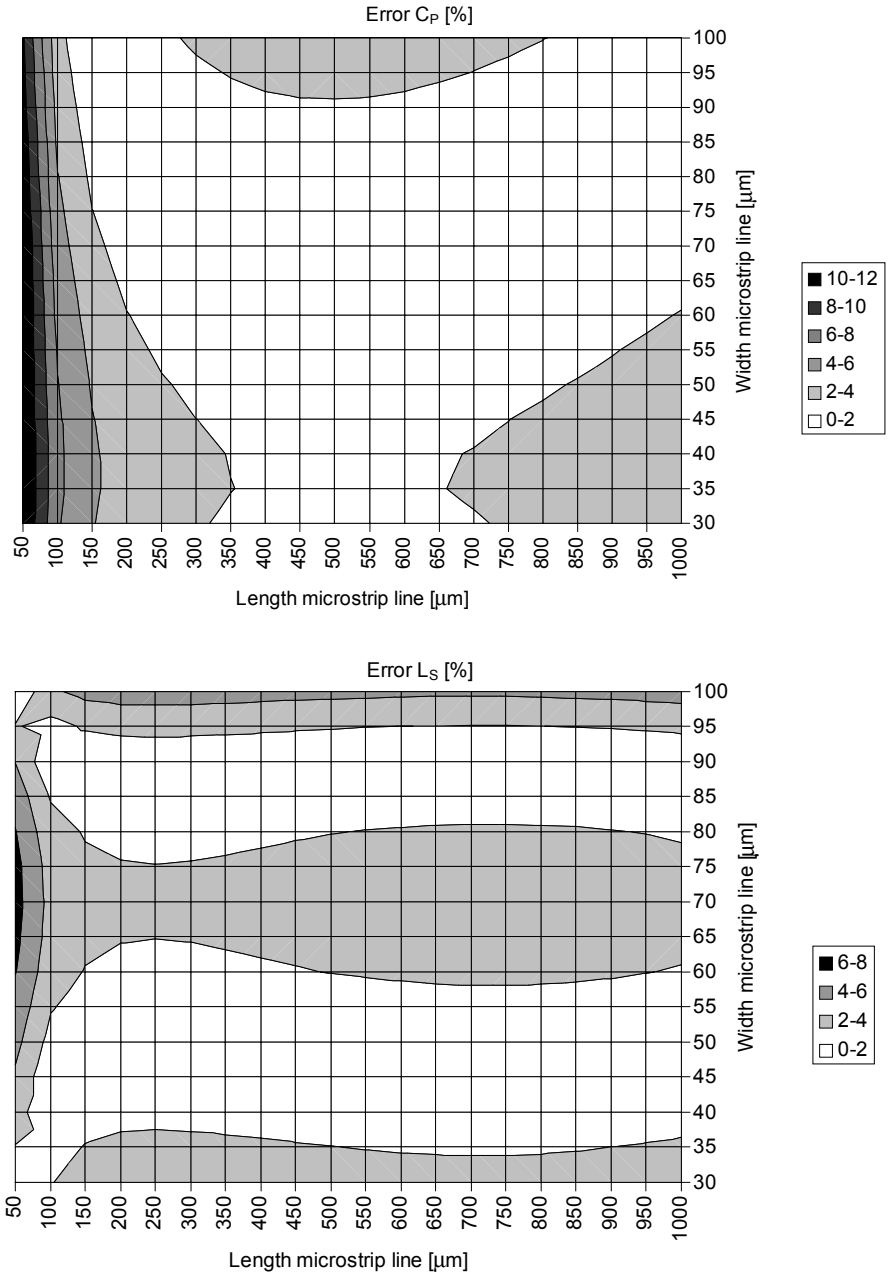

Figure A.2: Error percentage of fitted capacitor (top) and inductor (bottom) values for equivalent pi-network of microstrip line as a function of its length and width.

A comparison of the component values fitted with equation (A.6) and equation (A.7) and the actual value for given length and width is shown in figure A.2. The results show that excellent results have been obtained. For line lengths longer than 50 µm the error for L_S is below 1 %. The same observation is made for C_P, where for line lengths longer than 50 µm the error is below 2%. For line lengths smaller than 50 µm the error increases. It is advised for small line lengths to use the equations for L_S and C_P given for the capacitor in appendix A.8.

A.8 Model parameters of a MIM capacitor model

A MIM capacitor can be represented with the help of the equivalent circuit depicted in section 4.3.5. The effect of the physical size of the capacitor is modelled with the help of a microstrip line. This microstrip line is connected at the bottom plate side of the capacitor. The microstrip line can be replaced with the equivalent circuit shown in figure 4.25. Both models are used in practice. Only the latter model has the advantage that a direct compensation of the layout effects of the capacitor on the desired electrical performance is possible. This is discussed in detail in section 6.4 and appendix G.

The capacitance value depends on the thickness and the relative dielectric constant of the material used to form the capacitor. For most GaAs processes, the following equation can be used for the series capacitance of a MIM capacitor as a function of its length (L) and width (W):

$$C_S = b_1 \cdot W \cdot L + b_2 \cdot 2 \cdot (W + L). \tag{A.12}$$

The value of the series resistance of the bottom plate of the MIM capacitor is given with the help of the following equation:

$$R_S = b_3 \cdot \frac{L}{W}. \tag{A.13}$$

The values of b_1, b_2 and b_3 are process dependent and therefore confidential so that they are not presented here. The series inductance L_S and the parallel capacitor C_P are determined with the help of the microstrip line model available in Libra. Equation (A.14) and equation (A.15) are determined for a length and width of the capacitor that varies between 40 and 120 µm (smaller dimensions will result in a capacitor value < 0.4 pF, which is considered too small for the work described in this thesis),

$$L_S = 7.1400 \cdot \frac{L}{W} + 0.4685 \cdot L - 0.00118 \cdot L \cdot W, \tag{A.14}$$

$$C_P = 0.05025 \cdot L + 0.000627 \cdot L \cdot W. \tag{A.15}$$

The inductance L_S is given in pH, the capacitance C_P in fF and the length and width of the capacitor are in µm. These equations show that it is possible to reduce the influence of the series inductor by making the capacitor as wide as possible.

A.9 References

[A.1] J. Blonnet, "Modelbepaling en implementatie van microstriplijn-discontinuïteiten", TNO report FEL-96-S310, December 1996. (report in Dutch)

[A.2] A.P. de Hek, "Symmetrical Y-junction model", TNO-FEL Engineering analysis report, 6026250.220/ZA01, October 1998.

[A.3] A.P. de Hek, "Experimental verification of microstrip discontinuity models", TNO-report, to be published.

[A.4] A.P. de Hek, "An Accurate Scaleable microstrip T-junction discontinuity model valid up to 50 GHz", *Microwave and RF 1997 Symposium Digest*, October 1997.

Appendix B Power added efficiency calculations

In this appendix, some simple power added efficiency (*PAE*) calculation rules are derived, which enable the calculation of the overall power added efficiency of a complete high-power amplifier. The four calculation rules, given in this appendix, are based on the definition of the power added efficiency *PAE* given in the following equation (B.1):

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \frac{P_{OUT}}{P_{DC}} \cdot \left[1 - \frac{1}{G_P}\right]. \qquad \text{(B.1)}$$

The symbols in this formula have the following meaning:

PAE	: Power Added Efficiency of one amplifier element
P_{OUT}	: Output power device
P_{IN}	: Input power device
P_{DC}	: DC power consumption
G_P	: Power gain amplifier element

Situation 1: Two amplifier blocks in series:

The first situation that is commonly encountered is two amplifier blocks in series, see figure B.1.

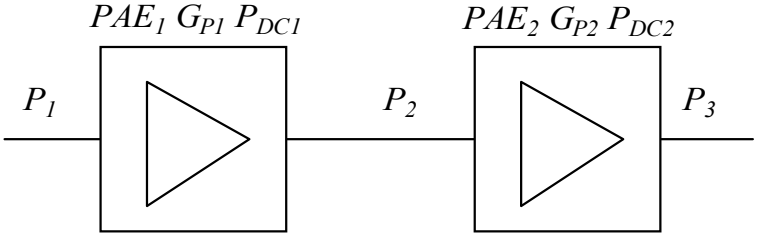

Figure B.1: PAE calculation for two amplifier blocks in series.

The overall power added efficiency PAE_T of the system depicted in figure B.1 can be calculated in the following manner:

$$PAE_1 = \frac{[P_2 - P_1]}{P_{DC1}} = \frac{P_1 \cdot [G_{P1} - 1]}{P_{DC1}} \Rightarrow P_{DC1} = \frac{P_1 \cdot [G_{P1} - 1]}{PAE_1}, \qquad \text{(B.2)}$$

$$PAE_2 = \frac{[P_3 - P_2]}{P_{DC2}} = P_1 \cdot G_{P1} \cdot \frac{[G_{P2} - 1]}{P_{DC2}} \Rightarrow P_{DC2} = P_1 \cdot G_{P1} \cdot \frac{[G_{P2} - 1]}{PAE_2}, \quad \text{(B.3)}$$

$$PAE_T = \frac{[P_3 - P_1]}{[P_{DC1} + P_{DC2}]} = \frac{P_1 \cdot [G_{P1} \cdot G_{P2} - 1]}{[P_{DC1} + P_{DC2}]}. \quad \text{(B.4)}$$

When equation (B.2) and equation (B.3) are substituted in equation (B.4) the following equation is found for the overall PAE_T:

$$PAE_T = \frac{PAE_1 \cdot PAE_2 \cdot [G_{P1} \cdot G_{P2} - 1]}{PAE_1 \cdot G_{P1} \cdot [G_{P2} - 1] + PAE_2 \cdot [G_{P1} - 1]}. \quad \text{(B.5)}$$

The overall gain of this combination is G_{P1}*G_{P2} and the total power dissipation is P_{DC1}+P_{DC2}.

Situation 2: Loss in front of an amplifier stage:

The second situation gives the power added efficiency calculation for a loss in front of an amplifier stage, see figure B.2.

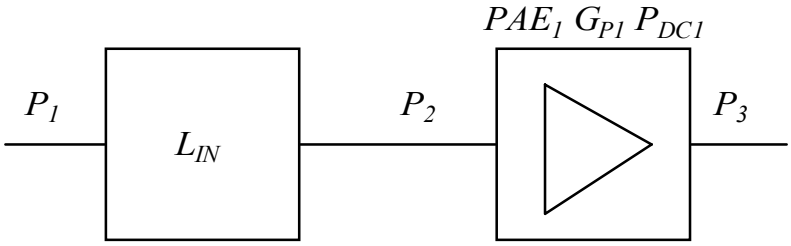

Figure B.2: PAE calculation for an amplifier stage with loss at the input (L_{IN}).

$$PAE_1 = \frac{[P_3 - P_2]}{P_{DC1}} = \frac{P_3}{P_{DC1}} \cdot \left[1 - \frac{1}{G_{P1}}\right] \Rightarrow \frac{P_3}{P_{DC1}} = \frac{PAE_1}{\left[1 - \frac{1}{G_{P1}}\right]}, \quad \text{(B.6)}$$

$$PAE_T = \frac{[P_3 - P_1]}{P_{DC1}} = \frac{P_3}{P_{DC1}} \cdot \left[1 - \frac{1}{L_{IN} \cdot G_{P1}}\right]. \quad \text{(B.7)}$$

When B.6 is substituted in B.7, the overall power added efficiency PAE_T for the combination depicted in figure B.2 can be found:

$$PAE_T = PAE_1 \cdot \frac{[G_{P1} \cdot L_{IN} - 1]}{L_{IN} \cdot [G_{P1} - 1]}. \tag{B.8}$$

The overall gain of this combination is G_{P1}*L_{IN} and the power dissipation is P_{DC1}.

Situation 3: Loss after an amplifier stage:

In figure B.3 the situation is shown for loss after an amplifier stage.

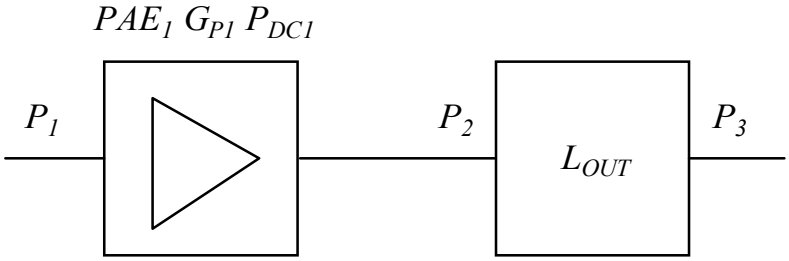

Figure. B.3: PAE calculation of an amplifier stage with loss at the output (L_{OUT}).

The power added efficiency PAE_T of the depicted combination could be calculated with the help of the following equations:

$$PAE_1 = \frac{[P_2 - P_1]}{P_{DC1}} = \frac{P_1}{P_{DC1}} \cdot [G_{P1} - 1] \Rightarrow \frac{P_1}{P_{DC1}} = \frac{PAE_1}{[G_{P1} - 1]}, \tag{B.9}$$

$$PAE_T = \frac{[P_3 - P_1]}{P_{DC1}} = \frac{P_1}{P_{DC1}} \cdot [G_{P1} \cdot L_{OUT} - 1]. \tag{B.10}$$

Substitution of equation (B.9) in equation (B.10) yields an equation for the overall power added efficiency PAE_T of the combination depicted in figure B.3 as a function of the power added efficiency of the amplifier PAE_1,

$$PAE_T = PAE_1 \cdot \frac{[G_{P1} \cdot L_{OUT} - 1]}{[G_{P1} - 1]}. \tag{B.11}$$

The overall gain of this combination is G_{P1}*L_{OUT} and the DC power dissipation is P_{DC1}.

Situation 4: Two amplifier stages in parallel:

In figure B.4 the situation is shown of two identical amplifier stages in parallel.

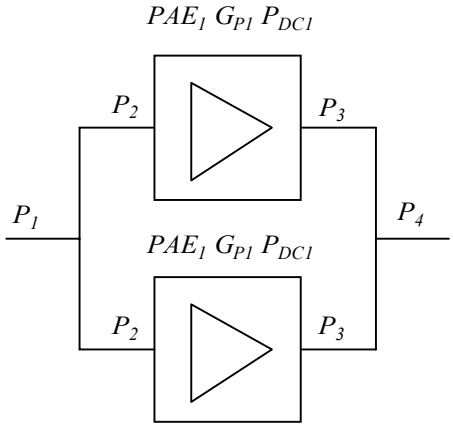

Figure. B.4: Power added efficiency calculation of two identical amplifier stages in parallel.

The total power added efficiency PAE_T of this combination can be calculated with the help of the following equations:

$$PAE_1 = \frac{[P_3 - P_2]}{P_{DC1}}, \tag{B.12}$$

$$PAE_T = \frac{[P_4 - P_1]}{P_{DC1} + P_{DC1}} = \frac{2 \cdot [P_3 - P_2]}{2 \cdot P_{DC1}} = PAE_1 . \tag{B.13}$$

The overall gain of this combination is G_{P1} and the dissipated power is $2*P_{DC1}$.

The symbols in the four described situations have the following meaning:

PAE	: Power Added Efficiency of one amplifier element
PAE_1	: Power Added Efficiency amplifier element 1
PAE_2	: Power Added Efficiency amplifier element 2
PAE_T	: Overall Power Added Efficiency for specific situation
P_{DC}	: DC power dissipation amplifier element
P_{DC1}	: DC power dissipation amplifier element 1
P_{DC2}	: DC power dissipation amplifier element 2
G_P	: Power gain amplifier element
G_{P1}	: Power gain amplifier element 1
G_{P2}	: Power gain amplifier element 2
L_{IN}	: Loss at input DUT
L_{OUT}	: Loss at output DUT

HPA power added efficiency calculation example:

For the high-power amplifier depicted in figure B.5 the overall power added efficiency is calculated with the help of the four standard situations discussed in this appendix. The depicted situation is the one that is encountered for most of the high-power amplifiers discussed in this thesis.

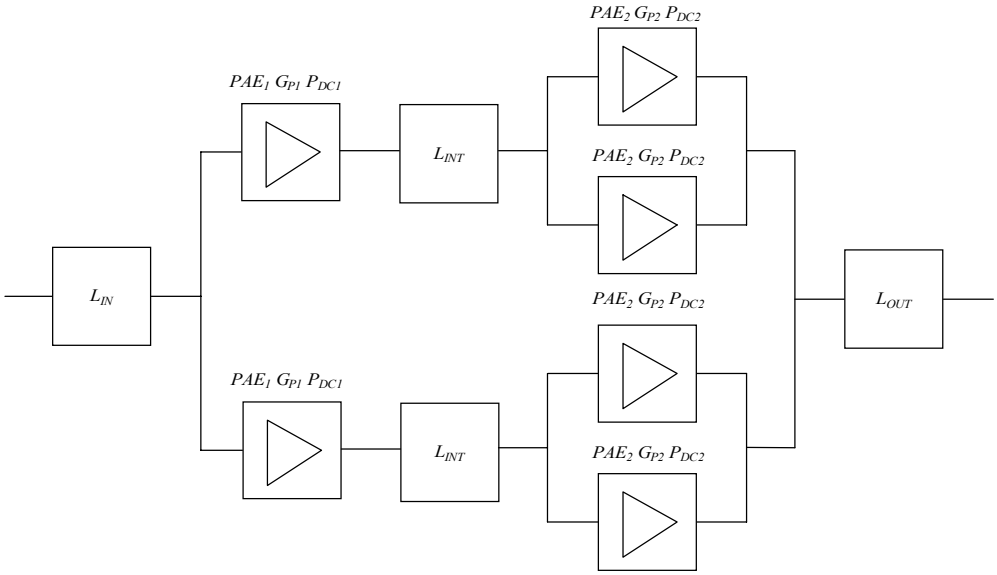

Figure B.5: Block diagram two-stage high-power amplifier.

The determination of the overall *PAE* of this amplifier is started by taking the two amplifier stages at the output in parallel with the help of standard situation 4. The result is given in the following equation:

$$PAE_{N1} = PAE_2 \,. \tag{B.14}$$

As next step, the losses in the interstage L_{INT} are added to this parallel circuit. The resulting PAE_{N2} is determined with the help of standard situation 2:

$$PAE_{N2} = PAE_{N1} \cdot \frac{\left[G_{P2} \cdot L_{INT} - 1\right]}{L_{INT} \cdot \left[G_{P2} - 1\right]} = PAE_2 \cdot \frac{\left[G_{P2} \cdot L_{INT} - 1\right]}{L_{INT} \cdot \left[G_{P2} - 1\right]} \,. \tag{B.15}$$

In the next step the influence of amplifier stage 1 is added with the help of standard situation 1:

$$PAE_{N3} = \frac{PAE_1 \cdot PAE_{N2} \cdot [G_{P1} \cdot L_{INT} \cdot G_{P2} - 1]}{G_{P1} \cdot [G_{P2} \cdot L_{INT} - 1] \cdot PAE_1 + [G_{P1} - 1] \cdot PAE_{N2}}. \tag{B.16}$$

Two of these stages in parallel are available so with the help of standard situation 4 the overall PAE_{N4} can be determined:

$$PAE_{N4} = PAE_{N3}. \tag{B.17}$$

As next step the losses at the output L_{OUT} are taken into account with the help of situation 3:

$$PAE_{N5} = PAE_{N4} \cdot \frac{[G_{P1} \cdot L_{INT} \cdot G_{P2} \cdot L_{OUT} - 1]}{[G_{P1} \cdot L_{INT} \cdot G_{P2} - 1]} = PAE_{N3} \cdot \frac{[G_{P1} \cdot L_{INT} \cdot G_{P2} \cdot L_{OUT} - 1]}{[G_{P1} \cdot L_{INT} \cdot G_{P2} - 1]}. \tag{B.18}$$

As last step the losses at the input L_{IN} are taken into account with the help of standard situation 2:

$$PAE_T = PAE_{N5} \cdot \frac{[L_{IN} \cdot G_{P1} \cdot L_{INT} \cdot G_{P2} \cdot L_{OUT} - 1]}{L_{IN} \cdot [G_{P1} \cdot L_{INT} \cdot G_{P2} \cdot L_{OUT} - 1]}, \tag{B.19}$$

which is equivalent to,

$$PAE_T = PAE_{N3} \cdot \frac{[L_{IN} \cdot G_{P1} \cdot L_{INT} \cdot G_{P2} \cdot L_{OUT} - 1]}{L_{IN} \cdot [G_{P1} \cdot L_{INT} \cdot G_{P2} - 1]}. \tag{B.20}$$

Equation (B.20) is further simplified by substituting equation (B.15) and equation (B.16). The resulting equation is the one that is used in chapter 5 for the calculation of the overall power added efficiency of a two-stage high-power amplifier:

$$PAE_T = \frac{PAE_1 \cdot PAE_2 \cdot (L_{IN} \cdot L_{INT} \cdot L_{OUT} \cdot G_{P1} \cdot G_{P2} - 1)}{PAE_1 \cdot G_{P1} \cdot L_{IN} \cdot L_{INT} \cdot (G_{P2} - 1) + PAE_2 \cdot L_{IN} \cdot (G_{P1} - 1)}. \tag{B.21}$$

Appendix C Temperature coefficients MESFET

C.1 Introduction

In this appendix, the temperature dependency of the power gain and output power of a MESFET is calculated. The calculation will be based on the assumption that the saturation velocity of the electrons is the dominant factor that determines the temperature dependency. The thermal resistance of the transistor is considered constant as a function of temperature. These assumptions in combination with the simplified MESFET transistor model of Ladbrooke [C.1], lead to simple equations for the temperature dependency of the power gain and the output power.

C.2 Determination temperature coefficients

Based on the simple model of Ladbrooke [C.1] the following equation for the cut-off frequency f_T is found, see also chapter 2:

$$f_T = \frac{\upsilon_{SAT}}{2 \cdot \pi \cdot (L_G + X/2)}. \tag{C.1}$$

The power gain of a transistor G_P is related to the cut-off frequency with the help of the following equation, see also chapter 2:

$$G_P = \left(\frac{f_T}{f} \right)^2 \cdot K. \tag{C.2}$$

The constant K in this equation contains the influence of the load impedance and parasitic transistor elements on the power gain G_P. They are considered to be temperature independent for this discussion and therefore have been summarised into one constant. It is assumed that major temperature dependency of the transistors is caused by the temperature dependency of the saturated electron velocity. In that case, the power gains of a transistor at two different temperatures can be related as follows:

$$\frac{G_P(T_1)}{G_P(T_2)} = \left(\frac{\upsilon_{SAT}(T_1)}{\upsilon_{SAT}(T_2)} \right)^2. \tag{C.3}$$

The temperature dependency of the saturated electron velocity of GaAs is described [C.2] with the help of the following equation:

$$\upsilon_{SAT}(T) = \upsilon_{300} \cdot \left(\frac{2090}{T + 1790} \right)^{3.568} \qquad 100K \le T \le 500K \,. \tag{C.4}$$

In this equation υ_{300} is the saturation electron velocity at 300 K. Substitution of equation (C.4) in equation (C.3) results in:

$$\frac{G_P(T_1)}{G_P(T_2)} = \left(\frac{1 + \frac{T_2}{1790}}{1 + \frac{T_1}{1790}} \right)^{7.136} \,. \tag{C.5}$$

Writing this equation in dB gives:

$$10 \cdot \log\left(\frac{G_P(T_1)}{G_P(T_2)} \right) = \frac{71.36}{\ln(10)} \cdot \ln\left(\frac{1 + \frac{T_2}{1790}}{1 + \frac{T_1}{1790}} \right). \tag{C.6}$$

The following series development of the natural logarithm is used:

$$\ln(1 + x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \frac{x^4}{4} \cdots for - 1 \le x \le 1 \,. \tag{C.7}$$

In this case, x is small, so only, the first two terms need to be used. Then the following equation is found:

$$10 \cdot \log\left(\frac{G_P(T_1)}{G_P(T_2)} \right) = 0.0173 \cdot \left(T_2 - T_1 + \frac{{T_1}^2 - {T_2}^2}{3580} \right). \tag{C.8}$$

Equation (C.6) has been simplified to equation (C.8) to be able to draw some conclusions about the temperature dependency of the power gain. Equation (C.8) shows that:

- The power gain decreases with increasing temperature.
- As first approximation, the power gain degradation varies linear with temperature. The power gain variation is -0.0173 dB/°C. This value is close to the -0.013 dB/°C found from measurements, see section 5.3.4.

For the output power, a similar expression can be found. As a starting point the following equations, which have been discussed in section 2.3.2, have been used:

$$P_{OUT} = \frac{(V_{MAX} - V_{MIN}) \cdot I_F}{8}, \tag{C.9}$$

$$I_F = q \cdot N_D \cdot Z_G \cdot \upsilon_{SAT} \cdot (W - d). \tag{C.10}$$

If it is assumed that the voltage swing is unaffected by the temperature variations and the temperature variation of I_F is only due to the temperature dependency of the saturated electron velocity the following equation is found:

$$10 \cdot \log\left(\frac{P_{OUT}(T_1)}{P_{OUT}(T_2)}\right) = \frac{35.68}{\ln(10)} \cdot \ln\left(\frac{1 + \frac{T_2}{1790}}{1 + \frac{T_1}{1790}}\right). \tag{C.11}$$

This equation can be simplified to:

$$10 \cdot \log\left(\frac{P_{OUT}(T_1)}{P_{OUT}(T_2)}\right) = 0.00866 \cdot \left(T_2 - T_1 + \frac{T_1^2 - T_2^2}{3580}\right). \tag{C.12}$$

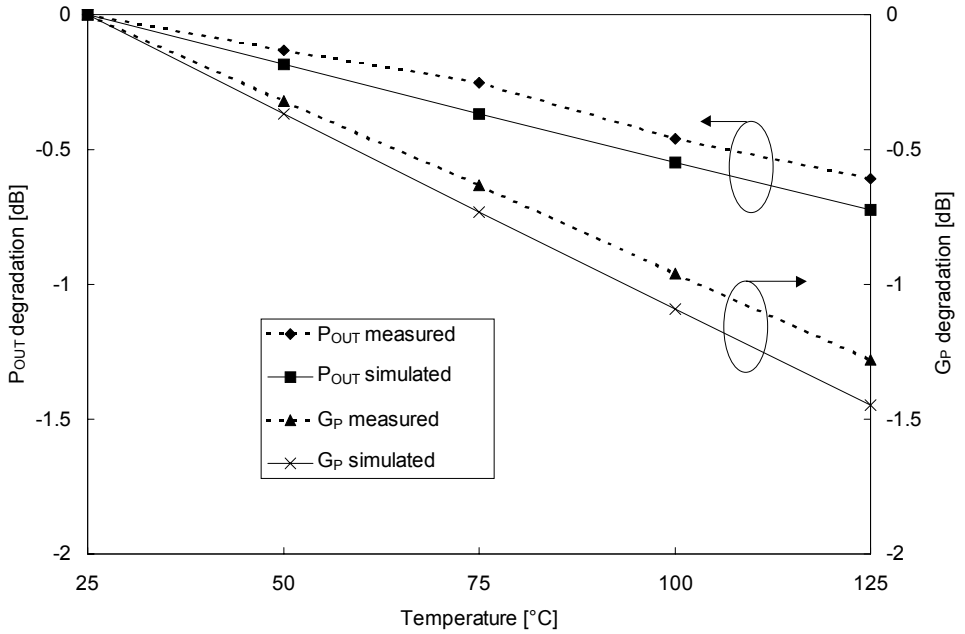

Figure C.1: Output power and power gain degradation as a function of temperature. The degradation is calculated relatively to a temperature of 25 °C.

This equation is very similar to the one that is found for the power gain variation. The only difference is the fact that output power variation is only half that of the power gain variation. This is similar to the difference found from measurements as were discussed in section 5.3.4.

In figure C.1, a comparison between the measurement results from section 5.3.4 and the results calculated with the help of equation (C.6) and equation (C.11) is shown. From the depicted results, a reasonable good agreement can be seen between measurements and simulations. The trends are predicted well and the calculated values are close to the measured ones. These results demonstrate that for MESFETs the temperature dependency of both the power gain and output power is directly related to the temperature dependency of the saturated electron velocity in GaAs. The calculated power gain variation is also in good agreement with the results that are given by Lardizabel [C.3]. In [C.3] several references are compared and an average power gain variation as a function of temperature of –0.015 dB/°C is found

C.3 References

[C.1] P.H. Ladbrooke, "MMIC Design: GaAs FETs and HEMTs", Artech House, 1989.

[C.2] Z. Nosal, "Temperature dependent functional small-signal and noise model of GaAs FET", *IEEE MTT-S Symposium Digest*, pp. 1339-1342, May 1995.

[C.3] S.M. Lardizabal, A.S. Fernandez and L.P. Dunleavy, "Temperature-Dependent Modeling of Gallium Arsenide MESFET's", *IEEE Trans. Microwave Theory and Tech.,* vol. MTT-44, pp. 357-363, March 1996.

Appendix D Large-signal S-parameter determination

In this appendix, the method used to determine the S-parameters of a transistor under large signal conditions is discussed. For this method, a multi-tone simulation is used. The input of the transistor is loaded with in general a complex source impedance Z_S. At the output of the transistor, a complex load impedance Z_L is present. Between the transistor and the load impedance a four port is connected, see figure D.1.

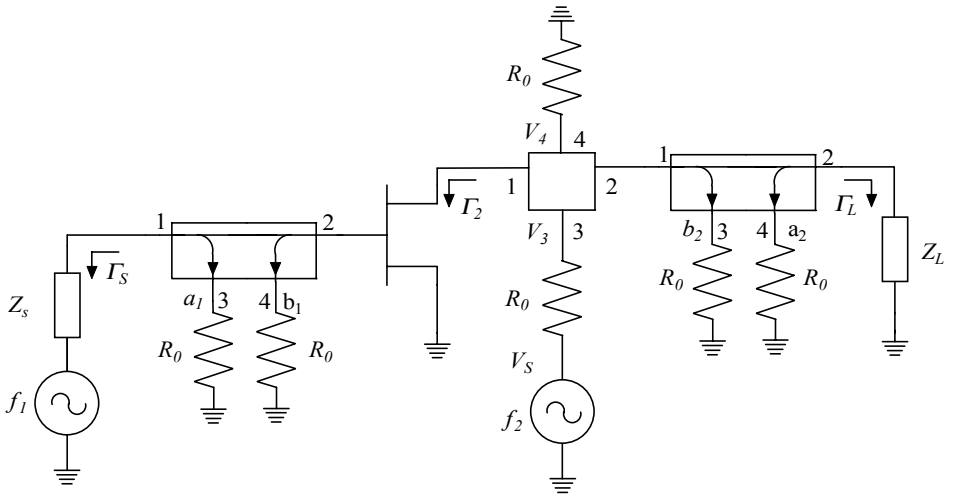

Figure D.1: Large-signal S-parameter simulation test bench.

The S-parameters of this four port have the following value at all frequencies:

$$S_{21} = 1\,, \tag{D.1}$$

$$S_{11} = S_{22} = S_{33} = S_{44} = S_{31} = S_{24} = S_{14} = S_{41} = S_{43} = S_{34} = S_{23} = S_{32} = 0\,. \tag{D.2}$$

The following S-parameters have frequency dependent properties:

$$S_{12} = 1 \text{ and,} \tag{D.3}$$

$$S_{13} = S_{42} = 0 \text{ at frequency } f_1, \tag{D.4}$$

$$S_{12} = 0 \text{ and,} \tag{D.5}$$

$$S_{13} = S_{42} = 1 \quad \text{at frequency } f_2. \tag{D.6}$$

This four-port is placed at the output of the active device and is used to inject a small signal into the transistor. To make this possible in Libra this second signal has to be injected at a different frequency. The chosen offset between both frequencies is 10 MHz. The first frequency f_1 is applied at the input of the transistor and its output power can be varied from small to large signal. The second frequency f_2 is only used for measurement purposes. The incident and reflected power waves of the transistor, see figure D.2, at both frequencies are measured with the help of the ideal dual power samplers available in Libra, see figure D.1.

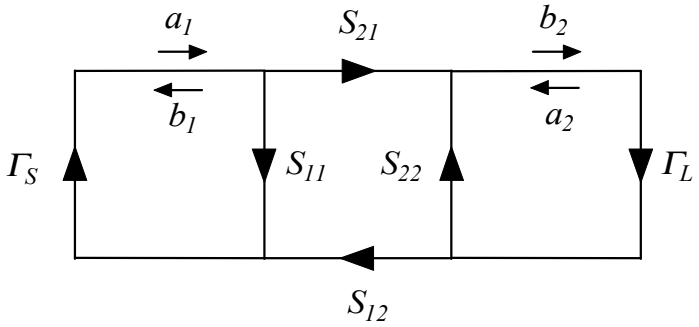

Figure D.2: Incident and reflected power waves.

The S-parameters of the dual power samplers are as follows:

$$S_{21} = S_{12} = S_{31} = S_{42} = 1, \tag{D.7}$$

$$S_{11} = S_{22} = S_{33} = S_{44} = S_{13} = S_{24} = S_{14} = S_{41} = S_{43} = S_{34} = S_{32} = S_{23} = 0. \tag{D.8}$$

The direction of the power waves for both frequencies is depicted in figure D.2. The four-port at the output of the transistor also offers the possibility to measure the product of $\Gamma_2 \cdot \Gamma_L$, this is done by measuring at the second frequency the voltage at port 3 and port 4. The product of the reflection coefficients can then be determined as follows:

$$\Gamma_{OSC} = \Gamma_2 \cdot \Gamma_L = \frac{V_4}{V_3}. \tag{D.9}$$

The value of Γ_L is measured at the large signal frequency f_1 with the help of the output sampler. With the help of this value and Γ_{OSC}, it is possible to calculate the value of Γ_2. This Γ_2 is equal to the uncorrected S_{22M}. The uncorrected S_{11M} and S_{21M} are measured at the large signal frequency with the help of the power samplers at the input and the output of the transistor. Next, the uncorrected S_{12M} is needed for the calculation of the corrected S-parameters of the transistor under large signal conditions. This parameter is calculated from

the voltage measured at the second frequency source and the voltage measured at port 4 of the input power sampler:

$$S_{12M} = \frac{2 \cdot V_S}{V_{b1}}. \tag{D.10}$$

The reflection coefficient of the source impedance is also measured at the second frequency. For this purpose, the dual power sampler at the input of the transistor is used in the reverse way. The reflection coefficient is calculated in the following way from the measured power waves,

$$\Gamma_S = \frac{a_1}{b_1}. \tag{D.11}$$

With this last equation, sufficient information is available to calculate the large signal S-parameters of the transistor. The calculated S-parameters are given in equations (D.12 – D.15):

$$S_{11} = \frac{S_{11M} - S_{21M} \cdot S_{12M} \cdot \Gamma_L}{1 - S_{21M} \cdot S_{12M} \cdot \Gamma_S \cdot \Gamma_L}, \tag{D.12}$$

$$S_{22} = \frac{S_{22M} - S_{21M} \cdot S_{12M} \cdot \Gamma_S}{1 - S_{21M} \cdot S_{12M} \cdot \Gamma_S \cdot \Gamma_L}, \tag{D.13}$$

$$S_{21} = S_{21M} \cdot \left(1 - S_{22} \cdot \Gamma_L\right), \tag{D.14}$$

$$S_{12} = S_{12M} \cdot \left(1 - S_{11} \cdot \Gamma_S\right). \tag{D.15}$$

The test bench depicted in figure D.1 can also be applied inside a complete high-power amplifier. The S-parameters determined with the help of the discussed method can be used for the analysis of the stability of the high-power amplifier as was discussed in section 6.7. The S-parameters found in this way give a good impression of the in band stability. On the other hand, they do not give, in a direct way, an indication how a large-signal in band, e.g. 10 GHz, will change the S-parameters out band, e.g. 1 GHz. The following methods were considered for the determination of the S-parameters as a function of frequency, due to one large-signal input signal:

1. A third signal generator can be added at the input of the test bench. This signal generator must be placed in series with the signal generator at frequency f_1. The third signal generator will be used at a very small output power and will be set at a frequency offset from f_1. The S-parameters can then be determined with the help of measurements at f_2 and f_3 in the same way as discussed before. A major disadvantage of this method is

the difficult and often impossible convergence of the simulations. This problem is circumvented with the method discussed at the next point.

2. If we assume that the extrinsic transistor parameters do not change under large-signal conditions then it is possible to calculate the intrinsic transistor model parameters from S-parameters determined at a single frequency, see section 4.2.1. With the help of the found transistor model parameters, the S-parameters at all other desired frequency points can be calculated. These S-parameters can then be used for the stability analysis.

Appendix E N-port to two-port network conversion

For the synthesis of a matching network, it is convenient to work with a two-port network. After the network topology is synthesised, this two-port network must be transformed to an n-port network, see figures E.1 and E.2. In this appendix, the transformation of a two-port network to an n-port network and vice versa will be discussed. After this discussion, some examples will be shown.

A two-port network can be described with the help of the ABCD parameters:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ I_2 \end{bmatrix}. \tag{E.1}$$

When n identical two-port networks are placed in parallel the following matrix representation is found:

$$\begin{bmatrix} U_1 \\ n \cdot I_1 \end{bmatrix} = \begin{bmatrix} A_N & B_N \\ C_N & D_N \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ n \cdot I_2 \end{bmatrix}. \tag{E.2}$$

After simple manipulations the following ABCD parameters for the n-port are found as a function of the ABCD parameters of the two-port:

$$A_N = A\,. \tag{E.3}$$

$$B_N = \frac{B}{n}\,. \tag{E.4}$$

$$C_N = n \cdot C\,. \tag{E.5}$$

$$D_N = D\,. \tag{E.6}$$

Some examples of the ABCD parameters of the elements used in the matching network design are the following. A series impedance Z_S has the following ABCD matrix:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & Z_S \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ I_2 \end{bmatrix}. \tag{E.7}$$

This means that when the original two-port is converted to an n-port the value of the series impedance Z_S has to be multiplied by n. For a parallel admittance Y_P, the following ABCD matrix is found:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y_P & 1 \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ I_2 \end{bmatrix}. \tag{E.8}$$

So the parallel admittance of an n-port is found by dividing Y_P by n. The series transmission line, which ABCD parameters are given by:

$$\begin{bmatrix} U_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_0 \cdot \sinh(\gamma l) \\ Y_0 \cdot \sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \cdot \begin{bmatrix} U_2 \\ I_2 \end{bmatrix}. \tag{E.9}$$

Therefore, it can be concluded that the only change for the n-port case is the characteristic line impedance, which has to be multiplied with n.

As a final example, the two-port equivalent of an output-matching network, which combines the output power of eight transistors in parallel, is discussed. The resulting equivalent circuit is depicted in figure E.1. Here the existing symmetry in the matching network is used. Therefore, only half the network has to be calculated. The original equivalent circuit is depicted in figure E.2. To account for the existing symmetry the input impedance has to be divided by four and the output impedance has to be multiplied with two.

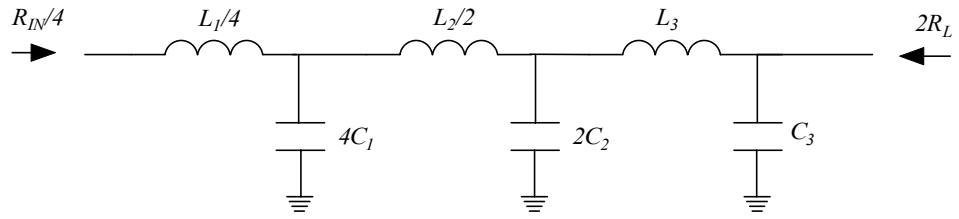

Figure E.1: Equivalent two-port circuit of an output-matching network that combines eight transistors in parallel (see figure E.2).

As already discussed the series elements are divided by the number of branches that are placed in parallel and the parallel admittances are multiplied by the number of branches used in parallel.

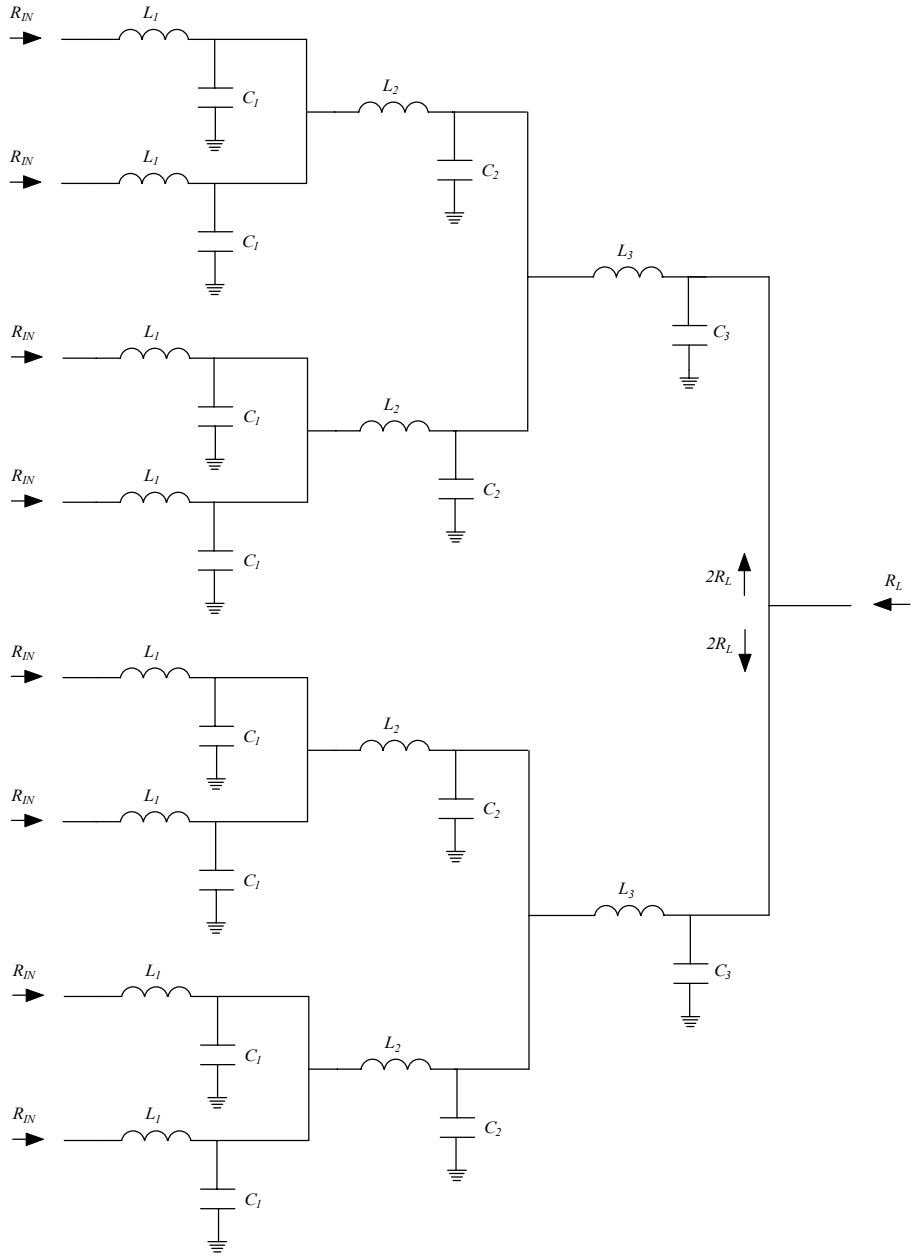

Figure E.2: Topology output-matching network of an amplifier using eight transistors in parallel.

Appendix F Modelling of the load and source impedance

F.1 Introduction

The determination of the equivalent circuit used for the load and source impedance, of the matching networks used in this thesis, is discussed in this appendix.

F.2 Modelling of source impedance

The source impedance of the output and interstage-matching networks has the topology depicted in figure F.1.

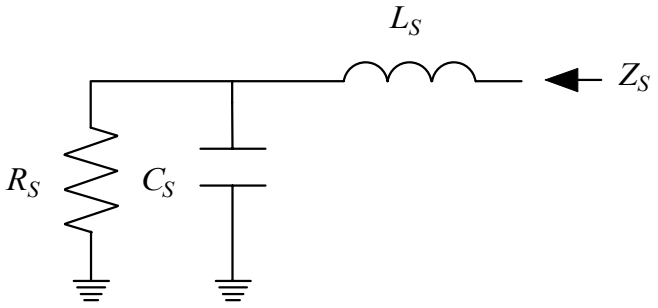

Figure F.1: Equivalent circuit of source impedance output and interstage-matching networks.

The depicted equivalent circuit, which closely resembles the output of the equivalent circuit of a FET, which was discussed in section 4.2, is based on load-pull measurement data. The equivalent circuit, which gives the best fit to the conjugate of this load-pull data was determined automatically with the help of the method described by Mellor [F.1], is depicted in figure F.1. This circuit is different from the one that is commonly used where the influence of the series inductor is neglected. Neglecting the series inductor is not allowed as can be seen from the results depicted in figure F.2. In this figure the measured source impedance is compared with the simulated results of the equivalent circuit depicted in figure F.1 (LRC) and the one where the inductor is neglected (RC) and the component values are calculated at 10 GHz.

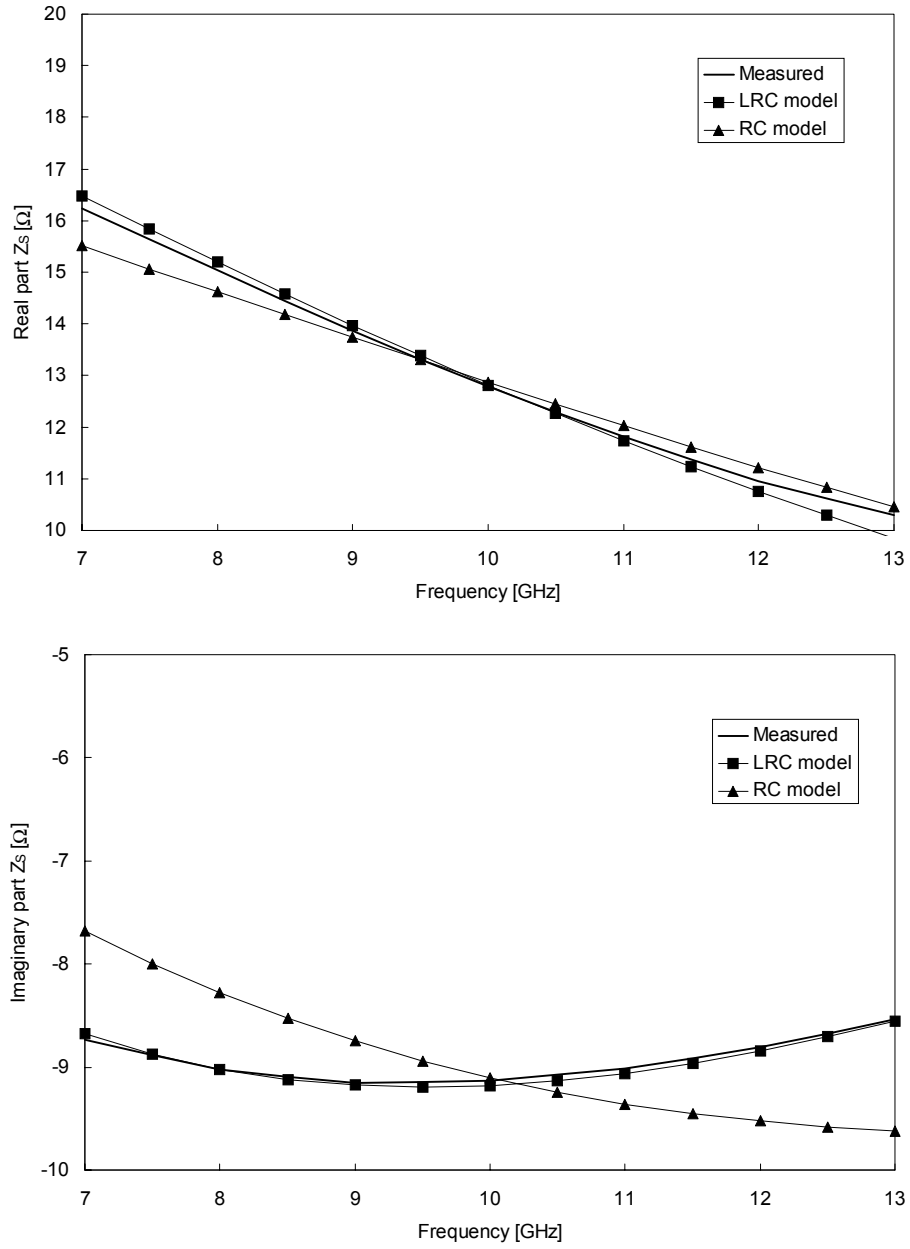

Figure F.2: Comparison between measured and simulated real and imaginary parts of the source impedance of the output and interstage-matching networks when a fishbone MESFET that has 32 gate fingers with a unit gate width of 75 μm is used. The measurement data is obtained at V_{DS} = 9 V and V_{GS} = -1.25 V.

The results show that especially the imaginary part does not fit well as a function of frequency when the influence of the series inductor is neglected. The results of the extraction of the source impedance for the various MESFETs, used in the high-power amplifiers described in this thesis, are listed in table F.1. The results listed in this table are determined for various sizes of transistors, layouts and are obtained from different wafers. The results show that the optimum load impedance scales reasonably well considering that the samples are taken from different wafers. An average value of 55.1 Ω.mm was found. In addition, the scaling of the parallel capacitor is reasonable. For the capacitor, an average value of 0.299 pF/mm was found.

The scaling of the series inductor is less clear; it is a function of the number of gate fingers, the unit gate width and a constant that accounts for the feed network. This trend is obviously visible in the results listed in table F.1. The first two transistors show an inductance, which is more or less equal. This is logical from the point of view that the unit gate width is similar and that the feed network is almost similar. The inductance of the third and fourth listed transistor also scales well. In that case, only the unit gate width is changed and as can be seen the inductance increases linear with increasing gate width. The last transistor has, as expected, a higher value due to the larger amount of gate fingers that has been used. The results also show that the transistors that have a fishbone layout have a higher inductance than the transistors that have a interdigitated layout.

Table F.1: Equivalent circuit elements source impedance of the used MESFETs. All measurements are performed at V_{DS} = 9 V and V_{GS} = -1.25 V.

N_{GF}	W_U [µm]	Wafer	Type	R_S [Ω.mm]	C_S [pF/mm]	L_S [pH]
12	125	YC201.5	Interdigitated	51.7	0.349	10.8
14	125	YC201.5	Interdigitated	51.9	0.310	10.9
32	40	YC501.2	Fishbone	59.1	0.287	16.5
32	75	YC501.2	Fishbone	54.5	0.257	33.2
48	63	YI505.6	Fishbone	58.2	0.294	45.6

Table F.2: Equivalent circuit elements source impedance of the used HFETs. All measurements were performed at V_{DS} = 8 V and V_{GS} = -0.3 V.

N_{GF}	W_U [µm]	Wafer	Type	R_S [Ω.mm]	C_S [pF/mm]	L_S [pH]
32	45	ASYL5C	Fishbone	41.0	0.495	81.6
48	45	ASYL5C	Fishbone	41.0	0.440	39.6

The results for some HFETs are listed in table F.2. The listed results show that both the load resistance and capacitance scale well, as was the case for the MESFETs. The series inductance is not constant, as it was the case for the MESFETs. The value of the load resistance is 41.0 Ω.mm for the HFETs, which is considerably lower than the 55.1 Ω.mm of the MESFETs. The lower resistance of the HFETs is caused by the higher maximum current of these devices. Therefore, it can also be expected that at the same drain-source voltage the output power of these devices will be higher.

F.3 Modelling of load impedance

The load impedance of the interstage and input-matching networks is determined in a manner similar to the one described for the source impedance. The resulting equivalent circuit is depicted in figure F.3. The input data for this model determination is found from simulation of the transistor with the realised output-matching network. The topology of the load impedance is straight forward if one looks at the equivalent model of the transistor as has been described in section 4.2. The values that have been found for various transistor sizes in both the MESFET and the HFET process are listed in tables F.3 and F.4.

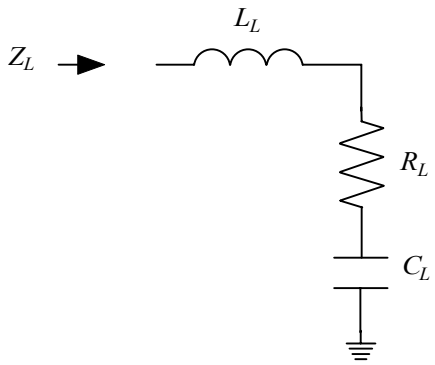

Figure F.3: Equivalent circuit of load impedance interstage and input-matching networks.

A comparison of the fit of the found load impedance with the simulation data that is used for the model extraction is shown in figure F.4 for two different transistors.

Table F.3: Equivalent circuit elements load impedance for the interstage and input-matching networks of the used MESFETs. All measurements are performed at V_{DS} = 9 V and V_{GS} = -1.25 V.

N_{GF}	W_U [µm]	Wafer	Type	R_L [Ω.mm]	C_L [pF/mm]	L_L [pH]
12	125	YC201.5	Interdigitated	5.1	1.100	23.4
14	125	YC201.5	Interdigitated	5.3	1.090	23.8
48	63	YI505.6	Fishbone	4.3	1.540	63.6

Table F.4: Equivalent circuit elements load impedance for the interstage and input-matching networks of the used HFETs. All measurements were performed at V_{DS} = 8 V and V_{GS} = -0.3 V.

N_{GF}	W_U [µm]	Wafer	Type	R_L [Ω.mm]	C_L [pF/mm]	L_L [pH]
48	45	ASYL5C	Fishbone	2.1	2.134	80.7

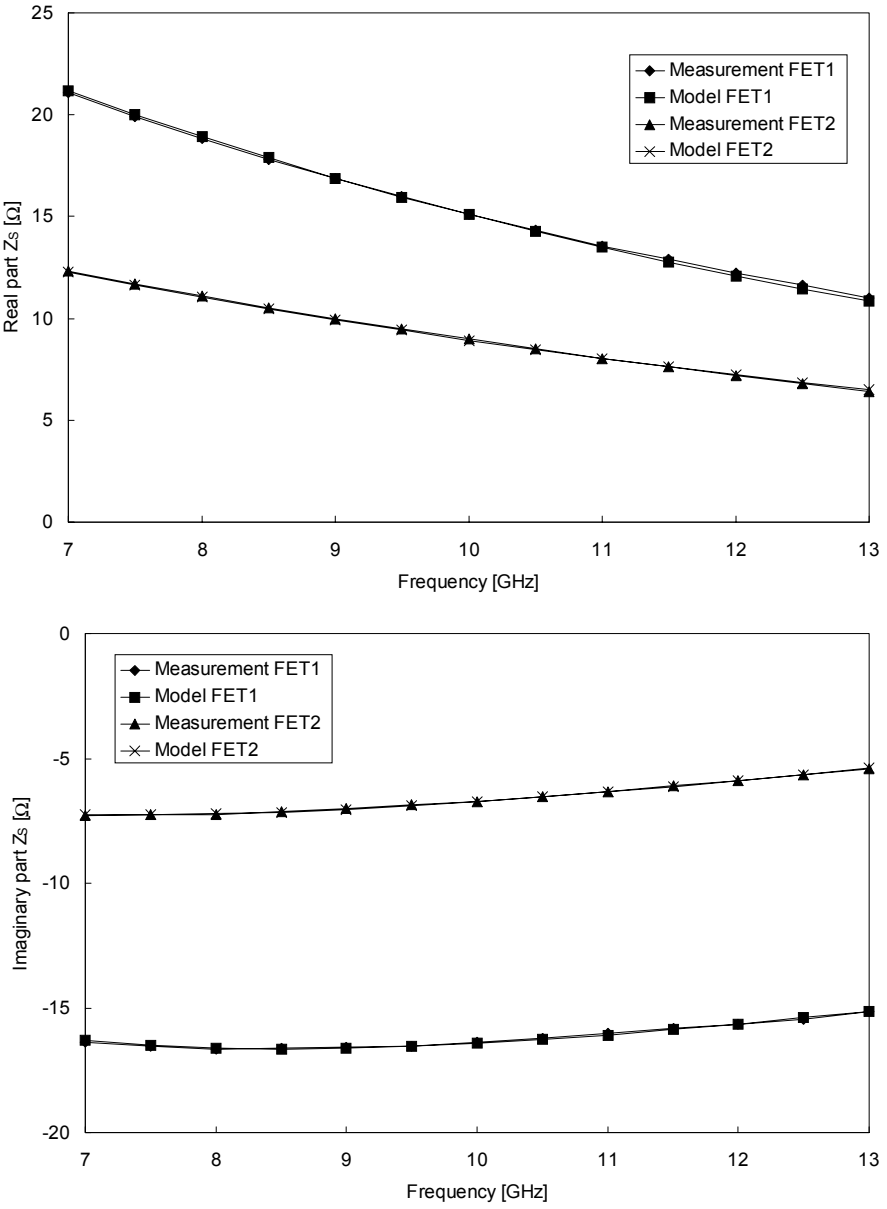

Figure F.4: Comparison between measured and simulated real and imaginary parts of the load impedance of the interstage and input-matching networks. FET1 is a MESFET that has an interdigitated layout with 12 gate fingers that have a unit gate width of 125 µm. FET2 is a MESFET with a fishbone layout which has 48 gate fingers that have a unit gate width of 63 µm. The measurement data is obtained at a V_{DS} = 9 V and a V_{GS} = -1.25 V.

The parameters of the equivalent load impedance that are listed in table F.3 show a difference between the interdigitated and fishbone transistors. For the fishbone transistor, a higher value for C_L is found. This value is higher for the fishbone transistors because in that type of transistor extra capacitance is added by the many source airbridges over the gate feed lines. In addition, the series inductance L_L is higher for the fishbone transistor. This is also caused by the increase in the length of the gate feed lines used in that type of transistor layout. It is also clear that for both MESFET and HFET technology the input resistance R_L is close to 1 Ω for transistors that have a large total gate width (> 2 mm). The results that are depicted in figure F.4 show that a good fit is obtained between the model depicted in figure F.3 and the input impedance of the transistor.

F.4 References

[F.1] D.J. Mellor, "Improved Computer-Aided Synthesis Tools for the Design of Matching Networks for Wide-Band Microwave Amplifiers", *IEEE Trans. Microwave Theory Tech*., vol. MTT-34, pp. 1276-1281, December 1986.

Appendix G Calculation of the dimensions of the layout

G.1 Introduction

The calculation of the dimensions of the layout of the components used is the subject treated in this appendix. A number of equations will be given that enable the calculation of the dimensions of the various components of the matching networks. These equations have been implemented in a computer program, which transforms a matching network with ideal components directly into a list of components with their dimensions, i.e. length and width.

G.2 Equations for the calculation dimensions matching elements

The discussion is started with some simple equations that form the basis for the discussion in the remainder of this appendix. The simplest form of parasitic elements is shown in figure G.1. In this figure, a series capacitor is shown with in series an inductor and an inductor with in parallel a capacitor is shown.

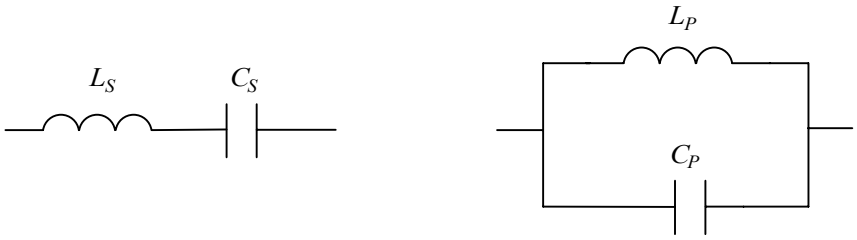

Figure G.1: Elementary circuits with parasitic elements.

The effect of these parasitic elements, when looked at a single frequency, is a modification of the element value required. The equations describing this effect are very simple and have been given here for completeness. The series case gives the following equations for the equivalent capacitance value and equivalent inductor value at the frequency f_C :

$$L_S = L_{ES} + \frac{1}{\omega_C{}^2 \cdot C_S}, \tag{G.1}$$

$$C_S = \frac{C_{ES}}{1 + \omega_C{}^2 \cdot L_S \cdot C_{ES}}. \tag{G.2}$$

In this equation, L_{ES} and C_{ES} are the required equivalent inductance and the required equivalent capacitance. The equation shows that a larger inductance is needed when a parasitic series capacitor is present. For the series capacitor, a smaller value is needed. Of course, the frequency range over which the value found in this way will be valid depends on the resonant frequency of the series connection. For the parallel case depicted in figure G.1, similar equations are found:

$$C_P = C_{EP} + \frac{1}{\omega_C{}^2 \cdot L_P}, \tag{G.3}$$

$$L_P = \frac{L_{EP}}{1 + \omega_C{}^2 \cdot C_P \cdot L_{EP}}. \tag{G.4}$$

In the parallel case, the capacitor becomes larger and the inductor becomes smaller. These very simple examples show a solution for the problem of the influence of parasitic elements on the capacative or inductive behaviour required of a component. In the remainder of this appendix, an example is discussed, which is very commonly encountered, in the design of high-power amplifiers. In this example, the conversion of an ideal low-pass matching network with a bias inductor L_B at the input of the network, into a layout is discussed. The equivalent circuit of this example is shown in figure G.2.

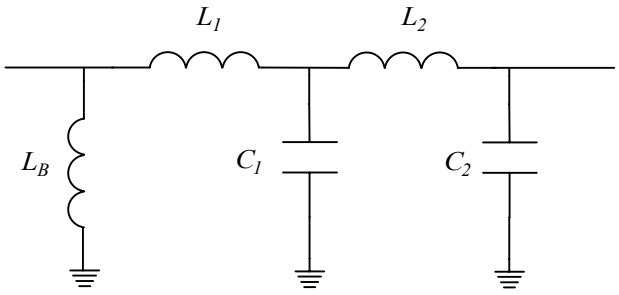

Figure G.2: Equivalent circuit of a low-pass network used for demonstration of electric schematic to layout conversion.

The first step is the calculation of the dimensions of the series elements in this case, the inductors L_1 and L_2. For the calculations of the dimensions of the microstrip lines that are used to form an inductor, see chapter 4, it is necessary to select one of them. Most of the time the width of the microstrip line will be selected because a maximum current density is specified for a given microstrip line width, see section 2.4.1. The length of the microstrip lines can then easily be calculated with the help of equation (A.6). Note that the equivalent

model of the microstrip line is described with a second order polynomial to make an easy analytical calculation of the dimensions possible. After the length and the width of the microstrip lines are known the value of the parasitic capacitors to ground can be calculated with the help of equation (A.7). The next step is the recalculation of the element values to ground taking into account the value of the parasitic capacitance values C_{P1} and C_{P2} of the microstrip lines and the viahole inductance L_{VIA}. The following equations can be used to calculate the new values:

$$L_{B\_NEW} = \frac{L_B}{1+\omega_C{}^2 \cdot L_B \cdot C_{P1}} - L_{VIA}, \tag{G.5}$$

$$C_{1\_NEW} = C_1 - C_{P1} - C_{P2}, \tag{G.6}$$

$$C_{2\_NEW} = C_2 - C_{P2}. \tag{G.7}$$

These equations show that the compensation for the bias inductor L_B is only valid at the selected frequency f_C. In general, this is no problem because the resonance frequency of the parallel circuit L_B and C_{P1} is far from the frequency band of interest. Next, the dimension of the capacitor to ground will be determined. Here both the length and the width of the capacitor can be chosen. In practice most of the time the width is chosen. Other factors that must be taken into account are the inductance of the viahole L_{VIA}, see section 4.3.7, and the extra length L_O in the capacitor that is needed to connect to the viahole and the series microstrip line in the capacitor. This overlap length L_O causes additional series induction, which modifies the value of the capacitor for a given set of dimensions. Equations (A.10) and (A.12) are used to calculate the values of the capacitance C_S and the inductance L_S of the capacitor. These equations are repeated here in a more general form, in appendix A, the actual value of the coefficients is given:

$$L_S = a_1 \cdot \frac{(L_C + L_O)}{W_C} + a_2 \cdot (L_C + L_O) + a_3 \cdot (L_C + L_O) \cdot W_C + L_{VIA}, \tag{G.8}$$

$$C_S = b_1 \cdot W_C \cdot L_C + b_2 \cdot (W_C + L_C). \tag{G.9}$$

In these equations, L_C is the length of the capacitor and W_C the width of the capacitor. In addition, the influence of the overlap length L_O and the viahole inductance L_{VIA} is taken into account in these equations. Combining equations (G.8) and (G.9) with equation (G.2) gives a solution for the calculation of the width or the length of the capacitor. When the length of the capacitor L_C is fixed, the width of the capacitor can be calculated with the help of the following equation:

$$c_3 \cdot W_C{}^3 + c_2 \cdot W_C{}^2 + c_1 \cdot W_C + c_0 = 0, \tag{G.10}$$

in this equation is:

$$c_3 = \omega_C{}^2 \cdot C_{ES} \cdot a_3 \cdot (L_C + L_O) \cdot (b_1 \cdot L_C + b_2), \tag{G.11}$$

$$c_2 = \omega_C{}^2 \cdot C_{ES} \cdot \{(b_1 \cdot L_C + b_2) \cdot [a_2 \cdot (L_C + L_O) + L_{VIA}] + b_2 \cdot L_C \cdot a_3 \cdot (L_C + L_O)\} + b_1 \cdot L_C + b_2, \tag{G.12}$$

$$c_1 = \omega_C{}^2 \cdot C_{ES} \cdot \{(b_1 \cdot L_C + b_2) \cdot a_1 \cdot (L_C + L_O) + b_2 \cdot L_C \cdot [a_2 \cdot (L_C + L_O) + L_{VIA}]\} + b_2 \cdot L_C - C_{ES} \tag{G.13}$$

$$c_0 = \omega_C{}^2 \cdot C_{ES} \cdot b_2 \cdot L_C \cdot a_1 \cdot (L_C + L_O). \tag{G.14}$$

The capacitor required is indicated with C_{ES}. The frequency at which the width of the capacitor W_C is calculated is f_C. The solution to equation (G.10) can be found analytically, see e.g. [G.1]. When the width of the capacitor is fixed the length of the capacitor can be calculated with the help of the following equation:

$$d_2 \cdot L_C{}^2 + d_1 \cdot L_C + d_0 = 0, \tag{G.15}$$

in this equation is:

$$d_2 = \omega_C{}^2 \cdot C_{ES} \cdot \left(\frac{a_1}{W_C} + a_2 + a_3 \cdot W_C \right) \cdot (b_1 \cdot W_C + b_2), \tag{G.16}$$

$$d_x = \left(\frac{a_1}{W_C} + a_2 + a_3 \cdot W_C \right) \cdot b_2 \cdot W_C, \tag{G.17}$$

$$d_1 = \omega_C{}^2 \cdot C_{ES} \cdot \left\{ d_x + \left[\left(\frac{a_1}{W_C} + a_2 + a_3 \cdot W_C \right) \cdot L_O + L_{VIA} \right] \cdot (b_1 \cdot W_C + b_2) \right\} + b_1 \cdot W_C + b_2 \tag{G.18}$$

$$d_0 = \omega_C{}^2 \cdot C_{ES} \cdot \left\{ \left[\left(\frac{a_1}{W_C} + a_2 + a_3 \cdot W_C \right) \cdot L_O + L_{VIA} \right] \cdot b_2 \cdot W_C \right\} + b_2 \cdot W_C - C_{ES}. \tag{G.19}$$

It is clear that for the case where the capacitor is used in series the variable L_{VIA} should be set to zero.

G.3 References

[G.1] M. Abramowitz and I.A. Stegun, “Handbook of Mathematical Functions”, Dover publications Inc., NewYork, 1970.

Appendix H Parametric oscillations

H.1 Introduction

In this appendix the condition for subharmonic oscillations as given by Teeter [H.1] will be derived. The derivation will be based on the assumption that a parametric subharmonic oscillation is the result of pumping a non-linear reactance at a multiple of the oscillation frequency [H.2]. It will be shown that pumping a non-linear reactance will result in a negative resistance at the gate of a FET. The input capacitor of a FET can be seen as a non-linear reactance that can result in subharmonic parametric oscillations. In the next section, a simple equation for the prediction of these subharmonic oscillations is derived.

H.2 Parametric oscillation condition

A direct relation between parametric oscillations and the design of parametric amplifiers can be made [H.3]. The input capacitance at the gate of a transistor varies at the pump frequency ω_0 as a function of time. This variation is described with the following equation:

$$C(t) = C_0 \cdot \left(1 + 2 \cdot \sum_{N=1}^{\infty} \gamma_N \cdot \cos(N \cdot \omega_0 \cdot t) \right). \tag{H.1}$$

Analogue to a parametric amplifier an oscillation frequency ω_1 and an idler frequency ω_2 are assumed. The relation between both frequencies is given by:

$$\omega_2 = \omega_0 - \omega_1 . \tag{H.2}$$

The current and voltage at the first harmonic of these frequencies are described with:

$$v(t) = V_1 \cdot e^{j\omega_1 t} + V_1^* \cdot e^{-j\omega_1 t} + V_2 \cdot e^{j\omega_2 t} + V_2^* \cdot e^{-j\omega_2 t} , \tag{H.3}$$

$$i(t) = I_1 \cdot e^{j\omega_1 t} + I_1^* \cdot e^{-j\omega_1 t} + I_2 \cdot e^{j\omega_2 t} + I_2^* \cdot e^{-j\omega_2 t} . \tag{H.4}$$

If the following equation is used with $N = 1$ for the capacitor,

$$i(t) = \frac{d}{dt} \cdot \left[C(t) \cdot v(t) \right], \tag{H.5}$$

and it is assumed that there only will exist signals at frequency ω_1 and frequency ω_2 then the following impedance matrix is found:

$$\begin{bmatrix} V_1 \\ V_2^* \end{bmatrix} = \begin{bmatrix} \dfrac{1}{j \cdot \omega_1 \cdot C_0 \cdot \left(1-\gamma_1^2\right)} & \dfrac{\gamma_1}{j \cdot \omega_2 \cdot C_0 \cdot \left(1-\gamma_1^2\right)} \\ \dfrac{-\gamma_1}{j \cdot \omega_1 \cdot C_0 \cdot \left(1-\gamma_1^2\right)} & \dfrac{-1}{j \cdot \omega_2 \cdot C_0 \cdot \left(1-\gamma_1^2\right)} \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2^* \end{bmatrix}. \tag{H.6}$$

A simplified equivalent circuit of the gate capacitor terminated with a load impedance Z_L is shown in figure H.1. In this figure, also the source impedance of the transistor Z_S is shown.

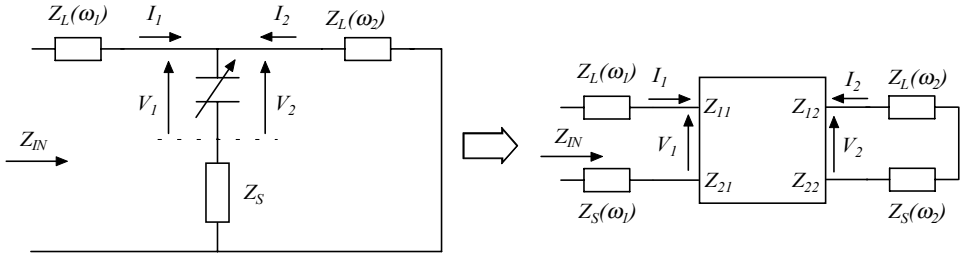

Figure H.1: Simplified equivalent circuit of gate capacitor with load and source impedance.

With the help of this schematic the following equations are found:

$$V_1 = Z_{11} \cdot I_1 + Z_{12} \cdot I_2^*, \tag{H.7}$$

$$V_2^* = Z_{21} \cdot I_1 + Z_{22} \cdot I_2^* = \left(\left(Z_L(\omega_2) + Z_S(\omega_2)\right) \cdot I_2\right)^*. \tag{H.8}$$

These equations result in the following input impedance for the circuit depicted in figure H.1:

$$Z_{IN} = Z_L(\omega_1) + Z_S(\omega_1) + Z_{11} - \frac{Z_{12} \cdot Z_{21}}{\left(Z_L(\omega_2) + Z_S(\omega_2) + Z_{22}^*\right)^*}. \tag{H.9}$$

If it is assumed that a subharmonic oscillation is present at frequency $\omega_0/2$ then $\omega_1 = \omega_2$, see equation (H.2). This in combination with the condition that oscillation may occur when $\mathrm{Re}(Z_{IN}) < 0$ leads to the following equation for the oscillation condition:

$$\left| Z_L(\omega_1) + Z_S(\omega_1) + \frac{1}{j \cdot \omega_1 \cdot C_0 \cdot \left(1 - \gamma_1^2\right)} \right| < \frac{\gamma_1}{\omega_1 \cdot C_0 \cdot \left(1 - \gamma_1^2\right)}. \tag{H.10}$$

This equation shows that:

1. Subharmonic parametric oscillations only exist under large-signal conditions ($\gamma_1 > 0$).
2. The stability margin will improve when the real part of the load impedance is enlarged. This is one of the purposes of the parallel RC stabilisation network described in this thesis, see section 5.6 and 5.7.
3. A third method to enhance the stability would be creating a large impedance at the left side of equation (H.10). This can be realised by resonating out the capacitor ($\omega_1.C_0.(1-\gamma_1^2)$) with the help of a parallel inductor.

The derivation described before gives insight in the existence of $\omega_0/2$ subharmonic oscillation and ways to prevent them. If it is assumed that for all other subharmonic frequencies the condition $\omega_1 = \omega_2$, stays valid the following equation can be used to relate the necessary higher harmonic frequency components, which can lead to subharmonic oscillations:

$$\omega_2 = k \cdot \omega_0 - l \cdot \omega_1, \tag{H.11}$$

and,

$$\omega_1 = \omega_2 = \frac{\omega_0}{n}, \tag{H.12}$$

the relation between the harmonic components is then,

$$k = \frac{1 + l}{n}. \tag{H.13}$$

This equation shows that for a $\omega_0/3$ subharmonic oscillation the combination with the lowest order of harmonics, and therefore the most likely to occur, is the first harmonic of ω_0 and the second harmonic of ω_1. Therefore, this subharmonic component will exist only under strong non-linear conditions. The magnitude of the second harmonic of ω_1 is much smaller than the magnitude at the fundamental frequency. Consequently, the probability that this type of oscillation will occur is much lower than a $\omega_0/2$ subharmonic oscillation. The change for $\omega_0/4$, $\omega_0/5$ etc is even lower. Therefore, in practice mainly $\omega_0/2$ subharmonic oscillation is observed for FETs.

H.3 References

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[H.2] J.F. Imbornone, M.F. Murphy, R.S. Donahue and E. Heaney, "New Insight Into Subharmonic Oscillation Mode of GaAs Power Amplifiers Under Severe Output Mismatch Condition", *IEEE Journal of Solid-State Circuits*, vol.32, pp. 1319-1325, September 1997.

[H.3] A. Blackwell and K. L. Kotzebue, "Semiconductor-Diode Parametric Amplifiers", Prentice-Hall, 1961.

Appendix I Overview of realised high-power amplifiers

I.1 Introduction

In this appendix, pictures of the realised high-power amplifiers not shown in chapter 7, are depicted. In appendix I.2 the amplifiers designed in the MESFET process of Infineon are shown. An overview of the amplifiers designed in the HFET process of FhG-IAF is shown in appendix I.3.

I.2 Overview MESFET amplifier designs

In this section, a picture of the 2-Watt amplifier is shown in figure I.1. The pictures of the 3 and 5 Watt amplifiers are shown in respectively figure I.2 and I.3.

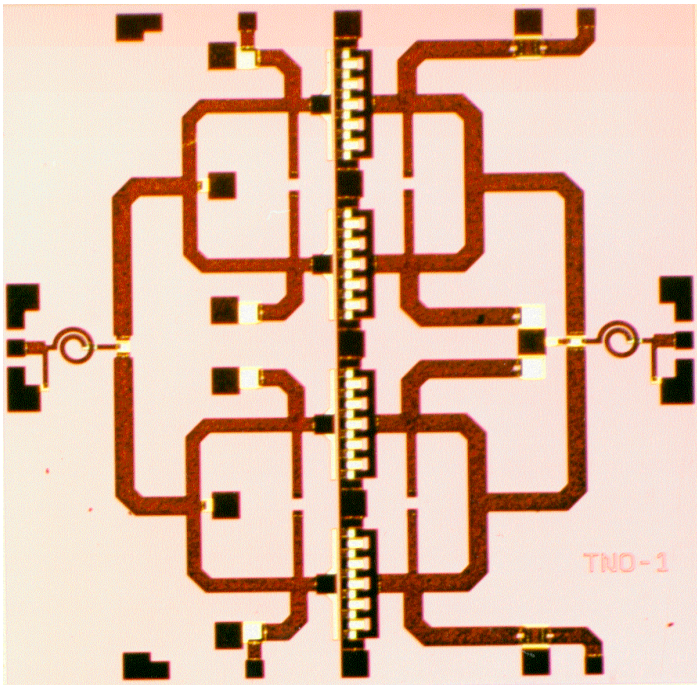

Figure I.1: One-stage 2-Watt power MESFET power amplifier. Chip size is 4 x 4 mm^2.

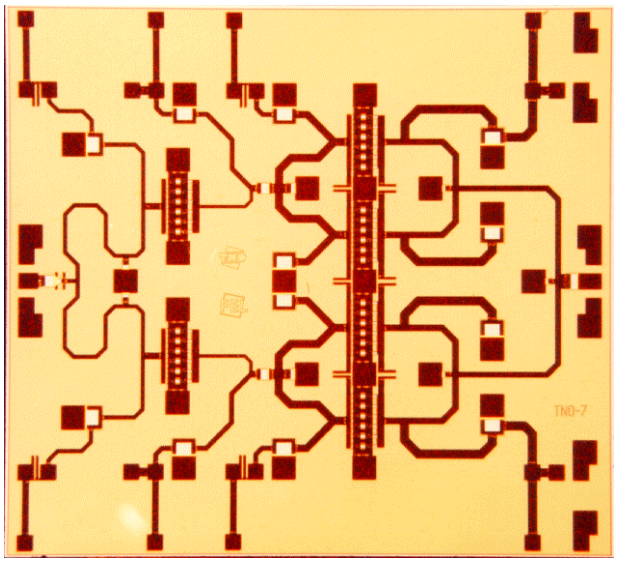

Figure I.2: Two-stage 3-Watt power MESFET power amplifier. Chip size is 3.8 x 3.4 mm^2.

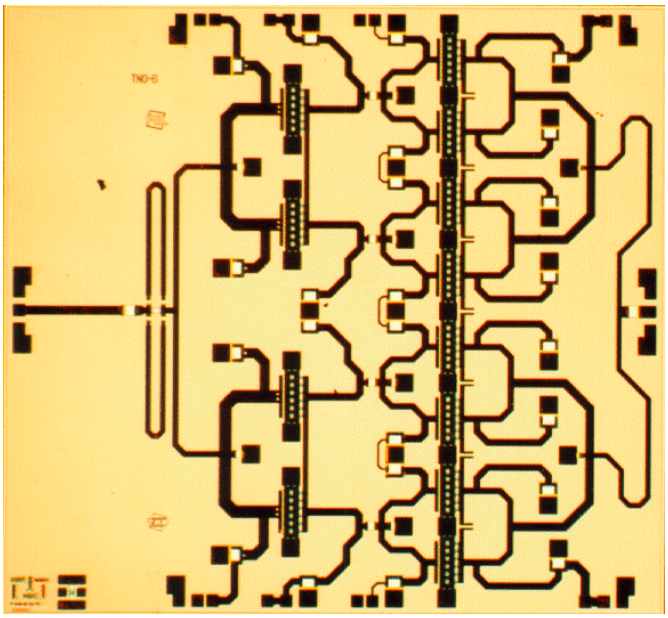

Figure I.3: Two-stage 5-Watt power MESFET power amplifier. Chip size is 4.5 x 4.9 mm^2.

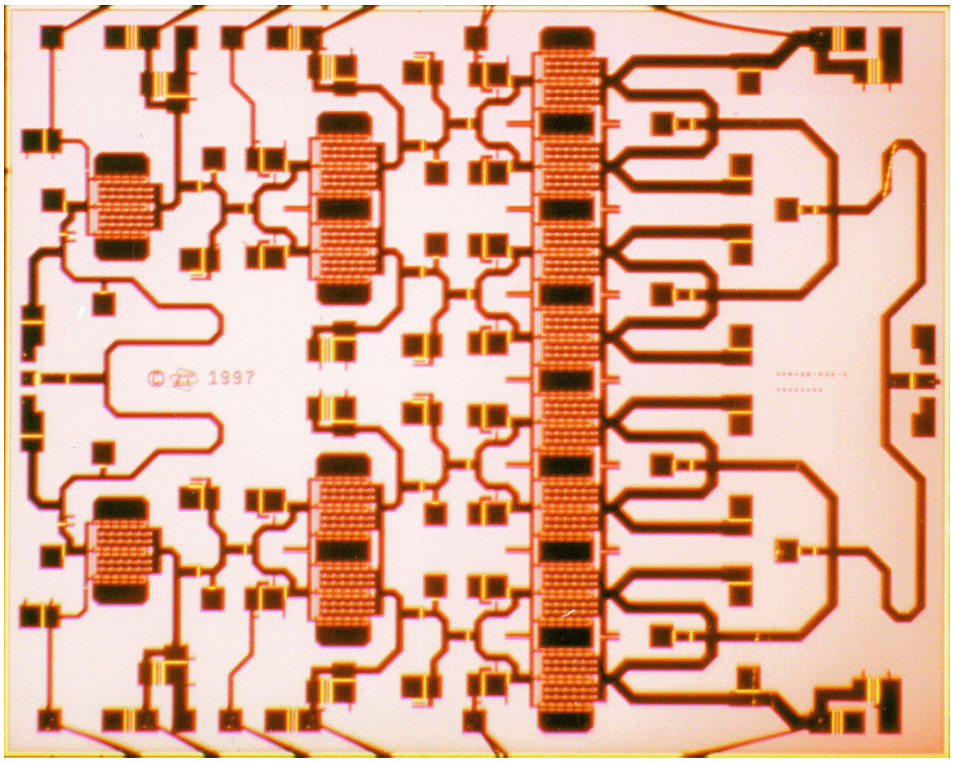

Figure I.4: Three-stage 7 - 10 Watt-power MESFET power amplifier. Chip size is 5.9 x 4.7 mm^2.

I.3 Overview HFET driver amplifier designs

In figures I.5 - I.7 the power amplifiers, realised in the predecessor of the current FhG-IAF HFET technology, are shown. Figure I.5 shows the 0.5-Watt driver amplifier. Two of these driver amplifiers were combined with the help of Lange couplers to form a 1-Watt power amplifier, see figure I.6. A three-stage 1.5-Watt power amplifier is depicted in figure I.7. Finally, in figure I.8 a picture of a 3-Watt power amplifier is shown.

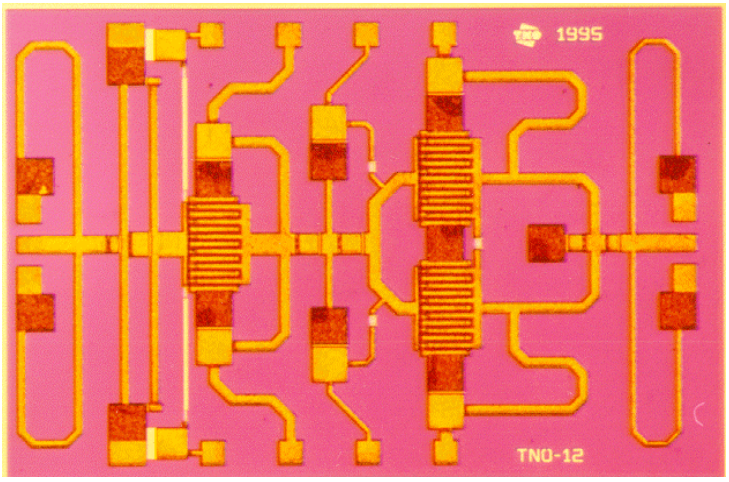

Figure I.5: Two-stage 0.5 Watt HFET driver amplifier. Chip size is 3 x 2 mm^2.

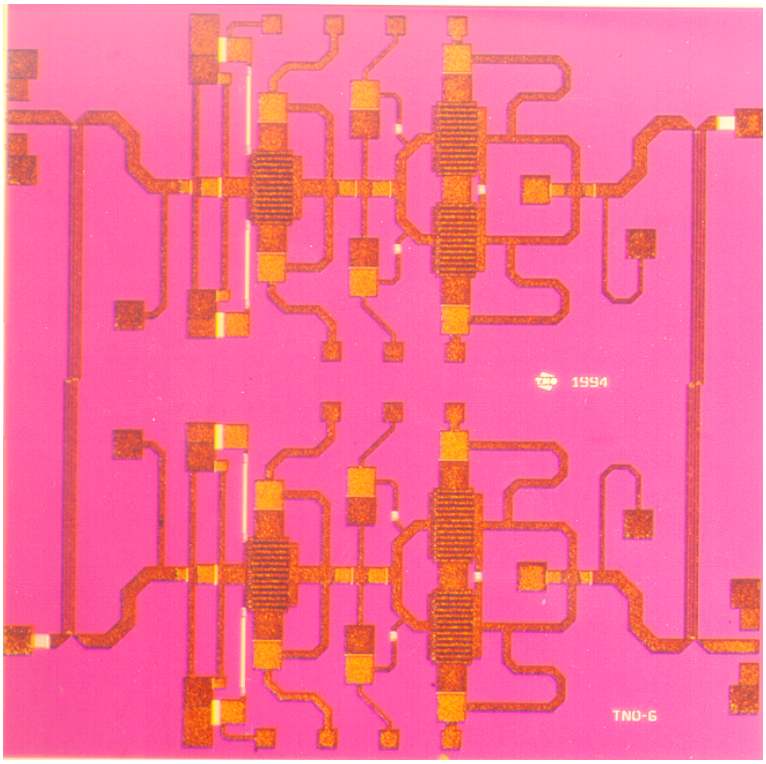

Figure I.6: Two-stage 1-Watt HFET driver amplifier. Chip size is 4 x 4 mm^2.

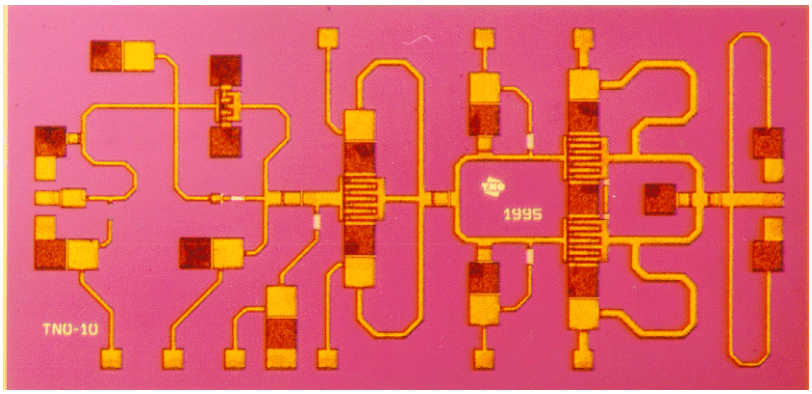

Figure I.7: Three-stage 1.5-Watt HFET driver amplifier. Chip size is 4 x 2 mm^2.

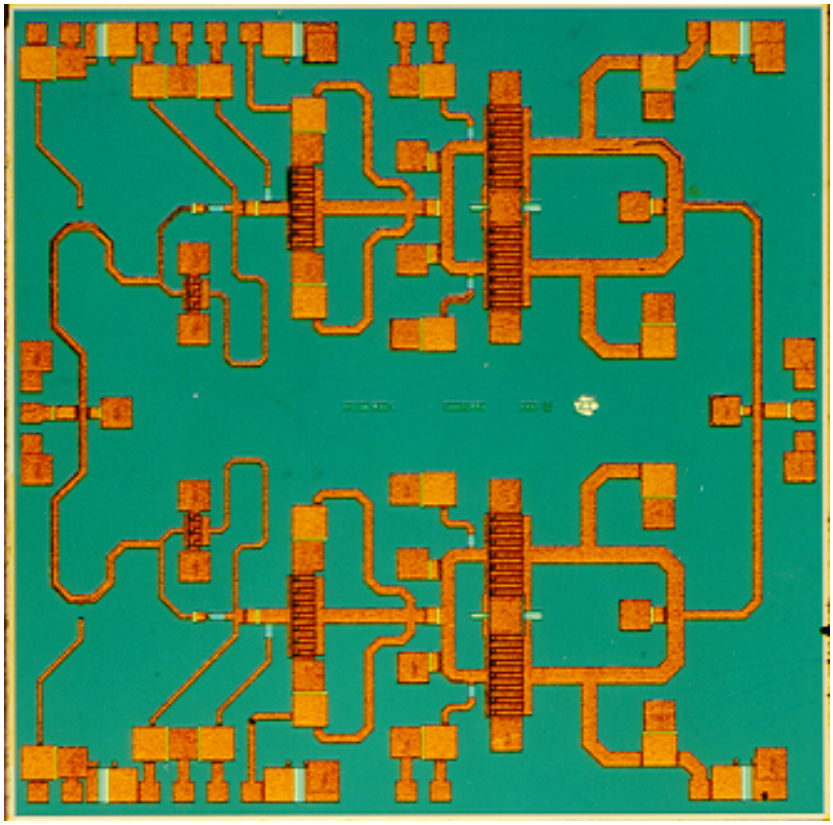

Figure I.8: Three-stage 3-Watt HFET power amplifier. Chip size is 4 x 4 mm^2.

Appendix J Summary X-band HPA results

In this appendix, ***the results presented in this thesis*** are compared with a summary of the X-band power amplifier results that have been published during the last decade. The published results are selected on the following criteria; the relative frequency bandwidth is at least 20% at X-band, and the gain of the amplifier is at least 9 dB. In addition, all of the matching has been performed on chip. The found references are listed in section 7.6. The listed output power, power added efficiency and gain are the average values obtained over the listed frequency band. In table J.1, the MESFET results are listed. The HFET and HBT results are listed in table J.2 and J.3 respectively.

Table J.1: Summary published average performance X-band HPA results realised with MESFET technology.

#	Frequency [GHz]	BW [%]	P_{OUT} [W]	PAE [%]	G_T [dB]	Chip area [mm^2]	Reference
1	7.0 – 10.5	40.8	3.6	41.0	10.0	4.0 x 3.2	[7.14]
2	8.5 – 12.0	34.7	2.5	34.0	10.0	3.8 x 2.2	[7.13]
3	8.0 – 11.0	32.0	12.0	36.0	21.8	4.6 x 4.6	[7.16]
4	8.0 – 12.0	40.8	2.5	27.5	11.0	5.0 x 3.2	[7.15]
5	8.0 – 11.3	34.7	3.4	36.5	10.2	3.8 x 2.4	***[7.3]***
6	7.8 – 10.6	30.8	6.1	34.8	12.9	4.5 x 4.9	***[7.3]***
7	8.0 – 10.0	22.4	9.0	22.5	13.5	5.9 x 4.7	***[7.4]***
8	8.5 – 10.5	21.2	8.9	28.1	19.5	6.5 x 5.0	***[7.5]***

Table J.2: Summary published average performance X-band HPA results realised with HFET technology.

#	Frequency [GHz]	BW [%]	P_{OUT} [W]	PAE [%]	G_T [dB]	Chip area [mm^2]	Reference
1	8.0 – 13.0	49.0	3.6	45.0	15.0	3.6 x 4.3	[7.19]
2	7.5 – 11.5	43.1	9.0	35.0	20.0	4.0 x 4.0	***[7.9, 7.10]***
3	8.0 – 11.0	32.0	6.5	29.0	29.0	5.0 x 4.0	***[7.11]***
4	6.5 – 11.5	57.8	7.9	35.0	15.0	4.5 x 3.0	[7.21]
5	7.5 – 10.5	33.8	5.5	54.0	17.0	3.1 x 3.0	[7.18]
6	8.0 – 10.5	27.3	5.0	35.0	13.0	5.4 x 3.0	[7.17]
7	7.0 – 10.0	35.9	4.5	35.0	17.5	4.5 x 3.3	[7.20]

Table J.3: Summary published average performance X-band HPA results realised with HBT technology.

#	Frequency [GHz]	BW [%]	P_{OUT} [W]	PAE [%]	G_T [dB]	Chip area [mm^2]	Reference
1	8.0 – 12.0	40.8	5.0	20.0	13.0	4.5 x 4.5	[7.27]
2	7.5 – 10.0	28.9	9.3	35.0	13.7	4.5 x 4.4	[7.24]
3	8.0 – 14.0	56.7	2.0	40.0	20.0	5.0 x 2.3	[7.23]
4	6.5 – 10.0	43.4	1.3	36.0	9.5	2.1 x 1.9	[7.22]
5	7.0 – 11.0	45.6	5.5	44.4	12.4	3.0 x 3.4	[7.25]
6	8.0 – 14.0	56.7	3.2	45.0	15.0	4.6 x 2.4	[7.26]

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Summary

Monolithic integrated high-power amplifiers are an essential part of both communication and radar systems. The use of monolithic integrated amplifiers is essential to keep the price of for instance a mobile telephone as cheap as possible. The same argument is also applicable for the use of high-power amplifiers in phased-array radar systems. In such systems, thousands of antenna elements are applied. Each antenna element has its own transmit and receive module with in each module a high-power amplifier. The design, test and results of such high-power amplifiers, intended for X-band (8 – 12.4 GHz) radar applications, are the subjects discussed in this thesis.

Due to the low loss of the passive components and high cut-off frequency of the transistors, GaAs has been chosen as substrate material. Two different transistor technologies have been used. The first technology is the DIOM20HP Metal Semiconductor Field Effect Transistor (MESFET) technology of Infineon. This MESFET technology is a technology, which has been mature for a considerable number of years, and allows for a relatively cheap realisation of high-power amplifiers. The second technology is the Heterojunction Field Effect Transistor (HFET) technology of the Institut für Angewandte Festkörperphysik, Fraunhofer Gesellschaft (FhG-IAF), Freiburg. The latter technology is more expensive than the MESFET technology but has at the same time an improved performance namely a higher gain and output power for a given transistor size.

At the start of the work discussed in this thesis, only little knowledge was available on how to design an integrated high-power amplifier. The design methodology developed is discussed in detail in this thesis. In addition, the models of the passive components used like resistors, MIM capacitors, microstrip discontinuities etc. turned out to be not accurate enough for design at X-band. For this reason, new models have been developed for the passive components mentioned before. These models, which most of the time are based on electromagnetic field simulations, are discussed in this thesis. For the verification of these models a multi-port on-wafer measurement system has been developed. The calibration and verification methods used are discussed in this thesis. In this scope, it is demonstrated that it is essential to remove the coplanar to microstrip transition from the measurement results. This means that self made on-wafer “Line-Reflect-Line” calibration standards have to be used. Based on measurements performed with the help of the developed measurement system is shown that the in the scope of this thesis developed models of passive components are valid to at least 30 GHz.

The necessity that a number of transistors must be used in parallel in a high-power amplifier is discussed in this thesis. Guidelines with respect to the choice of the dimensions of the unit transistor cell have been determined. This choice is determined by the layout of the transistor fingers, the width of the transistor fingers and the number of transistor fingers in parallel. In addition, the thermal aspects, which are relevant for the reliability of the transistor, are considered. Besides the selection of the transistor dimensions, also the equivalent electric model of a transistor is of importance. For this purpose a measurement

system has been developed, which is capable of performing load-pull measurements besides the necessary measurements for the electrical modelling. This measurement system is discussed in detail in this thesis. The load-pull measurement data gives essential information for model verification and gives insight in the large-signal performance, e.g. the output power of the transistor. The information acquired with the help of the load-pull measurement system also gives information regarding the optimum load impedance of the transistors. This information is also used for the design of the matching networks. Besides the determination of the dimensions and modelling of the transistor unit cell, also the effect of the selected operating class on the output power and power added efficiency of the transistor is analysed. For broadband X-band power amplifiers as optimum, a class AB operating point is found. In addition, the stability of the unit transistor cell and the design of stability improvement networks is discussed.

The design of the matching networks of the power amplifiers is done from the output of the amplifier to the input of the amplifier. For the design of the matching networks, the following strategy is used. First, a model of the load and source impedance of the matching networks is determined. In the next step these impedances are made real in such way that the necessary bias supplies can be provided to the transistors. Then the component values of the matching network are determined. As a final step, these component values are optimised to minimise the effect of the component losses and to maximise the frequency band. For the conversion of the ideal electrical component values into a layout a program has been developed, which calculates the dimensions of the components used.

After the design of the matching networks has been completed, the overall high-power amplifier performance must be simulated and optimised. With this, problems occur due to the strong non-linear character of the power amplifier. These problems can result in non-convergence of the simulation and long simulation times. The found solution where only one transistor per amplifier stage is simulated is discussed in this thesis. As final step in the amplifier design, the stability of the amplifier is analysed. The stability enhancement networks and stability analysis program in this scope developed are discussed in detail.

The results of a number of high-power amplifiers, which are developed based on the before mentioned models and design methodology, are discussed. For both of the used transistor technologies amplifiers with an output power of 10 Watt have been realised at X-band. The results show an excellent agreement between measurement and simulation results. This demonstrates the validity of the models and design methodology used. The results of the HFET amplifiers are better than the MESFET amplifier ones. For the HFET amplifiers, more or less the same output power has been reached with only half the occupied chip area. The last HFET amplifier that is discussed in this thesis demonstrates that it is possible to realise an amplifier that combines a high output power with a high gain. With this amplifier the number of chips necessary in a transmit receive module of a phased-array radar can be reduced. The majority of the models, measurement techniques and design methodology discussed in this thesis can be used in other frequency bands than X-band and for other applications than phased-array radar.

Samenvatting

Monolithisch geïntegreerde hoogvermogensversterkers zijn een essentieel onderdeel van zowel communicatie- als radarsystemen. Het gebruik van monolithisch geïntegreerde versterkers is essentieel om bijvoorbeeld een mobiele telefoon goedkoop te houden. Dit zelfde argument is ook van toepassing voor het gebruik van hoogvermogensversterkers in phased-array radar systemen. In dergelijke systemen worden duizenden antenne elementen toegepast. Ieder antenne element heeft een eigen zend- en ontvangstmodule met in iedere module een hoogvermogensversterker. Het ontwerp, het testen en de resultaten van dergelijke hoogvermogensversterkers, in eerste instantie bedoeld voor X-band (8 – 12.4 GHz) radar toepassing, is het onderwerp van dit proefschrift.

Vanwege de verliesvrijheid van de passieve componenten en de hoge afsnijfrequentie van de transistors is gekozen voor GaAs als substraat materiaal. Een tweetal verschillende transistor technologieën is gebruikt. De eerste technologie is de DIOM20HP Metal Semiconductor Field Effect Transistor (MESFET) technologie van Infineon (D). De MESFET technologie is een al sinds vele jaren volwassen technologie waarmee relatief goedkope hoogvermogensversterkers gefabriceerd kunnen worden. De tweede technologie is de Heterojunction Field Effect Transistor (HFET) technologie van het Institut für Angewandte Festkörperphysik, Fraunhofer Gesellschaft FhG-IAF, Freiburg (D). Deze laatste technologie is weliswaar duurder maar heeft ook sterk verbeterde eigenschappen, te weten hogere versterking en hoger uitgangsvermogen voor gegeven transistorafmetingen.

Bij de start van het werk, zoals beschreven in dit proefschrift, was weinig kennis aanwezig op welke wijze een geïntegreerde hoogvermogensversterker ontworpen moest worden. De ontwikkelde ontwerpprocedure is in detail bediscussieerd in dit proefschrift. De modellen van de gebruikte passieve componenten zoals weerstanden, MIM capaciteiten en microstriplijn discontinuïteiten enz. bleken of niet aanwezig, of niet nauwkeurig genoeg te zijn voor het ontwerp van X-band hoogvermogensversterkers. Daarom zijn nieuwe modellen voor de voorgenoemde componenten ontwikkeld. De toegepaste modellen, die veelal gebaseerd zijn op elektromagnetisch simulaties, worden in dit proefschrift besproken. Voor de verificatie van deze modellen is een multi-poort on-wafer meetsysteem ontwikkeld. De gebruikte calibratie- en meetalgorithmes zijn bediscussieerd in dit proefschrift. In dit kader is ook aangetoond dat de coplanair naar microstrip overgang, zoals die aanwezig is tussen het meetsysteem en de te meten structuur, uit het meetresultaat geëxtraheerd dient te worden. Dit betekent dat gebruik dient te worden gemaakt van zelf ontwikkelde on-wafer "Line-Reflect-Line" calibratie structuren. Op basis van het aldus ontwikkelde meetsysteem is aangetoond dat de in het kader van dit proefschrift ontwikkelde modellen van passieve componenten tot minstens 30 GHz geldig zijn.

De noodzaak dat een aantal parallel staande transistors gebruikt moet worden in een hoogvermogensversterker is besproken in dit proefschrift. Een aantal richtlijnen met betrekking tot de keuze van de afmetingen van deze zogenaamde transistor eenheidscellen is bepaald. De keuze wordt bepaald door de lay-out van de transistor vingers, de breedte

van de transistor vingers en het aantal transistor vingers dat parallel in een transistor eenheidscel gebruikt kan worden. Tevens worden de van belang zijnde thermische aspecten, die de betrouwbaarheid van de transistors bepalen, bekeken. Naast de dimensionering van de transistor is ook de elektrische modellering van belang. Hiervoor is een meetopstelling ontwikkeld die, naast de meetgegevens nodig voor de modellering, ook zogenaamde load-pull metingen kan verrichten. Dit meetsysteem wordt in detail besproken in dit proefschrift. De load-pull meetdata leveren essentiële informatie voor de modelverificatie en de hoogvermogens eigenschappen van de transistor zoals het uitgangsvermogen. De met het load-pull meetsysteem verkregen informatie omtrent de optimale belastingimpedantie van de transistors wordt gebruikt voor het ontwerp van de aanpasnetwerken. Naast de dimensionering en modellering van de transistor eenheidscellen is ook het effect van de klasseninstelling op het uitgangsvermogen en het rendement van de transistor bekeken. Voor breedbandige X-band vermogensversterkers is als optimum een klasse AB instelpunt gevonden. Als volgende punt worden de stabiliteitanalyse en het ontwerp van stabiliteitverbeterende netwerken voor de transistor eenheidscellen besproken.

Het ontwerp van de aanpasnetwerken van de vermogensversterkers vindt plaats van de uitgang naar de ingang. Voor het ontwerp van deze aanpasnetwerken is de volgende methodiek gebruikt. Als eerste stap wordt een model van de belastingsimpedanties van het netwerk bepaald. In de volgende stap worden deze impedanties reëel gemaakt op een dusdanige manier dat de benodigde voeding aan de transistors kan worden aangeboden. Vervolgens worden de component waarden van het aanpasnetwerk bepaald. Als laatste stap wordt het geheel geoptimaliseerd om het effect van de aanwezige verliezen in de componenten te minimaliseren en de frequentieband te maximaliseren. Voor het omzetten van de ideale component waarden naar een lay-out is in het kader van dit proefschrift een programma ontwikkeld, dat de afmetingen van deze componenten bepaalt.

Nadat de aanpasnetwerken zijn ontworpen moet de complete vermogensversterker gesimuleerd en geoptimaliseerd worden. Hierbij treden door het sterke niet lineaire karakter van de versterkers grote problemen op, te weten veel convergentie problemen van de simulator en lange simulatietijden. De hiervoor gevonden oplossing waarbij slechts een enkele transistor per versterkertrap wordt gesimuleerd is beschreven in dit proefschrift. Als laatste stap in het versterkerontwerp wordt de stabiliteit van de versterker besproken. De in dit kader gevonden stabiliteit verbeterende netwerken en het ontwikkelde stabiliteitanalyseprogramma voor een complete versterker worden in detail besproken.

De resultaten van een aantal met voornoemde modellen en ontwerp methodieken ontwikkelde geïntegreerde hoogvermogensversterkers worden behandeld. Voor beide gebruikte transistortechnologieën zijn uitgangsvermogens van 10-Watt in X-band gerealiseerd. De getoonde resultaten laten tevens een excellente overeenkomst tussen simulatie- en meetresultaten zien. Dit toont de geldigheid aan van de gebruikte modellen, meettechnieken en ontwerpmethodieken. Zoals verwacht zijn de resultaten van de HFET versterkers beter dan die van de MESFET versterkers. Globaal gesproken wordt voor de HFET versterkers hetzelfde uitgangsvermogen bereikt op de helft van het chipoppervlak. Verder tonen de resultaten van de laatste in dit proefschrift besproken HFET versterker aan dat het mogelijk is een versterker te realiseren die gelijktijdig zowel een hoog

uitgangsvermogen als een hoge versterking heeft. Hiermee kan het aantal chips dat in een zend- en ontvangst module gebruikt wordt, worden gereduceerd.

De meeste van de in dit proefschrift besproken modellen, meettechnieken en ontwerpmethodieken zijn zonder meer toepasbaar op andere frequentiebanden dan de X-band en voor andere toepassingen dan alleen vermogensversterkers voor phased-array radars.

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Curriculum Vitae

Peter de Hek was born in Hardinxveld Giesendam, in the Netherlands, on August 29, 1963. After graduating high-school (HAVO) in 1981 he started studying electrical engineering at Dordrecht Polytechnic. In 1985, he received his B.Sc. degree. His bachelor thesis dealt with communication between a number of mainframe computers. After fulfilling his service in the Dutch army, he joined the TNO Physics and Electronics Laboratory in 1987. He started working on the characterisation and design of antennas. Since 1990, he is involved in the design and characterisation of Monolithic Microwave Integrated Circuits. During the last years, he has been involved as project leader in a number of international projects. These projects involve the design of power amplifiers in MESFET, HFET and HBT technology. In September 2001, he was awarded with the price for the best oral paper presented during the GAAS/EuMW conference.