Common-mode currents and printed circuit boards

COMMON-MODE CURRENTS AND PRINTED CIRCUIT BOARDS

F.B.M. van Horck*, A.P.J. van Deursen**, P.C.T. van der Laan**
*Philips Components, P.O. Box 80002, 5600 JB Eindhoven, the Netherlands
**High-Voltage and EMC group, Eindhoven University of Technology,
P.O. Box 513, 5600 MB Eindhoven, the Netherlands
(Principle contact: a.p.j.v.deursen@cle.tue.nl)

Abstract: Common-mode (CM) currents through cables attached to printed circuit boards (PCB's) are often the main cause of interference and may even dominate the direct radiation of the board. In this contribution we predict the coupling between the differential-mode (DM) circuit on the board and the CM circuit in a Bersier setup, by means of a rapid transmission-line model. This coupling is expressed as the ratio of the CM current and the DM current. Several boards with different complexity were studied in the frequency domain. For demonstration purposes a board with modern digital electronics was developed. Measurements between 100 kHz – 1 GHz agree with the TL models.

1. Introduction

It is important to know the electromagnetic-compatibility (EMC) properties already in the design phase of a product. The aim of the present study is to predict in a rapid way the common-mode (CM) currents through the cables generated by the signal or differential-mode (DM) currents on a printed circuit board (PCB), see Fig. 1. The calculations are based on a coupled transmission-line model. The short time needed allows to judge changes in the CM current during the design stage of a product, thus avoiding expensive redesigns after prototyping. Routing of tracks, placement of decoupling capacitors etc. can then readily be optimized with respect to EMC.

The tracks and the ground plane of the PCB's in electronic systems interconnect the devices or components on the board (see Fig. 1). The tracks and the devices form closed loops for the signal or DM currents. Cables between PCB's or apparatus are primarily intended to transport DM signals. However, each cable is also a part of a larger circuit which closes via the environment of the PCB (parasitic capacitances in Fig. 1) or via ground leads; the large metallic plane below GP in Fig. 1 is often a nearby cabinet panel, e.g. in a computer. The CM current in this circuit is a net current through the cables. Because of their length, the cables act as efficient antennas for the CM currents, often producing more emission than the PCB itself. This fact is the basis of precompliance EMC tests for emission [1—5] and immunity; CM currents are measured or injected in cables attached to apparatus or (sub)systems.

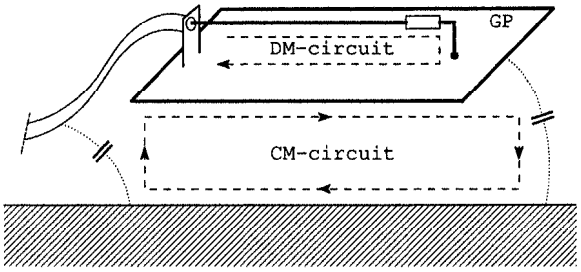

Fig. 1: Differential-mode (DM) and common-mode (CM) definition. The CM current path closes via the ground plane (GP), the parasitic capacitances and the metallic plane below GP.

The (conduction) current based method was proposed by Bersier [6] to replace the extensive standard tests in which electromagnetic fields are applied or measured at larger distance from the equipment. Nowadays precompliance tests often suffice to demonstrate conformity with the European EMC requirements. The expensive and laborious full-compliance radiated emission and radiated immunity tests are replaced by a rapid and a simple method.

Bergervoet's *et al.* [7] CM skeleton model bears resemblance to Bersier tests. These authors model the PCB and all components on it by CM voltage-sources at the edges of the PCB, which drive the CM current into each cable attached to the PCB. The voltage sources and their internal impedances were determined by measurements. Alternatively, a program based on the partial-element analysis proposed by Ruehli [8] or the equivalent circuit analysis implemented in Fasterix [9] may calculate the source. These calculations still consume appreciable time.

The theoretical model and the experimental setup are kept close to the successful Bersier precompliance setup. The tracks and the CM circuit are modeled as coupled transmission lines. In combination with accurate analytical approximations to be presented

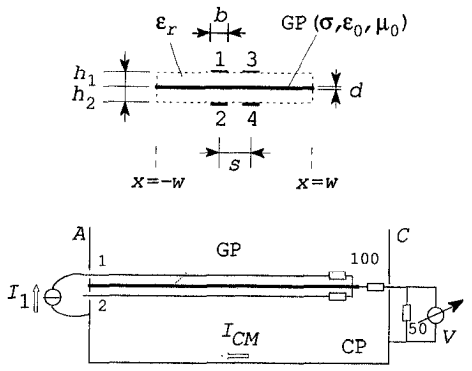

Fig. 2: Upper part: Cross section showing four tracks on a triple layer PCB with a continuous ground plane (GP) as middle layer. Lower part: Longitudinal cross section of the precompliance setup. The PCB is mounted between two endplates A and C. The current I_1 is injected in track 1 on top and returns through the GP. The common mode current I_{CM} is measured over the 150 Ω load which models a cable at resonance.

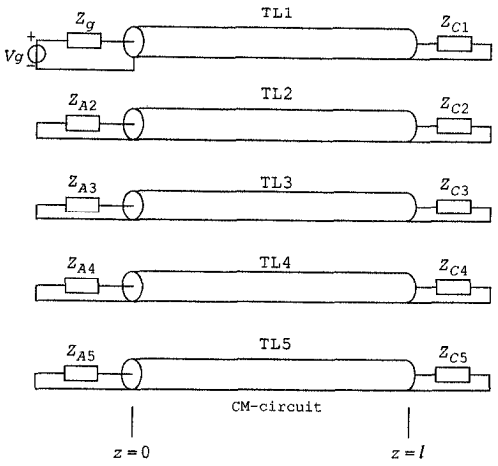

Fig. 3: Transmission-line (TL1-TL4) model of the four track PCB in Fig. 2; TL5 incorporates the DM–CM couplings as discussed in the text. The near side $z = 0$ corresponds with the side of brass plate A, the far end $z = \ell$ with brass plate C. The terminating impedances are discussed in Section 3.

for the TL parameters, the TL approach strongly reduces the computational effort or the computer hardware requirements. The comparison of the results with actual measurements was encouraging, in spite of the many simplifications by the model chosen.

The PCB's studied (Fig. 2) have three layers. A continuous ground plane (GP) of length $\ell = 20$ cm is the middle layer; the width $2w$ was varied between 5 and 10 cm. Tracks of $b = 1.5$ mm width are placed at $h_{1,2} = 1.5$ mm above and below the GP. The dielectric constant ε_r of the epoxy insulation is 4.7. Up to four tracks at different positions on the PCB allow us to study the DM-DM coupling or crosstalk as well (see e.g. [10—12]). The tracks run parallel to the length of the PCB; in later calculations track 1 meanders over the surface. A DM current is injected at side A; the tracks terminate into different impedances near end C. The CM circuit consists of the GP and a large brass plate (cabinet panel, CP) under the PCB at the distance $h_{CP} = 1$ cm. In a precompliance test, the common mode current is usually measured with a 150 Ω total CM load at C, which models the CM-radiation resistance of a cable at resonance. This resonance condition may not occur at all frequencies in the DM signal, but will most probably do so at some frequency for which the emission limits might then be exceeded.

2. Transmission-line approach

The four DM circuits and the CM circuit in Fig. 2 are considered as a set of transmission lines (TL's), see also Fig. 3. The coupling between the lines is described by the resistive and inductive transfer impedance and by the capacitive transfer admittance; the low-frequency transfer-impedance behavior is discussed elsewhere [10, 11]. We regard the tracks over the GP as microstrip lines. The dominant mode in a microstrip line is quasi-TEM: a TEM wave adapted to include a nonhomogeneous dielectric by modifying the line capacitance, and the conductor losses by adding a series resistance. Gupta *et al.* [13] give an overview of the vast literature published over the last decades and expressions for the characteristic impedance Z_m and the effective dielectric constant $\varepsilon_{r,eff}$ for a single track above a very wide GP:

$$Z_m = \frac{\eta}{2\pi\sqrt{\varepsilon_{r,eff}}} \ln\left(\frac{8h}{b} + 0.25\frac{b}{h}\right) \qquad (1)$$

$$\varepsilon_{r,eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left\{(1 + \frac{12h}{b})^{-\frac{1}{2}} + \right.$$
$$\left. + 0.04(1 - \frac{b}{h})^2\right\} \qquad (2)$$

where $\eta = \sqrt{\mu_0/\varepsilon_0} = 120\pi$ Ω and $b \leq h$; these equations apply for our tracks. The self-inductance L_s can be obtained from $L_s = Z_{0m}/c_0$, with Z_{0m} the characteristic impedance of the microstrip with the dielectric replaced by vacuum or $\varepsilon_{r,eff} = 1$, and c_0 the velocity of light in vacuo. For all tracks on our PCB's we use the same $L_s = 414$ nH/m, calculated as if the GP were of infinite extent. Inserting the proper value for $\varepsilon_{r,eff} = 3.34$, one finds for the capacitance $C_s = 88.9$ pF/m and for $Z_m = 68$ Ω. The series impedance Z_s for the track is $Z_s(\omega) = R_{DC} + R_s(\omega) + j\omega L_s$, where R_{DC} and $R_s(\omega)$ are the d.c. and skin-effect resistances.

Figure 3 shows the four tracks as coupled microstrip lines TL1-TL4 with the ground plane (GP) as reference; $z = 0$ corresponds with the side of plate A (near end) and $z = \ell$ with the side of plate C (far

end). The TL5 describes the CM current through the GP with return CP. The 5×5 impedance matrix $\mathbf{Z}(\omega)$ per unit length with GP as reference is then given by $\mathbf{Z}(\omega) = \mathbf{Z_d}(\omega) + \mathbf{Z_t}(\omega)$, with $\mathbf{Z_d}$=diag$(Z_s, Z_s, Z_s, Z_s, Z_{CM})$ the self-impedance diagonal matrix, $\mathbf{Z_t}(\omega)$ the transfer-impedance matrix with zeros on the diagonal, and $Z_{CM} = j\omega L_{CM}$ the proper impedance of the CM circuit formed by GP and CP. For high frequencies, the $\mathbf{Z_t}$ matrix is predominantly given by the mutual inductances M between the tracks and the CM circuit, which can readily be calculated from conformal mapping as described in [11, 12]; then $\mathbf{Z_t} = j\omega\mathbf{M}$ with $\mathbf{M}$ the inductance matrix with zeros on the diagonal. The self inductance L_{CM} of the CM circuit may be taken from Kuester and Chang [14] for large $2w/h_{CP}$. The capacitance C_{CM} in vacuum results from $C_{CM} \simeq 1/c_0^2 L_{CM}$. The 1.5 mm dielectric layer increases this value by about 13 percent for $h_{CP} = 1$ cm.

As admittance matrix we have $\mathbf{Y}(\omega) = j\omega\mathbf{C}$, where $\mathbf{C}$ is the 5×5 capacitance matrix. It is more difficult to accurately calculate the off-diagonal elements of the static capacitance matrix because of the boundary conditions on the dielectric. The numerical implementation and calculations are described in detail elsewhere [11, App. B]. From these calculations we derived analytical approximations which suffice in our TL model and considerably speed up the computations for a PCB.

For convenience, suppose that only one track i (Fig. 2) is present. The capacitance matrix then becomes

$$\mathbf{C} = \begin{bmatrix} C_s + C_{i-CP} & -C_{i-CP} \\ -C_{i-CP} & C_{CM} + C_{i-CP} \end{bmatrix}. \qquad (3)$$

In vacuo the capacitance matrix $\mathbf{C_0}$ satisfies the well-known relation

$$\mathbf{L}\mathbf{C_0} = \frac{1}{c_0^2}\mathbf{I_2} \qquad (4)$$

with $\mathbf{I_2}$ the 2×2 identity matrix and

$$\mathbf{L} = \begin{bmatrix} L_s & M_s \\ M_s & L_{CM} \end{bmatrix}, \qquad (5)$$

the inductance matrix. Fitting the rigorously calculated coupling capacitances with 'simple' expressions, we found the following approximate relation between C_{i-CP} and $C_{i-CP,0}$, the capacitive coupling coefficients with and without dielectric

$$C_{i-CP} \simeq \frac{C_{i-CP,0}}{\varepsilon_{r,eff}{}^{1/4}}. \qquad (6)$$

valid for $h_1 = h_2 = h$ and $b_1 = b_2 = b$. This procedure is tested for a wide range of parameters. For a maximum deviation of 25 percent between numerical results and approximate analytical expressions this parameter range is: $1 \le \varepsilon_r \le 12$, $0 \le x/2w \le 0.9$, $0.5 \le b/h \le 3$, $0.05 \le w/p \le 1$, and $0.1 \le 2w/h_{CP} \le 3$. For practical dielectrics used for PCB's, the error without the correction in the denominator was larger than 50 percent. The calculated diagonal elements of $\mathbf{C}$ scaled proportionally to $\sqrt{\varepsilon_{r,eff}}$, in agreement with (1) and (2).

A similar approach also applies to the capacitive coupling of the crosstalk between two circuits. Then the coupling between, say, tracks 1 and 2 becomes $C_{12} \simeq C_{12,0}/\sqrt{\varepsilon_{r,eff}}$ [11, 12].

With the matrices $\mathbf{Z}(\omega)$ and $\mathbf{Y}(\omega)$ the response of the system of coupled transmission lines can be calculated [15]. We will only consider linear loads here; this allows the modal expansion in the frequency domain of Djodjević and Sarkar [16].

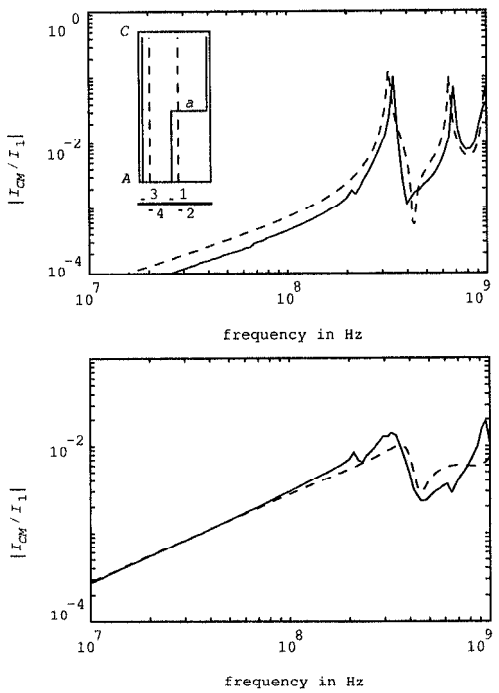

Fig. 4: Upper part: The measured (—) and calculated (- - -) current transfer $|I_{CM}/I_1|$ between the DM circuit of track 1 and the CM circuit. The current I_1 is injected in TL1 at side A (see also Figs. 2 and 3); for the terminations Z_{Aj} $(j = 1, \cdots, 5)$ see the main text. The inset shows bent track 1 and straight track 3 (—) on the upper layer of the PCB and tracks 2 and 4 (- - -) on the lower layer. All tracks are open ended to the ground plane at side C, i.e. $Z_{Cj} = \infty$ $(j = 1, \cdots, 4)$. Lower part: The same current transfer with the tracks terminated into $Z_m = 68\ \Omega$ at side C, i.e. $Z_{Cj} = 68\ \Omega$ $(j = 1, \cdots, 4)$.

3. PCB with linear terminations

The TL method appeared to work quite well for straight tracks parallel to the long axis [11], both for DM–DM crosstalk and for DM–CM conversion. Here we present the results on a PCB with a bend in track 1 half way on the GP (inset upper part of Fig. 4). The short perpendicular part a is included in the TL picture as an intermediate delay line. The CM circuit under part a is modeled as a TL section

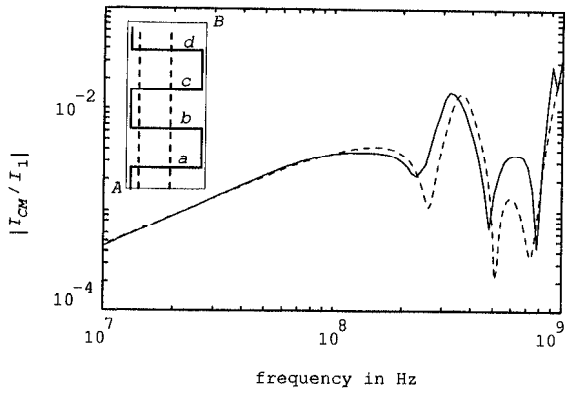

Fig. 5: The measured (—) and calculated (- - -) current transfer between the DM circuit of track 1 and the CM circuit. The current I_1 is injected at in TL1 at side A (see also Figs. 2 and 3). The inset shows the meandering track 1 (—) on the upper layer of the PCB and tracks 2 and 4 (- - -) on the lower layer. All tracks are terminated into $Z_m = 68\ \Omega$ at the far end C, i.e. $Z_{Cj} = 68\ \Omega$ $(j = 1, \cdots, 4)$.

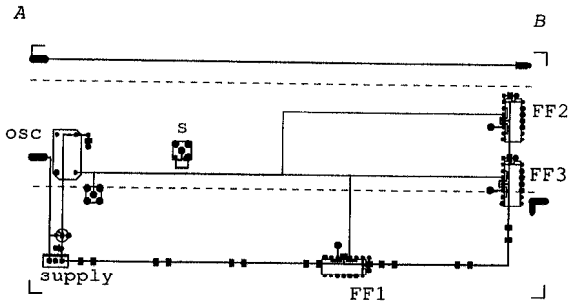

Fig. 6: Top view of the HCT board with three D flip flops (FF's) and a clock oscillator (OSC). The solid lines indicate the tracks at the upper layer of the PCB, the dashed lines those at the lower layer. Apart from the signal track three test tracks were incorporated. The DM current is measured with inductive current sensors s. The supply voltage was regulated by a stabilizer.

of the same length, with its inductance and capacitance modified such that the speed of propagation is a factor 50 larger, but the characteristic impedance remains constant. No magnetic coupling is expected between DM part a and the CM circuit. The current I_1 is injected in track 1 (TL1) by a voltage source V_g with impedance $Z_g = 50\ \Omega$ (see Fig. 3). The other tracks were open ended at the near end A; therefore, the impedances $Z_{Aj} = \infty$ $(j = 2, \cdots, 4)$ and $Z_{A5} = 0$ since the CM circuit is short circuited. The 150 Ω cable impedance is modeled by Z_{C5} in the TL model. Figure 4 shows the DM to CM current transfer with all tracks open ended to the GP near the end C $(Z_{Cj} = \infty,\ j = 1, \cdots, 4)$ or with the tracks terminated there into the characteristic impedance of 68 Ω $(Z_{Cj} = 68\ \Omega,\ j = 1, \cdots, 4)$; in both situations the near end impedances Z_{Aj} were the same as discussed above. For this PCB TL calculations and measurements agree quite well. The first peak in the open-ended case at 320 MHz is the half-wavelength resonance of track 1 with total length 25 cm and the transfer attains values well over 10^{-1}. The first minimum near 400 MHz is mainly caused by the velocity difference in the DM and CM circuit.

Figure 5 shows the current conversion of a more complicated PCB, with tracks terminated into Z_m at C. Track 1 meandered over the upper surface as shown in the inset of Fig. 5. The perpendicular parts $a, \cdots, d$ are again modeled as delay lines with capacitive coupling to the CM circuit. The general behavior with frequency, in particular near the maxima, is quite correctly calculated.

4. PCB with logic circuits

Two demonstration boards were designed with three D flip-flops (FF's, HCT and IILL type) driven by a clock oscillator; see Fig. 6 where only the HCT board is given, the HLL board is nearly the same. Each FF had its own branch of the signal trace; this provided some complexity and still kept the bookkeeping effort manageable. Clock oscillator frequencies were between 10 and 100 MHz; a translator placed near the oscillator on the HLL board transformed the 5 V signal into a 3.3 V signal.

We measured the actual DM current delivered by the clock. An inductive sensor s was placed at the position indicated; the mutual inductance M_{sens} with respect to the clock signal track was 0.97 nH for the HCT print, and 0.29 nH for the HLL print. The sensor output V_{sens} was integrated numerically: $I^m_{DM} = V_{sens}/j\omega M_{sens}$. The PCB was mounted in the Bersier setup of Fig. 2, with the oscillator near side A. The external power was also provided from side A. The CM current was determined by measuring the voltage V (Fig. 2) at end C with an HP 4396A spectrum analyzer. The resolution and video bandwidth (RBW and VBW) of the analyzer were both 30 kHz and the maximum frequency span was 100 kHz – 1.82 GHz.

In the TL model the devices were simplified/linearized according to an IBIS (Input/output Buffer Information System) model. The output impedances (Z_g in Fig. 3) of the Thévenin equivalent models for the oscillator and translator were 20 and 12 Ω, respectively. The rise and fall times of the voltage source (V_g in Fig. 3) were measured separately, about 2 ns for HCT and 1 ns for HLL logic. For the far end impedances on the boards (Z_C's in Fig. 3) we assumed the input capacitances $C_i = 3.5$ pF for both logic types. The minor nonlinearity of the capacitance due to the Miller effect inside the IC's, was neglected.

In order to assess the current transfer, we first assumed a voltage source $V_g = 1$ at the oscillator, and

Table 1: Mean and maximum deviation between measured and calculated harmonics of f_0 in the CM current for HCT and HLL boards; f_m indicates the frequency where the maximum deviation occurs. The frequency range considered was 10 MHz – 600 MHz.

f_0 [MHz]	HCT			HLL		
	mean [dB]	max. [dB]	f_m [MHz]	mean [dB]	max. [dB]	f_m [MHz]
10	5.5	18.3	400	5.5	16.8	350
20	5.4	17.4	580	4.5	16.5	480
50	6.6	15.1	350	7.0	18.6	400
100	-	-	-	4.9	9.8	400

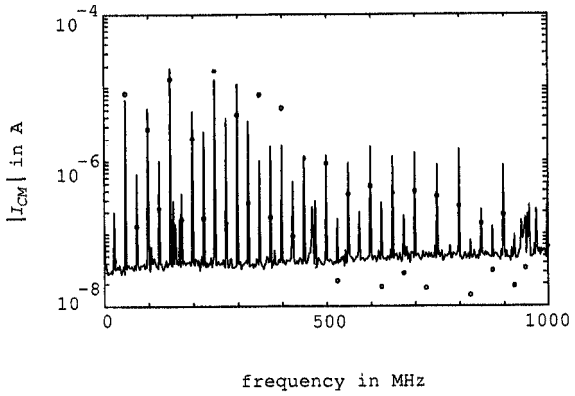

Fig. 7: Measured (—) and calculated (o) spectral component of the common-mode current I_{CM} in the Bersier setup for the HCT board with 50 MHz clock speed.

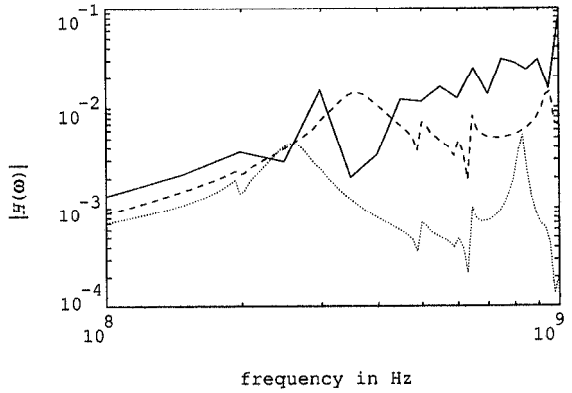

Fig. 8: Measured transfer function $H(\omega)$ for the harmonic components of the HCT board with 50 MHz oscillator (—) and the calculated $H(\omega)$ for a gap capacitance (see Section 5) $C_g = 0$ pF (- - -) and $C_g = 10$ pF ($\cdots$).

calculated the resulting DM current $I_{DM,s}$ seen by the current sensor s for a large number of frequencies. Knowledge of I_{DM} at one place suffices, since both forward and backward waves are taken into account in the linearized TL model. We then determined the transfer function $H(\omega) = I_{CM}/I_{DM,s}$ from the TL model and calculated the I_{CM} through the 150 Ω load from the measured $I_{DM,s}$ with the devices operating.

As an example, Fig. 7 shows the spectrum of I_{CM} for the HCT board with a 50 MHz clock. The measured current transfer $|H(\omega)|$ for the same clock speed (—) and the calculated transfer function (- - -) are given in Fig. 8. Table 1 shows the average deviation in dB between the measured and calculated I_{CM}, as well as the maximum deviation which occurred near f_m. The frequencies considered ranged between 10 MHz – 600 MHz. The branches in the HCT board clearly reduce the amplitude of the resonances in the current transfer, as is apparent when the $H(\omega)$ of Fig. 8 is compared to the open-ended tracks in Fig. 4a. The measured I_{CM} reaches values well over the 3 μA limit [17]. Without additional EMC measures this PCB proper does not comply with EMC regulations.

Measurements and calculations agree within 7 dB on the average. The maximum deviation, up to about 19 dB, is restricted to one or a few spectral components near the frequency f_m mentioned in the Table. We compared the experimental transfer functions for one type of logic (HCT) but with different clock frequencies. Large and abrupt variations in the measured $|H(\omega)|$ between subsequent harmonics were found near f_m as in Fig. 8, also at the lowest clock frequency. The calculated $H(\omega)$ were of course identical, since the electronics remained essentially the same; this $|H(\omega)|$ also showed smaller resonances above f_m. Where these resonances occurred, depended on many parameters, primarily on the difference in propagation speed in the DM and the CM circuit, and on the termination of the DM circuit. The actual values of the inductive and capacitive DM-CM coupling coefficients of the tracks were less decisive.

Since the FF's act as dividers, subharmonics are also present in the measured CM current. The calculated subharmonic amplitudes in I_{CM} are always lower than those measured. The local coupling at the IC sockets is probably more important than the contribution from the signal tracks. This coupling is not included yet in the TL model based on the tracks. For a passive component, a local off-diagonal capacitance and a mutual inductance could be selected. Each active device will act as a local series voltage source, and a parallel current source with respect to the CM circuit. Because of careful placement of the

decoupling capacitors, the contribution of the supply tracks can be neglected.

5. Concluding remarks

The proposed TL method estimates the equivalent sources for the common-mode current on a cable connected to a PCB quite well. For complicated tracks and an $\ell = 20$ cm long board the TL method starts to deviate above approx. 400-500 MHz. For digital circuits, the first few harmonics dominate the spectrum above 30 MHz, for which the current-injection or Bersier method is applicable. At these frequencies, the TL method is particularly accurate.

Resonance frequencies in the CM circuit are difficult to calculate correctly because of parasitic elements of tracks, components and ground plane. For instance the width of the gap in which the 100Ω CM series resistor (see Fig. 2) is placed, turned out to be important; a gap of 1 cm is a good choice. Smaller gaps resulted in an appreciable capacitance C_g parallel to the 100 Ω. This capacitance increased the quality factor Q of the CM resonances and lowered the part of I_{CM} seen by the measuring equipment. For instance, in Fig. 8 we presented the calculated current transfer for the HCT board with a 1 cm wide gap ($C_g = 0$ pF, curve (- - -)) and a 0.5 mm wide gap ($C_g = 10$ pF curve (· · ·)). If a harmonic of the digital circuits nearly coincides with a high-Q resonance, the calculated I_{CM} may largely deviate from measurements. This is true for any method.

In practical PCB's the DM resonances are often damped e.g. by a series or parallel resistor at the HLL logic inputs.

We used the measured I_{DM} in our TL model. One might prefer to also calculate the DM currents. However, in practice devices may be available earlier than the required IBIS models. In addition, interference sources which reside inside the devices such as processors, are not always presented in data sheets or files. One then has to resort to measurements [7].

We expect that the TL method can be extended to even higher frequencies when three-dimensional effects are addressed more accurately: local coupling at the devices and the fringing fields at the border of the PCB. In principle the immunity of a PCB with respect to interferences can also be determined by the TL method. The non-linearity of the devices should then be adequately known.

It would be worthwhile to investigate whether an approach similar to our TL model can also be found for an active device proper, as discussed at the end of the Section 4. This will certainly be necessary for densely packed PCB's, where the devices may contribute substantially.

References

[1] H. W. Ott, "Controlling EMI by proper wiring board layout," in *Proc. 6th Int. Symp. Electromagn. Compat.*, Zürich, Switzerland, 1985, pp. 127-132.

[2] C. R. Paul, "A comparison of the contributions of common- mode and differential-mode currents in radiated emissions," *IEEE Trans. Electromagn. Compat.*, vol. 31, no. 2, pp. 189-193, May 1989.

[3] S. Öing, W. John, and F. Sabath, "Computation of common mode radiation due to asymmetric coupling on printed circuit boards," in *12th Int. Wroclaw Symp. Electromagn. Compat.*, Wroclaw, Poland, June 1994, pp. 554-558.

[4] E. Leroux, S. Caniggia, F. Canavero, and B. Demoulin, "Evaluation of radiated emissions from printed circuit boards and cables at post-layout level," in *Proc. EMC'96 Roma*, Rome, Italy, Sept. 1996, pp. 662-667.

[5] D. M. Hockanson, J. L. Drewniak, T. H. Hubing, T. P. Van Doren, F. Sha, and M. J. Wilhelm, "Investigation of fundamental EMI source mechanisms driving common-mode radiation from printed circuit boards with attached cables", *IEEE Trans. Electromagn. Compat.*, vol. 38, pp. 557-566, Nov. 1996.

[6] R. Bersier and B. Szentkuti, "Rationale and new experimental evidence on the adequacy of conducted instead of radiated susceptibility tests," in *Proc. 5th Int. Symp. Electromagn. Compat.*, Zürich, Switzerland, 1983, pp. 257-262.

[7] J.R. Bergervoet, G. Maas, and M.J.C.M. van Doorn, "The common-mode skeleton model for assessment of electromagnetic compatibility at the system level," in *Proc. 12th Int. Symp. EMC*, Zürich, Switzerland, Feb. 1997, pp. 657-462.

[8] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Trans. Microwave Theory Tech.*, vol. 22, no. 3, pp. 216-221, March 1974.

[9] R. du Cloux, G.P.J.F.M. Maas, and A.J.H. Wachters, "Quasi-static boundary element method for electromagnetic simulation of PCBS," *Philips J. Res.*, vol. 48, no's 1-2, pp. 117-44, Jan. 1994.

[10] F.B.M. van Horck, A.P.J. van Deursen, and P.C.T. van der Laan, "Coupling effects on a multilayer printed circuit board," in *Proc. EMC'96 Roma*, Rome, Italy, Sept. 1996, pp. 596-601.

[11] F.B.M. van Horck, *Electromagnetic Compatibility and Printed Circuit Boards*, Ph. D. thesis Eindhoven University of Technology (EUT), 1998. This thesis encompasses two EUT earlier reports no's 96-E-300 and 97-E-305.

[12] F.B.M. van Horck, A.P.J. van Deursen, and P.C.T. van der Laan, "High-frequency crosstalk on a multilayer printed circuit board," in *Proc. EMC'98 Roma*, Rome, Italy, Sept. 1998, pp. 13-18.

[13] K.C. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip Lines and Slotlines*. 2nd ed., Norwood: Artech, 1996.

[14] E.F. Kuester and D.C. Chang, "Closed-form expressions for the current or charge distribution on parallel strips or microstrip," *IEEE Trans. Microwave Theory Tech.*, vol. 28, no. 3, pp. 254-259, March 1980.

[15] A.R. Djordjević, T.K. Sarkar, and R.F. Harrington, "Time-domain response of multiconductor transmission lines," *Proc. IEEE*, vol. 75, no. 6, pp. 743-764, June 1987.

[16] A.R. Djordjević and T.K. Sarkar, "Analysis of time response of lossy multiconductor transmission line networks," *IEEE Trans. Microwave Theory Tech.*, vol. 35, no. 10, pp. 898-907, Oct. 1987.

[17] J. Goedbloed, *Electromagnetic Compatibility*, London: Prentice Hall, 1992.