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# Citation for published version (APA):

Kwaspen, J. J. M., Lepsa, M. I., Roer, van de, T. G., Heyker, H. C., & Kaufmann, L. M. F. (1998). Accurate equivalent-network modelling of GaAs/AIAs based resonant tunnelling diode with symmetric thin barrier and spacer layers. In STW's SAFE 98 Workshop on Semiconductor Advances for Future Electronics (pp. 339-342)

Document status and date: Published: 01/01/1998

### Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

### Please check the document version of this publication:

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# Accurate Equivalent-Network Modelling of GaAs/AlAs Based Resonant Tunnelling Diodes with Symmetric Thin Barrier and Spacer Layers

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Abstract—On stable non-oscillating GaAs/AlAs based resonant tunnelling diodes with thin barriers, small-signal intrinsic impedances were measured at 21  $^{\circ}$ C in the full bias/frequency space (0-2V; 0.05-40.05 GHz). Equivalent-network optimisations for CAD, show that the classical Esaki model needs an extra degree of freedom for matching the measured intrinsic impedance throughout the whole active region. A very good impedance description in the entire bias/frequency space is obtained with four, frequency-independent intrinsic elements in the Quantum-Inductance model. Quasibound-state lifetime information and resistive cutoff-frequency, both against bias-voltage are shown.

*Keywords*— **Resonant tunnelling diodes, equivalent**network modelling, compound semiconductors

# I. INTRODUCTION

With the accent on accuracy and full bias-voltage/microwave frequency range coverage (0-2V; 0.05-40.05 GHz), the classical Esaki and the Quantum Inductance (QI) equivalent-network models [1,2,3] are used here to describe the measured small-signal intrinsic impedance  $Z_d$ of our Double Barrier Resonant Tunnelling diodes (RTDs) for CAD purposes. The GaAs/AlAs based, MBE-grown devices have a 5 nm quantum well and symmetric thin barrier and spacer layers, each nominal 2.5 nm thick (Fig. 1).

The RTDs are of planar type, with coplanar microwave probe access from the network analyser to the metallised signal (SIG) and ground (GND) pads on the semiinsulating substrate (Fig. 2a). The DC I-V curve and the microwave reflection coefficient  $S_{11}$  of the extrinsic RTD, and  $S_{11}$  of an OPEN and a SHORT reference structure are measured at the reference planes (pads) indicated. The



Fig. 1. RTD layer structure grown by molecular beam epitaxy (MBE); mesa definition by wet chemical etching; metallisation by lift-off technique; ohmic contacts Ge/Ni/Au; interconnections Ti/Pt/Au; isolation mesa-edge by SiO<sub>2</sub> or airbridge.

SHORT ( $Z_d = 0$ ) and OPEN ( $Z_d \Rightarrow \infty$ ) structures on the wafer (Fig. 2b,c) enable us to model the bias-voltage independent extrinsic elements of the equivalent-circuits:  $C_{ex}$ ,  $R_{ex}$  and  $L_{ex}$  (Fig. 3), describing the microwave behaviour of the Ti/Pt/Au pads-to-mesa interconnections [6,7]. Only  $R_{ex}$  is frequency-dependent due to skin losses in the metallisation.

# II. STABILITY CONDITIONS AND MEASUREMENTS

Accurate determination of the actual intrinsic elements  $R_d$  (dynamic device resistance),  $C_d$  (dynamic device capacitance),  $L_q$  (quantum inductance) and  $R_s$  (series resistance), makes a stable, non-oscillating RTD in the negative differential resistance (NDR) region a prerequisite. A stable RTD has at least no chair-like plateaus in the NDR region of its I-V curve, so the conductance  $G_d(= 1/R_d)$  has only one negative peak there (Fig. 4a,b). By proper

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Fig. 2. (a) Planar RTD with coplanar probe access. (b) SHORTreference structure  $(Z_d = 0)$  (c) OPEN-reference structure  $(Z_d \Rightarrow \infty)$ 



Fig. 3. Equivalent-circuit models of extrinsic RTD, consisting of interconnection elements Cex, Rex, Lex (pads-tomesa), and intrinsic RTD equivalent-circuits: Esaki-model and Quantum Inductance (QI)-model. Also shown are the SHORT and OPEN reference structures.

choice of the device area (20  $\mu$ m<sup>2</sup>; to make  $R_d + R_s + R_{ex}$ more negative than -50  $\Omega$  at the steepest slope in the NDR region, which gives a finite  $S_{11}$ ) and a specially designed bias circuit, the stability condition was met in our experiments.



Fig. 4. (a) DC I-V curve of extrinsic RTD, measured at 21 °C (on-wafer reference plane). (b) Differential conductance Gd [mS].

An array of  $S_{11}$ -data was collected in the 0 to +2 V range of the I-V curve (mesa top is +V), where  $S_{11}$  of the extrinsic RTD was measured at 75 bias points and from 0.05 - 40.05 GHz (401 points), after network analyser calibration with on-wafer standards. Fig. 5 shows some of these  $S_{11}$ 's in a compressed Smith chart, amongst them  $S_{11}$  in the smallest-NDR point ( $V_d = 1.0060V$ ;  $|S_{11}| \sim$ 3.9). The prober-chuck temperature was 21 °C.

## III. ESAKI AND MODIFIED ESAKI MODELS

Note that in a substantial range of NDR-region biasvoltages, the  $S_{11}$  curves show an inflection point, a feature that cannot be modeled by the Esaki equivalentcircuit with three, frequency-independent intrinsic elements (Fig. 3). Optimisation of these intrinsic parameters to carefully match the measured  $S_{11}$ -data (at each bias point), leads to the conclusion that the Esaki-model needs an extra degree of freedom to fit the measured  $S_{11}$  data array in the NDR region sufficiently accurate. Fig. 6a displays the real and imaginary parts of the intrinsic impedance  $Z_d$  at  $V_d = 1.0060$  V (largest negative  $G_d$ ), and Fig. 6b shows the dynamic conductance  $G_d$  and capacitance  $C_d$ , when these elements are taken frequencydependent (in accordance with [4]) to match the measured  $S_{11}$ . The mathematical equations that describe  $G_d$  and  $C_d$ as a function of frequency in the modified Esaki-model are also bias-dependent, which complicates CAD use.



Fig. 5. Measured  $S_{11}$  of SHORT-reference  $(Z_d = 0)$  and measured  $S_{11}$  of extrinsic RTD at several bias-voltages  $V_d$ , plotted in a compressed Smith chart (full scale= 4.0). Tchuck=21 °C.



Fig. 6. (a) Real and imaginary parts of measured intrinsic RTD impedance  $Z_d$ , at steepest slope of NDR region (1.0060V). (b) Frequency-dependence of optimized dynamic elements  $C_d$  and  $G_d$  of modified Esaki-model (1.0060V).



Fig. 7. Optimized intrinsic RTD elements Quantum Inductance (QI) model. Dynamic elements against bias-voltage, 75 points.

### IV. QUANTUM INDUCTANCE MODEL

The same measured small-signal  $S_{11}$  datasets can be described 'perfectly' by the Quantum Inductance circuit model (Fig. 3) over the full bias-voltage (0-2 V) and frequency ranges (0.05-40.05 GHz) with four, frequencyindependent intrinsic elements (Fig. 7a-d). The measurement of  $S_{11}$  on the stable RTD throughout the entire NDR region without hiatus, results in the correct determination of a time constant  $\tau$ , here defined as  $\tau = L_a/R_d (=$  $L_a \cdot G_d$ ) which, according to several authors [1,2], should be an indication of the quasibound-state lifetime in the quantum well. The display of this parameter  $\tau$  (Fig. 7e) and of  $L_q$  continuously over the whole undistorted NDR region is a novelty. Near the point where  $G_d$  has zero conductance (at the peak and valley voltages), the values of  $\tau$  are less reliable.  $\tau$  is not defined where  $G_d = 0$ . The peak value of  $\tau$  corresponds with the negative  $G_d$ peak (same bias). The calculated quasibound ground-state lifetime  $\tau_1$  given in [5] of ~ 50 ps for an AlAs barrier thickness of 2.547 nm and  $\sim$  18 ps for 2.264 nm (a decrease of 1 monolayer), compares well with the time constant  $\tau = 22$  ps measured. Fig. 7f shows the resistive cutoff frequency  $f_r$  against bias-voltage of the intrinsic RTD. In the passive regions of the I-V curve, the QI-model reduces to the Esaki-model, since the element-optimisation process finds there low values of  $L_q$ . For CAD purposes, a very good RTD intrinsic impedance description in the entire bias/frequency space (0-2V; 0.05-40.05 GHz) is obtained with four frequency-independent intrinsic elements, scalable with device area.

### REFERENCES

- E.R. Brown, et al, Appl. Phys. Lett., Vol. 54, (10), March 1989, pp. 934-936.
- [2] O. Vanbesien, et al, Microwave and Opt. Techn. Lett., Vol. 5, (8), 1992, pp. 351-354.
- [3] H.J.M.F. Noteborn, Ph. D.-thesis, Eindhoven University of Technology, Netherlands, May 1993.
- [4] J. Genoe, Ph. D.-thesis, Catholic University of Leuven, Belgium, 1994.
- [5] H. Brugger, et al, Proc. 18th Int. Symp. GaAs and Related Compounds, Seattle, Sept. 1991.
- [6] J.J.M. Kwaspen, et al, WOCSDICE'97, May 1997, Scheveningen, The Netherlands.
- [7] J.J.M. Kwaspen, et al, Electronics Letters, 1997, 33, (19), pp. 1657-1658.