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Energy recycling for a cost effective platform to optimize energy efficiency for low powered system

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Kapoor et al.

(54) **ENERGY RECYCLING FOR A COST EFFECTIVE PLATFORM TO OPTIMIZE ENERGY EFFICIENCY FOR LOW POWERED SYSTEM**

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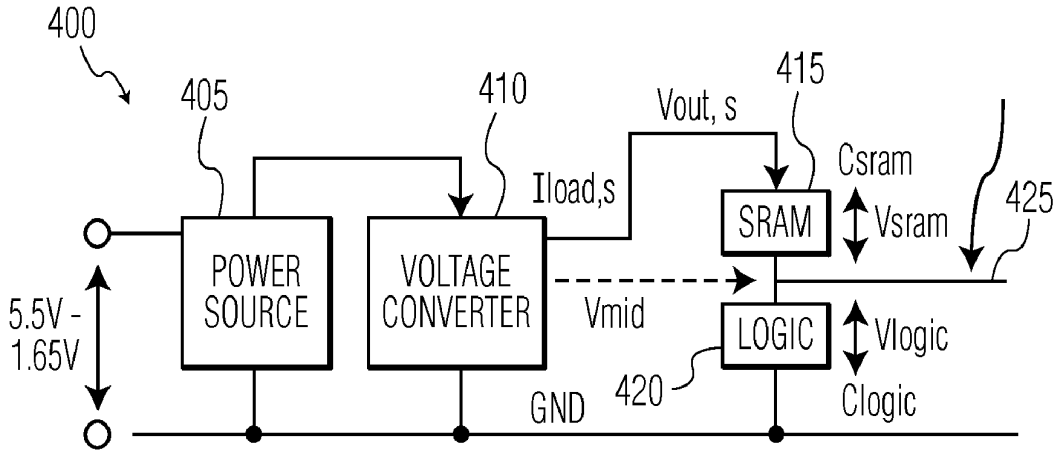
CPC ***G05F 1/46*** (2013.01)

(57) **ABSTRACT**

A system including: a voltage converter configured to convert a voltage from a power source to a different voltage; a memory coupled to the voltage converter; a digital logic circuit; and a level shifter coupled between the memory and digital logic circuit; wherein leakage current from the memory is stored in a capacitance in the digital logic circuit, wherein the voltage converter is further coupled to a node between the memory and digital logic circuit, and wherein the voltage converter is configured to: monitor a voltage at the node wherein the node has a desired operating voltage value; and adjust the voltage at the node when the voltage at the node varies from the desired operating voltage value.



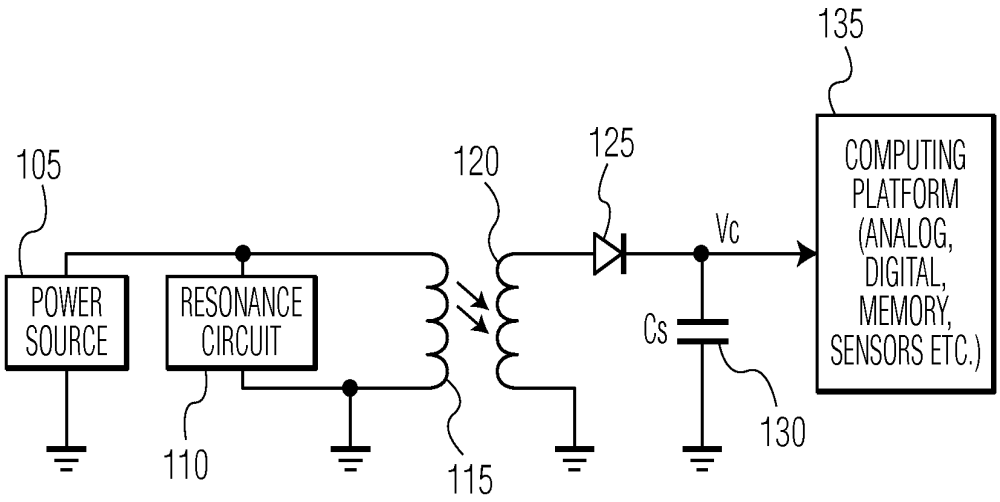

135
105
120
125
COMPUTING PLATFORM (ANALOG, DIGITAL, MEMORY, SENSORS ETC.)
Vc
POWER SOURCE
RESONANCE CIRCUIT
Cs
110
115
130

FIG. 1

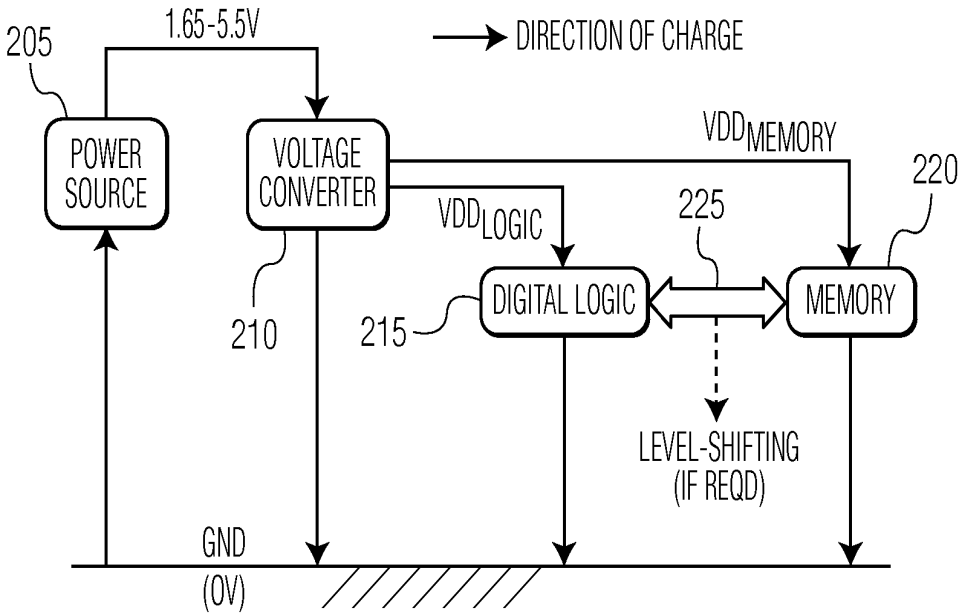

205
1.65-5.5V
DIRECTION OF CHARGE
POWER SOURCE
VOLTAGE CONVERTER
VDDMEMORY
220
VDDLOGIC
225
210
215
DIGITAL LOGIC
MEMORY
LEVEL-SHIFTING (IF REQD)
GND (0V)

FIG. 2

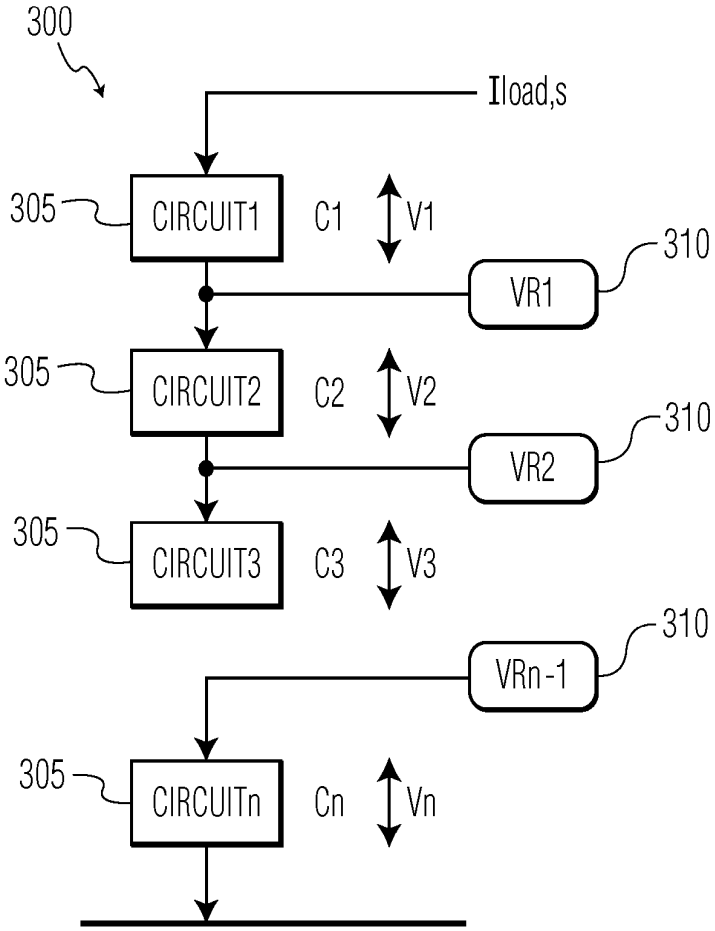

300
Iload,s
305
CIRCUIT1
C1
V1
310
VR1
305
CIRCUIT2
C2
V2
310
VR2
305
CIRCUIT3
C3
V3
310
VRn-1
305
CIRCUITn
Cn
Vn

FIG. 3

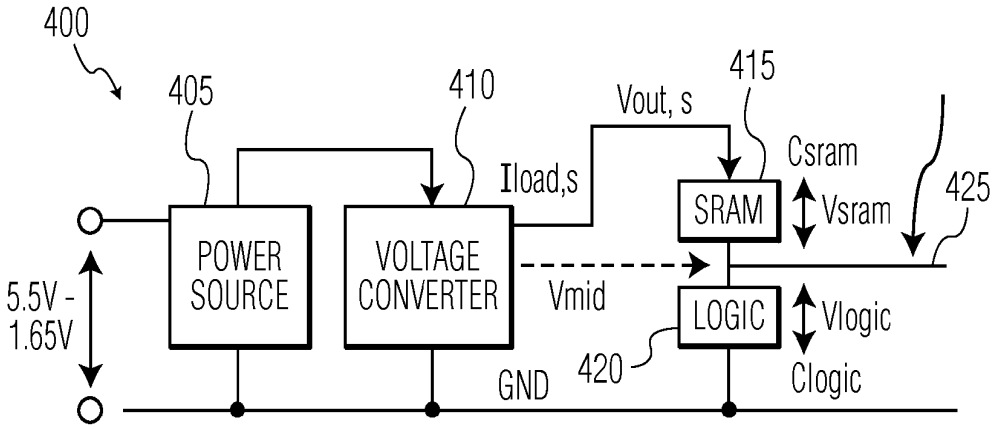

400
405
410
415
Vout, s
Csram
Iload,s
SRAM
Vsram
425
POWER SOURCE
VOLTAGE CONVERTER
Vmid
LOGIC
Vlogic
5.5V - 1.65V
GND
420
Clogic

FIG. 4

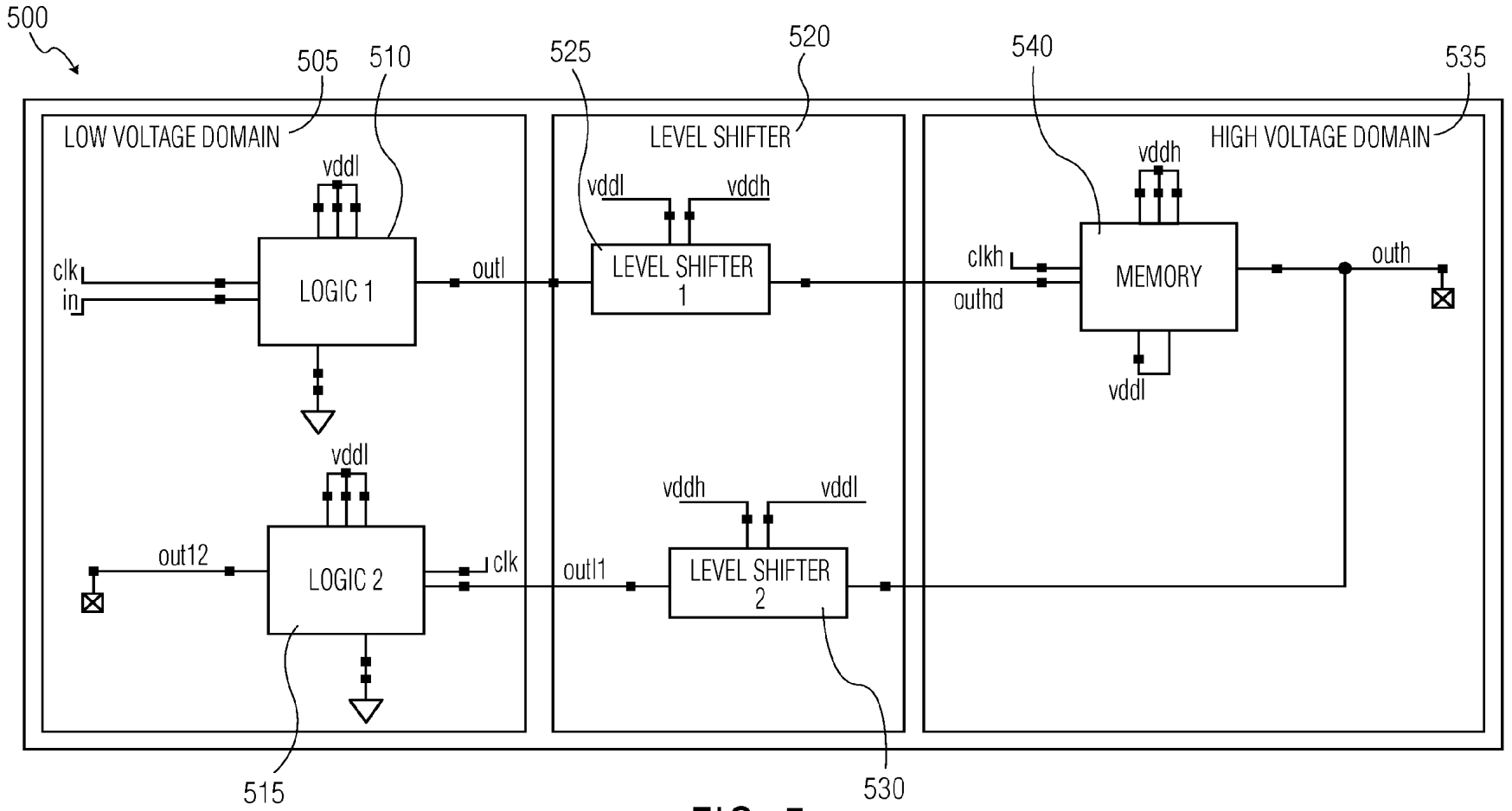

500
505
510
525
520
540
535
LOW VOLTAGE DOMAIN
LEVEL SHIFTER
HIGH VOLTAGE DOMAIN
vddl
vddl
vddh
vddh
clk
in
LOGIC 1
outl
LEVEL SHIFTER 1
clkh
outhd
MEMORY
outh
vddl
vddl
vddh
vddl
out12
LOGIC 2
clk
outl1
LEVEL SHIFTER 2
515
530

FIG. 5

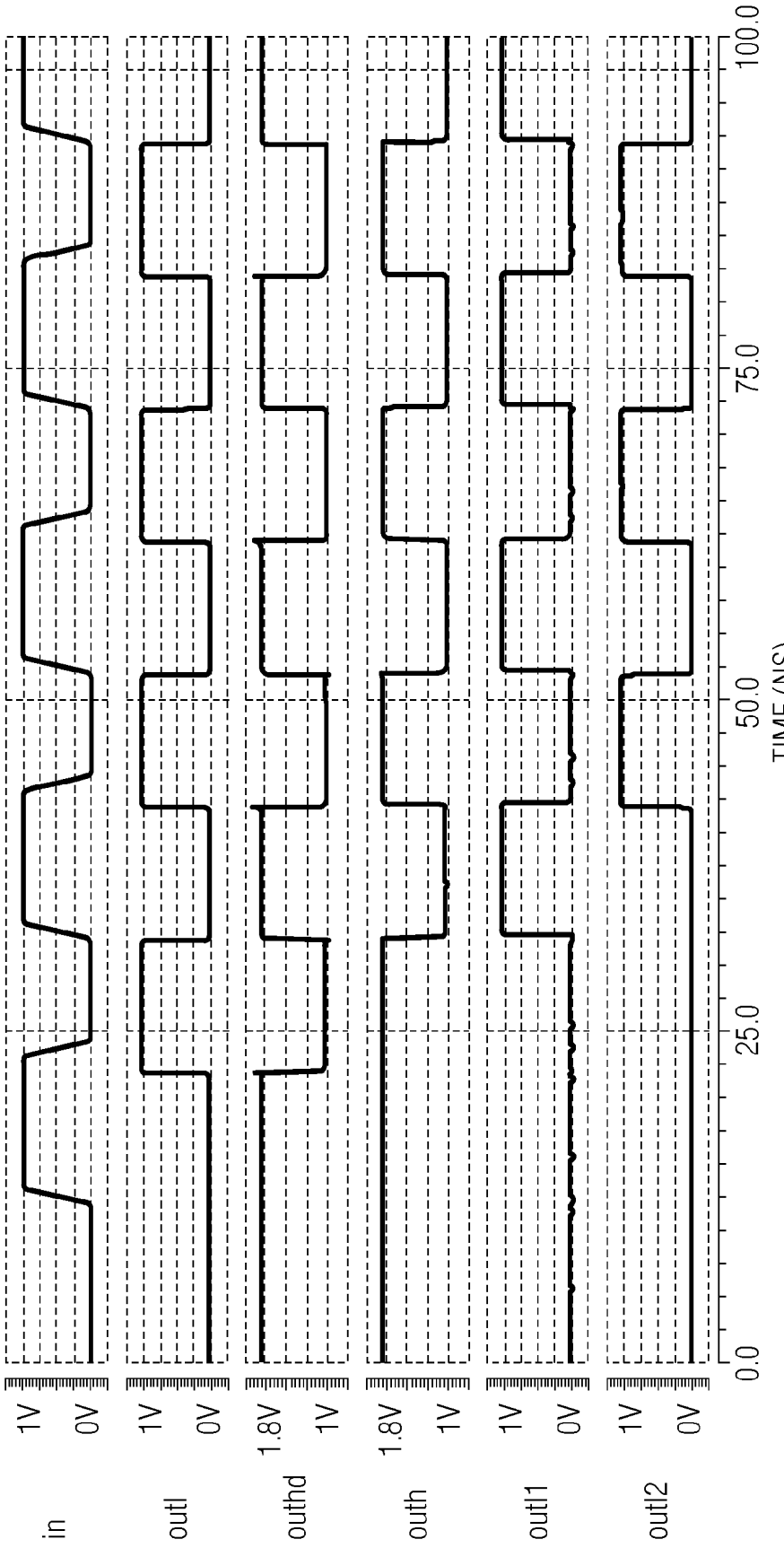

in
outl
outhd
outh
outl1
outl2
1V
0V
1.8V
0.0
25.0
50.0
75.0
100.0
TIME (NS)

FIG. 6

ENERGY RECYCLING FOR A COST EFFECTIVE PLATFORM TO OPTIMIZE ENERGY EFFICIENCY FOR LOW POWERED SYSTEM

TECHNICAL FIELD

[0001] Various exemplary embodiments disclosed herein relates generally to energy recycling for a cost-effective platform to optimize energy efficiency for low powered systems.

BACKGROUND

[0002] Low power design realization is a common challenge faced by various applications. With the advent of a new era of applications such as wireless energy based systems, Internet-of-things (IoT), etc., energy consumption of a design is becoming the most important specifications. This is in contrast to various somewhat traditional applications like computers, laptops, mobile phones etc. where power consumption was important but timing and area specifications were most important. It is also important to realize that often energy consumption in static modes, where leakage occurs, are equally or more important than dynamic energy consumption of a design. Moreover, these problems may be aggravated by the shrinking circuit technologies, where, leakages increase with each device and limited voltage scalability of memories. Given the limited energy budget various systems, there remains a need to explore new design techniques to maximize the energy utilization.

SUMMARY

[0003] A brief summary of various exemplary embodiments is presented below. Some simplifications and omissions may be made in the following summary, which is intended to highlight and introduce some aspects of the various exemplary embodiments, but not to limit the scope of the invention. Detailed descriptions of an exemplary embodiment adequate to allow those of ordinary skill in the art to make and use the inventive concepts will follow in later sections.

[0004] Various exemplary embodiments relate to a system including: a voltage converter configured to convert a voltage from a power source to a different voltage; a memory coupled to the voltage converter; a digital logic circuit; and a level shifter coupled between the memory and digital logic circuit; wherein the memory is coupled between the voltage converter and the digital logic circuit, wherein charge from the memory is stored in a capacitance in the digital logic circuit, wherein the voltage converter is further coupled to a node between the memory and digital logic circuit, and wherein the voltage converter is configured to: monitor a voltage at the node wherein the node has a desired operating voltage value; and adjust the voltage at the node when the voltage at the node varies from the desired operating voltage value.

[0005] Further, various exemplary embodiments relate to a method of powering a low power system including: converting an input DC voltage to an output voltage with a different level; applying the output voltage to a stack including a memory and a digital logic circuit wherein the memory is stacked on top of the digital logic circuit; level converting data signals between the memory and the digital logic circuit; storing a leakage current from the memory in a capacitance in the digital logic circuitry; monitoring a voltage at a node wherein the node has a desired operating voltage value; and adjusting the voltage at the node when the voltage at the node varies from the desired operating voltage value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] In order to better understand various exemplary embodiments, reference is made to the accompanying drawings, wherein:

[0007] FIG. **1** illustrates a generic system using magnetic coupling to transfer wireless energy;

[0008] FIG. **2** illustrates a low power system that may be powered using a power source;

[0009] FIG. **3** illustrates a stacked circuit system according to the related art;

[0010] FIG. **4** illustrates a system that implements a charge-recycling between memory and digital circuits;

[0011] FIG. **5** illustrates a system with a level shifter; and

[0012] FIG. **6** illustrates the various inputs and outputs associated with the level shifter of FIG. **5**.

[0013] To facilitate understanding, identical reference numerals have been used to designate elements having substantially the same or similar structure and/or substantially the same or similar function.

DETAILED DESCRIPTION

[0014] The description and drawings illustrate the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the principles of the invention and are included within its scope. Furthermore, all examples recited herein are principally intended expressly to be for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Additionally, the term, "or," as used herein, refers to a non-exclusive or (i.e., and/or), unless otherwise indicated (e.g., "or else" or "or in the alternative"). Also, the various embodiments described herein are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments. As used herein, the terms "context" and "context object" will be understood to be synonymous, unless otherwise indicated.

[0015] Wireless energy transfer was first envisioned by Nikola Tesla, but recent technological advancements have led to a renewed interest in this concept. In systems where wireless energy transfer is used, the power available is limited and needs to be used as efficiently as possible. As a result, systems powered by wireless energy transfer provide an example of a system that will benefit from the embodiments described below that provide increased energy utilization.

[0016] FIG. **1** illustrates a generic system using magnetic coupling to transfer wireless energy. The system **100** includes a power source **105**, a resonance circuit **110**, transmitter coils **115**, receiver coils **120**, a diode **125**, capacitor **130**, and a computing platform **135**. The basic principle of operation is that the transmitter coils **115** set up a magnetic field that induces current in the receiver coils **120** to charge the capacitor **130**. The power transmission part of the system include the power source **105**, resonance circuit **110**, and transmitting coils **115** to set up the electromagnetic field. The receiver portion of the system **100** is divided into a receiving coil **120**, a rectifying circuit **125**, and the capacitor **130** that acts as an

energy storage device. The received energy is stored on the capacitor **130** which may then power the elements on the computing platform **135**.

[0017] One main characteristic of the above described and similar systems is the non-static nature of energy availability from the energy source. Because of this, whenever possible, the wireless energy receiving system may capture the energy from the magnetic field and store it on the capacitor **130**. This stored energy allows the system to continue to operate even when there is no magnetic field. This need for energy storage leads to various design requirements for the system and especially the capacitor **130**. The size of the capacitor **130** is based on the energy consumption in the system. Often the capacitor **130** can take a significant area of the total silicon area of the system. It is also noted that the size of the capacitor **130** is strongly dependent on the amount of leakage current in the system. This leakage current consumes the charge stored on the capacitor **130** by the magnetic field.

[0018] Therefore, to limit the size of the capacitor **130** and its associated cost, it is very important to minimize the area of the capacitor **130**. This may be done by minimizing the charge consumption in the system, especially during the static mode of operation where leakage currents can deplete the charge on the capacitor. This goal of the embodiments described below.

[0019] In the wirelessly powered system like that shown in FIG. **1** above, which may be for example a contactless smart card, the system needs to remain powered up for certain time duration even in the absence of energy field. For this purpose, energy stored in a capacitor is used to supply the system energy, which in the case of contactless smart cards is mainly static leakage. However, the amount of capacitance required to supply this energy for the given duration gets prohibitively high and is a main contributor to the area of the design. This leads to high silicon costs for the system.

[0020] FIG.**2** illustrates a low power system that may be powered using a power source. The system **200** includes a power source **205**, voltage converter **210**, digital logic **215**, memory **220**, and level converter **225**. The power source **205** may provide a supply voltage of, for example, 1.65-5.5V. It is noted that the power source may be a battery or an energy storage capacitor. On the other hand, the digital logic **215** and memory **220** needs to operate at a minimum allowed supply voltage which is typically lower than the power source supply voltage. For example, the memory voltage may be 1V.

[0021] Accordingly, the power source **205** produces a higher voltage than the digital logic **215** and the memory **220** uses. Thus a voltage converter **210** is needed to convert the power source voltage to a voltage used by the digital logic **215** and the memory **220**. The voltage converter **215** takes up area and power. Low dropout regulators (LDOs) switching converters may be used for the voltage conversion. LDOs are simpler and smaller designs, but have lower efficiency of around 50-60%. Switching converters have a higher efficiency (>85%), but require more area and a more complex design. As a result many applications favor the use of an LDO, so the problem then becomes working with the lower efficiencies, but also less stringent constraints.

[0022] In the system topology illustrated in FIG. **2**, the digital logic **215** and memory **220** consume the charge from the power source **205** for their operation. The charge and current requirements are the summation of individual charge requirements of the digital logic **215** and the memory **220**. Also, the voltage converter **210** may have to produce two separate voltage levels, one for the digital logic **215** and one for the memory **220**. This leads to further inefficiency in the voltage converter **210**. Moreover, the security requirements on individual domains may require the placement of voltage sensors/monitors on logic and memory domains. This overhead of additional monitors often forces a designer to keep a single voltage domain for the logic and memory, thereby, reducing the energy efficiency of the design. Further, the current supplied by the power source **205** is the sum of the currents required by the digital logic **215** and the memory **220** that leads to increased conversion loss, because as current increases the a conduction and switching loss in the power converter **210** increases. Further, because the digital logic **215** and the memory **220** may operate at different voltage levels, level shifting may be required when the digital logic **215** communicates with the memory **220**.

[0023] One solution to improve the system efficiency is circuit stacking where the digital logic and memory are stacked or connected in series with the power converter. This has the effect of reducing the current supplied to the stack and increases the voltage supplied to the stack. This results in increase converter efficiency thus reducing the power source requirements.

[0024] Traditionally, circuit stacking techniques are deployed by decomposing the system design into multiple-stacks. The stacks may be so-designed such that there is almost equal activity between different stack-levels. This ensures that the charge from one level is completely balanced by the requirement on the other level. The mismatch in the activities can be compensated using various techniques described below. However, the charge recycling usage is limited by the activity balancing and switching timing synchronization between different levels. This charge recycling during the dynamic phase dictates the design strategy and often makes systems very complicated.

[0025] FIG. **3** illustrates a stacked circuit system according to the related art. The system **300** includes N stacked circuits **305** and N−1 voltage regulators **310**. The N stacked circuits **305** are connected in series and receive a supply current $I_{load,s}$. Further, there is a voltage drop V_n across each stacked circuit. Accordingly a power supply may supply a voltage of $V_1+V_2+\ldots V_N$ to the stacked circuits **305**. As discussed above one of the challenges is balancing the charge across the circuits as the different circuits operation varies relative to one another. This causes the voltage levels between the various stacked circuits **305** to vary. The voltage regulators **310** regulate this voltage to compensate for charge imbalances between the stacked circuits **305**. This solution adds cost and complexity to the design. This is especially undesirable in low power and low cost applications.

[0026] Two other solutions to charge balancing have been proposed in the related art. The first is using a software solution where a compiler and run-time scheduler are used to balance the operation of the stacked circuits **305**. The second is clock throttling, where the clock speed of each stacked circuit **305** is adapted in order to adjust the current and power draw of each stacked circuit **305**. Both of these solutions add cost and complexity. Further they still result in charge imbalances between the stacked circuits **305**.

[0027] The embodiments of the invention described below decompose the system such that: charge recycling is dictated by the leakage mode, thereby, reducing the limitations of the traditional circuit stacking; decomposition of memory and logic such that logic can operate at minimally required voltage; voltage-sensors/monitors for only one domain to reduce

the overhead on secure system, thereby, allowing the separate voltage domains for logic and memory. These features may lower the overall design costs and may make the system economically feasible.

[0028] To understand the embodiments described herein, it is important to realize that in a battery/capacitor operated design energy is consumed in the form of electrical charge moving from one place to another, e.g. between the terminals of the battery or the capacitor. The entities that drive the movement or this charge are mostly digital circuits that typically may include digital logic circuits and memories (e.g., RAM/ROM). Based on above observations with respect to decomposing the system, the charge-recycling between various parts of a digital circuitry may be implemented, such that same charge taken from the battery is reused for different tasks. This results in draining the battery at a slower pace than the conventional design techniques.

[0029] FIG. **4** illustrates a system that implements a charge-recycling between memory and digital circuits. The system **400** includes a power source **405**, voltage converter **410**, memory **415**, digital logic **420**, and a level shifter **425**. The power source **405** may be a battery, capacitor or any other power source used to power digital circuitry. The voltage converter **410** is a DC-DC converter that converts the voltage from the power source **405** to a voltage to be used to power the memory **415** and the digital logic **420**. The voltage converter may be any type of voltage converter, such as for example, an LDO or switching converter. The memory **415** includes the memory used by the system **400** and is shown as SRAM, but may be any type of memory needed by the system. The digital logic may include various types of digital circuitry including processors, signal processors, filters, multipliers, codecs, application specific integrated circuits (ASICs), clock generation unit, phase locked loops, other complimentary analog blocks, etc. used to carry out the functionality of the system **400**. The combination of the memory **415** and the digital logic **420** may be called the stack. The level shifter **425** connects the memory **415** to the digital logic **420** and allows for the communication between the memory **415** and the digital logic **420**. Because the memory **415** and the digital logic **420** are stacked, different voltage levels are used to implement the logic values in the memory **415** and the digital logic **420**. The level shifter **425** converts the digital signals between the memory **415** and the digital circuit **420** so that the digital information is correctly communicated. This will be further described below.

[0030] The operation of the system **400** will now be described including a method for balancing the charge between the memory **415** and the digital logic **420**. The power source **405** outputs a voltage and current to the power the memory **415** and the digital logic **420**. The voltage produced by power sources **405** is typically larger than the voltage used by the memory **415** and the digital logic **420**. For example, the voltage output of the power supply **405** may be in the range of about 1.65-5.5V, where the memory **415** and the digital logic **420** have operating voltages of <1.5 volts. The power source voltage may then be converted by the voltage converter **410** to the voltage required to drive the stack, which voltage is the combination of the voltage required to drive the memory **415** and the digital logic **420**.

[0031] The memory **415** is placed at the top of the stack, which means that the memory **415** receives the supply current first. Placing the memory **415** at the top of the stack has an advantage that the leakage current from the memory may be used to drive the digital logic circuit **420**. Memory cannot be turned off in order to preserve the stored data which results in a leakage current. This leakage current may be used to charge up a capacitance found in the digital logic **420**. Also, when the memory **415** requires more current than the digital logic **420**, excess charge may be stored in the digital logic **420**. This stored charge may then be used to power the digital logic **420**, when the memory **415** is idle. This results in a more balanced use of charge from the battery. Further, charge from the leakage current may be stored in the digital logic **420** to be used later, which reduces the overall draw on the power source **405**.

[0032] The leakage current charge from the memory **415** may be stored in a capacitance found in the digital logic. This capacitance may be the capacitance inherent in the various transistors and devices found in the digital logic **420**. Further, additional capacitance may be added to the digital logic **420** in order to increase the charge storage capacity. Also, additionally the leakage current may be stored in a capacitance in the voltage converter **410**.

[0033] Further, the voltage converter may be connected to the node between the memory **415** and the digital logic **420**. The voltage at this node should be kept at a desired voltage corresponding to the voltage drop across the memory **415** and the digital logic **420**. The voltage converter monitors the voltage of at this node to determine if it is deviating from its desired value. If so, the voltage converter **410** may supply or sink current as needed in order to maintain the node voltage at its desired value. This provides additional capability to balance the charge in addition to the storage of leakage current charge in the digital logic **420**.

[0034] FIG. **5** illustrates a system with a level shifter. FIG. **6** illustrates the various inputs and outputs associated with the level shifter of FIG. **5**. The system **500** includes a low voltage domain **505**, a level shifter **520**, and a high voltage domain **535**. The low voltage domain **505** has a voltage range of 0-1.0 V, with, for example, a voltage of 0 V indicating a logic 0 and a voltage of 1.0V indicating a logic 1. The high voltage domain **535** has a voltage range of 1.0-1.8 V, with, for example, a voltage of 1.0 V indicating a logic 0 and a voltage of 1.8 V indicating a logic 1. The level shifter **520** shifts signals between the low voltage domain **505** and the high voltage domain **535**. The low voltage domain **505** includes logic 1 **510** and logic 2 **515**. The level shifter **520** include level shifter 1 **525** and level shifter 2 **530**. The high voltage domain **535** includes memory **540**. The logic 1 circuit **510** receives an input voltage in that leads to an output voltage outl. Level shifter 1 **525** receives the voltage outl from the logic circuit 1 **510** and provides a shifted output voltage outhd. The memory **540** receives the voltage outhd and produces an output voltage outh. Level shifter 2 **530** receives the voltage outh and converts it to a voltage outl**1**. The logic 2 circuit **515** receives the voltage outl**1** and produces a voltage out l**2**. FIG. **6** shows various signals used in the system named in, outl, outhd, outh, outl**1**, and outl**2** as a function of voltage versus time. As the signal propagates between the low voltage domain **505** and the high voltage domain **535** via the level shifter **520**, the level of the signals are shifted to correspond to the correct level for the logic level in each domain.

[0035] The embodiments described herein provide various benefits. As discussed above, during a leakage mode, the leakage of the memory (which is usually larger than that of the digital logic) is used to supply charge to the digital logic. This charge may also be stored in a capacitor in the digital logic or voltage converter. This means that there will be less

charge drained from the battery. Stacking of the memory on top of the digital logic leads to a lower over all current draw from the voltage converter, but a higher output voltage from the voltage converter. This results in a higher efficiency in the voltage converter. For example, a voltage converter with a 65% voltage efficiency used to drive a memory and digital logic that are not stacked may increase to 85% when driving a stacked memory and digital logic.

[0036] Further, the system topology allows a single voltage-sensing between the two stack domains. This means that the voltage sensor overhead is reduced from the traditional approach of creating multiple supply voltages for each of the digital logic and memory. Also, the power management unit (PMU) overhead of creating separate power domain for logic and memory is also reduced.

[0037] It should be appreciated by those skilled in the art that any block diagrams herein represent conceptual views of illustrative circuitry embodying the principles of the invention. Further, in the circuits shown additional elements may also be included as needed, or variations to the structure of the circuit may be made to achieve the same functional results as the circuits illustrated.

[0038] Although the various exemplary embodiments have been described in detail with particular reference to certain exemplary aspects thereof, it should be understood that the invention is capable of other embodiments and its details are capable of modifications in various obvious respects. As is readily apparent to those skilled in the art, variations and modifications can be effected while remaining within the spirit and scope of the invention. Accordingly, the foregoing disclosure, description, and figures are for illustrative purposes only and do not in any way limit the invention, which is defined only by the claims.

What is claimed is:

1. A system comprising:

a voltage converter configured to convert a voltage from a power source to a different voltage;

a memory coupled to the voltage converter;

a digital logic circuit; and

a level shifter coupled between the memory and digital logic circuit;

wherein the memory is coupled between the voltage converter and the digital logic circuit,

wherein charge from the memory is stored in a capacitance in the digital logic circuit,

wherein the voltage converter is further coupled to a node between the memory and digital logic circuit, and

wherein the voltage converter is configured to:

monitor a voltage at the node wherein the node has a desired operating voltage value; and

adjust the voltage at the node when the voltage at the node varies from the desired operating voltage value.

2. The system of claim **1**, further comprising a capacitor in the digital logic circuit configured to store leakage current from the memory.

3. The system of claim **1**, further comprising a capacitor in the voltage regulator configured to store leakage current from the memory.

4. The circuit of claim **1**, wherein, the voltage converter is a linear dropout regulator.

5. The circuit of claim **1**, wherein, the voltage converter is a switching regulator.

6. The circuit of claim **1**, wherein, adjusting the voltage at the node includes the voltage converter supplying current to the node or sinking current from the node.

7. A method of powering a low power system comprising:

converting an input DC voltage to an output voltage with a different level;

applying the output voltage to a stack including a memory and a digital logic circuit wherein the memory is stacked on top of the digital logic circuit;

level converting data signals between the memory and the digital logic circuit;

storing a leakage current from the memory in a capacitance in the digital logic circuitry;

monitoring a voltage at a node wherein the node has a desired operating voltage value; and

adjusting the voltage at the node when the voltage at the node varies from the desired operating voltage value.

8. The method of claim **1**, further comprising storing leakage current in a capacitor in the digital logic circuit.

9. The system of method **1**, further comprising storing leakage current in a capacitor in the voltage regulator.

10. The method of claim **1**, wherein a linear dropout regulator performs the voltage conversion.

11. The method of claim **1**, wherein a switching regulator performs the voltage conversion.

12. The method of claim **1**, wherein, adjusting the voltage at the node includes supplying current to the node or sinking current from the node.

* * * * *