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# Apparatus and method for chip-scale package with capacitors as bumps

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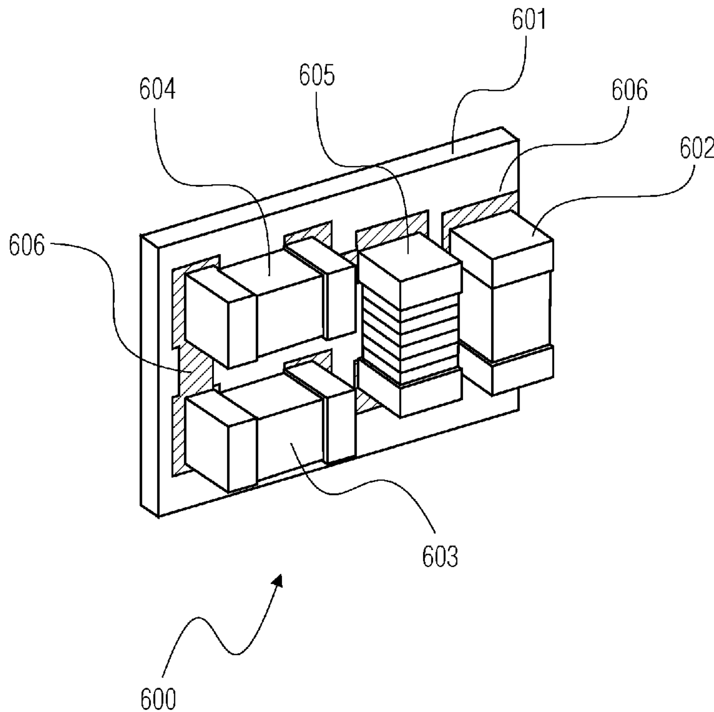


FIG. 6

**(57) Abstract:** A method and apparatus relating to chip-scale packaging is provided. According to an embodiment of the invention electrical solder bump interconnection between an integrated circuit package and a substrate is replaced by the placement and attachment of discrete SMD components between pads on the integrated circuit and substrate. Said substrate being for example a low-temperature co-fired ceramic such as alumina or a PCB such as FR4. Accordingly discrete SMD capacitors, inductors etc can be packaged with the system design goals of minimizing board real-estate, enhancing performance, and cost addressed in a novel manner without requiring substantial development of new processes by manufacturers. The embodiments of the invention minimizing the parasitic series impedance of decoupling capacitor connections for example whilst allowing a small-form-factor System-in-Package to be realized.

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# APPARATUS AND METHOD FOR CHIP-SCALE PACKAGE WITH CAPACITORS AS BUMPS

The invention relates to packaging semiconductor devices and more particularly to reducing the footprint and parasitics of such packages and their associated bulk external components, such as capacitors and inductors.

The electronics industry continues to rely upon advances in semiconductor technology to realize higher-function devices in more compact areas, and to reduce the operating voltage of these devices wherever possible in order to reduce power consumption. Over time many different semiconductor devices have been manufactured with various applications in numerous disciplines. Such semiconductor devices often include metal-oxide-semiconductor field-effect transistors (MOSFET), such as p-channel MOS (PMOS), n-channel MOS (NMOS) complementary MOS (CMOS) transistors, and CMOS with bipolar transistors, BiCMOS.

Concurrently with the drive for increased functional integration, there are similar drives for improved speed of the semiconductor devices, where they are digital devices, and improved noise, sensitivity, power and operating frequencies where they are analog devices such as within wireless and RF technology. In many instances of today's consumer electronics these digital, wireless and RF technologies are deployed simultaneously within portable and hand-held units. As a result today's semiconductor based devices typically include semiconductors based upon silicon, silicon germanium, and gallium arsenide material systems, and can simultaneously include devices exploiting many semiconductor building blocks for microprocessors, digital memory, input and output interfaces, wireless transceivers etc.

Accordingly it is not uncommon for system and sub-system designers therefore to generate designs requiring multiple supply voltages with varying magnitude, such as 1V, 1.5V. 2.5V, 3V and 5V. Additionally specific supply voltages may be replicated as there are specific requirements for voltage tolerance, stability, noise etc. As a result the number of supply voltages that need to be derived from the single battery voltage for various system parts in todays high volume, low cost portable electronic devices has increased dramatically over the years. Further as consumers demand extended operational and

stand-by performance of these portable electronic devices, and manufacturers seek to exploit this as a marketing tool, then the derivation of these multiple supply voltages from the single battery voltage needs to be done in an efficient way. Several methods exist in the prior art for deriving one DC voltage from another DC voltage, but basically
5 these fall into two groups: time-continuous voltage converters or linear regulators and time-discrete voltage converters.

In a time-continuous converter, or linear regulator, a transistor is used as a dissipative element. Unfortunately this method only permits voltage down conversion, and the efficiency is limited to the ratio of output voltage and input voltage of the voltage
10 converter.

In a time-discrete converter a passive component, a capacitor or an inductor, is used as an energy-storage element. The energy-storage element being first connected to the input source to store energy, after which it is connected to the load to release the energy. The two main sub-types are capacitive converters and inductive converters,
15 depending on the type of passive component used to temporarily store the energy. For both types, up conversion as well as down conversion is possible.

Capacitive converters have the disadvantage that the ratio between output voltage and input voltage is determined by the topology and cannot be controlled easily, except by combining several switchable topologies in one circuit which severely adds to the
20 number of components, complexity and cost. As a result, the output voltage changes when the input voltage changes, which is not acceptable for most applications where a constant output voltage is required to maintain circuit operation as the battery drains and the voltage it provides reduces. Further, rather large capacitors are needed in order to keep the efficiency at an acceptable level.

25 Inductive converters have the advantage that adjusting the duty cycle at which the power switches, used to control the storage and release of energy in the inductor, may be controlled and adjusted provides for control the output voltage rather easily. Therefore, the output voltage, i.e. the supply voltage to a certain system block, can be kept constant when the input voltage, i.e. the battery voltage, varies. Relatively high efficiencies are
30 possible for relatively high output powers compared to capacitive converters.

A typical DC/DC converter uses power switches and control circuits implemented on an integrated circuit (IC) together with external inductors. A disadvantage of this approach is that with an increasing number of voltages to be generated in a system, the occupied PCB space increases dramatically as the external inductors themselves take up a lot of space. Therefore, integrating the inductor into the package would seem an attractive option. However, since the inductance of an integrated inductor is typically much lower than its external counterparts, the converter switching frequency must be increased correspondingly. Without proper decoupling of internal supply rails this will lead to many problems with internal supply bounce seriously degrading the converter performance.

In order to appreciate the consequences of this, it is necessary to review the basic operation of a DC/DC down converter 100. Continuous Conduction Mode and voltage-mode control have been assumed for simplicity, but similar comments hold for discontinuous conduction mode and/or current-mode control as well. Referring to Fig. 1 there is illustrated a circuit schematic of a typical DC/DC down converter 100 with an integrated inductor 101. The schematic comprises a control and switch drivers block 102, control switch 103, synchronization switch 104, decoupling capacitors 105 (Cref) and 106 (Cbuf), and filter output capacitor 107 (Cout) respectfully. Control switch 103 and synchronization switch 104 conduct consecutively, i.e. never at the same time. When control switch 103 conducts, the current through the integrated inductor ramps up linearly. Synchronization switch 104 starts conducting after control switch 103 is opened, after which the current ramps down linearly again towards the same starting value. Now synchronization switch 104 opens and control switch 103 starts conducting again, and the cycle repeats. When the switching period time is T and control switch 103 conducts during a time fraction DT, with duty cycle $0 \leq D \leq 1$, then naturally synchronization switch 104 conducts during a time fraction (1-D)T.

It can be shown that for the DC/DC down converter 100 illustrated in Fig. 1 that the voltage at node 108 (Vout) equals D times the voltage at node 109 (Vin). Since Vout=DVin, therefore, Vout<Vin., as $0 \leq D \leq 1$. As a result the duty cycle D may be controlled using a control loop, where the actual output voltage at node 108 is compared to the desired output voltage expressed by the reference voltage at node 110 (Vref). The

DC/DC down converter 100 would also work if synchronization switch 104 is replaced by a diode, but this would lead to a lower efficiency since the conduction losses in the diode would be larger than those in low-ohmic power switches such as control switch 103 and synchronization switch 104.

5 Referring to Fig. 2 illustrated are the basic voltage and current waveforms of a DC/DC down converter 100 as presented supra in respect of Fig 1. Because of the relatively high switching frequency and the small inductance value associated with integrated DC/DC converters steep dI/dt transients are drawn from the input supply node 109 (Vin), see current Iin as shown in Fig. 2. Therefore, referring to Fig. 1, a decoupling

10 capacitor 106 (Cbuf) needs to be placed between the internal input supply node 111 and the internal ground node 112 to sustain the internal supply voltage value. The external ground node is indicated as node 118. This decoupling capacitor should accommodate the AC part of the supply current Iin, whereas the DC part of Iin is drawn from the external input supply node 109.

15 In order to make this measure effective, the parasitic series impedance 116 and 117 of the connections of the decoupling capacitor 106 (Cbuf) needs to be minimal, because otherwise large voltage fluctuations will occur on both the internal supply and the internal ground node. This will seriously degrade the performance of the DC/DC down converter 100. Alternatively, drawing AC current peaks from the external circuit

20 environment is not an option since: a) the series impedance of the current path to the external circuit environment will always be too high leading to an unacceptable voltage dip during current transients, since e.g. pin impedance, possible bond wires and PCB tracks all add to this impedance; and b) this will lead to EMI problems since the area looped by the high-frequency current will become too large.

25 In addition to the need of a decoupling capacitor for the internal power supply, decoupling capacitor 105 is also needed for the reference input for the control block. Here a short low-impedance connection to the input of the control block is also needed to minimize any disturbance picked up from the switching power stage that would influence the control behaviour. In Fig. 1, the reference input is referred to a separate GND pin 113

30 to allow a clean ground to refer to.

Finally, an LC output filter is provided by integrated inductor 101 and filter output capacitor 107 used in the DC/DC down converter 100. This LC output filter removing essentially all AC content of the voltage at node 114 (VLX) between the control switch 103 and synchronization switch 104 , leaving the DC part DVin at output node 116. Optionally the control and switch drivers block 102 can also be provided with a filtered clean supply. However this is not indicated in Fig. 1 for simplicity.

Referring to Fig, 2, the so-called current ripple □I will flow in and out of the buffer capacitor 107 (Cout). The current ripple in combination with the impedance of the capacitor (1/j□Cout) and its parasitic series impedance (Zout), indicated as 115 in Fig. 1, will determine the so-called voltage ripple on the output voltage (Vout) and output node 116. This voltage ripple needs to be kept at a minimum. Therefore, buffer capacitor 107 (Cout), should be chosen large enough, but its parasitic series impedance 115 (Zout) should be minimized.

As a result, a typical System-in-Package (SiP) containing the DC/DC down converter 100 explained above will contain an IC with the power switches, control and drive circuitry, an integrated inductor, and several capacitors.

Referring to Fig. 3 illustrated are prior art SiPs 300 based on Thin-Array-Plastic-Packaging (TAPP) technology that is similar to the Ultra-Thin Leadless Package (UTLP. The TAPP substrate is fabricated by plating up patterns on a copper-base substrate, which is later etched away. Wire bonding is applied for the IC (active die) and the die, passive components such as surface-mount device (SMD) capacitors and inductors are all placed in the same plane. It would evident that the majority of the footprint of the SiPs 300 is absorbed by the SMD devices 310 and not the surface mount ICs 320.

Fig. 4 illustrates a cross-sectional view of a prior art SiP 400 implemented using (TAPP) technology. Leads 401 and 402, screen print epoxy 403 and 404, embedded inductor 405, die attach pad 406, die attach epoxy 407, ground ring 408, passive components 409 and 410, die 411, bond wire loops 412 and molding compound 413 are depicted.

Fig. 5 illustrates an isometric exposed layer view of a prior art low-profile DC/DC converter 500 implemented using a Low-Temperature Co-fired Ceramic (LTCC) substrate with an embedded inductor. Here an integrated circuit (IC) 501 is shown

assembled with discrete capacitors 502, all of these being are placed in one nonmagnetic ferrite plane 503 stacked above interconnect layer 504 which provides the electrical interconnevtion and routing via internal connection pattern 505. Beneath interconnect layer 504 is a ferrite plate 506, which is used as part of the embedded inductor, which is
5 further completed by a winding or coil pattern 507.

Commercial SiPs for use in integrated DC/DC converters have the disadvantage that the connections between the decoupling capacitors, such as discrete capacitors 502, and the IC 501 are still relatively long. In the case of the TAPP SiPs, the passive components 405, for example capacitors are connected to the IC via bond wires 412,
10 which is very inefficient with respect to impedance, as it introduces a rather large inductance, of the order of several nanohenries, into the decoupling path thereby leading to a severe dip in the internal supply voltage, V=L dI/dt across the parasitic series inductance wherein both L and dI/dt are high, followed by damped ringing caused by the series LC oscillation of the internal supply network.

15 In contast SiPs implemented using LTCC substrates have capacitors that are connected to the die via tracks on the LTCC substrate. Although the die is flip-chipped on the substrate, the total series impedance still can become substantial, since the connections need to have a length determined by the requirement to route all connections to and from the IC, a length further determined by the minimum spacing design rules of
20 the LTCC substrate.

It would be advantageous therefore to provide a DC/DC converter with integrated inductor and decoupling capacitors allowing both a small-form-factor and reduced parasitic series impedance. It would be further beneficial if the design approach was implementable at low cost.

25 In accordance with the invention there is provided an apparatus comprising an integrated circuit comprising at least one bonding pad of a plurality of bonding pads. The invention also comprising at least one passive component of a plurality of passive components, each of the plurality of passive components comprising at least an upper connection surface and a lower connection surface electrically connected together, and a
30 package substrate with a surface connection layer comprising at least one landing pad of a plurality of landing pads, wherein the upper connection surface of the at least one

passive component is electrically connected to the least one bonding pad of the plurality of bonding pads and the lower connection surface of the at least one passive component is electrically connected to the least one landing pad of the plurality of landing pads.

In accordance with another embodiment of the invention there is provided a method comprising providing an integrated circuit comprising at least one bonding pad of a plurality of bonding pads, and providing at least one passive component of a plurality of passive components, each of the plurality of passive components comprising at least an upper connection surface and a lower connection surface electrically connected together. The invention further comprising providing a package substrate with a surface connection layer comprising at least one landing pad of a plurality of landing pads, coupling the upper connection surface of the at least one passive component to the least one bonding pad of the plurality of bonding pads thereby forming an electrical interconnection between them, and coupling the lower connection surface of the at least one passive component to the least one landing pad of the plurality of landing pads thereby forming an electrical interconnection between them.

Fig. 1 illustrates a prior art circuit schematic of a typical DC/DC down converter with an integrated inductor.

Fig. 2 illustrates the basic voltage and current waveforms of the prior art DC/DC down converter circuit schematic depicted in Fig. 1

Fig. 3 illustrates several prior art System-in-Package (SiP) based on Thin-Array-Plastic-Packaging (TAPP) technology.

Fig. 4 illustrates a cross-sectional view of a prior art SiP implemented using TAPP technology.

Fig. 5 illustrates an isometric exposed layer view of a prior art low-profile DC/DC converter with an embedded inductor implemented using a Low-Temperature Co-fired Ceramic (LTCC) substrate.

Fig. 6 illustrates a perspective view of a DC/DC converter according to an embodiment of the present invention.

Fig. 7 illustrates a perspective view a DC/DC converter according to an embodiment of the present invention.

Fig. 8 illustrates a perspective view of an integrated DC/DC converter according to an embodiment of the present invention.

Fig. 9 shows a simplified flow diagram of a method to implement a circuit with reduced parasitic series impedance of the decoupling-capacitor connections in a small-form-factor SiP.

The present invention is now described with reference to the drawings. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It may be evident, however that the present invention may be practiced without these specific details.

Referring to Fig. 6, a perspective view of a DC/DC converter 600 assembled according to an embodiment of the invention is shown. The power switches, control and driver circuitry, etc such as described in respect of DC/DC down converter 100 supra in respect of Fig.1 are implemented in an integrated circuit 601 having a plurality of bond pads 606. Assembled to the bond pads 606 of the DC/DC converter 600 are decoupling capacitors 602 (Cref) and 603 (Cbuf), filter output capacitor 604 (Cout), and inductor 605.

SMD components, such as industry standard footprint capacitors 0201, 0402, 0603 etc according to design rules and capacitance required, are used for capacitors 602, 603 and 604. Discrete SMD inductors, to provide inductor 605, with very good quality for use in integrated DC/DC converters by virtue of providing a large L/R ratio in a useable frequency range of several MHz, are available from several sources and in several sizes (even as small as 0201), e.g. Coilcraft, Murata, etc. Obviously, other small-form-factor inductors can also be used to integrate the inductor.

Referring to Fig. 7, a perspective view of a DC/DC converter 700 according to an embodiment of the present invention is shown absent the SMD components on the underside of ultra-thin leadless package (UTLP) substrate 701. ULTP substrate 701 is depicted with surface connection layer 702 comprising bond pads 703, 704, 705, 706, and 707. In this embodiment the DC/DC converter 700 is designed in accordance with the design of DC/DC down converter 100 supra. Accordingly bond pad 703 is coupled to ground (power), bond pad 704 is coupled to Vin, bond pad 705 is coupled to Vref, bond pad 706 is coupled to ground (clean) and bond pad 707 is coupled to Vout.

Alternatively, bond pads 703, 704, 705, 706, and 707 are through-connected to the bottom of substrate 701 to corresponding pins or solder balls (BGA). These corresponding pins or solder balls are coupled to ground (power), Vin, Vref, ground (clean), and Vout, respectively. Alternatively, other package substrates may be substituted for package substrate 701, for example, LTCC or other thin-film substrates, or even PCB materials such as FR4 material. The exact choice determined by performance and cost tradeoffs.

Referring to Fig. 8, a perspective view of an integrated DC/DC converter 800 according to an embodiment of the present invention. DC/DC converter 800 comprises an integrated circuit 810 with SMD passive components 802, as depicted in Fig. 6, coupled to the package substrate 803, as depicted in Fig. 7. Accordingly the decoupling capacitors and the filter output capacitor metallizations 802A and 802B replace conventional prior art solder bumps. By using the SMD capacitor metallizations as part of the electrical interconnection, the series impedance in all of the capacitor connections is reduced substantially as a result.

The total height of DC/DC converter 800 is comparable to the prior art solutions, such that the small form factor that is needed to make use of an integrated DC/DC converter feasible is not compromised. It would be apparent that the embodiments of the invention presented supra in respect of Figs. 6 through 9 provide for a very straight-forward implementation leveraging commercially available SMD components for low-cost implementations.

The total height of DC/DC converter 800 according to this embodiment is the combined height of the package substrate 803 plus the height of the SMD capacitors 802 and the height of the die of the integrated circuit 810. Since the die, typically comprising a silicon substrate, can be ground down to thicknesses of 200□m or even less, the total height is similar to that of the TAPP approach, where bondwire loops are significant portion of the total height, and that of the LTCC approach, having a typical thickness of 600□m. An 0201 series capacitor for example from AVX in their X5R range having a thickness of 330□m and providing capacitance values up to 0.1□F.

The invention is suitable for any integrated DC/DC converter, up or down converters and inductive, capacitive or even resonant converters. The important aspect is

that the converter needs integrated capacitors, which is the case for all time-discrete voltage converters.

Advantageously, the integrated DC/DC converter described above can be used in all applications where small form-factor integrated DC/DC converters are needed. These converters are becoming an increasingly important option to generate various system supply voltages from one battery voltage in mobile applications without an increase in PCB real estate normally associated with state-of-the-art DC/DC converters with external inductor and/or external capacitors.

Referring to Fig. 9, there is illustrated a flow diagram of a method to implement a circuit with reduced parasitic series impedance of the decoupling-capacitor connections in a small-form-factor System-in-Package (SiP).

An integrated circuit having bottom bond pads for receiving passive components, such as depicted in Fig. 6 is obtained at step 901. At least one passive component having upper and lower connection surfaces is obtained at step 902. Next a substrate having bond pads for receiving passive components as depicted in Fig. 7 is obtained at step 903. At step 904, the upper connection surface of the passive component is coupled to the bond pad for receiving passive components using solder or a conductive adhesive. The lower connection surface of the passive component is coupled to the bond pads on the substrate in step 905 using a solder or a conductive adhesive.

Whilst the embodiments described supra have employed a component interface for each pad of the assembly it would evident to one skilled in the art that in some instances not all electrical interconnection pads exploit inductors, capacitors, and resistors. Optionally these pads without specified component interconnects may exploit very low resistance resistor components to allow the invention to be applied to these circuits and derive the benefits outlined supra.

Although the descriptive above contains many specificities, these should not be construed as limiting the scope of the embodiment but as merely providing illustrations of some of the presently preferred embodiments. Thus the scope of the embodiment should be determined by the appended claims and their legal equivalents, rather than by the examples given. Accordingly it would evident to one skilled in the art that the

invention can be used in any stacked device where the ability to use components as interconnection exists.

Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.

What is claimed is:

1. An apparatus comprising:
an integrated circuit comprising at least one bonding pad of a plurality of bonding pads;
at least one passive component of a plurality of passive components, each of the plurality of passive components comprising at least an upper connection surface and a lower connection surface electrically connected together;
a package substrate with a surface connection layer comprising at least one landing pad of a plurality of landing pads;
wherein the upper connection surface of the at least one passive component is electrically connected to the least one bonding pad of the plurality of bonding pads and the lower connection surface of the at least one passive component is electrically connected to the least one landing pad of the plurality of landing pads.

2. An apparatus according to claim 1 wherein;
the plurality of bonding pads are electrically connected to upper connection surfaces of the plurality of passive components; and
the plurality of landing pads are electrically connected to the lower connection surfaces of the plurality of passive components.

3. An apparatus according to claim 1 wherein;
the plurality of bonding pads are electrically connected to upper connection surfaces of the plurality of passive components; and
a predetermined portion of the plurality of landing pads are electrically connected to the lower connection surfaces of the plurality of passive components.

4. An apparatus according to claim 1 wherein,
providing the integrated circuit comprises providing an integrated circuit packaged using leadless chip carrier (LCC) packaging.

5. An apparatus according to claim 1 wherein,
providing the at least one passive component comprises providing at least one of a capacitor, resistor and inductor.

6. An apparatus according to claim 1 wherein,

providing the at least one passive component comprises providing discrete SMD components.

7. An apparatus according to claim 1 wherein,
providing the package substrate is an ultra-thin leadless package (UTLP) substrate.

8. An apparatus according to claim 1 wherein,
said package substrate comprises providing the package substrate by at least one of a low-temperature co-fired ceramic (LTCC) substrate, a lead-frame, and printed circuit board (PCB) material.

9. An apparatus according to claim 1 wherein,
providing said surface connection layer of package substrate further comprises providing electrical via connections to the other side of said package substrate from that supporting the plurality of landing pads.

10. An apparatus according to claim 9 wherein,
providing at least one of the plurality of landing pads and electrical via connections comprises providing the plurality of landing pads electrically connected to package pins.

11. An apparatus according to claim 9 wherein,
providing the electrical via connections comprises providing the electrical via connections electrically connected to solder balls on the other side of the package substrate.

12. An apparatus according to claim 1 wherein,
in operation the plurality of landing pads are electrically connected to at least one of receive an unregulated DC voltage, ground, and provide at least one regulated DC voltage of a plurality of DC voltages generated by the integrated circuit.

13. A method comprising:
(a) providing a first substrate with at least a lower surface connection layer;
(b) providing a second substrate with at least an upper surface connection layer;
(c) providing at least one passive component with upper and lower connection surfaces;
(d) coupling said upper connection surface of said at least one passive component to said lower surface connection on said first substrate;

(e) coupling said lower connection surface of said at least one passive component to said upper surface connection on said second substrate.

14. A method comprising:
providing an integrated circuit comprising at least one bonding pad of a plurality of bonding pads;
providing at least one passive component of a plurality of passive components, each of the plurality of passive components comprising at least an upper connection surface and a lower connection surface electrically connected together;
providing a package substrate with a surface connection layer comprising at least one landing pad of a plurality of landing pads;
coupling the upper connection surface of the at least one passive component to the least one bonding pad of the plurality of bonding pads thereby forming an electrical interconnection between them; and
coupling the lower connection surface of the at least one passive component to the least one landing pad of the plurality of landing pads thereby forming an electrical interconnection between them.

15. A method according to claim 14 wherein;
coupling the upper connection surface of the at least one passive component to the least one bonding pad of the plurality of bonding pads and coupling the lower connection surface of the at least one passive component to the least one landing pad of the plurality of landing pads results the plurality of bonding pads and plurality of landings pads being electrically interconnected via the plurality of passive components.

16. A method according to claim 14 wherein;
coupling the upper connection surface of the at least one passive component to the least one bonding pad of the plurality of bonding pads and coupling the lower connection surface of the at least one passive component to the least one landing pad of the plurality of landing pads results the plurality of bonding pads and a predetermined portion of the plurality of landings pads being electrically interconnected via the plurality of passive components.

17. A method according to claim 14 wherein,

providing the integrated circuit comprises providing an integrated circuit packaged using leadless chip carrier (LCC) packaging techniques.

18 A method according to claim 14 wherein,
providing the at least one passive component comprises providing at least one of a capacitor, resistor and inductor.

19. A method according to claim 14 wherein,
providing the plurality of passive components comprises providing discrete SMD components.

20. A method according to claim 14 wherein,
providing the package substrate comprises providing an ultra-thin leadless package (UTLP) substrate.

21. A method according to claim 14 wherein,
providing the package substrate comprises providing the package substrate formed from at least one of a low-temperature co-fired ceramic (LTCC) material, a metal lead-frame, and a printed circuit board (PCB) material.

22. A method according to claim 14 wherein,
providing said surface connection layer of package substrate further comprises providing electrical via connections to the other side of said package substrate from that supporting the plurality of landing pads.

23. A method according to claim 9 wherein,
providing at least one of the plurality of landing pads and electrical via connections comprises providing the plurality of landing pads electrically connected to package pins.

24. A method according to claim 9 wherein,
providing the electrical via connections comprises providing the electrical via connections electrically connected to solder balls on the other side of the package substrate.

25. A method according to claim 1 wherein,
in operation the plurality of landing pads are electrically connected to at least one of receive an unregulated DC voltage, ground, and provide at least one regulated DC voltage of a plurality of DC voltages generated by the integrated circuit.

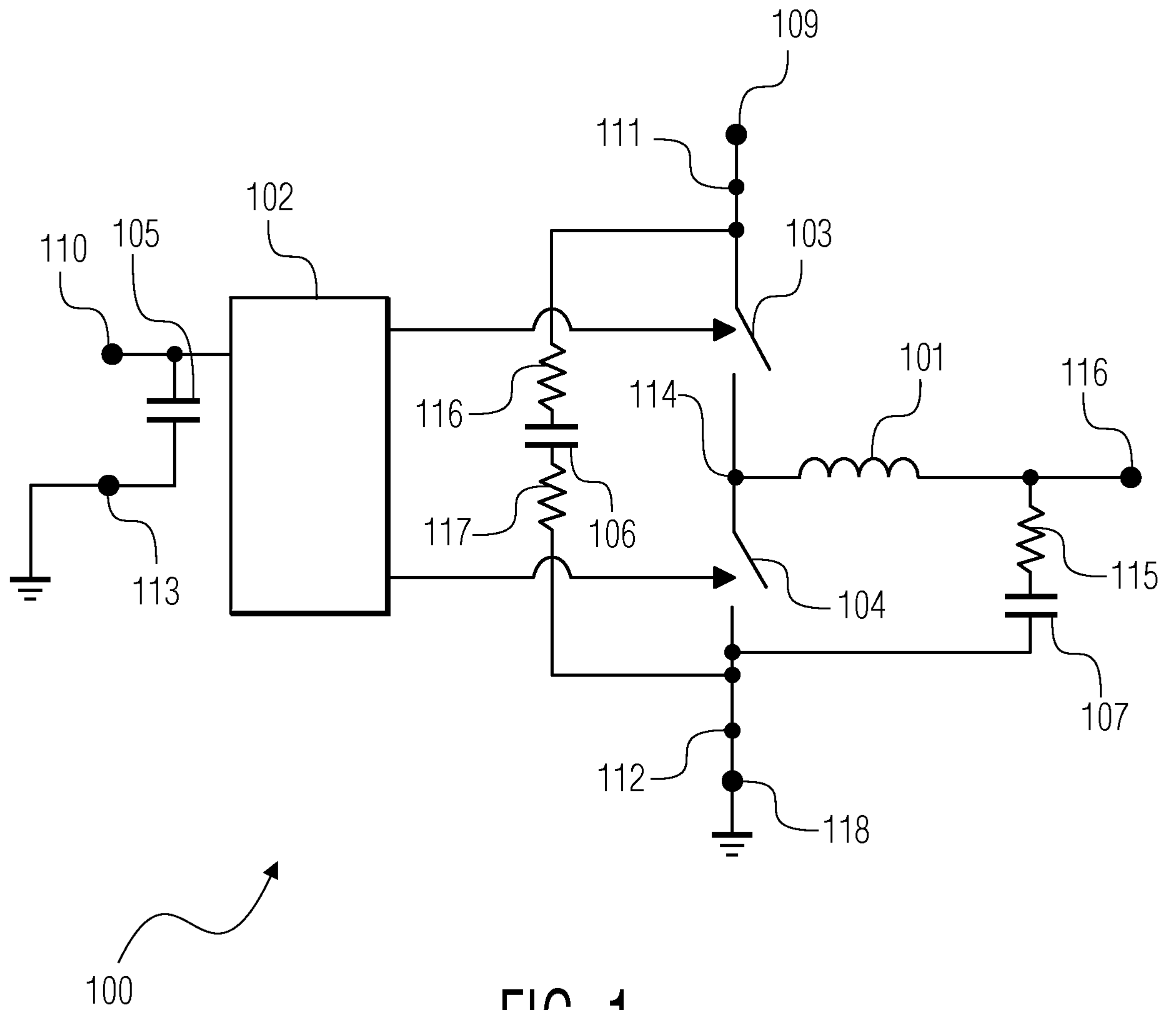


FIG. 1
PRIOR ART

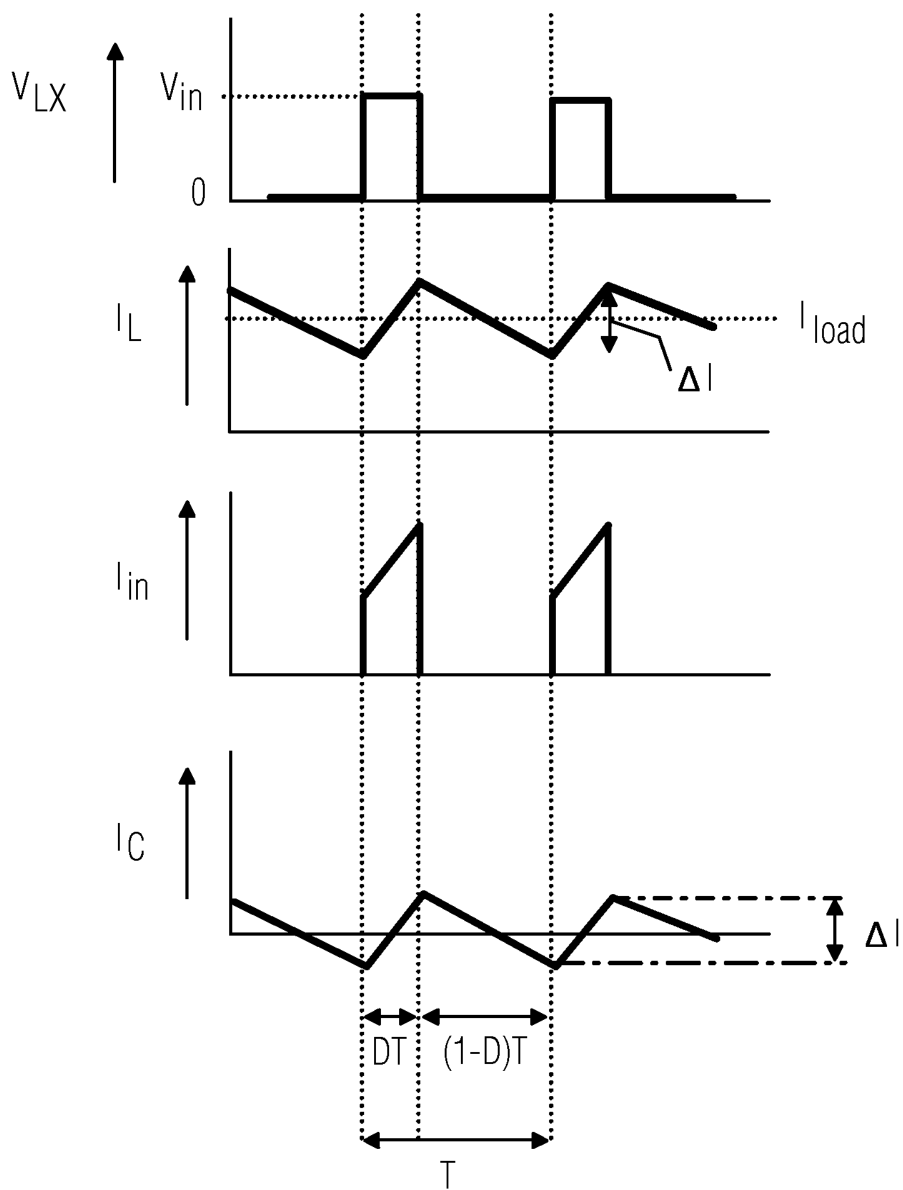


FIG. 2
PRIOR ART

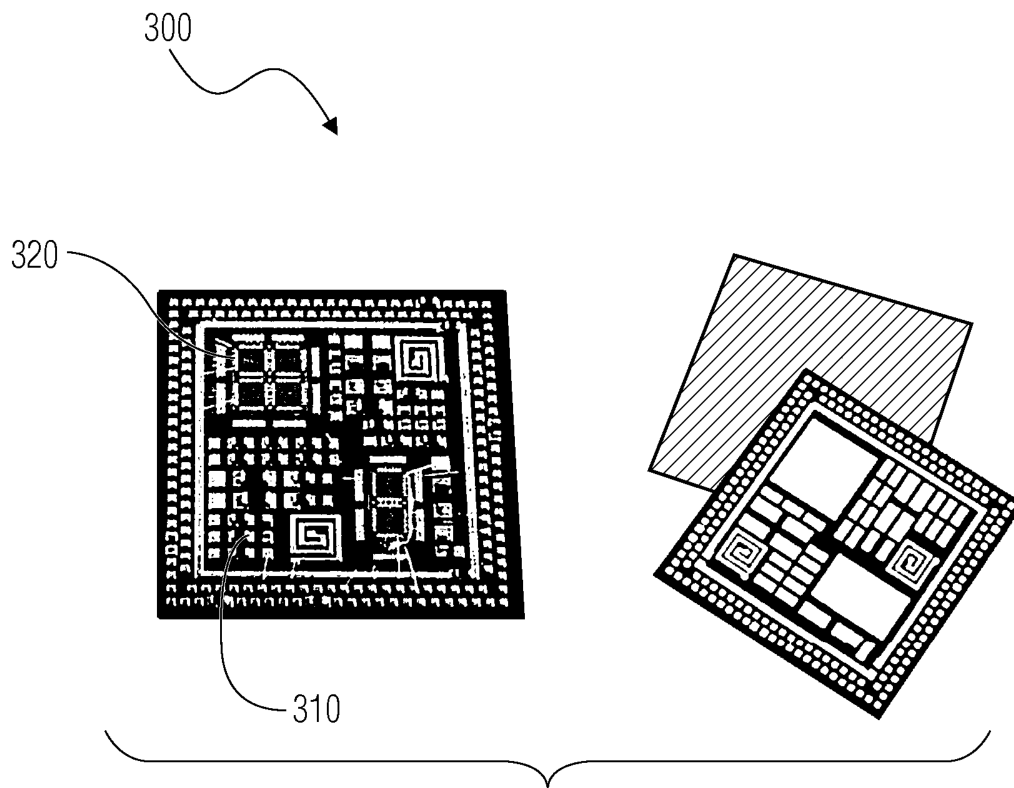


FIG. 3
PRIOR ART

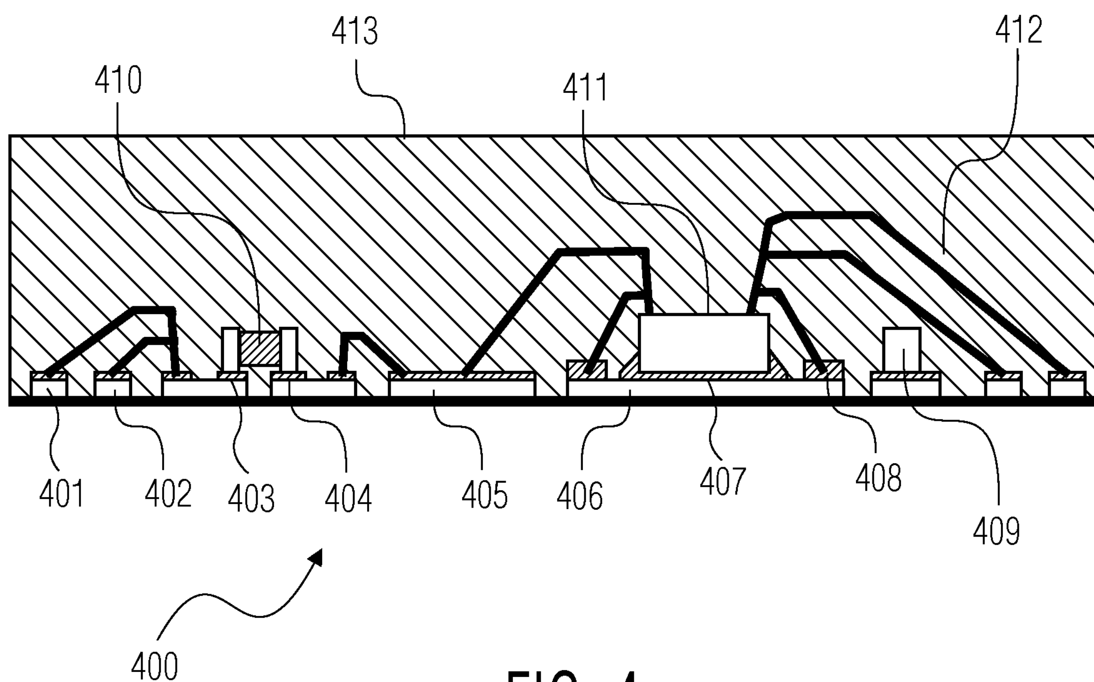


FIG. 4
PRIOR ART

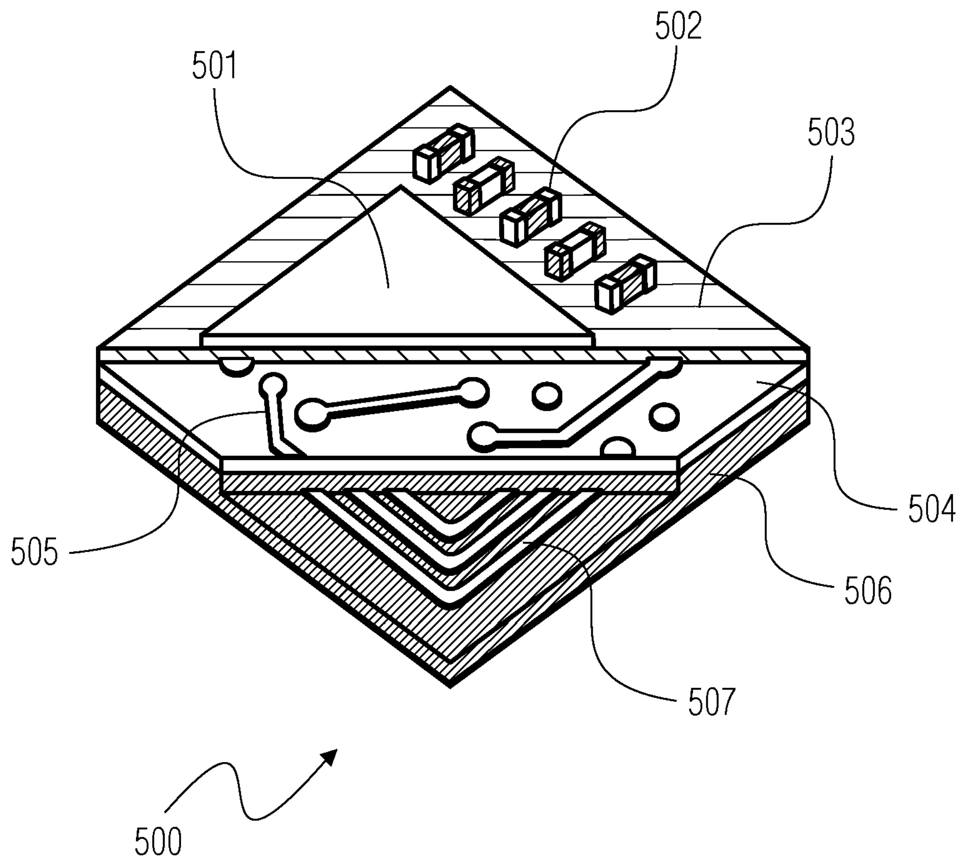


FIG. 5
PRIOR ART

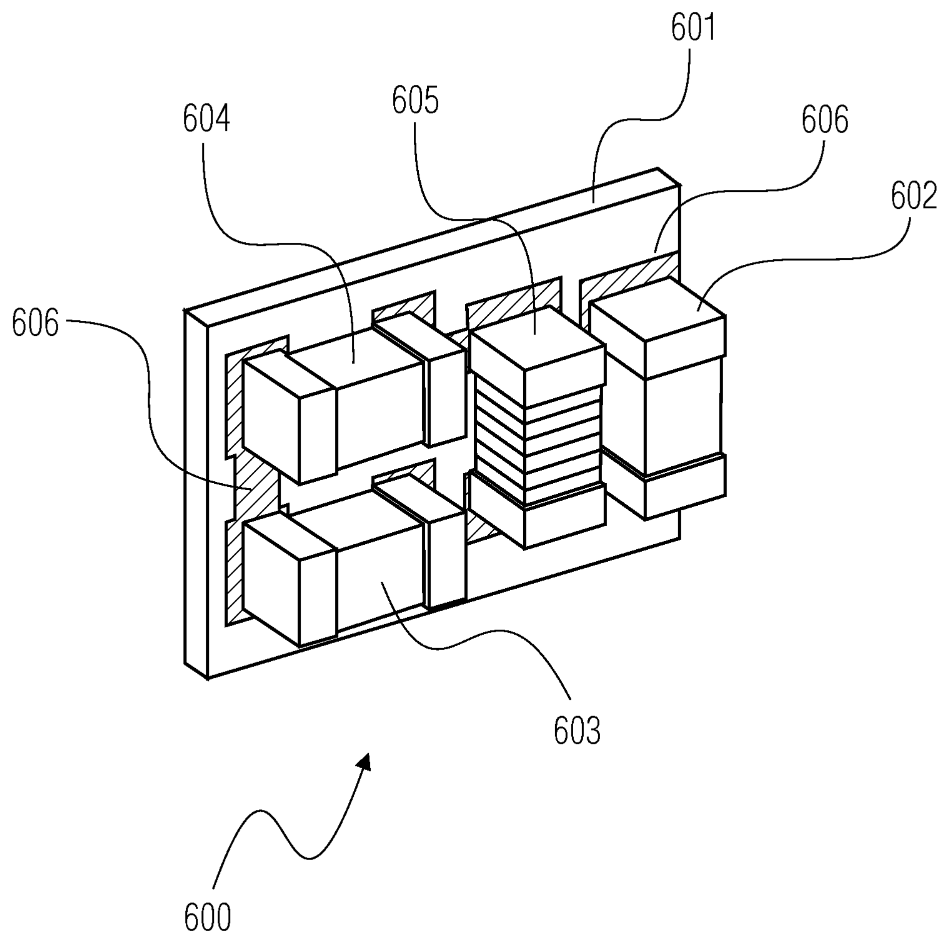


FIG. 6

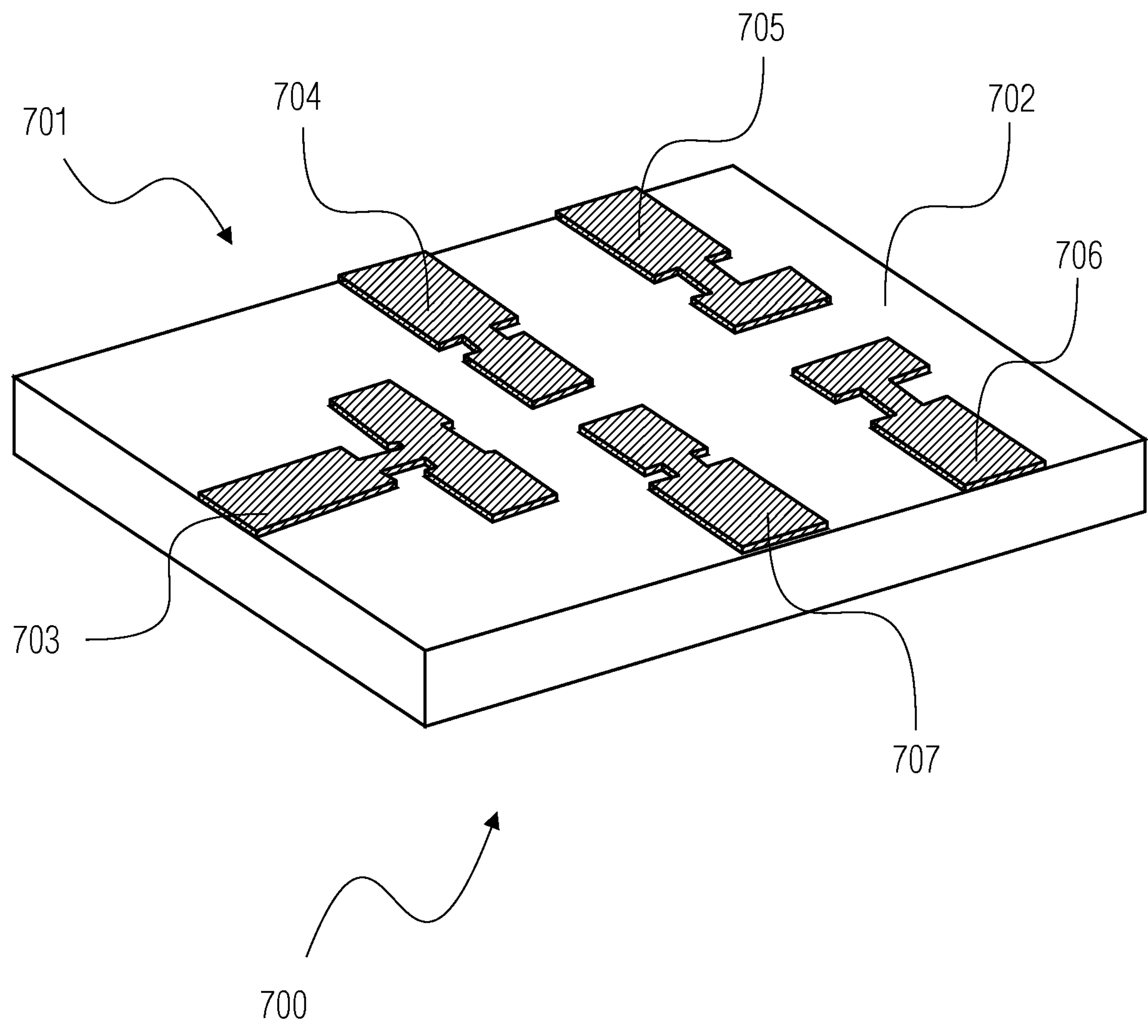


FIG. 7

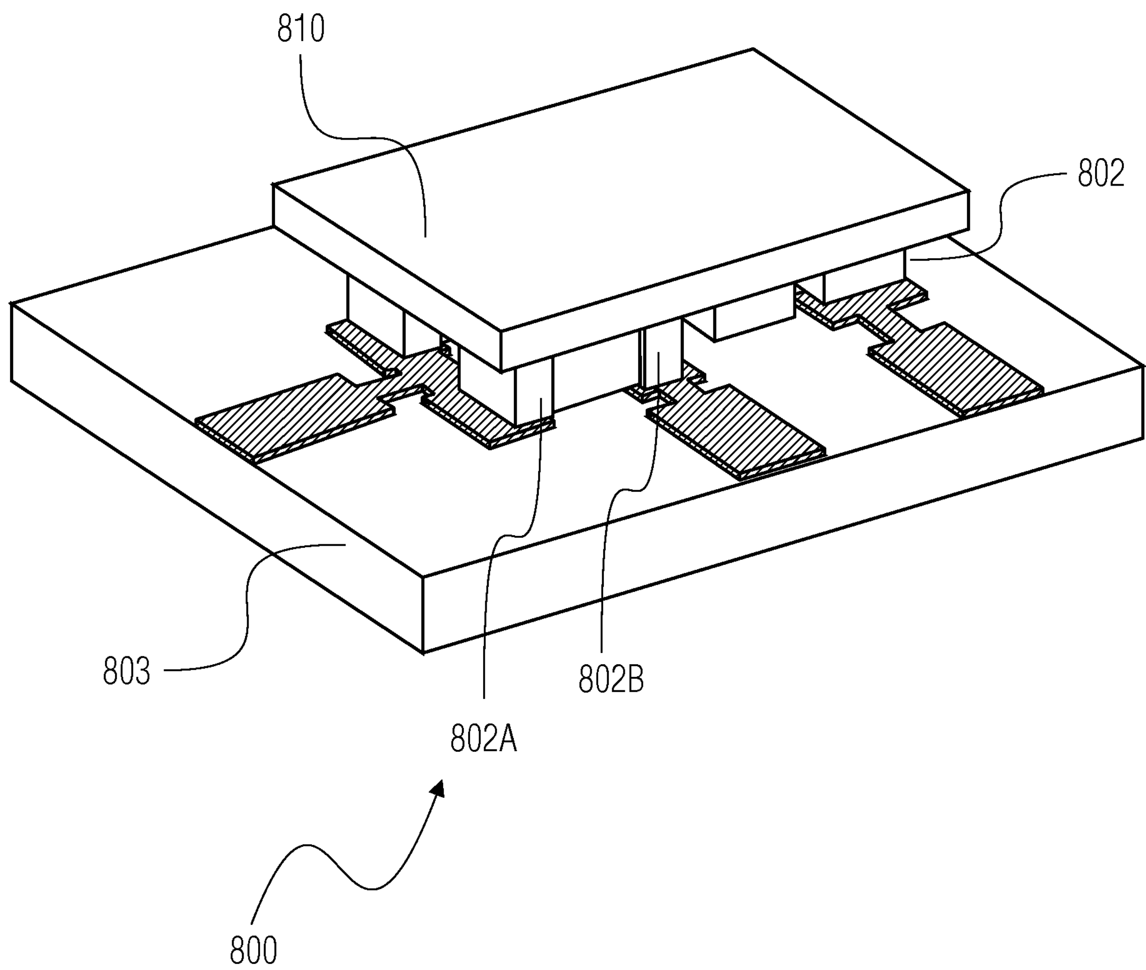


FIG. 8

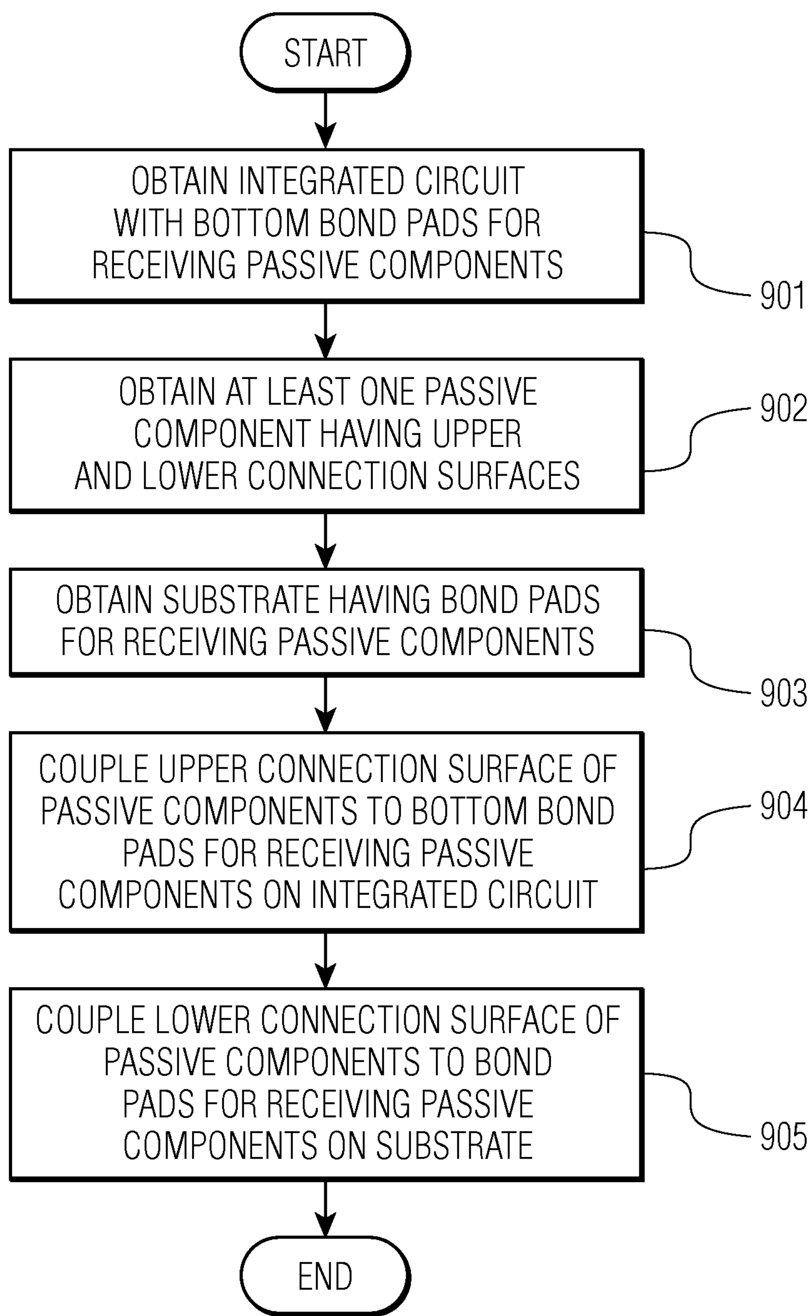


FIG. 9

# INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/055485

**A. CLASSIFICATION OF SUBJECT MATTER**
INV. H05K1/02
ADD. H05K1/14

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | EP 1 367 713 A (VISHAY ELECTRONIC GMBH [DE]) 3 December 2003 (2003-12-03)<br>the whole document<br>----- | 1-25 |
| X | EP 0 996 323 A (TDK CORP [JP]) 26 April 2000 (2000-04-26)<br>abstract<br>paragraph [0008]<br>paragraphs [0022] - [0027]<br>figures 1,2<br>----- | 1-25 |

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

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"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
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| 24 April 2009 | 07/05/2009 |

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Deconinck, Eric

**INTERNATIONAL SEARCH REPORT**

**Information on patent family members**

**International application No**
PCT/IB2008/055485

| Patent document cited in search report | | Publication date | Patent family member(s) | | | Publication date |
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| EP 0996323 | A | 26-04-2000 | JP | 2000114686 | A | 21-04-2000 |
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| | | | US | 6373714 | B1 | 16-04-2002 |