Class-D amplifier

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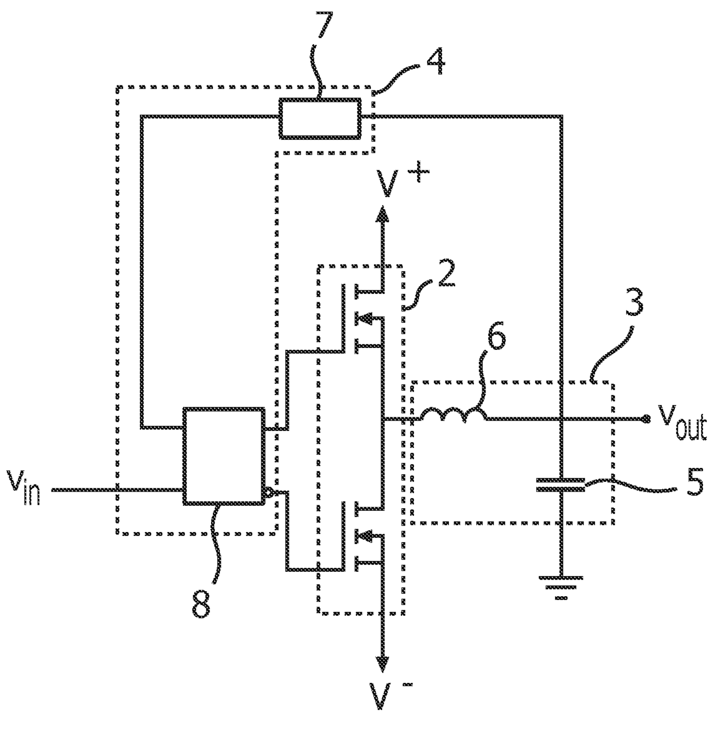
(54) Title: CLASS-D AMPLIFIER



(57) Abstract: The present invention relates to a closed loop class-D amplifier. The amplifier comprises a feedback arrangement with a low frequency path and a high frequency path. The high frequency path is used to obtain a self-oscillating condition in the amplifier and may contain passive components. The low frequency path comprises a low pass filter and a waveform correction circuit that reduces the amplifier distortion. Since the waveform correction circuit is applied in a low frequency path, the waveform correction unit may be realized using e.g. operational amplifiers that need not be rated for high frequencies. This allows a class-D amplifier to be realized with improved distortion and at a low cost.

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Class-D amplifier

FIELD OF THE INVENTION

The present invention relates to a closed loop class-D amplifier for amplifying an electric input signal, the amplifier comprising: a switching block, arranged to generate a block wave signal by alternately switching the block wave signal between first and second states, a low pass filter, arranged to filter the block wave signal to generate an output signal, and a control circuit, receiving the input signal and a feedback signal, which depends on the output signal, and providing a control signal to the switching block, the control signal depending on the feedback signal and the input signal.

BACKGROUND OF THE INVENTION

Such an amplifier is described e.g. in WO 03/090343, A2. This arrangement uses a feedback arrangement that provides a self-oscillating function. An amplifier of this kind is very efficient in terms of energy consumption. However the distortion may be too high for some demanding applications.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a class-D amplifier of the initially indicated type with improved distortion characteristics.

This object is achieved by an amplifier defined as in claim 1.

More specifically, the control circuit of the amplifier then comprises a high frequency feedback path and a low frequency feedback path, the high feedback frequency path comprising passive components, and the low feedback frequency path comprising a low-pass filter and waveform correction means.

This allows the use of active but yet inexpensive components in the low frequency path. The amplifier can therefore provide improved distortion at low cost.

The amplifier may be designed as a full bridge amplifier.

In a preferred embodiment, the high frequency path may comprise passive components only. Then the amplifier may be designed at a comparatively low cost.

The waveform correction means may comprise one or more active elements, such as an operational amplifier. The waveform correction means may for example comprise a differential amplifier, generating a correction signal that corresponds to the difference between the input signal and a fraction of the output signal, and a summing circuit adding the correction signal and the input signal. Such an arrangement may provide substantially improved (reduced) harmonic distortion.

It is also possible to use more than two feedback paths, the feedback paths operating in different frequency bands.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a block diagram of a closed loop class-D amplifier.

Fig. 2a illustrates a schematic embodiment of the amplifier in Fig. 1.

Fig. 2b illustrates a full bridge class-D amplifier configuration.

Fig. 3 illustrates a block diagram of a class-D amplifier according to an embodiment of the invention.

Fig. 4 illustrates a detailed embodiment of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 1 illustrates a block diagram of a closed loop class-D amplifier. The amplifier 1 receives an input signal v_{in} and generates an amplified output signal v_{out}. The output signal is generated by letting a switching block 2 produce a block wave signal, alternating between first and second states, such as the supply voltages V^+ and V^-, (e.g. V^+=+60 V and V^-=-60 V). The block wave signal is filtered by a low-pass filter 3 to generate the output signal v_{out}. The instantaneous amplitude of the output signal depends on the pulse ratio of the block wave signal. A control circuit 4 controls the switching block 2 in order to produce an output signal v_{out} that is an amplified version of the input signal v_{in}.

In this closed loop configuration, the control circuit receives a feedback signal, and the input signal v_{in}. This configuration is suitable for high power applications, e.g. 150 W.

In contrast, an open loop configuration, mostly used in low power applications, does not need a feedback loop. Instead, the input signal and a constant frequency saw tooth or triangle wave signal is compared with the input signal, and the output of the comparator is used to control the switching block.

A closed loop configuration may use a hysteres function as described in US 6107875. As an alternative a configuration using self-oscillation without hysteres effect may be used as disclosed in WO, A2, 03/090343.

Fig. 2a illustrates a schematic embodiment of the amplifier in Fig. 1. The low-pass filter 3 may consist of a capacitor 5 and an inductor 6. The capacitor 5 and the inductor 6 should have such values, that the filter blocks the block wave switching frequency. The control circuit 4 may comprise a feedback network 7 and a comparator 8.

The comparator 8 may have a two complementary outputs, as illustrated, each controlling one switch of a switching block 2. The switches may preferably be MOSFET switches. One switch is connected to a first supply voltage V^+ and the other to a second supply voltage V^-. The switches are further connected to each other at a connection point that constitutes the output of the switching block. Since the switches are controlled in a complementary fashion, one of the switches will always be active while the other is blocked. Therefore, the switching block will output either V^+ or V^-. A self-oscillating condition may be obtained by providing a sufficient phase shift and delay with the feedback network 7 as is known by the skilled person.

The switching frequency f_{sw} of such a class-D amplifier may be defined as:

$$f_{sw} = f_{sw0}\left(1 - M^2\right)$$

where f_{sw0} is the switching frequency near a signal zero-crossing (e.g. 400-500 kHz), and M is the modulation index, i.e. the ratio between the output peak voltage and the supply voltage.

Fig. 2b illustrates a full-bridge configuration corresponding to the embodiment in Fig. 2a. This configuration uses only one supply voltage V^+. Instead, two sets of switching blocks 2’, 2’’ are used. The comparator 8 controls these switching blocks in a complementary fashion, such that, in a first switching state, the output of the first switching block 2’ is connected to earth and the output of the second switching block 2’’ is connected to V^+, whereas, in a second switching state, the output of the second switching block 2’’ is connected to earth and the output of the first switching block 2’ is connected to V^+. Each switching block 2’, 2’’ has a low-pass filter 3’, 3’’, respectively, and a load 10 is connected between the outputs of these filters. The feedback network 7’ may be common to the switching blocks.

Fig. 3 illustrates a block diagram of a class-D amplifier according to an embodiment of the invention. This configuration is directed towards providing a class-D amplifier with improved waveform correction resulting in reduced harmonic distortion. To this end, the feedback configuration has an inner high frequency path, comprising blocks B and C, and an outer low-frequency path, comprising blocks D and E. The configuration further comprises a negated output comparator 8'.

The inner feedback path B, C may comprise passive components only. Preferably resistors and capacitors are used, but in principle also inductors are feasible. This path should be configured to provide self-oscillation, in combination with the comparator 8', the switching block, and the low pass filter 3. As is known to the skilled person, such oscillations may be obtained by providing a feedback loop with a sufficient phase shift and delay. The frequency of this oscillation should preferably be at least approximately ten times higher than the highest possible input signal frequency. Thus, when no input signal is provided, the inner feedback path generates an oscillation with zero average voltage at a frequency that is blocked by the amplifier output filter 3. By applying an input signal at a first summing point 9, the average voltage will rise or fall in such a way that a corresponding, but amplified, output signal is outputted from the filter 3.

The outer low-frequency path comprises a filter block D and an active block E. The filter block D constitutes a low pass filter and provides a filtered low-frequency signal to the active block E. The active block E also receives the input signal v_{in}, and generates a correction signal v_c, which is fed to a second summing point 11. The correction signal can have any polarity, and corresponds to an error induced by the amplifier, i.e. a difference between the input signal and the output signal when the amplifier gain is disregarded. The correction signal can therefore be used to compensate for any non-ideal properties of the amplifier. At the second summing point 11, the input signal v_{in} is added with v_c, and the sum is used as an input signal to the self-oscillating arrangement at the first summing point 9. Since only signals well below the switching frequency is fed to the active block E, this block may comprise more complex active components such as operational amplifiers, without causing high production cost, since the operational amplifiers need not to handle high frequencies.

Of course, other block layouts with separated high frequency and low frequency feedback paths are feasible. In its most general form, the invention can be expressed as providing in the feedback arrangement of a closed loop class-D amplifier an additional low-pass filter and a waveform correction arrangement operating on a signal outputted from this low-pass filter. This may reduce the overall distortion of the amplifier without adding much cost, since the waveform correction arrangement may be designed with inexpensive low frequency components. Of course, such an arrangement may be designed in many different ways.

Fig. 4 illustrates a detailed embodiment of the invention. The class-D amplifier then comprises a low-pass output filter 3 comprising inductor L1 and capacitor C1. This filter receives a block wave signal outputted from the switching block 2, which is controlled by a negated output comparator 8. The output signal v_{out} is fed back to the comparator 8 input via a network 12, comprising resistors R2, R3, R4, R5, capacitors C2 and C3, and a time delay element X1. The network 12 corresponds to blocks B and C as well as the summing point 9 in Fig. 3.

The output signal v_{out} is also fed to a voltage divider and filter network 13, comprising resistors R7, R11 and R17 as well as the capacitor C4. The resistors R11 and R17 constitute a voltage divider, outputting a predetermined fraction of the output signal v_{out}, and Resistor R7 and capacitor C4 constitute a low-pass filter, which filters the divided signal.

The signal outputted from the voltage divider and filter network 13 is fed to a waveform correcting circuit 14, which also receives the input signal v_{in}. The inputted signals are fed to an operational amplifier based differential amplifier circuit, comprising resistors R9, R10, R15, R16, and operational amplifier E2. The differential amplifier outputs a correction signal v_c, which is fed, together again with the input signal v_{in}, to an operational amplifier based summing circuit R12, R13, R14, R18, E3. The output signal generated by the summing circuit is fed to the network 12 where it is used as an input signal for the self-oscillating arrangement.

Of course, other circuit layouts are possible.

In summary, the invention relates to a closed loop class-D amplifier. The amplifier comprises a feedback arrangement with a low frequency path and a high frequency path. The high frequency path is used to obtain a self-oscillating condition in the amplifier and may contain passive components. The low frequency path comprises a low pass filter and a waveform correction circuit that reduces the amplifier distortion. Since the waveform correction circuit is applied in a low frequency path, the waveform correction unit may be realized using e.g. operational amplifiers that need not be rated for high frequencies. This allows a class-D amplifier to be realized with improved distortion and at a low cost.

The invention is not restricted to the described embodiments. It can be altered in different ways within the scope of the appended claims.

CLAIMS:

1. A closed loop class-D amplifier for amplifying an electric input signal (v_{in}) the amplifier comprising:

a switching block (2, 2’, 2’’), arranged to generate a block wave signal by alternately switching the block wave signal between first and second states,

a low pass filter (3), arranged to filter the block wave signal to generate an output signal (v_{out}), and

a control circuit (4), receiving the input signal and a feedback signal, which depends on the output signal, and providing a control signal to the switching block, the control signal depending on the feedback signal and the input signal, wherein

the control circuit comprises a high frequency feedback path and a low frequency feedback path,

the high frequency feedback path (B, C, 9) comprising passive components, and

the low frequency feedback path (D, 11, E) comprising a low-pass filter and waveform correction means.

2. A closed loop class-D amplifier according to claim 1, wherein the amplifier is a full bridge amplifier.

3. A closed loop class-D amplifier according to claim 1 or 2, wherein the high frequency path comprises passive components only.

4. A closed loop class-D amplifier according to any of the preceding claims, wherein the waveform correction means comprises an active element.

5. A closed loop class-D amplifier according to claim 4, wherein the waveform correction means comprises a differential amplifier (E), generating a correction signal (v_c) that corresponds to the difference between the input signal (v_{in}) and a fraction of the output

signal (v_{out}), and a summing circuit (11), adding the correction signal (v_c) and the input signal (v_{in}).

6. A closed loop class-D amplifier according to any of the preceding claims, comprising more than two feedback paths, the feedback paths operating in different frequency bands.

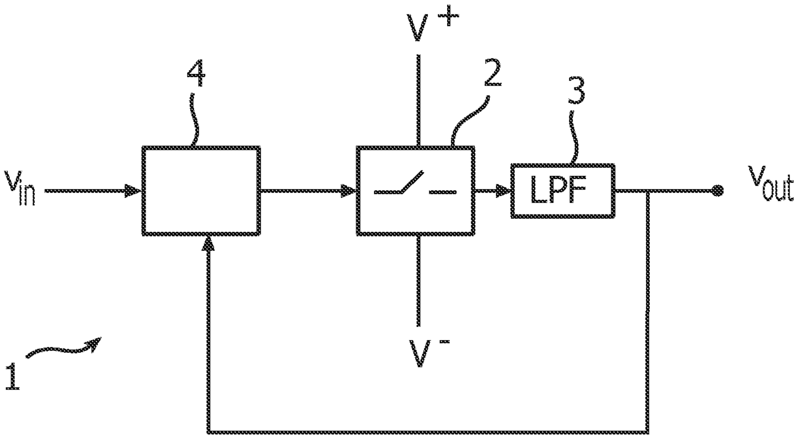


FIG.1

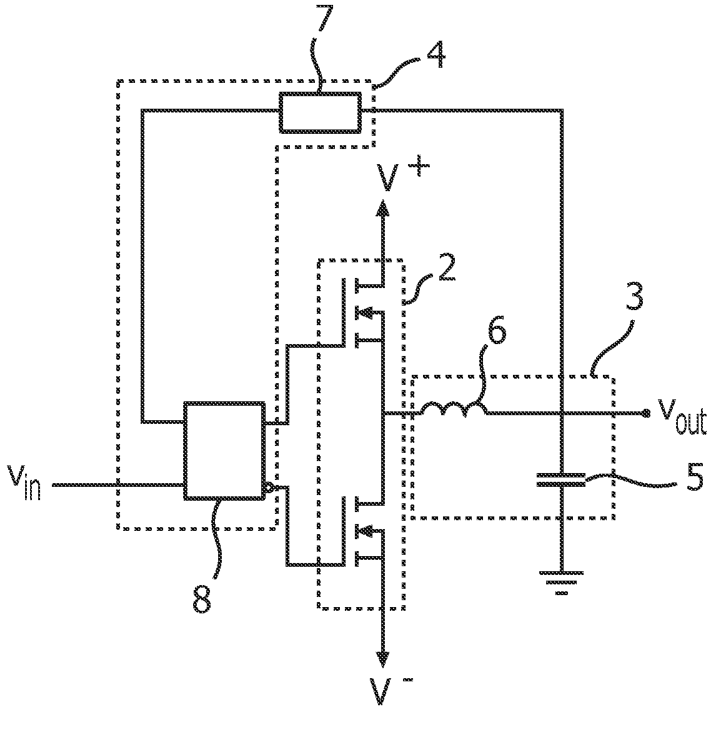


FIG.2a

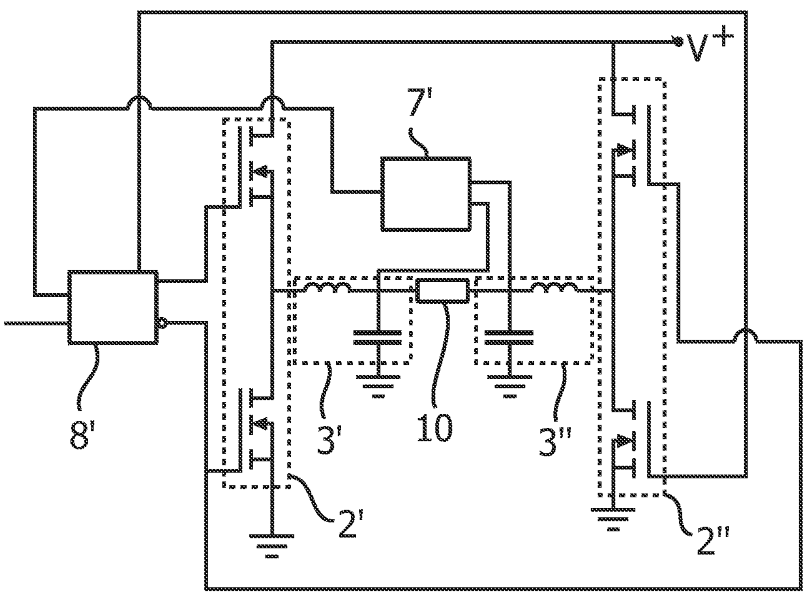


FIG.2b

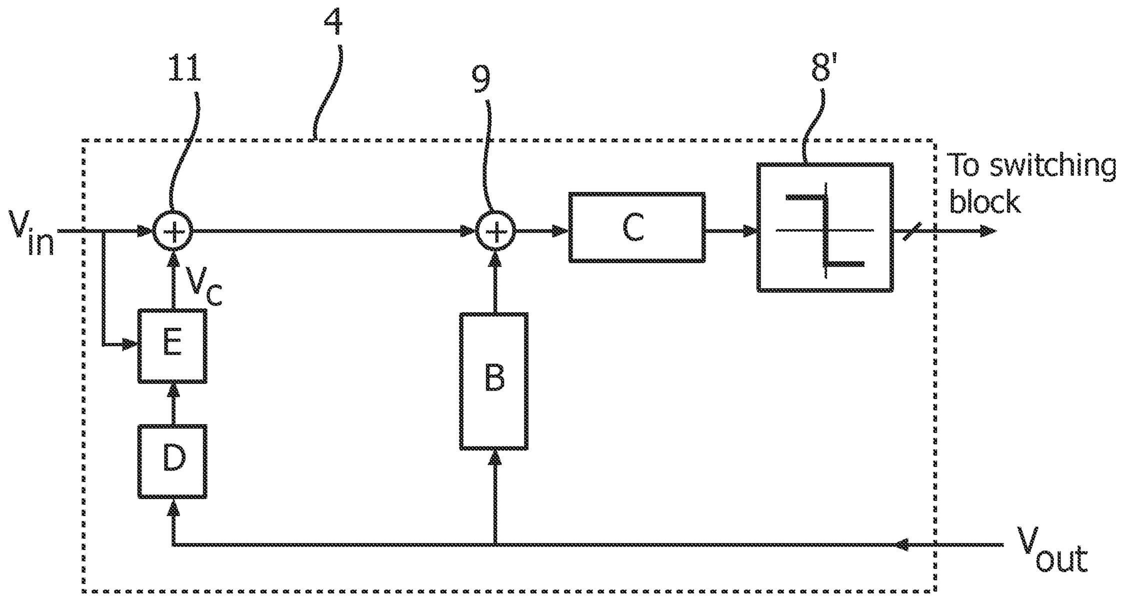
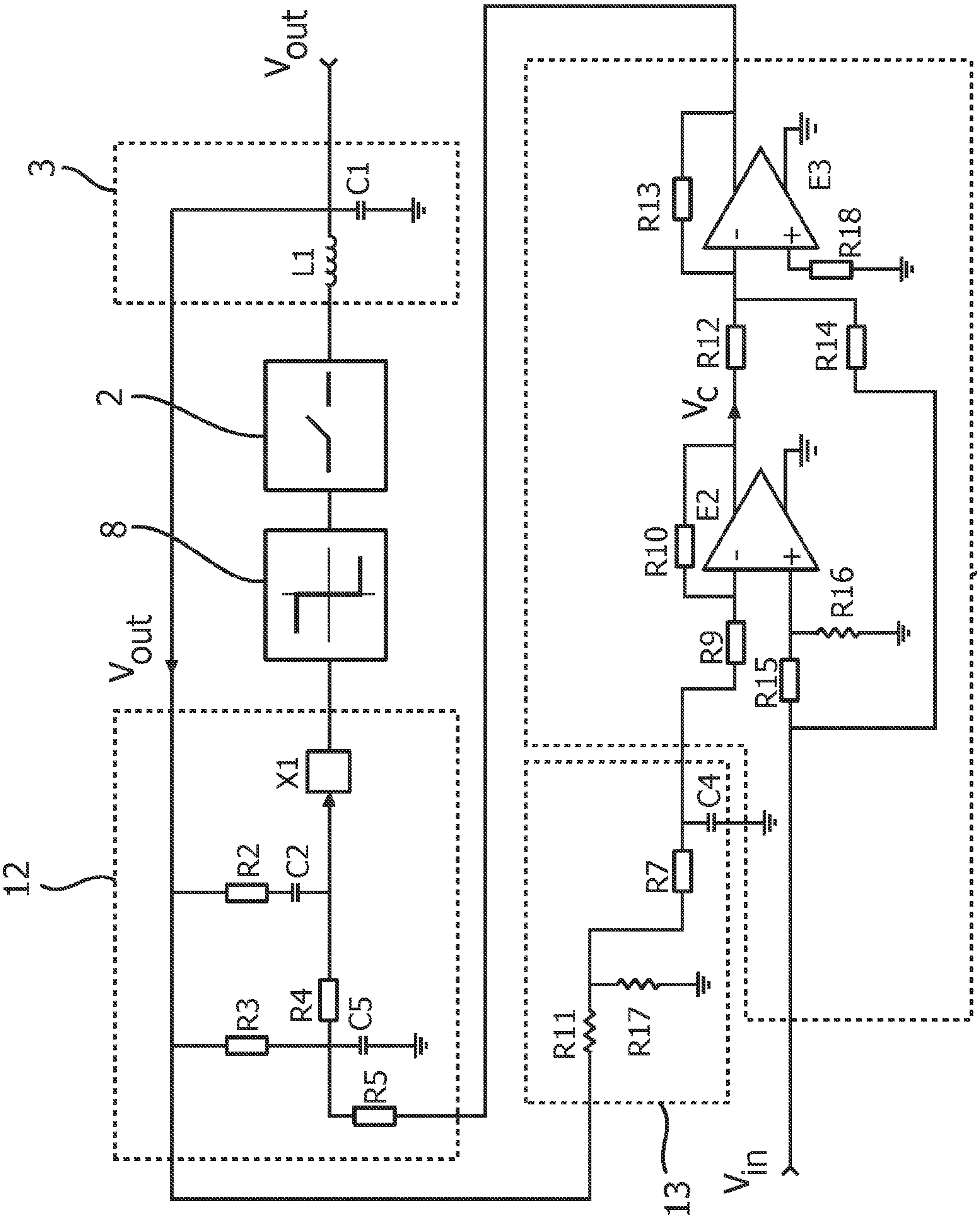


FIG.3

FIG.4


V_{out}
3
C1
L1
2
8
V_{out}
12
R2
C2
X1
R3
R4
C5
R5
R13
E3
R18
R12
V_C
R14
R10
E2
R9
R16
R15
14
C4
R7
R11
R17
13
V_{in}

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051107

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F3/217

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 552 606 B1 (VELTMAN ANDRE ET AL) 22 April 2003 (2003-04-22) abstract; figures 3,4,13	1-4,6
X	PATENT ABSTRACTS OF JAPAN vol. 005, no. 095 (E-062), 20 June 1981 (1981-06-20) & JP 56 039606 A (MATSUSHITA ELECTRIC IND CO LTD), 15 April 1981 (1981-04-15) abstract; figure 4	1-4
X	US 5 352 986 A (MODGIL ET AL) 4 October 1994 (1994-10-04) figures 2,8	1,2,4

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 July 2006	20/07/2006

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2006/051107

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2004/100356 A (DANMARKS TEKNISKE UNIVERSITET; POULSEN, SOEREN) 18 November 2004 (2004-11-18) pages 14-15,22; figures 6-8,21	1-4,6
X	WO 2004/034577 A (DMB TECHNOLOGY CO., LTD; JANG, BYUNG-TAK; RYOO, TAE-HA) 22 April 2004 (2004-04-22) abstract	1
A	WO 03/061117 A (ADVANCED DIGITAL BROADCAST POLSKA SP. Z.O.O; ADVANCED DIGITAL BROADCST) 24 July 2003 (2003-07-24) abstract	1
A	WENKANG HUANG ED - INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "A new control for multi-phase buck converter with fast transient response" APEC 2001. 16TH. ANNUAL IEEE APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION. ANAHEIM, CA, MARCH 4 - 8, 2001, ANNUAL APPLIED POWER ELECTRONICS CONFERENCE, NEW YORK, NY : IEEE, US, vol. VOL. 1 OF 2. CONF.16, 4 March 2001 (2001-03-04), pages 273-279, XP010536007 ISBN: 0-7803-6618-2 the whole document	1
A	US 4 178 556 A (ATTWOOD, BRIAN E) 11 December 1979 (1979-12-11) abstract	1
A	US 6 441 685 B1 (MACMILLAN BRUCE E) 27 August 2002 (2002-08-27) abstract	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2006/051107

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 6552606	B1	22-04-2003	AT	264020	T	15-04-2004
			AU	754082	B2	07-11-2002
			AU	2130000	A	01-08-2000
			CA	2360345	A1	20-07-2000
			CN	1337089	A	20-02-2002
			DE	60009656	D1	13-05-2004
			DE	60009656	T2	12-08-2004
			DK	1142106	T3	21-06-2004
			EP	1142106	A1	10-10-2001
			ES	2216854	T3	01-11-2004
			HK	1041569	A1	15-04-2005
			ID	30217	A	15-11-2001
			JP	2002535863	T	22-10-2002
			MX	PA01006295	A	17-04-2002
			WO	0042702	A1	20-07-2000
			NL	1011002	C2	20-07-2000
			NO	20012866	A	28-08-2001
			NZ	512718	A	31-01-2003
			PT	1142106	T	31-08-2004
			TR	200102000	T2	21-12-2001
			TW	504896	B	01-10-2002
JP 56039606	A	15-04-1981	JP	1355422	C	24-12-1986
			JP	61021007	B	24-05-1986
US 5352986	A	04-10-1994	AU	6266894	A	15-08-1994
			CA	2154490	A1	04-08-1994
			WO	9417588	A1	04-08-1994
			US	5521549	A	28-05-1996
WO 2004100356	A	18-11-2004	EP	1632024	A2	08-03-2006
WO 2004034577	A	22-04-2004	AU	2003271195	A1	04-05-2004
			JP	2006502652	T	19-01-2006
			US	2006001488	A1	05-01-2006
WO 03061117	A	24-07-2003	AU	2003214729	A1	30-07-2003
			PL	351783	A1	28-07-2003
			US	2005083113	A1	21-04-2005
US 4178556	A	11-12-1979	GB	1560195	A	30-01-1980
			JP	53146337	U	17-11-1978
			JP	59000814	Y2	11-01-1984
US 6441685	B1	27-08-2002	AU	4748701	A	03-10-2001
			WO	0171905	A2	27-09-2001