# Next Generation of Ultra-High Precision Amplifiers 

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# Next Generation of Ultra-High Precision Amplifiers 

Pelle Weiler

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In Gedenken an Carl-Heinz Weiler

# Next Generation of Ultra-High Precision Amplifiers 

## PROEFSCHRIFT


#### Abstract

ter verkrijging van de graad van doctor aan de Technische Universiteit Eindhoven, op gezag van de rector magnificus prof. dr. S. K. Lenaerts, voor een commissie aangewezen door het College voor Promoties, in het openbaar te verdedigen op donderdag 6 juli 2023 om 11:00 uur.


door

Bjoern Pelle Weiler
geboren te Bremen, Duitsland

Dit proefschrift is goedgekeurd door de promotor. De samenstelling van de promotiecommissie is als volgt:

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Het onderzoek dat in dit proefschrift wordt beschreven is uitgevoerd in overeenstemming met de TU/e Gedragscode Wetenschapsbeoefening.

## Summary

## Next Generation of Ultra-High Precision Amplifiers

IN recent years power electronics has seen vast improvements in integration, size reduction and bandwidth, partly thanks to advances in semiconductor and manufacturing technology. In 2014 Google's "Little Box Challenge" revealed the potential of wide-bandgap devices, particularly gallium-nitride, which just arrived on the commercial market.

As a new technology, gallium-nitride still undergoes rigorous qualification for application in industry applications. In the field of high-precision power electronics, such as amplifiers for medical imaging or semiconductor lithography, the qualities of gallium-nitride devices show promises for increased control bandwidth, higher precision and higher power density. These benefits are due to higher switching frequencies, better timing tolerances and smaller device footprints and passive components. At the same time, these advantages lead to new design boundaries, which still need to be explored.

This thesis presents analytic methods for fast and accurate quantification of several effects and limits encountered when utilizing wide-bandgap devices at high switching frequencies. The focus lies on the basic half-bridge topology, but the developed methods can be easily adapted to more advanced topologies.

The thesis begins with thermal analysis to semiconductors, leading to a new way of calculating the temperature swing of transistors, including temperature dependent losses. The provided insight into the transistor's junction temperature profile allows to dimension a half-bridge correctly and make the trade-off between conduction and switching losses. To maximize the dissipation of these losses, the thermal interface for wide-bandgap devices is investigated. A new performance metric is introduced, which designates an insulator's capability of cooling a device, while providing a low parasitic capacitance between the device and heatsink.

Using the presented temperature calculation method, the limits with regards to output power, switching frequency, efficiency and temperature of a single halfbridge can be calculated. To improve further, more advanced topologies have to be used. In this work, the interleaved inverter is investigated. By connecting multiple half-bridges in parallel, the output current can be increased, without increasing the current stress of each individual half-bridge. Additionally, by phase shifting each bridge, a higher effective switching frequency and sample-rate can be achieved, in addition to cancellation of current output ripple at specific operating points. Furthermore, adding magnetic coupling between the filter inductors introduces additional, operating-point dependent benefits. It is shown that the number of interleaved half-bridges and the strength of magnetic coupling have a profound impact on the achievable output bandwidth, as well as output current ripple. This dependence leads to highly application specific design decisions to be made.

The effect of propagation delay related errors and noise in current measurements is analyzed for a half-bridge inverter. A proposed weighting of consecutive samples allows to mitigate the error introduced through propagation delay. To keep a high power density, small package shunt resistors are investigated for high-bandwidth measurements. Analytical methods are developed to quickly gauge the distortion introduced by the resistor's thermal properties. The model for thermal distortion is experimentally verified and allows to select devices with sufficiently low thermal dependence to eliminate the measurable distortion in the frequency range of interest.

A prototype is developed and constructed with the focus on ultra high-precision positioning systems for semiconductor lithography. The design process of all components is described in detail and the performance is verified through measurements.

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## 1 <br> Introduction

"No physical quantity can continue to change exponentially forever. Your job is delaying forever."

Gordon Moore

IN the late 1950s and early 1960s, photolithography emerged as the dominant method for creating patterns on semiconductor materials. Photolithography involves the use of light to transfer a pattern onto a light-sensitive material, which is then developed and used to etch the pattern into the semiconductor substrate. Over the years, the resolution and accuracy of photolithography have been improved through the use of more advanced light sources, mechanical and optical systems, as well as photoresists. Current immersion lithography is limited to pattern sizes down to 40 nm with a single exposure pass [60]. With the continuing trend towards miniaturization in electronics, there has been a significant effort towards the development of extreme ultraviolet (EUV) lithography as a means of achieving the high resolution and accuracy needed for next-generation semiconductor devices.


Figure 1.1 Early lithography machine ${ }^{1}$.

### 1.1 A brief history of semiconductor lithography

The term lithography, stems from the two ancient greek words $\lambda \boldsymbol{i} \hat{\vartheta} \circ \rho$ (líthos, "stone") and $\gamma \rho \dot{\alpha} \varphi \varepsilon \iota \nu$ (gráphein, "to write"). Originally a method for printing on paper, it emerged in the late 1700s as a new way to print text and images on an industrial scale. By treating the surface of a limestone, oil paint can be applied in specific patterns and pressed against paper to print the pattern repeatedly, enabling mass printing of text and pictures. The industrialized process is depicted in Figure 1.1. Because the stone made direct contact with the paper, print quality degraded with each successive print.

About 200 years later, a similar issue was faced in semiconductor production by early contact lithography. Here, light is used to transfer a desired pattern through a mask, exposing a light sensitive lacquer on the wafer. The photomask is in direct contact with the wafer surface and illuminated from behind. This contact damaged both mask and wafer, making it unsuitable for very large volume production. Proximity lithography introduces a small gap between wafer and mask, at the cost of attainable resolution. At the end of the 70 s, the semiconductor industry quickly moved on to projection lithography, where light is passed through a lens system and projected onto the wafer [31]. Still, the chip design was fully illuminated in one step and the wafer advanced, to expose the adjacent area. Position accuracy during movement was not important, as the light source was turned off.

The next big advance came with the advent of wafer scanners [10]. Here, the exposure area is reduced to a thin slit, which moves continuously across the wafer's surface. The mask is moved accordingly, such that the correct part of the design matches the position on the wafer. This approach allows to operate the light source

[^0]

Figure 1.2 Modern EUV-lithography machine.
continuously, significantly increasing the processing speed of wafers. The rate of wafer production is commonly referred to as throughput, or 'troepoet' if you reside within in the vicinity of Eindhoven. In addition, the reduction of the optical area to a slit allows to further increase optical resolution, critical for the advancement of semiconductor technology [11]. Such a machine is depicted in Figure 1.2, where extreme ultraviolet light at a wavelength of 13.5 nm is used to expose state of the art feature sizes.

However, as the light is continuously exposing the now moving mask, the position accuracy of mask and wafer-stage have to be maintained during motion. Additionally, due to the optical magnification, the mask has to be moved at four times the speed of the wafer stage. In the beginning, this task was partly performed by linear power amplifiers, which quickly led to an overly large, inefficient power rack required to operate the machine. As the machine's throughput is critical, the scanning process needs to become faster. To halve the duration of the entire process, the time of the scanning itself, as well as the time spent accelerating needs to be reduced by half. To move the wafer stage and mask at twice the speed entails four times the mechanical energy. Including acceleration, both elements also need to be brought up to double the speed in half the time. Four times the amount of energy in half the time leads to eight times the required power. This step can only be taken a few times before the size of the required power electronics grows out of proportion. At some point, switched-mode power electronics became essential to provide the required power.


Figure 1.3 Simplified motion system of an EUV lithography machine [56]. While one wafer is already being exposed, the other wafer is aligned to prepare the exposure. The actuators exert force against a floating balance mass, cancelling most of the mechanical excitation of the base frame.

### 1.2 Power amplifiers for high-precision motion systems

The task of power amplifiers is to follow a reference current from the positioning system as closely as possible to ensure high position accuracy. In modern lithography machines, the total positioning error is about 100 pm , and has to decrease further to facilitate the demand for smaller feature sizes. This precision, while moving the wafer across the machine spanning meters, is obtained by splitting the motion system of each moving element in two separate stages, as shown in Figure 1.3.

The purpose of the first stage, commonly referred to as long-stroke actuator, is to move the wafer through the machine on a scale of meters, at a precision of micrometer. The actuator is driven by a three-phase power amplifier. The output power is immense, as the entire mass of the wafer stage and mask is accelerated for each scanning process. Recent research investigated amplifiers with a supply voltage of 2 kV , as a means to supply more power to the actuators [51]. To reach the required position accuracy, a second stage is located on top, whose purpose is to reduce the remaining micrometer error down to picometers.

To achieve picometer precision, the second stage, known as short-stroke actuator, drives a highly linear, single-phase actuator. As the force is linked directly to the supplied current, the magnitude, bandwidth and accuracy of this current determines the achievable throughput and position error.

To produce more wafers with smaller feature size, output power, control bandwidth and precision of both power amplifiers needs to increase. As secondary objective, the resulting amplifiers should stay cost effective and minimal in volume. At some point, a single inverter will run into physical limitations.

At it's thermal limit, the output current can only be increased by reducing the switching frequency. As a result, the control bandwidth decreases. Vice versa, the output current needs to decrease if higher switching frequency is desired. However, higher switching frequency entails faster sampling of the output current, which negatively affects precision. These and many more interactions limit the possible implementations. Finding a viable, cost effective implementation is impaired by the sheer number of possibilities and the vastly different timescales, at which component choices affect inverter performance.

### 1.3 Research objectives

The goal of this thesis is to provide insight into the power, bandwidth and precision dependencies on an analytic or computationally efficient level, such that synthesis of a viable inverter becomes easier and faster. To achieve this, several research objectives have been formulated.

- Obtain an analytic solution for junction temperature and losses of power semiconductors
As the thermal limit of a transistor determines the maximum output power and bandwidth of any inverter, knowledge of this limit is critical for inverter design. While it is possible to obtain the device temperature through simulation, an analytic method, if precise and fast enough, would allow to evaluate a larger set of topologies, devices and component values in significantly less time.
- Formulate a design metric of thermal interfaces for wide-bandgap devices Wide-bandgap devices allow to switch faster compared to standard silicon components. However, this increase in switching speed also results in proportionally larger currents through parasitic capacitances. Combined with physically smaller device packages, material selection and dimensioning of a thermal interface for wide-bandgap devices requires additional attention, particularly towards parasitic elements.
- Find the parametric interrelationship of power, bandwidth and precision At some point, increasing one attribute, be it output power, bandwidth or precision leads to degradation of another. By knowing the relationship between each of these, topology and component values can be formulated to fulfill the desired requirements.
- Establish an inverter design targeted towards time-gated, high position accuracy
Several metrics exist to specify the output quality of an inverter, such as signal-to-noise ratio (SNR) or total harmonic distortion (THD). However, these factors usually consider a sinusoidal load current. Positioning of a wafer follows a trapezoidal acceleration reference, and precision is only important while exposure is taking place. By analyzing the operating point dependency of current ripple and measurement errors, design choices beneficial for positioning accuracy can be made.


### 1.4 Thesis outline

Chapter 2 begins with the analytic solution for the junction temperature of a transistor, including temperature dependent losses. The introduced method, based on the concept of harmonic balance, is shown to be multiple orders of magnitude faster compared to standard simulation tools, while maintaining very high accuracy. The method is verified by comparison to simulation results of over one thousand inverter configurations.

Next, chapter 3 investigates the impact of thermal interfaces on wide-bandgap devices. A performance metric for insulation materials is introduced, which directly links thermal performance to the parasitic impact. Using analytic methods for heat-transfer, heat-spreaders are designed to enhance the thermal performance of small-sized gallium-nitride devices. The resulting parasitic effect on switching performance is verified with a double-pulse setup. Finally, using the introduced harmonic balance method, it is shown how to obtain the optimal heat-spreader for arbitrary inverters.

As the thermal limit one half-bridge can be calculated, chapter 4 covers the operation of multiple interleaved half-bridges to increase output power and bandwidth. Interleaving reduces the current stress per half-bridge, which allows to operate at a higher switching frequency. In addition, implementing phase shift of the respective carriers further increase control bandwidth, as well as ripple cancellation at the input and output. Lastly, by coupling the inductors of multiple phases, further bandwidth increase or ripple reduction of the phase currents can be achieved.

While the bandwidth and output power can be increased through interleaving, control and subsequently sensing of each individual phase current is required. Increasing the bandwidth or input range of this measurement potentially degrades attainable precision. Chapter 5 investigates timing related noise in high-bandwidth current measurements and proposes a straight-forward compensation method.

Next, chapter 6 investigates the effect of power dissipation in shunt resistors. A simplified method is developed to quickly calculate the resulting distortion levels due to thermal dependency of the resistance. The method is verified through experiment and allows to select shunt resistors for current measurements with sufficiently low distortion.
Using the established knowledge, chapter 7 covers the design, implementation and experimental evaluation of an amplifier targeted towards position accuracy of a short-stroke actuator. Full dynamic current control of a coupled inductor is realized and experimentally verified. Operation of the inverter is tested by following the reference current provided by a typical position system of a semiconductor lithography machine.

Finally, chapter 8 concludes this work and provides an overview over the scientific contributions, as well as recommendations for future research.

## 2 <br> Junction temperature calculation using harmonic balance

> "There are times in life when people must know when not to let go. Balloons are designed to teach small children this."

Terry Pratchett

ACCURATE calculation of semiconductor losses and temperature is the foundation of any design methodology for a power electronic converter. Computation accuracy and speed play a vital role, if a large set of parameters needs to be explored over a large range. Averaged loss models often neglect the temperature dependence of transistors, leading to fast, but inaccurate results [15]. In contrast, iterative methods and simulation tools, which can include temperature dependence, take significantly longer to compute, but yield more precise results. This chapter presents a best of both worlds approach, by using the harmonic balance method to directly obtain the steady-state solution for any inverter topology including temperature dependent conduction and switching losses. The proposed method solves for the discrete Fourier series of the device temperature, by expressing the temperature dependence and operating parameters in the frequency domain. The set of equations for each Fourier coefficient is solved by a single matrix inversion, resulting in very fast computation for steady-state temperature cycles.

[^1]

Figure 2.1 Pulse-width modulated half-bridge.

### 2.1 Simulating temperature-dependent losses

Optimizing power electronic converters typically involves the pursuit of multiple objectives, such as efficiency, power density, component lifetime and cost [43] [6]. This optimization procedure often starts with a large number of potential operating parameters and components, in order to meet the desired specifications. For each set of parameters, the losses and performance of the converter are either calculated based on averaged states or iterated in time for more precise results [9] [29]. Usually, averaged models are much faster than iterative ones, but iterative solutions can include non-linear effects often neglected in averaged models [77]. Depending on the severity of the non-linearity, iterative simulation might be the only commonly available option towards correct results. In case of power electronic devices, such as $\mathrm{Si}, \mathrm{SiC}$ or GaN transistors, accurate calculation of the total device losses is severely impeded by the temperature dependency of both conduction and switching losses [28] [78]. The temperature dependent losses can either be obtained through device characterization [14] or analytic modelling [20].

Given the half-bridge inverter in Figure 2.1, each transistor experiences a temperature swing because of varying load conditions during each ac cycle. Because the device losses depend on temperature, an algebraic loop is formed: as the device heats up, the losses increase, which in turn further increases the temperature [29]. The convergence of this loop depends on the output frequency of the inverter as well as the thermal interface of the device. Given proper thermal design, the device will reach a periodic steady-state that is within the allowed operating parameters, after a certain number of cycles. Once in steady-state, the device temperature cycles between a constant minimum and maximum. The average device losses during this cycle can then be used to determine the operating efficiency of the inverter. Furthermore, the temperature swing experienced by the transistor is relevant for lifetime estimation, as thermal expansion of the device, and subsequent bond-wire lift-off or solder-cracks are dominant failure mechanisms in power converters [61]. Therefore, precise models and tools are crucial for correct converter optimization.

One state-of-the-art tool for simulating non-linear thermal behaviour is PLECS [2] [18]. Starting from a given initial condition, it solves the differential equations for all system-states step by step. To do this, PLECS describes the circuit as a set of statespace matrices denoting the change in electric quantities of all passive components, for all possible switching states of semiconductors. To reduce the matrix size and accelerate computation, PLECS can decouple parts of circuits where possible. More detailed information is given in [47].

While PLECS is faster than traditional time-based simulation, a search through a vast solution space still takes a significant amount of time, as several full thermal cycles need to be simulated per parameter set until a steady state can be determined. This chapter presents a direct solution which includes temperature dependence, to significantly improve the speed of optimization routines.

### 2.2 Junction temperature calculation

The basis for the presented method is the equation for the junction temperature of a device $T_{\mathrm{j}}(t)$, given time-varying conduction losses $P_{\mathrm{c}}(t)$ and switching losses $P_{\mathrm{sW}}(t)$ over time. The device is cooled through a thermal network with a given thermal impulse response $z_{\text {th }}(t)$, connected to the ambient temperature $T_{\mathrm{amb}}$. The device's junction temperature is then given by

$$
\begin{equation*}
T_{\mathrm{j}}(t)=T_{\mathrm{amb}}+z_{\mathrm{th}}(t) *\left(P_{\mathrm{c}}(t)+P_{\mathrm{sw}}(t)\right), \tag{2.1}
\end{equation*}
$$

where $*$ represents a convolution between the thermal impulse response $z_{\text {th }}(t)$ and the losses in the transistor. Transformed to the frequency domain, the convolution becomes a multiplication of the thermal impedance $Z_{\text {th }}(j \omega)$ and the loss spectrum, expressed as

$$
\begin{equation*}
T_{\mathrm{j}}(j \omega)=T_{\mathrm{amb}}+Z_{\mathrm{th}}(j \omega)\left(P_{\mathrm{c}}(j \omega)+P_{\mathrm{sw}}(j \omega)\right) \tag{2.2}
\end{equation*}
$$

The goal is to obtain the device temperature

$$
\begin{equation*}
T_{\mathrm{j}}(t)=\sum_{k=-N}^{N} T_{\mathrm{j}}\left(j \omega_{0} k\right) e^{j k \omega_{0} t} \tag{2.3}
\end{equation*}
$$

from the temperature spectrum, where each component corresponds to discrete frequencies $k \omega_{0}$. This approach, known as harmonic balance, is commonly used to solve nonlinear circuits in microwave and analog RF applications. The underlying assumption is that any sinusoidal current will only cause harmonics at integer multiples of its own frequency. This assumption allows to express each Fourier coefficient of the temperature as a linear combination of the dissipated power and thermal impedance.


Figure 2.2 Cauer network used to model the thermal path from device junction to ambient.

Only a finite set of $N$ harmonics needs to be considered, as the devices thermal network acts as a low pass and higher harmonics tend towards zero. The procedure will generate a system of linear equations for this finite set of harmonics, involving the thermal network, conduction losses and switching losses of the device, including their temperature dependence. First, each of these quantities is evaluated at discrete time steps spanning one load cycle $T_{\mathrm{O}}$, in steps of $T_{\mathrm{o}} / \mathrm{N}$. By transferring them to the Fourier domain, a solution for the temperature of the device can be obtained.

### 2.2.1 Vector notation

To solve the set of linear equations, the discrete Fourier coefficients of each series are written as a vector

$$
\vec{T}_{\mathrm{j}}=\left(\begin{array}{lllll}
\ldots & T_{\mathrm{j}}[-1] & T_{\mathrm{j}}[0] & T_{\mathrm{j}}[1] & \ldots \tag{2.4}
\end{array}\right)^{T},
$$

such that the center element corresponds to the average component at zero frequency. Components to the right correspond to positive $k$ and components to the left to negative $k$. The same representation can be used for other quantities of the inverter, such as the thermal impedance $\overrightarrow{Z_{\mathrm{th}}}$ or the device losses $\vec{P}_{\mathrm{c}}$ and $\overrightarrow{P_{\mathrm{sw}}}$. Using this vector notation, and by writing the thermal impedance as a diagonal matrix of the discrete coefficients $Z_{\text {th }}=\operatorname{diag}\left(\overrightarrow{Z_{\text {th }}}\right)$, the discrete form of (2.2) can be written as

$$
\begin{equation*}
\vec{T}_{\mathrm{j}}=\overrightarrow{T_{\mathrm{amb}}}+\mathbf{Z}_{\mathrm{th}}\left[\vec{P}_{\mathrm{c}}\left(T_{\mathrm{j}}\right)+\overrightarrow{P_{\mathrm{sw}}}\left(T_{\mathrm{j}}\right)\right] \tag{2.5}
\end{equation*}
$$

### 2.2.2 Thermal network

Each transistor has a thermal path from junction to ambient, which describes the thermal response to the power dissipated in the junction. A cauer network can be used to model this path, as depicted in Figure 2.2. Each of the consecutive RC elements can model individual layers within the device or external layers, such as the electric insulation from the device to the heatsink or the heatsink's resistance to


Figure 2.3 Inductor current of a half-bridge. The current ripple is centred around the load current $i_{\text {out }}$ and stays between an envelope of $\Delta i_{\mathrm{d}}$, dictated by the supply voltage, output inductance, switching frequency and duty ratio.
ambient temperature. As described in [16], the transfer function of this network can be expressed as

$$
\begin{equation*}
Z_{\mathrm{th}}(j \omega)=\frac{1}{j \omega C_{\mathrm{th}_{0}}+\frac{1}{R_{\mathrm{th}_{0}}+\frac{1}{j \omega C_{\mathrm{th}_{1}}+\frac{1}{\mathrm{Rth}_{1}+\ldots}}}} . \tag{2.6}
\end{equation*}
$$

### 2.2.3 Conduction losses

The calculation of the conduction losses is based on a two-dimensional lookup table (LUT), which returns the device forward voltage for a given temperature and load current. The LUT is used to obtain the losses for ambient temperature, by means of simple evaluation, as well as a temperature dependent component by linear interpolation. For simplicity of the loss calculation, the device temperature is assumed to be constant within one switching cycle, which is reasonable given that typical switching frequencies are significantly above the thermal network's cut-off frequency.

To begin, the device current is modelled as the sum of the modulated output current $i_{\text {out }}[t]$ and the superimposed current ripple, as depicted in Figure 2.3. The load


Figure 2.4 Device current, voltage and resulting losses during one switching period. Due to the zero crossing of the load current, the average losses can be calculated as two separate sections marked in red and blue.
current can be of arbitrary shape over a period of $T_{0}$, controlled by the modulating the duty ratio $d[t]$ of the half-bridge. Furthermore, it is assumed that the output capacitor completely filters the inductor current ripple, while maintaining constant output voltage within one switching period. The amplitude of the current ripple can now be written as

$$
\begin{equation*}
\Delta i_{\mathrm{L}}[t]=T_{\mathrm{sw}} d[t] \frac{\left(v_{\mathrm{in}}-v_{\mathrm{out}}[t]\right)}{L} \tag{2.7}
\end{equation*}
$$

given that input and output voltage remain constant within one switching cycle. As the high-side device turns on, the drain-source current $i_{\text {ds }}$ will rise from $i_{\text {on }}[t]=$ $i_{\text {out }}[t]-\Delta i_{\mathrm{L}}[t] / 2$ towards $i_{\text {off }}[t]=i_{\text {out }}[t]+\Delta i_{\mathrm{L}}[t] / 2$. It crosses the load current $i_{\text {out }}[t]$ at half-of the conduction interval, as depicted in Figure 2.4. The corresponding device forward voltage is found using the look-up table $V_{\mathrm{ds}}\left(i_{\mathrm{ds}}, T_{\mathrm{amb}}\right)$. The losses for ambient temperature are the product of the two functions for voltage and current, such that

$$
\begin{equation*}
P_{\mathrm{ds}}\left(i_{\mathrm{ds}}, T_{\mathrm{amb}}\right)=i_{\mathrm{ds}} V_{\mathrm{ds}}\left(i_{\mathrm{ds}}, T_{\mathrm{amb}}\right) \tag{2.8}
\end{equation*}
$$

The average losses per switching period $T_{\text {SW }}$ can be found by integrating this function and averaging the result over the period.

The integral is found using Simpson's rule [13], which gives an exact solution for second order polynomials provided values at the integral's start $a$, center $a+b / 2$ and end $b$ of a second order polynomial $f(x)$, such that

$$
\begin{equation*}
\int_{a}^{b} f(x) d x=\frac{b-a}{6}\left(f(a)+4 f\left(\frac{a+b}{2}\right)+f(b)\right) . \tag{2.9}
\end{equation*}
$$

The calculation is done in two individual sections, to account for a zero crossing of the current, as indicated in Figure 2.4 in blue and red.

In case of $i_{\text {on }}<0<i_{\text {off }}$, the time duration of the sections can be calculated as

$$
\begin{equation*}
T_{\mathrm{blue}}[t]=\frac{i_{\mathrm{on}}[t]}{\frac{d i_{\mathrm{ds}}}{d t}}=d[t] T_{\mathrm{sw}} \frac{i_{\mathrm{on}}[t]}{i_{\mathrm{on}}[t]-i_{\mathrm{off}}[t]} \tag{2.10}
\end{equation*}
$$

and

$$
\begin{equation*}
T_{\mathrm{red}}[t]=\frac{i_{\mathrm{off}}[t]}{\frac{d i_{\mathrm{ds}}}{d t}}=d[t] T_{\mathrm{sw}} \frac{i_{\mathrm{off}}[t]}{i_{\mathrm{off}}[t]-i_{\mathrm{on}}[t]} \tag{2.11}
\end{equation*}
$$

Applying simpson's rule to (2.8) and averaging over one switching period $T_{\mathrm{sw}}$, the ambient conduction losses are

$$
\begin{align*}
P_{\mathrm{c}, \mathrm{amb}}[t] & =\underbrace{\frac{d[t]}{6} \frac{i_{\mathrm{on}}[t]}{i_{\mathrm{on}}[t]-i_{\mathrm{off}}[t]}\left(P_{\mathrm{ds}}\left(i_{\mathrm{on}}[t], T_{\mathrm{amb}}\right)+4 P_{\mathrm{ds}}\left(i_{\mathrm{on}}[t] / 2, T_{\mathrm{amb}}\right)+0\right)}_{\text {blue area }} \\
& +\underbrace{\frac{d[t]}{6} \frac{i_{\mathrm{off}}[t]}{i_{\mathrm{off}}[t]-i_{\mathrm{on}}[t]}\left(0+4 P_{\mathrm{ds}}\left(i_{\mathrm{off}}[t] / 2, T_{\mathrm{amb}}\right)+P_{\mathrm{ds}}\left(i_{\mathrm{off}}[t], T_{\mathrm{amb}}\right)\right)}_{\text {red area }} \tag{2.12}
\end{align*}
$$

Due to the assumption of linear rising current, the interval length of each area is proportional to either $i_{\text {on }}[t]$ or $i_{\text {off }}[t]$, and the center point of each section is where the current reaches $i_{\text {on }}[t] / 2$ or $i_{\text {off }}[t] / 2$. For cases with no zero crossing of the current, the calculation simplifies significantly, as depicted in Figure 2.5.

For $i_{\text {on }}<i_{\text {off }}<0$ or $0<i_{\text {on }}<i_{\text {off }}$, the losses are

$$
\begin{equation*}
P_{\mathrm{c}, \mathrm{amb}}[t]=\frac{d[t]}{6}\left(P_{\mathrm{ds}}\left(i_{\mathrm{on}}[t], T_{\mathrm{amb}}\right)+4 P_{\mathrm{ds}}\left(I_{\mathrm{L}}[t], T_{\mathrm{amb}}\right)+P_{\mathrm{ds}}\left(i_{\mathrm{off}}[t], T_{\mathrm{amb}}\right)\right) . \tag{2.13}
\end{equation*}
$$

In this case, the interval length is the entire conduction period, and the value at the center of the interval corresponds to the load current $I_{\mathrm{L}}[t]$. Using (2.12) and (2.13) the conduction losses are obtained for each switching cycle on a case by case basis, as if the device were at ambient temperature.


Figure 2.5 Device current, voltage and resulting losses during one switching period for (a) completely negative current and (b) completely positive current. Due to the absence of a zero crossing in the device current, the losses can be directly evaluated as one area using simpson's rule.

To include the temperature dependence, a second-order temperature-dependent polynomial is fitted to the lookup table, with arbitrary functions $f_{v}\left(i_{\mathrm{ds}}\right)$ for the device current, such that

$$
\begin{equation*}
V_{\mathrm{ds}}\left(i_{\mathrm{ds}}, T_{\mathrm{j}}\right)=V_{\mathrm{ds}}\left(i_{\mathrm{ds}}, T_{\mathrm{amb}}\right)+f_{v_{1}}\left(i_{\mathrm{ds}}\right) \Delta T_{\mathrm{j}}+f_{v_{2}}\left(i_{\mathrm{ds}}\right) \Delta T_{\mathrm{j}}^{2} \tag{2.14}
\end{equation*}
$$

where $\Delta T_{\mathrm{j}}$ is the temperature difference towards $T_{\mathrm{amb}}$. For a given silicon-carbide device (C3M0065100K) used as an example, the two functions are chosen as

$$
\begin{equation*}
f_{v_{1}}\left(i_{\mathrm{ds}}\right)=26.82 \mu \mathrm{~V} / \mathrm{pA} i_{\mathrm{ds}}+319.45 \frac{\mathrm{nV}}{\mathrm{~A}^{2}} i_{\mathrm{ds}}^{2}+23.23 \frac{\mathrm{nV}}{\mathrm{~A}^{3}} i_{\mathrm{ds}}^{3} \tag{2.15}
\end{equation*}
$$

and

$$
\begin{equation*}
f_{v_{2}}\left(i_{\mathrm{ds}}\right)=1.41 \frac{\mu \mathrm{~V}}{\mathrm{~A}} i_{\mathrm{ds}}+0.96 \frac{\mathrm{pV}}{\mathrm{~A}^{4}} i_{\mathrm{ds}}^{4} . \tag{2.16}
\end{equation*}
$$

The fit from the resulting functions is depicted in Figure 2.6 in addition to the data from the look-up table for the example device. Visualized for $25^{\circ} \mathrm{C}$ and $150^{\circ} \mathrm{C}$, the voltage fit (dashed line) matches the table data, when multiplied by the temperature difference and added to the voltage at $25^{\circ} \mathrm{C}$.

Now, analogue to (2.12) and (2.13), the linear and quadratic dependencies can be formulated as $P_{\mathrm{c}, 1}[t]$ and $P_{\mathrm{c}, 2}[t]$, proportional to the linear or square of the temperature


Figure 2.6 Forward voltage and polynomial fit for a $1000 \mathrm{~V} 65 \mathrm{~m} \Omega$ SiC transistor (C3M0065100K).
difference. The temperature dependent conduction losses can then be expressed as

$$
\begin{equation*}
P_{\mathrm{c}}[t]=P_{\mathrm{c}, \mathrm{amb}}[t]+P_{\mathrm{c}, 1}[t] \Delta T_{\mathrm{j}}[t]+P_{\mathrm{c}, 2}[t] \Delta T_{\mathrm{j}}[t]^{2} . \tag{2.17}
\end{equation*}
$$

From this expression in the time domain, the spectrum of the conduction losses can be obtained through a Fourier transform, yielding

$$
\begin{equation*}
\left.P_{\mathrm{c}}[j \omega]=P_{\mathrm{c}, \mathrm{amb}}[j \omega]+\left(P_{\mathrm{c}, 1}[j \omega]+P_{\mathrm{c}, 2}[j \omega] * \Delta T_{\mathrm{j}}[j \omega]\right]\right) * \Delta T_{\mathrm{j}}[j \omega] . \tag{2.18}
\end{equation*}
$$

Using the vector notation described in section 2.2.1, the coefficients of the conduction loss spectrum can be formulated as

$$
\begin{equation*}
\vec{P}_{\mathrm{C}}=\vec{P}_{\mathrm{c}, 0}+\boldsymbol{P}_{\mathbf{c}, \mathrm{T}} \Delta \vec{T}_{\mathrm{j}}, \tag{2.19}
\end{equation*}
$$

where $\boldsymbol{P}_{\mathbf{c}, \mathbf{T}}$ is a Toeplitz matrix ${ }^{1}$ built from

$$
\begin{equation*}
\vec{P}_{\mathrm{c}, \mathrm{~T}}=\vec{P}_{\mathrm{c}, 1}+\vec{P}_{\mathrm{c}, 2} * \Delta \vec{T}_{\mathrm{j}} \tag{2.20}
\end{equation*}
$$

Multiplication of a vector with a Toeplitz matrix carries out the convolution of two discrete Fourier series. $\boldsymbol{P}_{\mathbf{c}, \mathbf{T}}$ still contains the unknown junction temperature resulting from the second-order terms. This issue is addressed by assuming $\vec{T}_{\mathrm{j}}=\vec{T}_{0}$ for the initial calculation of $\boldsymbol{P}_{\mathbf{c}, \mathbf{T}}$ and $\vec{T}_{\mathrm{j}}$, and a subsequent second iteration with the resulting $\vec{T}_{\mathrm{j}}$. Further iteration is possible to improve the results. However, for the example device, based on observation of the difference in temperature only little benefit is found for more than two iterations.


Figure 2.7 Turn-on energy of the example SiC transistor at 700 V . The fit is only valid for positive turn-on currents. For correct calculation of the switching losses over the fundamental period, the polynomial is multiplied with a boolean function which is zero at times of negative turn-on current.

### 2.2.4 Switching losses

The switching losses are the sum of the switching energies which are dissipated in the device each switching cycle at turn-on and turn-off. Again, due to the low pass behaviour of the thermal network, the nearly impulse-like switching energy can be averaged over one cycle, yielding

$$
\begin{equation*}
P_{\mathrm{sw}}[t]=f_{\mathrm{sw}}\left(E_{\mathrm{on}}[t]+E_{\mathrm{off}}[t]\right) \tag{2.21}
\end{equation*}
$$

For brevity, this section only covers the derivation of the turn-on losses $E_{\text {on }}[t]$. The turn-off losses $E_{\text {off }}[t]$ are obtained using the same methodology and the resulting equations are listed at the end.

The turn-on losses depend on the device current at the beginning of the conduction interval, previously established as $i_{\text {on }}[t]$. Depending on the direction of this current, the device will either experience a hard-switched commutation, dissipating a significant amount of energy, or a soft commutation with little to no energy loss. For a given device, the losses for set of currents and junction temperatures are listed in a look-up table $E_{\text {on }}\left(i_{\mathrm{ds}}, T_{\mathrm{j}}\right)$. For the calculation with harmonic balance, similar as with the conduction losses, the turn-on losses are formulated as an ambient component

$$
\begin{equation*}
E_{\mathrm{on}, \mathrm{amb}}[t]=E_{\mathrm{on}}\left(i_{\mathrm{on}}[t], T_{\mathrm{amb}}\right), \tag{2.22}
\end{equation*}
$$

obtained directly through the loss table.

[^2]

Figure 2.8 Turn-off energy of the SiC transistor at 700 V . The fit is only valid for positive turn-off currents. For correct calculation of the switching losses over the fundamental period, the polynomial is multiplied with a boolean function which is zero at times of negative turn-off current.

To include the temperature dependence, an arbitrary function $f_{E_{\mathrm{on}}}\left(i_{\mathrm{ds}}\right)$ is fitted, such that

$$
\begin{equation*}
E_{\mathrm{on}}\left(i_{\mathrm{ds}}, T_{\mathrm{j}}\right)=E_{\mathrm{on}}\left(i_{\mathrm{ds}}, T_{\mathrm{amb}}\right)+f_{E_{\mathrm{on}}}\left(i_{\mathrm{ds}}\right) \Delta T_{\mathrm{j}} \tag{2.23}
\end{equation*}
$$

For the example device the function is chosen to be

$$
\begin{equation*}
f_{E_{\mathrm{on}}}\left(i_{\mathrm{ds}}\right)=37.4 \frac{\mathrm{~nJ}}{\sqrt{\mathrm{~A}}} i_{\mathrm{ds}}^{0.5}-5.77 \frac{\mathrm{~nJ}}{\mathrm{~A}} i_{\mathrm{ds}}+0.15 \frac{\mathrm{~nJ}}{\mathrm{~A}^{2}} i_{\mathrm{ds}}^{2}-1.15 \frac{\mathrm{pJ}}{\mathrm{~A}^{3}} i_{\mathrm{ds}}^{3} \tag{2.24}
\end{equation*}
$$

with the result depicted in Figure 2.7.
As most turn-on loss models have zero losses for soft-commutation, the fit $f_{E_{\mathrm{on}}}\left(i_{\mathrm{ds}}\right)$ only needs to be correct for positive turn-on currents. To eliminate any wrong values at negative turn-on currents, the resulting energy is multiplied with a boolean function

$$
B_{\mathrm{on}}\left[i_{\mathrm{on}}\right]= \begin{cases}1, & \text { for } i_{\mathrm{on}} \geq 0  \tag{2.25}\\ 0, & \text { otherwise }\end{cases}
$$

zeroing all values when the inverter is operating in soft-commutation. The turn-on losses over time can then be expressed as

$$
\begin{equation*}
E_{\text {on }}[t]=E_{\text {on }, \mathrm{amb}}[t]+\underbrace{E_{\text {on, }}[t]}_{B_{\text {on }}[t] f_{E_{\text {on }}}\left(i_{\text {on }}[t]\right)} \Delta T_{\mathrm{j}}[t], \tag{2.26}
\end{equation*}
$$

which can be transformed into the frequency domain as

$$
\begin{equation*}
E_{\mathrm{on}}(j \omega)=E_{\mathrm{on}, \mathrm{amb}}(j \omega)+E_{\mathrm{on}, \mathrm{~T}}(j \omega) * \Delta T_{\mathrm{j}}(j \omega) \tag{2.27}
\end{equation*}
$$

Analog to the conduction loss calculation, the vector form of the turn-on loss spectrum is obtained by construction of a convolution matrix $\boldsymbol{E}_{\mathbf{o n}, \mathrm{T}}$ from the temperature dependent spectrum $E_{\text {on, }}(j \omega)$, resulting in

$$
\begin{equation*}
\overrightarrow{E_{\mathrm{on}}}=E_{\mathrm{on}, \mathrm{amb}}+E_{\mathrm{on}, \mathrm{~T}} \overrightarrow{\Delta T_{\mathrm{j}}} . \tag{2.28}
\end{equation*}
$$

The same steps can be followed to obtain the expression

$$
\begin{equation*}
\overrightarrow{E_{\mathrm{off}}}=E_{\mathrm{off}, \mathrm{amb}}+E_{\mathrm{off}, \mathrm{~T}} \overrightarrow{\Delta T_{\mathrm{j}}}, \tag{2.29}
\end{equation*}
$$

for the turn-off losses, using the turn-off current $i_{\text {off }}$, its corresponding look-up table and boolean function $B_{\text {off. }}$. The example device is fitted with the function

$$
\begin{equation*}
f_{E_{\mathrm{off}}}\left(i_{\mathrm{ds}}\right)=-17 \frac{\mu \mathrm{~J}}{\sqrt{\mathrm{~A}}} i_{\mathrm{ds}}^{0.5}+4.7 \frac{\mu \mathrm{~J}}{\mathrm{~A}} i_{\mathrm{ds}}-0.1 \frac{\mathrm{~nJ}}{\mathrm{~A}^{2}} i_{\mathrm{ds}}^{2}+0.42 \frac{\mathrm{pJ}}{\mathrm{~A}^{3}} i_{\mathrm{ds}}^{3} \tag{2.30}
\end{equation*}
$$

and the result is depicted in Figure 2.8. The turn-on and turn-off energies can be collected in a single term for switching losses, such that

With all loss components modelled in vector format, the equation for the discrete junction temperature (2.5) can be solved.

### 2.2.5 Solving for the junction temperature

Using the conduction losses (2.19) and switching losses (2.31), (2.2) can be rewritten into

$$
\begin{equation*}
\vec{T}_{\mathrm{j}}=\vec{T}_{0}+\boldsymbol{Z}_{\mathrm{th}}\left(P_{\mathrm{c}, \mathrm{amb}}+\boldsymbol{P}_{\mathbf{c}, \mathbf{T}} \overrightarrow{\Delta T_{\mathrm{j}}}+\vec{P}_{\mathrm{sw}, 0}+\boldsymbol{P}_{\mathbf{s w}, \mathbf{T}} \overrightarrow{\Delta T_{\mathrm{j}}}\right) \tag{2.32}
\end{equation*}
$$

The terms proportional to $\Delta \vec{T}_{\mathrm{j}}$ can be collected to obtain

$$
\begin{equation*}
\vec{T}_{\mathrm{j}}=\vec{T}_{0}+\mathbf{Z}_{\mathrm{th}}\left(P_{\mathrm{c}, \mathrm{amb}}+\vec{P}_{\mathrm{sw}, 0}\right)+\mathbf{Z}_{\mathrm{th}}\left(\boldsymbol{P}_{\mathbf{c}, \mathbf{T}}+\boldsymbol{P}_{\mathrm{sw}, \mathbf{T}}\right) \overrightarrow{\Delta T_{\mathrm{j}}} \tag{2.33}
\end{equation*}
$$

Subsequent subtraction and inversion of these terms yield

$$
\begin{equation*}
\overrightarrow{\Delta T_{\mathrm{j}}}=\vec{T}_{\mathrm{j}}-\vec{T}_{0}=\left[\boldsymbol{I}-\mathbf{Z}_{\mathrm{th}}\left(\boldsymbol{P}_{\mathbf{c}, \mathbf{T}}+\boldsymbol{P}_{\mathbf{s w}, \mathbf{T}}\right)\right]^{-1}\left[\vec{T}_{0}+\boldsymbol{Z}_{\mathrm{th}}\left(P_{\mathrm{c}, \mathrm{amb}}+\vec{P}_{\mathrm{sw}, 0}\right)\right] \tag{2.34}
\end{equation*}
$$

the solution for the junction temperature.

Table 2.1 Inverter parameters

| Parameter | Symbol | Value |
| :---: | :---: | :---: |
| Switching frequency | $f_{\mathrm{sw}}$ | 30 kHz |
| Output frequency | $f_{\mathrm{o}}$ | 50 Hz |
| Supply voltage | $v_{\text {in }}$ | 700 V |
| Grid voltage | $v_{\text {out }}$ | 230 Vrms |
| Transistors | $Q_{1}, Q_{2}$ | C 3 M 0065100 K |
| Output current | $I_{\mathrm{o}}$ | 16 Arms |
| Output inductor | $L$ | $600 \mu \mathrm{H}$ |
| Ambient temperature | $T_{0}$ | $40{ }^{\circ} \mathrm{C}$ |
| External thermal interface | $R_{\mathrm{th}}, C_{\text {th }}$ | $1 \frac{\mathrm{~K}}{\mathrm{~W}}, 0.05 \mathrm{~J} \mathrm{~K}$ |

### 2.3 Results

For demonstration, the junction temperature of a grid inverter is calculated, with the circuit parameters and components specified in Table 2.1. The results obtained through harmonic balance are compared to simulations done in PLECS, which is considered the ground truth in the evaluation. The temperature is obtained through PLECS' steady-state tool at standard settings. Both the harmonic balance method and PLECS use the same look-up table for the device losses, available from the device manufacturer. Thus any discrepancy can be entirely addressed to the proposed method. For now, both simulation and calculation do not include dead-time, which can become a noticeable contributor to losses at higher switching frequencies [1]. Next to additional losses, dead-time leads to distortion in the output voltage of the inverter [80], which would result in different current ripple and modulation of the device, hindering a direct comparison between calculation and simulation. Figure 2.9 shows the obtained temperature and losses for the high-side switch of the inverter. The results from harmonic balance are compared against a reference simulation in PLECS. Already a very low number of harmonics $\mathrm{N}=16$ yields good accuracy in power losses and temperature. For a higher number of harmonics the calculated temperature approaches the shape of the simulated reference, but at a slight offset. The difference in average temperature can be explained by the slightly lower peak conduction losses. Still, the rest of the curve matches well with simulation results. The switching losses also show very good agreement, with a slight improvement at larger $N$ for the discontinuous sections, where the device enters soft-commutation. To show how the proposed method can be used for fast evaluation and design of inverters, the next section will explore a multitude of operating points for a grid inverter, again using PLECS as reference, for both accuracy as well as computation time.


Figure 2.9 Results obtained with harmonic balance (dashed lines) compared to simulation in PLECS (solid line). $N$ denotes the number of harmonics used for harmonic balance.

### 2.3.1 Verification through design space simulation

To demonstrate the speed and accuracy of the proposed method, the grid-inverter is analysed by search through a vast design space. This space, given in Table 2.2, spans different load currents, switching frequencies, as well as different filter sizes, yielding a total of 1014 possible combinations. As an application example, the load current is stepped through the profile of the European Efficiency for solar inverters, given by

$$
\begin{equation*}
\eta_{\text {euro }}=0.03 \eta_{5 \%}+0.06 \eta_{10 \%}+0.13 \eta_{15 \%}+0.10 \eta_{30 \%}+0.48 \eta_{50 \%}+0.20 \eta_{100 \%} \tag{2.35}
\end{equation*}
$$

where $\eta_{\mathrm{x}}$ is the inverter efficiency at the indicated percentage $x$ of the maximum load current. For simplicity, the inductive component is treated as lossless, yet its impact on the semiconductor losses is considered.

Table 2.2 Design space and runtime of simulation

| Parameter | Symbol | Value | Steps |
| :---: | :---: | :---: | :---: |
| Line frequency | $f_{\mathrm{g}}$ | 50 Hz | - |
| Line voltage | $v_{\mathrm{a}, \mathrm{b}, \mathrm{c}}$ | 230 VAC | - |
| Ambient temperature | $T_{\text {amb }}$ | $40^{\circ} \mathrm{C}$ | - |
| Supply voltage | $v_{\text {in }}$ | 700 V | - |
| Switching frequency | $f_{\text {sw }}$ | 10 kHz to 70 kHz | 13 |
| Line current | $I_{\text {O,rms }}$ | $\begin{gathered} 0.8 \mathrm{~A} / 1.6 \mathrm{~A} / 2.4 \mathrm{~A} \\ 4.8 \mathrm{~A} / 8 \mathrm{~A} / 16 \mathrm{~A} \end{gathered}$ | 6 |
| Output Inductor | $L$ | $400 \mu \mathrm{H}$ to $1000 \mu \mathrm{H}$ | 13 |
| Transistors | $Q_{1 \ldots 6}$ | C3M0065100K | - |
| Total number of simulations |  | 1014 |  |
| Runtime PLECS 4.6.5 |  | 18 min 23 s |  |
| Runtime Harm. Balance ( $\mathrm{N}=32$ ) |  | 0 min 11 s |  |
| Runtime Harm. Balance ( $\mathrm{N}=64$ ) |  | 0 min 18 s |  |
| Runtime Harm. Balance ( $\mathrm{N}=128$ ) |  | 0 min 46 s |  |

### 2.3.2 Simulation and calculation setup

Within PLECS, the steady-state analysis tool is used to obtain the device temperature and losses of a single grid cycle. For a fair comparison, both PLECS and the harmonic balance method are run on the same machine (Intel Core i5-7500), as single threaded applications. In a practical scenario, paralleled computing can be used to significantly reduce the absolute computation time of both methods. To evaluate each method's computation time, and not the machine's disk speed, both methods are run without saving of the time domain waveforms, as this significantly affects the time spent by each method. Moreover, the time PLECS takes is extremely dependent on tolerances and other settings. Thus, PLECS is kept at the default parameters preset after installation.

### 2.3.3 Results and analysis

The runtime of each program is listed in Table 2.2, with PLECS taking 18 min 23 s to analyze all 1014 possible circuit variations. In contrast, harmonic balance run at $N=32$ harmonics finishes after 11 s . For slightly higher accuracy, the number of harmonics can be increased to $N=128$, which leads to a computation time of 46 s , still considerably faster than PLECS. The calculation results are shown in Figure 2.10. For each current, the upper plot shows the average junction temperature over one fundamental cycle obtained with harmonic balance.


Figure 2.10 Calculation results of a grid-tied inverter, obtained using harmonic balance ( $\mathrm{N}=128$ ). The load current ranges from 0.8 A to 16 A . Each stack of plots displays the average device temperature over one grid cycle and the respective rms error towards the simulation result.


Figure 2.11 Calculation result of a grid-tied inverter, obtained using harmonic balance ( $\mathrm{N}=128$ ). The plots depict the average conduction and switching losses at a load current of 16 A , as well as their respective rms error towards the simulation results.

To quantify how close the calculation is to simulation, the plot below shows the respective rms error in temperature, calculated by

$$
\begin{equation*}
\text { Error }_{\text {RMS }}=\sqrt{\frac{1}{T_{0}} \int_{0}^{T_{0}}\left(T_{\mathrm{j}, \text { PLECS }}[t]-T_{\mathrm{j}, \text { Harm.Balance }}[t]\right)^{2} d t} \tag{2.36}
\end{equation*}
$$

For all operating points, the error stays well below $1^{\circ} \mathrm{C}$. Figure 2.11 shows the conduction and switching losses at a load current of 16 A and their respective rms error to PLECS. Again, the error stays below $1^{\circ} \mathrm{C}$ and 1 W respectively. At low inductance and low switching frequency, the high current ripple leads to increased conduction losses. Increasing the switching frequency reduces the conduction losses at first, at a cost of increased switching losses. By further increasing the switching frequency, the feedback effect mentioned in section 2.1 sets in: the increased switching losses heat the device, resulting in higher on-state resistance, and thus more conduction losses.

### 2.4 Conclusion

The calculation of device temperature using harmonic balance offers a fast, precise alternative to iterative steady-state solvers, which includes temperature dependence and saturation present in commonly available transistor loss models. The results match simulations obtained with commercial state-of-the-art steady-state solvers within an rms error of $1 \%$. The remaining error likely results from the use of simpson's rule for integration of the conduction losses. As it is implemented, the method assumes an underlying polynomial function, the product of linear rising current and linear voltage. Saturation is partly accounted for, by using the values from the LUT including saturation. However, the shape during interval might differ. Evaluation of the conduction losses using more points along the interval might reduce the remaining error. The steady state is calculated given a temperature dependent look-up table for the device losses available from the manufacturer, as well as the device current and duty ratio. For well known topologies, these operating parameters are easily written analytically. Otherwise, harmonic balance could serve as an addition to steady-state solvers, producing a solution after the device operating parameters are obtained through a first simulation cycle.

In combination with analytic loss models such as [20], it could enable fast, fully analytic evaluation of a power stage solely from the transistor datasheet. Next to thermal design of the inverter, the obtained temperature cycles can serve as input for life-time estimations [23]. State-of-the-art calculation methods for inductor and capacitor losses could be added to optimize the complete system [41,46]. With lifetime prediction methods based on mapping steady-state cycle simulations, such as [12], harmonic balance could further increase the evaluation speed. Beyond design of inverters, a possible application of harmonic balance could be over-temperature protection. Given that harmonic balance only requires standard matrix functions, it could be implemented on capable DSPs used to control the inverter. As the calculation produces the inverter's steady-state response, the controller could predict over-temperature of the transistors, before their thermal network reaches the undesired operating point and limit the load current to prevent this. Several aspects of the presented method can be improved for more accurate results and universal application. As previously addressed, dead-time was omitted to simplify the analytic description of the inverter's output voltage and to limit potential error sources. For future work, dead-time losses need to be added as a term proportional to the switching frequency, including load current and temperature dependence. Furthermore, the conduction losses are calculated assuming a triangular output current, as is the case for PWM inverters or buck/boost converters. To extend application of the harmonic-balance calculation method to other topologies, different current ripple has to be modelled, such as sinusoidal waveforms for resonant converters, or trapezoidal waveforms for active-bridge converters.

The next chapter investigates possible implementations of the transistor's thermal network, with a focus on the often required electric insulation. Specifically for widebandgap devices, this insulation barrier can lead to unwanted parasitic behaviour, with an effect on the losses, and ultimately temperature of the inverter, next to potential electromagnetic interference issues.

## $B$ <br> Thermal interfaces for wide-bandgap devices

> "Any experienced electronics technician will tell you that magic smoke is what really makes electronics work - when the magic smoke comes out of a part, it stops working.'

John R. Barnes

TlHE junction temperature of a transistor is one of the parameters which limits the performance of a power-electronic amplifier. At a certain point, the output current and switching frequency have to be limited to keep the transistors within an acceptable maximum temperature or to limit their temperature swing. The previous chapter answered the question on how to obtain the junction temperature of a transistor given the inverter operating parameters and the thermal interface. Now, the latter of the two will be investigated in detail. This chapter focuses on a GaN half-bridge mounted to a heat-sink with an electrically insulating thermal interface. Due to the high switching speeds of GaN , significant currents are induced through this interface. Thus proper material selection and dimensioning of the insulation layer are key in keeping this effect to a minimum while retaining low thermal resistance.


Figure 3.1 (a) Half-bridge attached to heatsink through an insulating thermal interface. The insulation layer creates a parasitic capacitance towards the heatsink. (b) Simplified model of thermal interface. Each layer is represented by a single thermal resistance, dictated by layer thickness and area.

### 3.1 Thermal interface for a half-bridge

Figure 3.1(a) shows a GaN half-bridge mounted to a heatsink. The interface between the heatsink and devices acts as a thermal conductor and an electric insulator. The total thermal resistance can be modelled as a series connection of several components, which includes the chip's packaging, insulation layer and remaining interface layers, such as an aluminium baseplate as depicted in Figure 3.1(b).

Next to the thermal path, the insulation layer creates an electrical capacitance between each device's cooling surface and the heatsink. In most discrete GaN FETs, the cooling surface is internally connected to the source terminal [68]. In case of the high-side device, the source terminal is the half-bridges switching node. Thus, the parasitic capacitance of the high-side device experiences fast switching transients. While the transient induces current through the high-side parasitic, both devices are influenced equally, as the capacitance adds a charge to the switching node. This charge is dissipated by either the low or high-side device during a hard-switched turn-on [24]. For soft-switched transitions, slightly more reactive energy is necessary to complete the commutation [37].

Figure 3.2 depicts this effect for the low-side device. The rapid change in voltage induces a current $i_{\text {par }}$ through the capacitance $C_{\text {par }}$, leading to an increased device current $i_{\mathrm{ds}}$ and increased turn-on time. The combination of these two factors potentially leads to a significant increase in switching losses, as the integral of the device dissipation, i.e. voltage current product, increases. In addition, as the parasitic current returns through the heatsink, it is likely to cause radiated emissions [26].


Figure 3.2 Simulated turn-on of a GaN half-bridge for varying parasitic capacitance on the switching node. A larger capacitance leads higher switching losses due to larger drain-source voltage and current, as well as increased current flowing through the heatsink.

Next to issues with compliance, these emissions may disturb other parts of the system. For simplicity, this chapter continues with the parasitic capacitance as the defining metric, as it is one of the determining factors for the amplitude of the return current [22]. As wide-bandgap devices typically have small package size as well as fast switching transients, it is essential to consider both thermal resistance and parasitic capacitance when choosing an insulation material.

### 3.2 Figure of merit for insulation materials

An insulating material should have two key properties: to insulate two components in the electric domain, but conduct heat between the two in the thermal domain. Given the geometry in Figure 3.1(b), the insulation material exhibits a thermal resistance from the top surface to the bottom. Given low thermal conductivity $\lambda_{\text {ins }}$ and/or thin layer height $t_{\text {ins }}$ relative to the cooling area $A_{\text {chip }}$, the heat can be assumed to traverse mostly vertically. The insulation's thermal resistance can then be approximated by

$$
\begin{equation*}
R_{\mathrm{th}, \mathrm{ins}} \approx \frac{1}{\lambda_{\mathrm{ins}}} \frac{t_{\mathrm{ins}}}{A_{\mathrm{chip}}} \tag{3.1}
\end{equation*}
$$

For now, assuming a fixed chip area and insulating material, the only way to reduce the thermal resistance is to decrease the materials thickness. Ideally, the insulation should be as thin as possible to achieve the lowest thermal resistance. Here, the limit is determined by safety standards in conjunction with the dielectric breakdown strength of the material. However, particularly for wide-bandgap devices, as thin as possible might not be the ideal configuration for the thermal interface.

As mentioned previously, next to its thermal path, the insulation adds an electric path in the form of a parasitic capacitance. This capacitance can be approximated as a parallel plate capacitor by

$$
\begin{equation*}
C_{\mathrm{par}} \approx \varepsilon_{0} \varepsilon_{\mathrm{r}} \frac{A_{\mathrm{chip}}}{t_{\mathrm{ins}}} \tag{3.2}
\end{equation*}
$$

where $\varepsilon_{\mathrm{r}}$ is the material's relative dielectric constant and $\varepsilon_{0}$ the vacuum permittivity. Given this simplified model, the capacitance is inversely proportional to the thermal resistance: a lower thermal resistance leads to a larger parasitic capacitance. Ideally, a thermal interface should have both a low thermal resistance and a small parasitic capacitance. This characteristic can be represented as the product of the two quantities, which allows to define a figure of merit (FOM) equal to

$$
\begin{equation*}
p_{\lambda \varepsilon}=R_{\mathrm{th}, \mathrm{ins}} C_{\mathrm{par}}=\frac{\varepsilon_{0} \varepsilon_{\mathrm{r}}}{\lambda_{\mathrm{ins}}} . \tag{3.3}
\end{equation*}
$$

With the assumption of solely vertical heat transfer, the geometry of the thermal interface cancels, which leads to a constant FOM for a given insulating material.

Table 3.1 Insulation materials and their figure of merit

|  | Material | $\lambda_{\text {ins }}\left[\frac{\mathrm{W}}{\mathrm{mK}}\right]$ | $\varepsilon_{\mathrm{r}} @ 1 \mathrm{MHz}$ | $p_{\lambda \varepsilon}\left[\frac{\mathrm{pFK}}{\mathrm{W}}\right]$ |
| :--- | :--- | :---: | :---: | :---: |
| Printed ciruit board | Glass/Resin | 0.25 | 4.5 | 159 |
| IMS | VT-4B1 | 1.0 | 4.8 | 42 |
| IMS | GL12 | 1.0 | 1.8 | 16 |
| IMS | VT-4B3 | 3.0 | 4.8 | 14 |
| IMS | VT-4B7 $^{2}$ | 7.0 | 4.8 | 6 |
| Aluminium-oxide | $\mathrm{Al}_{2} \mathrm{O}_{3}$ | 20 | 10.2 | 4.5 |
| Aluminium-nitride | $\mathrm{AlN}^{\text {Beryllium-oxide }}$ | BeO | 180 | 9.2 |

The FOM denotes the material's thermal resistance at a given parasitic capacitance, with the unit of $\mathrm{pFK} / \mathrm{w}$. Choosing a material with a lower FOM will offer either less thermal resistance at the same parasitic capacitance, or less capacitance at the same thermal resistance. The FOM conveniently states the parasitic capacitance at a thermal resistance of $1 \mathrm{~K} / \mathrm{w}$, or the thermal resistance at a parasitic capacitance of 1 pF . A selection of common insulation materials is listed in Table 3.1, sorted by descending figure of merit.

At the top of the list is standard PCB material, which demonstrates that electrically insulating any component through a PCB layer comes at the cost of tremendous parasitic capacitance or large thermal resistance. Next are polymer based insulation materials, ranging from $1 \mathrm{~W} / \mathrm{mK}$ to $7 \mathrm{~W} / \mathrm{mK}$. Most of the polymer based materials have relative dielectric constants of 4 to 5 . However, the material GL12 offers much better performance than its counterpart VT-4B1, which has the same thermal conductivity. Due to its lower relative dielectric constant, the FOM is nearly equal to VT-4B3, which has a three times higher thermal conductivity. Given free choice of material thickness, both materials could be used to make a thermal interface with similar properties, excluding dielectric breakdown strength.

At the bottom of the list are ceramic materials. Even the worst ceramic, aluminium oxide (Al2O3), offers similar performance as one of the higher-end polymer materials. However, moving on to aluminium-nitride (AlN), shows an improvement by a factor of ten. One of the best FOM is achieved with beryllium-oxide, further improving by a factor of three. Considering both thermal resistance and parasitic capacitance of the insulation, ceramics are the best option for achieving both good electric insulation and thermal coupling. However, the insulating layer is only part of the total thermal interface. Considering the entire thermal path from transistor junction to ambient, over-optimization of the insulation is unnecessary ${ }^{1}$.

[^3]

Figure 3.3 Simplified model of a heatspreader. The chip is attached to a larger copper surface $A_{\mathrm{Cu}}$ prior to insulation. The larger area causes the heat to spread horizontally, before passing through the insulation. The increased effectively used insulation area leads to an overall lower thermal resistance, despite the additional thermal resistance through the copper.

Moving towards practical implementation, other factors need to be considered as well, such as structural integrity, complexity or cost. While not the best in terms of parasitic capacitance, polymer solutions are available as laminated substrates. The combination of copper, polymer insulation and aluminium backing offers a good combination of accessibility, cost and ease of implementation. The copper surface can be designed to act as a heat-spreader, further improving the thermal performance of the interface, albeit at the cost of increased parasitic capacitance.

### 3.3 Heat-spreading in insulated metal substrates

Insulated metal substrates (IMS) have become a popular solution for cooling GaN devices [35], as they offer a cost-effective way of accommodating the custom surfacemount packages most GaN devices come in. Given the freedom to design the substrate's copper surface, an area larger than the chip cooling surface can be utilized to spread the heat in-plane, as depicted in Figure 3.3. This spreading creates a larger equivalent area across the polymer insulation, which yields a lower thermal resistance through this layer of relatively low thermal conductivity. Despite a typically thin layer thickness of $50 \mu \mathrm{~m}$ to $100 \mu \mathrm{~m}$, a low thermal conductivity of $3 \mathrm{~W} / \mathrm{mK}$ to $10 \mathrm{~W} / \mathrm{mK}$ can still lead to significant thermal resistance. Given the vast difference in thermal conductivity of polymers and copper, in addition to the insulation's thin layer depth, allows for significant simplifications of the heat flow.

Within the polymer, the heat essentially traverses vertically. Meanwhile, the copper offers a horizontal thermal path, to spread the heat over the entire copper area at little resistance. An analytic solution for this single layer spreading resistance was derived in [30]. The authors simplified the problem by assuming radial symmetry and solving the heat transfer in cylindrical coordinates, but proved good agreement between their solutions and simulation results, even for square geometries. The areas of the heat source $A_{\text {chip }}$ and spreader $A_{\mathrm{Cu}}$ are converted to equivalent radii as follows:

$$
\begin{equation*}
a=\sqrt{\frac{A_{\mathrm{chip}}}{\pi}}, \quad b=\sqrt{\frac{A_{\mathrm{Cu}}}{\pi}} . \tag{3.4}
\end{equation*}
$$

The solution works with dimensionless quantities and the heat source radius $a$ and spreader thickness $t_{\mathrm{Cu}}$ are normalized with the spreader radius, giving the dimensionless aspect ratios

$$
\begin{equation*}
\epsilon=\frac{a}{b}, \quad \tau=\frac{t_{\mathrm{Cu}}}{b} . \tag{3.5}
\end{equation*}
$$

The high heat-conductivity of aluminium in the base layer results in a mostly vertical heat transfer within the insulation layer, as the heat is drawn out of the polymer. The uniformity of the distribution is indicated by the Biot number, defined as

$$
\begin{equation*}
B_{\mathrm{i}}=\frac{b \lambda_{\mathrm{ins}}}{t_{\mathrm{ins}} \lambda_{\mathrm{Al}}}, \tag{3.6}
\end{equation*}
$$

with $\lambda_{\mathrm{Al}}$ and $\lambda_{\text {ins }}$ denoting the heat conductivity of aluminium and the insulation material respectively. The solution consists of empirical equations developed by the authors with the two dimensionless parameters $\lambda_{c}$ and $\Phi_{c}$, equal to

$$
\begin{equation*}
\lambda_{\mathrm{c}}=\pi+\frac{1}{\epsilon \sqrt{\pi}} \quad \text { and } \quad \Phi_{\mathrm{c}}=\frac{B_{\mathrm{i}} \tanh \left(\lambda_{\mathrm{c}} \tau\right)+\lambda_{\mathrm{c}}}{B_{\mathrm{i}}+\lambda_{\mathrm{c}} \tanh \left(\lambda_{\mathrm{c}} \tau\right)} \tag{3.7}
\end{equation*}
$$

The constriction resistance

$$
\begin{equation*}
\Psi_{\max }=\frac{\epsilon \tau}{\sqrt{\pi}}+\frac{1}{\sqrt{\pi}}(1-\epsilon) \Phi_{\mathrm{c}} \tag{3.8}
\end{equation*}
$$

can be converted to the heatspreader resistance with the conductivity of copper $\lambda_{\mathrm{Cu}}$ according to

$$
\begin{equation*}
R_{\mathrm{th}, \mathrm{cu}}=\frac{\Psi_{\max }}{a \lambda_{\mathrm{Cu}} \sqrt{\pi}} \tag{3.9}
\end{equation*}
$$

This analytic expression allows quick dimensioning of a heatspreader within an acceptable margin of error.


Figure 3.4 Thermal resistance of heatspreaders for varying copper thickness. The graph shows the combined thermal resistance of the copper and insulation layer obtained with the analytic solution (lines) and finite-element simulation(crosses). The dashed line indicates the contribution of the insulation layer to the total thermal resistance.

For verification, calculations are compared against finite element simulations for a transistor with a cooling area of $19 \mathrm{~mm}^{2}$. Figure 3.4 depicts the thermal resistance of the copper and insulation layer for increasing copper thickness. Except for thin copper, the analytic approach matches the simulation data. At larger spreader areas the analytic model predicts an increase in thermal resistance, which is physically impossible. However, simulations also show, that a spreader thickness of $35 \mu \mathrm{~m}$ provides almost no heatspreading at all. Thus, a layer of $35 \mu \mathrm{~m}$ should not be considered for a design unless the initial chip area suffices for a low enough thermal resistance. For spreading over a small area, up to a factor of two, a spreader thickness of $300 \mu \mathrm{~m}$ is sufficient. Generally, larger areas require thicker copper for sufficient heatspreading, albeit with diminishing returns. The thermal resistance can be improved by two more factors: the insulation's conductivity or its thickness, with the latter being limited by the breakdown voltage of the insulation material. Both affect the insulation resistance according to (3.1). What changes however, is the spreading capability, as the biot number (3.6) is affected inversely. The reduction of spreading capability is depicted in Figure 3.5, where the thermal resistance is plotted for varying insulation conductivities.

A higher conductivity, while directly decreasing thermal resistance, leads to reduced heatspreading. At a conductivity of $1.1 \mathrm{~W} / \mathrm{mK}$, a heat spreader with double the chip area provides an improvement from $3.3 \mathrm{~K} / \mathrm{W}$ to $1.8 \mathrm{~K} / \mathrm{W}$. In contrast, an insulation layer with a conductivity of $2.3 \mathrm{~W} / \mathrm{mK}$ only improves from $1.65 \mathrm{~K} / \mathrm{W}$ to $0.95 \mathrm{~K} / \mathrm{W}$.


Figure 3.5 Thermal resistance of heat-spreaders for varying thermal conductivity. Higher thermal conductivity reduces the effectiveness of heatspreading.

In low-power applications, it can be sufficient to choose a lower thermal conductivity and design the heat spreader accordingly, rather than going for a more conductive, but more expensive material. Moreover, a heat spreader also adds thermal capacitance, which may damp peak temperatures under transient conditions. However, any benefit from heatspreading needs to be weighed against the increased parasitic capacitance, which grows linear with area. Contrary to this linear growth, double the spreading area does not lead to half the thermal resistance. Thus the attainable ratio of thermal resistance and parasitic capacitance is above the previously established figure of merit if heat-spreading is used. As previously mentioned, neglecting this capacitance can have unforeseen impacts on switching performance, which is demonstrated with a double-pulse setup.

### 3.4 Experimental verification

The parasitic effects and analytic design methods established in the previous section were verified through experiments. A set of heat-spreaders has been designed for a GaN half-bridge, depicted in Figure 3.6. The heat-spreaders are constructed using IMS with an insulation layer thickness of $70 \mu \mathrm{~m}$ and a relative dielectric constant of 1.8. A soldered copper layer of 1 mm thickness proves sufficient heat-spreading for the larger areas, while contributing negligible vertical thermal resistance for the smaller spreaders. The backing plate is aluminium, with a thickness of 1 mm .


Figure 3.6 Heat-spreaders for the top and bottom switch of a GaN half-bridge.


Figure 3.7 Calculation and measurement results of the heat-spreaders. The thermal resistance decreases with increasing area, with diminishing returns for very large area. The parasitic capacitance, however, increases linearly.

The heat-spreaders are mounted between both GaN devices and the heatsink. Good thermal contact between layers is provided by a low-resistive indium interface material, which conforms to the surfaces and eliminates most voids. At a conductivity of $80 \mathrm{~W} / \mathrm{mK}$ and a layer thickness below $100 \mu \mathrm{~m}$, the indium has a total theoretical contribution to the thermal path well below $0.066 \mathrm{~K} / \mathrm{w}$. Figure 3.7 shows the measured and calculated thermal resistance from the transistor junction towards the bottom surface of the heatspreader, as well as the parasitic capacitance. The capacitance is measured between the top surface of the heatspreader and the aluminium backplate with an LCR meter.

To measure the thermal resistance, 10 W is dissipated in the transistor and the resulting temperature increase is measured. Due to the chipscale package of the GaN transistors, a thermocouple can be placed near the transistor's junction through a hole in the PCB. A second thermocouple is used to measure the heatsink's sur-


Figure 3.8 (a) Half-bridge PCB with shunt resistor to measure the drain-source current of the low-side transistor. (b) Schematic of the double-pulse setup. The load inductor is charged by the low-side transistor to a specified current. The transistor is then pulsed off and on to measure the device current and voltage during commutation. The product of these two quantities is integrated to obtain the turn-on and turn-off losses.
face temperature. The transistor's total junction-to-case resistance is given in the datasheet as $0.5 \mathrm{~K} / \mathrm{w}$. Excluded from the measurement is the heatsink to ambient resistance, which would need to be considered for a final application.

Despite this straightforward approach, the calculation agrees well with the measured results, except for the smaller heat-spreaders, where the calculated thermal resistance is up to $10 \%$ below the measured value. With no heat-spreading, the thermal path has a total measured thermal resistance of $4 \mathrm{~K} / \mathrm{W}$ at a parasitic capacitance of 7 pF . By increasing the spreader area by a factor of six, the total resistance can be reduced to $1.3 \mathrm{~K} / \mathrm{w}$, but the parasitic capacitance reaches 39 pF . At a drain-source capacitance per transistor of 89 pF this already equates to a significant amount of charge, which leads to a corresponding increase in switching energy. To verify this correlation, each heatspreader is tested in a double-pulse setup.

### 3.4.1 Double-pulse setup

A half-bridge, shown in Figure 3.8(a), is connected according to the schematic depicted in Figure 3.8(b). The load inductor is connected between the switching node and the positive supply voltage. The low-side transistor is used to ramp the inductor current up to a specified point and then pulsed off and on in rapid succession. The losses for turn-on are then obtained by measuring both drain-source
voltage and current of the transistor simultaneously and integrating the product of the two measurements.

Due to the fast switching times of GaN , the measurements require high bandwidth to obtain accurate loss measurements. While the device voltage is relatively simple to capture with a high-bandwidth probe, the device current requires a specialized sensor. Several methods have been investigated in [52] for silicon-carbide devices. For this setup the coaxial shunt (T\&M Research SDN-414-10) was chosen because of its high bandwidth, linearity and ease of use.

The coaxial shunt and its equivalent circuit is depicted in Figure 3.8(b). Because of its internal construction, the voltage measured on the BNC connector contains little to no inductive spike during pulsed currents, creating an accurate high-bandwidth sensor. The manufacturer specifies a 2 GHz passband. However, compared to the other current sensors, such as the Rogowski coil with a contribution as low as 200 pH , the coaxial shunt adds a significant inductance to the power loop. During turn-on, this inductance reduces the drain-source voltage as it counteracts the commutation current, which reduces the turn-on losses. However, the overall loop inductance of the setup including the shunt resistor is comparable to evaluation boards available from the device manufacturers [17]. The exact value of the shunt's additional inductance is determined by observation of the voltage drop prior to commutation.

A low power loop inductance is achieved through a multi-layer PCB, with the power loop closed through internal layers below the transistors [58]. Furthermore, the shunt is mounted as shown in Figure 3.9, with a threaded terminal, as opposed to the wired connection in [17]. The M4 thread is bolted into a threaded insert from the bottom, such that the outer casing makes contact on the bottom layer with the low-side source and the thread contacts dc- on the top layer. Via stitching is used to route the dc supply from the top layer back to the internal layers. From there, the negative power rail is routed underneath the switching devices back to the dc-link capacitor.

The oscilloscope used to measure both voltage and current is an MDO64 from Tektronix, measuring the voltage and current at a sample-rate of $12.5 \mathrm{GS} / \mathrm{s}$ with 12 bits of resolution. The device voltage is measured with a TPP1000 and the shunt is connected with a $50 \Omega$ termination to the oscilloscope input, both measured at 1 GHz bandwidth. The probes for voltage and current are de-skewed to ensure proper time-alignment during testing. The double-pulse test is carried out at a supply voltage of 400 V , with the load current ranging from 0 A to 30 A . The half-bridge is mounted to a heat-sink with the heat-spreader in-between the PCB and heat-sink. The double-pulse test is then carried out in increments of 5 A up to a maximum of 30 A . This set is repeated for each of the heat-spreaders. Furthermore, two more reference measurements are carried out. First, with no heat-spreader attached to the


Figure 3.9 PCB cross-section. Inner layers close the power loop for reduced inductance. Outer to inner layer separation is $200 \mu \mathrm{~m}$, total PCB thickness is 1.5 mm .
transistors, and then additionally with the shunt removed. These two measurements demonstrate the impact the shunt has on the switching performance by itself.

### 3.4.2 Measurement results

The results of the no shunt reference, no heat-spreader and the largest heat-spreader are shown in Figure 3.10. The inductive impact of the shunt is evident from the increased voltage drop $\Delta v$ observed at the beginning of the turn-on process. During this interval, the loop inductance counteracts the commutation which causes a sudden drop in drain-source voltage. With the shunt connected, the voltage drop nearly doubles from 14 V to 27 V . The additional impedance of the shunt acts as a turn-on snubber, reducing the drain-source voltage before commutation of the load current. Using the fundamental equation for inductors, the voltage drop $\Delta v$, in conjunction with the current measurement, can be used to estimate the total loop inductance

$$
\begin{equation*}
L_{\mathrm{loop}}=\frac{\Delta v}{\frac{d i_{\mathrm{ds}}}{d t}} . \tag{3.10}
\end{equation*}
$$

The change of device current $\frac{d i_{\mathrm{ds}}}{d t}$, shown in Figure 3.10, peaks near the end of the initial voltage drop. In this case, the loop inductance with the shunt connected is estimated to 2.1 nH . Assuming proportional behaviour of the loop inductance, i.e. no voltage drop if the inductance were zero, the loop inductance without the shunt is estimated to 1.1 nH . Thus, on its own, the coaxial shunt contributes 1 nH to a circuit, if mounted as depicted in Figure 3.9.

The snubber effect of the shunt inductance effectively lowers the device voltage during turn-on, and thus the turn-on energy will be reduced. However, measurements with this specific setup are still comparable to each other and the impact of


Figure 3.10 Turn-on measurement at $v_{\mathrm{gs}}=0 \mathrm{~V}$ to $6 \mathrm{~V}, R_{\mathrm{g}, \text { on }}=10 \Omega, R_{\mathrm{g}, \text { off }}=2 \Omega$. The drop in drain-source voltage is caused by parasitic inductance in the power loop. Use of the shunt resistor adds extra inductance in series, leading to a larger voltage drop $\Delta v$. By examining the derivative of the device current, estimates for the parasitic inductance can be made.
heat-spreaders can be investigated. By integration of device voltage and current, the turn-on energy is obtained and shown in Figure 3.11. It also depicts the increase in losses between the measurements with the heatspreaders and the reference measurement.

From intuition, the losses must increase at least by the energy stored in the parasitic capacitance at the time of commutation, marked in dashed lines. At this time instant, the parasitic inductance reduces the voltage on the switching node by the amount $\Delta v$, as previously indicated in Figure 3.10. However, all measurements show a larger increase at zero turn-on current, which decreases towards the stored capacitor energy for larger currents. This is to be expected, as at zero turn-on current, the parasitic capacitance not only contributes its stored energy, but also increases the peak commutation current by a significant amount. As the device doesn't need to commutate a large load of current, the commutation is fast and a small absolute increase in peak current has a large relative impact on the losses. In contrast, at
$\therefore$ No IMS $\quad$ - IMS $20 \mathrm{~mm}^{2} \multimap$ IMS $80 \mathrm{~mm}^{2} \multimap$ IMS $120 \mathrm{~mm}^{2}$



Figure 3.11 Turn-on losses from the double-pulse measurement for varying spreader size. The stored energy in the spreader's parasitic capacitance is indicated in dashed lines. For low currents, the additional losses exceed this energy by a significant amount, which decreases for larger turn-on currents.
large load currents, most of the losses are generated in the time frame where the device current increases towards the load current and thus, the slightly increased commutation current has less impact on the overall losses.

Given that the experiment used heatspreaders with a low dielectric constant of 1.8, the absolute increase in losses still remained small. However, most polymer based solutions tend to have a dielectric constant between 4 and 5 . At the same insulation layer thickness, this would increase the parasitic capacitance by almost a factor of 3 and the resulting switching losses would quickly become noticeable in typical converter applications. The question which spreader size to choose for a given transistor can be solved with the harmonic balance method introduced in chapter 2.

### 3.5 Optimization using harmonic balance

As established in the the previous section, the switching losses of GaN devices increase when using heatspreading. While a larger heatspreader reduces the thermal resistance, the increase in switching losses can negate the desired benefit. At which exact point this happens, depends on the load current, switching frequency and other operating parameters. Using the analytic solution for heatspreaders shown


Figure 3.12 Operating point of a GaN transistor in a full-bridge grid-inverter for various heatspreader sizes. A larger area leads to lower average junction temperature.
in Section 3.3, in combination with the method introduced in chapter 2, creates a quick way of dimensioning a good heatspreader for any given inverter. Figure 3.12 shows the effect of heatspreading on a GaN device in a full-bridge grid-inverter, as specified in Table 3.2. For simplicity, the increase in losses due to the parasitic capacitance is simplified to the stored energy. For more precise optimization, a set of loss measurements for varying capacitance and varying temperature would have to be obtained or supplied by the manufacturer.

Initially, with no heatspreading for a cooling surface of $20 \mathrm{~mm}^{2}$, the resulting large thermal resistance leads to a certain amount of conduction and switching losses, at a relatively high operating temperature. By doubling the area, the operating temperature decreases significantly, and with it the conduction and switching losses, as they increase with temperature. While further increase of the spreader size still decreases the thermal resistance, the spreader's parasitic capacitance grows and the switching losses begin to rise again. For larger spreaders, the decrease in temperature reduces, while the total system losses increase. Most notably, the heatspreader with lowest losses is different from the one for lowest temperature. As device temperature can be an important metric for the expected lifetime, heatspreader design becomes a trade-off between efficiency and lifetime. The device temperature and losses are depicted in Figure 3.13 for increasing spreader size, for several load currents and switching frequencies. At 8 A , using a heatspreader initially reduces the operating temperature, but shows almost no change in device losses. Further increase has

Table 3.2 Inverter parameters

| Parameter | Symbol | Value |
| :---: | :---: | :---: |
| Output frequency | $f_{\mathrm{o}}$ | 50 Hz |
| Supply voltage | $V_{\mathrm{dc}}$ | 400 V |
| Grid voltage | $V_{\text {grid }}$ | 230 Vrms |
| Transistors | $Q_{1}, Q_{2}$ | GS 66508 T |
| Output inductor | $L$ | $500 \mu \mathrm{H}$ |
| Ambient temperature | $T_{0}$ | $40^{\circ} \mathrm{C}$ |
| Insulation permeability | $\varepsilon_{\mathrm{r}}$ | 4 |
| Insulation conductivity | $\lambda_{\text {ins }}$ | $4 \frac{\mathrm{~W}}{\mathrm{mK}}$ |

little to no effect in temperature, but shows a significant increase in device losses. In contrast, at larger currents heatspreading becomes essential in reducing the losses as well as temperature.

However, after a certain point, the previous pattern re-emerges and the losses increase, at no significant benefit in temperature. Thus, overly large heatspreader design can have a detrimental effect on system performance. In addition, unnecessarily large heatspreaders will induce excessive circulating currents through the heatsink and cause further issues with regards to electromagnetic interference.

Next to optimization, this method can also show the fundamental limits of a halfbridge, given a number of restrictions. Figure 3.14 depicts the previously defined inverter in addition to versions with smaller and larger transistors. At 16 A and 200 kHz , the original $50 \mathrm{~m} \Omega$ device shows the lowest achievable losses. However, due to it's larger thermal interface, the $25 \mathrm{~m} \Omega$ device shows lower attainable operating temperature, despite higher losses.

### 3.6 Conclusion

While GaN offers several advantages over silicon or SiC due to its smaller size, cooling it effectively is not an easy endeavour. The design of a thermal interface needs to take the switching speed of GaN into account, and provide a good thermal resistance, while not adding too much parasitic capacitance. This relationship between resistance and capacitance can be represented by a proposed figure of merit for a given material. This FOM makes it easier to compare suitable materials for electric insulation of GaN devices. While ceramic materials show the best possible characteristics, other materials stay relevant due to cost and ease of use.

One such option is insulated metal substrates. Using their customizable copper


Figure 3.13 Pareto fronts of heatspreader size as a function of load current and switching frequency. The load current is sinusoidal, corresponding to the specified rms value. Each step along a line respresents a spreading area increase of $20 \mathrm{~mm}^{2}$ up to a total area of $200 \mathrm{~mm}^{2}$.


Figure 3.14 Pareto fronts for heatspreader size for different semiconductors. The load current is sinusoidal, corresponding to the specified rms value. Each step along a line represents a spreading area increase of $20 \mathrm{~mm}^{2}$ up to a total area of $200 \mathrm{~mm}^{2}$. The $50 \mathrm{~m} \Omega$ device shows the best tradeoff between achievable junction temperature and losses. The smaller device is less efficient and operates at a higher temperature. The larger device can operate at a lower temperature, but is less efficient as well.
surface, the heat can be spread out prior to insulation, effectively lowering the total thermal resistance. Determining this resistance can be done through a simplified analytic approach, which matches in simulation as well as in experiments.

While heat-spreading shows a decrease in thermal resistance with spreading area, the parasitic capacitance increases. A resulting growth of switching losses has been verified with a double-pulse setup. When faced with the task to design a heatspreader for a given converter, harmonic balance serves as a powerful tool to find a good trade-off between reduced thermal resistance and total system losses. In the end, material choice and whether or not heatspreading is helpful will depend on the application and budget.

As mentioned before, the average junction temperature or the temperature swing during a cycle are an indication for the expected life time of a device. Given additional restrictions for parameters such as control bandwidth (dictating the switching frequency), output power (determining the load current), and efficiency (limiting the losses), certain inverters cannot be realized with a single half-bridge. The next chapter explores one of the simplest and intuitive solutions to this problem.

# 4 <br> <br> Magnetic coupling for <br> <br> Magnetic coupling for interleaved half-bridges 

 interleaved half-bridges}
"How can less be more? That is impossible. More is more!"

Yngwie Malmsteen

IN order to increase the output power in an inverter, just increasing the transistor size only works up to a certain point. For MOSFETs or GaN HEMTs and given double the output current, the transistors area needs to increase by a factor of four just to achieve the same conduction losses. At the same time, the switching losses increase, due to the larger current being switched and due to larger device capacitances. With the additional increase in switching energy, the total losses per device can easily overwhelm the capabilities of a single transistor. As shown in chapter 3, a larger device can perform worse for a set of restrictions. As paralleling two devices indirectly creates a chip of double the die area, it is not the answer to this problem.

Instead of just duplicating the number of transistors, duplicating the entire commutation cell allows to increase the output current while maintaining or even increasing the switching frequency. By operating the individual carriers of each half-bridge at a phase shift, i.e. interleaving, a higher effective control-bandwidth can be achieved. In addition, cancellation of input and output current-ripple occurs at specific operating points of the inverter. Furthermore, by using magnetic coupling between interleaved bridges, a similar effect greatly reduces the current ripple within each inductor.


Figure 4.1 Flying capacitor inverter with $N+1$ levels.


Figure 4.2 Interleaved inverter with $N$ phases.

### 4.1 Multi-level topologies

As shown in the previous chapter, a single half-bridge might not suffice to meet application requirements with regards to output power, switching frequency, operating temperature or efficiency. Any number of these parameters can be improved by utilizing additional switches. Moving beyond a single half-bridge, several options become available. To increase the output voltage, multiple transistors can be operated in series. One example is the flying capacitor converter, depicted in Figure 4.1, where the device voltage is limited by capacitors across series connected half-bridges [42]. To increase the output current, the most intuitive approach is to parallel separate half-bridges, as depicted in Figure 4.2, each with their respective filter inductors as done in [75]. The two approaches of parallel and series connected half-bridges can be combined, as done in [45].

One benefit of using multiple half-bridges, whether in series or parallel, is to operate them at phase shifted carriers, i.e. interleaving. By separating the switching instants of different half-bridges, a higher effective switching frequency can be achieved. This leads to benefits regarding current ripple and control bandwidth. Especially for parallel interleaved half-bridges, certain operating points show almost complete cancellation of input and output current ripple.


Figure 4.3 PWM carriers for $N=1 \ldots 4$. With regular asymmetric PWM, each duty cycle is sampled at the top and bottom of the respective carrier. This allows to adjust the steady-state current per phase at a rate of $T_{\text {sw }} / 2$. Consequently, the sum of all phase currents can be adjusted whenever any phase is sampled. Given an odd number of phases, these sampling instants never overlap, yielding a higher effective output sample-rate compared to an even number of phases.

### 4.2 Parallel interleaved half-bridges

The basic principle of interleaving $N$ number of half-bridges is depicted in Figure 4.2. Each half-bridge has an individual filter inductor connected to a common output node at voltage $v_{\text {out }}$ and common input supply $v_{\text {in }}$. Given lossless operation in steady-state, the duty cycle of each bridge corresponds to $d=v_{\text {out }} / v_{\text {in }}$ and the average current per inductor over a switching period is $i_{\text {out }} / N$. For large control bandwidth and low distortion each half-bridge is modulated by a regular asymmetric PWM carrier [62]. This modulation scheme samples the duty cycle twice per switching period $T_{\mathrm{sw}}$, at fixed intervals of $T_{\mathrm{sw}} / 2$. By shifting the PWM carriers of each phase by increments of $360^{\circ} / \mathrm{N}$, as depicted in Figure 4.3, control over the summed output current can occur at a higher effective rate.

This is particularly effective for an odd number of bridges, with a resulting updaterate of $2 N / T_{\text {sw }}$, as the peaks and valleys of the carriers do not overlap. With an even number of bridges, the sample instants of carriers with a respective phase shift of $180^{\circ}$ overlap, thus reducing the update rate to $N / T_{\text {sw }}$. Initially, this favours an odd number of phases when control bandwidth is of concern. However, as the number of phases is increased, the current stress per phase decreases. This allows to operate each device at a higher switching frequency, choose a smaller device or a combination of both.


Figure 4.4 Attainable switching frequency and update rate for an interleaved inverter with $N$ phases, at a sinusoidal output current with a peak of 60 A . The average current per half-bridge reduces by a factor of $1 / \mathrm{N}$. As the conduction losses decrease asymptotically, the switching frequency can be increased. The achievable update rate corresponds to $N / T_{\text {sw }}$ for even, and $2 N / T_{\text {sw }}$ for odd phases.

Using the harmonic balance method introduced in chapter 2, the junction temperature for a large number of viable configurations can be calculated quickly. By calculating a half-bridge for an output current of $i_{\text {out }} / \mathrm{N}$ and a large range of switching frequencies, the results can be filtered for the desired operating temperature. Figure 4.4 depicts the attainable switching frequency and update rate for an interleaved inverter with a sinusoidal output current at a peak of 60 A . The device area is normalized to a single $650 \mathrm{~V} 25 \mathrm{~m} \Omega$ device. The conduction voltage and switching losses are scaled with $N$ and $1 / N$ respectively. In addition, the size of the thermal pad is scaled by $1 / N$, and the total thermal resistance from junction to ambient is assumed to be three-times the internal junction-to-case resistance. The inductance per phase is scaled such that the peak-to-peak current ripple per phase is always kept at $20 \%$ of the average phase current. By imposing different peak-to-peak temperature swings a clear pattern in attainable switching frequency and update-rate emerges. The maximum switching frequency grows asymptotically with the number of phases. Thus, for a small $N$ the step from an odd to the next higher number comes at reduced penalty in update rate. For large $N$, the benefit of an odd number of phases emerges clearly.

Next to considering system complexity, choosing the number of phases becomes a cost optimization. While smaller devices also cost less, at some point cost and volume of other components, such as inductors, gate drivers, their supplies and

$$
-i_{\mathrm{L}_{1}}-i_{\mathrm{L}_{2}}-i_{\mathrm{L}_{3}}-i_{\mathrm{L}_{4}}-i_{\mathrm{L}_{\Sigma}}
$$



Figure 4.5 Phase currents (color) and summed inductor current (black) for $N=$ $1 . . .4$ interleaved half-bridges. Due to the phase shift of $360^{\circ} / \mathrm{N}$ per half-bridge, the current ripple cancels exactly whenever the duty cycle is an integer multiple of $1 / \mathrm{N}$.
current measurements become significant. In addition, other benefits of interleaving should be considered. While an odd number generally yields higher bandwidth, for specific applications an even number can show operating point dependent improvements regarding input and output current ripple.

### 4.2.1 Output current ripple

As each phase outputs a triangular current at a phase shift, cancellation can occur in the summed inductor current $i_{\mathrm{L}_{\Sigma}}$. In an $N$-phase inverter the summed current ripple cancels completely, whenever the duty cycle is an integer multiple of $1 / \mathrm{N}$. This relationship is shown by several examples in Figure 4.5.

The peak-to-peak summed current ripple is given by

$$
\begin{equation*}
\Delta i_{\mathrm{L} \Sigma}=\frac{1}{N}(N d-\lfloor N d\rfloor)(\lceil N d\rceil-N d) \frac{v_{\mathrm{in}} T_{\mathrm{sw}}}{L} \tag{4.1}
\end{equation*}
$$

where floor $(\rfloor)$ and ceiling $(\rceil)$ operators round the variable down or up to the nearest integer. Figure 4.6 depicts the peak-to-peak current ripple of interleaved


Figure 4.6 Peak-to-peak summed current ripple for interleaved half-bridges, normalized to $\Delta I_{\mathrm{L}}$.
converters for $N=1 \ldots 4$, normalized to the single-phase, worst-case peak-to-peak current of $\Delta I_{\mathrm{L}}=v_{\text {in }} T_{\mathrm{sw}} / 4 L$. In addition to the operating points of full cancellation, each increase in the number of phases reduces the maximum output current ripple, which occurs halfway between every two cancellation points. A similar effect occurs for the input current of the inverter.

### 4.2.2 Input current ripple

Next to the output ripple, the input ripple also has cancellation effects from interleaving, as depicted in Figure 4.7. As the inductors are only connected to the input when the high-side switch is on, the input current consists of $N$ trapezoidal pulses with a width of $d T_{\mathrm{sw}}$. The trapezoids consist of two parts, the rectangular average current of a phase $i_{\text {out }} / N$, in addition to the superimposed current ripple of the corresponding inductor. At certain duty cycles the high-side transistor currents sum up in such a way, that their average equals the input current $i_{\text {in }}$. Only a sawtooth current ripple, proportional to the filter inductance remains. These duty cycles are again integer multiples of $1 / \mathrm{N}$. As the input capacitor is subjected to the difference between input current and the summed transistor currents, operation at these cancellation points would allow to reduce the capacitor size.

To calculate the rms current ripple, the capacitor current can be split in two parts, representing the rectangular and sawtooth component. The split in two rms quantities is possible, as both components are orthogonal to each other. The rectangular component is equal to

$$
\begin{equation*}
i_{\rho, \mathrm{rms}}=i_{\mathrm{out}} N \sqrt{(N d-\lfloor N d\rfloor)(\lceil N d\rceil-N d)} \tag{4.2}
\end{equation*}
$$



Figure 4.7 Combined high-side device current and average input current for $N=1 \ldots 4$ interleaved half-bridges.
displaying the same cancellation pattern as the output current.
The sawtooth component is equal to

$$
\begin{equation*}
i_{v, \mathrm{rms}}=\frac{\Delta I_{\mathrm{L}}}{\sqrt{3}} \frac{(1-d)}{2 N} \sqrt{\left[\lceil N d\rceil^{2}(N d-\lfloor N d\rfloor)^{3}+\lfloor N d\rfloor^{2}(\lceil N d\rceil-N d)^{3}\right]} \tag{4.3}
\end{equation*}
$$

Figure 4.8 depicts the rectangular and sawtooth rms current ripple, normalized to an output current $i_{\text {out }}=1 \mathrm{~A}$ and worst-case phase current ripple $\Delta I_{\mathrm{L}}=1 \mathrm{~A}$.

Unlike the rectangular component, the sawtooth component reaches its maximum whenever the duty cycle is an integer multiple of $1 / \mathrm{N}$. Normalized to 1 A , it is nearly one order of magnitude below the rectangular current ripple. However, given common design practice for PWM inverters, the filter inductor is dimensioned such that the peak-to-peak current ripple $\Delta I_{\mathrm{L}}$ is $20 \%$ to $40 \%$ of the load current $i_{\text {out }}$.

Thus, despite the opposite behaviour, the local minima of combined rectangular and trapezoidal current ripple will likely remain at duty cycles of integer multiples of $1 / \mathrm{N}$. Given both minimized output and input ripple, operation at these points can potentially reduce losses in the required filter capacitances at the input and output of the inverter. Since the input capacitor's main purpose is filtering of the rectangular input current ripple, its size can be reduced significantly given the right operating


Figure 4.8 Rectangular ( $i_{\rho, \text { rms }}$ ) and sawtooth ( $i_{v, \text { rms }}$ ) rms input capacitor current for interleaved half-bridges. The rectangular component is normalized to the output current, whereas the sawtooth component is normalized to the maximum peak-to-peak phase current ripple.
conditions and number of phases.
As the average current per inductor is reduced to $i_{\text {out }} / N$, the volume per inductor can be reduced, but $N$ separate inductors are required. As discussed in [57], scaling down inductors reduces achievable power density, which favours topologies with a lower number of inductors and thus phases. However, this problem can be circumvented by utilizing more than one phase per magnetic component, i.e. coupled inductors.

### 4.3 Coupled inductors

By coupling the individual inductors on a common magnetic core, as depicted in Figure 4.9, further improvement in steady-state operation, as well as transient performance can be obtained. The concept of coupling was proposed for voltage regulator modules (VRM) commonly used on computer mainboards, where quick and tight regulation of voltage rails is necessary [76]. By magnetically coupling the inductors, the voltage applied to one phase will affect the currents in all other phases. The coupling factor and inductance can be tuned to reduce the current ripple or


Figure 4.9 Coupled inductors. The coupling between any two windings can be expressed through a coupling coefficient $k=\frac{L_{\mathrm{m}}}{L_{\mathrm{s}}}$, where $L_{\mathrm{s}}$ and $L_{\mathrm{m}}$ are the windings self and mutual inductance.
increase the transient response. As all phases can interact with each other, the easiest way to fully describe any arbitrary coupled system is through an inductance matrix

$$
\boldsymbol{L}=\left[\begin{array}{ccccc}
L_{11} & \ldots & L_{1 n} & \ldots & L_{1 N}  \tag{4.4}\\
\ldots & \ldots & \ldots & \ldots & \ldots \\
L_{n 1} & \ldots & L_{n n} & \ldots & L_{n N} \\
\ldots & \ldots & \ldots & \ldots & \ldots \\
L_{N 1} & \ldots & L_{N n} & \ldots & L_{N N}
\end{array}\right]
$$

Here, the main diagonal contains the self-inductance of each inductor, and the remaining terms are the mutual inductances between two any two inductors.

The slope of all inductor currents can be obtained by multiplying the inverse of $L$ with a vector $v_{\mathrm{q}}$ describing the switching node voltage $v_{n}$ of each half-bridge, minus the output voltage $v_{\text {out }}$ such that

$$
\begin{equation*}
\frac{d \overrightarrow{i_{\mathrm{L}}}}{d t}=L^{-1} \cdot\left(\overrightarrow{v_{\mathrm{q}}}-v_{\text {out }}\right), \quad \text { with } \quad \overrightarrow{v_{\mathrm{q}}}=\left(v_{1} \ldots v_{N}\right)^{T} \tag{4.5}
\end{equation*}
$$

The solution for an arbitrary coupled system with more than two phases quickly becomes cumbersome to obtain. By assuming a fully symmetric core and winding design a general solution for any number of phases can be obtained, as presented in [33].

The two components necessary to describe the coupled inductor are the self inductance $L_{\mathrm{s}}$ and mutual inductance $L_{\mathrm{m}}$. Given full symmetry, the coupling between any two windings can be expressed through a coefficient $k$, such that $k=L_{\mathrm{m}} / L_{\mathrm{s}}$. The reduction in peak-to-peak ripple or increase of bandwidth is achieved by choosing a coupling matrix such that $k$ is negative. The resulting operating waveforms for varying $k$ are depicted in Figure 4.10.

Whenever the duty cycle is an integer multiple of $1 / N$, the peak-to-peak ripple sees reduction at stronger coupling. Given a symmetric coupling matrix, the peak-to-peak


Figure 4.10 Phase current ripple for coupled inductors with coupling factor $k$. When the duty cycle is an integer multiple of $1 / N$, coupling further reduces the peak-to-peak ripple. Outside of these operating points, past a certain threshold coupling increases the peak-to-peak current.
current ripple of coupled phase inductors can be formulated as

$$
\begin{equation*}
\Delta i_{\mathrm{L}, \mathrm{n}}=\underbrace{\frac{v_{\mathrm{in}} T_{\mathrm{sw}}}{L_{\mathrm{s}}(1+k)} d(1-d)}_{\substack{k=-1}} \frac{N-1+\frac{k}{1-d}\left(N+d-2\lceil N d\rceil+\frac{\lceil N d\rceil\lfloor N d\rfloor}{N d}\right)}{N-1-k} . \tag{4.6}
\end{equation*}
$$

From this equation, it can be seen that for stronger coupling the first term tends toward infinity. The second term, similar to the input and output ripple cancellation, tends towards zero for specific duty cycles. At these points, the equation converges towards a stable operating point. Outside of the points, the peak-to-peak ripple will grow indefinitely as $k$ approaches -1 . The normalized peak-to-peak amplitude for varying duty cycle is depicted in Figure 4.11.

For weak coupling, the overall peak-to-peak ripple decreases slightly, with the largest reduction at integer multiples of $1 / N$. For stronger coupling, the reduction at these points improves further, but the ripple outside these points begins to surpass the case of no coupling.

Outside of steady-state, for small perturbations the coupled inductor will exhibit transient behaviour equivalent to an inductance of $L_{\mathrm{s}}(1+k)$ [76]. Together with
药




$$
\boxed{-} k=0 \_k=-0.25-k=-0.5-k=-0.75--k=-0.95
$$

Figure 4.11 Normalized inductor current ripple as function of coupling coefficient detailed for $N=2 \ldots 4$.
a filter capacitance, this equivalent inductance defines the inverter's open loop bandwidth. The coupling coefficient and subsequently self-inductance can then be chosen to adjust the worst-case peak-to-peak current in accordance with the capacitors current ripple rating.

### 4.4 Conclusion

Considering the problem formulation in chapter 1, interleaving and coupling are essential tools with which the boundaries of bandwidth and power can be extended by significant margin. In addition, increasing the number of phases decreases the worst case input, output and phase current ripple. However, the optimal number of phases is very application specific. While an odd number of phases typically yields higher control bandwidth, the ripple reduction for input, output and phase current is highly operating point dependent. Both aspects need to be considered. An odd number of interleaved phases might operate only rarely at the points of optimal ripple cancellation, or vice versa.

For coupled inductors with more than two windings, realizing a fully symmetric coupling matrix can become difficult without resorting to custom core shapes. Instead, several symmetric two-winding transformers can be used to construct a desired coupling matrix, as presented in [36]. Independent of how the coupled inductor is realized, control and thus measurement of each phase is required to ensure equal distribution of the load current. As high bandwidth correlates to large
current slopes in the inductors, timing related effects start to have noticeable impact in the measurements [40]. The next chapter will investigate these effects in detail for regular sampled PWM.

# Low-noise high-bandwidth current measurements 

"Come on feel the noise
Girls, rock your boys "
Quiet Riot

FOR bandwidth and power density it is desirable to increase switching frequency and lower the filter inductance. Subsequently, measurements of the inductor current need to be obtained at a higher bandwidth as well [55]. Ideally, the sampling occurs synchronous to operation of the half-bridge at twice the switching frequency, such that the obtained measurement represents the average inductor current [32]. However, with lower inductance, seemingly minor time variations begin to take a noticeable effect on the measurement [40]. This chapter investigates the distortion and noise added due to timing mismatches, and presents a compensation and mitigation technique relying solely on existing quantities known to the control system.


Figure 5.1 Half-bridge with fully isolated output current measurement. The current is measured with a shunt resistor, whose output voltage is amplified and sampled by the ADC. The control system interfaces the gate drivers and the ADC through digital isolators. Due to a mismatch in propagation delays, the samples of the ADC occur an unspecified time $T_{\mathrm{p}}$ away from the switching actions of the half-bridge.

### 5.1 Half-bridge current measurement

As presented in previous work, shunt resistors are a good choice for measuring the inductor current of a half-bridge [40]. Compared to other solutions such as flux-gate sensors, they can provide a high bandwidth in a much smaller form factor. However, the downside is a direct electric connection to the half-bridge. As depicted in Figure 5.1, the shunt resistor $R_{\mathrm{s}}$ is connected in series with the filter inductor and should be referenced to the output voltage. A connection prior to the inductor would need to withstand the high voltage slopes generated by the half-bridge [53]. Isolation prior to digital conversion is possible, for instance using isolated modulators. However, their noise performance and signal bandwidth is lacking for high-precision, high-bandwidth applications. The same holds for other forms of isolated current measurements, i.e. hall-effect sensors.

Instead, by applying analog-to-digital conversion (ADC) of the shunt voltage prior to isolation, the digital signal can be transmitted via digital signal isolators without any loss of information. However, every isolator adds propagation delay, which can vary over time and from component to component. The delay appears at a constant value of $T_{p}$, typically on a timescale of nanoseconds. On top of the constant delay is a minor time variation in the order of picoseconds, commonly referred to as jitter. Jitter varies between switching events and is represented by its rms quantity $T_{\mathrm{jit}}$.


Figure 5.2 Idealized sampling of output current. The samples are offset by the unknown difference $T_{\mathrm{p}}$ of driver and ADC propagation delay. Depending on the current slope, the obtained sample is above or below the correct value. In addition to propagation delay, the each isolator adds random jitter to the delay, which adds a Gaussian distribution to the sample instant.

Next to the ADC, the gate drivers are usually also interfaced through such digital isolators, adding another unknown delay to the system. For now, the delay of the two gate signal isolators is assumed to be equal. If the control system is unaware of the delay between gate drivers and ADC $T_{\mathrm{p}}$, the switching actions of the half-bridge and sampling of the ADC occur at different time instances. However, most control systems assume ideal switching and sampling instants. The samples should occur exactly half-way between the switching events, to capture the inductor current at the periodic average. However, as depicted in Figure 5.2, the unknown delay $T_{\mathrm{p}}$ offsets the sampling instant from the ideal point. The result are samples with errors corresponding to the unknown delay and operating point dependent current slope.

### 5.2 Propagation delay distortion and compensation

The errors are determined by considering the switching states at the top and bottom of the carrier and an unknown delay between half-bridge and ADC of $T_{\mathrm{p}}$. Excluding duty cycles of zero or one, the voltage across the inductor is $v_{\text {in }}-v_{\text {out }}$ at the carrier top and $-v_{\text {out }}$ at the carrier bottom. The voltage drop across the transistors and shunt resistor is neglected for this analysis. The system is controlled closed-loop, such that the average inductor $\overline{i_{\mathrm{L}}}$ follows a reference value. At the top of the carrier, the high-side switch is conducting and the measurement obtained at the top of the carrier is

$$
\begin{equation*}
i_{\mathrm{t}}=\overline{i_{\mathrm{L}}}+\underbrace{\frac{v_{\mathrm{in}}-v_{\mathrm{out}}}{L} T_{\mathrm{p}}}_{e_{\mathrm{t}}}, \tag{5.1}
\end{equation*}
$$

Subsequently, sampling at the bottom of the carrier leads to a measurement of

$$
\begin{equation*}
i_{\mathrm{b}}=\overline{i_{\mathrm{L}}} \underbrace{-\frac{v_{\text {out }}}{L} T_{\mathrm{p}}}_{e_{\mathrm{b}}} . \tag{5.2}
\end{equation*}
$$

Thus, this creates two separate, output voltage dependent errors $e_{\mathrm{t}}$ and $e_{\mathrm{b}}$. As depicted in Figure 5.3, the two errors appear interleaved every other sample on the measurement, adding an average, operating-point dependent offset plus a component at the switching frequency. Assuming the control loop is bandwidth limited, the average current error

$$
\begin{equation*}
e_{\mathrm{avg}}=0.5 e_{\mathrm{t}}+0.5 e_{\mathrm{b}}=\frac{v_{\mathrm{in}}-2 v_{\mathrm{out}}}{2 L} T_{\mathrm{p}} \tag{5.3}
\end{equation*}
$$

will appear inverted on the controlled output current. Figure 5.4 shows the errors of an unaccounted delay of 5 ns and an inductance of $50 \mu \mathrm{H}$. Depending on the output current range and application, the resulting average error can become significant, especially when operating at high or low output voltage. However, at an output voltage of $v_{\text {in }} / 2$ the two sample errors average out to zero.

By introducing a set of two dynamic weights, $x_{\mathrm{t}}$ and $x_{\mathrm{b}}$, the error can be reduced to zero for all operating points. By equating the sum of weighted samples to zero,

$$
\begin{equation*}
x_{\mathrm{t}} e_{\mathrm{t}}+x_{\mathrm{b}} e_{\mathrm{b}}=\left(x_{\mathrm{t}}\left(v_{\text {in }}-v_{\text {out }}\right)-x_{\mathrm{b}} v_{\text {out }}\right) \frac{v_{\text {in }} T_{\mathrm{p}}}{L}=0 \tag{5.4}
\end{equation*}
$$

and setting $x_{\mathrm{t}}+x_{\mathrm{b}}=1$, the two weights can be determined to

$$
\begin{equation*}
x_{\mathrm{t}}=\frac{v_{\text {out }}}{v_{\text {in }}} \quad \text { and } \quad x_{\mathrm{b}}=1-\frac{v_{\text {out }}}{v_{\text {in }}} . \tag{5.5}
\end{equation*}
$$

Calculating these weights requires measurements of the input and output voltage at sufficient bandwidth. However, in most controlled inverters both quantities are


Figure 5.3 Closed-loop control diagram with controller $C$, plant $P$ and feedback filter $H$. Due to an unknown time delay, sampling of the output current contains alternating errors depending on the slope of the current.


Figure 5.4 Sample error caused by an uncompensated delay between the inverter and ADC . The samples on the rising and falling edge contain the largest errors at zero or full output voltage respectively. For the average of the two samples, the error cancels at half of the input voltage.
available. Since the unknown delay and the inductance are cancelled, the method is resilient against the temperature dependency of the inductor or the isolators propagation delay. To implement the dynamic weights, the transfer function in the feedback path needs to alternate the most recent sample between the two weights such that

$$
H(z)= \begin{cases}x_{\mathrm{t}}+x_{\mathrm{b}} z^{-1} & \text { if } \frac{d i_{\mathrm{L}}}{d t}>0  \tag{5.6}\\ x_{\mathrm{b}}+x_{\mathrm{t}} z^{-1} & \text { otherwise }\end{cases}
$$

In the worst case, at zero or full output voltage, the filter acts as a unit delay for every other sample, which needs to be considered during tuning of the control loop.

### 5.3 Jitter induced noise

On a much smaller timescale compared to the previously discussed unknown propagation delay, jitter causes a similar error in the measurement. However, given the random distribution of the jitter, this variation appears as white noise on the acquired signal. Both the ADC and gate-driver isolators exhibit jitter on their outputs, with the specified rms distributions $T_{\mathrm{ADC}-\mathrm{jit}, \mathrm{rms}}$ and $T_{\mathrm{gd}-\mathrm{jit}, \mathrm{rms}}$. Whether or not the ADC samples too early or too late, or the gate driver switches too early or too late makes no difference in perceived noise, as either the sampling instant is moved relative to the triangular current, or the triangular current is shifted relative to the sampling instant. However, as these two sources are uncorrelated, their respective rms jitter adds to the perceived sampling jitter as

$$
\begin{equation*}
T_{\mathrm{jit}, \mathrm{rms}}=\sqrt{T_{\mathrm{gd}-\mathrm{jit}, \mathrm{rms}}^{2}+T_{\mathrm{ADC}-\mathrm{jit}, \mathrm{rms}}^{2}} . \tag{5.7}
\end{equation*}
$$

Usually with wide-bandgap semiconductors, the isolators for the gate-drivers become the major contributor of sampling jitter, as the fast slopes of wide-bandgap devices require the use of isolators with high common-mode transient immunity (CMTI). In contrast, the isolators interfacing the ADCs do not require a high CMTI, as they are placed on the output of the converter. Typical state of the art low-voltage differential signaling (LVDS) isolators add 0.7 ps rms to the transferred signals [67]. However, these isolators are expensive and require a fair amount of power supplied to the isolated plane. Thus, cheaper, single-ended isolators with higher jitter are still a valid option if cost needs to be reduced. To select the correct component the achievable SNR needs to be calculated.

The impact on SNR is the product of jitter and deviation in current. Similar to the previously established delay error, this can be derived as two separate terms for the samples obtained at the top and bottom of the carrier, with

$$
\begin{equation*}
\Delta i_{\mathrm{t}}=\frac{v_{\mathrm{in}}-v_{\mathrm{out}}}{L} T_{\mathrm{jit}, \mathrm{rms}} \quad \text { and } \quad \Delta i_{\mathrm{b}}=\frac{v_{\text {in }}-v_{\mathrm{out}}}{L} T_{\mathrm{jit}, \mathrm{rms}} \tag{5.8}
\end{equation*}
$$

To obtain the SNR of a fixed inductor current $i_{\mathrm{L}}$ sampled at the top of the carrier, the variation of the sample $\Delta i_{\mathrm{t}}$ is related to the inductor current as

$$
\begin{equation*}
\mathrm{SNR}_{\Delta i_{\mathrm{t}}}=20 \log _{10}\left(\frac{i_{\mathrm{L}}}{\Delta i_{\mathrm{t}}}\right) . \tag{5.9}
\end{equation*}
$$

The SNR for the bottom of the carrier is calculated in the same manner with $\Delta i_{b}$, with both results depicted in Figure 5.5 for $i_{\mathrm{L}}=20 \mathrm{~A}$. At an output voltage of 200 V , the top and bottom samples cross 100 dB . To increase the SNR, two consecutive samples can be averaged, such that

$$
\begin{equation*}
\mathrm{SNR}_{\frac{\Delta i_{\mathrm{t}}+\Delta i_{\mathrm{b}}}{2}}=20 \log _{10}\left(\frac{i_{\mathrm{L}}}{\frac{\Delta i_{\mathrm{t}}+\Delta i_{\mathrm{b}}}{2}}\right) . \tag{5.10}
\end{equation*}
$$



Figure 5.5 SNR of individual and weighted samples for a load current of 20 A . The samples at the top and bottom carrier decrease in SNR as the output voltage approaches either zero or $v_{\text {in }}$ respectively. Average of the two samples yields a signal with the highest SNR at $v_{\mathrm{in}} / 2$. Using the dynamic weights for delay compensation results in a signal with significantly higher SNR at high and low output voltages.

The average of two consecutive top and bottom samples shows an increase of 3.01 dB at $v_{\text {in }} / 2$. As $v_{\text {out }}$ tends toward zero or $v_{\text {in }}$ the SNR degrades, because the noise in either one of the samples dominates. Using the weights $x_{\mathrm{t}}$ and $x_{\mathrm{b}}$ for delay error compensation, the SNR becomes

$$
\begin{equation*}
\mathrm{SNR}_{x_{\mathrm{t}} \Delta i_{\mathrm{t}}+x_{\mathrm{b}} \Delta i_{\mathrm{b}}}=20 \log _{10}\left(\frac{i_{\mathrm{L}}}{x_{\mathrm{t}} \Delta i_{\mathrm{t}}+x_{\mathrm{b}} \Delta i_{\mathrm{b}}}\right) \tag{5.11}
\end{equation*}
$$

Instead of degrading like the average, the SNR of the weighted samples increases as the output deviates from $\frac{v_{\text {in }}}{2}$. At its worst, the weighted SNR matches the average SNR at its best.

As the SNR is operating point dependent, the overall performance for a sinusoidal load can be determined by integration of the rms error over the desired signal period [40]. To formulate the SNR for a sinusoidal current, a resistive load $R_{\mathrm{L}}$ connected between the output and half the supply voltage. The half-bridge is modulated such that the output voltage is

$$
\begin{equation*}
v_{\text {out }}(t)=v_{\text {in }}\left(\frac{1}{2}+\frac{\hat{m}}{2} \sin \left(\frac{2 \pi}{T_{\mathrm{o}}} t\right)\right), \tag{5.12}
\end{equation*}
$$



Figure 5.6 SNR of individual, averaged and weighted samples over fundamental period. While use of single samples or averaging shows decreasing SNR with modulation depth, use of the dymanic weights shows a continuous improvement up to 6.02 dB .
where $\hat{m}$ is the modulation depth ${ }^{1}$. The resulting inductor current obtained through sampling is equal to

$$
\begin{equation*}
i_{\mathrm{L}, \mathrm{rms}}=\hat{m} \frac{v_{\mathrm{in}}}{\sqrt{2} R_{\mathrm{L}}} \tag{5.13}
\end{equation*}
$$

The rms error of using only the top or bottom sample can be obtained by integration over one fundamental period $T_{\mathrm{o}}$. Due to symmetry around $v_{\text {out }}=v_{\text {in }} / 2$, the rms error of the top and bottom samples is equal. For the top sample, the error is calculated as

$$
\begin{equation*}
\Delta i_{\mathrm{t}, \mathrm{rms}}=\sqrt{\frac{1}{T_{\mathrm{o}}} \int_{0}^{T_{\mathrm{o}}}\left[T_{\mathrm{jit}, \mathrm{rms}} \frac{v_{\mathrm{in}}-v_{\mathrm{out}}(t)}{L}\right]^{2} d t}=T_{\mathrm{jit}, \mathrm{rms}} \frac{v_{\mathrm{in}}}{2 L} \sqrt{1+\frac{\hat{m}^{2}}{2}} . \tag{5.14}
\end{equation*}
$$

The resulting SNR is obtained by relating the rms signal to the rms error similar to (5.9). Averaging of two subequent samples again yields

$$
\begin{equation*}
\Delta i_{\Delta i_{\mathrm{b}} / 2+\Delta i_{\mathrm{t}} / 2, \mathrm{rms}}=T_{\mathrm{jit}, \mathrm{rms}} \frac{v_{\mathrm{in}}}{4 L} \sqrt{1+\frac{\hat{m}^{2}}{2}} \tag{5.15}
\end{equation*}
$$

with a constant improvement of 3.01 dB . When using the introduced weights for delay compensation, the overall error is

$$
\begin{equation*}
\Delta i_{\Delta i_{x_{\mathrm{b}} \Delta_{\mathrm{b}}+x_{\mathrm{t}} \Delta i_{\mathrm{t}}, \mathrm{rms}}}=T_{\mathrm{jit}, \mathrm{rms}} \frac{v_{\mathrm{in}}}{4 L} \sqrt{1-\hat{m}^{2}+\frac{3}{8} \hat{m}^{4}} . \tag{5.16}
\end{equation*}
$$

The resulting SNR is shown in Figure 5.6. For single samples, modulation results in a decrease of SNR with modulation depth, as half of the period is spent at output

[^4]voltages with increased noise. With the average of two consecutive samples, the SNR increase by 3.01 dB . Using the dynamic weights, the resulting SNR increases by more than 6.02 dB at full modulation depth, equivalent to one additional bit of resolution.

Whether or not the proposed dynamic weights are used, the expected jitter related noise of a system can be calculated and appropriate component choices can be made. Realistically, the noise only needs to be reduced to a level comparable to other noise sources in the current measurement. As uncorrelated noise adds with a square-root sum, lowering the jitter noise any further yields diminishing returns for overall SNR.

### 5.4 Conclusion

When reducing the size of filter inductor, be it for higher power density or faster transient response, the increasing effect of propagation delay and jitter introduced by digital isolators needs to be considered. With the presented equations, the impact on distortion and noise can be quantified. Using the proposed dynamic weights on two subsequent samples, the delay distortion can be mitigated entirely, at the cost of slightly reduced dynamic response. At its worst case, the introduced filter acts as a unit delay. Furthermore, use of the dynamic weights has a beneficial impact on SNR, as the less noisy sample is given higher weight. An improvement of up to 6.02 dB , or one effective bit, can be reached compared to a simple moving average filter of length two. Next to delay distortion, the resistive element itself experiences variation in value due to temperature dependencies of the material. As the resistor's losses and thus temperature vary with the load current, the voltage across the resistor becomes distorted. The next chapter quantifies this thermally dependent distortion.

# 6 <br> <br> Intermodulation distortion <br> <br> Intermodulation distortion in resistive current in resistive current measurements 

 measurements}
> "Pray, Mr. Babbage, if you put into the machine wrong figures, will the right answers come out?"

Charles Babbage

AS one of the forefathers of computing said, any output can only be as good as the input provided to the system. The same can be applied to amplifiers, in the sense that a controlled output can only be as precise as the sensor used to measure it. For closed-loop control, the electrical quantities of the amplifier need to be measured, the most basic of which are voltages and currents. Voltages can be measured directly, usually by means of a voltage divider, followed by additional signal conditioning and analog-to-digital conversion. Each of these steps adds correlated and uncorrelated errors to the signal, i.e. distortion and noise. Care must be taken in design of the signal conditioning and conversion circuits to keep these errors below a given threshold dictated by the application. Currents, however, need to be translated into to a measurable voltage prior to conversion. There are a multitude of current sensing methods. For low to medium power applications, shunt resistors provide a good trade-off between volume, cost, bandwidth and precision. This chapter aims to quantify the distortion in sensing of resistive elements due to the its thermal properties.


Figure 6.1 Low cost shunt resistors in the $m \Omega$ range, suitable for high-bandwidth current measurements. (a) WSK2512 with a maximum power dissipation of 1 W . (b) WSL3637 with a maximum power dissipation of 3 W .

### 6.1 Distortion in shunt resistors

At low frequencies a shunt resistor's output voltage is the product of the sensed current and the resistance, which should create an ideal linear translation from current to voltage. However, due to material properties, the resistance varies with temperature [7]. This temperature dependence ultimately leads to an error in the output voltage. In the field of microwave electronics, this effect is referred to as intermodulation distortion due to self-heating, which can occur in both passive and active circuit components [49], [66]. The same mechanism results in distortion in a resistor. Audio applications encounter this distortion when using resistors in feedback circuits, where they add unwanted spectral components [50]. This effect has been demonstrated in [54]. The source of the distortion is the varying power dissipation in the resistor, caused by the sensing current. ${ }^{1}$

As the power dissipation is proportional to the square of the current, the shunt's temperature will experience two extrema in one period, and so does its resistance due to the temperature dependence. For sinusoidal currents, this varying resistance results in an output voltage containing harmonics of the measured signal. The magnitude of these harmonics can be reduced by selecting a shunt with a lower temperature coefficient of resistance (TCR). Modern shunt elements offer TCRs of less than $5 \mathrm{ppm} / \mathrm{K}$, which is more than sufficient to reach a total harmonic distortion (THD) well below -120 dB [39], [59]. However, component cost can also be a driving factor, which encourages the use of lower cost resistors with larger TCR, such as the components depicted in Figure 6.1.

Selection of the right shunt resistor then becomes a trade-off between attainable

[^5]

Figure 6.2 Idealized quadratic temperature dependence of a thin film $5 \mathrm{~m} \Omega$ shunt resistor. The change of resistance per degree depends itself on the temperature.
precision and cost. Given the application requirements, simple distortion approximations can be made by considering the power dissipation caused by the nominal shunt resistance and input current. For more precise results, time-based simulation including the temperature dependence can be done, followed by a Fourier transform to obtain the shunt's voltage spectrum [38]. To obtain steady-state results at high accuracy, the simulation needs to run in small time intervals. However, it also needs to run long enough for the shunt's thermal network to settle. Together, this can lead to prolonged simulation time. Instead of a time-based approach, modelling the temperature in the frequency domain allows for a direct computation of the low-order harmonic components.

### 6.2 Computation of intermodulation distortion

Most shunt resistors are specified with a worst case TCR over a given temperature range, for example $100 \mathrm{ppm} / \mathrm{K}$ from $0^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$, indicating a rise of resistance with temperature. The TCR is obtained by measuring the resistance at the beginning and end of the range, and then dividing the difference by the temperature delta [79]. Across this range, the resistance $R_{\mathrm{S}}$ of the shunt can then be expressed by

$$
\begin{equation*}
R_{\mathrm{s}}=R_{\mathrm{amb}}\left(1+\alpha T_{\mathrm{s}}\right) \tag{6.1}
\end{equation*}
$$

where $R_{\mathrm{amb}}$ is the resistance at a specified temperature, $T_{\mathrm{s}}$ the temperature deviation from this specified point and $\alpha$ the TCR. However, the resistance of a shunt depicted in Figure 6.2 demonstrates that a linear approximation fails to fully describe the shunt's behaviour. Due to material properties, the TCR itself varies over temperature [8]. This variation can be expressed as

$$
\begin{equation*}
\alpha=\alpha_{1}+\alpha_{2} T_{\mathrm{s}} \tag{6.2}
\end{equation*}
$$

with $\alpha_{1}$ as a temperature independent and $\alpha_{2}$ as a temperature dependent coefficient. Including this dependence in (6.1), yields

$$
\begin{equation*}
R_{\mathrm{s}}=R_{\mathrm{amb}}\left(1+\alpha_{1} T_{\mathrm{s}}+\alpha_{2} T_{\mathrm{s}}^{2}\right) \tag{6.3}
\end{equation*}
$$

Given this temperature dependence, the shunt's resistance depends on the thermal connection of the shunt to a cooling system and the power dissipated in the shunt.

For constant power dissipation, generated by a dc current $I_{s}$, the thermal connection can be modelled as a single resistance $R_{\text {th }}$. The shunt temperature can then be expressed as

$$
\begin{align*}
T_{\mathrm{s}}=R_{\mathrm{th}} R_{\mathrm{s}} I_{\mathrm{s}}^{2}=R_{\mathrm{th}} R_{\mathrm{amb}}\left(1+\alpha_{1} T_{\mathrm{s}}\right. & \left.+\alpha_{2} T_{\mathrm{s}}^{2}\right) I_{\mathrm{s}}^{2} \\
& \Rightarrow \alpha_{2} T_{\mathrm{s}}^{2}+\left(\alpha_{1}-\frac{1}{R_{\mathrm{th}} R_{\mathrm{amb}} I_{\mathrm{s}}^{2}}\right) T_{\mathrm{s}}+1=0, \tag{6.4}
\end{align*}
$$

which indicates the effect of self-heating within the shunt resistor. This quadratic equation, however, is only valid for dc currents.

Alternating currents require consideration of time dependent effects in the thermal network, as the shunt can heat up or cool down within cycles. Figure 6.3(a) depicts a shunt conducting an ac current of

$$
\begin{equation*}
i_{\mathrm{s}}(t)=\hat{i}_{\mathrm{s}} \sin \left(\omega_{0} t\right) \tag{6.5}
\end{equation*}
$$

with a peak value of $\hat{i}_{\mathrm{s}}$ and an angular frequency of $\omega_{0}$. As the power dissipation depends on the square of the current, both the positive and negative peak of $i_{\text {s }}$ lead to positive peaks in the temperature, essentially creating a temperature swing with double the fundamental frequency, illustrated in Figure 6.3(b). However, as the frequency increases, the temperature swing will decrease, due the thermal capacitances in the shunt. These capacitances, in combination with the thermal resistance create a low-pass filter. Figure 6.3(c) shows a Cauer model which can be fitted to represent the shunt's thermal characteristic.

(c)

Figure 6.3 Shunt used for current sensing. (a) The voltage measured across the shunt is proportional to current and resistance. However, the resistance itself depends on the temperature, which is linked to the current. (b) Temperature variation due to the load current. (c) Cauer model of the resistors thermal network.

For clarity, a single order network is used in the following equations, with a transfer function of

$$
\begin{equation*}
\mathrm{Z}_{\mathrm{th}}(j \omega)=\frac{R_{\mathrm{th}}}{1+j \omega \tau^{\prime}} \quad R_{\mathrm{th}}=R_{\mathrm{th}_{0}} \quad \tau=R_{\mathrm{th}_{0}} C_{\mathrm{th}}^{0} \tag{6.6}
\end{equation*}
$$

The shunt's temperature can now be written as a convolution in the time domain as

$$
\begin{equation*}
T_{\mathrm{s}}(t)=z_{\mathrm{th}}(t) * R_{\mathrm{amb}}\left[1+\alpha_{1} T_{\mathrm{s}}(t)+\alpha_{2} T_{\mathrm{s}}(t)^{2}\right] i_{\mathrm{s}}^{2}(t) \tag{6.7}
\end{equation*}
$$

where $z_{\mathrm{th}}(t)$ is the step response of the thermal network, with

$$
\begin{equation*}
z_{\mathrm{th}}(t)=R_{\mathrm{th}} e^{-t / \tau} \tag{6.8}
\end{equation*}
$$

Compared to the case of a dc current, the convolution in (6.7) makes a direct solution for ac currents difficult ${ }^{2}$. However, using certain assumptions, reasonable approximations of the shunt temperature, and thus distortion, are obtainable.

The problem of intermodulation distortion can be simplified significantly by neglecting the influence of the TCR on the power dissipation, but keeping it's influence on the shunt voltage. As the power dissipation is linear to the resistance, neglecting the TCR results in a power and thus worst case temperature error proportional to the TCR, with $T_{\text {error }} \sim T C R$. The resulting change in resistance is again proportional to

[^6]this temperature difference with $R_{\text {error }} \sim T C R \cdot T_{\text {error }} \sim T C R^{2}$. Overall, this leads to a voltage error proportional to the squared TCR. With a TCR of $100 \mathrm{ppm} / \mathrm{K}$ and a temperature swing of $10^{\circ}$ this already limits the worst case error to a factor of $1 \mathrm{e}-6$, or -120 dB . If this factor is below the required accuracy, ignoring the TCR for power dissipation still leads to a valid solution. In most practical applications, the influence is further diminished by damping of the temperature swings by the thermal network.

Now, assuming that the power dissipation is independent of temperature variation, the average junction temperature over a fundamental cycle $T_{s, a v g}$ can be determined by solving (6.4) with the rms value of $i_{\mathrm{s}}(t)$. Given the average temperature, the temperature profile of one load current cycle be approximated by

$$
\begin{equation*}
T_{\mathrm{s}}(t) \approx z_{\mathrm{th}}(t) * R_{\mathrm{amb}}\left(1+\alpha T_{\mathrm{s}, a v g}\right) \frac{\hat{i}_{s}^{2}}{4}\left(-e^{j 2 \omega_{0} t}+2-e^{-j 2 \omega_{0} t}\right) \tag{6.9}
\end{equation*}
$$

A Fourier transform of (6.9) and setting $\omega=n \omega_{0}$ yields

$$
\begin{equation*}
T_{n} \stackrel{\omega=n \omega_{0}}{\approx} \frac{R_{\mathrm{th}} R_{\mathrm{amb}}}{1+j n \omega_{0} C_{\mathrm{th}} R_{\mathrm{th}}}\left(1+\alpha T_{s, a v g}\right) \frac{\hat{i}_{s}^{2}}{4}\left[-\delta_{n-2}+2 \delta_{n}-\delta_{n+2}\right] \tag{6.10}
\end{equation*}
$$

as the complex Fourier-series coefficients of $T_{\mathrm{S}}(t)$, where $d_{n}$ is the discrete unit sample function. These functions show that the simplified temperature spectrum only contains a dc offset

$$
\begin{equation*}
T_{0}=R_{\mathrm{th}} R_{\mathrm{amb}}\left(1+\alpha T_{\mathrm{s}, a v g}\right) \frac{\hat{i}_{s}^{2}}{2} \tag{6.11}
\end{equation*}
$$

and a second harmonic component with the complex conjugate coefficients

$$
\begin{equation*}
T_{2}=-\frac{R_{\mathrm{th}} R_{\mathrm{amb}}}{1+j \omega_{0} C_{\mathrm{th}} R_{\mathrm{th}}}\left(1+\alpha T_{s, a v g}\right) \frac{\hat{i}_{s}^{2}}{4} \tag{6.12}
\end{equation*}
$$

and

$$
\begin{equation*}
T_{-2}=-\frac{R_{\mathrm{th}} R_{\mathrm{amb}}}{1-j \omega_{0} C_{\mathrm{th}} R_{\mathrm{th}}}\left(1+\alpha T_{s, a v g}\right) \frac{\hat{i}_{s}^{2}}{4} . \tag{6.13}
\end{equation*}
$$

The temperature can then be expressed in the time domain as

$$
\begin{equation*}
T_{\mathrm{s}}(t)=\sum_{n=-\infty}^{\infty} T_{n} e^{j \omega_{0} n t} \tag{6.14}
\end{equation*}
$$

Using the Fourier series of the temperature, it is possible to directly obtain the voltage spectrum across the shunt, given a sinusoidal current. The current is multiplied with the shunt resistance (6.3) and the temperature terms are replaced by their Fourier series, yielding

$$
\begin{align*}
& v_{\mathrm{s}}(t)=R_{\mathrm{amb}} \cdot\left[1+\alpha_{1} T_{\mathrm{s}}(t)+\alpha_{2} \cdot T_{\mathrm{s}}(t)^{2}\right] i_{\mathrm{s}}= \\
& \frac{R_{\mathrm{amb}} \hat{i}_{\mathrm{s}}}{2 j}\left(e^{j \omega_{0} t}-e^{-j \omega_{0} t}\right)\left[1+\alpha_{1} \sum_{n=-\infty}^{\infty} T_{n} e^{j \omega_{0} n t}+\alpha_{2}\left(\sum_{n=-\infty}^{\infty} T_{n} e^{j \omega_{0} n t}\right)^{2}\right] \\
& =\frac{R_{\mathrm{amb}} \hat{i}_{s}}{2 j}\left[\left(e^{j \omega_{0} t}-e^{-j \omega_{0} t}\right)+\alpha_{1} \sum_{n=-\infty}^{\infty} e^{j \omega_{0} n t}\left(T_{n-1}-T_{n+1}\right)\right. \\
& \left.\quad+\alpha_{2} \sum_{n=-\infty}^{\infty} e^{j \omega_{0} n t} \sum_{m=-\infty}^{\infty} T_{m}\left(T_{n-m-1}-T_{n-m+1}\right)\right] \tag{6.15}
\end{align*}
$$

Using the convolution theorem, the square of the junction temperature series can be expressed as a convolution with itself. For the final step, the indices inside the infinite sums are swapped between the exponential function and Fourier coefficients.

The voltage spectrum is obtained through a Fourier transform of (6.15), with the $n$-th element equal to

$$
\begin{align*}
V_{n}=\frac{R_{\mathrm{amb}} \hat{i}_{s}}{2 j}\left[\delta_{n-1}-\delta_{n+1}+\alpha_{1}\left(T_{n-1}\right.\right. & \left.-T_{n+1}\right) \\
& \left.+\sum_{m=-\infty}^{\infty} \alpha_{2} T_{m}\left(T_{n-m-1}-T_{n-m+1}\right)\right] \tag{6.16}
\end{align*}
$$

for the complex Fourier-series coefficients of the shunt voltage. In this case, the voltage spectrum contains first, third and fifth harmonic components, resulting from the dc and second order temperature components. The non-zero positive components are

$$
\begin{gather*}
V_{1}=\frac{R_{\mathrm{amb}} \hat{i}_{s}}{2 j}\left[1+\alpha_{1}\left(T_{0}-T_{2}\right)+\alpha_{2}\left(T_{0}^{2}+2 T_{-2} T_{2}-2 T_{0} T_{2}\right)\right]  \tag{6.17}\\
V_{3}=\frac{R_{\mathrm{amb}} \hat{i}_{s}}{2 j}\left[\alpha_{1} T_{2}+\alpha_{2}\left(2 T_{0} T_{2}-T_{2}^{2}\right)\right] \tag{6.18}
\end{gather*}
$$

and

$$
\begin{equation*}
V_{5}=\frac{R_{\mathrm{amb}} \hat{i}_{s}}{2 j} \alpha_{2} T_{2}^{2} \tag{6.19}
\end{equation*}
$$

The components for negative $n$ are the complex conjugate of their respective positive component. Figure 6.4 shows the voltage spectrum of a $5 \mathrm{~m} \Omega$ shunt resistor obtained with the proposed closed-form spectral computation, compared to simulation in PLECS.


Figure 6.4 Spectrum of the shunt voltage for different load frequencies obtained through simulation (bars) and computation (dots). The higher harmonics are filtered by the shunt's thermal capacitance.

PLECS is a commercial solver for dynamic and switched state-space models, able to model the time-dependent behaviour of electronic components [2]. The timeintervals at which PLECS solves the system state are determined by a prescribed tolerance. If strict tolerances are required to observe low distortion levels, the simulation time increases significantly. In contrast, the closed-form spectral computation only requires to solve (6.16) for $n=1,3,5$. The precision is determined by the utilized data type, i.e. float or double. The match of closed-form spectral computation and simulation shows that the impact of temperature dependent power dissipation on the shunt's temperature is negligible. Simplification of the power losses leads to a solution with no seventh or higher harmonic, but given the low-pass behaviour of the shunt, it is guaranteed that any higher harmonic is smaller than the fifth. Furthermore, even the magnitude of the fifth harmonic is of little concern for realistic scenarios, even at very low fundamental frequencies. In fact, the fifth harmonic is can sink below the inherent thermal noise of the resistor. The thermal noise level, described in [27], is obtained through

$$
\begin{equation*}
v_{\text {noise }}=\sqrt{4 k_{\mathrm{B}} T_{\mathrm{s}} R_{\mathrm{s}} f_{\mathrm{BW}}} \tag{6.20}
\end{equation*}
$$

Given a bandwidth $f_{\mathrm{BW}}$ of 1 MHz and an ambient temperature of 300 K , the thermal noise is above the fifth harmonic for 1 Hz or higher frequencies, with a value of -160 dB . Still, measuring voltages at this level would require an effective resolution of at least 26 bits, far off from any currently conceivable practical application.

Figure 6.5 shows the THD over varying thermal resistance, obtained with the proposed closed-form spectral computation and time-based simulation in PLECS. The distortion of the time-based waveforms is calculated internally in PLECS. Computation and simulation agree very well, except for a THD below -120 dB . This


Figure 6.5 Calculated THD of the shunt voltage over varying thermal resistance. The marks show time-based simulation results done with PLECS. The mismatch for 100 Hz is attributed to the numerical precision of PLECS.
deviation can be attributed to numerical errors due to the solver precision of PLECS. Contrary to intuition, an increase in thermal resistance does not necessarily increase the THD. This behavior can be attributed to two factors. Initially one would think that an increase in thermal resistance of the shunt results in higher temperature swings, which would increase the distortion. However, a higher thermal resistance also increases the time constant of the resistor's thermal network, which, at high frequencies, dampens the temperature swing and thus reduces distortion. This effect is encapsulated in (6.10), as the thermal resistance $R_{\text {th }}$ appears in both the nominator and the denominator. The second aspect is the quadratic temperature coefficient of the resistor. Given a negative $\alpha_{2}$, the TCR of the resistor decreases at higher temperatures, again reducing distortion. The exact match with simulation results makes the direct computation viable. However, to see whether such simulation and computation are a good behavioral representation of real components, the results need to be verified by experiments.

### 6.3 Experimental verification

This section demonstrates how well the analytic solutions match with experimental observation. One problem with the verification is the low distortion of high-precision shunt resistors. As demonstrated in the previous section, a level well below -100 dB is achievable. To provide accurate measurements of the distortion caused by the shunt, the distortion of the used test current must be significantly lower. Given this limit, the presented experiment is designed to characterize shunts with a distortion of up to -80 dB . The goal is to verify the proposed computation method for various shunt resistances and frequencies.


Figure 6.6 Shunt verification board. Each of the four resistors is measured through a four point connection. Thermal vias conduct the heat through the PCB, the backside of which is mounted against a heatsink. Vertical slots in the PCB are used to decouple a resistor from its neighbours.


Figure 6.7 Push-pull class-A stage used to generate a test current with low distortion. The output current is controlled through an analog PI controller, which follows a reference provided by a high precision DAC.

To cover multiple resistance values as well as package sizes, the board depicted in Figure 6.6 was used. The board is populated with four shunts, each with connectors for a four-terminal voltage measurement. The shunts are cooled through the PCB, with the backside mounted against an over-sized heatsink. The large thermal mass of the heatsink acts as a constant temperature source and allows to simplify the shunt's thermal model. The thermal network of the shunts is modeled by a second order Cauer network, being characterized by experiment, for the two packages WSK2512 [64] and WSL3637 [65]. The distortion was measured at various frequencies, set at the current source. As stated earlier, the current source needs to have a distortion below the expected shunt distortion, as to not significantly affect the measurement. The experiment was carried out with a linear amplifier, consisting of two class A stages in a push-pull configuration, as depicted in Figure 6.7. The amplifier's output current was measured with an IT 60-S Ultrastab from LEM and used as feedback for an analog PI controller, which controls the push-pull stage.


Figure 6.8 Test setup. The output of the linear amplifier is measured with a fluxgate sensor (LEM IT 60-S Ultrastab), to provide feedback for an analog PI controller (Texas Instruments OPA1612) driving the amplifier. The reference is generated by a 22-bit DAC (Applicos ATX7006A).

Thus, the linearity of the setup is inherently limited by the sensor's precision. The reference for the controller was generated with an Applicos ATX7006A, using the 22-bit waveform generator. The whole setup is shown in Figure 6.8.

The amplifier is able to generate a 20 A sine wave with a distortion of less than -100 dB at 100 mHz . However, with increasing frequency the amplifier's distortion rises at a rate of 20 dB per decade due to the first-order control loop. As the distortion across the shunts is expected to decrease with frequency, conclusive statements can be made only at low frequencies, before the amplifier's distortion and the shunt's distortion cross over. The shunt voltage was measured with the 20-bit digitizer channel of the APX2000, synchronous to the reference generation, with a noise floor below -110 dB . Prior to measuring the distortion, the thermal drift and thermal network of each shunt was identified. First, the temperature dependence of each shunt was characterized in a thermal chamber. The chamber swept the temperature from $0^{\circ} \mathrm{C}$ to $100^{\circ} \mathrm{C}$ over a span of 20 minutes and the shunt temperature was monitored with a thermocouple attached to each shunt element. The resistance of the shunts was measured with a 1 A current passing through each shunt and the resulting voltage drop was measured with a twisted pair, soldered directly to each package ${ }^{3}$. The measurement results are depicted in Figure 6.9, with the resistance

[^7]

Figure 6.9 Temperature characterization of the four shunt resistors in the thermal chamber. The test current to measure the resistances is 500 mA , resulting in negligible power loss of several mW .
normalized to room temperature.
Each shunt displays a positive temperature coefficient slightly dropping of towards higher temperature, most noticeable in the $2 \mathrm{~m} \Omega$ resistor. Each curve was fitted to a second order polynomial according to (6.3), with the resulting coefficients listed in Table 6.1. Given $R_{\mathrm{amb}}$ and $\alpha_{1}$, each resistor is within specification of the datasheet regarding accuracy and drift. With the TCR determined for each resistor, the thermal network can be measured and quantified.

The resistors equivalent thermal network was obtained in two steps. First, the sum of all thermal resistances was determined by applying a dc current $I_{\mathrm{dc}}$ to generate the maximum rated power for each resistor and measuring the difference in resistance compared to ambient temperature. The measured difference in resistance was converted to an observed temperature difference $\Delta T$ using the polynomial fit of each shunt. The shunt's total thermal resistance was then obtained through

$$
\begin{equation*}
R_{\mathrm{th}}=\frac{\Delta T}{R_{\mathrm{s}} I_{\mathrm{dc}}^{2}} \tag{6.21}
\end{equation*}
$$

The second step determines each element of the Cauer thermal network, by observing the transient thermal response to a pulsed power dissipation. To inject power, each resistor was heated with a hot-air gun, using a 2 mm nozzle focused on the resistive element ${ }^{4}$. After turn-off of the heat source, the resulting response of each shunt is measured and depicted in Figure 6.10.

[^8]Table 6.1 Shunt resistor characterization

| Resistor | max. TCR | $R_{\mathrm{amb}}(\mathrm{m} \Omega)$ | $\alpha_{1}\left(\frac{1}{\mathrm{~K}}\right)$ | $\alpha_{2}\left(\frac{1}{\mathrm{~K}^{2}}\right)$ |
| :---: | :---: | :---: | :---: | :---: |
| WSK2512 $2 \mathrm{~m} \Omega$ | $\pm 250 \mathrm{ppm}$ | 2.008 | 112.3 ppm | -0.31 ppm |
| WSK2512 $4 \mathrm{~m} \Omega$ | $\pm 75 \mathrm{ppm}$ | 4.005 | 58.2 ppm | -0.05 ppm |
| WSL3637 $5 \mathrm{~m} \Omega$ | $\pm 50 \mathrm{ppm}$ | 4.976 | 19.6 ppm | -0.03 ppm |
| WSL3637 $10 \mathrm{~m} \Omega$ | $\pm 50 \mathrm{ppm}$ | 9.996 | 28.6 ppm | -0.04 ppm |

Table 6.2 Thermal impedance fit

| Resistor | $R_{\text {th }}\left(\frac{\mathrm{K}}{\mathrm{W}}\right)$ | $T_{\mathrm{amb}}(\mathrm{K})$ | $q_{0}(\mathrm{~W})$ | $A_{1}\left(\frac{\mathrm{~K}}{\mathrm{~W}}\right)$ | $A_{2}\left(\frac{\mathrm{~K}}{\mathrm{~W}}\right)$ | $\tau_{1}(\mathrm{~s})$ | $\tau_{2}(\mathrm{~s})$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| WSK2512 $2 \mathrm{~m} \Omega$ | 35.07 | 19.68 | 1.32 | 25.19 | 7.65 | 2.72 | 0.37 |
| WSK2512 $4 \mathrm{~m} \Omega$ | 38.83 | 19.19 | 0.96 | 29.06 | 11.96 | 2.89 | 0.6 |
| WSL3637 $5 \mathrm{~m} \Omega$ | 37.26 | 20.3 | 0.99 | 31.41 | 6.17 | 3.12 | 0.89 |
| WSL3637 $10 \mathrm{~m} \Omega$ | 41.21 | 20.65 | 0.71 | 27.14 | 15.67 | 3.57 | 0.75 |

Using the method proposed in [4,5], the temperature responses are used to fit a second order Cauer model to each shunt. First, the transient response is numerically fitted to

$$
\begin{equation*}
T_{\mathrm{s}}(t)-T_{\mathrm{amb}}=q_{0}\left(A_{1} e^{-\frac{t}{\tau_{1}}}+A_{2} e^{-\frac{t}{\tau_{2}}}\right) \tag{6.22}
\end{equation*}
$$

which describes the temperature decline as a sum of two exponential functions with two different amplitudes $A_{1}, A_{2}$ and time constants $\tau_{1}, \tau_{2}$. The power injected by the hot-air gun $q_{0}$ is determined by dividing the peak temperature of the shunt by the previously established total thermal resistance. The coefficients are listed in Table 6.2. After the numerical calculation of all coefficients, the Fourier transform of (6.22) yields the fitted thermal impedance

$$
\begin{equation*}
Z_{\mathrm{s}}(j \omega)=R_{\mathrm{th}}-\frac{j \omega A_{1} \tau_{1}}{1+j \omega \tau_{1}}-\frac{j \omega A_{2} \tau_{2}}{1+j \omega \tau_{2}}, \tag{6.23}
\end{equation*}
$$

which is equated to the thermal impedance of the Cauer network

$$
\begin{equation*}
Z_{\mathrm{s}}(j \omega)=\frac{j \omega C_{2} R_{1} R_{2}+R_{1}+R_{2}}{(j \omega)^{2} C_{1} C_{2} R_{1} R_{2}+j \omega\left(C_{1}\left(R_{1}+R_{2}\right)+C_{2} R_{2}\right)+1} \tag{6.24}
\end{equation*}
$$

All coefficients are listed in Table 6.3. Interestingly, the resistances $R_{1}$ increase significantly with the increased nominal resistance for both package sizes. This coincides with the resistor's construction, as cuts within the element are used to create the nominal resistance [63].


Figure 6.10 Pulse test to identify the dominant time constant of the thermal network. Measured temperature (solid line) and exponential fit (dashed). The resistors are heated with a hot air gun using a 2 mm nozzle focused on the resistive element and the resistance deviation is measured using a current of 1 A . With resistors in the $\mathrm{m} \Omega$ range, the test current causes only miniscule power loss, and is neglected in any further temperature calculations.

Table 6.3 Equivalent Cauer network


Figure 6.11 Thermal impedances extracted from the pulse test. The parameters are determined by fitting the previously measured exponential decay against the impulse response of a lumped element model.

Next, the frequency response of each network is depicted in Figure 6.11. The low frequency behaviour is determined by the total thermal impedance, where the $2 \mathrm{~m} \Omega$ resistor has the lowest impedance. At higher frequencies, the thermal capacitances come into effect, causing a -20 dB per decade roll-off. The larger internal capacitance of the WSL3637 package causes the roll-off to occur sooner for the $5 \mathrm{~m} \Omega$ and $10 \mathrm{~m} \Omega$ resistors, offering more damping of thermal swings at higher frequencies.

After the thermal network is identified, the distortion in each shunt is measured using the linear amplifier for a set of frequencies. The test frequencies are chosen such that the harmonics are distinct from any background noise specifically at 50 Hz . In addition, one cycle of the current contains 32678 samples to allow accurate calculation of the spectrum. The harmonics are obtained by measuring a single cycle after several seconds of continuous operation, to ensure steady-state of the thermal network is reached. At 196 Hz , the average of ten consecutive cycles was taken. To achieve the largest possible measurement accuracy, the amplitude was set to the maximum of 20 A . Due to setup limitations, measurement at larger currents was not feasible. At lower amplitudes the effect of intermodulation distortion became difficult to observe. Furthermore, the setup illustrates the problem addressed in Section 3.1. The controller uses the flux-gate sensor for feedback, assuming the


Figure 6.12 Distortion measurement of shunt current (black, circle) and voltage (color, cross). At low frequencies the shunt voltage shows an increase in THD due to intermodulation effects. At higher frequencies the inherent distortion of the setup becomes dominant. Error bars (black, dash) show worst case current distortion resulting from the flux-gate sensor's non-linearity of 20 ppm .


Figure 6.13 Measured voltage spectra (bars) and computations (dots) across the shunt resistors for 196 mHz and 1.96 Hz . The third harmonic from intermodulation distortion is evident in each resistor and matches the computation results. The fifth harmonic of each shunt is likely below the noise floor of the amplifier, as indicated by the computation.
sensor's output is the exact value of the current. However, a flux-gate sensor also contains non-linearity in its output, in this setup an error of 20 ppm full scale. Since the shape of this non-linearity is unknown, the error for the shunt voltage measurements is obtained by attributing the full non-linearity to every harmonic component.

The results for each resistor are shown in Figure 6.12. As indicated earlier, at low frequencies the added distortion from self-heating is evident. However, as the distortion from self-heating is expected to decrease with frequency, and the amplifier distortion increases with frequency, no observation of intermodulation distortion is possible at higher frequencies.

For 196 mHz and 1.96 Hz , where the measurements are conclusive, the individual harmonics are shown in Figure 6.13 and compared against results of the closed-form spectral computation as well as simulation results. The measurements all show a pronounced third harmonic, which matches the calculation and simulation results. In contrast to the analytic solution and simulation, significant even ordered components can be seen in the shunt voltage. Their amplitude is within the possible error attributed to the fluxgate sensor, but most likely other components also contribute to the underlying noise floor. Judging from the calculation and simulation results,
the fifth harmonic is too small and disappears below this noise floor. As the noise is less than the possible error, the upper error bound on the respective harmonics is more than 10 dB above the measured value. At the same time, the error could be negative enough to exactly cancel the measured amplitude, resulting in a theoretical lower error bound of $-\infty \mathrm{dB}$. For most of the 3rd harmonics however, the signal is large enough to have upper and lower error bounds within a few dB. At 196 mHz more conclusive statements can be made as the measurements are further above the amplifiers noise floor.

The $5 \mathrm{~m} \Omega$ has the lowest third harmonic of -78 dB , which agrees with the TCR measurements, where it showed the smallest temperature dependence of all tested resistors. In contrast, the $10 \mathrm{~m} \Omega$ device, with only a slightly worse TCR, shows a higher third harmonic of -73 dB , as the power dissipation is doubled. Between the $5 \mathrm{~m} \Omega$ and $4 \mathrm{~m} \Omega$ resistors, where the power dissipation is similar, the higher TCR and lower time constant of the $4 \mathrm{~m} \Omega$ device result in a third harmonic of -71 dB . The $2 \mathrm{~m} \Omega$ device, with even worse TCR, has nearly the same distortion at -73 dB , as it only dissipates half of the power. At 1.96 Hz , the measured distortion is higher than expected for three of the four resistors. While within the negative error bars, this is likely due to a mismatch in the thermal model. As shown in Figure 6.11, the second order component of the thermal network becomes dominant before 1.96 Hz . A slight mismatch in the fitted model can result a significant change in thermal impedance at higher frequencies, and thus different results for the calculated distortion.

### 6.4 Conclusion

As demonstrated, the distortion in shunt resistors resulting from self-heating can be calculated accurately including typical non-linear effects. The results are obtained directly in the frequency domain, skipping Fourier transforms of time-based temperature simulations and potential errors due to numerical precision. The analytic solution matches numeric simulation accurately, while computation is several orders of magnitude faster. This enables a quick search for a suitable resistor for low-distortion current measurements.

For an inverter with a specified maximum output distortion and frequency range, the closed-form spectral computation can be used to see if a specific shunt adds acceptable distortion in this range. This allows to select a component based on their expected distortion for the application, instead of over-dimensioning by choosing a shunt resistor with an extremely low TCR. The theoretical findings are confirmed through experiments, where a linear amplifier with an output distortion of -90 dB was used to observe self-heating distortion in different shunt resistors with TCRs of 50 ppm to 250 ppm . For low frequencies, distortions of up to -70 dB are measured,
matching the results from the presented computation method as well as simulation. If required, the harmonic-balance method presented in chapter 2 can be used for more precise results.

# 7 <br> Inverter design for high-precision positioning systems 

"There is a way out of every box, a solution to every puzzle; it's just a matter of finding it."

Jean-Luc Picard

WITH the knowledge established in the previous chapters, a high-precision amplifier for semiconductor lithography is designed, implemented and teste=d. As shown in the preceding chapters, effects on noise and current ripple are highly operating point dependent, and the topology as well as components should be tailored for a given application. In this case, a single phase short-stroke actuator. To drive the actuator, a two-phase interleaved full-bridge inverter with coupled-inductors is selected as the topology. Full dynamic control of the two coupled inductor currents is realized and experimentally validated using decoupled controllers for the summed and differential current. The output current capability of the prototype is tested by following the reference current necessary to drive a short-stroke amplifier.


Figure 7.1 Fourth-order motion profile of a motion stage. By having a finite fourth derivative, the motion introduces little to no mechanical ringing in the application.


Figure 7.2 Simplified position loop. The position is controlled through the actuator current. The power amplifier should follow the reference as close as possible to minimize the position error.

### 7.1 Motion profile and controller

Figure 7.1 shows a standard fourth order motion profile used in a lithography machine. The wafer stage is accelerated and the lithography process, i.e. the scanning phase, begins once constant velocity is achieved. During scanning, the position error directly influences the attainable accuracy of the process, and thus achievable feature size. It is the task of the position controller to ensure a small enough error. A simplified model of the position controller is depicted in Figure 7.2. The simplified model focuses solely on the short-stroke actuator. As explained in chapter 1 , it is the long-stroke actuator which supplies the kinetic energy to the wafer stage. However, the short-stroke actuator has to exert a force to maintain the position of the wafer stage. This force and acceleration is directly linked to the actuator current through the actuator's moving mass $m_{\text {act }}$ and force constant $k_{\text {act }}$. The link between the actuator and position controller is the power amplifier. Its job is to follow the current reference as close as possible. Any discrepancy will directly increase the position error. Modern lithography machines allow for errors contributed by the power amplifier below 20 picometer. The goal is to design a power amplifier that can supply the requested current, within the allowed error, fast enough. In other terms: power, precision and bandwidth.

### 7.2 Inverter design

The design goal is an amplifier operating at 400 V and a peak output current of 18 A . To maintain position accuracy, the output current has to be controlled at a bandwidth of 10 kHz . The realized topology is depicted in Figure 7.3. The actuator is driven by a two-phase interleaved full-bridge with coupled filter inductors operated at a switching frequency of 400 kHz . Specifically for the short-stroke actuator, using an even number of interleaved legs shows several benefits. During the scanning phase,


Figure 7.3 Two-phase interleaved full-bridge inverter. The filter inductors are coupled to achieve reduced current ripple at zero output voltage.

Table 7.1 Amplifier specification

| Parameter | Symbol | Value |
| :---: | :---: | :---: |
| Switching frequency | $f_{\mathrm{sw}}$ | 400 kHz |
| Supply voltage | $V_{\mathrm{dc}}$ | 400 V |
| Peak output current | $I_{\mathrm{O}}$ | 20 A |
| Filter self-inductance | $L_{\mathrm{s}}$ | $228 \mu \mathrm{H}$ |
| Filter coupling coefficient | $k$ | -0.82 |
| Filter capacitance | $C_{\mathrm{o}}$ | $1.6 \mu \mathrm{~F}$ |
| Filter damping resistance | $R_{\mathrm{d}}$ | $1.2 \Omega$ |
| Actuator resistance | $R_{\mathrm{act}}$ | $2.5 \Omega$ |

the output current and thus differential output voltage is maintained near zero. At this operating point, an even number of phases show high cancellation of the input and output current ripple, which in turn reduces the voltage ripple present on the input and output of the amplifier. Moreover, coupling of the filter inductors also leads to reduction of the phase current ripple, which leads to decreased noise in the phase current measurement and reduced conduction losses in the transistors.

The fully realized amplifier is depicted in Figure 7.4. To increase overall power density in the power cabinets, two amplifiers share the same input supply and coldplate. The entire design is mirrored across the plane of the coldplate. The front board carries the input capacitors, as well as the output filters of the two amplifiers. An interface board in the back allows connection to the control platform. The specification of the amplifier is given in Table 7.1.

The following sections discuss each functional block of the inverter in detail.

### 7.2.1 GaN half-bridge

The individual half-bridges, depicted in Figure 7.6(a), are implemented using the GS66508T from GaN Systems, a $50 \mathrm{~m} \Omega \mathrm{GaN}$ HEMT with a rated breakdown voltage


Figure 7.4 Realized power amplifier. For high power-density of the entire power electronics cabinet, two amplifiers share the same isolated supply and coldplate.
of 650 V . The device is selected through analysis with harmonic balance, depicted in Figure 7.5. The plots show the operating point of the high-side devices supplying the positive phase currents $i_{\mathrm{p}_{1}}$ and $i_{\mathrm{p}_{2}}$, as well as the low-side devices supplying the negative phase currents $i_{\mathrm{n}_{1}}$ and $i_{\mathrm{n}_{2}}$. Due to symmetry of the topology and waveforms, the other devices show the same temperature and loss profile mirrored around the center of the motion profile. Compared to a smaller and larger GaN device from the same manufacturer, the selected device offers a good trade-off between total device losses and peak-to-peak junction temperature. While the smaller device is overall more efficient, the reduced size also leads to a smaller thermal interface and larger temperature swing. In contrast, the larger device offers a much better thermal interface, but the large increase in switching losses offsets any benefit in temperature swing.

Operating at a high switching frequency, the devices need to be cooled sufficiently. To achieve high heat-removal in a confined space, water-cooling is used. The thin cold-plate, depicted in Figure 7.6(b) is mounted below the PCB, and each transistor is connected through an electrically insulating thermal interface. Design of the thermal interface needs to take the added parasitic capacitance into account. To reach a low parasitic capacitance while maintaining low thermal resistance, 0.6 mm aluminiumnitride ceramic sheets are used to electrically insulate each device. Thermal contact between all layers is made using soft indium sheets, which conforms to rough surfaces. Remaining air gaps between two surfaces are filled, ensuring a good thermal connection. The entire thermal path has a junction-to-coolant thermal resistance of


Figure 7.5 Operating point of the positive-phase high-side transistors in a continuous cycle of half the reference current. The temperature, as well as conduction and switching losses are evaluated for three different GaN devices at a switching frequency of 400 kHz .

(b)

Figure 7.6 (a) Stackup of interleaved half-bridges and cold-plate. (b) 3d-printed stainless-steel watercooled coldplate. The maximum wall thickness between surface and coolant is $150 \mu \mathrm{~m}$. Pin fins are inside the section where the insulated devices make contact with the coldplate's surface.
$1.4 \frac{\mathrm{~K}}{\mathrm{~W}}$ and a parasitic capacitance of less than 3 pF , as experimentally verified in [71]. Considering the transistor's internal junction-to-case resistance contributes $0.5 \frac{\mathrm{~K}}{\mathrm{~W}}$, further optimization on any external part will only yield diminishing returns in overall thermal resistance.

As the GaN devices are only 0.6 mm in height, the dc-link capacitors are mounted on the opposite side of the PCB, which comes at the cost of slightly increased power loop inductance. The internal layers are used to connect the dc-supply to each halfbridge. The internal layer closest to the transistors is used to route a kelvin-source connection to the gate driver.

Each transistor gate is driven by a LMG1025 from Texas Instruments, with a fully isolated supply per driver. Due to the low gate capacitance of GaN , driving the gate consumes little power compared to SiC or Si devices. Thus, the supply voltage for each gate driver is provided by a UCC12050 from Texas instruments, an integrated 500 mW isolated dc/dc converter in a SOIC-16 package. The supplies low isolation capacitance of 2 pF is critical, as the high-side driver supply is subjected to the fast voltage slopes of the switching node and a parasitic current is induced through the isolation barrier.

To further isolate the control system from the induced current, the input of the


Figure 7.7 (a) Interlock gate driver circuit. The additional isolator between high and low-side driver disables one transistor while the other is turned on. The propagation delay across the driver thus results in a minimal dead-time before the transistors can turn on. (b) Timing diagram of the interlocked drivers. When a larger dead-time is applied by the control system, the circuit has no impact on the timing of the drivers.
high-side driver supply is sourced from the already isolated low-side driver supply. This eliminates the most significant parasitic capacitance from the switching node to the control system. However, the low-side supply needs to be able to supply the input power for both the high-side supply as well as the gate driver. To send transfer the gate-signals from the control system to the gate-drivers, low-capacitive digital signal isolators are used. The selected component, the MAX2234x from Analog Devices, has a worst case propagation delay below 10 ns , at an rms jitter of 7.5 ps .

Due to the low propagation delay, and low part-to-part skew, the dead-time can be set to 20 ns . To protect against accidental cross-conduction, another digital isolator is added between the low and high-side drivers, as depicted in Figure 7.7(a). The concept closely follows the principle shown in [34], where the conduction state of one IGBT is transmitted through an isolated connection and blocks the turnon of the opposing device. The result is a minimum dead-time, which prevents cross-conduction.

When applying the concept to GaN , the gate voltage matches the operating voltage of the digital isolators, which allows a direct connection of the driver output to the isolator. The isolated driver output is then applied directly to the inverting input of the opposing driver, inhibiting accidental turn-on. The resulting switching patters are depicted in Figure 7.7(b). With a dead time $T_{d}$ applied to the driver inputs, the interlock will not affect the timing. If the applied dead time is shorter than the interlock delay $T_{\mathrm{i}}$ or there is no dead time applied at all, the interlock will take effect and insert the interlock delay between turn-off and turn-on. The operation is verified


Figure 7.8 (a) Core cross-section and winding arrangement. The core is constructed by combining two planar E and I cores. The center and outer gap are adjusted to obtain the desired coupling coefficient and saturation current. (b) Core saturation for varying center gap and number of tuns per winding, at a dc bias of 10 A . The implemented design is marked in red, with a gap of 1.4 mm and 9 turns per winding. The used material is 3F36 from Ferroxcube, with a relative permeability of $\mu_{r}=1600$.
experimentally in [70]. A low dead-time is critical for operation at high switching frequency, as it has detrimental effects on distortion and operating efficiency [80].

### 7.2.2 Coupled inductor

As described in [25], a two-phase coupled inductor can be implemented with a set of 'E' and 'I' cores as depicted in Figure 7.8(a). The coupling coefficient can be tuned through the center gap. Addition of an outer gap allows to increase the saturation current, but it also affects the coupling coefficient. Figure 7.8(b) shows the saturation percentage of the magnetic material at a dc bias of 10 A . In this case, a center gap is sufficient to achieve a viable design. In case no suitable gap configuration is feasible, addition of a third gap is possible, as described in [19]. With the use of fully custom cores, further volume reduction is possible [48]. The realized coupled inductor is depicted in Figure 7.9, with a self-inductance of $228 \mu \mathrm{H}$ at a coupling coefficient of -0.82 . The core size of E43 was chosen as it was the smallest core to realize a coupled inductor with a saturation current of 15 A , while providing sufficient inductance. To maintain equal current sharing between the two windings, the output voltage and inductor currents are measured and regulated.


Figure 7.9 Two-phase coupled inductor, constructed from two E43 and PLT43 ferrite cores, with the material 3F36 from Ferroxcube. The coupled inductor has a self-inductance of $228 \mu \mathrm{H}$ and a coupling coefficient of -0.82 .


Figure 7.10 Two channel isolated current measurement. The currents are measured through four-terminal shunt resistors terminated to the same ground. The output voltage of each shunt is amplified through a multiple feedback low-pass filter and connected to the respective ADC. Each ADC has a resolution of 18 -bit and a sample-rate of up to 15 MSPS. The conversion result is transmitted through digitally isolated LVDS channels. The supplies for the analog and digital section are generated by separate isolated DC/DC converters on the back of the board.

### 7.2.3 Voltage and current measurements

The input and output voltages are measured through resistive voltage dividers, by internal ADCs of the control platform at a resolution of 16-bit and a sample-rate of 800 kSPS synchronous to the triangular PWM carrier. The actuator current is measured with a flux-gate sensor (Hioki CT6904A), which provides a galvanically isolated measurement at a linearity of 5 ppm at a bandwidth of up to 4 MHz . As the sensor is rated for a maximum of 500 A , sixteen turns are wired through the sensor to achieve a larger output amplitude with the relatively low load current of 20 A . The output of the flux-gate sensor is also measured by the internal control platform at a resolution of 16 -bit and a sample-rate of 800 kSPS . The signal is low-pass filtered with a cut-off frequency of 25 kHz to gain more resolution.

The inductor currents are measured by isolated ADCs referenced to the respective output capacitor. Implemented in separate pairs, each pair of ADCs has a fully isolated supply, isolated digital LVDS interface and a preamplifier, to adjust the respective shunt output to its input range. One of the implemented current measurement boards is depicted in Figure 7.10. The shunts are $5 \mathrm{~m} \Omega$ four terminal resistors, with a power dissipation rating of 3 W . The voltage across the two sense terminals is amplified by a multiple-feedback filter with gain of 10, realized with an ADA4895 operational amplifier from Analog Devices. Each ADC is an integrated acquisition solution from Analog Devices (ADAQ23878), with internal differential amplifier, reference voltage and conversion circuit. The attainable resolution is 18 -bit, at a sample-rate of up to 15 MSPS . With an input range of $\pm 20 \mathrm{~A}$, this leads to a resolution of $76.3 \mu \mathrm{~A}$. However, the actual resolution will be limited by noise sources in the system. The conversion result is passed through an isolated, serial LVDS interface to the control system (ADN4650), contributing an rms jitter of 2.6 ps . The analog section is supplied by a 6 W fully isolated dc/dc converter (Murata MGJ6), plugged in to the back of the board. The LVDS interface is powered by two integrated 3.3 V dc/dc converters (UCC12050).

Together with the rms jitter of the gate driver, the filter inductance of $227 \mu \mathrm{H}$ and coupling factor of -0.82 , the expected jitter related noise on samples during the scanning is calculated with (5.8). At $38.8 \mu \mathrm{~A}$, the jitter related white noise is below the theoretical resolution of the ADC. However, the unknown propagation delay between gate drivers and ADC interface is in the order of nanoseconds. The error caused by this delay, obtained through (5.4), is at 4.9 mA for each unaccounted nanosecond. However, as control bandwidth is critical, the proposed weighting is not implemented. As weighting of two consecutive samples comes at the cost of one unit delay in the feedback path, the proposed compensation method is more suited for applications with lower bandwidth requirements. As the error appears averaged in the inductor current, it will be compensated by the subsequent controllers in the control loop.


Figure 7.11 (a) Equivalent circuit for two coupled inductors [46]. They are connected between an output voltage $v_{\text {out }}$ and square wave sources at $180^{\circ}$ phase shift with a voltage of $v_{\text {in }}$ and duty cycles of $d_{1}$ and $d_{2}$ respectively. (b) Modulation strategy for decoupled control of output and circulating current.

### 7.3 Control

As the current and voltage of every component is measured, each state can be controlled by its individual controller. The control of the filter currents and output voltages are shown for the positive phase. This approach leads to a series of three cascaded control loops, for the actuator current, output voltage and phase currents. A fourth, independent controller regulates the current circulating between the two coupled inductors. Each controller is designed in the continuous time domain with continuous plant models, followed by discretization of the resulting transfer functions.

### 7.3.1 Decoupled control of coupled inductor

The currents of the coupled inductor are separated into the summed output

$$
\begin{equation*}
i_{\Sigma}=i_{\mathrm{p}_{1}}+i_{\mathrm{p}_{2}} \tag{7.1}
\end{equation*}
$$

and circulating current

$$
\begin{equation*}
i_{\Delta}=i_{\mathrm{p}_{1}}-i_{\mathrm{p}_{2}} \tag{7.2}
\end{equation*}
$$

for fully decoupled control.
The dutycycles of the half-bridges $d_{\mathrm{p}_{1}}$ and $d_{\mathrm{p}_{2}}$ are separated into two components with

$$
\begin{equation*}
d_{\mathrm{p}_{1}}=d_{\Delta}+d_{\Sigma} \quad \text { and } \quad d_{\mathrm{p}_{2}}=d_{\Delta}-d_{\Sigma} \tag{7.3}
\end{equation*}
$$

The dutycycle corresponds to the steady-state output voltage, such that a small signal approximation only needs to consider $d_{\Delta}$ and $d_{\Sigma}$. To simplify the model, for


Figure 7.12 Control-loop diagram. By controlling each filter component individually, the controllers can be designed with additional dc gain for increased error rejection.
now $d_{\mathrm{p}_{1}}$ and $d_{\mathrm{p}_{2}}$ are assumed to be below 0.5 . Given this limit, during a switching event the opposing switching node is guaranteed to be at 0 V , and a variation of $d_{1}$ or $d_{2}$ can be analyzed using the two models depicted in Figure 7.11. Analysing the system at $d_{\mathrm{p}_{1}}$ and $d_{\mathrm{p}_{2}}$ above 0.5 and the respective switching node at $v_{\text {in }}$ yields the same transfer function. The system can be represented by a set of linear equations such that

$$
\binom{\frac{d i_{\mathrm{p}_{1}}}{d t}}{\frac{d i_{\mathrm{p}_{2}}}{d t}}=v_{\text {in }}\left(\begin{array}{cc}
\frac{1}{L_{\mathrm{s}}\left(1-k^{2}\right)} & -\frac{k}{L_{\mathrm{s}}\left(1-k^{2}\right)}  \tag{7.4}\\
-\frac{1}{L_{\mathrm{s}}\left(1-k^{2}\right)} & \frac{1}{L_{\mathrm{s}}\left(1-k^{2}\right)}
\end{array}\right)\binom{d_{\mathrm{p}_{1}}}{d_{\mathrm{p}_{2}}} .
$$

This set can be replaced by the proposed $d_{\Delta}$ and $d_{\Sigma}$, and the corresponding sum and circulating current $i_{\Delta}$ and $i_{\Sigma}$, such that

$$
\binom{\frac{1}{2} \frac{d i_{\Sigma}}{d t}+\frac{1}{2} \frac{d i_{\Delta}}{d t}}{\frac{1}{2} \frac{d i}{d t}-\frac{1}{2} \frac{d i_{\Delta}}{d t}}=v_{\text {in }}\left(\begin{array}{cc}
\frac{1}{L\left(1-k^{2}\right)} & -\frac{k}{L_{\mathrm{s}}\left(1-k^{2}\right)}  \tag{7.5}\\
-\frac{k}{L\left(1-k^{2}\right)} & \frac{1}{L_{\mathrm{s}}\left(1-k^{2}\right)}
\end{array}\right)\binom{d_{\Sigma}+d_{\Delta}}{d_{\Sigma}-d_{\Delta}} .
$$

Addition of the two equations leads to the response of the combined current

$$
\begin{equation*}
\frac{d i_{\Sigma}}{d t}=v_{\text {in }}\left(2 \frac{1-k}{L_{\mathrm{s}}\left(1-k^{2}\right)}\right) d_{\Sigma} \Longrightarrow P_{\Sigma}(s)=\frac{2}{s L(1+k)} \tag{7.6}
\end{equation*}
$$

whereas subtraction of the two equations leads to the circulating current transfer function

$$
\begin{equation*}
\frac{d i_{\Delta}}{d t}=v_{\text {in }}\left(2 \frac{1+k}{L_{\mathrm{s}}\left(1-k^{2}\right)}\right) d_{\Delta} \Longrightarrow P_{\Delta}(s)=\frac{2}{s L(1-k)} \tag{7.7}
\end{equation*}
$$

### 7.3.2 Phase current controller

Beginning with the phase current controller, the goal is to shape the transfer function of the system to a $-20 \frac{\mathrm{~dB}}{\mathrm{dec}}$ slope at the desired crossover frequency $f_{i_{\Sigma}}$, and $-60 \frac{\mathrm{~dB}}{\mathrm{dec}}$ everywhere else, as depicted in Figure 7.13(a). The high initial gain created by the $-60 \frac{\mathrm{~dB}}{\mathrm{dec}}$ leads to strong error rejection. The reduction to $-20 \frac{\mathrm{~dB}}{\mathrm{dec}}$ around the crossover frequency is necessary to create sufficient phase margin. Afterwards,


Figure 7.13 (a) Open-loop transfer function of the circulating and combined current controllers. The gain for the circulating current controller is adjusted to obtain the same frequency response. (b) Closed-loop transfer function of the circulating and combined current controller.
returning to $-60 \frac{\mathrm{~dB}}{\mathrm{dec}}$ makes the closed-loop system resilient to high-frequency noise. The total system is the product of the controller transfer function $C_{i_{\Sigma}}$ and the plant model $P_{i_{\Sigma}}$. Since both inductor currents $i_{\mathrm{p}_{1}}$ and $i_{\mathrm{p}_{2}}$, as well as the capacitor voltage $v_{p}$ are measured, the plant model for the combined inductor current reduces to a single order system with

$$
\begin{equation*}
P_{i_{\Sigma}}(s)=\frac{2}{s L_{\mathrm{s}}(1+k)} . \tag{7.8}
\end{equation*}
$$

The controller is based on the following transfer function

$$
\begin{equation*}
C_{i_{\Sigma}}(s)=\underbrace{\frac{1}{s^{2}}}_{\text {Integrators }} \underbrace{\frac{\left(s+f_{i_{\Sigma}} / \alpha_{i_{\Sigma}}\right)^{2}}{\left(f_{i_{\Sigma}} / \alpha_{i_{\Sigma}}\right)^{2}}}_{\text {Zeros }} \underbrace{\frac{\left(\alpha_{i_{\Sigma}} f_{i_{\Sigma}}\right)^{2}}{\left(s+\alpha_{\Sigma_{\Sigma}} f_{i_{\Sigma}}\right)^{2}}}_{\text {Poles }} \underbrace{g_{i_{\Sigma}}}_{\text {Gain }} \tag{7.9}
\end{equation*}
$$

to achieve the desired crossover frequency and slope. The two integrators, together with the plant model create the initial $-60 \frac{\mathrm{~dB}}{\mathrm{dec}}$ slope. The two zeros, placed at a factor of $1 / \alpha_{i_{\Sigma}}$ before the crossover frequency, reduce the slope to $-20 \frac{\mathrm{~dB}}{\mathrm{dec}}$, to create sufficient phase margin at $f_{i_{\Sigma}}$. Afterwards, the two poles are place at a factor of $\alpha_{i_{\Sigma}}$ behind the crossover frequency to return to the $-60 \frac{\mathrm{~dB}}{\mathrm{dec}}$ slope. Finally, the dc gain $g_{i_{\Sigma}}$ is chosen to achieve 0 dB at the crossover frequency. The resulting closed-loop
transfer function is equal to

$$
\begin{equation*}
C L_{i_{\Sigma}}(s)=\frac{P_{i_{\Sigma}}(s) C_{i_{\Sigma}}(s)}{1+P_{i_{\Sigma}}(s) C_{i_{\Sigma}}(s)} \tag{7.10}
\end{equation*}
$$

and depicted in Figure 7.13(b). The resulting closed-loop system provides a response with good magnitude and phase response up to 50 kHz , after which the magnitude begins to drop at $-40 \frac{\mathrm{~dB}}{\mathrm{dec}}$. This roll-off is of use in the design of the subsequent voltage controller, which will request a phase current to regulate the output voltage.

The circulating current controller is designed the same way, merely with a plant model of

$$
\begin{equation*}
P_{i_{\Delta}}(s)=\frac{2}{s L_{\mathrm{s}}(1-k)}, \tag{7.11}
\end{equation*}
$$

which results in a gain of

$$
\begin{equation*}
g_{i_{\Delta}}=g_{i_{\Sigma}} \frac{1-k}{1+k} . \tag{7.12}
\end{equation*}
$$

The remaining parts of the controller stay the same, leading to the same transfer function as the combined current controller depicted in Figure 7.13.

### 7.3.3 Output voltage controller

The approach for the output voltage controller follows the same guidelines as the phase-current controller. By subtracting the actuator current from the inductor currents, the plant model simplifies to

$$
\begin{equation*}
P_{v_{\mathrm{p}}}(s)=\frac{1}{s C_{\mathrm{o}}} . \tag{7.13}
\end{equation*}
$$

By choosing a crossover frequency of $f_{v_{p}}=f_{i \Sigma} / \alpha_{v_{p}}$, the closed-loop transfer function of the current controller can be used directly to generate the high-frequency roll-off. Including the roll-off the controller transfer function simplifies to

$$
\begin{equation*}
C_{v_{\mathrm{p}}}(s)=\underbrace{\frac{1}{s^{2}}}_{\text {Integrators }} \underbrace{\frac{\left(s+f_{v_{\mathrm{p}}} / \alpha_{v_{\mathrm{p}}}\right)^{2}}{\left(f_{v_{\mathrm{p}}} / \alpha_{v_{\mathrm{p}}}\right)^{2}}}_{\text {Zeros }} \underbrace{g_{v_{\mathrm{p}}}}_{\text {Gain }} . \tag{7.14}
\end{equation*}
$$

The resulting open-loop frequency response is show in Figure 7.14.
The closed-loop response $C L_{v_{p}}(s)$ can be obtained by including the plant, controller and the closed-loop response of the phase-current controller, such that

$$
\begin{equation*}
C L_{v_{\mathrm{p}}}(s)=\frac{P_{v_{\mathrm{p}}}(s) C_{v_{\mathrm{p}}}(s) C L_{i_{\Sigma}}(s)}{1+P_{v_{\mathrm{p}}}(s) C_{v_{\mathrm{p}}}(s) C L_{i_{\Sigma}}(s)} \tag{7.15}
\end{equation*}
$$



Figure 7.14 (a) Open-loop transfer function of the output voltage controller. The high frequency roll-off is provided by the inner closed-loop current controller. (b) Closed-loop transfer function of the output voltage controller.

The resulting frequency response is depicted in Figure 7.14. The cascade of voltage and current controller shows a good magnitude and phase response up to 20 kHz , after which the roll-off in phase begins. In the same manner as the filter current rolloff was used in the tuning of the voltage-controller, the closed-loop voltage response response needs to be considered when tuning the actuator current controller.

### 7.3.4 Output current controller

With a purely resistive load, the transfer function is

$$
\begin{equation*}
P_{i_{\mathrm{act}}}(s)=\frac{1}{R_{\mathrm{act}}} \tag{7.16}
\end{equation*}
$$

Same as before, the cascaded voltage controller is used to create the high-frequency roll-off for this control loop. The crossover frequency is $f_{i_{\text {act }}}=\frac{f_{v_{\mathrm{p}}}}{\alpha_{i_{\text {act }}}}$. The resulting desired transfer function is

$$
\begin{equation*}
C_{i_{\text {act }}}(s)=\underbrace{\frac{1}{s^{3}}}_{\text {Integrators }} \underbrace{\frac{\left(s+f_{i_{\text {act }}} / \alpha_{i_{\text {act }}}\right)^{2}}{\left(f_{i_{\text {act }}} / \alpha_{i_{\text {act }}}\right)^{2}}}_{\text {Zeros }} \underbrace{R_{\text {act }}}_{\text {Gain Compensation }} \underbrace{g_{i_{\text {act }}}}_{\text {Gain }} . \tag{7.17}
\end{equation*}
$$



Figure 7.15 (a) Open-loop transfer function of the output current controller. (b) Closed-loop transfer function of the output current controller. The high-frequency roll-off is provided by the closed-loop response of the output voltage controller.

The open-loop transfer of the whole system is depicted in Figure 7.15. As with the voltage controller, the closed-loop response $C L_{i_{\text {act }}}(s)$ now considers the cascaded controller and it's closed loop transfer function $C L_{v_{p}}(s)$, such that

$$
\begin{equation*}
C L_{i_{\mathrm{act}}}(s)=\frac{P_{i_{\mathrm{act}}}(s) C_{i_{\mathrm{act}}}(s) C L_{v_{\mathrm{p}}}(s)}{1+P_{i_{\mathrm{act}}}(s) C_{i_{\mathrm{act}}}(s) C L_{v_{\mathrm{p}}}(s)} \tag{7.18}
\end{equation*}
$$

### 7.4 Experimental verification

The amplifier is controlled with the Micro Lab Box from dSpace, which consists of a 2 GHz dual-core processor and a Kintex-7 FPGA from Xilinx, operating at 100 MHz clock frequency. The digital IO is used to control the half-bridges and read out the cycle average phase current measurements. Internal ADCs are used to sample the input and output voltages and output current at 16 -bit at a rate of 800 kSPS , synchronous to the PWM carrier. The phase voltages and currents are additionally measured on a Tektronix MSO64 using Hioki 3273-50 current probes for acquisition of the current ripple. Due to limitations in the control system, the voltage controller was implemented at a maximum discrete sample rate of 40 kSPS . Subsequently the control bandwidth had to be scaled down to 5 kHz for the voltage controller and


Figure 7.16 Step response of the combined current controller for a step of -1 A . Each phase current settles to -500 mA within $20 \mu \mathrm{~s}$.

1 kHz for the output current controller. The phase current controller remains at its intended bandwidth.

The control of the coupled inductor is verified through measurements of the step response of the combined and circulating current controllers. Figure 7.16 depicts the response of a -1 A step in the output current, which leads to each of the phase currents settling to -500 mA within $20 \mu \mathrm{~s}$. The step response of the circulating controller is shown in Figure 7.17 for a step of -500 mA . The currents settle to $\pm 250 \mathrm{~mA}$ within $30 \mu \mathrm{~s}$.

The ripple cancellation of the coupled inductor is verified by raising the common mode voltage from $12.5 \%$ to $87.5 \%$ of the supply voltage. Due to a common mode limitation the test is carried out at a supply voltage of 200 V . The resulting amplitude of the current ripple for one phase (red) as well as the summed current ripple of both phases (blue) is depicted in Figure 7.18. The values for the current ripple are obtained through the average of ten consecutive switching periods. The shapes follow the expected curves (dashed lines) for output and phase current ripple cancellation detailed in chapter 4 . At a dutycycle of 0.5 , the measurement of the phase current ripple of 263 mA is close the expected value of 301 mA . At dutycycles of 0.25 or 0.75 the current ripple is $50 \%$ above the expected value. However, the function to calculate current ripple cancellation is highly sensitive to the coupling coefficicent. The lower current ripple at a dutycycle of 0.5 and a higher current ripple elsewhere indicates a slightly stronger coupling coefficient than the measured value of -0.82 . The summed current ripple of both phases matches the expected


Figure 7.17 Step response of the circulating current controller for a step of 500 mA . The phase currents settle to $\pm 250 \mathrm{~mA}$ within $30 \mu \mathrm{~s}$.
value at all operating points.
The distortion of the amplifier is evaluated by supplying a sinusoidal current with an amplitude of 20 A at a frequency of 40 Hz . The resulting output spectrum, obtained from the load current measurement, is depicted in Figure 7.19. A moving average filter with a width of 16 samples is applied to the 800 kSPS measurement to decrease the noise level at low frequencies. The second harmonic is at a level of -91 dB and the third harmonic is near -100 dB .

The output current is set to follow a reference $i_{\text {ref }}$ provided by a typical positioning loop [21], proportional to the acceleration depicted in Figure 7.1. The circulating current reference is set to zero. The tracking error is depicted in Figure 7.20. The measured phase currents, output voltages and load current are shown in Figure 7.21. As evident, the slow output current control leads to significant lag behind the reference, with errors of up to 600 mA . Faster control is necessary to reduce this error and provide better tracking. Furthermore, feed-forward can be added to provide better transient performance.

### 7.4.1 Discussion

Implementation of the voltage controller within the FPGA of the control system would allow to discretize the voltage controller at the sample rate of 800 kHz and set control bandwidth to the desired value. As it is, the amplifier provides very dynamic filter current regulation, whose potential remains partly unused. However,


Figure 7.18 Phase and summed inductor current ripple over varying dutycycle, measured at $v_{\text {in }}=200 \mathrm{~V}$. Measurement (marks) and expected value from calculation (dashed lines).


Figure 7.19 Spectrum for a regulated sinusoidal load current of 20 A peak at 40 Hz . The spectrum is obtained through the low-pass filtered current measurement and serves as an indication of the amplifiers attainable output distortion.


Figure 7.20 Tracking error of the amplifier.


Figure 7.21 Measurement of the amplifiers phase currents, output voltage and load current. The grey area indicates the current ripple per phase.
control of circulating and combined filter current has been demonstrated successfully, with fast settling times of tens of microseconds. The amplifier is able to produce a sinusoidal current with a spurious free range of 91 dB . Given the trapezoidal application profile for semiconductor lithography machines, the amplifier can follow the reference current, but lags behind by up to 500 mA whenever the slope of the reference changes. During the scanning phase, regulation to zero current is well maintained, at very low phase current ripple. Interleaving of an even number of phases leads to a output current ripple of less than 200 mA during the scanning phase, where the dutycycle is close to 0.5 . Furthermore, use of the coupled inductor leads to a reduction of the peak-to-peak phase current ripple down to 500 mA . As demonstrated, the amplifier has high-bandwidth and can provide precise currents. To achieve both simultaneously, the control system needs to be revised.

## 8 <br> Conclusion and recommendations

"Don't want to think about it ~
'Cause that was yesterday ~
Tomorrow brings more opportunity."
Striker

AMPLIFIERS for semiconductor lithography or other high-precision applications need to be powerful, efficient, fast and precise. The combination of all these factors requires the use of emerging technologies in power electronics to facilitate the ever increasing miniaturization of semiconductors and increasing production speed. The methods introduced in this work will not only help to develop the next generation of high-precision amplifiers, but also the generations after. This chapter summarizes the main conclusions and contributions of this work, and provides recommendations for future work.

### 8.1 Conclusions

The harmonic balance method for calculating the temperature of power semiconductors has been introduced, which significantly speeds component selection and inverter design. At its current single-threaded implementation, the computation speed is already one hundred times faster than conventional simulation software, while maintaining high accuracy in its results. Using widely available loss models for transistors, the steady-state junction temperature is obtained for arbitrary modulation and output waveform. Throughout the thesis, the harmonic balance method has been used to evaluate thermal designs for a given inverter or to determine the required topology for a set of parameters. What would have taken hours by standard simulation tools has been carried out in a matter of minutes.

Wide-bandgap devices push the boundaries of efficiency, as they offer increased switching speed over standard silicon devices. However, this increase in switching speed has a detrimental impact on thermal design. As the cooling surface of a semiconductor is internally connected to either drain or source, one thermal interface in a half-bridge is subjected to high-voltage slopes. Subsequently, any parasitic capacitance across the insulation will induce unwanted currents into the system, proportional to its size. A performance coefficient for insulation materials has been introduced, which allows to weigh the cooling performance of a material against the added parasitic capacitance. Specifically for GaN devices, proper insulation is critical, as careless design can result in parasitics equivalent to the device capacitance and a significant increase in switching losses, next to highly likely electromagnetic interference issues. An analytic method for heat-spreading has been adopted specifically to insulated metal substrates, an increasingly popular solution for cooling GaN devices. Together with the harmonic balance method, fully analytic thermal design and optimization for inverters becomes possible. It was shown that specific design requirements for power, switching frequency, temperature and efficiency, can be impossible to realize with a single half-bridge.

The interleaved inverter is a well known topology for proving high-output current and increased control bandwidth compared to a single half-bridge. Choosing the number of interleaved legs is always a trade-off between performance gain and cost. The general rule is that an odd number of phases provide a significant control bandwidth increase when using digital control. As the sample points do not overlap, the output current can be altered at twice the rate compared to an even number of carriers. However, when considering a normalized device area, it was shown that this rule only begins to take effect for a larger number of interleaved legs. As the output current gets divided by the number of legs, the conduction losses per device decrease asymptotically. Subsequently, at a low number of phases, adding one more phase allows for a significant increase in switching frequency. The gain in switching
frequency can offset the reduction in update rate when moving from odd to even number of legs. Taking other operating point dependent benefits into consideration, choosing the number of legs is highly application specific.

When designing high-bandwidth inverters with low filter inductances, the effect of propagation delay and jitter needs to be considered. Due to the output voltage dependent current slope, they add distortion and noise to the current measurement. The propagation delay related error can be cancelled with a proposed filter, at the cost of slightly reduced dynamic performance. The same filter also reduces the jitter related noise, and even improves the SNR for large modulation depths. The distortion due to thermal expansion of the shunt resistor can be calculated effectively with the proposed spectral computation method, which allows to select components with sufficiently low temperature dependence.

Using the established methods, a prototype amplifier has been designed and implemented. It was shown that using an even number of phases, together with coupled inductors, leads to significant current ripple reduction, particularly during the exposure phase of a semiconductor lithography machine. Full dynamic current control over coupled filter inductors has been verified.

### 8.2 Thesis contributions

- Harmonic balance method for junction temperature calculation including temperature-dependent losses.
The calculation of device temperature using harmonic balance offers a fast, precise alternative to iterative steady-state solvers, which includes temperature dependence and saturation effects. The results match simulations obtained with commercial state-of-the-art steady-state solvers, at one hundred times faster computation speed.
- Figure of merit for evaluation of insulation materials.

For a given insulation material, lower thermal resistance always comes at the cost of larger parasitic capacitance. The introduced FOM provides a geometry independent value, with which a thermal resistance can be equated to a guaranteed parasitic capacitance, or vice versa. Given restrictions for both values, only materials with a FOM below the desired value need to be considered.

- Analytic optimization of heat-spreader design for arbitrary topologies.

The introduced harmonic balance has been combined with existing analytic models for heat transfer. This allows to evaluate hundreds of devices and heatspreaders for a desired inverter operating efficiency or junction temperature in a matter of seconds.

- Distortion mitigation and noise reduction through dynamic filtering.

When measuring currents, the propagation delay of the trigger signal causes an error to occur on the measurement, proportional the current slope and delay. The introduced dynamic filter cancels the distortion by weighing two consecutive samples, such that the summed error reduces to zero. In addition, the filter also reduces the noise on the acquired current signal, as measurements taken during lower slopes are weighted higher. For high modulation depths, a gain of 6.02 dB in SNR can be achieved.

- Closed-form computation of temperature-swing induced distortion in resistive current measurements.
The dominant harmonics caused by self-heating in resistive elements are calculated in the frequency domain. The introduced method skips the need for transformation algorithms, while proving the same accuracy as computationally intensive time-based simulations.
- Amplifier design and evaluation targeted towards position accuracy in semiconductor lithography.
A high-precision amplifier is designed, implemented and experimentally verified. Full control over the circulating and combined output current of a coupled inductor is demonstrated. The amplifier is shown to have a spurious free range of 91 dB . The resulting minimal current ripple during the exposure phase of a semiconductor lithography machine leads to several benefits regarding noise and subsequently position accuracy.


### 8.2.1 Conference publications

- Weiler, P., Bokmans, B., Lemmen, E., Vermulst, B., Wijnands, K., "Parasitic Effects from Cooling of GaN Power Transistors: Impact on Switching Losses and Common-Mode Currents", IPEC-Himeji 2022 - ECCE Asia, 2022
- Weiler, P., Vermulst, B., Lemmen, E., Wijnands, K., "High Power GaN Module Using 3D-Printed Liquid Coolers for Hard-Switching at Megahertz", PCIM Europe 2021, 2021
- Weiler, P., Vermulst, B., Roes, M., Wijnands, K., "Design Limitations of Heat Spreaders for Gallium Nitride Power Modules", PCIM Europe 2020, 2020
- Weiler, P., Vermulst, B., "Gate Driver with Short Inherent Dead-Time for WideBandgap High-Precision Inverters", APEC 2020, 2020


### 8.2.2 Journal publications

- Weiler, P., Vermulst, B., Lemmen, E., Wijnands, K., "Spectral Steady-State Analysis of Inverters with Temperature-Dependent Losses using Harmonic Balance", IEEE Open Journal of Power Electronics, 2020
- Weiler, P., Vermulst, B., Lemmen, E., Wijnands, K., "Closed-Form Spectral Computation of Intermodulation Distortion for Shunt-Based Current Measurements", IEEE Open Journal of Instrumentation and Measurement, 2022


### 8.3 Recommendations

The harmonic balance based temperature calculation is still in its infancy. Additional effects such as dead-time or magnetic coupling between phase legs need to be included for a complete loss calculation. However, together with magnetic field solvers there is an enormous potential for extremely fast, complete topology evaluation and design. The current single-threaded CPU implementation already outperforms optimized simulation tools by a factor of one hundred. As the method only requires solving of linear systems, a potential parallel implementation on a GPU would likely increase this to a factor of ten thousand [3]. Thus, virtually any combination of device, cooling solution and magnetic component could be evaluated for different input parameters in the time it takes to drink a coffee.

For cooling of GaN devices, the introduced material coefficient shows that aluminiumnitride is one of the best available insulation materials. During the writing of this thesis, one company has already adopted a thin ceramic insulation layer in their package, completely removing the task of designing a suitable solution. Other major advancements have been made regarding integration of circuitry into GaN devices. Fully integrated 650 V half-bridge ICs have become available, with integrated drivers, over temperature protection and current sensing, in a $6 \mathrm{~mm} \times 8 \mathrm{~mm}$ package. As the integrated sensing uses the internal drain-source resistance, the provided output signal comes at no cost of additional conduction losses [44].

Sensing per transistor would also eliminate the delay related distortion, as ADC and gate driver could use the same digital isolator, with well matched channel-to-channel delays. Using insulated metal substrates, together with integrated acquisition solutions, implementing analog fronted, ADC and reference in a single BGA package, a fully isolated, sensed and cooled 400 V half-bridge could be implemented in a footprint of less than $6 \mathrm{~cm}^{2}$.

## 宏 <br> Symbols and notation

## A. 1 Symbols

| Symbol | Quantity | Unit |
| :---: | :--- | :--- |
| $a$ | Normalized heat source radius | m |
| $A$ | Area | $\mathrm{m}^{2}$ |
| $b$ | Normalized heat-spreader radius | m |
| $B_{\mathrm{i}}$ | Biot number | - |
| $B_{\text {on }}$ | Turn-on blanking | - |
| $B_{\text {off }}$ | Turn-off blanking | - |
| $C_{\text {par }}$ | Parasitic capacitance to heatsink | F |
| $C_{\text {th }}$ | Thermal capacitance | $\frac{\mathrm{J}}{\mathrm{Kkg}}$ |
| $d$ | duty cycle | - |
| $e_{\mathrm{b}}$ | Sample error at bottom of carrier | - |
| $E_{\text {on }}$ | Turn-on energy | J |
| $E_{\text {off }}$ | Turn-off energy | J |
| $\epsilon$ | Heat source-spreader ratio | - |
| $\varepsilon_{\mathrm{r}}$ | Relative dieletric constant | - |
| $e_{\mathrm{t}}$ | Sample error at top of carrier | - |
| $\eta$ | Operating efficiency | - |
| $f_{\mathrm{E}}$ | Numeric energy fit | $\frac{\mathrm{J}}{{ }^{\mathrm{C}}}$ |
| $f_{\mathrm{sw}}$ | Switching frequency | Hz |
| $f_{v}$ | Numeric voltage fit | $\frac{\mathrm{V}}{{ }^{\circ} \mathrm{C}}$ |


| Symbol | Quantity | Unit |
| :---: | :---: | :---: |
| $i_{\mathrm{b}}$ | Sample at bottom of carrier | A |
| $i_{\text {ds }}$ | Drain-source current | A |
| $i_{\text {L }}$ | Inductor current | A |
| $i_{v}$ | Sawtooth input current | A |
| $i_{\text {off }}$ | Turn-off current | A |
| $i_{\text {on }}$ | Turn-on current | A |
| $i_{\text {out }}$ | Output current | A |
| $i_{\text {par }}$ | Parasitic current through heatsink | A |
| $i_{\rho}$ | Rectangular input current | A |
| $i_{\text {t }}$ | Sample at top of carrier | A |
| $k$ | Coupling coefficient | - |
| $\lambda$ | Thermal conductivity | $\frac{\mathrm{W}}{\mathrm{mK}}$ |
| $\lambda_{\text {c }}$ | Empirical heatspreading parameter | - |
| $L_{\text {loop }}$ | Power loop inductance | H |
| $L_{\mathrm{m}}$ | Mutual inductance | H |
| $L_{\text {s }}$ | Self inductance | H |
| $\hat{m}$ | Modulation depth | - |
| $N$ | Number of interleaved phases | - |
| $\omega$ | Angular frequency | $\frac{\mathrm{rad}}{\mathrm{s}}$ |
| $P_{\text {c }}$ | Conduction losses | W |
| $P_{\text {ds }}$ | Drain-source losses | W |
| $\Phi_{\text {c }}$ | Heatspreading parameter | - |
| $p_{\kappa \varepsilon}$ | Performance coefficient for insulation material | $\frac{\mathrm{pFK}}{\mathrm{W}}$ |
| $\Psi_{\text {max }}$ | Dimensionless constriction resistance | - |
| $P_{\text {sw }}$ | Switching losses | W |
| $R_{\text {th }}$ | Thermal resistance | ${ }_{\text {K }}{ }^{\text {W }}$ |
| $T_{\text {amb }}$ | Ambient temperature | ${ }^{\circ} \mathrm{C}$ |
| $\tau$ | Normalized heatspreader thickness | - |
| $t_{\text {ins }}$ | Insulation layer thickness | m |
| $T_{\mathrm{j}}$ | Junction temperature | ${ }^{\circ} \mathrm{C}$ |
| $T_{\text {jit,rms }}$ | Timing jitter | S |
| $T_{\mathrm{p}}$ | Propagation delay | S |
| $T_{\text {s }}$ | Sampling period | S |
| $T_{\text {sw }}$ | Switching period | s |
| $V_{\text {ds }}$ | Drain-source voltage | V |
| $v_{\text {in }}$ | Supply voltage | V |
| $v_{n}$ | Amplifier input noise density | $\mathrm{V} / \sqrt{\mathrm{Hz}}$ |
| $v_{\text {out }}$ | Output voltage | V |
| $x_{\text {b }}$ | Bottom sample coefficient | - |
| $x_{\text {t }}$ | Top sample coefficient | - |
| $\mathrm{Z}_{\text {th }}$ | Thermal impedance | $\underset{W}{\text { K }}$ |


| Symbol | Quantity | Unit |
| :---: | :--- | :---: |
| $z_{\text {th }}$ | Thermal impulse response | $\frac{\mathrm{K}}{\mathrm{W}}$ |

## A. 2 Acronyms

| Acronym | Meaning |
| :---: | :--- |
| ADC | Analog-to-digital conversion |
| AlN | Aluminium-nitride |
| BeO | Beryllium-oxide |
| CMTI | Common-mode transient immunity |
| DAC | Digital-to-analog conversion |
| DSP | Digital signal processor |
| EUV | Extreme ultraviolet |
| FET | Field effect transistor |
| FOM | Figure of merit |
| FPGA | Field-programmable gate array |
| HEMT | High electron-mobility transistor |
| IGBT | Insulated-gate bipolar transistor |
| IMS | Insulated metal substrate |
| GaN | Gallium-nitride |
| GPU | Graphics processing unit |
| LUT | Look-up table |
| LVDS | Low-voltage differential signaling |
| PCB | Printed circuit board |
| PLECS | Piecewise linear electrical circuit simulation |
| PWM | Pulse-width modulation |
| RF | Radio frequency |
| Si | Silicon |
| SiC | Silicon-carbide |
| SMB | Sub-miniature version B |
| SNR | Signal-to-noise ratio |
| TCR | Temperature coefficicent of resistance |
| THD | Total harmonic distortion |
| VRM | Voltage regulator model |

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[^0]:    1"Die Buchdruckerei" by Daniel Chodowiecki, ca. 1770.

[^1]:    This chapter is based on [73].

[^2]:    ${ }^{1}$ A Toeplitz matrix $\boldsymbol{A}$ is constructed from a vector $\vec{a}$ by $\boldsymbol{A}_{i, j}=a_{i-j}$.

[^3]:    ${ }^{1}$ There's no need for a $0.1 \mathrm{~K} / \mathrm{W}$ insulation resistance, when the device and heatsink each add $1 \mathrm{~K} / \mathrm{W}$.

[^4]:    ${ }^{1}$ In [40] $\hat{m}$ ranges from 0 to 0.5 . In this work, $\hat{m}$ ranges from 0 to 1 , to have 1 indicate full depth of modulation. Hence the equations between works will differ by factors of 2 or 4 due to squaring of $\hat{m}$.

[^5]:    ${ }^{1}$ Similarly, a speaker also experiences distortion due to resistive losses in its voice coil, a term coined as power compression. With temperature the resistance increases, leading to a decrease in current and output amplitude. However, in this case the resistive load is voltage driven, causing a decrease in current and thus audible compression.

[^6]:    ${ }^{2}$ Pursuit of this problem led to the more evolved method presented earlier in chapter 2.

[^7]:    ${ }^{3}$ The temperature drift was initially measured through the SMB connectors on the board and the observed TCR was far greater than the datasheet specification. The drift in voltage seems to have been caused by an asymmetric material transition in the coaxial connector. Using a twisted pair without the SMB connector resolved this issue.

[^8]:    ${ }^{4}$ As an alternative, the thermal step response can be observed by applying a pulsed current. However, the cables to the shunt resistor will respond to the pulse as well, creating an oscillation in the shunt voltage which can mask the voltage change due to temperature.

