Noise-Shaping SAR ADCs: From Discrete Time to Continuous Time

NOISE-SHAPING SAR ADCS: FROM DISCRETE TIME TO CONTINUOUS TIME

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Abstract

Noise-Shaping (NS) SAR ADCs become popular recently thanks to their low-power and high-resolution features. This article first summarizes and benchmarks different discrete-time (DT) NS-SAR implementations in literature. An open-loop duty-cycled residue amplifier is selected as a power-efficient solution to realize high residue gain. Then, a digital-predicted mismatch error shaping technique is introduced to improve the DAC linearity. The proposed DT NS-SAR ADC achieves 80 dB SNDR and 98 dB SFDR in a 31.25 kHz bandwidth while consuming 7.3 μW. Next, the NS-SAR architecture is extended from DT operation to continuous-time (CT) operation. The ADC sampling switch is removed and the loop filter is duty cycled to realize the CT NS-SAR operation. Compared to DT designs, the CT NS-SAR ADC is easy to drive and has an inherent anti-aliasing function. As a proof of concept, the proposed CT NS-SAR ADC achieves 77 dB SNDR and 86 dB SFDR in a 62.5 kHz bandwidth with a power consumption of 13.5 μW.

1. Introduction

Noise-shaping successive-approximation-register (NS-SAR) analog-to-digital converters (ADCs) have emerged in recent years as a promising architecture to realize high-resolution and low-power data converters [1]. It combines the merits from a SAR ADC and a $\Delta\Sigma$ ADC, and thus reaches an optimization between resolution and power consumption. Its application ranges from sensor readout [2] to wireless communication [3], and its research remains active in both academia and industry.

This article focuses on two types of NS-SAR ADCs: discrete-time (DT) NS-SAR ADCs and continuous-time (CT) NS-SAR ADCs. For DT NS-SAR ADCs, different loop filter design choices will be benchmarked in terms of their power

efficiency. The mismatch error shaping (MES) technique will be discussed as an effective solution to enhance the linearity. For CT NS-SAR ADCs, its architecture will be explained in detail, and its design considerations will be elaborated. Design examples will be presented for each type of ADC, and conclusions will be drawn at last.

2. Discrete-Time Noise-Shaping SAR ADC

The diagram of a DT NS-SAR ADC [4] is shown in Fig. 1. Its basic principle is as follows. After the normal SAR conversion is finished, the residue voltage V_{RES} is directly obtained at the output of its digital-to-analog converter (DAC). This residue voltage is then integrated by the loop filter $L(z)$ and added to the next input signal. In this way, the quantization noise and comparator noise can be high-pass shaped by using a low-pass $L(z)$ function.

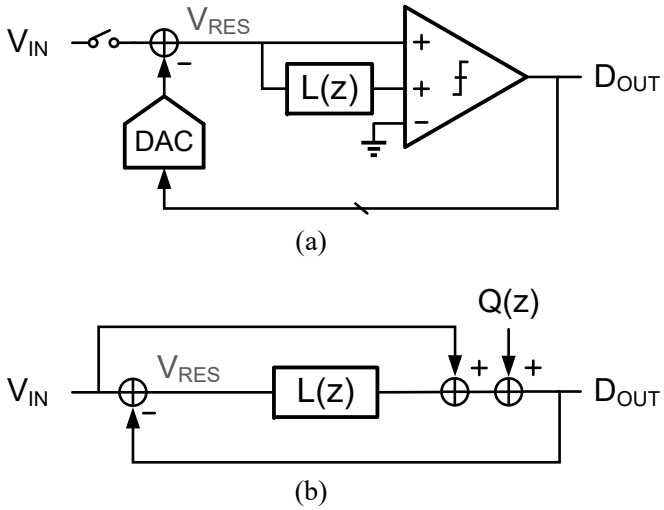


Fig. 1. (a) Block diagram and (b) signal diagram of a DT NS-SAR ADC.

The NS-SAR ADC has the same noise-shaping principle as the $\Delta\Sigma$ ADC, but the hardware implementation is different. First, the NS-SAR ADC contains only one DAC in the system, unlike a SAR-assisted $\Delta\Sigma$ ADC [5] where one DAC is needed in the SAR quantizer and another DAC is needed in the noise-shaping feedback loop. Second, there exists one feedforward path from the ADC input to the comparator input in the signal diagram. This feedforward path does not alter the noise transfer function (NTF), but makes sure that the integrator only sees the noise signal, and its output swing and linearity requirements are relaxed. These two features provide more possibilities in the loop filter choice, as will be discussed later.

This section is based on [6], and it will discuss the following topics in the DT NS-SAR ADC: choice of loop filter structure and circuit topology, and mitigation of the DAC mismatch error.

2.1. Loop filter

Because the residue information is directly available on the DAC output after the SAR conversion, an NS-SAR ADC does not require an additional feedback DAC to subtract the ADC output from the input. Therefore, the loop filter does not necessarily have to be a switched-capacitor integrator as in a conventional DT $\Sigma\Delta$ ADC. Fig. 2 shows the three commonly used loop filter structures:

1. A passive integrator followed by a gain stage [7], referred as 'passive loop filter (PLF)'.
2. An active open-loop amplifier followed by a passive integrator [8], referred as 'open-loop amplifier (OLA)'.
3. A closed-loop switched-capacitor integrator [9], referred as 'closed-loop integrator (CLI)'.

Because the majority of the noise in a NS-SAR ADC comes from the sampling kT/C noise and the loop filter noise, the power efficiency of the DAC and loop filter can be used as an indicator to reflect the power efficiency of the whole converter. We can use the figure-of-merit (FoM) definition from [10] to benchmark the power efficiency of different loop filter structures. This FoM is defined as:

$$\text{FoM} = (\text{Energy consumption}) \cdot (\text{Noise power}) \tag{1}$$

where 'Energy consumption' means the total energy consumed by the DAC (E_{DAC}) and the loop filter (E_{LF}), and 'Noise power' includes the noise from DAC sampling ($\overline{V_{n,\text{DAC}}^2}$) and loop filter ($\overline{V_{n,\text{LF}}^2}$) as well. A smaller FoM value indicates that lower energy is needed for the same noise target. The FoM expressions for the three loop filters can be found in [6]. Fig. 3 shows the theoretical FoM range for each loop filter structure when different DAC switching schemes and circuit topologies are considered. For the CLI-based loop filter, both floating inverter amplifier (FIA) [11] and conventional amplifiers are included. The FoM value for closed-loop FIA is obtained from [12] following the same definition as in (1). Fig. 4 summarizes the performance of the prior NS-SAR ADC designs categorized by their loop filter structures from [1] and three recent works [13], [14], [15]. Note that in Fig. 3, a lower FoM means a higher power efficiency, while in Fig. 4, a

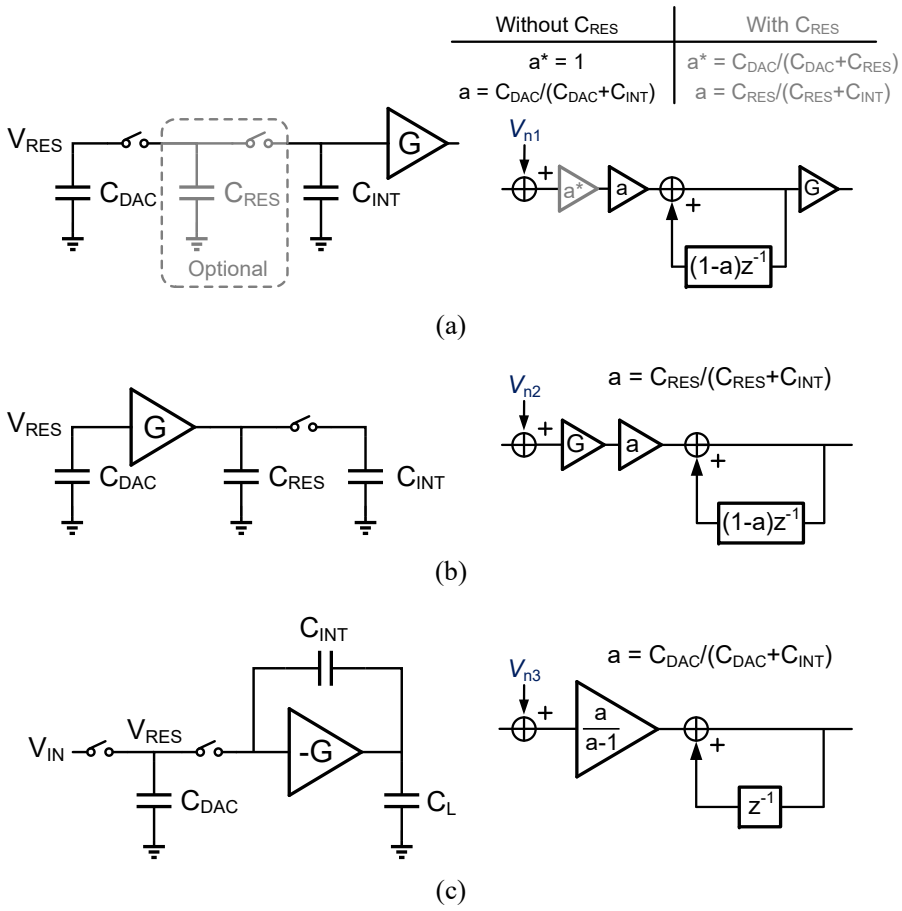


Fig. 2: Different loop filter structures in NS-SAR ADCs: (a) PLF, (b) OLA and (c) CLI.

higher Schreier FoM (FoM_S) is better. By comparing Fig. 3 and Fig. 4, we can have the following observations:

1. The PLF has the best theoretical FoM defined in (1). The FoM improvement in PLF mainly comes from smart charge sharing schemes among capacitors to reduce the additional sampling noise [16]. However, this power-efficient PLF in [16] has only been demonstrated in a first-order NS-SAR ADC and may not be easy to extend to higher order. Therefore, its noise-shaping ability can be limited when compared to OLA- and CLI-based designs.
2. The OLA-based designs show excellent power efficiency, because the noise from the passive integrator is attenuated by the amplifier gain and the amplifier usually consumes only dynamic power. The key to achieve a better FoM is to use a low-power amplifier topology. Inverter-based amplifiers [6], [10] and multi-phase settling technique [17] can be considered for the purpose of saving power. The cascade of passive integrators [6] or active stages [17] can be used to realize high-order noise-shaping with minimal hardware overhead.

3. The CLI-based designs exhibit a wide range of FoM values, which is caused by the different choices on the amplifier topology. A conventional amplifier with a static bias current could be power hungry, while the emerging FIA-based closed-loop integrator [11] has demonstrated a significant power reduction benefit.

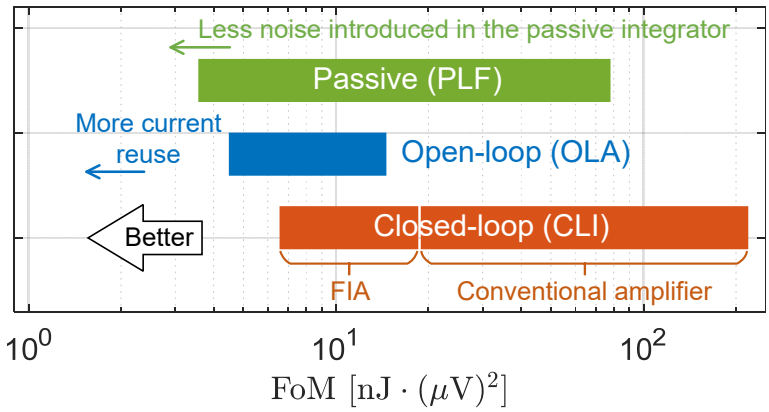


Fig. 3. Theoretical FoM of different loop filters.

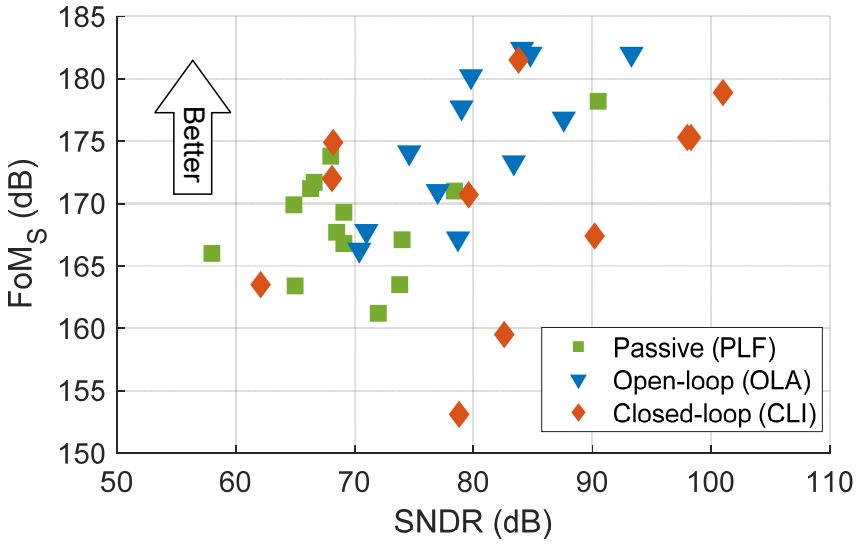


Fig. 4. NS-SAR ADC survey.

Overall, the calculated FoM from Fig. 3 matches well with the performance of actual designs listed in Fig. 4. Based on the above benchmark results, this work chooses the OLA-based loop filter for its high power efficiency and its ability to achieve higher-order noise-shaping.

Fig. 5 shows the proposed DT NS-SAR ADC. Its loop filter consists of one active amplifier and two cascaded passive integrators. The whole converter operates as follows: After the SAR quantization, the residue voltage V_{RES} is amplified during Φ_{AMP}, and the result is stored on the amplifier load capacitors C_{RES}. Then,

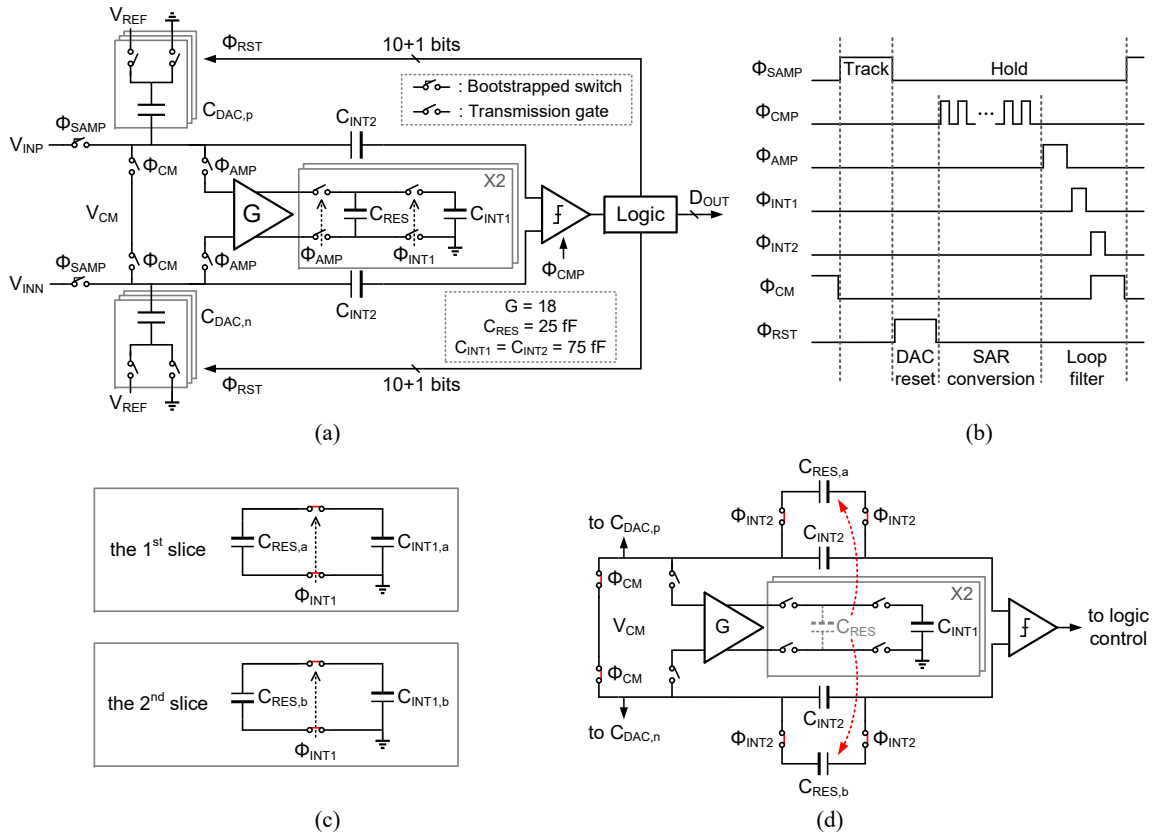


Fig. 5: (a) Proposed DT NS-SAR ADC. (b) Timing diagram. (c) The first integration phase. (d) The second integration phase.

the first integration takes place between the two sets of C_{RES} and C_{INT1} [see Fig. 5(c)]. After that, the second integration continues between C_{RES} and C_{INT2} [see Fig. 5(d)]. Therefore, a second-order noise-shaping is achieved. With an amplifier gain of 18×, and a capacitor ratio of 3 ($C_{\mathrm{INT1}}/C_{\mathrm{RES}} = C_{\mathrm{INT2}}/C_{\mathrm{RES}} = 3$), the in-band noise suppression reaches 30 dB at an oversampling ratio (OSR) of 16.

To achieve the required 18× gain, a duty-cycled amplifier is used in this design, as shown in Fig. 6. This amplifier is enabled by the control clock Φ_{AMP}. By designing the power-on time shorter than the amplifier's time constant, the power efficiency of this amplifier is comparable to an FIA [6]. In this work, the dc gain of the amplifier is 40×, and the active time is designed as 0.58× of the amplifier's time constant to achieve the desired 18× gain. The bias current generation circuit is also duty cycled. The bias voltage V_{B} is stored on a large capacitor C_{B} (2 pF). The voltage V_{B} is refreshed in every 16 sampling clock cycles to avoid leakage drift. Even though a lower current in the bias circuit can be used together with a high-ratio current mirror to provide the same current for the main amplifier, this duty-cycled operation ensures that the amplifier and its bias generation circuit

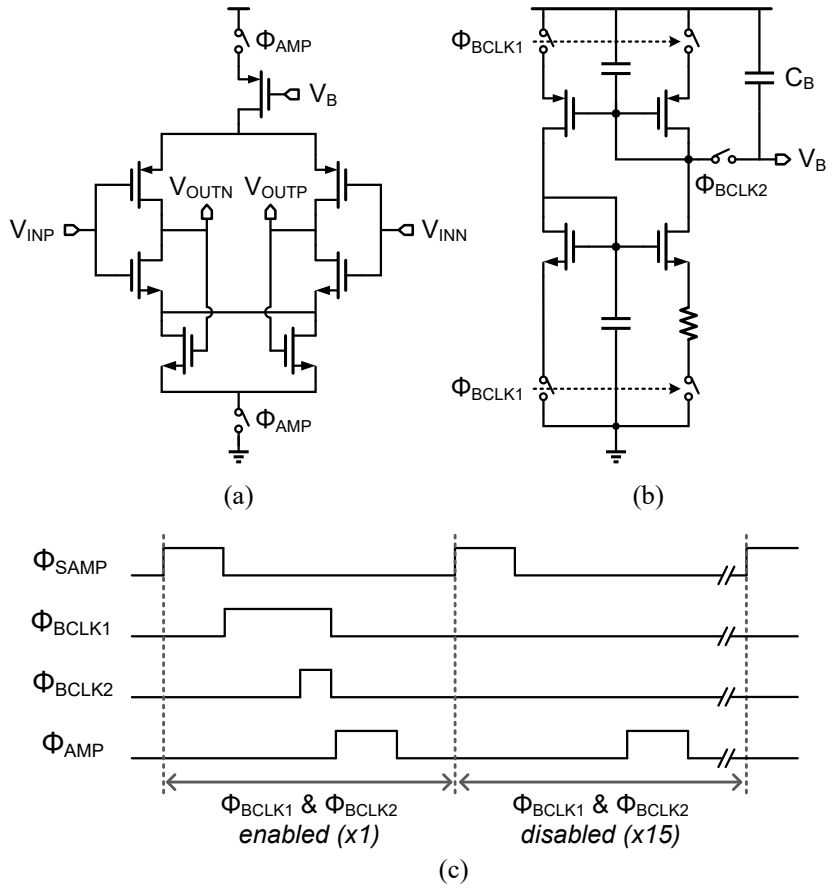


Fig. 6: (a) Duty-cycled amplifier. (b) Duty-cycled bias circuit. (c) Timing diagram for the amplifier and bias circuit.

both consume only dynamic power, and the power consumption of the whole converter can thus scale with its sampling frequency.

2.2. Mismatch error shaping

The mismatch errors in the DAC array can limit the linearity of the NS-SAR ADC. Mismatch error shaping (MES) has been proposed in [2] to shape the DAC mismatch errors out of band. Its principle is illustrated in Fig. 7. After the SAR conversion of the previous input signal is done, only the most significant bit (MSB) capacitor is reset, while the control signals for the other bits are held. Before the SAR conversion for the current input starts, all the least significant bits (LSB) are reset [Φ_{RST} in Fig. 5(b)], which adds the mismatch error E(n-1) contained in the previous LSB voltage ($z^{-1}V_{\mathrm{LSBs}}$) to the current input. This additional LSB signal is then subtracted in the digital domain, and a first-order mismatch error shaping can be realized. However, the extra LSB voltage added at the input may cause the ADC to saturate. To avoid this problem, a digital

prediction scheme has been proposed in [18]. By using the current ADC output to predict the next sample, we can know if over range will occur and then toggle the MSB capacitor accordingly to prevent over range. In this way, the ADC full input range can be kept.

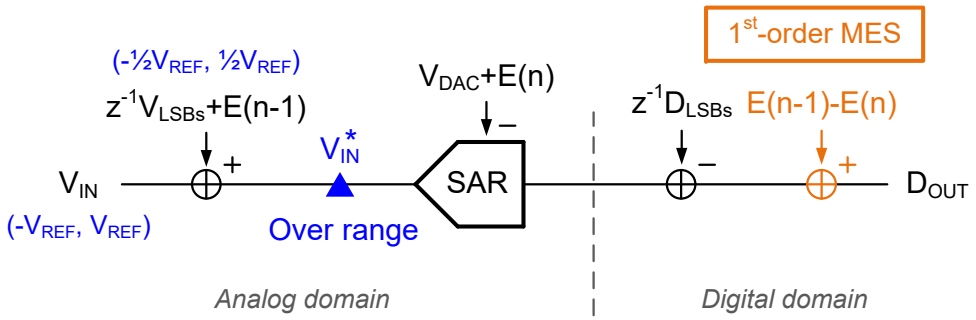


Fig. 7. Principle of MES.

The digital prediction scheme in [18] uses a tri-level decision criterion, which corresponds for compensating positively, compensating negatively or no compensation, dependent on the predicted signal level. However, this tri-level prediction cannot deal with the mismatch between the two MSB capacitors (C_{L} and C_{R} in Fig. 8) when a split switching scheme is used. Therefore, in this work we adopt a two-level prediction scheme where the compensation is done based on the polarity of the prediction result, as shown in Fig. 9. Since a two-level switching ensures an inherently linear two-point compensation voltage (V_{COMP}), the mismatch between C_{L} and C_{R} will not cause distortion in the spectrum.

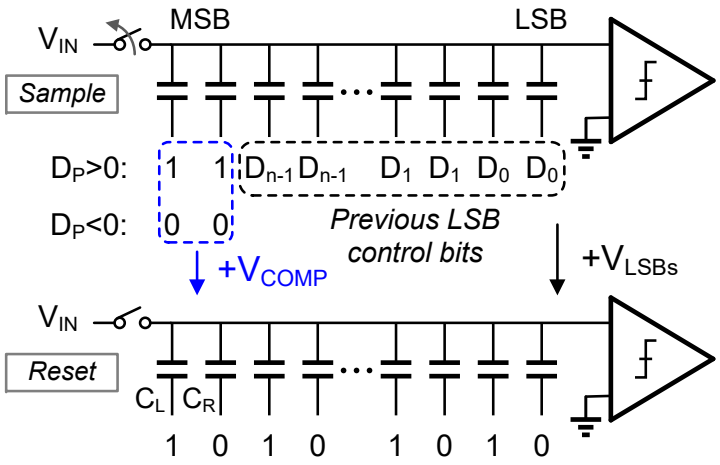


Fig. 8: DAC switching sequence in the proposed MES with two-level digital prediction.

The simplification from the tri-level prediction to the two-level prediction leads to a reduction in the maximum tolerable prediction error. Fig. 10 illustrates the

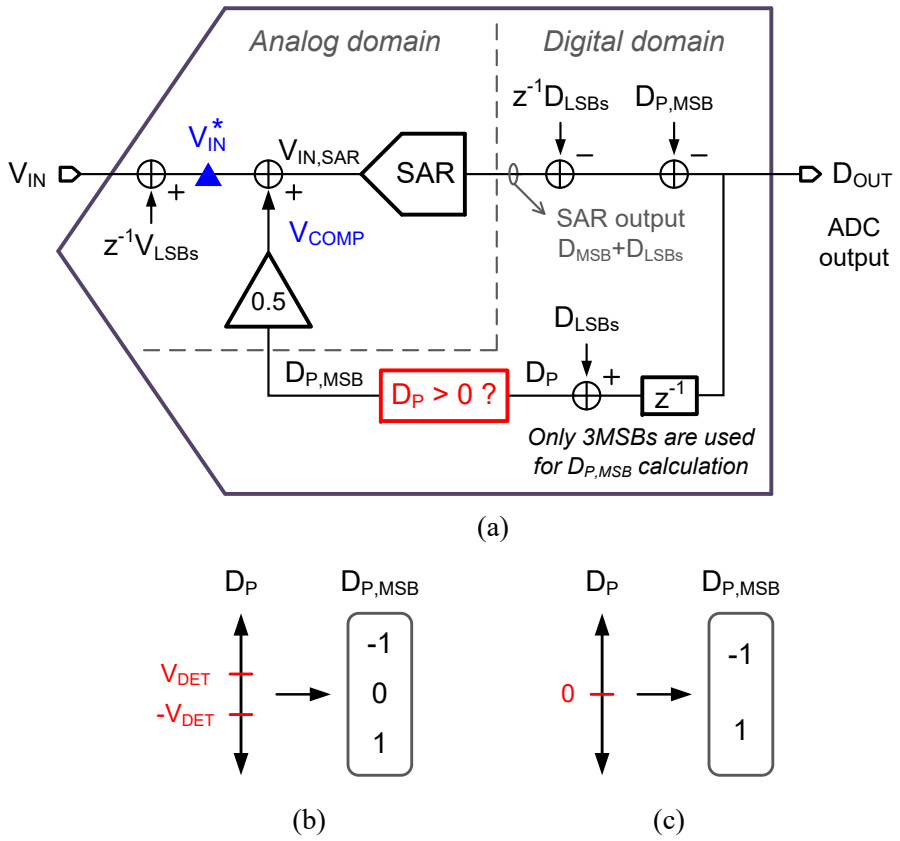


Fig. 9: (a) Principle of the MES with digital prediction. (b) Tri-level prediction scheme proposed in [18]. (c) Two-level prediction scheme in this work.

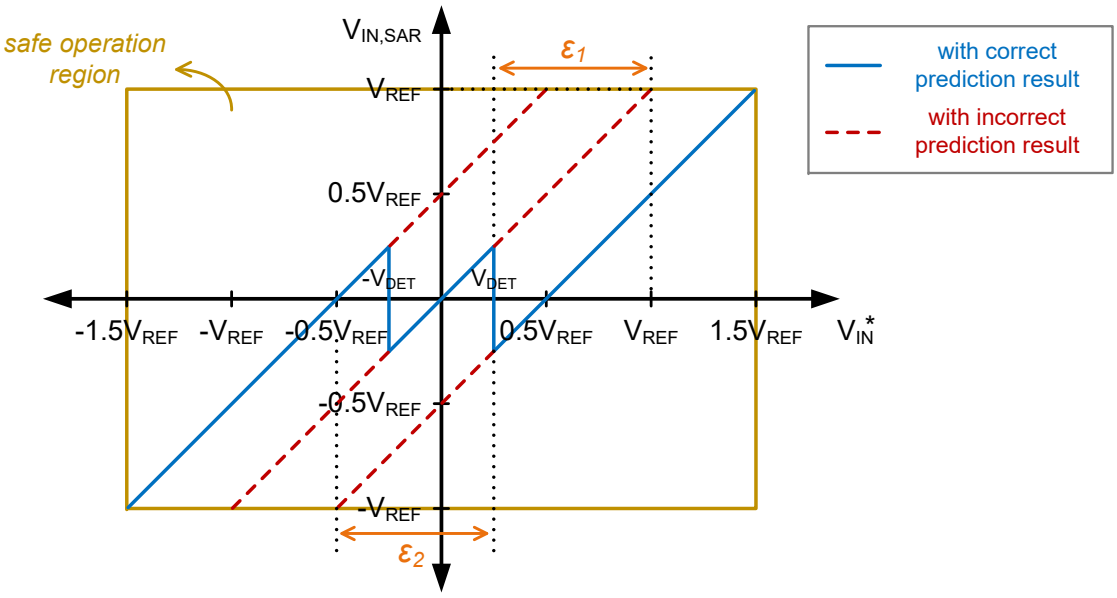


Fig. 10. Illustration of the tolerable prediction error.

prediction errors in the tri-level scheme. The possible ranges of the voltage before compensation (V^*_{IN}) and after compensation ($V_{\mathrm{IN,SAR}}$) are shown, and the

goal of the prediction scheme is to make the combination of V_{IN}^{*} and $V_{\mathrm{IN,SAR}}$ locate in the yellow area ('safe operation region'). When the prediction error occurs (dashed red line), $V_{\mathrm{IN,SAR}}$ with the wrong compensation may go beyond the yellow box. The horizontal distance of the extended red line indicates the prediction error that can be accepted. Therefore, the maximum tolerable prediction error ($\varepsilon_{\mathrm{tol}}$) can be expressed as the minimum value between ε_1 and ε_2, namely,

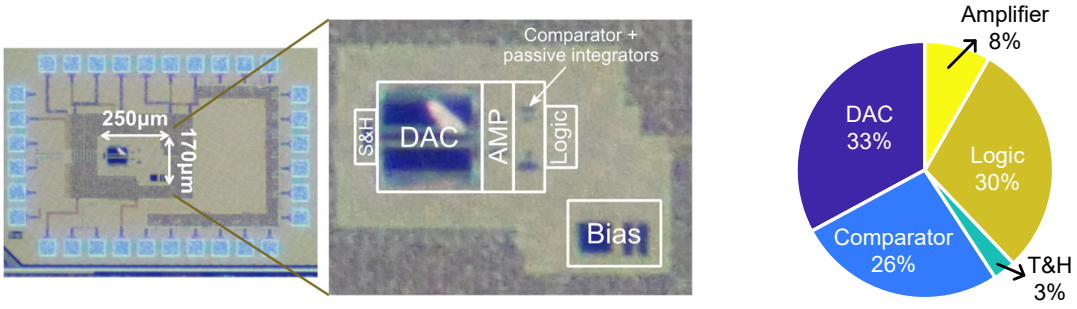
$$\varepsilon_{\mathrm{tol}} = \min(\varepsilon_1, \varepsilon_2) = \min(V_{\mathrm{REF}} - V_{\mathrm{DET}}, 0.5V_{\mathrm{REF}} + V_{\mathrm{DET}}). \quad (2)$$

In [18], V_{DET} is $0.25V_{\mathrm{REF}}$, while in our design, V_{DET} is reduced to 0. This reduces $\varepsilon_{\mathrm{tol}}$ from $0.75V_{\mathrm{REF}}$ to $0.5V_{\mathrm{REF}}$, which can be translated to a tighter OSR requirement from 3.8 to 5.6 [6].

In summary, the two-level prediction approach can avoid the input range loss and solve the mismatch problem between the two MSB capacitors in the split DAC switching scheme, but at the cost of a stricter OSR requirement.

2.3. Measurement results

The proposed DT NS-SAR ADC is fabricated in a 65 nm CMOS technology, and the die photo is shown in Fig. 11(a). It operates at 1 MHz sampling rate with an OSR of 16. Under a 1.2 V supply, it consumes 7.3 μW power with a power breakdown as shown in Fig. 11(b). Thanks to the MES, the DAC capacitance in this design is limited by the noise requirement, and it is only 1 pF per side with a power consumption of 33% of the total power. The amplifier consumes only 8% of the total power thanks to its duty-cycled operation.



(a) (b)

Fig. 11. (a) Die photo. (b) Power breakdown.

Fig. 12 shows the measured spectrum without and with MES. When MES is enabled, the measured signal to noise and distortion ratio (SNDR) is 80 dB and spurious free dynamic range (SFDR) is 98 dB. As can be seen, MES facilitates

29 dB improvement in SFDR. As can be seen from Fig. 13, over the whole 31.25 kHz bandwidth, the measured SNDR is above 80 dB and SFDR remains above 95 dB. The dynamic range (DR) is 81.4 dB.

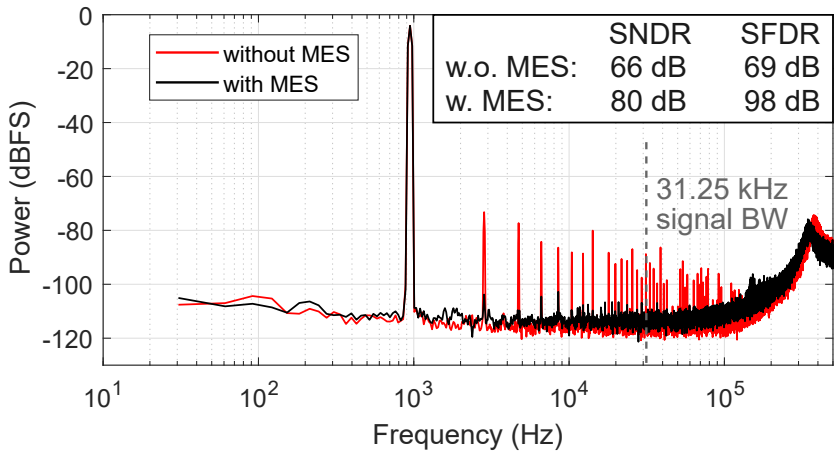


Fig. 12. Measured spectrum without and with MES.

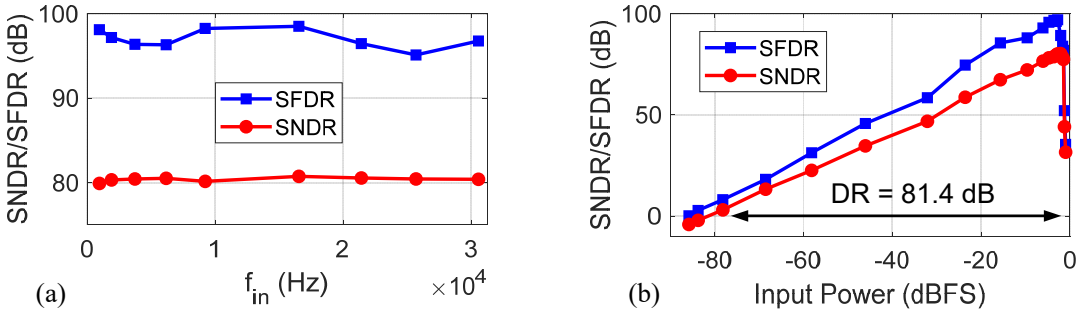


Fig. 13: (a) Measured performance over different input frequencies and (b) different input amplitudes.

3. Continuous-Time Noise-Shaping SAR ADC

As a hybrid architecture of SAR ADC and $\Delta\Sigma$ ADC, NS-SAR ADCs are expected to have the main features from the original ADC architectures. As we know, $\Delta\Sigma$ ADCs can be implemented as DT converters as well as CT converters. However, NS-SAR ADCs are conventionally designed as a DT converter. In this section, the NS-SAR architecture is extended to the CT domain, so that the NS-SAR architecture can have the advantages from CT designs, such as easy to drive and inherent anti-aliasing function. This section is based on [19], and it will introduce the concept of a CT NS-SAR ADC and provides its circuit implementation.

3.1. Architecture

Because the NS-SAR ADC is derived from a SAR ADC which typically operates in a DT manner, most NS-SAR ADCs also work as a DT converter by nature. On the other hand, a CT noise-shaping ADC would need to perform a continuous integration of the residue voltage, and this integration would be interrupted in an NS-SAR architecture due the DT SAR operation. Therefore, the fundamental challenge to develop a CT NS-SAR is to deal with the conflict between the DT-operated SAR conversion and the desired CT residue integration.

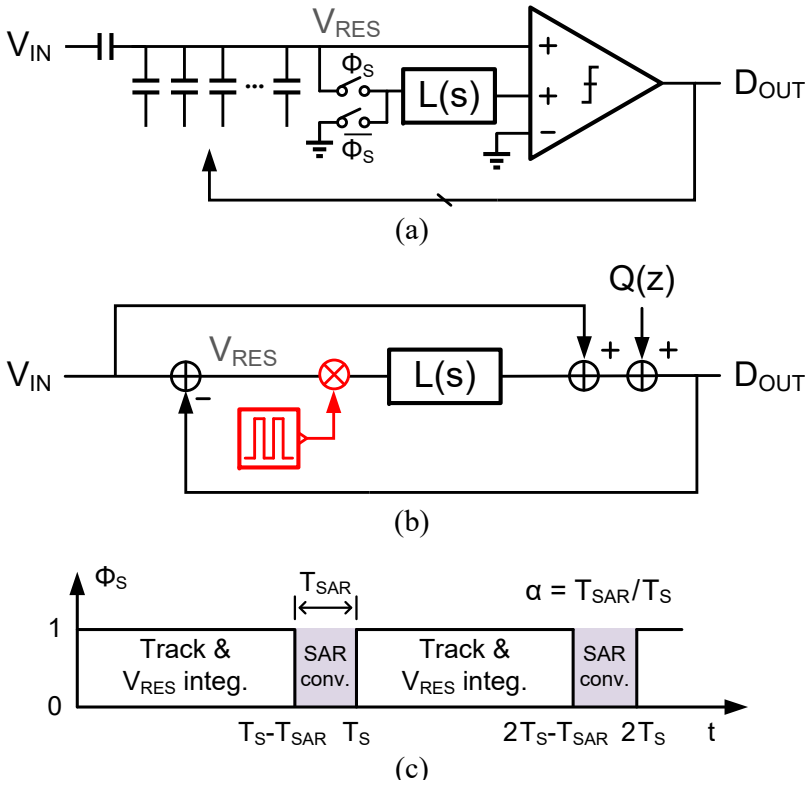


Fig. 14: (a) Block diagram, (b) signal diagram and (c) timing diagram of the proposed CT NS-SAR ADC.

This challenge can be illustrated from two aspects. First, the residue voltage V_{RES} only becomes available on the DAC after the SAR conversion is completed, which makes a continuous residue integration impossible during the SAR conversion phase. Second, the residue information on the DAC is lost in the ADC tracking phase, because the DAC is reconnected to the ADC input. In our design, two techniques are proposed to solve these two problems. First, the loop filter is duty cycled to leave sufficient time for the SAR conversion without significantly degrading the noise-shaping performance. Second, the sampling switch is removed to keep V_{RES} also in the tracking phase, and the input signal is ac coupled to the comparator, similar to the first-stage of a CT two-step SAR ADC [20].

Fig. 14 shows the diagram of the proposed CT NS-SAR ADC. The loop filter is enabled by the sampling clock Φ_{S}, and this duty-cycling operation is modeled as a clock signal multiplying the loop filter input. Here, the duty-cycle rate α is defined as the SAR conversion time T_{SAR} over the sampling period T_{S}, namely:

$$\alpha = T_{\mathrm{SAR}}/T_{\mathrm{S}}. \tag{3}$$

For a first-order loop filter ($L(s) = 1/s$), assuming the sampling frequency is 1 Hz, the noise transfer function (NTF) and the signal transfer function (STF) can be derived as [19]:

$$\mathrm{NTF}(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}}. \tag{4}$$

$$\mathrm{STF}(f) = \frac{1 - e^{-j2\pi f}}{1 - \alpha e^{-j2\pi f}} \cdot \left[\frac{1}{j2\pi f} \frac{1}{1 - e^{-j2\pi f}} \left(1 - e^{-j2\pi f(1-\alpha)}\right) + 1 \right]. \tag{5}$$

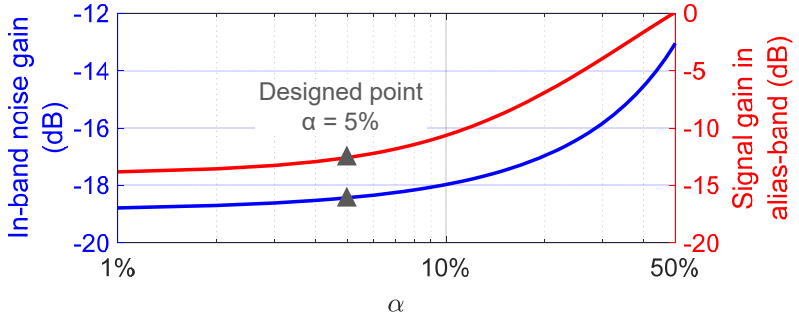


Fig. 15. In-band noise gain and alias-band signal gain with different α values.

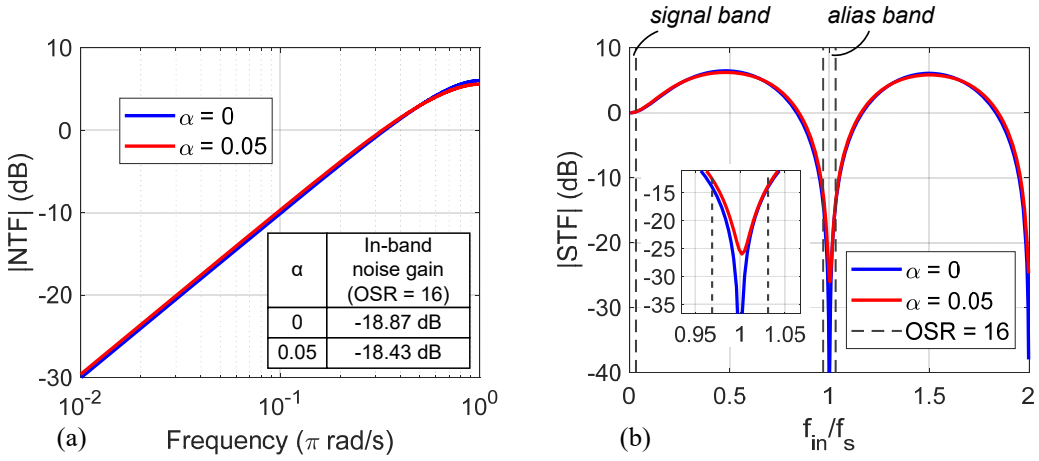


Fig. 16. (a) NTF with different α values. (b) STF with different α values.

Fig. 15 shows the in-band noise gain and the alias signal suppression with different α values. As can be seen, when α is small, the noise attenuation and the

anti-aliasing function are hardly affected. In this design, the sampling frequency is 2 MHz and α is 5% to leave enough time for the SAR conversion while minimizing the degradation on NTF and STF. Fig. 16 compares the NTF and STF magnitudes when α is 0 and α is 5%. As expected, the in-band noise gain is only degraded by 0.44 dB, and the anti-aliasing property is well preserved.

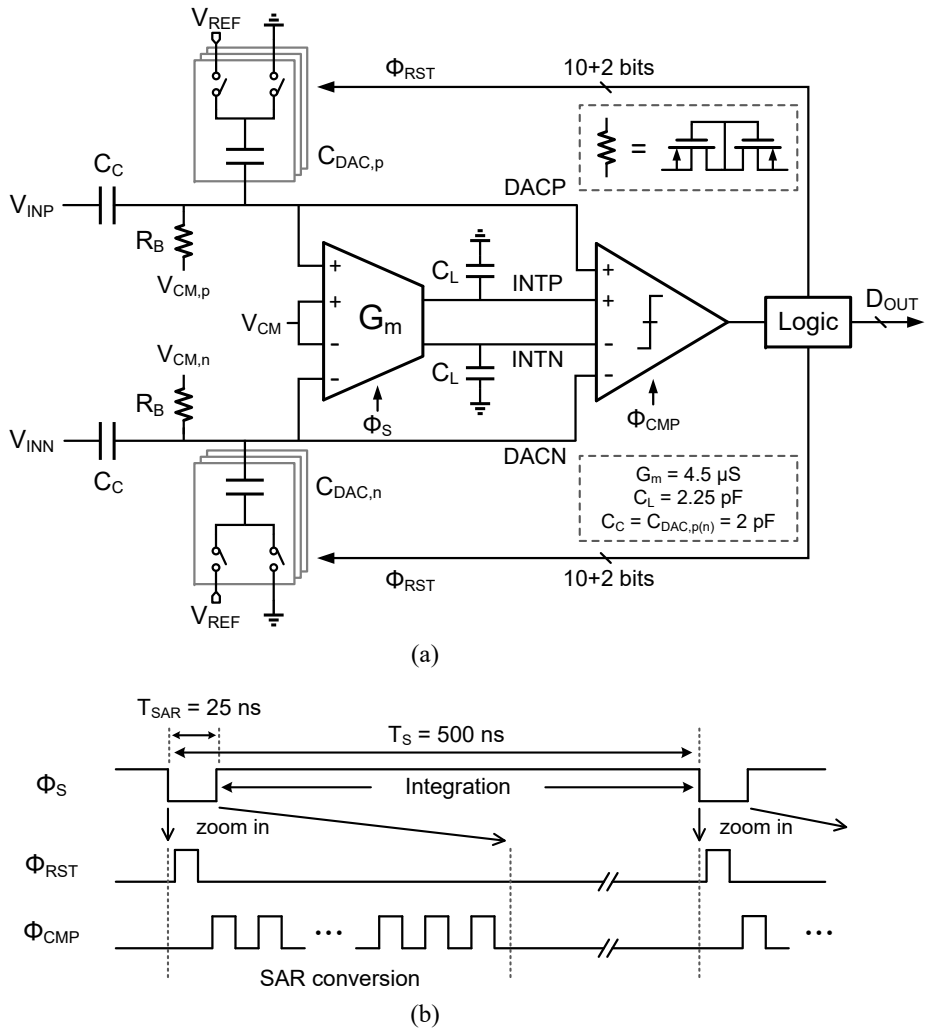


Fig. 17. (a) Proposed first-order CT NS-SAR ADC. (b) Timing diagram.

Fig. 17 shows the overall ADC architecture. The input signal is ac coupled through capacitor C_{C} to the DAC and comparator, and a pseudo-resistor R_{B} provides its dc bias. The bias resistor R_{B} and the capacitors C_{C} and $C_{\mathrm{DAC,p(n)}}$ form a high-pass filter which blocks the input dc information [20]. The integrator is on in the 95% of the sampling period, and it is switched off in the remaining 5% time for the SAR conversion. During the SAR conversion phase, the DAC is first reset, and then the converter performs the binary search quantization. Because the input signal is not a static voltage sampled on the DAC, two redundancy bits are added in the DAC to compensate for the quantization error occurring from the

varying input.

Since the integrator only integrates the small residue voltage, its output swing is relaxed, and thus a Gm-C integrator is used in this design. Instead of inserting switches as shown in Fig. 14(a) between the integrator input and the DAC, this work uses two input pairs inside the integrator which are operated in a current-steering manner, as shown in Fig. 18. The purpose of this implementation is to avoid any DAC output disturbance brought by the enable switches from Fig. 14(a) and the integrator input parasitic capacitance. When Φ_S is high, the blue branch is enabled, and the residue integration takes place. When Φ_S is low, the red branch is activated to stop the integration, and the SAR conversion starts. The bias current of the integrator is 200 nA, which leads to a transconductance of 4.5 μS to meet the noise requirement.

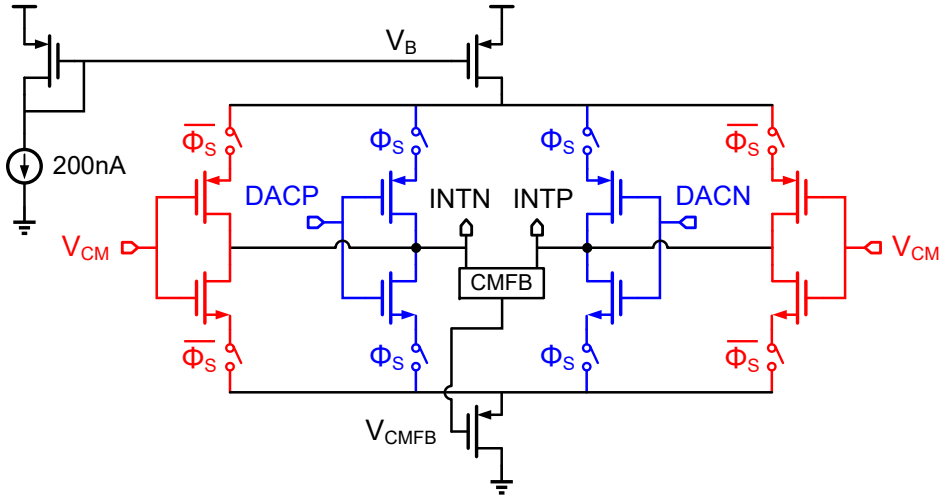


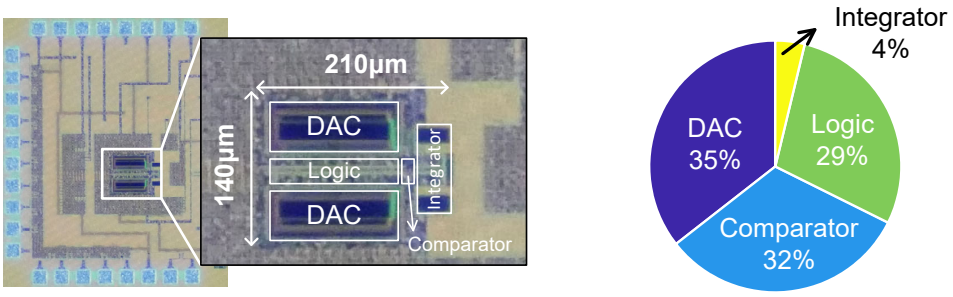
Fig. 18. Duty-cycled integrator.

3.2. Measurement results

This design is fabricated in a 65 nm CMOS technology. The 200 nA bias current is provided off-chip, and the offsets from the comparator and integrator are calibrated off-chip by tuning the DAC bias voltages $V_{\mathrm{CM,p}}$ and $V_{\mathrm{CM,n}}$. The supply voltage is 1 V, and the total power consumption is 13.5 μW. The DAC, comparator and logic consume similar power, while the integrator consumes only 4% of the total power.

Segmented data weighted averaging (DWA) is applied to the first 5 MSBs and 3 middle bits in the DAC array to improve the linearity. At a sampling rate of 2 MHz and an OSR of 16, the measured SNDR is 77 dB and SFDR is 86 dB, as shown in Fig. 20. The SNDR remains above 75 dB and the SFDR remains above 85

dB in the whole bandwidth. The measured DR is 80 dB, as shown in Fig. 21(b). The measured STF is shown in Fig. 21(c), and the theoretical calculation matches well with the measured result. It achieves at least 15 dB anti-aliasing suppression. The out-of-band peaking in STF is caused by the inherent feedforward path in the NS-SAR architecture.



(a) (b)

Fig. 19. (a) Die photo. (b) Power breakdown.

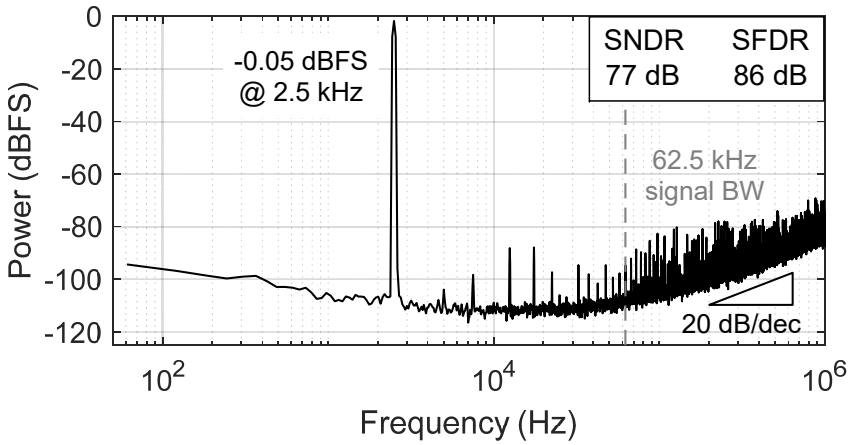


Fig. 20. Measured spectrum.

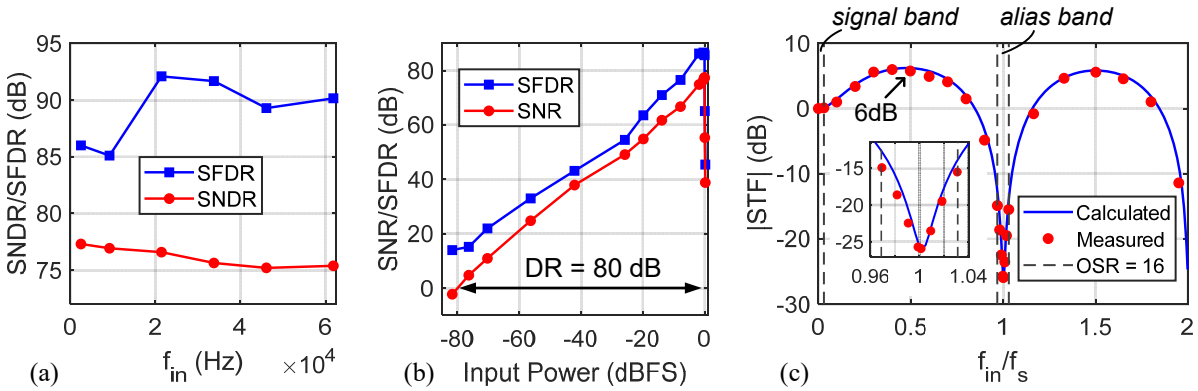


Fig. 21: (a) Measured performance over different input frequencies and (b) different input amplitudes. (c) Measured STF.

4. Discussion

Both DT and CT NS-SAR ADC architectures integrate the residue voltage on the capacitive DAC after the SAR conversion to achieve a noise-shaping function, but the main difference is the implementation of the loop filter and DAC array. The loop filter in a DT NS-SAR ADC is composed of DT circuits, such as passive integrators and DT amplifiers. Instead, the loop filter in a CT NS-SAR ADC is a CT integrator which needs to be switched off periodically. The DAC in a DT NS-SAR ADC is the same as that in a conventional SAR ADC, while the DAC in a CT NS-SAR ADC is an ac coupled capacitor network without the input sampling switch.

These different hardware implementations lead to different system properties of DT and CT NS-SAR ADCs, which are in line with the well-known pros and cons from DT and CT $\Delta\Sigma$ ADCs. DT NS-SAR ADCs can usually operate at different sampling rates easily, and its power consumption scales with the sampling frequency because (most of) its circuits only consume dynamic power. CT NS-SAR ADCs lose this flexibility in the sampling speed, but they have an inherent anti-aliasing function and are easier to drive. Because they do not require a high current to charge the load capacitor to a certain level in a given tracking time as in DT ADCs, the power consumption of the input driver could be potentially reduced.

When compared to conventional $\Delta\Sigma$ ADCs, NS-SAR ADCs are more hardware efficient because they reuse the DAC in the SAR quantizer to perform the feedback voltage subtraction as well. Moreover, the loop filter in NS-SAR ADCs only deals with the small residue voltage, which relaxes the integrator output swing and eases the system-level design. For example, the proposed CT NS-SAR ADC can avoid the static power consumption from the resistive or current DAC found in typical CT $\Delta\Sigma$ ADCs, and it does not need an extra feedforward amplifier to reduce the integrator output swing as in [21]. However, due to the recursive SAR conversion steps and the constraint on the duty-cycle rate α, the CT NS-SAR ADC is only suitable for low-speed applications.

5. Conclusion

This paper presents NS-SAR ADC designs in both DT and CT domains. For the DT NS-SAR ADC, three loop filter structures are benchmarked in terms of their power efficiency. A duty-cycled amplifier is proposed to achieve high gain and dynamic power consumption together with its duty-cycled bias generation

circuits. A two-level digital-predicted MES technique is used to improve the linearity without saturating the ADC. For the CT NS-SAR ADC, a 5% duty-cycling is applied to the loop filter to accommodate for the SAR conversion without significant degradation on the noise-shaping performance. As other CT ADC architectures, the proposed CT NS-SAR ADC has an implicit anti-aliasing function and is easy to drive.

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