A 10-bit 4 MS/s SAR ADC with Fully-Dynamic Duty-Cycled Input Driver

A 10-bit 4 MS/s SAR ADC with Fully-Dynamic Duty-Cycled Input Driver

Hanyue Li, Yuting Shen, Eugenio Cantatore and Pieter Harpe
Integrated Circuits Group, Eindhoven University of Technology, Eindhoven, The Netherlands
Email: h.li2@tue.nl

***Abstract*—This paper presents a duty-cycled input driver for a SAR ADC. Being a discrete-time system, the SAR ADC requires an accurate input signal only at its sampling moment. This motivates the use of a duty-cycled input driver which can be turned off during the conversion phase to save power. In this way, the power consumption of the SAR ADC together with its input driver becomes fully dynamic. This idea is applied to a 10-bit 4 MS/s SAR ADC with unity-gain input drivers. Fabricated in 65 nm CMOS, the prototype achieves 8.9 ENOB and 69.9 dB SFDR while consuming 35.0 μW. This leads to a Walden FoM of 18.3 fJ/conversion-step for the ADC including driver.**

***Index Terms*—SAR ADC, input driver, unity-gain buffer, duty cycle, low power**

I. Introduction

Thanks to its simple structure and low power consumption, successive-approximation-register (SAR) analog-to-digital converters (ADC) have become popular in both research and commercial applications where the energy is constrained. Despite the excellent power efficiency of the SAR ADC core, its peripheral blocks, such as input driver, filter, reference buffer and digital communication interface, can still consume a considerable amount of power [1]. Therefore, low-power techniques for these peripheral circuits are also indispensable to optimize the power efficiency of the overall system.

This paper focuses on the input driver for the SAR ADC. Generally speaking, an ADC input driver can realize multiple functions, such as signal gain, level shifting, single-ended to differential conversion, high driving capability, etc. In different analog signal processing systems, the configuration of the ADC input driver can also vary, depending on the system requirements. This work chooses a unity-gain buffer as a basic input driver solution, as shown in Fig. 1. The load for the input driver is the capacitive digital-to-analog converter (DAC) inside the SAR ADC. In the tracking phase, the driver output (V_{BUF}) tries to follow the input signal (V_{IN}). In the conversion phase, the buffered input is sampled on C_{DAC}, and the SAR conversion starts. At the beginning of the tracking phase, a kickback voltage (V_{kick}) can be observed at the driver output, due to the difference between the initial V_{BUF} voltage and the voltage on C_{DAC} from the last conversion period. To guarantee an accurate sampling result, the settling error (V_{error}) needs to be small enough (e.g. less than half an LSB) at the end of the tracking phase. This requires a low output impedance from the driver, which translates in minimum requirements for its power consumption. Therefore, for a given ADC resolution, the input driver power can be estimated to be inversely proportional to the tracking time (T_{track}), namely:

$$P_{\mathrm{driver}} \propto \frac{1}{T_{\mathrm{track}}}. \tag{1}$$

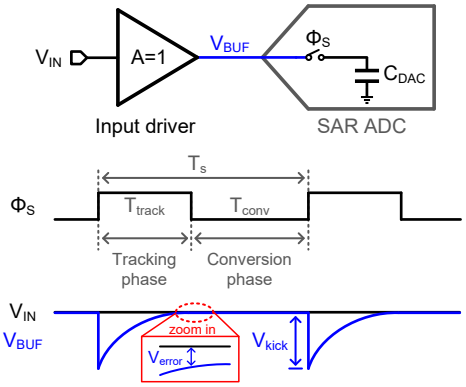

Fig. 1. Model of the input driver with a SAR ADC.

Fig. 2 shows three possible realizations of the unity-gain input driver for a differential SAR ADC. Amplifiers in a unity-gain feedback loop can be directly connected to the SAR ADC as the most straight forward approach [2]. On top of that, a passive RC filter can be inserted between the input driver and the ADC to provide extra filtering [3]. Thanks to the large C_{FIL}, this approach limits the amplifier noise bandwidth, helps with stability and reduces the kickback voltage V_{kick} shown in Fig. 1. However, this large C_{FIL} requires an even stronger driving capability and may not be an optimal idea for on-chip implementation due to its area cost. A source follower can be embedded in the SAR feedback loop, so that the input signal and DAC output go through the same non-linear driver function [4]. In this way, the overall system can achieve high linearity despite the non-linear behaviour in the driver itself. However, the settling error needs to be examined not only in the tracking phase, but also in each SAR comparison cycle. This work aims to provide a low-power input driver solution for a 10-bit SAR ADC. The structure in Fig. 2(a) is adopted, as it is generic, and can easily satisfy the noise and linearity requirements for 10-bit resolution.

This paper is organized as follows. Section II presents the proposed duty-cycled input driver. Section III shows the measurement results, and Section IV draws conclusions.

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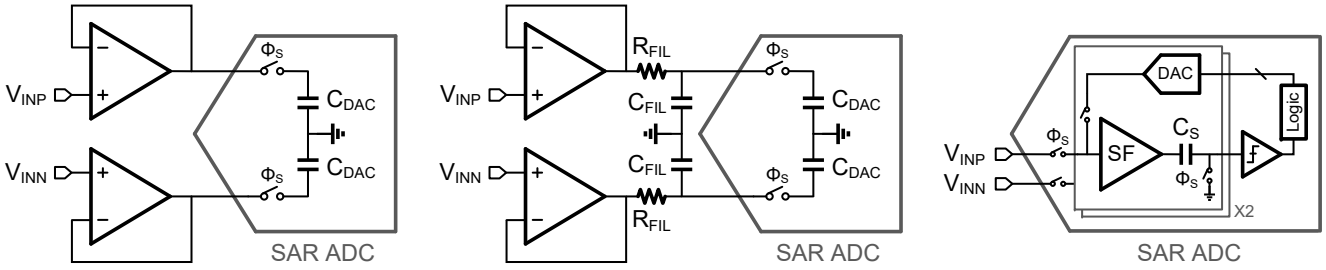

Fig. 2. Three unity-gain input driver structures: (a) unity-gain buffer directly connected with SAR ADC, (b) unity-gain buffer with an extra RC filter, and (c) loop embedded source follower.

II. Duty-Cycled Input Driver

A prior work [2] swaps two input drivers according to the differential input signal polarity, so that the maximum output swing is reduced for each amplifier, but the input driver still consumes 15× higher power compared to the ADC itself. This is mainly because the input driver is always on with a static bias current. In contrast, the SAR ADC only consumes dynamic power. Note that the main function of the input driver is to provide an accurate replica of the input signal to the ADC at the end of the tracking phase. Therefore, the driver output is most critical at the sampling moment, and it is less relevant during the conversion phase. This provides the possibility to disable the input driver in the conversion phase. As long as the driver can start up again and track the input signal properly in the given tracking time, the final ADC performance should not be affected. In this way, the driver power from (1) becomes fully dynamic, as we have:

$$P_{\text{driver}} \propto \frac{1}{T_{\text{track}}} \cdot \frac{T_{\text{track}}}{T_{\text{s}}} = \frac{1}{T_{\text{s}}} = f_{\text{s}}. \tag{2}$$

This dynamic power consumption indicates the flexibility of the driver to operate efficiently at different sampling rates (f_{s}). For an always-on driver, the amplifier needs to be redesigned for a different sampling speed, due to the change in settling time. Instead, for a duty-cycled driver, the same amplifier can be used at different sampling rates by keeping a constant T_{track} duration. Therefore, this duty cycling technique can provide higher efficiency, flexibility, and re-usability.

The idea of duty cycling an amplifier can be traced back to [5], where it was named as "switched-opamp". This approach was initially proposed to solve the low conductivity problem of CMOS switches under low supply conditions in older technologies. In our work, it is applied to the ADC input driver for the purpose of saving power. Fig. 3 shows the proposed duty-cycled input driver. It is designed in 65 nm CMOS for a SAR ADC [6] operating at 1 V supply. The supply voltage of the driver is 1.6 V to ensure sufficient voltage headroom for the full-scale ADC input range (1 $V_{\text{pp,diff}}$). The PMOS current mirror and top switches are built with thick-oxide devices, while the other transistors are thin-oxide devices. The bulk terminals of the input transistors are connected to their source terminals to avoid the body effect. The enable clock Φ_{DRIVER} is the same as the ADC sampling clock Φ_{S}, thus the driver is only

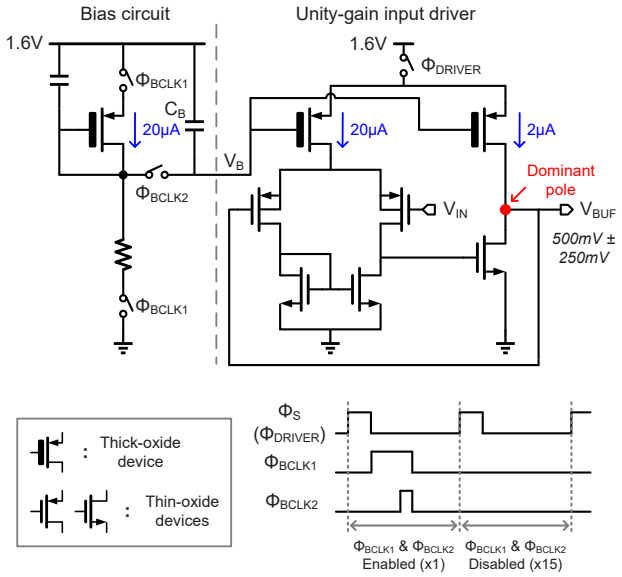

Fig. 3. Proposed duty-cycled input driver.

enabled in the tracking phase. The dominant pole is located at the second stage, so no Miller compensation is needed. When the load capacitor is disconnected after the tracking phase, the amplifier can become unstable and start ringing. But this is not a concern in this design as the amplifier is also turned off after the sampling moment. When the amplifier is on, the static bias current is 22 μA. The bias generation circuit is also duty-cycled to achieve a dynamic operation, similar to [7]. The bias voltage V_{B} is kept on the capacitor C_{B} (2 pF), and the duty-cycling control clocks Φ_{BCLK1} and Φ_{BCLK2} are enabled once every 16 sampling clock cycles to refresh V_{B} with minimal power overhead. Both Φ_{BCLK1} and Φ_{BCLK2} are derived from the ADC control logic.

A pseudo-differential version of the duty-cycled driver is used to drive a 10-bit SAR ADC [6] at 4 MS/s sampling rate. The DAC capacitance is 250 fF per side. With this 250 fF load capacitor, the open-loop amplifier has a dc gain of 53 dB and a -3dB bandwidth of 200 kHz to meet the linearity and speed requirements. In closed-loop, it has an input-referred noise of 170 μV_{rms} and an input capacitance of 3 fF based on post-layout simulation results.

III. Measurement Results

The input driver and the 4 MS/s 10-bit SAR ADC are fabricated in a 65 nm CMOS technology. They occupy in total 0.0066 mm^2 area, as shown in Fig. 4(a). With a 30% duty-cycle rate ($T_{track}/T_s = 30\%$), the total power consumption is 35.0 μW: 24.5 μW for the driver and 10.5 μW for the ADC. The power breakdowns for always-on and duty-cycled operation are shown in Fig. 4(b). Compared to the case where the input driver is always on, the duty-cycled amplifier together with its duty-cycled bias circuit saves 76% of the input driver power, while it only causes 2% increase in the ADC power to generate the bias control clocks Φ_{BCLK1} and Φ_{BCLK2}.

Fig. 5 shows the measured spectrum at near-Nyquist input frequency when the input driver is always on or duty cycled. When the driver is duty cycled, the measured SNDR and SFDR are 55.33 dB and 69.94 dB, respectively. As can be seen, the SNDR and SFDR are hardly affected by the duty cycled operation. Fig. 6 shows the measured INL and DNL also in these two modes. Similar code error patterns can be observed no matter the driver is duty cycled or not. When the driver is always on, more fuzzy tones can be seen in the INL and DNL results. This is likely due to the underdamped amplifier ringing after the sampling moment. Fig. 7 shows the measured performance with different input frequencies and input amplitudes. The dynamic range is 56.2 dB. Fig. 8 shows the measured performance at different duty-cycle rates. The minimum functional duty-cycle rate is 30%, because the amplifier may not settle completely with a shorter T_{track}. The driver power consumption scales linearly with the duty-cycle rate as expected. Fig. 9 shows the measured performance at different sampling rates, where T_{track} is kept the same (75 ns). This duty-cycled driver can work down to 2 kS/s sampling rate. A lower SFDR can be observed at lower sampling rates, which is because the internal nodes in the amplifier leak away with a long sampling period, and more time is needed for the amplifier to start up. A longer T_{track} may help to improve the

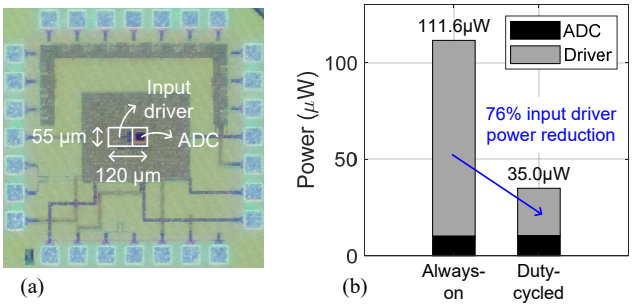

Fig. 4. (a) Die photo. (b) Power breakdown.

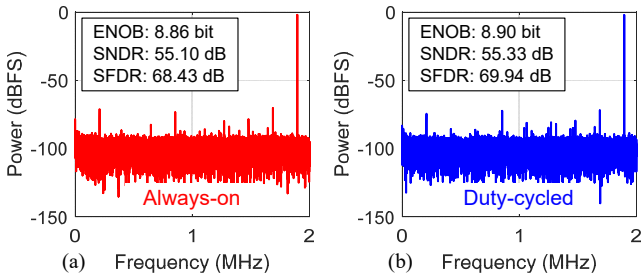

Fig. 5. Measured spectrum when the driver is (a) always on and (b) duty cycled.

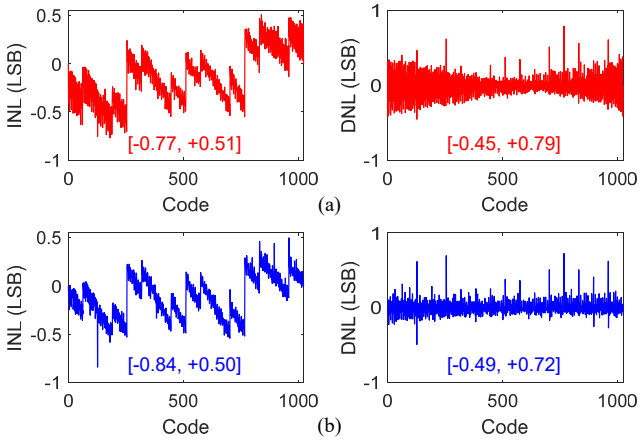

Fig. 6. Measured INL and DNL when the driver is (a) always on and (b) duty cycled.

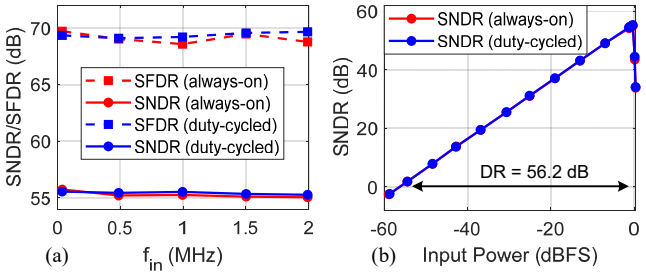

Fig. 7. Measured performance at different (a) input frequencies and (b) input amplitudes.

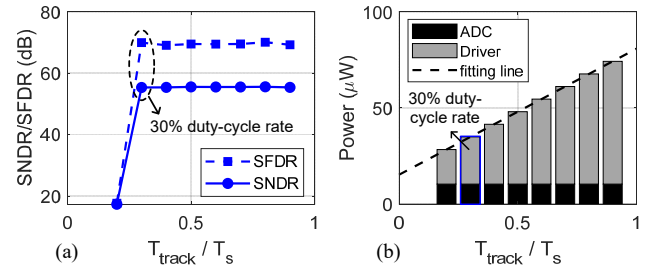

Fig. 8. (a) Measured SNDR and SFDR, and (b) measured power at different duty-cycle rates. All measurements are at 4 MS/s.

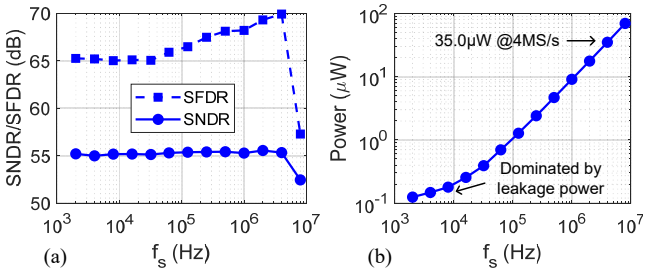

Fig. 9. (a) Measured SNDR and SFDR, and (b) measured power of driver + ADC at different sampling rates (T_{track} is fixed to 75 ns).

TABLE I
BENCHMARK WITH OTHER SAR ADCS INCLUDING A CO-DESIGNED INPUT DRIVER

Reference	ISSCC'15 [4]	CICC'19 [9]	A-SSCC'19 [10]	ISSCC'22 [11]	A-SSCC'15 [8]	CICC'19 [2]	This work	
Technology (nm)	40	65	180	65	28	65	65	
Supply (V)	1.2 / 2.5	0.9 / 2.1	1.5	1.2 / 2	1.1 / 1.2	1.2	1 / 1.6	
F_{sample} (MHz)	35	80	5.12	5	104	4	4	
Bandwidth (MHz)	17.5	2	0.32	0.5	52	2	2	
Area (mm^2)	0.236	0.081	0.192	0.075	0.024	0.04	0.0066	
Input driver type	Loop embedded source follower				Class-AB amplifier	Class-A unity-gain buffer with pre-comparison	Class-A unity-gain buffer	
							always-on	duty-cycled
ENOB (bit)	12.1	12.0	12.1	13.7	7.2	8.7	8.9	8.9
SNDR (dB)	74.4	73.8	74.8	84.1	45	54.3	55.1	55.3
SFDR (dB)	90	87.3	86.1	97	51	66	68.4	69.9
Power (μW)	54500	2130	180.1	133.88	2340	149	111.6	35.0
FoM_W (fJ/conv.-step)	363.1	133.0	62.0	10.2	154.9	87.7	60.0	18.3
FoM_S (dB)	159.5	163.5	167.3	180.0	148.5	155.6	157.6	162.9
Fully dynamic	No	No	No	No	No	No	No	Yes

FoM_W = Power / ($2^{ENOB} \times 2 \times$Bandwidth) FoM_S = SNDR + $10\log_{10}$(Bandwidth/Power)

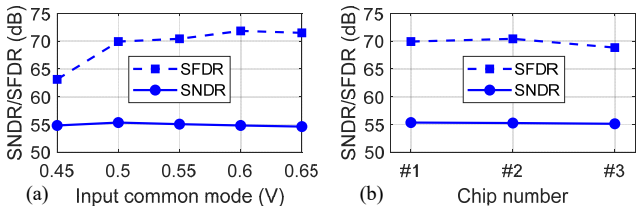

Fig. 10. (a) Measured SNDR and SFDR at different input common mode voltages. (b) Measured SNDR and SFDR over 3 samples.

SFDR at low sampling rates. The total power also scales with the sampling rate, thus a fully dynamic operation is realized. Fig. 10(a) shows the measured results with different input common mode voltages. The default input common mode is 0.5 V, which is half of the ADC supply. The performance is consistent over 3 measured chips, as shown in Fig. 10(b).

Table I shows the comparison table with other ADCs featuring a co-design of a SAR ADC and its input driver. Compared to [2] with the same bandwidth and resolution, this design has a similar Walden FoM (FoM_W) when the driver is always on. When the duty cycling technique is applied, the FoM_W improves by 3×. High-resolution designs tend to use a loop embedded source follower, as explained in Section I. A recent work [11] achieves outstanding power efficiency, because its sampling noise cancellation technique helps to reduce the sampling capacitor size, and this greatly relaxes the output impedance requirement for the input driver. Compared to other works, this work is the only design with a dynamic driver, enabling scalability of power vs sampling rate over 3 orders of magnitude.

IV. CONCLUSIONS

A duty-cycled input driver for SAR ADCs is proposed in this paper. By switching off the input driver during the conversion phase, the driver power can be reduced by 76% without degrading the ADC performance. Moreover, the entire system consumes only dynamic power, and is thus efficiently scalable with the sampling rate over 3 orders of magnitude. Thanks to this technique, the 10-bit 4 MS/s SAR ADC together with its input driver achieves 55.3 dB SNDR and 69.9 dB SFDR, and it consumes only 35.0 μW.

V. ACKNOWLEDGMENT

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