Small-Area SAR ADCs With a Compact Unit-Length DAC Layout

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Hanyue Li, *Graduate Student Member, IEEE*, Yuting Shen, *Graduate Student Member, IEEE*, Eugenio Cantatore, *Fellow, IEEE*, and Pieter Harpe, *Senior Member, IEEE*

***Abstract*—This paper presents four small-area SAR ADCs with a resolution from 8 to 11 bits. Two area-saving techniques are utilized. First, the DAC layout is implemented with custom designed unit-length capacitors, which are optimized for each resolution to minimize the chip area. Second, dynamic logic is applied to the 8-bit design to further reduce the number of transistors and save area. Fabricated in 65 nm CMOS, the 8/9/10/11-bit SAR ADCs only occupy 20×21 μm, 20×36 μm, 36×36 μm and 36×36 μm, respectively. At 10 MHz sampling rate, their measured ENOB is 7.5, 8.3, 9.1 and 9.8 bits with an SFDR of 65.4 dB, 67.4 dB, 78.0 dB and 76.5 dB, respectively. Compared to prior-art, these designs achieve the smallest areas for the achieved ENOBs.**

***Index Terms*—SAR ADC, small area, area efficiency, unit length, DAC layout, dynamic logic.**

I. Introduction

OVER the past two decades, the power efficiency of analog-to-digital converters (ADC) has improved more than 1000× thanks to various circuit and architecture innovations [1], [2]. Among ADCs, the successive-approximation-register (SAR) ADC is a key contributor owing to its simple structure and compatibility to new technologies. Besides power consumption, the area efficiency can also be of great importance for emerging applications like neural recording, ultrasound imaging and image sensing where an ADC array is needed [3], [4]. Small-area SAR ADCs can be a well-suited choice for these application scenarios.

Typically, the area of a charge redistribution SAR ADC [5] is dominated by the switched-capacitor digital-to-analog converter (DAC). Due to the binary scaled DAC structure, the total DAC capacitance grows exponentially with increased resolution. The size of the DAC array is determined mainly by three factors: kT/C sampling noise, mismatch requirements and minimum physical size constraints [2]. Among these, the kT/C sampling noise is regarded as the fundamental limit in most designs, as mismatch could be calibrated, and physical size depends on technology. Table I summarizes the required DAC capacitance in a differential SAR ADC for different resolutions when only kT/C noise is considered. It is assumed that for an N-bit ADC, 2^N DAC unit capacitors are needed per side. The kT/C noise power is set to be equal to the quantization noise, and the reference voltage V_{REF} is 1 V. As can be seen, on the one hand, the DAC capacitance can reach a few pF for high-resolution SAR ADCs. In this case, ADC area reduction can be achieved by oversampling [6] or sampling noise cancellation techniques [7]. On the other hand, for low-resolution SAR ADCs, the required unit capacitor is so small that it is often overdesigned due to practical physical size limitations, leading to unnecessary area cost. Therefore, this paper aims to optimize the area of SAR ADCs with a resolution from 8 to 11 bits. Note that the thermal noise limited minimum capacitance decreases with V_{REF}, so this area optimization is particularly important at higher V_{REF}.

TABLE I
CAPACITOR SIZE FOR DIFFERENT SAR ADC RESOLUTIONS

# bits N	C_{DAC} (pF)	C_{u} (aF)	# bits N	C_{DAC} (pF)	C_{u} (aF)
8	0.0016	6	12	0.4	102
9	0.0065	13	13	1.7	203
10	0.026	25	14	6.7	407
11	0.1	51	15	26.7	814

* C_{DAC} is the DAC capacitance per side. C_{u} is the unit capacitance. $C_{\text{DAC}} = 2^N C_{\text{u}}$.

Different solutions have been proposed in literature to reduce the chip area for low-resolution SAR ADCs. A bridge capacitor can be used with a compact layout as in [8], but it requires a careful examination of the parasitics. A charge injection cell [9] eliminates the necessity for binary-scaled capacitors, but it requires a high frequency synchronous clock for the internal logic control [10]. MOS transistors have also been used as capacitors in the DAC [11], but its area is still limited by the minimum transistor size provided by the technology. Custom designed capacitors are widely used because they can realize unit capacitors below 1 fF. A unit-element-based layout approach can be found in [12], [13] and [14], but the DAC interconnections can still occupy substantial area [13]. Recently, a unit-length-based layout is proposed [4], and it has reduced the area of a 10-bit SAR ADC to 36×36 μm in 65 nm CMOS. This work is based on the same unit-length DAC layout principle, but expands it to achieve even better area efficiency for the 8, 9 and 11-bit SAR ADCs.

This paper is organized as follows. Section II describes the proposed compact DAC layout structure. Section III details

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The authors are with the Department of Electrical Engineering, Eindhoven University of Technology, 5600 MB Eindhoven, The Netherlands (e-mail: h.li2@tue.nl).

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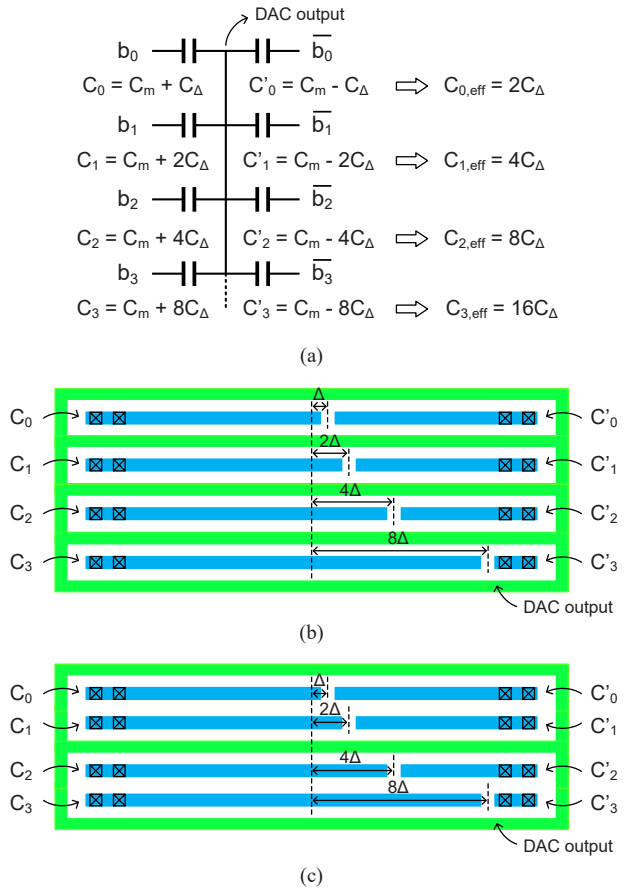


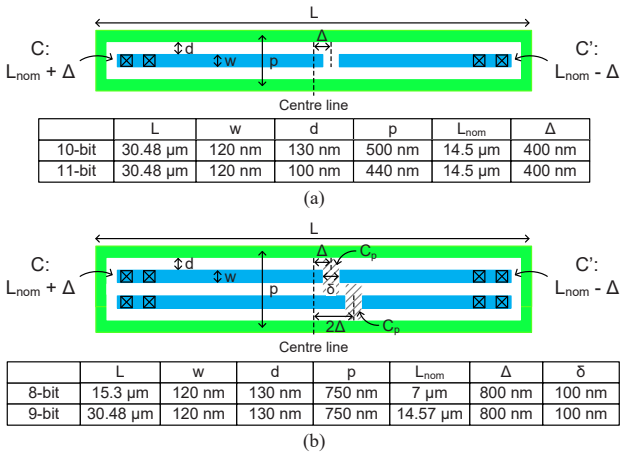
Fig. 1. (a) DAC schematic. (b) Original unit-length DAC layout in [4]. (c) Modified unit-length DAC layout. A 4-bit DAC is shown for simplicity.

the dynamic logic for the 8-bit ADC. Section IV presents the measurement results and Section V draws conclusions.

II. Unit-Length DAC Layout

A conventional charge-redistribution SAR ADC utilizes a binary-scaled capacitive DAC, where the unit cell in the DAC array is implemented as a single capacitor. Instead, in the unit-length DAC [4], each unit cell consists of two capacitors driven by opposite control bits, as shown in Fig. 1(a) and Fig. 1(b). In this way, the effective DAC unit cell is formed by the difference between a "positive" capacitor (C_0) and a "negative" capacitor (C_0'), e.g. $C_{0,\text{eff}} = C_0 - C_0' = 2C_\Delta$. The accuracy of the DAC capacitors is then determined by the relative length difference (Δ, 2Δ, 4Δ, etc.) of metal strips instead of their absolute length value. This unit-length configuration greatly reduces the number of unit cells in the DAC array while maintaining 10-bit linearity without calibration [4].

This unit-length DAC layout can be further simplified to provide even lower unit capacitance and smaller area for a SAR ADC with lower resolution. Fig. 1(c) shows the proposed DAC layout. The green metal strips between two adjacent unit cells are removed, and two DAC bits are merged into a single enclosed structure. In this way, the DAC capacitor is formed by the single-side coupling capacitor between the DAC bottom



	L	w	d	p	L_{nom}	Δ	δ
10-bit	30.48 µm	120 nm	130 nm	500 nm	14.5 µm	400 nm	
11-bit	30.48 µm	120 nm	100 nm	440 nm	14.5 µm	400 nm	
8-bit	15.3 µm	120 nm	130 nm	750 nm	7 µm	800 nm	100 nm
9-bit	30.48 µm	120 nm	130 nm	750 nm	14.57 µm	800 nm	100 nm

(b)

Fig. 2. Dimension of the unit-length DAC layout in (a) 10-bit and 11-bit ADCs, and in (b) 8-bit and 9-bit ADCs.

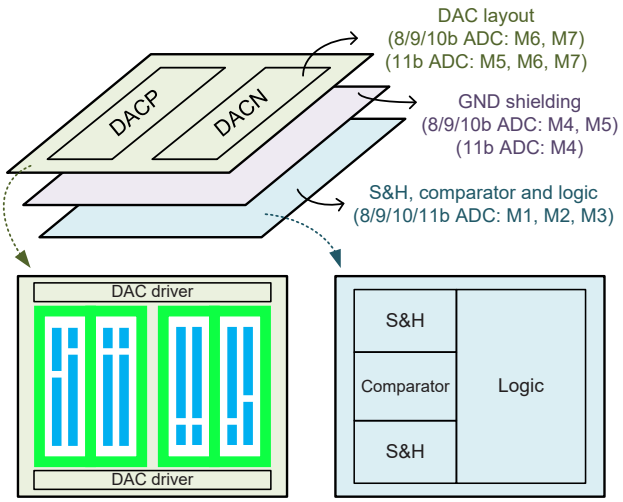


Fig. 3. ADC layout floorplan.

plate (blue strips) and the DAC top plate (green strips), which halves the minimum C_Δ compared to the original layout in Fig. 1(b). With the same number of bits, this modified layout can also save about 25% DAC area compared to the original one. Both the reduction of capacitance and area are beneficial, especially for low-resolution SAR ADCs (Table I).

Despite the compactness of the proposed layout, a drawback is the undesired coupling capacitance C_p between the DAC bottom plate and the opposite top plate, as shown in Fig. 2(b). This parasitic capacitance C_p exists only for either C or C', thus it cannot be cancelled by subtracting C' from C during the SAR conversion. This causes systematic non-linearity for the converter. To minimize its effect, the distance between the two confronting blue metal strips [δ in Fig. 2(b)] is set to the minimum allowed space. In practice, the DAC least significant bits (LSBs) are implemented with unit-length layout cells and the DAC most significant bits (MSBs) are built with unary layout cells [4], so the C_p-induced non-linearity will only affect LSB mismatch. The proposed layout is used in the 8-bit and 9-bit SAR ADCs, where lower accuracy is acceptable

and reduced capacitor values and area are preferred. Based on parasitic extraction, C_p is about 12 aF, and it causes a systematic error of 0.2 LSB INL and 0.2 LSB DNL for both the 8-bit and 9-bit ADCs. The exact capacitor dimensions in Fig. 2 are determined by two aspects: firstly, the experimental results in [4] were used to estimate which dimensions can achieve acceptable matching. Secondly, the dimensions were minimized as much as possible to fit in the overall ADC area.

The 10-bit ADC is the same as in [4] as a reference design. The original DAC layout in Fig. 1(b) is adopted in the 11-bit ADC. To meet the more stringent kT/C noise requirement in an 11-bit ADC, the capacitance density is increased by using the minimum spacing between DAC plates [d in Fig. 2(a)] and stacking 3 rather than 2 metal layers. This approach results in minimal area but is sub-optimal for matching. As an alternative, one could investigate to use less stacked metals and instead increase the L, Δ, d, p and w dimensions (Fig. 2) to improve matching while maintaining a small total capacitance value, at the cost of increased chip area. The DAC layout is placed on top of the other blocks, as shown in Fig. 3 [4]. For the 8, 9 and 10-bit ADCs, the DAC layout is composed of metal 6 (M6) and metal 7 (M7), and metal 1 (M1) to metal 3 (M3) are used for wiring the circuitry. Metal 4 (M4) and metal 5 (M5) are used as shielding layers. For the 11-bit ADC, three metal layers (M5 to M7) are stacked to form the DAC, which leaves only one metal layer (M4) for shielding.

III. Dynamic Logic

The DAC layout area scales exponentially with resolution, but the logic area only scales linearly. For the 10-bit ADC in [4], standard-cell-based logic is used and that fits well in the space under the DAC layout. However, in an 8-bit ADC layout, the DAC can be scaled to only a quarter of the original design in [4], while the logic area has only shrunk by 20%. In this case, the digital logic can be the bottleneck in the whole ADC area scaling. To further reduce the logic area, dynamic logic [13] is used in the 8-bit ADC because it requires less transistors than the standard-cell-based logic.

The overall logic diagram is shown in Fig. 4(a). A conventional DAC switching scheme [5] is used in this design, so the MSB control logic (Fig. 4(b)) is slightly different from the other bits (Fig. 4(c)). After the input is sampled on the DAC, the $reset$ signal goes low and this triggers the MSB comparison. After one bit is resolved, the $next\_bit\_set$ (namely, bit_set in the next bit control stage) goes high to enable the next bit DAC toggling. When all the 8 bits are available, $reset$ goes high to reset the DAC, and a $latch$ pulse is generated for the data read-out. The control logic state information is stored on the internal nodes, denoted as red dots in Fig. 4. These nodes can be floating during part of the conversion process. In [13], additional capacitors were added to safely maintain the state. This work removes those capacitors and uses high-V_t transistors for the critical nodes to save area. This approach shows stable digital functionality over PVT variations. Moreover, compared to [13], one redundant transistor connected to $\overline{cmp\_rdy}$ is removed to simplify the design.

A double-tail dynamic comparator [15] is used in the 10-bit and 11-bit ADCs, while a simpler StrongARM latch [16] is chosen for the 8-bit and 9-bit ADCs thanks to the relaxed noise requirement at lower resolutions. The sampling switch is implemented as an NMOS switch with a boosted clock for all the four ADCs. The DAC capacitance per side is 55 fF, 107 fF, 250 fF and 690 fF, for the 8/9/10/11-bit designs, respectively.

IV. Measurement Results

All four designs are fabricated in a single 65 nm CMOS test chip, where the 10-bit ADC is a copy from [4] as a reference design. Fig. 5(a) shows the die photo. The proposed 8, 9 and 11-bit ADCs occupy an area of only 20×21 μm, 20×36 μm and 36×36 μm, respectively. Fig. 5(b) shows the power breakdown of each ADC. For low-resolution SAR ADCs, the DAC power is only a small fraction of the total ADC power, while digital power can become dominant.

Fig. 6 shows the measured spectrum for all four ADCs at Nyquist input frequency. The sampling rate is 10 MS/s. The

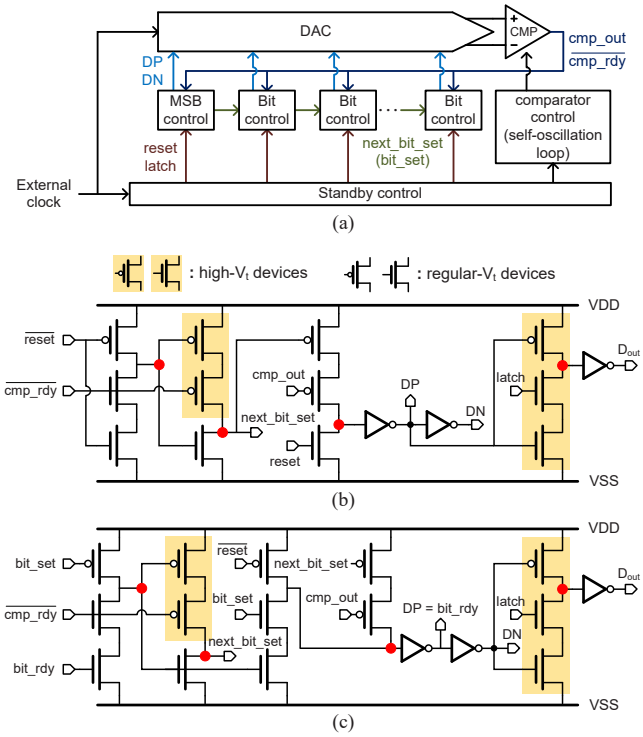


Fig. 4. (a) Overall logic diagram. (b) MSB control block and (c) control block for other bits.

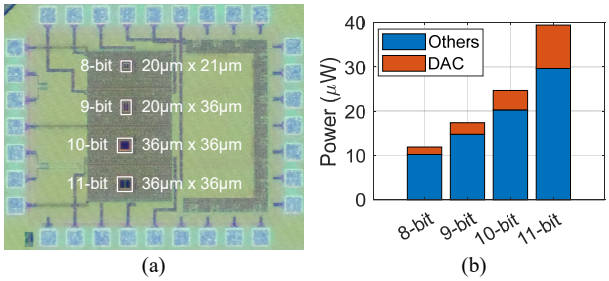


Fig. 5. (a) Die photo with all four ADCs. (b) Power breakdown.

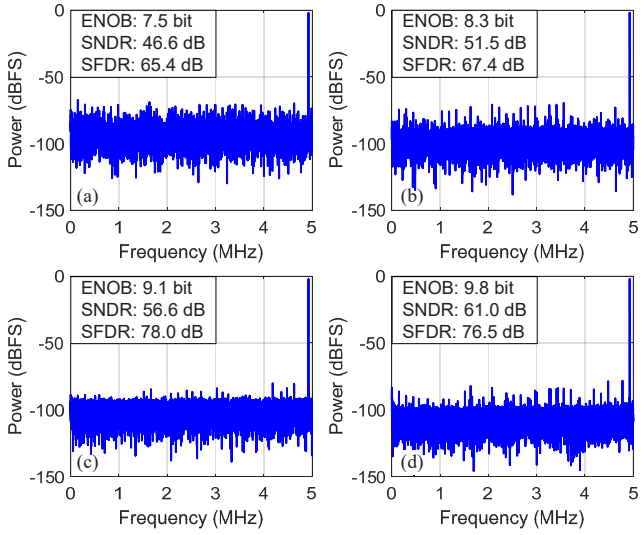


Fig. 6. Measured spectrum of (a) 8-bit, (b) 9-bit, (c) 10-bit and (d) 11-bit ADCs.

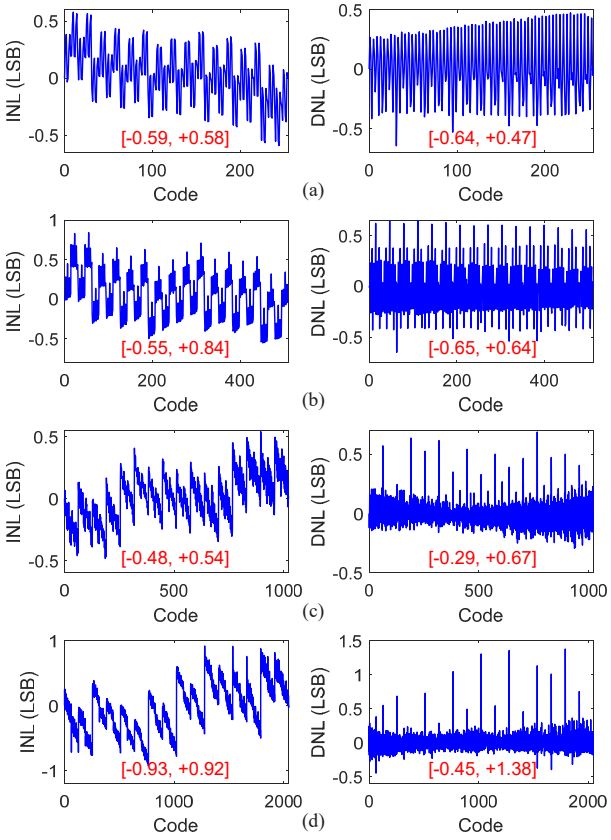
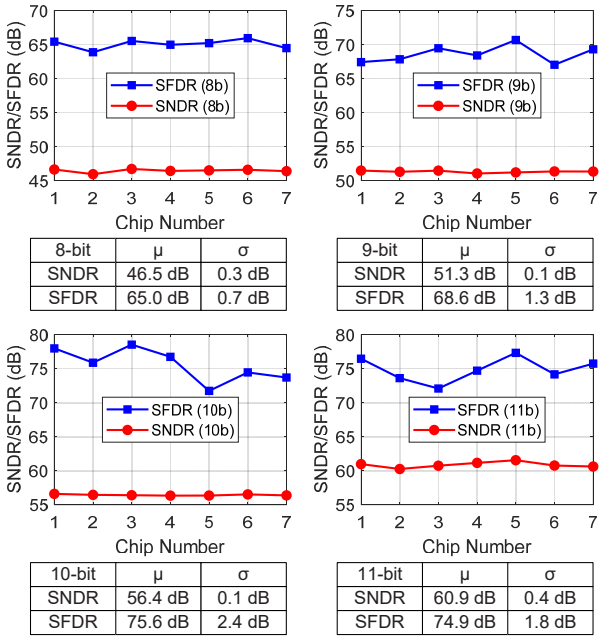


Fig. 7. Measured INL and DNL of (a) 8-bit, (b) 9-bit, (c) 10-bit and (d) 11-bit ADCs.

measured effective-number-of-bits (ENOB) of the four ADCs are 7.5, 8.3, 9.1, and 9.8 bits, and the measured spurious-free-dynamic-range (SFDR) results are 65.4 dB, 67.4 dB, 78.0 dB and 76.5 dB, respectively. Fig. 7 shows the measured integral non-linearity (INL) and differential non-linearity (DNL) performance. For the 8-bit and 9-bit designs, the systematic



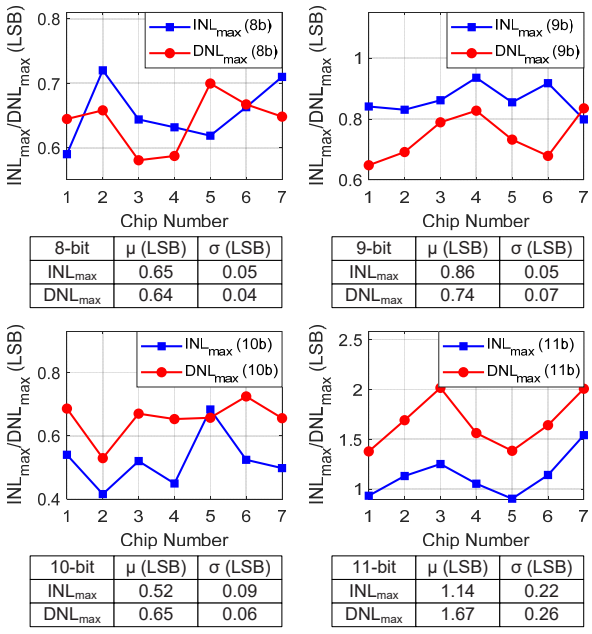
8-bit	μ	σ
SNDR	46.5 dB	0.3 dB
SFDR	65.0 dB	0.7 dB

9-bit	μ	σ
SNDR	51.3 dB	0.1 dB
SFDR	68.6 dB	1.3 dB

10-bit	μ	σ
SNDR	56.4 dB	0.1 dB
SFDR	75.6 dB	2.4 dB

11-bit	μ	σ
SNDR	60.9 dB	0.4 dB
SFDR	74.9 dB	1.8 dB

Fig. 8. Measured SNDR and SFDR of 7 samples.



8-bit	μ (LSB)	σ (LSB)
INL_{max}	0.65	0.05
DNL_{max}	0.64	0.04

9-bit	μ (LSB)	σ (LSB)
INL_{max}	0.86	0.05
DNL_{max}	0.74	0.07

10-bit	μ (LSB)	σ (LSB)
INL_{max}	0.52	0.09
DNL_{max}	0.65	0.06

11-bit	μ (LSB)	σ (LSB)
INL_{max}	1.14	0.22
DNL_{max}	1.67	0.26

Fig. 9. Measured INL and DNL of 7 samples.

errors are caused by the parasitic C_p. For the 11-bit design, the linearity is limited by the intrinsic matching of the unit-length layout. Fig. 8 and Fig. 9 show the performance spread over 7 measured chips, which indicates consistent results. Fig. 10 benchmarks this work with other designs from [1]. Thanks to the different optimization strategies for each resolution, this work features the smallest area for each design when compared to other designs with similar signal-to-noise-and-distortion-ratio (SNDR), despite using a relatively old 65 nm technology. Compared to the original 10-bit design, the area of the 8-bit and 9-bit ADC scales down by 68% and 44%, respectively. With the same area cost as [4], the 11-bit ADC achieves 4.4

TABLE II
BENCHMARK WITH OTHER WORKS

Reference	[12]	[13]	[14]	[10]	[11]	This work			
Technology (nm)	130	90	20	65	130	65			
Supply (V)	1.2	1	1	1.2	0.6	1			
F_{sample} (MHz)	50	10.24	320	100	1	10			
Resolution (bit)	10	8	10	9	9	8	9	10 [4]	11
DAC implementation	Unit-element layout	Unit-element layout	Unit-element layout	Charge injection cell	MOSCAP	Unit-length layout			
ENOB (bit)	9.18	7.77	9.2	7.5	8.48	7.5	8.3	9.1	9.8
SNDR (dB)	57.0	48.5	57.1	47.0	52.76	46.6	51.5	56.6	61.0
SFDR (dB)	65.9	61.8	78.1	62	71.01	65.4	67.4	78.0	76.5
Power (μW)	826	26.3	1520	4000	2.78	11.9	17.4	24.7	39.5
FoM_W (fJ/conv.-step)	28.5	11.8	8.1	219	7.8	6.8	5.7	4.5	4.3
Area (mm^2)	0.052	0.055	0.0012	0.02	0.046	0.00042	0.00072	0.0013	0.0013
Normalized area ($\times 10^6$)	3.08	6.79	3.00	4.73	2.72	0.10	0.17	0.31	0.31

FoM_W = Power / ($2^{ENOB} \times F_{sample}$)
Normalized area = Area / feature size^2

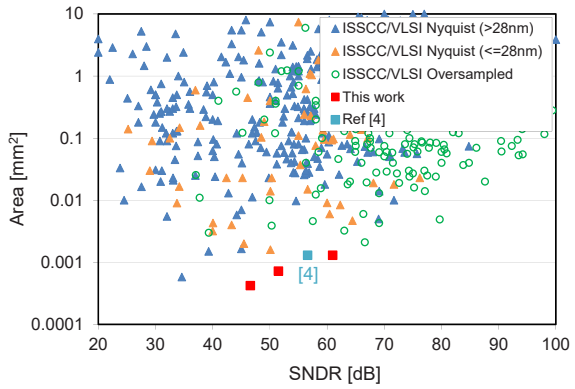


Fig. 10. ADC area benchmark, data from [1].

dB higher SNDR. Table II shows the benchmark table with other SAR ADC designs. This work shows a clear advantage in chip area when compared to other SAR ADCs implemented with different DAC structures.

V. CONCLUSION

The unit-length DAC layout facilitates substantial area reduction in SAR ADCs. This work extends its usage to SAR ADCs with 8 to 11-bit resolution. A modified unit-length layout is proposed to build compact 8-bit and 9-bit ADCs, while more metal layers are stacked and spacing is minimized to get higher capacitance density for the 11-bit ADC. Moreover, dynamic logic is used for the 8-bit SAR ADC to further reduce the digital logic area. Thanks to these techniques, the designs in this work show state-of-the-art area efficiency.

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