A 2.98pJ/conversion 0.0023mm2 Dynamic Temperature Sensor with Fully On-Chip Corrections

23.6 A 2.98pJ/conversion 0.0023mm² Dynamic Temperature Sensor with Fully On-Chip Corrections

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Nowadays, many battery-operated SoCs for IoT and environmental monitoring applications are equipped with temperature sensors. In these miniaturized systems, power and area are two critical concerns. One challenge for temperature sensors is that they are sensitive to process corners and random mismatch. Generally, a 2-point trim and systematic non-linear error removal are required, especially for resistor-based sensing front-ends with two types of resistors, whose spread is partially uncorrelated [1,2]. These corrections are done off-chip and digitally in most publications. In particular for low power sensors, they may consume more power and area than the sensor itself when integrated on-chip [3]. This work presents a resistive temperature sensor that integrates on-chip analog offset, gain and non-linearity correction techniques, while keeping state of the art power and size performance. The prototype consumes 2.98 pJ/conversion with an area of 0.0023 mm² including all the correction techniques and achieves +0.7/-0.6 °C inaccuracy.

Fig. 1 shows the architecture of the temperature sensor, which is similar to [5,6]. It consists of a dynamic resistive bridge to sense the temperature, a 9-bit asynchronous SAR ADC to read out the temperature and a power gating switch (MPG) to minimize the leakage of the system. Power switches (M1-M4) are applied to the Wheatstone bridge to realize system level correlated double sampling (controlled by a direction signal DIR) and to duty-cycle the resistive sensing front-end. Thanks to the dynamic operation, P-type polysilicon resistors (R_p) and N-type diffusion resistors (R_n) with a relatively small value of 100 kΩ can be employed with high energy efficiency [5]. On top of this, the offset, gain and non-linearity correction techniques are integrated into the ADC. The basic principle of the three corrections is to replicate the errors caused by the resistive sensing front-end in the ADC but with an opposite polarity so they will cancel out each other for the final output. To minimize area overhead, the corrections re-use the existing DAC capacitance, supplemented with several small capacitors (C_f, C_g, C_B, C_{AUX}) and extra logic. First, offset correction with a range of $\pm 2^{N-1}$ LSB is realized by pre-setting the DAC capacitors of an N-bit DAC during the tracking phase and then resetting them after the sampling moment [6] to induce a voltage step that compensates for the offset. Fine tuning capacitors (C_f) are added to further improve the offset correction accuracy to ½LSB. By adding a programmable capacitor (C_g), the ADC range can be adjusted to compensate gain errors [6]. A 3-bit C_g array is used in this work to achieve a gain correction range of 6.4% with a step size of 0.8%.

The differential output of a Wheatstone Bridge (WhB) sensor front-end can be calculated as shown in Fig. 1, where α_1 and α_2 are the temperature coefficients for R_p and R_n respectively. Since α_1 is not equal to $-\alpha_2$, V_{out} is inherently a non-linear function of ΔT. This mostly second-order distortion is the dominant non-linearity source of the entire system. While offset and gain errors are randomly distributed for each sample and thus require individual calibration, non-linearity errors are more systematic within a batch of samples and could be corrected based on batch-level characterization.

Fig. 2 shows the operation of the non-linearity correction. A fixed 5-bit C_{aux} capacitor array, controlled by a digital correction function f(x), creates a piecewise linear approximation of a second-order function. A programmable capacitor C_B is placed in series, with which the magnitude of f(x) can be adjusted. During the tracking phase, the C_{aux} capacitors are pre-set to D_{NL}, which corresponds to the non-linearity error of the sensor. After sampling, C_{aux} will be reset to zero before the regular SAR conversion starts. Due to charge redistribution of C_{aux} via C_B, the corresponding non-linearity error is subtracted from the input signal at the comparator input. Since temperature changes slowly, the previous output sample is used to predict the correction code D_{NL} of the current sample. While the overall non-linearity is mostly a systematic distortion, there can be minor variations in the distortion coefficient over process corners. By means of the programmable bridge capacitor C_B, the non-linear correction created by C_{aux} can be scaled, effectively fine tuning the distortion compensation. Also, because the non-linearity error is relatively small, with a bridge capacitor C_B, the capacitance of C_{aux} can be made larger so that the matching of the C_{aux} capacitors is improved. A piecewise linear approximation instead of a polynomial function is adopted in this work (Fig. 2 bottom right) to reduce the overhead to a minimum.

The detailed circuit implementation is shown in Fig. 3. After the offset and gain correction, the output codes for a certain temperature are consistent for all samples. In this work, the output code after offset and gain correction is at the mid-scale (256) at the middle temperature (50°C). Hence, the MSB transition coincides with the middle of the second-order distortion curve, which simplifies the logic to create the required piecewise linear function, as the function is mirrored around the MSB transition point. This can be achieved by flipping the bits dependent on the polarity of the MSB, D<8>. Likewise, the bits may need to be inverted as well dependent on the phase of the correlated double sampling technique (determined by the DIR signal). After this first step, the only required function is ax or $ax - b$, dependent on the code range. The gain factor a is implemented by selecting appropriate bits of code D, and by scaling the C_{aux} and C_B capacitors. A 4-bit linear compensation is chosen to minimize design overhead. Moreover, more precise compensation has little benefit due to quantization noise limitations (Fig. 3 bottom right). The conditional subtraction of b is done in the analog charge-sharing domain by a dedicated capacitor, which prevents the overhead of a digital subtraction. During the tracking phase, C_{aux} is controlled by the non-linearity correction function. During the rest phases, C_{aux} is reset to ground, which effectively subtracts the correction value from the sampled input voltage prior to AD conversion. The values of the C_{aux} capacitors are 4fF, 2fF, 1fF, 0.5fF and 1fF respectively, of which the last 1fF capacitor is used to create the value b near the mid code. Unit-length capacitors are used for both the main DAC and for C_{aux} to ensure the correction accuracy with small capacitors [5]. A 1-bit programmable C_B is used, whose nominal values are 5fF and 7fF. More programmability could be added to C_B to cover more process spread if desired. The extra capacitors for correction are placed on top of the ADC circuitry so that no extra area is needed for them. In total, the non-linearity correction logic requires 6 XOR, 11 NAND and 12 NOT gates.

The temperature sensor including corrections is fabricated in 65nm CMOS and occupies 0.0023 mm² (Fig. 7). The extra correction occupies an area of 170 µm², which equals to the area of only 5.5 D-flip flops in the used technology. Most circuits operate from a 0.6V supply, but the bridge switches and power gating switches are driven by 1V drivers to reduce the drain-source leakage. 15 samples are measured with a temperature range of -20 to 120 °C. The on-chip offset and gain correction are set by 2 trimming points at 50 and 100 °C. The non-linearity correction is fixed to the same setting for all samples. The sensor, including all correction functions, consumes 2.98pJ/conversion and can at least maintain this efficiency from 1kS/s to 100kS/s.

To confirm functionality, Fig. 4 shows the measured temperature error curves with various offset, gain and non-linearity correction settings. As shown in Fig. 4 (top left), a ± 4LSB offset could already result in significant temperature errors (around 2 °C). Simulations show that the offset of the sensor can be tens of LSBs, which makes it the largest error source. Mismatch also results in random gain variations but in a secondary way [6]. As can be seen from Fig. 4 (top right), a 2.2% variation could result in a temperature error of around 2.5 °C. Besides, the temperature error also depends on the non-linearity compensation setting, whose magnitude is controlled by C_B (Fig. 4 bottom). For the given batch of samples, an appropriate compensation setting helps to improve the maximum inaccuracy from approximately 2.73 °C to 0.68 °C.

Fig. 5 summarizes the measured offset, gain, non-linearity and noise characteristics. With the analog correction, the measured offset value is improved from 58-to-100 LSB to ±0.5 LSB. The gain variation is improved from 3.5% to 0.8%. As can be seen from Fig. 5, with the analog non-linearity correction, the systematic non-linearity is significantly mitigated. There are still offset and gain errors remaining since the offset and gain corrections are quantized. This sensor achieves an inaccuracy of +0.7/-0.6°C and the resulting relative inaccuracy is 0.97%. The measured RMS resolution for this sensor is around 0.47K at room temperature. Thanks to CDS, 1/f noise is mitigated. The measured output spectra are shown in Fig. 5 (bottom right). The performance of this work is summarized in Fig. 6. Compared to state-of-the-art WhB temperature sensors, it is the only low-power and compact WhB temperature sensor which integrates on-chip offset, gain and non-linearity error corrections. These features make it suitable for IoT ambient temperature monitoring applications in which low power and small size are demanded, together with moderate resolution.

Acknowledgement

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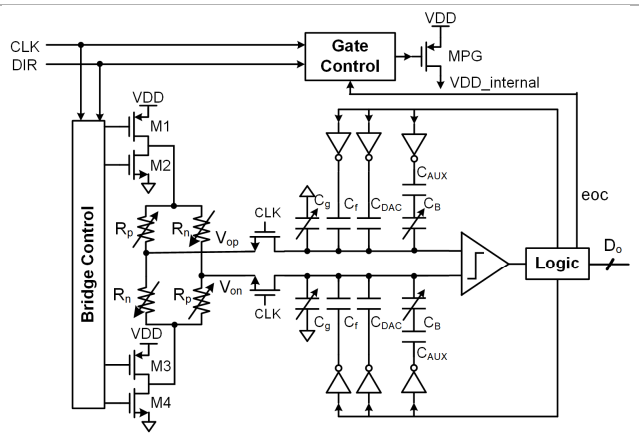
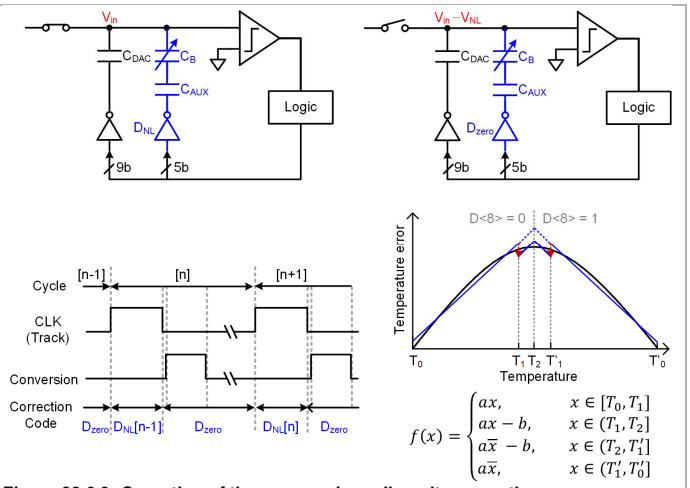


$$V_{out} = V_{op} - V_{on} = \frac{(\alpha_2 - \alpha_1)\Delta T}{2 + (\alpha_2 + \alpha_1)\Delta T} VDD \approx \frac{2(\alpha_2 - \alpha_1)\Delta T - (\alpha_2 + \alpha_1)(\alpha_2 - \alpha_1)(\Delta T)^2}{4} VDD$$

Figure 23.6.1: Architecture of the dynamic temperature sensor and output voltage as function of temperature



$$f(x) = \begin{cases} ax, & x \in [T_0, T_1] \\ ax - b, & x \in (T_1, T_2] \\ a\bar{x} - b, & x \in (T_2, T'_1] \\ a\bar{x}, & x \in (T'_1, T'_0] \end{cases}$$

Figure 23.6.2: Operation of the proposed non-linearity correction

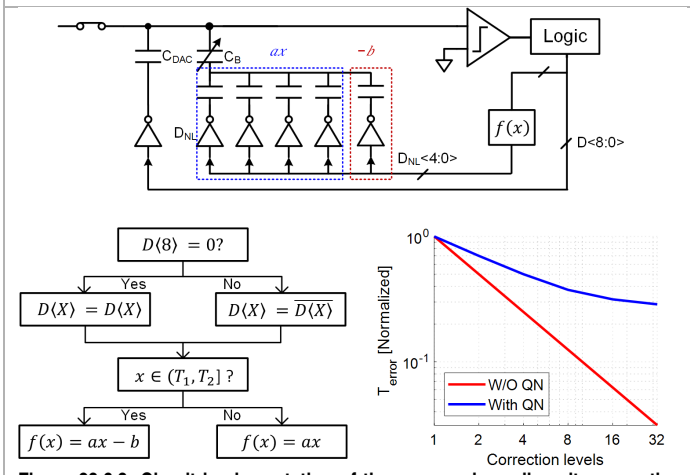


Figure 23.6.3: Circuit implementation of the proposed non-linearity correction. Circuit implementation of the non-linearity correction

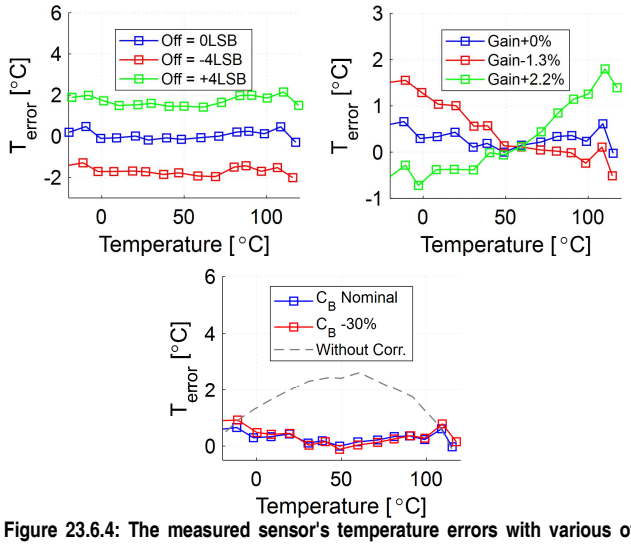


Figure 23.6.4: The measured sensor's temperature errors with various offset, gain and non-linearity correction settings

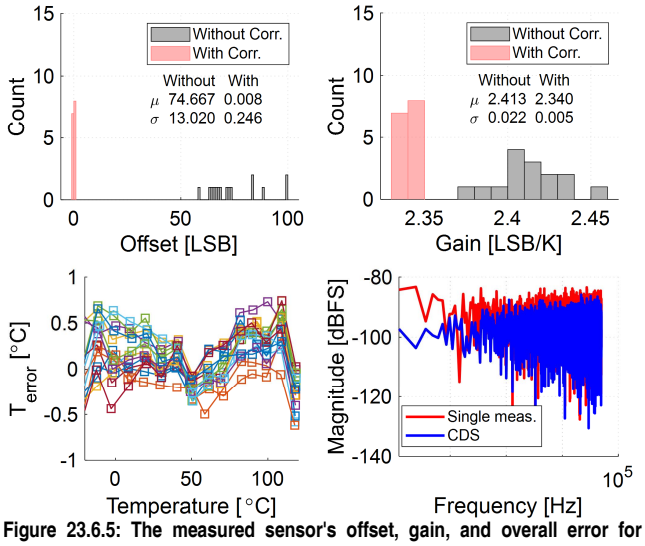


Figure 23.6.5: The measured sensor's offset, gain, and overall error for 15 samples, and noise characteristics

	[1]	[2]	[3]	[4]	[5]	[6]	This work
Technology [nm]	180	180	65	65	65	65	65
Area [mm²]	0.43	0.11	1.37	0.044	0.0017	0.0018	**0.0023**
Supply voltage [V]	1.5	1.8	0.75	0.8	1/0.6	1/0.6	1/0.6
Temp. range [°C]	-45 to 125	-55 to 125	0 to 90	-45 to 85	-20 to 120	-20 to 120	-20 to 120
Inaccuracy [K] (Trimming points)	±0.4 (2[a])	±0.1 (2[a])	±0.2 (4[a])	+1.6/-1 (2[b])	1.2 (2[b])	0.6/-0.6 (2[b])**	0.7/-0.6 (2[b])
Resolution [K]	0.01	0.15m	1.75m	0.121	0.53	0.47	0.47
Power [µW]	64.5	55	15*	47.2	0.108	0.137	0.149
Conv. time [s]	100µ	8m	100m	10µ	20.6µ	20µ	20µ
Conv. energy [pJ]	6450	440000	1500000	472	2.18	2.74	2.98
FoM [pJ·K²]	0.65	0.01	4.6	6.9	0.61	0.60	0.66
On-chip corr.	Trimming resistors	Trimming resistors	Digital polynomial generator	None	None	Offset, gain	Offset, gain, non-linearity
Off-chip corr.							
1st order fit	Y	Y	Not available	Y	Y	N	**N**
Decimation filter	Y	Y	Not available	N	N	N	**N**
Polynomial engine	Y	Y	N	Y	Y	Y	**N**

[a]: 3σ inaccuracy [b]: Maximum inaccuracy * Excluding the on-chip digital blocks. **Result without off-chip 1st order fit.

Figure 23.6.6: Summary of measurement results and comparison with state-of-the-art WhB temperature sensors

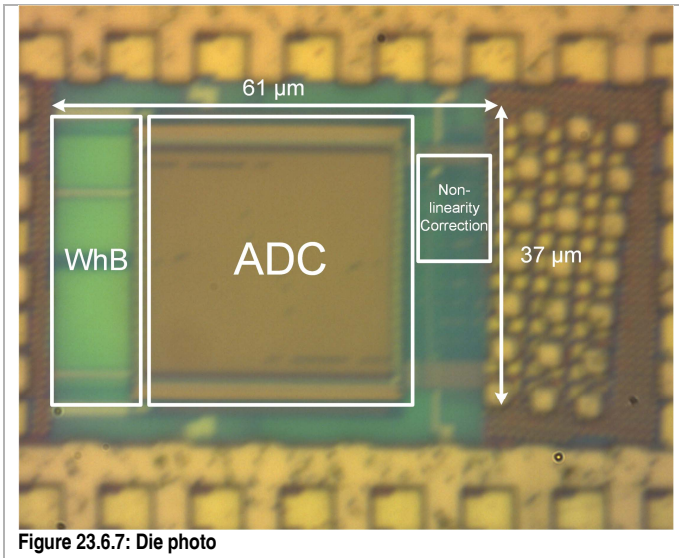


Figure 23.6.7: Die photo