A 2.2 fJ/Conversion-Step 9.74-ENOB 10 MS/s SAR ADC With 1.5×Input Range

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***Abstract*—This brief presents a 10.5-bit 10 MS/s successive-approximation-register (SAR) analog-to-digital converter (ADC) with 1.5× input range (IR). By pre-setting and resetting the most significant bit (MSB) of the digital-to-analog converter (DAC) to shift the input signal accordingly, the input range of the ADC is enhanced by a factor of 1.5. This effectively relaxes the noise requirement and thus improves the power efficiency of the ADC. The prototype implemented in 65-nm CMOS technology achieves a signal-to-noise-and-distortion ratio (SNDR) of 60.37 dB and a spurious-free dynamic range (SFDR) of 82.2 dB. It consumes 18.65 μW at 10 MS/s with a 0.8V supply and only occupies an area of 0.0013 mm^2. The resulting Walden figure of merit (FoM$_W$) is 2.2 fJ/conversion-step.**

***Index Terms*—Analog-to-digital converter (ADC), area efficiency, energy efficiency, input range, successive approximation register (SAR).**

I. Introduction

In THE last decades, successive-approximation-register (SAR) analog-to-digital converters (ADCs) have been widely used in a large range of applications (e.g., Internet of Things) for their power-efficiency [1], [2]. Many techniques, for example, various digital-to-analog converter (DAC) switching schemes, comparator topologies, noise cancellation techniques and so on, have been proposed to further improve the power efficiency of SAR ADCs [3]–[5]. Extending the equivalent input range of the ADC is one of the options. From one perspective, with the same supply voltage and signal-to-noise ratio (SNR) requirement, the absolute noise constraint of the circuits is effectively relaxed with a larger input signal. From another perspective, for a required input signal range, the used supply voltage can be lowered to reach the same SNR and thus the power consumption of the ADC can be reduced, which often scales with VDD^2. This is also convenient for applications with limited supply voltages, for example, an environment monitoring system powered by photo diodes, where the usable supply voltage is below 0.6V. For these applications, techniques which can extend the input range can be very helpful.

To enhance the equivalent input range of an ADC, [6] proposes a most significant bit (MSB) prediction technique. The MSB is obtained by prediction and the used reference voltage can be half for the less significant bits (LSBs) with the same input signal. Multi-bit prediction and redundancy are used to guarantee the prediction accuracy. Extra capacitors are introduced for prediction. The simulated Walden figure of merit (FoM$_W$) is 9.5 fJ/conversion-step. Reference [7] proposes to use two identical sub-ADCs with different input ranges. Depending on the MSB decision, one of the two sub-ADCs will be enabled and thus the input range of the ADC increases by a factor of 2. [7] is very energy efficient and achieves a FoM$_W$ of 0.44 fJ/conversion-step. However, redundancy is required to guarantee a sufficient overlap range for the sub-ADCs. Besides, to guarantee the linearity of the ADC, foreground calibration is required to calibrate the mismatch between the sub-ADCs

Different from the above approaches, this brief proposes to use an MSB compensation technique which enhances the input range of the ADC by a factor of 1.5 and increases the ideal resolution by 0.5-bit with negligible area cost and limited power cost. A 10 MS/s SAR ADC is implemented in 65-nm CMOS technology to verify the idea, which achieves 9.74 effective number of bits (ENOB) with a FoM$_W$ of 2.2 fJ/conversion-step and occupies an area of 0.0013 mm^2.

The rest of this brief is organized as follows. Section II introduces the proposed MSB compensation technique. Section III describes the circuit implementation details. Section IV presents the measured results and summarizes the performance of this brief. Finally, Section V draws the conclusion.

II. Proposed MSB Compensation Technique

A. Principle and Operation

Fig. 1 shows a behavioral model of the SAR conversion with the proposed MSB compensation technique. The basic principle is to inject a negative input to partly cancel the input signal swing and then add it back in the digital domain. This compensation can be implemented using the already available MSB capacitors inside the DAC.

Assume that the ideal input range is $[-V_{ref}, V_{ref}]$ for a SAR ADC with a differential input. As conceptually shown in Fig. 2, the MSB compensation technique will shift positive

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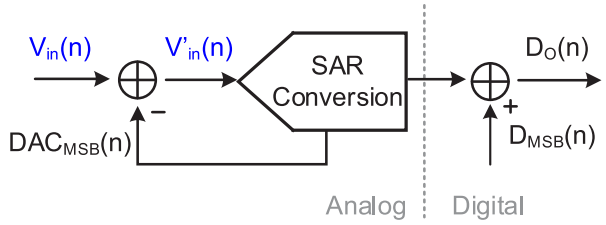

Fig. 1. Behavioral model of SAR conversion with MSB compensation.

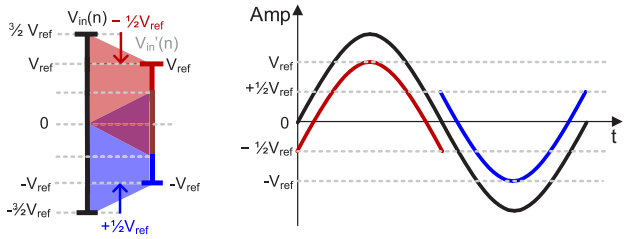

Fig. 2. Equivalent input signals before and after MSB compensation.

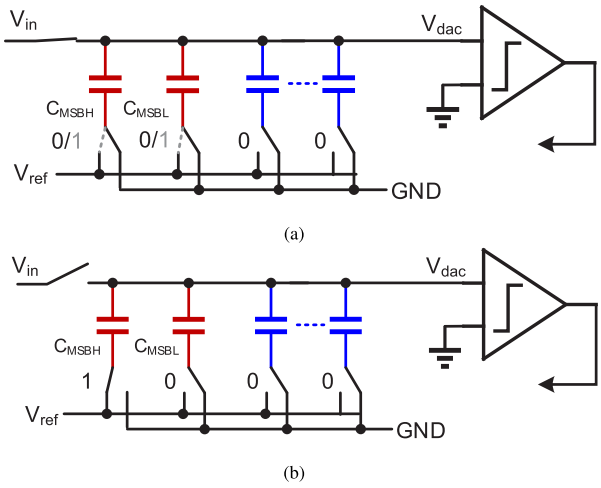

Fig. 3. DAC operation during pre-set phase (a) and reset phase (b).

input signals V_{in} downwards by $\frac{1}{2}\ V_{ref}$, and will shift negative input signals upwards by $\frac{1}{2}\ V_{ref}$ prior to the actual SAR conversion. As a result, the input range is extended to $[-\frac{3}{2}V_{ref}, +\frac{3}{2}V_{ref}]$.

The circuit level operation of the proposed MSB compensation technique is shown in Fig. 3. A single-ended diagram is shown for simplicity. The MSB capacitor is split in two capacitors C_{MSBH} and C_{MSBL}. An additional pre-set phase will be inserted before the sample moment and an additional reset phase will be inserted after the sampling moment. During the pre-set phase, an additional comparison is performed to detect the polarity of V_{in} and the MSBs of the DAC are pre-set. For positive V_{in}, both MSB capacitors will be pre-set to 1. During the reset phase, the bottom plate of C_{MSBH} will be reset to 1 and the bottom plate of C_{MSBL} will be reset to 0. This operation will cause a $-\frac{1}{2}V_{ref}$ voltage shift for V_{dac}. Then, a normal SAR conversion starts.

Correspondingly, for negative V_{in}, the MSB capacitors are pre-set to 0 and then the reset creates a $\frac{1}{2}V_{ref}$ shift for V_{dac}. By pre-setting and resetting the MSB capacitors, the input

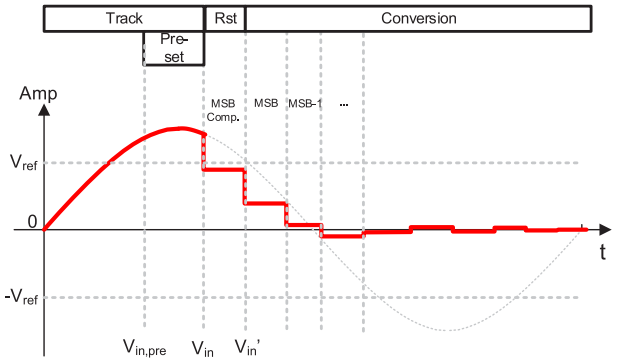

Fig. 4. Signal behavior at the comparator input.

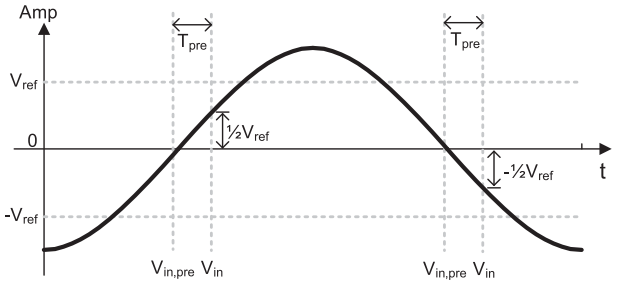

Fig. 5. Critical cases where compensation errors may occur.

range of the ADC is thus enhanced by a factor of 1.5. Fig. 4 shows an example of the signal at the comparator input when $V_{in,pre} > 0$. After the MSB compensation, $V'_{in} = V_{in} - \frac{1}{2}V_{ref}$, and the regular conversion is performed, starting with the MSB decision.

B. Pre-Comparison Timing Requirements

Because the MSB compensation step is decided based on the polarity of $V_{in,pre}$ prior to the sampling moment, V_{in} and $V_{in,pre}$ may have different polarities, causing an incorrect compensation step. When V_{in} is in the range of $[-\frac{1}{2}V_{ref}, \frac{1}{2}V_{ref}]$, the converted signal V'_{in} is always in the conversion range regardless of being shifted up or down. In this case, it does not matter whether the MSB compensation is correct.

For $V_{in} > \frac{1}{2}V_{ref}$ or $< -\frac{1}{2}V_{ref}$, a correct compensation should be made. The most critical case happens when V_{in} is near $\frac{1}{2}V_{ref}$ (or $-\frac{1}{2}V_{ref}$). As shown in Fig. 5, when $V_{in,pre}$ is negative and V_{in} is larger than $\frac{1}{2}V_{ref}$ (or $V_{in,pre}$ is positive and V_{in} is smaller than $-\frac{1}{2}V_{ref}$), V'_{in} will overrange due to a wrong compensation. The tolerable pre-set timing margin T_{pre} can be calculated according to:

$$\frac{1}{2}V_{ref} = \frac{3}{2}V_{ref}sin\left(2\pi f_{in}T_{pre}\right) \tag{1}$$

Since $f_{in} < \frac{1}{2}f_s$ and $f_s = \frac{1}{T_s}$, it can be derived from (1) that:

$$T_{pre} \leq 11\%T_s \tag{2}$$

The duration of T_{pre} should be smaller than 11% of one sampling period to ensure an accurate compensation. It should be noted that a short duration of T_{pre} may imply a penalty in the required driving strength.

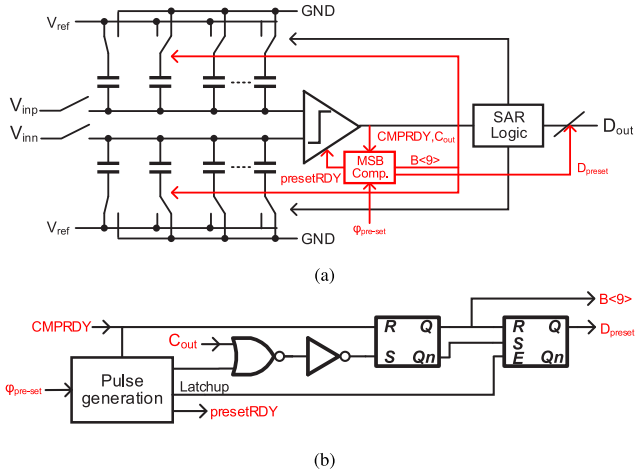

Fig. 6. ADC architecture (a) and MSB compensation logic (b).

Overall, by applying the proposed MSB compensation technique, the ideal resolution of a SAR ADC is improved to N+0.5 bit using a N-bit hardware, which makes it area efficient. Also, the ideal input range of the ADC is enhanced to $\pm 1.5V_{ref}$, which effectively relaxes the noise requirement and is especially helpful for cases with a limited supply.

III. Circuit Implementation

To verify this idea, a 10(+0.5) bit 10 MS/s SAR ADC is implemented as an example. Fig. 6(a) shows the architecture of the ADC, which consists of a sample and hold circuit, a comparator, a DAC, SAR logic and the new-added MSB compensation logic. The input switches are NMOS transistors driven by a clock boosting circuit [8] for linearity requirements. The used comparator is a fully dynamic two-stage comparator composed of a pre-amplifier and a latch [9]. Conventional self-synchronized SAR logic is used [10]. A 10-bit charge-redistribution DAC is used with custom designed unit-length finger capacitors [11] to minimize chip area. However, the proposed method could be applied equally well to other DAC implementations. The total sampling capacitance is around 250 fF, which results in 64 dB SNR for a normal SAR ADC with a supply voltage of 0.8V and 67 dB SNR for this design with 1.5× input range.

Fig. 8 shows the DAC capacitor implementation, which is the same as [11]. Each capacitor consists of two sub cells (C_p and C_n). The effective DAC capacitance (C_{eff}) is equal to the difference between the two sub cells which are almost equal except for a small $2 \times C_\Delta$. Thus, a very small unit capacitance can be achieved with decent matching [11]. Moreover, binary scaled capacitors can be made by changing Δ in a binary scaled fashion, which is much more area efficient compared to placing identical units in parallel to achieve binary scaling. The DAC capacitors are placed on top metals (Metal 6 and 7) and are vertically connected to the DAC drivers underneath. The rest of the ADC is also placed underneath to minimize chip area.

The detailed implementation of the MSB compensation logic is shown in Fig. 6(b). During the pre-set phase ($\varphi_{pre-set}$),

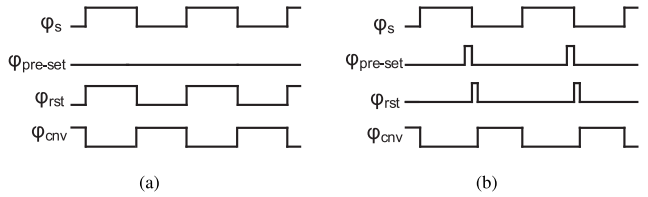

Fig. 7. Timing diagrams: 'IR×1' mode (a) and 'IR×1.5' mode (b).

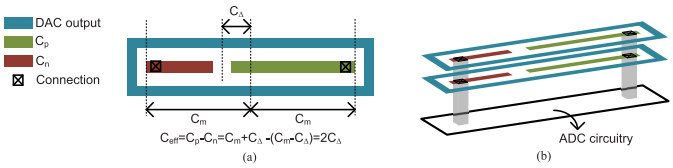

Fig. 8. DAC capacitor implementation: top view (a), and 3D view (b).

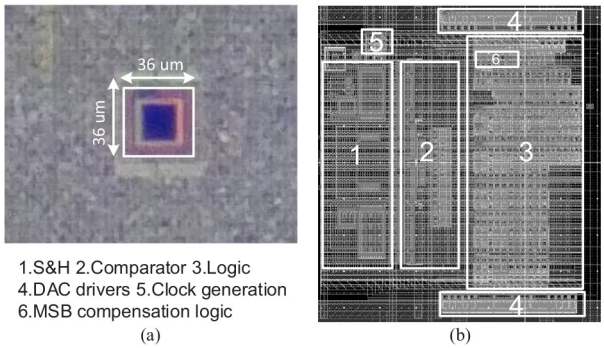

Fig. 9. Die micrograph (a) and layout-view (b).

the dynamic comparator of the SAR ADC will be enabled. After the comparison, a comparison ready signal (CMPRDY) and a comparator output signal (C_{out}) will be generated. Depending on the comparator output, a DAC control signal $B\langle 9\rangle$ will be generated to control the switching of the MSBs of the DAC, a pre-set ready signal (presetRDY) will be generated to disable the dynamic comparator and a digital output signal D_{preset} will be generated.

Fig. 7 shows an overview of the timing diagram. The ADC can operate in two input range modes: a conventional 'IR×1' mode (Normal SAR mode) and an 'IR×1.5' (SAR with 1.5× input range) mode. When working in 'IR×1' mode, the DAC will reset (φ_{rst}) during the sampling phase (φ_s) and after that the SAR conversion starts (φ_{cnv}). When working in 'IR×1.5' mode, the MSB of the DAC will be pre-set in the pre-set phase ($\varphi_{pre-set}$) and then be reset in an extra reset phase (φ_{rst}). After that, a normal SAR conversion starts (φ_{cnv}).

IV. Measured Results

The prototype fabricated in 65-nm CMOS is shown in Fig. 9. It occupies an area of 0.0013 mm^2. The implemented ADC consumes 18.65 μW at 10 MS/s with a 0.8-V supply voltage.

Fig. 10 shows the measured spectrum with an input frequency of 4.901 MHz. When working as a normal SAR ADC, this design achieves 56.8 dB signal-to-noise-and-distortion ratio (SNDR), 82.9 dB spurious-free dynamic range

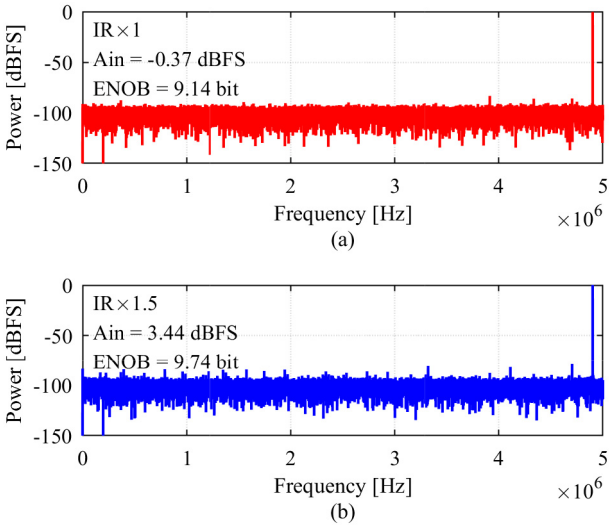

Fig. 10. Measured spectrum with an input frequency of 4.901 MHz in 'IR×1' mode (a) and 'IR×1.5' mode (b).

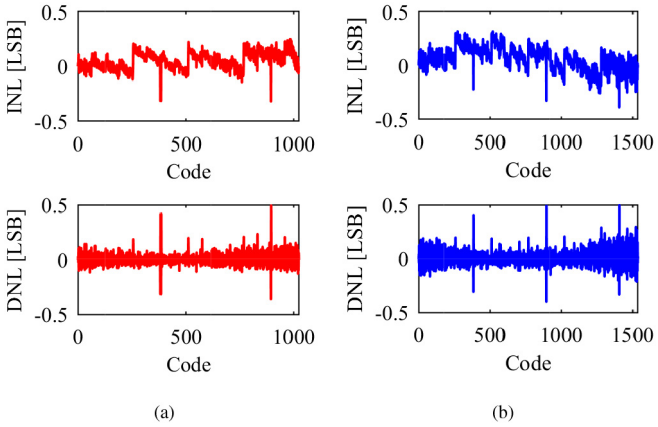

Fig. 11. Measured INL and DNL in 'IR×1' mode (a) and 'IR×1.5' mode (b).

(SFDR) and 9.14-bit ENOB with a maximum input amplitude of −0.37 dBFS. When working in 'IR×1.5' mode, the maximum input amplitude is improved to 3.44 dBFS while the noise level remains the same. Thus the SNDR is improved to 60.37 dB and the ENOB is improved to 9.74-bit. The measured SFDR is 82.2 dB. The resulting Schreier FoM and Walden FoM are 174.7 dB and 2.2 fJ/conversion-step, respectively.

The measured integrated non-linearity (INL) and differential non-linearity (DNL) of the ADC are shown in Fig. 11. The INL/DNL measurement is done by a histogram test with 1 million points. The measured maximum INL and DNL for this brief in 'IR×1' mode are 0.32LSB and 0.49LSB, respectively. In 'IR×1.5' mode, the measured maximum INL is 0.39LSB and the measured maximum DNL is 0.50LSB, which is similar to 'IR×1' mode.

Fig. 12 shows the measured SNDR versus the input amplitude. By applying the proposed MSB compensation technique, the maximum input of the ADC is improved by around 3 dB and the ADC achieves a dynamic range of 60.64 dB in 'IR×1.5' mode.

TABLE I
POWER DISSIPATION AND BREAKDOWN AT 10 MS/S

	'IR×1'	'IR×1.5'
Comparator	8.8μW	9.68μW
Logic	3.75μW	4.33μW
DAC	2.6μW	3.37μW
T&H	0.92μW	0.92μW
Clock	0.19μW	0.32μW
Total	16.3μW	18.6μW

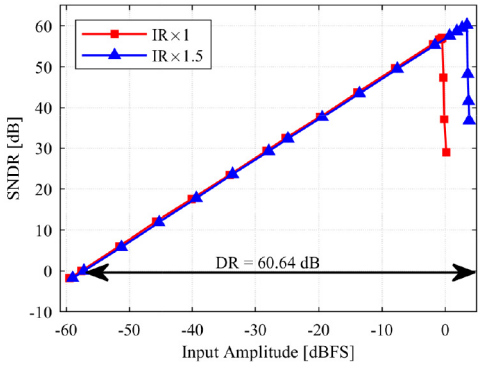

Fig. 12. Measured SNDR versus input amplitudes.

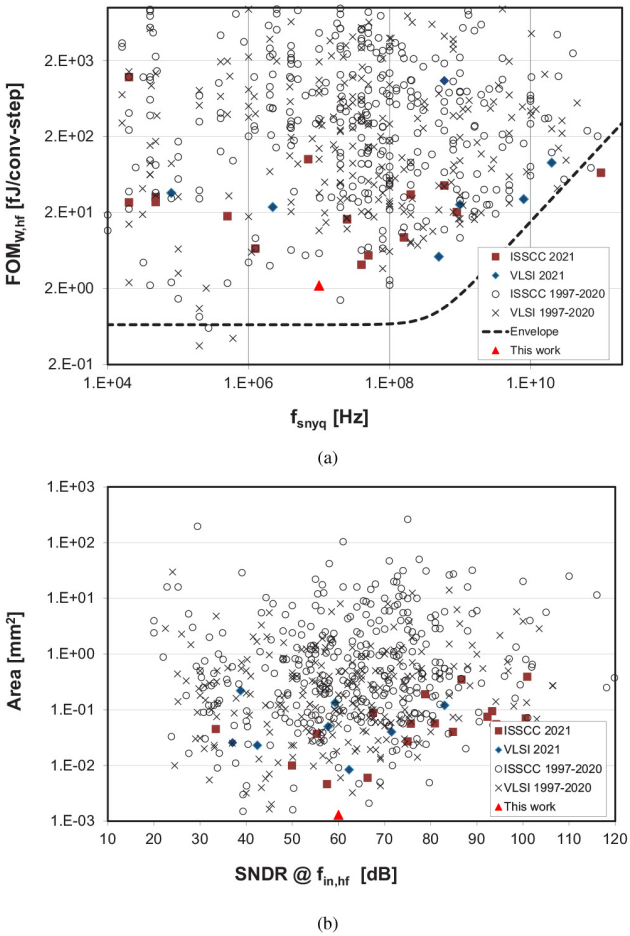

Fig. 13. Efficiency benchmark (a) and area benchmark (b), data from [1].

Table I shows the post-layout simulated power dissipation and breakdown of the ADC working in different modes. In measurements, this ADC consumes 18.65 μW at 10 MS/s in

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[6][3]	[7]	[9]	[11]	[12]	[13]	[14]	This work	
Technology [nm]	180	90	65	65	65	20	130	65	
Area [mm^2]	-	0.035	0.026	0.0013	0.046	0.0012	0.052	0.0013	
Supply voltage [V]	0.8	0.3	1	1	1.2	1	1.2	0.8	
Resolution [bit]	10	11	10	10	8	10	10	10	
Sample rate [MS/s]	2	0.6	1	10	90	320	50	10	
Bandwidth [MHz]	1	0.3	0.5	5	11	160	25	5	
Ideal input swing [V_{ref}]	±2	±2	±1	±1	±1	±1	±1	±1	±1.5
Power [μW]	16.07	0.187	1.9	24	806	1520	826	16.28	18.65
ENOB [bit]	9.72	9.46	8.75	9.18	10	9.2	9.18	9.14	9.74
SFDR [dB]	69.35	72.0	-	75.7	72.46	78.1	65.9	82.9	82.2
FoM$_W$ [fJ/conv-step] [1]	9.53	0.44	4.42	4.1	35.8	8.1	28.5	2.9	2.2
FOM$_S$[dB][2]	168.2	180.8	168.6	170.2	163.3	167.4	161.8	167.7	174.7

[1] $FOM_W = Power/(2^{ENOB} \times 2 \times BW)$
[2] $FOM_S = SNDR + 10 \times \log 10(BW/Power)$
[3] Simulated results

'IR×1.5' mode, which is an increase of 14% compared to the regular 'IR×1' mode. The additional logic only occupies an area of 13 μm^2, which is negligible and can easily fit into the existing design. No extra capacitors are needed.

Table II summarizes the performance of this brief and compares it with state-of-the-art designs. Compared to advanced designs [6], [7] with $\pm 2V_{ref}$ input range, only a few logic gates are needed for this brief and thus this brief is much more area efficient. The supply voltage of this brief could be further reduced to save power. Compared to SAR ADCs with similar SNDR and bandwidth (Fig. 13), this brief achieves state-of-the-art energy efficiency and area efficiency.

V. CONCLUSION

This brief presents a 10(+0.5) bit 10 MS/s SAR ADC in 65-nm CMOS technology. With the proposed MSB compensation technique, the input range of the ADC is improved by a factor of 1.5 while the resolution is improved by 0.5-bit with negligible area cost and 14% power cost. The prototype consumes 18.65 μW at 10 MS/s from a 0.8-V supply voltage and occupies an area of 0.0013 mm^2. The achieved SNDR, SFDR, ENOB are 60.37 dB, 82.2 dB and 9.74-bit, respectively. This results in a FoM$_W$ of 2.2 fJ/conversion-step, which is competitive among state-of-the-art designs. It is also area efficient, which makes it suitable for low-power low-cost applications.

REFERENCES

[1] B. Murmann. "ADC Performance Survey 1997-2021." [Online]. Available: http://web.stanford.edu/ murmann/adcsurvey.html (Accessed: May 1, 2022).

[2] P. Harpe, H. Li, and Y. Shen, "Low-power SAR ADCs: Trends, examples and future," in *Proc. IEEE 45th Eur. Solid State Circuits Conf. (ESSCIRC)*, 2019, pp. 25–28.

[3] C. Liu, S. Chang, G. Huang, Y. Lin, and C. Huang, "A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18μm CMOS," in *Proc. Symp. VLSI Circuits*, 2010, pp. 241–242.

[4] H. S. Bindra, C. E. Lokin, A. Annema, and B. Nauta, "A 30fJ/comparison dynamic bias comparator," in *Proc. 43rd IEEE Eur. Solid State Circuits Conf.*, 2017, pp. 71–74.

[5] J. Liu, X. Tang, W. Zhao, L. Shen, and N. Sun, "A 13-bit 0.005-mm2 40-MS/s SAR ADC with kT/C noise cancellation," *IEEE J. Solid-State Circuits*, vol. 55, no. 12, pp. 3260–3270, Dec. 2020.

[6] Z. Fu and K.-P. Pun, "An SAR ADC switching scheme with MSB prediction for a wide input range and reduced reference voltage," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 12, pp. 2863–2872, Dec. 2018.

[7] S.-E. Hsieh and C.-C. Hsieh, "A 0.44-fJ/conversion-step 11-Bit 600-kS/s SAR ADC with semi-resting DAC," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2595–2603, Sep. 2018.

[8] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, Mar. 1995.

[9] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9μW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2008, pp. 244–610.

[10] S. M. Chen and R. W. Brodersen, "A 6-bit 600-MS/s 5.3-mW asynchronous ADC in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2669–2680, Dec. 2006.

[11] P. Harpe, "A 0.0013*mm*^{2}ă10b 10MS/s SAR ADC with a 0.0048*mm*^{2} 42dB-rejection passive FIR filter,"ăin *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2018, pp. 1–8.

[12] J. Fredenburg and M. Flynn, "A 90MS/s 11MHz bandwidth 62dB SNDR noise-shaping SAR ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2012, pp. 468–470.

[13] C. Liu, "A 10-bit 320-MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20-nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2014, pp. 77–80.

[14] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR IR1RE," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.