A 7.3-μ W 13-ENOB 98-dB SFDR Noise-Shaping SAR ADC With Duty-Cycled Amplifier and Mismatch Error Shaping

A 7.3μW 13-ENOB 98dB-SFDR Noise-Shaping SAR ADC With Duty-Cycled Amplifier and Mismatch Error Shaping

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***Abstract*—This paper presents a second-order noise-shaping SAR ADC that employs a duty-cycled amplifier and digital-predicted mismatch error shaping. The loop filter is composed of an active amplifier and two cascaded passive integrators to provide a theoretical 30 dB in-band noise attenuation. The amplifier achieves 18× gain in a power-efficient way thanks to its inverter-based topology and duty-cycled operation. The capacitor mismatch in the DAC array is mitigated by first-order mismatch error shaping (MES). A two-level digital prediction scheme is adopted with MES to avoid input range loss. Fabricated in 65 nm CMOS technology, the prototype achieves 80 dB peak SNDR and 98 dB peak SFDR in a 31.25 kHz bandwidth with 16× OSR, leading to a Schreier FoM of 176.3 dB and a Walden FoM of 14.3 fJ/converstion-step.**

***Index Terms*—Noise-shaping SAR ADC, loop filter, duty-cycled amplifier, mismatch error shaping, high linearity.**

I. Introduction

NOISE-SHAPING Successive-Approximation-Register (NS-SAR) Analog-to-Digital Converters (ADC) have emerged in recent years as a promising candidate to realize low-power and high-resolution ADCs. These ADCs are for instance suitable for low-speed IoT sensor interfaces or recording of electrophysiological signals. As a hybrid architecture of SAR ADC and $\Sigma\Delta$ ADC, the NS-SAR ADC inherits the merits from the individual architectures and therefore, it draws great attention from circuit designers and continuously advances the frontier of ADC performance in recent literature [1], [2].

A typical NS-SAR ADC diagram is shown in Fig. 1. Compared to a conventional SAR ADC, a loop filter is inserted to integrate the residue voltage V_{RES} which is directly obtained at the end of the SAR conversion. Compared to a typical $\Sigma\Delta$ ADC with SAR quantizer, only one digital-to-analog converter (DAC) is present in the loop, which serves both as a reference voltage generator during the SAR binary-search process and as a feedback DAC in the noise-shaping loop. With a single feedback DAC, the possible loop filter implementations are

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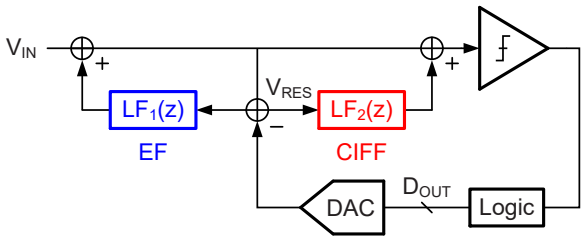

Fig. 1. Block diagram of an NS-SAR ADC with EF and CIFF filter options.

the error-feedback (EF) topology, and the cascade-integrator-feedforward (CIFF) topology, shown as $LF_1(z)$ and $LF_2(z)$ in Fig. 1, respectively, while a cascade-integrator-feedback (CIFB) topology is not feasible. The signal transfer function (STF) of an NS-SAR ADC is 1, and the noise transfer function (NTF) is $1 - LF_1(z)$ or $1/[1 + LF_2(z)]$, dependent on the selected filter topology. By implementing an FIR integrator as LF_1 or an IIR integrator as LF_2, a similar NTF can be obtained from both EF and CIFF topologies. Therefore, this work only focuses on the CIFF implementation without losing generality.

Despite the advantages brought from the hybridization of different ADC architectures, it also poses several challenges to design a high-performance NS-SAR ADC. These challenges are summarized below from three aspects:

1) The quantization noise and comparator noise in an NS-SAR ADC are high-pass filtered thanks to the loop filter. Therefore, the first challenge is to design a proper NTF to achieve sufficient in-band noise reduction at the system level.
2) Compared to a SAR ADC with only oversampling [3], an NS-SAR ADC introduces additional noise and power overhead from its loop filter circuitry. Thus, the second challenge is to design a low-noise and energy-efficient integrator at the circuit level.
3) Since a SAR ADC has typically 8 to 12 bits resolution, this multi-bit quantizer leads to improved stability and reduced sensitivity to integrator nonlinearity. But its DAC mismatch errors limit the overall linearity. So the third challenge is to mitigate the DAC mismatch to achieve high linearity at the algorithm level.

This paper, as an extension of [4], addresses these three challenges by analyzing different system and circuit level choices in terms of their power efficiency. After that, a

second-order NS-SAR ADC with a duty-cycled amplifier and mismatch error shaping (MES) is proposed. The paper is organized as follows. Section II provides a benchmark of loop filters in prior NS-SAR ADCs and shows the overall ADC architecture of this design. Section III presents the proposed duty-cycled amplifier together with a duty-cycled bias circuit. Section IV describes the two-level digital-predicted MES. Section V shows the measurement results and Section VI draws conclusions.

II. System Overview

This section first reviews three common loop filter structures known from literature, selects the most appropriate one, and then discusses the selection of the filter coefficients. Finally, the detailed system operation steps will be presented.

A. Filter Structures in Prior NS-SAR ADCs

Despite the rapid development in the NS-SAR ADC field in recent years, a comprehensive benchmark of the power efficiency of different NS-SAR ADCs is nontrivial due to the numerous parameters involved in an ADC design. Fortunately, the benchmark work can be simplified with reasonable assumptions as follows. In a properly designed NS-SAR ADC, quantization noise and comparator noise are both high-pass shaped and become non-dominant in the system, while the sampling kT/C noise and the integrator noise in the loop filter are only oversampled and occupy most of the noise budget. Since the DAC is an original block already existing in a SAR ADC, the key to design a power-efficient NS-SAR ADC is to select an appropriate loop filter with high power efficiency. Therefore, this section aims to provide a comparison of the loop filters in prior NS-SAR ADC designs in terms of their power efficiency.

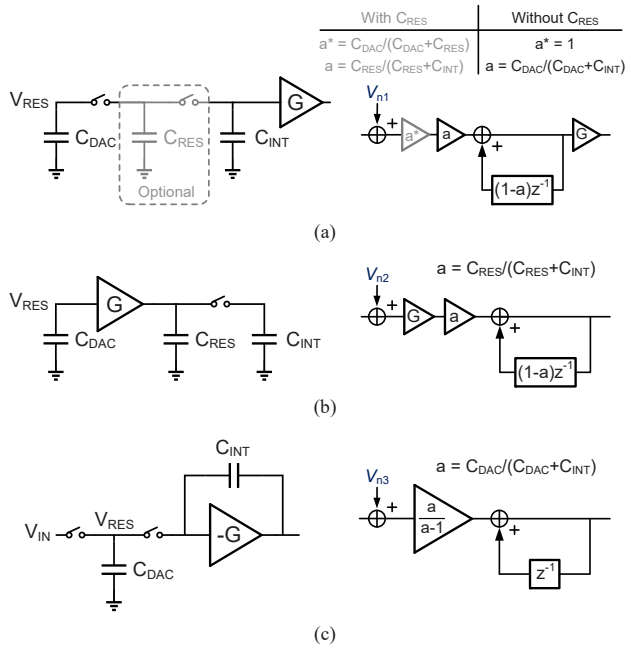

Fig. 2. Different loop filter structures in NS-SAR ADCs: (a) passive integrator, (b) active integrator with open-loop amplifier and (c) active integrator with closed-loop amplifier.

The figure-of-merit (FoM) definition from [5] is used to benchmark different loop filters. This FoM is defined as the product of circuit energy consumption and its input-referred noise power, namely,

$$\text{FoM} = (\text{Energy}) \cdot (\text{Noise power}), \tag{1}$$

where 'Energy' denotes the total energy consumption from the DAC and the loop filter (E_{DAC} + E_{LF}) and 'Noise power' includes also the noise from both DAC sampling and loop filter ($\overline{V_{n,\text{DAC}}^2}$ + $\overline{V_{n,\text{LF}}^2}$). A lower FoM value indicates a lower energy consumption with the same noise performance, which also implies an overall lower power consumption for the whole converter. The loop filters in prior NS-SAR ADCs can be categorized into three different types according to which residue integration strategy is used, as shown in Fig. 2. The circuits in Fig. 2 are single-ended, but the calculation afterwards assumes a differential implementation.

First, passive charge-sharing among multiple capacitors can be utilized for residue integration, as shown in Fig. 2(a). The residue voltage V_{RES} on C_{DAC} can be directly charge-shared with the integration capacitor C_{INT} [6] or via an intermediate C_{RES} [7]. A gain function usually follows the passive integrators using capacitor stacking [6] or using a multiple-input comparator [7]. This passive loop filter (PLF) is simple and robust, but it suffers from the extra kT/C noise introduced by each sampling process. This excess noise power $\overline{V_{n1}^2}$, when referred to the loop filter input, is [6]:

$$\overline{V_{n1}^2} = \frac{\lambda kT}{C_{\text{DAC}}}. \tag{2}$$

where λ is a coefficient dependent on the specific loop filter realization. It can range from 1.6 up to 17.7 for a differential loop filter [6]. The total noise power in (1) is thus $(2+\lambda)kT/C_{\text{DAC}}$ including the sampling kT/C noise whose power is $2kT/C_{\text{DAC}}$ due to the differential implementation. The PLF itself consumes zero power (ignoring the digital control power), so the FoM of the PLF can be expressed as the product of the DAC energy consumption and total noise power, namely,

$$\text{FoM}_{\text{PLF}} = mC_{\text{DAC}}V_{\text{REF}}^2 \cdot \frac{(2+\lambda)kT}{C_{\text{DAC}}}. \tag{3}$$

where m is a parameter determined by the DAC switching scheme. The value of m varies typically from 0.17 (V_{cm}-based switching scheme) to 0.67 (conventional switching scheme) for a 10-bit SAR resolution [8]. When a multiple-input comparator is used to implement a relative gain function, the comparator power efficiency also becomes lower. But this penalty is not included here for simplicity.

Second, an open-loop amplifier (OLA) can be inserted in front of the passive integrator to attenuate the passive integrator noise [9]. In this loop filter structure, the design of the DAC and the amplifier are independent, because the amplifier noise is decoupled from C_{DAC} (unlike the PLF case).

Hence, the FoM of DAC and loop filter can be defined and calculated separately:

$$\text{FoM}_{\text{DAC}} = \text{E}_{\text{DAC}} \cdot \overline{V_{n,\text{DAC}}^2} = mV_{\text{REF}}^2 \cdot 2kT, \tag{4}$$

$$\text{FoM}_{\text{LF}} = \text{E}_{\text{LF}} \cdot \overline{V_{n,\text{LF}}^2} = \eta \cdot nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{g_m}, \tag{5}$$

where η is a coefficient determined by the amplifier topology (typically from 2 to 4), and V_{DD} is the supply voltage which can be assumed to be equal to V_{REF} (1.2 V). The derivation of (5) will be provided in Section III-B. The value of g_m/I_D for a transistor in sub-threshold region is $1/(nU_T)$, where n is a technology dependent factor and $U_T = kT/q$. In our calculation, n is set to 1.4 and g_m/I_D equals 27. The noise from the passive capacitor network is assumed to be negligible thanks to the relatively high gain (usually over 6×) of the amplifier. The final FoM defined in (1) for the OLA-based loop filter can be written as:

$$\begin{aligned}\text{FoM}_{\text{OLA}} &= (\text{E}_{\text{DAC}}+\text{E}_{\text{LF}}) \cdot (\overline{V_{n,\text{DAC}}^2} + \overline{V_{n,\text{LF}}^2}) \\ &= \text{FoM}_{\text{DAC}} + \text{FoM}_{\text{LF}} + \text{E}_{\text{DAC}} \cdot \overline{V_{n,\text{LF}}^2} + \text{E}_{\text{LF}} \cdot \overline{V_{n,\text{DAC}}^2} \\ &= \text{FoM}_{\text{DAC}} + \text{FoM}_{\text{LF}} \\ &+ \text{FoM}_{\text{DAC}} \frac{\overline{V_{n,\text{LF}}^2}}{V_{n,\text{DAC}}^2} + \text{FoM}_{\text{LF}} \frac{\overline{V_{n,\text{DAC}}^2}}{V_{n,\text{LF}}^2}.\end{aligned} \tag{6}$$

Note that for a positive variable x and two positive coefficients a and b, it can be shown that $ax + b/x \geq 2\sqrt{ab}$. The minimum value is obtained when $ax = b/x$, namely, $x = \sqrt{b/a}$. With $x = \overline{V_{n,\text{LF}}^2}/\overline{V_{n,\text{DAC}}^2}$, $a = \text{FoM}_{\text{DAC}}$ and $b = \text{FoM}_{\text{LF}}$, (6) is bounded by:

$$\text{FoM}_{\text{OLA}} \geq \text{FoM}_{\text{DAC}} + \text{FoM}_{\text{LF}} + 2\sqrt{\text{FoM}_{\text{DAC}} \cdot \text{FoM}_{\text{LF}}}, \tag{7}$$

and the minimum value of FoM_{OLA} can be obtained when the noise distribution satisfies $\overline{V_{n,\text{LF}}^2}/\overline{V_{n,\text{DAC}}^2} = \sqrt{\text{FoM}_{\text{LF}}/\text{FoM}_{\text{DAC}}}$.

Third, the loop filter can be built with a closed-loop integrator (CLI) [10]. This approach is similar to a ΣΔ ADC, and it can achieve a well-defined NTF thanks to the closed-loop feedback. For simplicity, a single-stage OTA is assumed in this loop filter. Its equivalent amplifier output resistance R_{eq} is $1/[(1-a)G_m]$, where G_m is the transconductance of the OTA, and its equivalent output capacitance C_{eq} is $a \cdot C_{\text{INT}}$ [11]. The input-referred noise power $\overline{V_{n3}^2}$ is:

$$\overline{V_{n3}^2} = \frac{2\xi kT}{(1-a)C_{\text{eq}}} \cdot \left(\frac{C_{\text{INT}}}{C_{\text{DAC}}}\right)^2, \tag{8}$$

where ξ is a factor whose value ranges from 1 to 2, dependent on the amplifier topology [11]. In our calculation, C_{INT} is equal to C_{DAC} to achieve an NTF of $(1-z^{-1})$ and a is $1/2$. The energy consumption of the amplifier (loop filter) E_{LF} can be calculated as:

$$\text{E}_{\text{LF}} = V_{\text{DD}} \cdot (2I_D) \cdot T_{\text{on}}, \tag{9}$$

where I_D is the bias current of a single input transistor, and T_{on} is the amplifier on-time. T_{on} equals the sampling period T_s if the amplifier is always-on, or it can be reduced to the duration of the amplification phase T_{amp} if a dynamic bias is used. The amplifier time constant τ_0 is $R_{\text{eq}}C_{\text{eq}}$. The amplification phase duration T_{amp} can be expressed as $\alpha \cdot \tau_0$, where α is determined by the settling requirement. Note that $\overline{V_{n3}^2}$ is a function of C_{DAC}, similar to the PLF scenario, so the FoM value in (1) can be directly obtained without individually calculating DAC and loop filter FoM values. Finally, the FoM of a CLI-based loop filter is:

$$\text{FoM}_{\text{CLI}} = (mV_{\text{REF}}^2 + 2\alpha \cdot nU_TV_{\text{DD}}\frac{T_{\text{on}}}{T_{\text{amp}}}) \cdot (2+8\xi)kT. \tag{10}$$

In our calculation, α varies from 3 to 5, and $T_{\text{on}}/T_{\text{amp}}$ ranges from 1 to 5, as a practical estimation for FoM_{CLI}. Note that this calculation is based on a conventional amplifier design, with recent emerged dynamic-amplifier-based designs [10], [12], FoM_{CLI} can be significantly reduced.

Fig. 3 shows the calculated FoM of the three loop filters using (3), (7) and (10), with the parameter (λ, m, η, ξ, α) ranges discussed before. As can be seen, PLF and OLA-based loop filter show similar minimum FoM values, while PLF and CLI-based loop filters show a large variety of FoM values which relies on the exact implementation. Fig. 4 summarizes the Schreier FoM (FoM_{S}) and signal-to-noise-and-distortion-ratio (SNDR) of the prior NS-SAR ADCs listed in [1] and two recent works [13], [14]. As indicated in Fig. 4, the OLA-based designs show in general higher power efficiency and higher SNDR compared to their PLF counterparts. The reason for the higher power efficiency is that most PLF-based designs have a large λ, which makes FoM_{PLF} from (3) typically higher than FoM_{OLA} from (7). The design in [6] successfully reduces λ to 1.6, thus outperforming the other PLF-based designs.

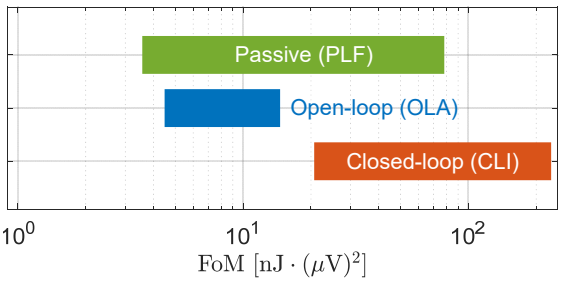

Fig. 3. Theoretical FoM of different loop filters.

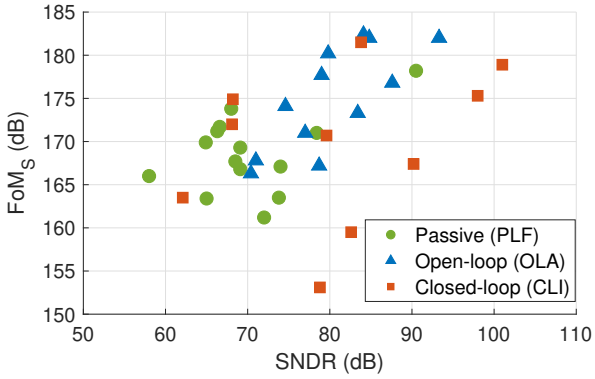

Fig. 4. NS-SAR ADC survey.

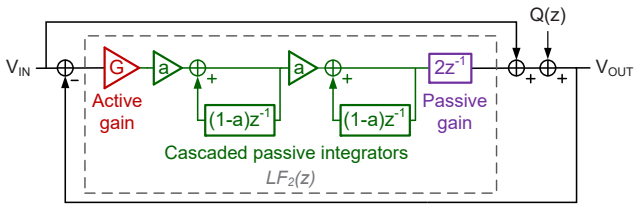

Fig. 5. Signal diagram of the proposed NS-SAR ADC.

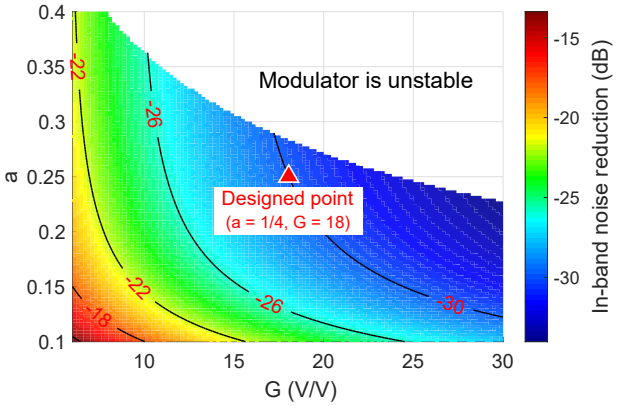

Fig. 6. In-band noise reduction with different G and a values.

The reason for the higher SNDR of OLA-based designs is that they can achieve higher-order noise shaping. In contrast, even though a high-order PLF is theoretically feasible, it is less practical, because the required high gain cannot be easily achieved due to either the parasitic capacitance in the passive gain stage [6] or the excess noise from the comparator gain stage [7]. For example, the loop filter structure in [6] has only been demonstrated with first-order noise shaping. The designs including CLI exhibit a wide range of power efficiency, which is caused by the different design choices for the closed-loop amplifier topology. Based on the above analysis, this work selects the OLA-based structure due to its high power efficiency and its potential to realize higher SNR.

B. Proposed NS-SAR Architecture

A prior OLA-based CIFF NS-SAR ADC adopts an FIR-IIR loop filter structure [9], but this limits the loop filter order to 1 because only one zero is created in the NTF by the single IIR filter in the loop. In this work, two identical passive IIR filters are cascaded to achieve second-order noise shaping, and a passive gain stage is included to further boost the loop filter gain, as shown in Fig. 5. With an oversampling ratio (OSR) of 16, the amplifier gain G and the coefficient a are swept in MATLAB based on the model from Fig. 5 to obtain the optimal in-band noise reduction, as shown in Fig. 6. As can be seen, higher gain in general helps achieve stronger in-band noise suppression at the cost of stability degradation. In this design, a is chosen as $1/4$ and G is 18 as a compromise of amplifier output range, noise suppression effect and modulator stability. Hence, the nominal NTF can be expressed as:

$$\text{NTF} = \frac{1 - 1.5z^{-1} + 0.56z^{-2}}{1 + 0.75z^{-1} + 0.56z^{-2}}. \tag{11}$$

Compared to prior works with a similar single-amplifier loop filter structure, the in-band noise attenuation of this design is 30 dB, which is 8 dB higher than in [9] and 4 dB higher than in [15] when the same OSR of 16 is assumed. The design in [16] achieves higher-order noise shaping by reusing the amplifier for both the CIFF and EF loops, which is a hardware-efficient solution to increase loop filter order. Overall, the high amplifier gain in this work facilitates competitive noise shaping performance compared to other NS-SAR ADCs with only one active amplifier.

Fig. 7(a) shows the circuit-level implementation for the proposed system. The main blocks of this ADC include a differential 10-bit binary-scaled DAC with 1-bit redundancy, an amplifier, two slices of load capacitors C_{RES} for the amplifier, two integration capacitors C_{INT1} and C_{INT2}, a comparator and logic control. The timing diagram is shown in Fig. 7(b). The frequency of the external sampling clock Φ_{SAMP} is 1 MHz and the ADC has an OSR of 16. After the sampling moment, the DAC is first reset by Φ_{RST} to achieve mismatch error shaping [17] (as will be explained in Section IV). When all 11 bits are resolved, the amplifier is enabled by Φ_{AMP} and the amplified residue voltage from the SAR conversion is stored on C_{RES}. The first passive integration between the two sets of C_{RES} and C_{INT1} takes place subsequently during Φ_{INT1}, as shown in Fig. 7(c). After that, the two C_{RES} capacitors which now contain the integrated residue are split to the positive and negative side and perform the second integration with C_{INT2} during Φ_{INT2}, as shown in Fig. 7(d). Since C_{INT2} is in series with $C_{\text{DAC,p}}$ and $C_{\text{DAC,n}}$, it will implement the summation of V_{IN} with the integrated residue in front of the quantizer, which is shown in Fig. 5. By placing two C_{INT2} capacitors in series with the DAC, the effective gain of the loop filter is further increased by $2\times$ [18]. The DAC outputs are connected to V_{CM} during the second integration phase to avoid signal-dependent charge injection at the end of the integration phase. The first passive integrator noise is attenuated by the amplifier gain and the second integrator noise is first-order shaped. Therefore, the integration capacitors can be made small. In this design, C_{RES} is set to 25 fF. Capacitor C_{INT1} is equal to C_{INT2}, and both are 3 times C_{RES} to realize $a = 1/4$, namely, C_{INT1} = C_{INT2} = $3C_{\text{RES}}$ = 75 fF.

III. Duty-Cycled Amplifier

This section starts with a discussion of the available amplifier solutions that are suitable for this ADC. After that, the duty-cycled amplifier is introduced to meet the gain requirement. Finally, a comparison between the proposed amplifier and other solutions will be provided.

A. Amplifier Topology

To implement the amplifier with $18\times$ gain efficiently, several topology options can be considered. A dynamic amplifier (DA) is a promising candidate thanks to its power efficiency.

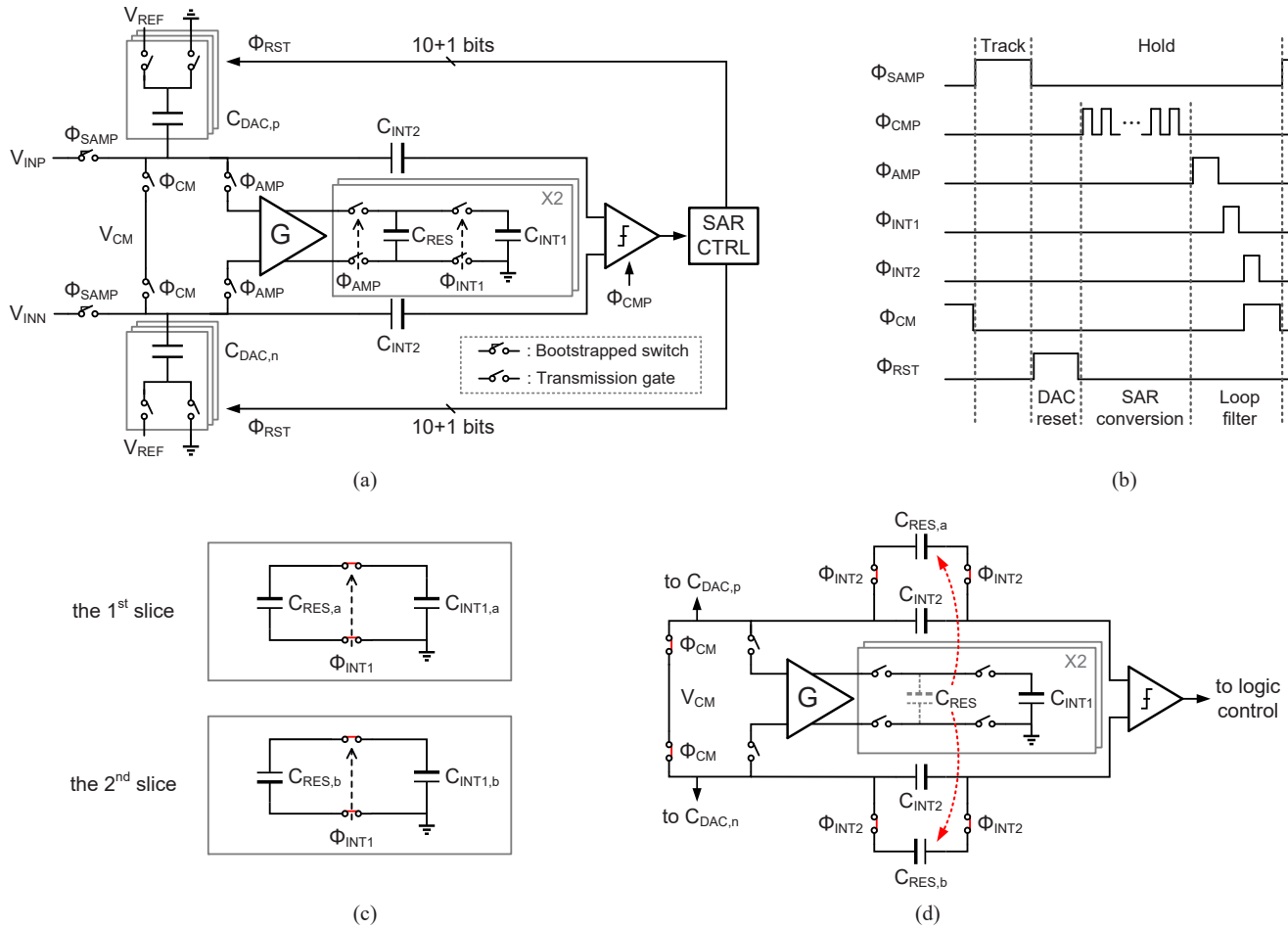

Fig. 7. (a) Proposed NS-SAR ADC. (b) Timing diagram. (c) The first integration phase. (d) The second integration phase.

However, its gain is limited by the allowed output common mode headroom, which is determined by the supply voltage. For instance, the dynamic amplifier in [9] has a gain of 13.3×, which is not enough for the proposed ADC. The comparator has been reused as a high-gain amplifier in [15], but it is hard to control the gain accurately due to the positive feedback in the comparator regeneration phase. The floating inverter amplifier (FIA) [5], [19] is an emerging choice to realize open-loop amplification, and it also fits the needs of this ADC.

Apart from the solutions discussed above, this work proposes a duty-cycled amplifier (DCA), as shown in Fig. 8. This amplifier has an inverter-based input stage to boost transconductance, and it includes switches to enable duty-cycling. The DC gain of this amplifier is designed to be 40× and the required 18× gain can be obtained by controlling the enable time to achieve incomplete settling [20], [21]. The static bias current of the amplifier is 17 μA and the power-on time is 14 ns. The common mode feedback (CMFB) of the amplifier is implemented by splitting the bottom tail current source and connecting their gates to the output nodes. This CMFB approach is suitable here, because the design does not require an accurate output common mode and the differential output range of the amplifier is only ±200 mV. The linearity of the amplifier is also not critical, because the amplifier input is the residue voltage, which consists of only quantization noise and comparator noise: amplifier non-linearity will thus only result in a slight increase in noise floor, but will not produce signal distortion.

Duty-cycled amplifiers have been used in prior ADC works [22], [23], but the current consumption associated with the bias current generation is usually neglected. In this work, a duty-cycled constant-gm bias circuit is also developed to provide the bias voltage V_{B} for the amplifier, as shown in Fig. 8(b). The start-up circuit is not drawn for simplicity. Besides the decoupling capacitors between the gate of the current mirror and supply/ground, another decoupling capacitor C_{B} (2 pF) is added to further stabilize V_{B} during duty-cycling. The control clocks Φ_{BCLK1} and Φ_{BCLK2} are derived from the asynchronous SAR logic and are only enabled once per 16 sampling clock cycles. The bias circuit is disabled in the other cycles, while the voltage V_{B} is kept by C_{B}. Refreshing V_{B} once per 16 clock cycles is sufficient to mitigate drift due to capacitor leakage. In this way, the consumption of the bias generator is reduced to only 18% of the amplifier power in this design.

Post-layout simulation of the amplifier together with the bias circuit and enabling time control logic shows a gain variation from 14.8× to 18.6×, under 1.1V to 1.3V supply voltage, $0°C$ to $80°C$ temperature range and process variations. This

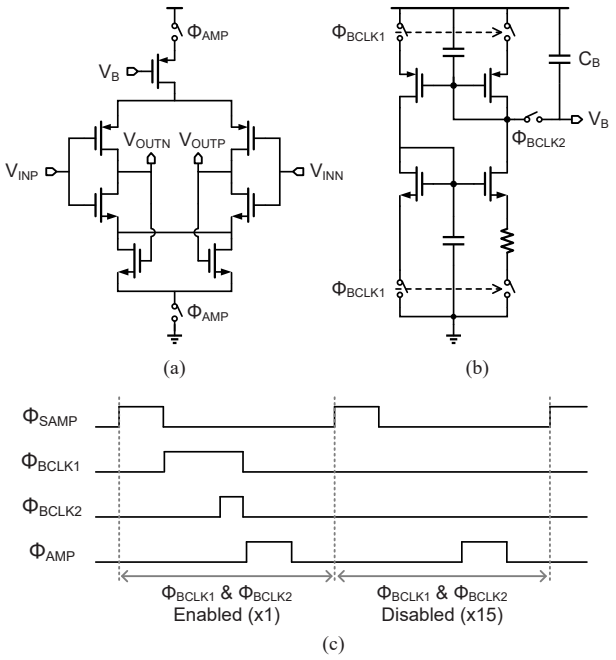

Fig. 8. (a) Duty-cycled amplifier. (b) Duty-cycled bias circuit. (c) Timing diagram for the amplifier and bias circuit.

is sufficient to keep the modulator stable according to Fig. 6, with a maximum SQNR variation of 1.9 dB.

B. Comparison of Different Open-Loop Residue Amplifiers

The power efficiency of the proposed DCA is benchmarked with DA and FIA using the same FoM definition as before (1). In this context, we only consider the energy consumption and noise power of the amplifier itself. All the amplifiers are assumed to operate in the sub-threshold region for a maximum g_m/I_D value. For the DA [9] shown in Fig. 9(a), the amplifier energy consumption E_{DA} can be directly calculated as:

$$E_{\text{DA}} = V_{\text{DD}} \cdot 2I_D \cdot T_{\text{int}}, \tag{12}$$

where T_{int} is the integration time.

The current noise power spectrum density for a single transistor in the sub-threshold region is $2qI_D$, and the equivalent noise bandwidth is $1/(2T_{\text{int}})$ [24]. Hence, the input-referred noise power $\overline{V_{n,\text{DA}}^2}$ is:

$$\overline{V_{n,\text{DA}}^2} = \frac{4qI_D}{g_m^2} \cdot \frac{1}{2T_{\text{int}}}, \tag{13}$$

where g_m is the transconductance of a single input transistor. With a g_m/I_D value of $1/(nU_T)$ in sub-threshold region, the FoM of the DA can be written as:

$$\text{FoM}_{\text{DA}} = 4nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{g_m}. \tag{14}$$

For the proposed DCA shown in Fig. 9(b), the energy consumption E_{DCA} is:

$$E_{\text{DCA}} = V_{\text{DD}} \cdot 2I_D \cdot T_{\text{on}}, \tag{15}$$

where T_{on} is the on-time of the amplifier. It can be expressed as a function of the settling time constant τ_0 of the amplifier, namely,

$$T_{\text{on}} = \alpha \cdot \tau_0. \tag{16}$$

The input-referred noise for the DCA can be expressed as:

$$\overline{V_{n,\text{DCA}}^2} = \frac{8qI_D}{(2g_m)^2} \cdot \frac{1}{4\tau_0} \cdot F_{\text{noise}}, \tag{17}$$

This noise power expression is composed of the noise from a fully-settled amplifier and a factor F_{noise} due to the noise increase when the amplifier is not fully settled. The transconductance of the input PMOS and NMOS transistors is assumed to be both g_m. The noise penalty from the incomplete settling can be found as [20], [25]:

$$F_{\text{noise}} = \frac{1 - e^{-2\alpha}}{(1 - e^{-\alpha})^2}. \tag{18}$$

The FoM of the DCA can then be written as:

$$\text{FoM}_{\text{DCA}} = nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{g_m} \cdot \alpha F_{\text{noise}}. \tag{19}$$

For the FIA shown in Fig. 9(c), its FoM is derived in [5]:

$$\text{FoM}_{\text{FIA}} = 2nkT \cdot V_{\text{DD}} \cdot \frac{I_D}{g_m}. \tag{20}$$

The three FoM values can be normalized to $nkT \cdot V_{\text{DD}} \cdot I_D/g_m$ to get η in (5), and the normalized FoM values are plotted in Fig. 10 with α from 0.1 to 3. The FIA is assumed to be fully settled, so that its FoM is independent on α. As can be seen, the theoretical minimum FoM_{DCA} and FoM_{FIA} are about half of FoM_{DA}. This is due to the current reuse in the inverter-based input pairs in DAC and FIA, which boosts the amplifier transconductance by $2\times$. The FoM_{DCA} is approximately proportional to α as a result of the linear relationship between the amplifier energy consumption and its on-time in (16). When α approaches zero, FoM_{DCA} is equal to FoM_{FIA} because the initial RC settling behavior of an amplifier can be approximated as a linear integration phase. The amplifier time constant τ_0 in this design is 24 ns, and α is 0.58. This makes the proposed DCA achieve similar power efficiency as the FIA. Note that the derivation for FoM_{FIA} assumes an infinite output impedance from the input transistors [5], which models the FIA as an ideal integrator and overestimates its gain. This finally leads to a rough FoM value that can be higher in an actual circuit implementation. The derivation for FoM_{DCA} takes the amplifier settling behavior into consideration and is thus a more practical result. The three amplifiers all require timing logic to stop the integration or amplification, which is assumed to cause similar power overhead. The gain of a DA or DCA is controlled by various circuit parameters (like g_m) and the active time, and thus it is susceptible to PVT variations. On the other hand, the gain of a fully-settled FIA is determined by the ratio of the reservoir capacitor C_{R} and load capacitor C_{L}, and that makes it more robust.

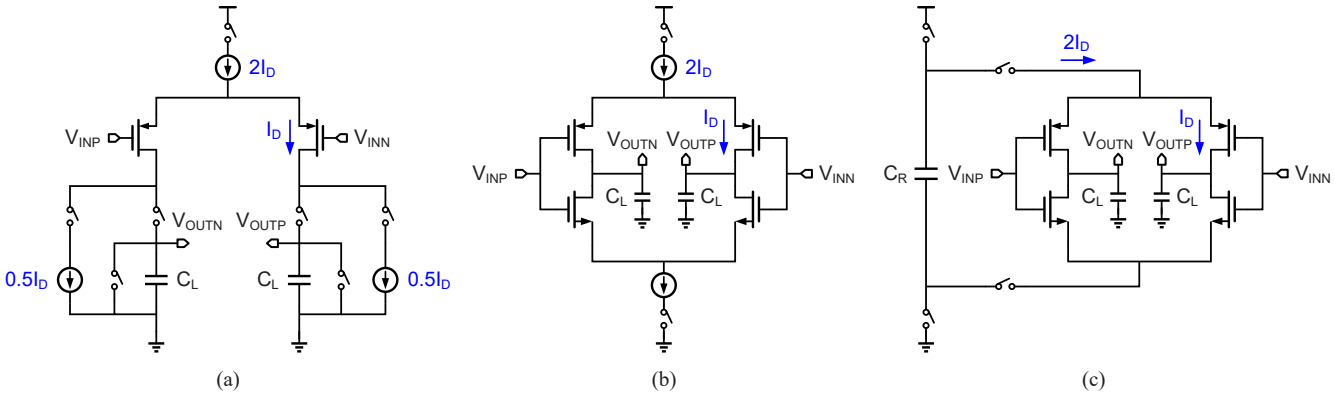

Fig. 9. (a) Dynamic amplifier [9]. (b) Duty-cycled amplifier. (c) Floating inverter amplifier [5].

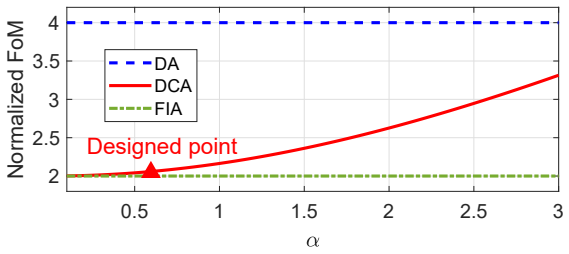

Fig. 10. Theoretical FoM of different amplifiers.

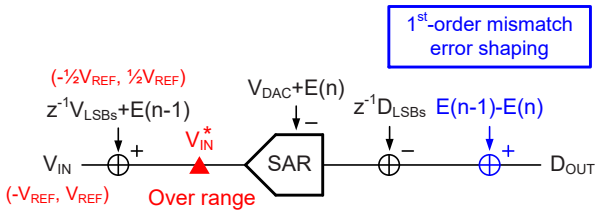

Fig. 11. Principle of the 1st-order MES and its over range problem.

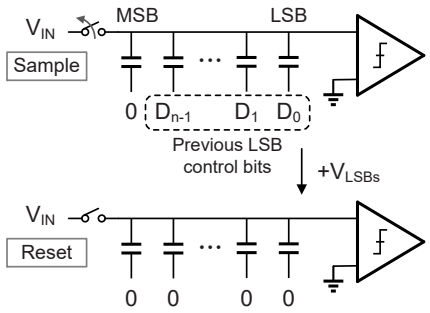

Fig. 12. The DAC switching sequence for MES proposed in [17].

IV. Mismatch Error Shaping

This section first briefly reviews the principle of the mismatch error shaping (MES) technique and available solutions to overcome its over range problem. After that, a two-level digital prediction scheme is explained and its difference with the prior tri-level prediction scheme [26] is highlighted.

A. Principle of MES

An effective method to deal with DAC mismatch in an oversampled SAR ADC is MES [17]. Fig. 11 illustrates the principle of MES. During the SAR conversion, the DAC generates the reference voltage, modelled as an ideal DAC voltage V_{DAC} and a mismatch error E(n), for the comparator. After the SAR conversion is finished, the MSB control bit is reset immediately, but the LSB control bits ($D_{\mathrm{n\text{-}1}}$, ..., D_1, D_0 as shown in Fig. 12) are held until the sampling of the next input signal. After the sampling phase, the DAC LSBs (MSB-1 to LSB) are reset, which equivalently adds the ideal DAC LSB voltage V_{LSBs} and the mismatch error E(n-1) from the previous sample to the current input. By altering the reset timing in this way and subtracting the additional V_{LSBs} in the digital domain, mismatch errors are first-order shaped [17]. Note that the delayed mismatch error E(n-1) is injected at the converter input, so that it also goes through an STF of 1. Therefore, the first-order MES effect is always valid irrespective of the specific loop filter transfer function.

However, because V_{LSBs} has a theoretical range between $-\frac{1}{2}V_{\mathrm{REF}}$ and $+\frac{1}{2}V_{\mathrm{REF}}$, over range may occur at the input of the converter as indicated in Fig. 11. Several measures can be adopted to solve this problem. First, data weighted averaging (DWA) can be used to mitigate the mismatch errors in the first few MSBs, and MES is only applied to the remaining LSBs [17]. This method alleviates the over range problem but complicates the logic design by involving two sets of mismatch shaping algorithms. Second, an analog input signal attenuation method is proposed in [13] by using another capacitor to divide each input signal by 2. However, this may cost more chip area due to the need for an extra attenuation capacitor which has the same capacitance as the DAC array. Third, a signal prediction scheme can be used to predict and prevent an over range occurrence by injecting a compensation signal. This approach can be implemented either in a digital way [26] or in an analog manner [27]. It takes full advantage of MES and only requires a small change to the circuit to implement the prediction logic and compensation step. Therefore, a digital prediction scheme is used in this work.

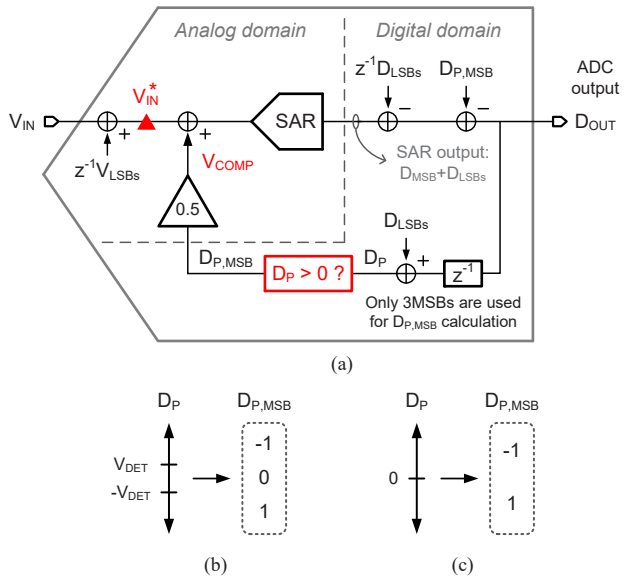

Fig. 13. (a) Principle of the MES with digital prediction. (b) Tri-level prediction scheme proposed in [26]. (c) Two-level prediction scheme in this work.

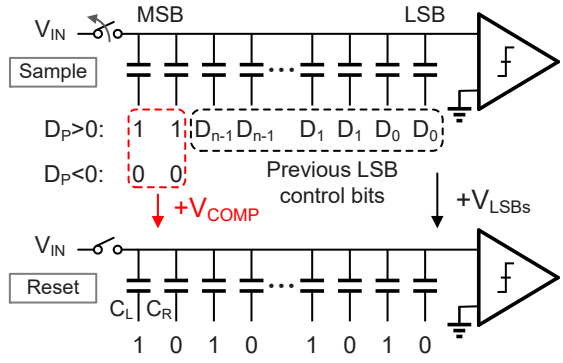

Fig. 14. DAC switching sequence in the proposed MES with two-level digital prediction.

B. Two-Level Digital Prediction Scheme

The main idea behind the digital prediction scheme is that, in an oversampled system, the current ADC output can be used as a rough guess for the next input sample of the ADC. Therefore, the actual input (V_{IN}^{*} in Fig. 11) can be estimated from the available ADC output information. Using this estimate, the MSB capacitors in [26] are pre-set according to the estimate before sampling to compensate for the V_{LSBs} shift.

This work simplifies the method described in [26] by introducing a two-level over range detection scheme, as shown in Fig. 13 and Fig. 14. The estimated next ADC input D_P is calculated by adding the first 3 bits (MSB to MSB-2) from the current ADC output code D_{OUT} and the first 2 bits from the current SAR output code D_{LSBs}. To provide MSB compensation, a split switching scheme is used in the DAC. By judging if D_P is greater or less than zero, the MSB capacitors are pre-set to '11' or '00' before the track phase. Therefore, a compensation voltage V_{COMP} can be obtained by resetting the

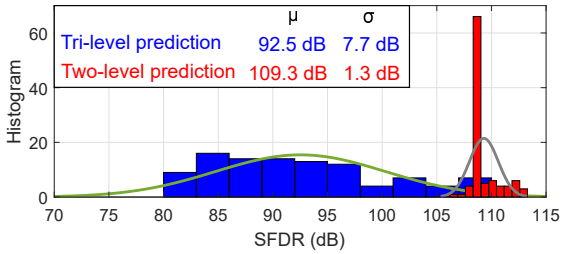

Fig. 15. Simulated SFDR histogram from 100× Monte-Carlo simulations with random DAC capacitor mismatch.

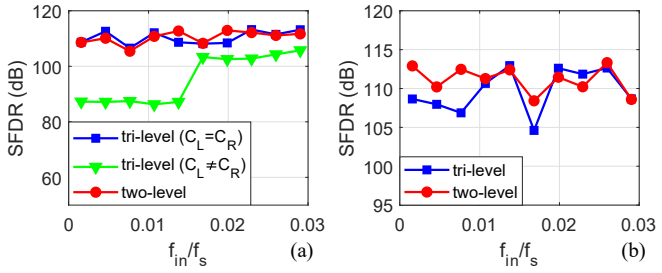

Fig. 16. SFDR versus input signal frequency (OSR = 16) with (a) split switching scheme and (b) V_{CM}-based switching scheme. Each data point is averaged over 100× Monte-Carlo simulations with random capacitor mismatch.

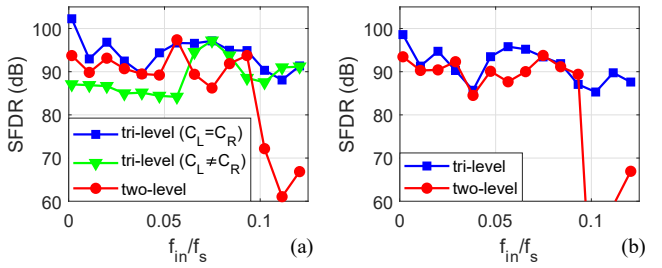

Fig. 17. SFDR versus input signal frequency (OSR = 4) with (a) split switching scheme and (b) V_{CM}-based switching scheme. Each data point is averaged over 100× Monte-Carlo simulations with random capacitor mismatch.

MSB capacitors after the sampling moment, as shown in Fig. 14. The tri-level prediction scheme in [26] works similarly, but when D_P is between $-V_{DET}$ and V_{DET}, the MSB capacitor does not switch and provides V_{COMP} = 0 V. In this case, the mismatch between the MSB capacitors (C_L and C_R in Fig. 14) causes asymmetry in the positive and negative V_{COMP} values and exhibits distortion tones in the spectrum. The proposed two-level detection scheme, instead, ensures that the MSB capacitors are always involved in the over range compensation, so that an inherently linear two-point compensation voltage is created. Fig. 15 shows the simulated spurious-free-dynamic-range (SFDR) histogram with the tri-level and the two-level schemes. Only quantization noise is included in the simulation and the other noise sources are excluded. The unit capacitor is 0.5 fF, and the capacitor mismatch is assumed to be 1% for 1 fF capacitance. It can be seen that with the two-level prediction, the average SFDR is improved by 17 dB. It is worth

mentioning that this advantage of two-level prediction over tri-level prediction is less relevant if a V_{CM}-based switching scheme is used, because with $V_{CM} = 1/2V_{REF}$, the value of V_{COMP} will be symmetric around zero. In this case, the two-level and tri-level prediction schemes perform similarly in terms of linearity. This is verified by Fig. 16 where the simulated SFDR using both switching schemes is presented. The unit capacitor is 1 fF for the V_{CM}-based switching scheme to make sure that the total DAC capacitance is the same for both switching schemes. As can be seen in Fig. 16(a), tri-level prediction performs worse than two-level prediction in case of a split switching scheme if there is mismatch between C_L and C_R. If a V_{CM}-based scheme is used (Fig. 16(b)), the performance is similar for both prediction methods.

The maximum tolerable prediction error $\varepsilon_{tol,dig}$ in a digital prediction scheme can be expressed as [26]:

$$\varepsilon_{tol,dig} = \min(0.5V_{REF} + V_{DET}, V_{REF} - V_{DET}), \tag{21}$$

where $0 \leq V_{DET} \leq 0.5V_{REF}$. In [26], V_{DET} is $0.25V_{REF}$ to achieve a maximum tolerable error of $0.75V_{REF}$. With a two-level digital prediction where $V_{DET} = 0$ V, $\varepsilon_{tol,dig}$ is reduced to $0.5V_{REF}$. The value of $\varepsilon_{tol,dig}$ can be translated to the maximum input frequency f_{in} at which a certain prediction scheme remains functional, namely,

$$\frac{f_{in}}{f_s} \leq \frac{\varepsilon_{tol,dig}}{2\pi A_{in}}, \tag{22}$$

where f_s is the sampling frequency, and A_{in} is the input signal amplitude. For a -1 dBFS input signal ($A_{in} = 0.89V_{REF}$), the maximum f_{in} that the tri-level prediction can support is $0.13f_s$ (OSR = 3.8), while it drops to $0.09f_s$ (OSR = 5.6) for the two-level prediction scheme due to the reduction in $\varepsilon_{tol,dig}$. Fig. 17 shows the simulated SFDR at different input frequencies with the two-level or the tri-level prediction following the same capacitor mismatch setup as in Fig. 16. The input signal power is -1 dBFS and the OSR is fixed to 4. Note that the OSR is set to 4 here just to verify the correctness of (22), and in the actual design it is 16. As can be seen, the SFDR with the tri-level prediction remains relatively constant when f_{in}/f_s is smaller than 0.12, while the SFDR with the two-level prediction drops when f_{in}/f_s exceeds 0.09, which agrees with the calculation results from (22). Thus, while the two-level scheme is simpler to implement, it restricts the input frequency range and requires higher OSR compared to tri-level prediction.

In an analog prediction approach [27], the over range detection is done directly for the input signal V_{IN} instead of V_{IN}^* shown in Fig. 13(a), so the maximum tolerable error $\varepsilon_{tol,ana}$ becomes:

$$\varepsilon_{tol,ana} = \min(V_{DET}, 0.5V_{REF} - V_{DET}). \tag{23}$$

With $V_{DET} = 0$ V in [27], $\varepsilon_{tol,ana}$ reduces to zero. This implies that prediction errors cannot be avoided, but by sufficient design margin, the probability and magnitude of the induced errors can be designed to remain under the noise floor of the converter [27].

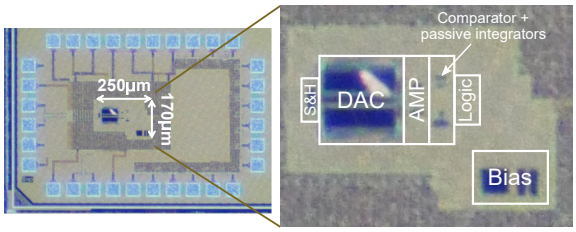

Fig. 18. Die photo.

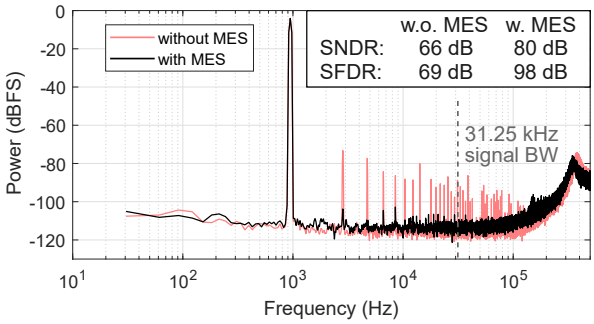

Fig. 19. Measured spectrum without and with MES.

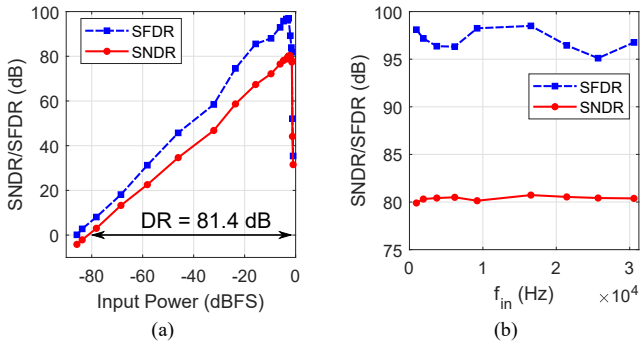

Fig. 20. Measured SNDR and SFDR vs. (a) input power and (b) input frequency.

V. Measurement Results

The prototype is fabricated in a 65 nm CMOS technology. The area of the ADC is 0.043 mm^2, as shown in Fig. 18. Thanks to MES, the DAC capacitance is reduced to 1 pF per side. It is only limited by noise requirements and occupies less than half of the total area. Except for the sampling clock, other logic blocks (SAR logic, MES prediction logic, NS logic to generate all the clocks shown in Fig. 7 and Fig. 8) are implemented on-chip. The final output code processing (redundancy bit addition, LSB digits and prediction bit addition in MES) is done off-chip.

Fig. 19 shows the measured spectrum without and with MES at an input signal frequency of 946.07 Hz and a sampling frequency of 1 MS/s. Each spectrum uses a 2^{15}-point FFT with a Hamming window, and is averaged 10 times. After enabling MES, the SNDR and SFDR improve from 66 dB to 80 dB and from 69 dB to 98 dB, respectively. The odd-order harmonics caused by DAC mismatch are reduced significantly. From analysis of the measurements, it is likely that the measured

TABLE I
BENCHMARK WITH OTHER WORKS

	ISSCC'16 [17]	VLSI'16 [28]	ISSCC'17 [9]	ISSCC'20 [6]	ISSCC'20 [29]	ISSCC'21 [16]	ISSCC'21 [30]	This work
Technology	55 nm	28 nm	28 nm	40 nm	28 nm	40 nm	40 nm	65 nm
Supply (V)	1.2	1.8 / 1.1	1	1.1	1	1.1	1.1	1.2
Loop filter order	1	3	1	1	4	3	4	2
SAR resolution	12	12	10	13	8	10	9	10
Fs (MS/s)	1	1	132	2	2	10	5	1
BW (kHz)	4	20	5000	40	100	625	250	31.25
OSR	125	25	13.2	25	10	8	10	16
Loop filter type	CLI	CLI	OLA	PLF	OLA	OLA	OLA*	OLA
Amplifier topology	Cascode amplifier	Two-stage amplifier	Dynamic ampilifier	N.A.	Cascode amplifier	Floating inverter amplifier	Flipped voltage follower	Duty-cycled amplifier
Amplifier gain	100×	N.A.	13.3×	N.A.	9.5×	16×	1×	18×
Cap mismatch solution	1st-order MES + DWA	DEM + dither	DWA	2nd-order MES + DWA	Off-chip calibration	Off-chip calibration	Off-chip calibration	1st-order MES
DAC cap per side (pF)	2.4	N.A.	1.6	18	7.7	0.4	16	1
SNDR (dB)	96.1	94.0	81.3	90.5	87.6	84.8	93.3	80
SFDR (dB)	105.1	108.0	92.2	102.2	102.8	103	104.4	98
Power (μW)	15.7	493.1	480	67.4	120	119	340	7.3
FoMw (fJ/conv. step)	37.6	302.6	5.1	30.8	30.6	6.7	18.1	14.3
FoMs (dB)	180.2	170.0	181.5	178.2	176.8	182.0	182.0	176.3
Area (mm^2)	0.072	0.116	0.0049	0.061	0.02	0.04	0.094	0.043

FoMw = Power/($2^{ENOB}\times 2\times$BW)
FoMs = SNDR + $10\log_{10}$(BW/Power)
* This design uses capacitor stacking with buffering to avoid passive integration loss. Since its first stage in the loop filter is an open-loop amplifier, it is categorized as OLA.

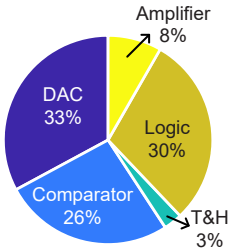

Fig. 21. Power breakdown.

SNDR and SFDR are limited by IO disturbances. Fig. 20 shows the ADC performance over input signal frequency and input signal power. As can be seen, the SNDR remains above 80 dB and SFDR remains above 95 dB in the whole 31.25 kHz bandwidth. The dynamic range (DR) of this ADC is 81.4 dB.

The total power consumption is 7.3 μW with a 1.2 V supply when MES is enabled. Based on simulations, the ADC power breakdown is shown in Fig. 21. The amplifier power only occupies 8% of the total power owing to the duty-cycled operation and the DAC power occupies 33% as a result of the noise-limited total capacitance. After MES is enabled, the DAC power and digital power have increased by 20% and 5%, respectively.

Table I presents a performance summary and comparison to state-of-the-art NS-SAR ADCs. The duty-cycled amplifier in this design provides higher gain than the other amplifiers used in OLA-based NS-SAR ADCs, which helps increase the loop filter gain and suppress the in-band noise. Higher-order NS-SAR ADCs [16], [29], [30] are shown in recent literature by cascading more integrator stages. The loop filter in this design can also be extended to higher order with additional integration stages. The amplifier presented in this work is also applicable to build other loop filter topologies, such as EF [15] or hyrid EF-CIFF [16] loops. The simplified MES prediction scheme avoids external DAC calibration, leading to lower DAC capacitance when targeting the same linearity performance. This work uses only 1 pF DAC capacitance per side while achieving comparable SFDR as other works. In summary, the duty-cycled amplifier and MES techniques can be used as simple and versatile solutions in NS-SAR ADC design.

VI. Conclusion

Different loop filter structures and open-loop amplifier topologies are benchmarked in this paper regarding their power efficiency. The OLA-based loop filters are considered as an attractive option to realize low-power NS-SAR ADCs. It is proposed to use a duty-cycled amplifier together with a duty-cycled bias generator to build the loop filter, which achieves high loop filter gain in a power-efficient way. Furthermore, a two-level digital-predicted MES technique solves the DAC mismatch problem and prevents over range, at the cost of slightly tighter OSR requirements. Thanks to these techniques, the ADC reaches 80 dB SNDR and 98 dB SFDR in a 31.25 kHz bandwidth while consuming 7.3 μW.

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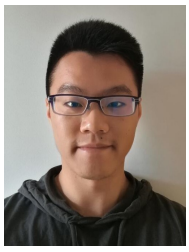

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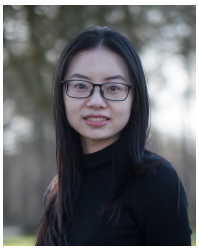

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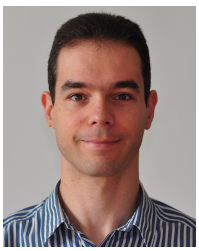

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