A SAR ADC with Reconfigurable Delay and Redundancy to Relax the Reference Driver

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***Abstract*—This work presents a reconfigurable delay and redundancy technique, which relaxes the reference driver requirements for a charge-redistribution SAR ADC. By selectively adding delay to the most critical SAR cycle, the overall speed of the ADC is only slightly degraded, while the output impedance of the driver or the amount of decoupling capacitance can be reduced substantially. In a simulated 10-bit 10 MS/s SAR ADC prototype, the proposed technique reduces the decoupling capacitance by 16× while maintaining 59.2 dB SNDR and 71.2 dB SFDR at a power consumption of 32 μW. The estimated area is 0.002 mm^2 including decoupling capacitors.**

***Index Terms*—Analog-to-digital converter, decoupling capacitor, reference voltage driving, redundancy.**

I. Introduction

Successive-approximation register (SAR) analog-to-digital converters (ADCs) with capacitive digital-to-analog converters (DACs) are the most popular choice in Internet-of-the-Things (IoT) or biomedical sensing systems thanks to their energy efficiency and simple architecture [1], [2]. In practice, several auxiliary circuits are required to make an ADC work properly. For example, a clean and stable reference voltage is required for the DAC [3]. Fig. 1 shows a typical reference voltage driving network for capacitive DACs, which consists of a buffer and a decoupling capacitor [3]. During the SAR conversion, the DAC capacitors take charges from the reference voltage and thus cause glitches at $V_{REF,IN}$ due to the finite driver bandwidth. As shown in Fig. 2a, the reference recovery time needs to be smaller than the time of a single bit-cycle of the SAR ADC to ensure an accurate conversion. However, due to the limited bandwidth of the buffer, the timing may be insufficient for the reference voltage to recover which may result in conversion errors (Fig. 2b). A generic solution to address this problem is either to use a power-hungry buffer with large bandwidth or to use a large decoupling capacitor. However, as ADCs have become very efficient in energy and area, the power consumption or area cost of the reference voltage driving network may become dominant compared to the ADC [4], [5].

To address the reference voltage driving problem, a widely used approach is to add redundancy [2], [6]. What should be noted here is that adding redundancy can not fix the errors happening after the redundancy bit(s) or exceeding the redundancy range. Also, extra digital post processing is needed to reconstruct the final output code. When low-power buffers or small decoupling capacitors are used, it is likely that the reference errors are too large to be fixed by just adding 1-bit redundancy. Multi-bit redundancy or sub-2-radix redundancy [2] might be required, which complicates the overall design.

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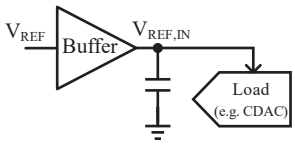


Fig. 1: A typical reference voltage driving network.

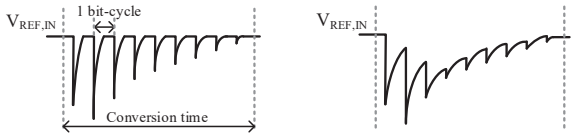


Fig. 2: Reference settling behavior with sufficient settling time (a) and insufficient settling time (b).

Recently, more advanced designs have been proposed to address the reference voltage driving problem. [3], [7], [8] adopt reservoir capacitors to drive the reference voltage, thus the ADC reference voltage is isolated from external interference. A main drawback of using a reservoir capacitor is that the reference voltage suffers from signal-dependent voltage drop. To address this problem, [3], [7], [8] propose various techniques, for example, adding an auxiliary DAC to make the DAC step linear, adding switched capacitor circuits to compensate for the reference voltage drop, using multiple supplies, and so on. Another drawback of this method is that the external supply still sees a switched capacitor load, which may not be preferred in practice. Except for using reservoir capacitors, [9] proposed to add a charge neutralization circuit to compensate for the reference voltage loss continuously. [10] proposed to replicate the reference errors by another cancellation DAC and feed it back to a multi-input comparator. For both [9] and [10], an extra compensation DAC and two extra references are required.

The goal of this work is to relax the reference voltage driving requirement adaptively depending on the required performance and reduce the decoupling capacitor size. A reconfigurable delay technique is proposed, which, combined with redundancy, can compensate adaptively for the reference

voltage drop. A 10-bit 10 MS/s SAR ADC in 65 nm CMOS technology is designed as an example. By applying the proposed technique, the decoupling capacitance can be reduced from 32 pF to 2 pF (assuming a driver output impedance of 2 kΩ), and chip area is reduced from 0.0061 mm^2 to 0.002 mm^2.

This paper is organized as follows. Section II presents the analysis of the reference voltage driving network and the proposed reconfigurable delay technique. Circuit implementation details are shown in Section III. Results and conclusions are presented in Section IV and Section V, respectively.

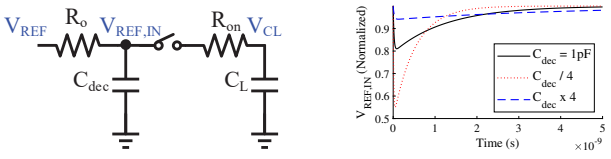
II. Proposed Reconfigurable Delay

A. Basic reference settling model

To gain insight in the reference driving problem, the reference voltage settling behavior is analyzed. Fig. 3a shows a simplified DAC switching model for a charge redistribution SAR ADC. R_o stands for the output resistance of the buffer, which is related to the inverse of the energy consumption of the buffer. C_{dec} is the on-chip decoupling capacitance, which dominates the area of the reference driving network. R_{on} stands for the on-resistance of the DAC unit driver and C_L is the load capacitance. The buffer transfer function can be calculated as

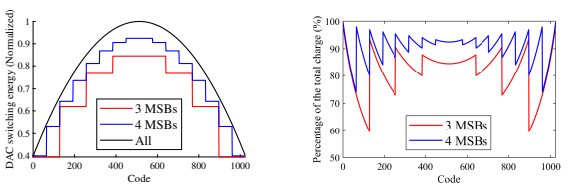
$$\frac{V_{REF,IN}(s)}{V_{REF}(s)} = \frac{R_oC_{dec}R_{on}C_Ls^2 + (R_oC_{dec} + R_{on}C_L)s + 1}{R_oC_{dec}R_{on}C_Ls^2 + (R_oC_{dec} + R_{on}C_L + R_oC_L)s + 1} \quad (1)$$

The time domain response is shown in Fig. 3b. With a smaller C_{dec}, the reference voltage has a larger drop but recovers faster, while with a larger C_{dec}, the reference voltage has a smaller voltage drop but a longer recovery time. To meet the linearity requirement, the reference voltage needs to be recovered to a certain level within a certain time after each switching activity. Instead of making the reference recovery faster (which costs power in the driver), an alternative way is to make the AD conversion slower at the critical bit decisions to tolerate a longer settling time. However, since the settling behaviour is different for different driver parameters (Fig. 3b), such an intentional delay should be adjustable.



(a) (b)

Fig. 3: (a) Simplified DAC switching model and (b) Time domain reponses with various values of C_{dec} when R_o = 1 kΩ, R_{on} = 100 Ω, C_L = 256 fF and $V_{REF,IN}(initial) = V_{REF}$, $V_{CL}(initial) = 0V$.



(a) (b)

Fig. 4: (a) DAC switching energy and (b) Percentage of the charge taken by the first 3 or 4 bits.

B. DAC switching behavior

The reference ripples are directly related to the DAC switching scheme. A split monotonic switching scheme is used in this work as an example. Fig. 4a shows the DAC switching energy for each code for a 10-bit ADC. Fig. 4b shows the percentage of charge the first 3-bit/4-bit switching takes. The reset energy for each conversion is not included in Fig. 4 since usually sufficient time can be ensured for the DAC reset and it will not affect the reference settling during conversion. As is shown in the figure, the first 3-bit/4-bit DAC switching takes most of the charge and causes a large voltage drop. For the LSBs, the requirement of the reference driver network is much more relaxed. Thus, extra delay can be generated after these initial 3 or 4 bits to make sure that the reference voltage is sufficiently recovered for the LSBs.

C. Proposed Reconfigurable delay

In this design, it is assumed that asynchronous SAR logic is used, where the conversion timing is controlled by a self-oscillation loop [11]. The conversion time for each bit-cycle is determined by the comparison time and the self-oscillation loop delay. The latter loop delay is normally fixed while the comparison time is signal dependent. To relax the reference driver's requirement, the self-oscillation loop delay could be extended at the cost of reducing the ADC speed.

The principle applied here is to generate an extra delay for the most critical cycle only. By adding delay to only one cycle, the impact on overall ADC speed is minimized. However, the most critical cycle and the required delay depend on the driver, and thus they should be made reconfigurable. As an example, Fig. 5 illustrates the reference voltage with/without extra delay. By adding extra delay, the reference voltage is

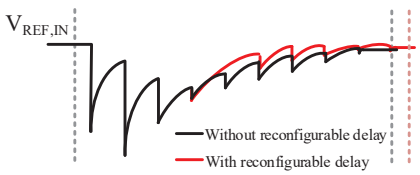


Fig. 5: $V_{REF,IN}$ with/without reconfigurable delay.

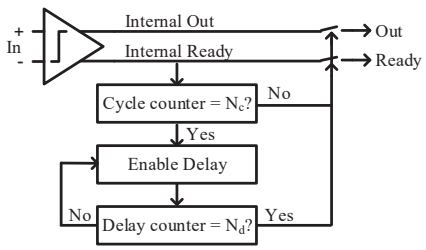


Fig. 6: Flow diagram of reconfigurable delay.

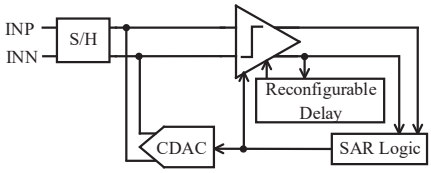


Fig. 7: SAR ADC architecture.

able to recover to a safe level before the LSB switching starts. When combined with redundancy [6], this can mitigate reference-induced errors.

Fig. 6 shows a flow diagram of the proposed reconfigurable delay. Here, N_c stands for the bit-cycle where extra delay is enabled. N_d stands for the length of the extra delay, expressed as the number of oscillation cycles of the asynchronous logic [9]. N_c and N_d are reconfigurable to adapt to various reference voltage driving networks with different driving abilities. As shown in Fig. 6, if the active cycle is not N_c, the comparator output is immediately forwarded to the SAR logic. In cycle N_c, a delay of N_d cycles is activated before the comparator result is forwarded to the SAR logic. The effect of different N_c and N_d settings will be investigated with an example design.

III. Circuit implementation

A. ADC overview

Fig. 7 shows the architecture of the 10-bit ADC, which is used as a test design for the proposed technique. It consists of a sample and hold circuit, a DAC, a comparator, asynchronous SAR logic and a reconfigurable delay block (as in Fig. 6). The sample and hold switches are clock boosted [12]. A split monotonic switching scheme is used for the DAC to save power and the DAC unit cells are implemented as unit-length capacitors [13]. The total sampling capacitance is $\approx$ 250 fF. To add redundancy to the ADC, the DAC has an additional capacitor with a value of 8LSB, creating overlap in the search algorithm [6].

B. Reconfigurable Delay

Fig. 8 shows the schematic design of the comparator with the proposed reconfigurable delay. A fully dynamic 2-stage comparator with a pre-amplifier and a latch is used [14]. The comparator is controlled by an enable signal (ENABLE, Fig. 8b) from the SAR logic and the clock signal (CLK) from the self-oscillation loop. N_c selects in which bit-cycle the delay is activated by multiplexing the appropriate RDYi signal, which is generated by the main SAR logic when bit-cycle i is ready. Prior to cycle N_c, the comparator ready indication (CMPRDY) will directly generate a RDY trigger towards the SAR logic via path 1. However, in the cycle selected by N_c, gate X stops the operation of path 1. Now, the counter first needs to reach N_d cycles of delay such that CNTD goes high, which enables path 1 again by switching gate X. After cycle N_c, since CNTD remains high, CMPRDY is forwarded directly to RDY again. N_c and N_d can be programmed through an on-chip serial register to define the reconfigurable delay settings.

An example timing diagram when N_c = 4 and N_d = 1 is shown in Fig. 8c. Once the input signal is sampled, the ENABLE signal will be set to 1 and the SAR conversion starts. At the fourth cycle, CNTC will go high, and the delay counter is enabled. Then, the delay counter starts to count. The delay ready signal (CNTD) will go high when N_d delay units are reached. In this case (N_d = 1), one more loop delay is generated. When N_d is set to 0, the reconfigurable delay is disabled. Once the conversion is ready, the ENABLE signal will be set to 0 by the SAR logic and the internal signals will be reset. The reconfigurable delay function only requires the shown logic gates, and does not require any changes in the DAC or digital processing. Therefore, the proposed method is simple to implement.

IV. Simulated results

The proposed idea was designed and simulated at transistor-level in a commercial 65 nm CMOS technology using Cadence. To investigate the effects of the various techniques, 10-bit ADCs without any enhancing technique (Original), with longer self-oscillation loop delay for all bit-cycles (Slow), with 1-bit redundancy at bit 8 (+R), with reconfigurable delay (+D) and with both redundancy and reconfigurable delay (+R&D) are made. In total, 5 designs are simulated and compared. All simulations are done at a sample rate of 10 MS/s, an input signal frequency of 0.137 MHz, and a supply of 1 V.

An ADC can be reused in different systems with different reference driver networks. This implies that the values of R_o and C_{dec} (as shown in Fig. 3a) can be different as well. The simulated SNDR with various N_c and N_d settings is shown in Fig. 9. When $R_o \leq$ 2 kΩ and C_{dec} = 2 pF, the optimal choice of N_c is around the 4^{th} bit. When R_o is larger, N_c = 5 works slightly better. For N_d settings, the longer the delay is, the better the performance is. However, a longer delay also means more power consumption and a longer conversion time. In this design, the combination of N_c = 4 and N_d = 1 achieves a good compromise between performance and limited loss of conversion time. When the reference driving network is strong enough, the reconfigurable delay can be disabled.

Fig. 10a shows the simulated SNDR as a function of the decoupling capacitance for the 5 designs. With an R_o of 2 kΩ, a 32 pF decoupling capacitance is required to achieve an SNDR of 61 dB for the original design, which is near the ideal SNDR of a 10-bit ADC. If the decoupling capacitance is reduced to 2 pF, to save chip area, the SNDR of the original ADC reduces to 52 dB. With only redundancy or only reconfigurable delay, this can be improved to 55.5 dB, while if they are both applied, the SNDR is recovered to 59.2 dB. A similar performance can be achieved by adding sufficient delay to all bit-cycles, but this degrades the overall conversion time unnecessarily.

Fig. 10b shows the simulated SNDR as a function of R_o when C_{dec} is 2 pF. As can be seen, all versions of the ADC design will have a degrading performance when R_o increases, because the amount of delay or redundancy is not sufficient to fully counteract the reference voltage drop. However, the ADC

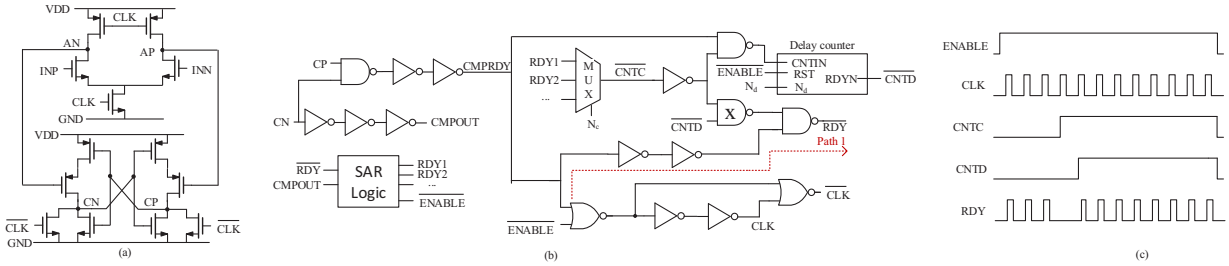


Fig. 8: Comparator (a) with reconfigurable delay (b) and timing diagram (c).

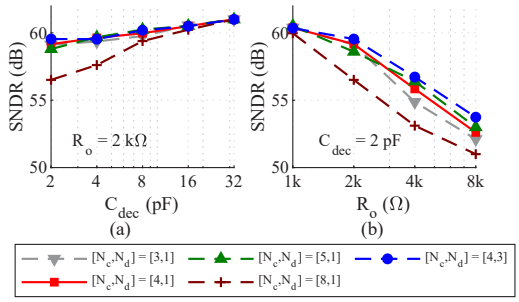


Fig. 9: Simulated SNDR with various settings, as function of C_{dec} (a) and as function of R_o (b).

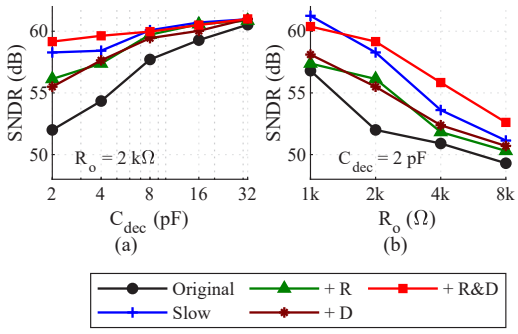


Fig. 10: Simulated SNDR for 5 ADC versions, as function of C_{dec} (a) and as function of R_o (b).

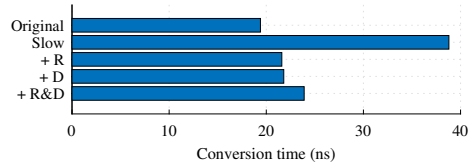


Fig. 11: Simulated conversion time for the 5 versions of the ADC design.

with the proposed techniques still maintains the best performance. With additional delay (increasing N_d) and additional redundancy, the performance for higher values of R_o could be further enhanced.

Fig. 11 shows the simulated typical conversion time. When redundancy or reconfigurable delay is used, the conversion time increases by around 11%. When both techniques are adopted, the conversion time increases by 23%. For the ADC with longer loop delay, the conversion time is increased

TABLE I: Performance summary and comparison

	[2][1]	[3][1]	[10][1]	This work[2]
Technology (nm)	20	65	40	65
Area (mm^2)	0.0012	0.074	0.023	0.002
Supply voltage (V)	0.9	1/0.8	1.2	1
Resolution (bit)	10	10	10	10
Sample rate (MS/s)	320	20	120	10
R_o (kΩ)	-	-	-	2
Decoupling Capacitor (pF)	-	20	3	2
Power (mW)	1.52	0.15	.12	0.032
SNDR (dB)	56.8	56.8	57.5	59.2
SFDR (dB)	74.8	72.4	76.1	71.2
FOM_W(fJ/conv.step) [3]	16.5	13.3	20.5	4.3

[1] Area excluding decoupling capacitors, measured results.
[2] Area including decoupling capacitors, simulated SNDR/SFDR, estimated power from an existing design.
[3] $FOM_W = Power/(2^{ENOB} \cdot f_s)$

by 100%. Thus, overall, the proposed technique using reconfigurable delay and redundancy offers a similar SNDR performance as the ADC with longer loop delay, but it has a far smaller penalty on conversion time and thus enables higher speed of operation.

Table I summarizes the simulated performance of this work and compares it with state-of-the-art designs. When reconfigurable delay and redundancy are enabled, a relatively small C_{dec} of only 2 pF is sufficient to maintain an SNDR of 59.2 dB, resulting in a good power-efficiency of 4.3fJ/conversion-step with a small chip area including decoupling capacitors.

V. Conclusions

In this paper, a reconfigurable delay and redundancy technique was added to a SAR ADC, to make the performance less dependent on the quality of the reference. As shown with a simulated design example, the proposed technique enables a reduction of the decoupling capacitance by 16× or an increase in reference output impedance by 4×, while maintaining good SNDR. As a result, area or power in the reference driver can be saved, which is often the bottleneck in systems that combine reference generation with an ADC. Further, compared to increasing the overall delay of the ADC, the proposed method has a much lower penalty on overall conversion time since it applies delay selectively. Compared to prior-art, this 10-bit ADC design achieves a good power efficiency (4.3fJ/conversion-step) and area (0.002 mm^2) while offering a simple approach to relax the reference requirements.

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