A 77.3-dB SNDR 62.5-kHz Bandwidth Continuous-Time Noise-Shaping SAR ADC With Duty-Cycled G_m-C Integrator

A 77.3-dB SNDR 62.5-kHz Bandwidth Continuous-Time Noise-Shaping SAR ADC With Duty-Cycled G_m-C Integrator

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***Abstract*—This paper presents a first-order continuous-time (CT) noise-shaping successive-approximation-register (NS-SAR) analog-to-digital converter (ADC). Different from other NS-SAR ADCs in literature, which are discrete-time (DT), this ADC utilizes a continuous-time G_m-C integrator to realize an inherent anti-aliasing function. To cope with the timing conflict between the DT SAR ADC and the CT integrator, the sampling switch of the SAR ADC is removed, and the integrator is duty cycled to leave 5% of the sampling clock period for the SAR conversion. Redundancy is added to track the varying ADC input due to the absence of the sampling switch. A theoretical analysis shows that the 5% duty-cycling has negligible effects on the signal transfer function and the noise transfer function. The output swing and linearity requirements for the integrator are also relaxed thanks to the inherent feedforward path in the NS-SAR ADC architecture. Fabricated in 65 nm CMOS, the prototype achieves 77.3 dB peak SNDR in a 62.5 kHz bandwidth while consuming 13.5 μW, leading to a Schreier FoM of 174.0 dB. Moreover, it provides 15 dB attenuation in the alias band.**

***Index Terms*—Continuous time, noise-shaping SAR ADC, anti-aliasing, duty-cycled integrator, current steering.**

I. Introduction

THE combination of successive-approximation-register (SAR) and $\Delta\Sigma$ analog-to-digital converter (ADC) architectures has gained popularity in recent years as a promising solution to realize low-power and high-resolution ADCs. This hybrid SAR-$\Delta\Sigma$ architecture optimizes the trade-off between power and resolution by leveraging the binary search algorithm from the SAR conversion and the noise-shaping function from the $\Delta\Sigma$ modulator.

Three mainstream SAR-$\Delta\Sigma$ hybrid architectures have been discussed in prior works: SAR-assisted $\Delta\Sigma$ ADC ($\Delta\Sigma$ ADC with a SAR quantizer) [1], zoom ADC [2] and noise-shaping (NS) SAR ADC [3]. It is known that a conventional $\Delta\Sigma$ ADC can be implemented either as a discrete-time (DT) ADC to achieve sampling frequency scalability, or as a continuous-time (CT) ADC to ease the driver design and to achieve an inherent anti-aliasing function [4]. Therefore, one could also expect both DT and CT realizations for hybrid SAR-$\Delta\Sigma$ architectures. For SAR-assisted $\Delta\Sigma$ ADCs and zoom ADCs, both DT and CT designs have been investigated [5]–[8]. However, in the NS-SAR ADC realm, only DT designs have been presented in literature. Therefore, this paper aims to extend the concept of the NS-SAR ADC to the CT domain and provide a prototype circuit realization.

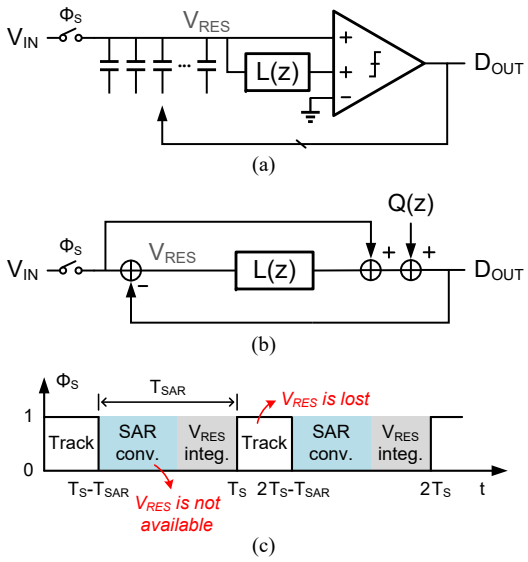

Fig. 1. (a) Block diagram, (b) signal diagram and (c) timing diagram of a DT NS-SAR ADC.

Fig. 1 shows the diagram of a typical DT NS-SAR ADC [3]. Its basic operation principle is as follows: After the SAR conversion finishes, the residue voltage V_{RES} is directly available at the output of the capacitive digital-to-analog converter (DAC). This residue voltage is then integrated by the loop filter $L(z)$ and added to the next ADC input in front of the comparator. In this way, the quantization noise and comparator noise contained in V_{RES} are shaped out of band by using a low-pass filter $L(z)$.

The noise-shaping principle in the NS-SAR ADC is the same as that in the $\Delta\Sigma$ ADC, but the hardware implementation is different. These differences can be observed by a closer examination of Fig. 1. First, only *one* DAC is present in the whole ADC. It acts as the binary-scaled reference-generation DAC in the SAR conversion, as well as the negative-feedback DAC to the first integrator in the $\Delta\Sigma$ noise-shaping loop. From this perspective, the NS-SAR ADC is hardware efficient by reusing the DAC for two purposes. Second, there exists a feed-

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forward path from the overall ADC input to the comparator input. This is a natural result from the DAC reuse, because this path is needed to conduct the normal SAR quantization and cannot be changed by the loop filter. This feedforward path guarantees that the in-band signal transfer function (STF) is always 1, and it does not alter the noise transfer function (NTF). These two features, the DAC reuse and the input feedforward path, distinguish the NS-SAR ADC from other hybrid SAR-$\Delta\Sigma$ architectures.

During the development of NS-SAR ADCs in the last decade, most research has focused on the optimization of DT NS-SAR ADC performance, such as lower power, higher bandwidth and smaller area. For example, open-loop [9] and closed-loop [10] dynamic amplifiers were proposed to reduce the analog power. High-order noise-shaping became favorable to reduce the oversampling ratio (OSR) and thus save digital power [11]. Time-interleaved [12], [13] and bandpass [14] NS-SAR ADCs were developed to increase or configure their bandwidth. Sampling noise cancellation [15] and mismatch error shaping techniques [16] were applied to reduce the DAC size and DAC power. However, these designs were all based on DT operation, while CT NS-SAR ADCs remained unexplored. Reference [17] has shown a CT $\Delta\Sigma$ ADC with a DT NS-SAR quantizer, but this cannot be categorized as a CT NS-SAR ADC because it still contains more than one DAC. This paper explores the possibility to apply CT operation to the NS-SAR architecture and proposes the first CT NS-SAR ADC.

This article is an extension of [18], and it is organized as follows: Section II presents the CT NS-SAR ADC architecture. Section III details its circuit implementation. Section IV shows the measurement results, and Section V draws conclusions.

II. CT NS-SAR Architecture

This section first explains the challenges of configuring an NS-SAR ADC as a CT converter. Then, the corresponding solutions are proposed, and the theoretical NTF and STF expressions are derived.

A. Overview

We encounter two problems when replacing the DT loop filter in Fig. 1(a) with a CT loop filter. First, the residue voltage V_{RES} is not available during the binary search process, nor is it available during the tracking phase, which interrupts the desired CT integration. As indicated in Fig. 1(c), both aspects lead to intermittently available V_{RES} information and make the continuous residue integration impossible. Second, to act as an anti-aliasing filter, the filter should occur prior to the input sampling moment rather than afterwards. While a DT NS-SAR ADC could address the first issue with adjusted timing, it cannot solve the second challenge as it is inherently operating on sampled data.

In this section, two techniques are proposed to solve these problems. First, the loop filter is duty cycled to leave enough time for the SAR quantization without significantly degrading the noise-shaping function. Second, the sampling switch of the SAR ADC is replaced by an ac-coupling capacitor to keep the residue information available in the tracking phase and to make sure the loop filter is applied to the CT input signal.

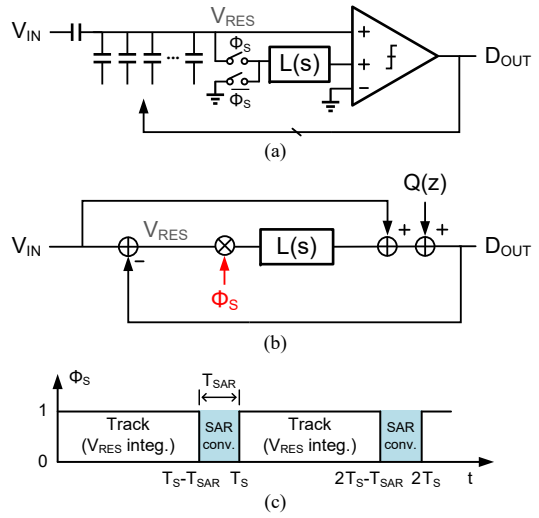

Fig. 2. (a) Block diagram, (b) signal diagram and (c) timing diagram of the proposed CT NS-SAR ADC.

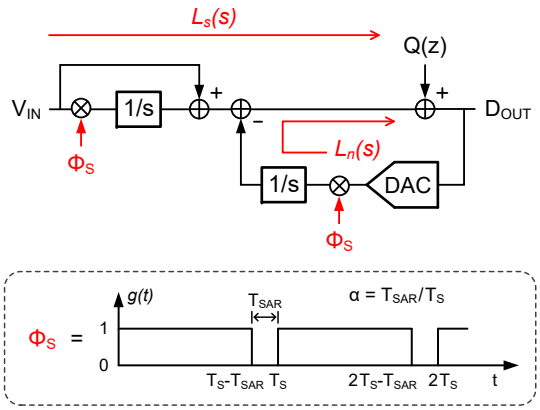

Fig. 3. Signal diagram of the first-order CT NS-SAR ADC.

Fig. 2(a) shows the block diagram of the proposed CT NS-SAR ADC. The duty-cycling of the loop filter is realized by inserting enable switches between the DAC output and the integrator input. The switches are controlled by the two-phase non-overlapping clocks Φ_{S} and $\overline{\Phi_{\mathrm{S}}}$. Its equivalent signal diagram is shown in Fig. 2(b), where the duty-cycling operation of the integrator is modeled as the clock signal Φ_{S} multiplying the loop filter input. When Φ_{S} is high, the residue voltage V_{RES} is integrated by the loop filter $L(s)$. In the other phase, when $\overline{\Phi_{\mathrm{S}}}$ is high, the integration stops, and the SAR quantization takes over, as indicated in Fig. 2(c). If the SAR conversion time T_{SAR} only occupies a small fraction of the clock period T_{S}, the effect of duty-cycling on the loop filter function is minimal, as will be explained later.

Compared to the DT NS-SAR ADC from Fig. 1, there is no sampling action on the DAC output, so that V_{RES} can be kept, and the integration can continue. This configuration is similar to the first stage of the CT two-step SAR ADC [19]. To deal with the changing ADC input, redundancy is needed

in the DAC, which will be further explained in Section III. Note that the diagram shown in Fig. 2 has a single feedback DAC and an embedded feedforward path, so it complies with the characteristics of the NS-SAR ADC mentioned in Section I, and that is basically why it can be named as a CT NS-SAR ADC.

B. NTF and STF Analysis

The introduction of the duty-cycling mode changes the behavior of the loop filter. Therefore, its impact on the NTF and STF needs to be examined. We define the duty-cycle rate α as the ratio between the SAR conversion time T_{SAR} and the sampling period T_{S} in Fig. 2(c) to simplify the following calculation, namely,

$$\alpha = \frac{T_{\mathrm{SAR}}}{T_{\mathrm{S}}}. \tag{1}$$

If α is 0, the CT NS-SAR ADC becomes an ideal CT $\Delta\Sigma$ ADC with a feedforward path from the input to the quantizer. For simplicity, only a first-order CT NS-SAR ADC is covered in this paper, but CT NS-SAR ADCs with higher-order loop filters can also be analyzed in the same way. Further, the effect of ac coupling is ignored in the analysis, as it only impacts near-dc frequencies. To avoid scaling factors in the loop filter expression $L(s)$, the ADC is assumed to operate at 1 Hz sampling rate, so that the first-order loop filter $L(s)$ can be directly written as:

$$L(s) = \frac{1}{s}. \tag{2}$$

To calculate the NTF, we need to obtain the actual loop filter function seen from the DAC output to the quantizer input, denoted as $L_n(s)$ in Fig. 3. Since the DAC output is a constant after each SAR conversion, the duty-cycling of the integrator merely appears as an attenuation factor $(1-\alpha)$. Therefore, $L_n(s)$ is simply:

$$L_n(s) = \frac{1-\alpha}{s}, \tag{3}$$

and the NTF can be calculated as:

$$\mathrm{NTF}(s) = \frac{1}{1+L_n(s)}. \tag{4}$$

Its equivalent z-domain expression is:

$$\mathrm{NTF}(z) = \frac{1-z^{-1}}{1-\alpha z^{-1}}. \tag{5}$$

The NTF curves with different α values are plotted in Fig. 4. It can be observed that the duty-cycling plays the same role as the RC time-constant variation in a CT $\Delta\Sigma$ ADC. Higher α (longer SAR conversion time) leads to a higher in-band magnitude and lower out-of-band gain, and vice versa. Note that this duty-cycling operation of the integrator does not cause an excess loop delay problem that one may encounter in a CT $\Delta\Sigma$ ADC, thus the stability of the modulator is not harmed.

Due to the existence of the clock function $g(t)$ in Fig. 3, the modulator becomes a linear periodically time-varying system. Therefore, the nulls located at multiples of the sampling frequency (f_s) in the STF of a typical CT $\Delta\Sigma$ ADC are expected to disappear [20]. The STF in this architecture can

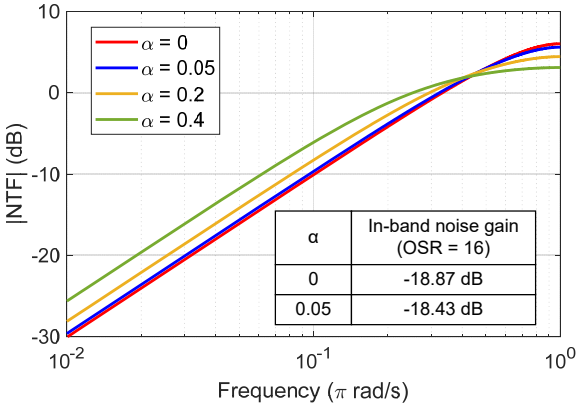

Fig. 4. NTF magnitudes with different α values.

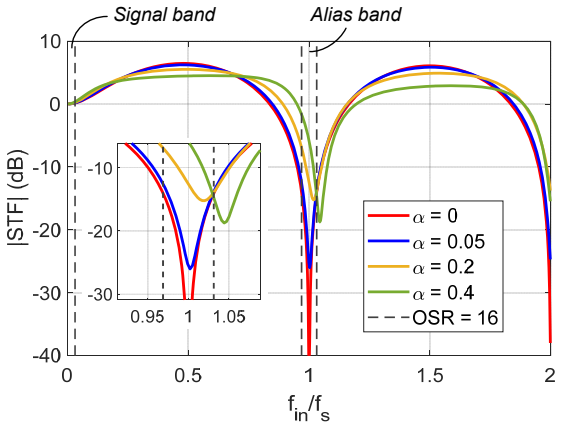

Fig. 5. STF magnitudes with different α values.

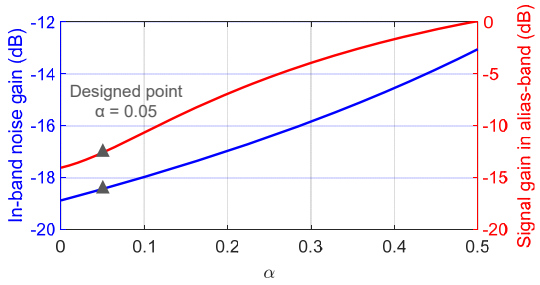

Fig. 6. In-band noise gain and alias-band signal gain with different α values when OSR is 16.

be derived as the product of two transfer functions: the loop filter function seen from the input to the quantizer, denoted as $L_s(s)$, and the transfer function from the quantizer to the ADC output, which is simply the NTF. The function $L_s(s)$ is calculated as:

$$\begin{aligned} L_s(s) &= \mathcal{L}\{g(t)\} \cdot L(s) + 1 \\ &= \frac{1}{s}\left(\frac{1}{1-e^{-s}}\right)\left[1-e^{-s(1-\alpha)}\right] + 1. \end{aligned} \tag{6}$$

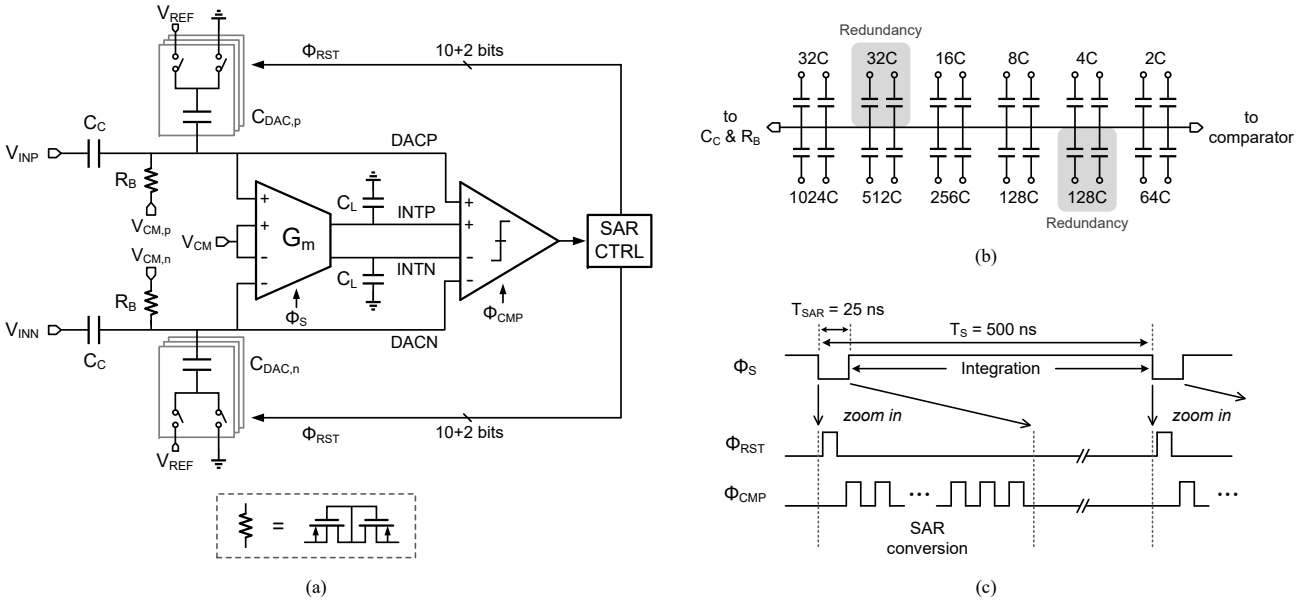

Fig. 7. (a) Proposed first-order CT NS-SAR ADC. (b) DAC implementation. (c) Timing diagram.

The STF is then obtained by multiplying (5) and (6):

$$\mathrm{STF}(f) = \frac{1-e^{-j2\pi f}}{1-\alpha e^{-j2\pi f}} \cdot \left[\frac{1}{j2\pi f}\frac{1}{1-e^{-j2\pi f}}\left(1-e^{-j2\pi f(1-\alpha)}\right)+1\right]. \tag{7}$$

The STF amplitudes with different α values are shown in Fig. 5. As expected, the STF suppression at multiples of f_s is reduced. The out-of-band peaking is caused by a zero in the loop transfer function, which is introduced by the input feedforward path. This indicates that a large blocker signal may saturate the ADC. However, as a first-order system, the modulator will recover after the blocker signal is removed.

Fig. 6 shows the effect of different duty cycles on the in-band noise attenuation and aliasing suppression. Note that $\alpha = 0$ coincides with a CT design. As can be seen, by choosing a small α value, the in-band noise gain is hardly affected, and the inherent anti-aliasing benefit from the CT integration is also well preserved. Since the loop filter is only first order, the OSR is chosen to be 16, a relatively high value to reduce the in-band noise. The α value is chosen as 5% as a compromise between NTF/STF performance and SAR conversion speed. First, with a 5% duty-cycle rate, the in-band noise increases by 0.44 dB, and the anti-aliasing suppression degrades by 1.5 dB compared to a true CT implementation, which are both minor degradations. With a higher α value, these degradations will gradually increase. Second, since the SAR conversion must be completed within 5% of the clock period, the conversion process has to be 10× faster as compared to a SAR converter operating at the same sampling rate, but with a 50% duty-cycle. Therefore, choosing a low α value requires speeding up the comparator, DAC settling and logic, which ultimately comes at the cost of increased power consumption. In this work, the SAR conversion time is dominated by the comparator speed. Since the sampling rate is relatively low (2 MHz), an α value of 5% is still achievable for the SAR conversion. To relax the SAR ADC design, it is attractive to increase α, at the cost of degraded NTF and STF performance. It should further be noted that a larger α value implies that more DAC redundancy is needed to avoid conversion errors due to the non-sampled input [19].

III. Circuit Implementation

As a proof of concept, a 10-bit first-order CT NS-SAR ADC is built, as shown in Fig. 7. The input signal is ac coupled to the comparator input by C_C without using a sampling switch. A large resistor R_B is used to provide the dc bias for the DAC output. It is implemented with pseudo-resistors to achieve high resistance. The bias resistor R_B, together with the capacitors C_C and $C_{\mathrm{DAC,p(n)}}$, forms a high-pass filter (HPF) at the input, so this ADC is only capable of processing ac signals while blocking the dc information [19]. To minimize the in-band noise contribution of R_B, the high-pass corner is typically designed well under the bandwidth of interest. Targeting a bandwidth from 60 Hz up to 62.5 kHz in this prototype, the nominal high-pass corner frequency is thus designed for 10 Hz, which leads to a value of 4 GΩ for R_B given that C_C and $C_{\mathrm{DAC,p(n)}}$ are equal to 2 pF. As R_B is a pseudo resistor, it has a large variation (of about 400×) under different process corners with a temperature range from 0 °C to 80 °C. While R_B cannot be tuned in this prototype, manual tuning or PVT compensation techniques [21] could be used to minimize this spread. By choosing C_C equal to $C_{\mathrm{DAC,p(n)}}$, the input signal and the reference voltage are both attenuated by half, so that the input signal range does not change. The proposed ADC is controlled by asynchronous logic. The ADC sampling frequency is 2 MHz providing an OSR of 16. After the SAR conversion starts (Φ_S is low), the DAC is first reset by Φ_RST, and then the ADC performs the binary search quantization. With 5% duty cycle, the time reserved for the SAR conversion

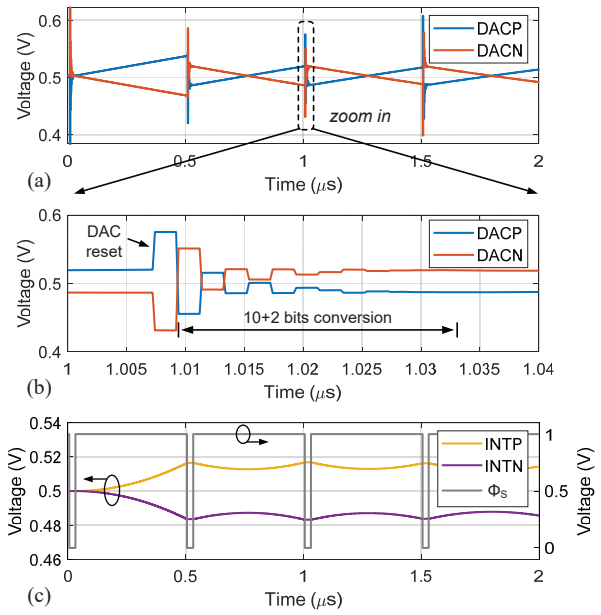

Fig. 8. Time-domain waveform of the signals: (a) DAC outputs, (b) DAC outputs in one SAR conversion period, and (c) integrator outputs.

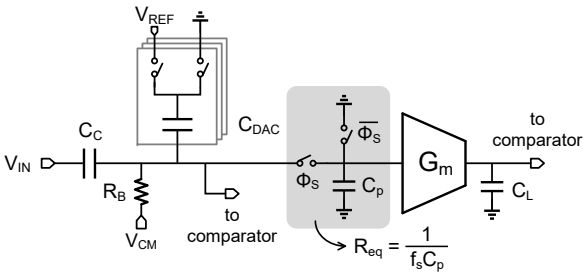

Fig. 9. Illustration of the effect of the integrator input parasitic capacitor. A single-ended diagram is shown for simplicity.

(including DAC reset) is 25 ns. A simplified time-domain waveform from a behavioral model is shown in Fig. 8. When Φ_S is high, the DAC tracks the sine-wave input signal (via ac coupling) and the integrator integrates this function. When Φ_S is low, a SAR conversion takes place and the integration is paused. The design of the key blocks in this ADC will be elaborated in this section.

A. Integrator

Thanks to the DAC reuse in the NS-SAR architecture, there is no explicit resistive or current feedback DAC needed as in a CT $\Delta\Sigma$ ADC. Since the loop filter only processes a relatively small SAR residue signal, it can be implemented by an open-loop G_m-C integrator. Fig. 9 shows a straightforward circuit implementation according to Fig. 2(a). However, this direct solution suffers from several adverse effects brought by the integrator input capacitance C_p. First, it introduces undesired charge sharing between C_p and C_{DAC} when Φ_S goes high, making V_{RES} inaccurate. Second, C_p causes different attenuation factors for the input signal in different phases. When C_p is connected to C_C and C_{DAC}, V_{IN} is attenuated by $C_C/(C_C + C_{DAC} + C_p)$. When C_p is disconnected, this

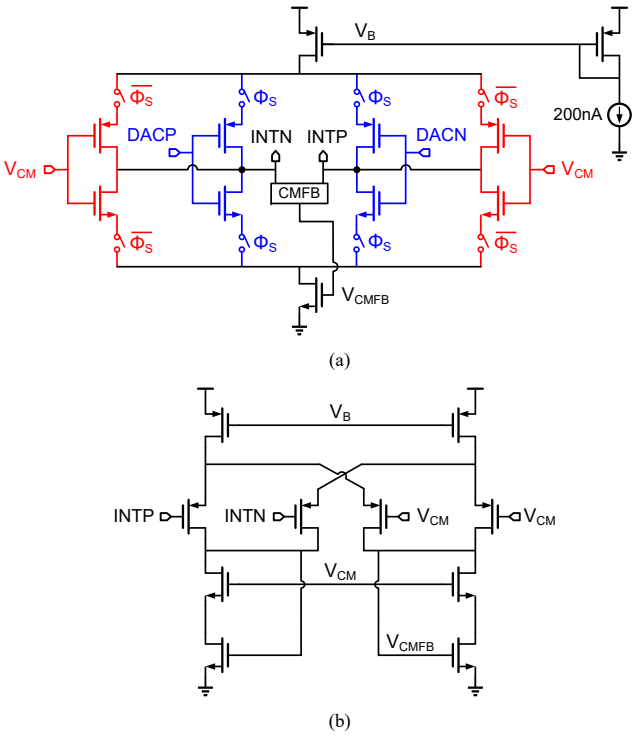

Fig. 10. (a) Duty-cycled integrator and (b) its CMFB circuit.

attenuation factor becomes $C_C/(C_C + C_{DAC})$. Third, the input parasitic C_p together with the two-phase clocks Φ_S and $\overline{\Phi_S}$ constitutes a switched-capacitor network, which is equivalent to a resistor R_{eq} of $1/f_sC_p$. Suppose C_p is 5 fF, at a 2 MHz sampling rate, the equivalent resistance R_{eq} is 100 MΩ. This R_{eq} is much smaller than the pseudo-resistor R_B, which is typically a few GΩ. This small R_{eq} together with C_C and C_{DAC} forms a high-pass filter whose corner frequency may fall in the signal band. Therefore, the loop filter $L(s)$ is no longer a low-pass filter, but a band-pass filter considering the effect of C_p, which degrades the noise shaping performance in the low frequency region.

To avoid these problems, this work adopts a duty-cycled integrator with two input branches, as shown in Fig. 10. The switches are moved inside the integrator. The two inverter-based input pairs are enabled in a current-steering manner. During the SAR conversion phase, the red branches with V_{CM} inputs are enabled to stop the integration. In the tracking phase, the blue branches connected to the DAC are activated and the integration resumes. The common-mode feedback (CMFB) circuitry is the same as in [22]. Because the integrator input only contains the residue voltage, its maximum differential output swing is limited to ±20 mV in this design. This greatly relaxes the output swing and linearity requirements for the integrator. The load capacitance is 2.25 pF per side to satisfy the noise requirement. The nominal transconductance is 4.5 μS with a total bias current of 200 nA.

B. DAC and Comparator

A split switching scheme is used in the DAC array, where each bit is composed of two identical capacitors [23], as

TABLE I
DAC STRUCTURE WITH DWA

Bit weight	512	256	128	64		64R*	
Method	DWA (group 1)						
Bit weight	32	16	16R*	8	4	2	1
Method	DWA (group 2)			No DWA			

* 'R' stands for redundancy.

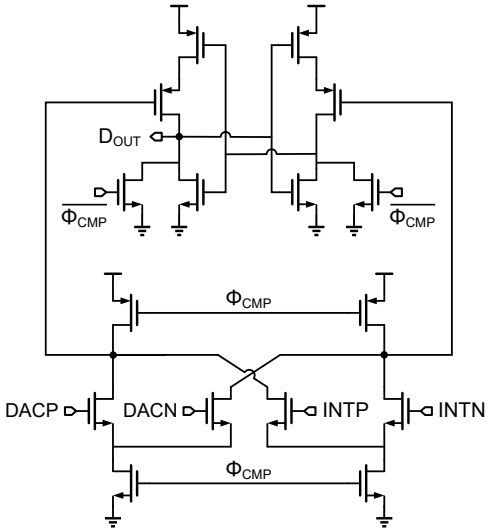

Fig. 11. Comparator with two input pairs.

shown in Fig. 7(b). The unit capacitor C is 1 fF, and the total capacitance per side $C_{\mathrm{DAC,p(n)}}$ is 2 pF. Two redundancy bits (128C and 32C) are added to avoid conversion errors due to the non-sampled input [19]. Due to the absence of sampling, the mismatch error shaping techniques as used in prior DT NS-SAR ADCs [24], [25] are not applicable here. Instead, segmented data weighted averaging (DWA) is applied to the first 5 most significant bits (MSBs) and 3 middle bits to improve the DAC linearity, as illustrated in Table I. However, the capacitor mismatch between different DWA groups and the mismatch from the least significant bit (LSB) capacitors can still limit the final performance.

Fig. 11 shows the comparator which has two input pairs to sum the ADC input with the integrated residue. Two separate current tails are used in the first stage to better accommodate for any common-mode mismatch between the two input paths [26].

C. Offset Calibration

Unlike conventional CT $\Delta\Sigma$ ADCs, the offset errors from the comparator and integrator in this architecture can be detrimental to the ADC performance. As illustrated in Fig. 12, when offsets are considered in the SAR conversion, the DAC output will not converge to V_{CM} at the end of the conversion. Instead, the differential DAC output will deviate by V_{os}, where V_{os} is the total offset from the comparator and the integrator. This final convergence voltage is no longer the same as the desired dc bias voltage V_{CM}, which causes non-zero average

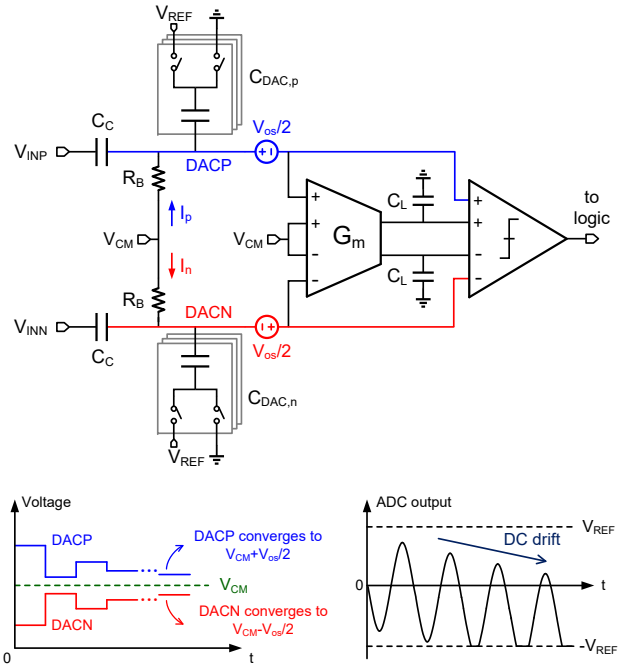

Fig. 12. Illustration of the effects caused by comparator and integrator offsets.

currents flowing from the V_{CM} bias to the DAC on each side, namely, $\overline{I_p} \neq 0$ and $\overline{I_n} \neq 0$. Due to this undesired charging (or discharging) current, a differential error voltage is equivalently added to the ADC input. This error causes a dc drift in the ADC output code, and may finally saturate the converter over time.

In this work, a manual offset calibration is carried out by using two separate bias voltages [$V_{\mathrm{CM,p}}$ and $V_{\mathrm{CM,n}}$ in Fig. 7(a)] to compensate for the offsets, instead of directly calibrating the offsets from the individual blocks. By observing the direction of the dc drift in the output code, one of the two bias voltages is tuned higher or lower until the dc drift becomes negligible. This method works as a temporary solution, while the chopping scheme used in [27] and [28] could be considered as a more viable approach to completely solve this problem.

D. Noise Analysis

The simulated in-band noise contributors are listed in Table II, all referred to the V_{RES} node [Fig. 2(a)]. Since the input signal and the reference voltage are both attenuated by 2× due to the ac-coupled input network, the equivalent signal power and quantization noise power at the V_{RES} node are reduced by 4×. The quantization noise and comparator noise are both noise-shaped, resulting in an in-band noise suppression of -18.43 dB as shown in Fig. 4, on top of the 12 dB improvement thanks to 16× oversampling. The integrator noise is calculated by integrating its noise over the bandwidth of interest (from 60 Hz to 62.5 kHz). Simulation results show that 80% of the in-band integrator noise is flicker noise, while 20% is thermal noise. The bias resistor R_{B} also contributes noise with a noise transfer function of $1/[1 + sR_{\mathrm{B}}(C_{\mathrm{C}} + C_{\mathrm{DAC}})]$. Therefore, the R_{B} noise power can be obtained by integrating its noise power spectral density ($= 4kTR_{\mathrm{B}}$) with the square of the noise

TABLE II
NOISE BREAKDOWN

Specification	Simulation result	Measurement result
Quantization noise	7.1×10^{-11} V^2	N.A.
Comparator noise	2.9×10^{-10} V^2	N.A.
Integrator noise	3.0×10^{-10} V^2	N.A.
Bias resistor R_B noise	2.1×10^{-10} V^2	N.A.
Total noise	8.7×10^{-10} V^2	1.4×10^{-9} V^2
SNR	81.6 dB	79.4 dB

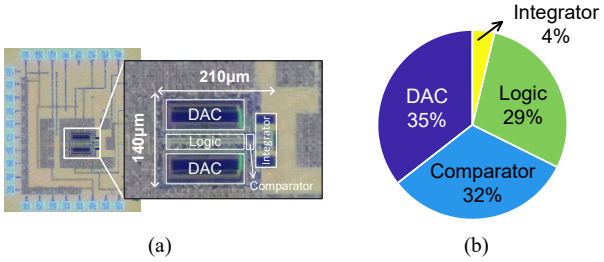

Fig. 13. (a) Die photo. (b) Power breakdown.

transfer function from 60 Hz to 62.5 kHz. With a full scale 2 V_{pp} input signal, the theoretical signal-to-noise-ratio (SNR) is 81.6 dB.

IV. Measurement Results

The prototype is fabricated in a 65 nm CMOS technology. The offset calibration is performed off-chip, and the 200 nA bias current for the integrator is provided off-chip. The power supply is 1 V, and the power consumption is 13.5 μW (including the 200 nA external bias current) at 2 MS/s sampling rate and an OSR of 16×. Fig. 13(a) shows the die photo where the DAC occupies approximately 41% of the total area, and the G_m-C integrator occupies 17%. The power breakdown in Fig. 13(b) indicates that DAC, comparator and logic have similar contributions to the overall consumption, while the integrator consumption of 4% is negligible.

Fig. 14 shows the measurement setup. A DS360 low-distortion signal generator together with a passive low-pass filter is used to provide the sinusoidal input signal for the ADC. An 81134A clock generator provides the sampling clock Φ_S. The ADC output data is stored on a FPGA and processed by MATLAB. The ADC settings are also configured via the FPGA. Another 33500B waveform generator is used to provide input signals up to 4 MHz for the STF measurement. The low-pass filter is removed in the STF measurement to avoid any signal attenuation from the filter.

Fig. 15 shows the measured spectra without and with DWA, with a 2.5 kHz input signal after offset calibration. Each spectrum uses a 2^{15}-point FFT with a Hanning window, and is averaged over 12 runs. When DWA is enabled, the measured SNR is 79.4 dB, the signal to noise and distortion ratio (SNDR) is 77.3 dB, and the spurious free dynamic range (SFDR) is 86.0 dB. From the measured SNR, the total noise power is calculated and listed in Table II. As can be seen, the

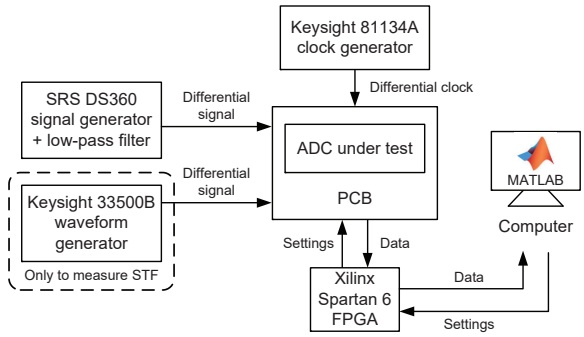

Fig. 14. Measurement setup.

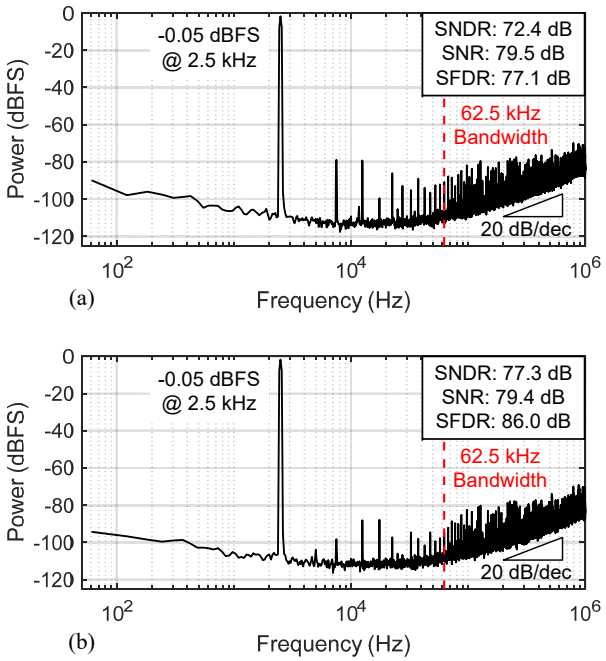

Fig. 15. Measured spectrum (a) without DWA and (b) with DWA.

measured noise power is about 2 dB higher than the expected value. This noise performance difference could be caused by the following factors: first, some noise sources which were ignored in the simulation, such as supply noise, external noise sources, etc. Second, the pseudo-resistors R_B might have a lower resistance due to process variations, which would result in more in-band noise.

As can be seen from Fig. 16, the SNDR and SFDR remain above 75 dB and 85 dB, respectively, in the whole 62.5 kHz signal band, while the dynamic range is 80 dB. Fig. 17 shows the measured performance when the off-chip integrator bias current is varied by ±15%. The SNR variation is within 1.5 dB and the SNDR variation is within 1.0 dB. The bias current determines the G_m value, which in turn defines the NTF and integrator noise level. However, since the total noise is dominated by the sum of integrator flicker noise and R_B thermal noise, the final SNR is only mildly affected by G_m, and accurate G_m tuning is not required in this design. Fig. 18 (a) shows the measured performance at different supply and common-mode voltages, and Fig. 18 (b) shows the post-layout

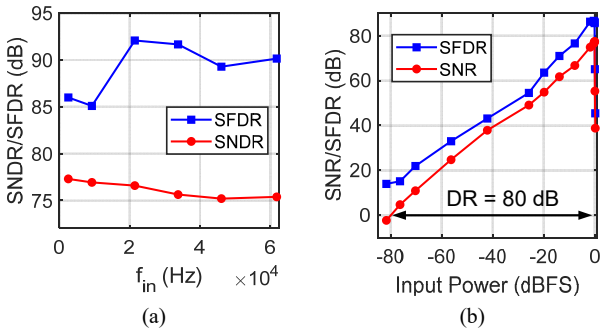

Fig. 16. Measured performance over (a) different input frequencies and (b) different input amplitudes.

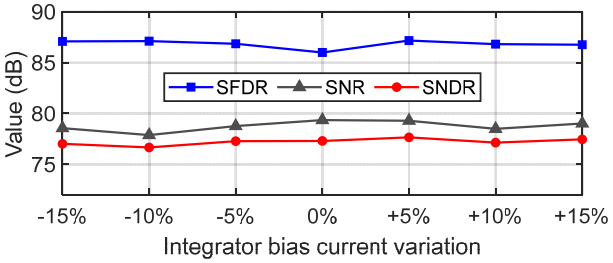

Fig. 17. Measured performance with different integrator bias currents.

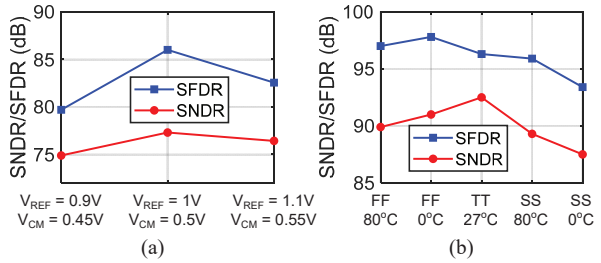

Fig. 18. (a) Measured performance over voltage corners. (b) Simulated performance (without circuit noise) over process and temperature corners.

simulation results under different process and temperature corners without circuit noise. The duty-cycle rate is also adjusted from 5% to 12% in the SS corner to accommodate for the slower SAR conversion speed.

The STF is measured with a differential input signal amplitude of 200 mV_{pp}, and the measured STF is shown in Fig. 19. It matches well with the theoretical calculation from (7), and it achieves more than 15 dB suppression in the alias band. The 6 dB out-of-band peaking is caused by the inherent feedforward path in the NS-SAR architecture. Fig. 20 shows the simulated signal gain for input signals at $f_s/2$ and f_s. For small signals, this gain is constant, but the gain starts to deviate when the amplitude is increased. This indicates that the system starts to saturate. For instance for an input frequency near f_s, this happens for an amplitude of about 200 mV_{pp}.

Table III summarizes the performance of this work and benchmarks it with other state-of-the-art ADCs. In general, this design is easier to drive because it does not require a high peak driving current to charge the switched-capacitor input as in a DT NS-SAR ADC [11], and it provides inherent anti-aliasing. When compared to other CT ADC architectures, this

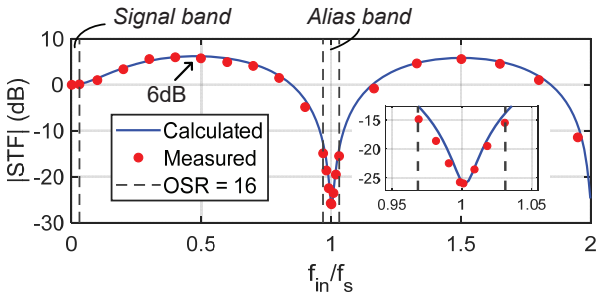

Fig. 19. Measured STF.

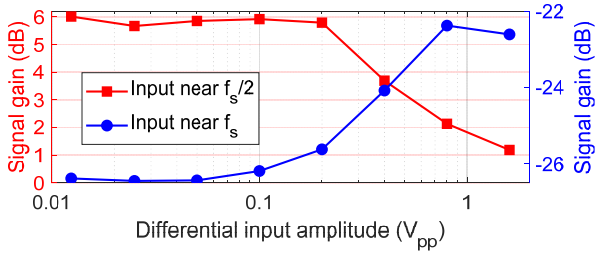

Fig. 20. Simulated signal gain versus different input amplitudes.

design features the following aspects: Compared to the CT two-step SAR ADC [19], this work achieves higher SNDR owing to the additional noise-shaping loop, but at the cost of lower bandwidth. The anti-aliasing function in [19] comes from the finite bandwidth of the inter-stage residue amplifier. However, the residue amplifier's bandwidth is typically a few times larger than the ADC bandwidth, which means the associated anti-aliasing effect is much milder. Compared to a CT $\Delta\Sigma$ ADC with a similar G_m-C integrator and SAR quantizer [29], this design avoids the power consumption and hardware cost from the resistive feedback DAC thanks to the DAC reuse in the NS-SAR architecture. Moreover, compared to another CT $\Delta\Sigma$ ADC [28] which has a similar ac coupled input network and G_m-C integrator, this design benefits from the inherent feedforward path in the NS-SAR diagram, and hence does not need an explicit feedforward amplifier as in [28] to reduce the integrator output swing.

V. Conclusion

This paper proposes the first CT NS-SAR ADC. By duty cycling the loop filter and removing the sampling switch, this design both provides implicit anti-aliasing and is easy to drive, as CT ADC architectures. A 5% duty-cycle rate is adopted to minimize its impact on the STF and NTF, and a current-steering G_m stage is proposed to maintain the signal accuracy at the DAC output. Thanks to these techniques, the ADC achieves 77.3 dB peak SNDR in a 62.5 kHz bandwidth with a 13.5 μW power consumption, while the anti-aliasing suppression is more than 15 dB. Even though this suppression is mild, it could relax the preceding anti-aliasing filter by about 1 order. Moreover, the proposed CT concept could be extended towards a higher order to achieve more substantial anti-aliasing.

TABLE III
BENCHMARK WITH OTHER WORKS

	ISSCC'20 [11]	ISSCC'19 [19]	VLSI'15 [29]	VLSI'18 [28]	This work
Technology	28 nm	40 nm	65 nm	180 nm	65 nm
Architecture	DT NS-SAR	CT two-step SAR	CT SAR-assisted $\Delta\Sigma$	CT SAR-assisted $\Delta\Sigma$	CT NS-SAR
Anti-aliasing	No	Yes	Yes	Yes	Yes
Supply (V)	1	0.7 / 1.1	1.1	1	1
Sampling frequency (MHz)	2	2	3.072	0.0128	2
Bandwidth (kHz)	100	1000	24	0.3	62.5
SAR resolution (bit)	8	13	5	5	10
Peak SNDR (dB)	87.6	73.5	85	84.3	77.3
SFDR (dB)	102.8	87.8	95[†]	104.7	86.0
Power (μW)	120	25.2	121	6.5	13.5
FoM_W (fJ/conv.-step)	30.6	3.3	173.4	807.9	18.0
FoM_S (dB)	176.8	179.5	168.0	160.9	174.0
Area (mm^2)	0.02	0.01	0.6	0.55	0.03

FoM_W = Power/($2^{ENOB}\times 2\times$Bandwidth) FoM_S = SNDR + $10\log_{10}$(Bandwidth/Power)

[†] Estimated from the measured spectrum in [29].

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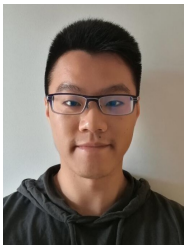

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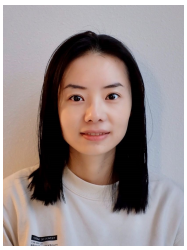

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